AN1544
APPLICATION NOTE

Designing an Application with ST10F269

This note brings advices in designing applications based on ST10F269. It includes six mains items which are:

- Information and recommendations in the use of external resonator with the on-chip oscillator,
- Details on start-up configuration and necessary precautions,
- Filtering, decoupling and special pins use,
- Recommendations to reduce ADC conversion errors,
- Memory interface,
- Interfacing with the L4969 CAN interface.

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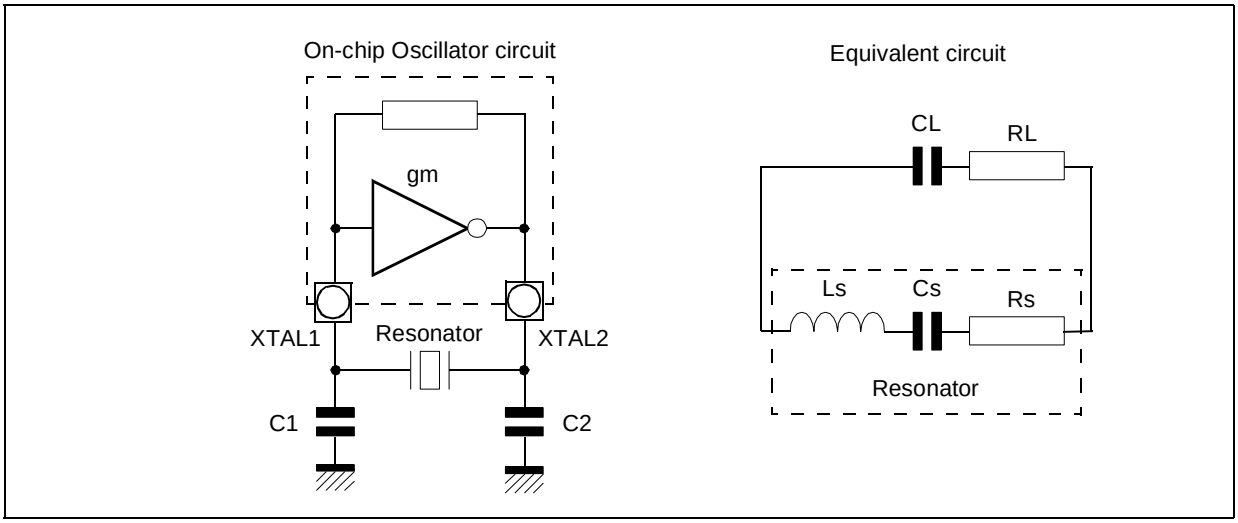
1 - OSCILLATOR

The ST10F269 can run with an external clock connected to XTAL1 input pin of the oscillator inverter or with a clock signal generated by a resonator connected to XTAL1 / XTAL2 pins. Refer to the ST10F269 datasheet for the possible combinations. This chapter provides with detailled information on the use of the on-chip oscillator in conjunction with an external resonator.

1.1 - Oscillator Characteristics

Using an external resonator (crystal or ceramic resonator) although simple to implement needs few basic precautions. Referring to the schematic of the on-chip oscillator (Figure 1), the key items are described in the following section.

Figure 1 ST10 Oscillator Equivalent Schematic



The resonator component can be a crystal or a ceramic resonator. It is represented as a series resonant branch Rs, Ls, Cs. The amplification ability of the oscillator inverter is replaced by a negative resistance RL and the capacicatance CL contains the C1, C2 load capacitances and the stray capacitance of the resonator .

The load capacitors C1 and C2 transform the gain of the amplifier (gm) into a negative series resistance RL to compensate for the losses of the crystal.

The best frequency stability is obtained when C1 = C2. The oscillation occurs when the sum of RL and Rs (the series resistance of the crystal) is negative.

By choosing C1 = C2 = C, the minimal gain of the amplifier (gm) is exressed as following:

$$gm_{min} = Rs \times C^2 \times \omega^2 = Rs \times C^2 \times (2 \times \pi \times f)^2$$

The minimal gain of the amplifier also implicitly sets the on-chip oscillator start-up time.

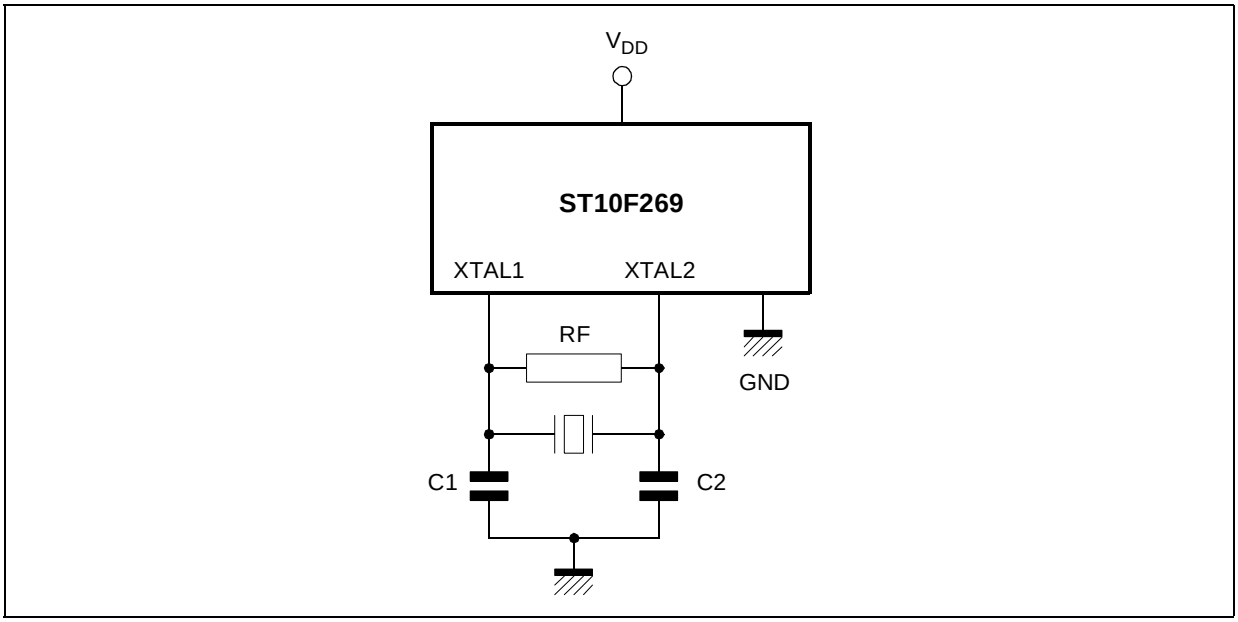
The minimum transconductance (gm) of the ST10F269 oscillator inverter is **5 mA/V** so the minimun series resistance value can be easily choosen in the crystal provider catalog.

The oscillation stability mainly depends on external parameters so only the transconductance (gm) can be guaranteed and the start-up time value will be defined by measurement at the application level.

1.2 - Recommanded Crystals / Ceramic Resonators

The Figure 2 shows the components to add to ST10F269 oscillator. The value of those components (C1, C2, RF) are given in the tables of recommanded crystals and ceramic resonators.

Figure 2 Additional Components to Use with External Resonator



1.2.1 - Murata Resonators

These are the recommanded ceramic resonators from Murata :

Frequency [Hz]	Type	Part Number	C1 [pF]	C2 [pF]	RF [Ω]
4.0 M	SMD	CSTCR4M00G15A( )-R0	(39)	(39)	Open
4.0 M	SMD	CSTCC4M00G16A( )-R0	(47)	(47)	Open
8.0 M	SMD	CSTCE8M00G15A( )-R0	(33)	(33)	Open
8.0 M	SMD	CSTCC8M00G16A( )-R0	(47)	(47)	Open
10 M	SMD	CSTCE10M0G15A( )-R0	(33)	(33)	Open
10 M	SMD	CSTCC10M0G16A( )-R0	(47)	(47)	Open
12 M	SMD	CSTCE12M0G15A( )-R0	(33)	(33)	Open
16 M	SMD	CSTCV16M0X11Q( )-R0	(5)	(5)	Open
22 M	SMD	CSTCV22M0X11Q( )-R0	(5)	(5)	Open
24 M	SMD	CSTCV24M0X11Q( )-R0	(5)	(5)	Open
40 M	SMD	CSTCV40M0X11Q( )-R0	(5)	(5)	Open

For each of the ceramic resonators, Murata analysed :

– Oscillating frequency versus temperature,

– Oscillator start-up time, oscillating frequency, oscillating voltage, versus ST10F269 external supply voltage,

– Correlation between Murata standard test conditions (using 74HCU04) and ST10F269.

The reports are available on request to Murata.

1.2.2 - AVX Ceramic Resonators

The analysis is pending with AVX. This document will be updated as soon results are available.

1.2.3 - NDK Crystals

The analysis is pending with NDK. This document will be updated as soon results are available.

1.3 - Start-up Time

Ceramic resonators have a much shorter start-up time than crystals (about 100 times faster) but have a lower accuracy on the frequency (initial tolerance, temperature variations, drift).

Depending on applications requirements and possiblities, users can choose between short oscillator start-up time and frequency accuracy.

From ST10 perspective, the worst case for the oscillator start-up time is high temperature and low voltage.

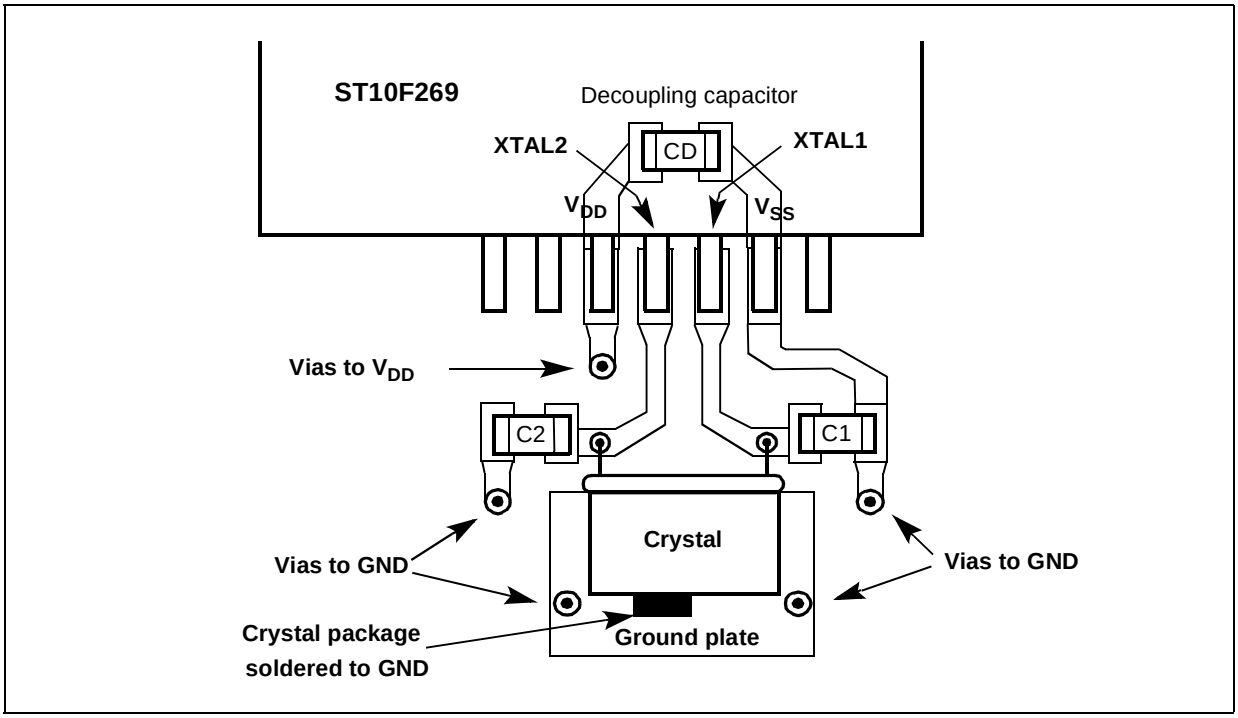
1.3.1 - Start-up Time Results

The measurements done by Murata on ST10F269 and ceramic resonators show start-up times in the 0.05ms range.

1.4 - PCB Layout for ST10F269 Oscillator

The following figure shows the proposed layout for ST10F269 oscillator.

Figure 3 Example of Layout fot External Crystal



1.5 - Oscillator and EMC

ST10F269/ST10F280 oscillator has an integrated gain control to minimize EMC and power consumption. This does not prevent users to check the following rules :

– Avoid other high frequency signals near the oscillator circuitry. These can influence the oscillator.

– Layout the ground supply on the basis of low impedance.

– Shield the crystal with an additional ground plane underneath the crystal.

– Do not layout sensitive signals near the oscillator. Analyze cross-talk between different layers.

– V_{SS} pin close to XTAL pins must be connected to the ground plane and decoupled to the closest V_{DD} pin.

– Capacitors shall be placed at both ends of the crystal, directly connected to the ground plane while keeping the overall loop as small as possible.

– Crystal package, when metalic, shall be directly connected to the ground.

2 - PORT0 START-UP CONFIGURATION

A reset sequence may be triggered by the following reasons:
– Hardware reset signal on pin $\overline{\text{RSTIN}}$ (Hardware reset input).
– Execution of the Software reset instruction SRST
– Overflow of the Watchdog Timer

After recognition of a reset the ST10F2xx will proceed with the actions listed below :
– Complete internal RAM write operation before the internal reset procedure begins
– Cancel pending internal hold states
– Abort external memory access cycles
– Wait 1024 TCL = 12.8us @ 40MHz to perform a complete reset sequence
– Start program execution from memory location 0000h in code segment 0

Note: Please refer to the datasheet and user's manual for reset event definitions.

2.1 - Port0

Pull-down resistors

Pull-down resistors shall be low enough so that Input voltage in P0.x is within circuit specification when taking the circuit pull-up current (see PORT0 configuration current for $V_{in}=V_{ILmax}$) and other leakage currents from external circuits connected to PORT0 pins into account.

$R_{pd} < (V_{ILmax})/ (I_{POl} + I_{other\ circuits})$

Recommended maximum value : R_{pd} = 8KΩ; commonly used values are, although larger than the calculated result, 10KΩ.

Pull-up resistors

PORT0 supplies internal pull-up resistors that are active during Reset. Pull-up resistors shall be low enough so that Input voltage in P0.x is within circuit specification when taking into account the circuit pull-up current (see PORT0 configuration current for $V_{in}= V_{IHmin}$) and other leakage currents from external circuits connected to PORT0 pins. For worse case evaluation, leakage current from other external circuits shall always be added to circuit leakage current.

$R_{pu} < (V_{ddmin} - V_{IHmin})/ (I_{other\ circuits} - I_{POh})$

No external pull-up resistor is necessary if $I_{other\ circuits} < I_{POH}$.

Clock Options on PORT0 P0H.5 - P0H.7

P0H.7	P0H.6	P0H.5	CPU Frequency $f_{CPU} = f_{XTAL} \times F$	External Clock Input Range[1]	Notes
1	1	1	f_{XTAL} x 4	2.5 to 10MHz	Default configuration
1	1	0	f_{XTAL} x 3	3.33 to 13.33MHz	
1	0	1	f_{XTAL} x 2	5 to 20MHz	
1	0	0	f_{XTAL} x 5	2 to 8MHz	
0	1	1	f_{XTAL} x 1	1 to 40MHz	Direct drive[2]
0	1	0	f_{XTAL} x 1.5	6.66 to 26.66MHz	
0	0	1	f_{XTAL} x 0.5	2 to 80MHz	CPU clock via prescaler[3]
0	0	0	f_{XTAL} x 2.5	4 to 16MHz	

Notes: 1. The external clock input range refers to a CPU clock range of 1...40MHz.
2. The maximum input frequency depends on the duty cycle of the external clock signal, refer to the latest datasheet
3. The maximum input frequency is 25MHz when using an external crystal with the internal oscillator; providing that internal serial resistance of the crystal is less than 40Ω. However, higher frequencies can be applied with an external clock source on pin XTAL1, but in this case, the input clock signal must reach the defined levels V_{IL} and V_{IH2}.

2.2 - PORT0 Start-up Configuration

Figure 4 PORT0 Pin Assigment for Power-on Configuration

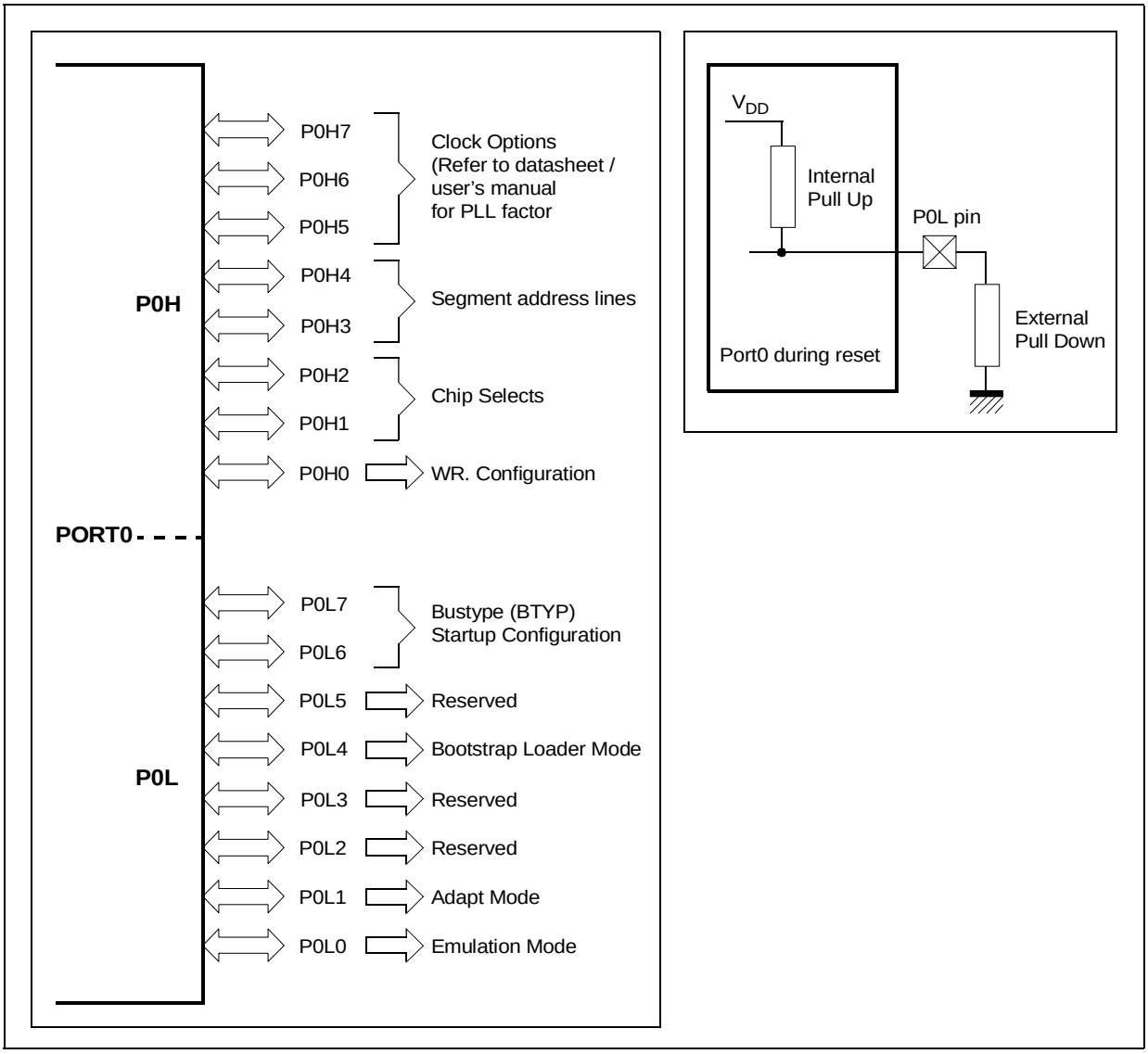


Figure 3 is showing the usage of PORT0 pins to configure ST10F269. All pins are sampled at power-on reset and some of them are not sampled for specific reset conditions. For details, please refer to the product datasheet and the AN1334 "ST10F269/ST10F280 System Reset" application note.

3 - FILTERING / DECOUPLING

3.1 - Decoupling on DC1 and DC2 Pins

DC1 and DC2 are the outputs of ST10F269 internal voltage regulator. They are available on the package to connect external decoupling capacitors.

A capacitor, X7R dielectric or equivalent, with a minimum value of 330nF, must be connected between each of these pins and its nearest V_{SS} pin. This is done for decoupling the output of the internal regulator with the ground.

As DC1 and DC2 pins are internally connected, the voltage regulator sees an equivalent capacitor of 660nF. This is the minimum value that must be provided for correct operation. In case of space issue on the PCB, the capacitors can be of different values provided that the biggest value is on DC1 (pin 56) (DC1 provides the feedback of the regulator). For example DC1 could be connected to a 470nF capacitor and DC2 to a 220nF capacitor.

3.2 - Decoupling on +5V Supply

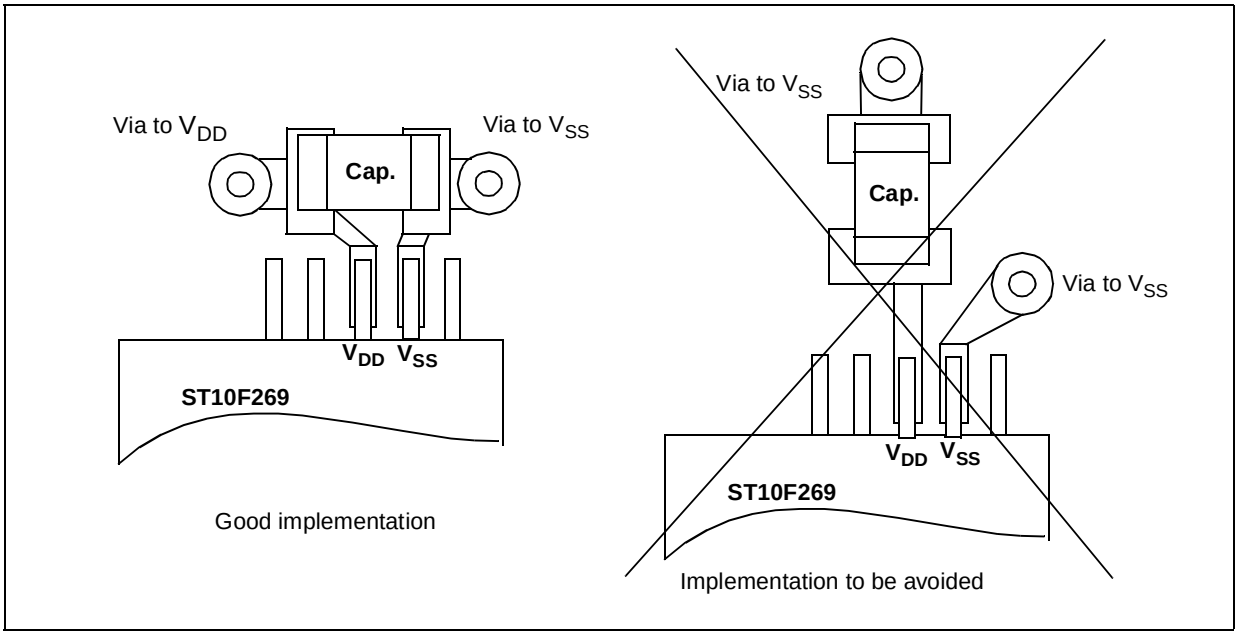
Decoupling capacitors shall be placed as close as possible to the chip V_{SS}/V_{DD} pins,

– Connected to both V_{DD} and V_{SS} pins (adjacent pins).

– Connected to each V_{DD}/V_{SS} pair.

For EMC reasons, decoupling capacitors shall be connected to the V_{DD} and V_{SS} of adjacent pins. This is illustrated by Figure 5 below :

Figure 5 : Implementation of Decoupling Capacitors



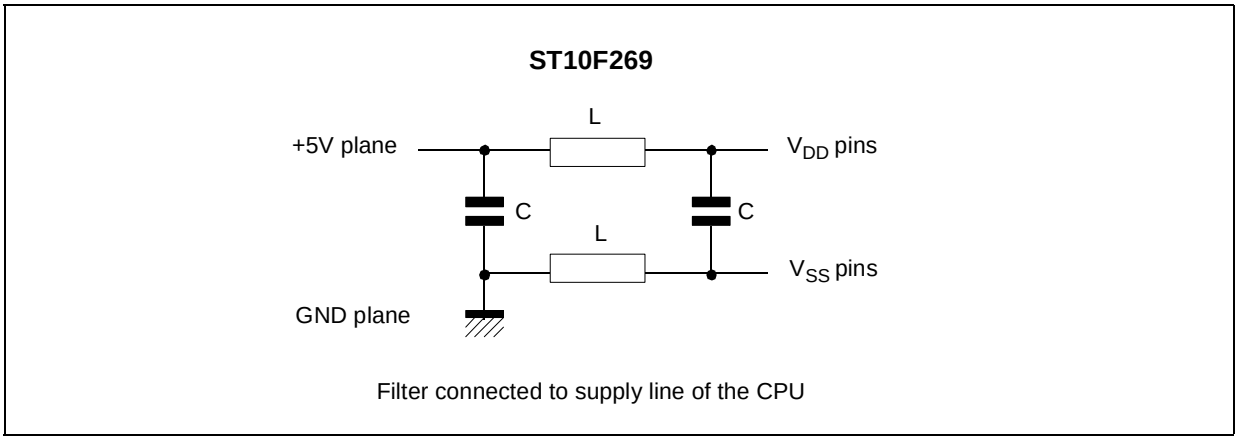
3.3 - Filtering / EMC

As ST10F269 has an internal voltage regulator, +5V pins are not differentiated between output-buffers and internal logic. This means that when EMC filters are used to isolate the CPU from the supply, all ST10F269 supply pins should be isolated with the filter(s).

Example of filter

Filter placed on supply line of the CPU to remove the conducted noise from the supply line of the module.

Figure 6 : Filter Based on Discrete Components



Filter connected to supply line of the CPU

3.4 - Unused Pins

Unsed pins may be an additional source of noise if not properly connected.

Unsed pins shall **NOT** be left floating.

They shall be :

– Connected to V_{SS} via external pull down resistors.

– Configured by software as output (set direction bit to 0) with output=0 (data=0).

Note : Avoiding floating pins in an application also ensures a good control on power consumption.

4 - SPECIAL PINS

4.1 - $\overline{EA}$ External Access Enable pin

. A low level applied to this pin during and after reset forces the ST10F2xx to start the program execution from the external memory space. A high level will start the program execution from internal memory.

If only internal memory will be used, this pin can be tied directly to V_{DD} .

4.2 - RPD Pin

RPD pin (Return from Power-Down) is used to generate the proper internal timing sequence when interruptible power-down mode is used.

If not used, PRD pin can be tied to GND via a pull-down resistor (max = 1MΩ).

5 - RESET

For information on ST10F269 reset, please refer to the AN1334 "ST10F269/ST10F280 System Reset" application note.

6 - ADC

Analog input signal error can be created by poor matching of the source internal resistance with the ADC input parameters, either caused by,

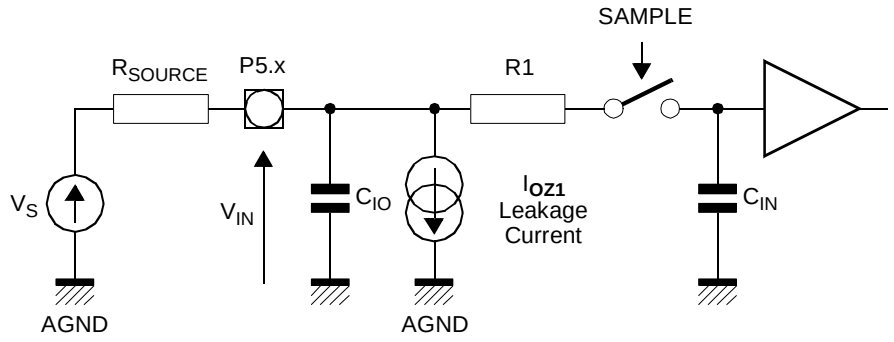
– Voltage drop in the voltage source resistance due to input leakage current,

– Or by poor charging of the ADC internal capacitance (Cin).

– Analog input error can also be caused by noise from the analog input signal.

This section describes each of these causes.

Figure 7 Source Internal Resistance Errors



I_{OZ1} (Input leakage current Port5): maximum ± 200nA (test Condition: 0.45V<V_{IN}<V_{DD})
C_{IO} (Pin capacitance Port5): maximum 10pF (test Condition: f = 1MHz, TA = 25°C, guaranteed by design characterization)
C_{IN} (ADC Internal capacitance): maximum 5pF (guaranteed by design characterization)
R1 (series input resistance): maximum 1.5kΩ (guaranteed by design characterization)

6.1 - Voltage Drop in the Source Resistance

The error generated by the voltage source internal resistance is:

$$error(LSB) = \frac{R_{SOURCE} \times I_{(0Z1)}}{V_{AREF} - V_{AGND}} \times 1024$$

$I_{(OZ1)}$ = specified leakage current.

Refer the latest product datasheet for the value of **$I_{(OZ1)}$** .

Note Input leakage current is caused by parasitic current into the on-chip protection of the input pin; this protection is necessary to protect the device against ESD (Electrical Static Discharge) and against overload.

6.2 - Poor Charging of the ADC Internal Resistance

During the sample time, the input capacitance (C_{IO} and C_{IN}) must be charged/discharged by the external source. The internal resistance of the source must allow the capacitance to reach its final value before the end of sample time:

If this does not happen, i.e. if the source resistance is mismatched to the sample time, a voltage loss will occur at the sample and hold stage. This voltage loss causes an accuracy loss when increasing or decreasing the input voltage from Vref/2 (hold capacitor is pre-charged to Vref/2 before sampling to reduce charge/discharge time).

The error is be calculated by the formula:

$$Max.error_{(LSB)} = \frac{1}{2} \times 1024 \times e^{\left(-\frac{t_S}{RC}\right)}$$

Where: t_S = sample time in µs, R = R_{SOURCE} + R1 in Ω, C = C_{IN} + C_{IO} in µF.

Since the error is proportional to the difference between V_{IN} and Vref/2, the effect produces a non-linearity in the conversion of large-amplitude signals. In practice, if t_S>7RC, the maximum error is reduced to <1/2 LSB (<0.05%).

6.3 - Errors Due to High Frequencies from Input Signal

Small but high frequency signal variations can result in increased conversion error: During sampling time, the analog signal is fed to an internal auto-zero circuitry. Signal variations (2 opposite transitions at least) during this time can generate auto-zero error. Signal variations during sampling time generate excessively high or low conversion results; big variations (ex: 150mV peak to peak variations at 1.5MHz, with a 2.5V offset for 1us sampling time) can generates clamped results (0x000 or 0x3FFh).

Although the sample and hold internal circuitry is integrating signal variations, other internal analog circuitry can be affected by signal transitions during sampling time.

The input analog signal shall always be low pass filtered to ensure that high frequencies are rejected.

6.4 - Reducing ADC Errors

There are four possible optimisations :

Minimise the total source impedance seen by the ST10: This means choosing sensors with low output impedance (not always easy for some types of sensor), and minimising the serial resistance of any protection devices between the analog source and the input pin (while still providing a voltage protection level compatible with the circuit specification).

Match the sample time to the analog source impedance: Use the formula that relates sample time to source internal resistance (given in the ST10 datasheet) to match the source resistance to one of the available sample times.

For example: With a source impedance of 10KΩ, and given

$$R_{ASRC} = t_s / 330 - 0.25$$

then the minimum sample time is:

$$t_s = 330 \times (R_{ASRC} + 0.25)$$

$$t_s = 3380ns(min)$$

Note: This formula includes a safety factor of 10, therefore, dynamic errors are ≈0.02LSB.
Also, R_{ASRC} is the total source impedance seen by the device and, therefore, includes any protection components.

Match the sample time to the analog filter cut-off frequency to remove high frequencies : the ST10F269 sampling time (ADC silicon configuration) shall be 5 to 10 times shorter than the period of the cut-off frequency of the low-pass filter on ADC input signal.

Reduce noise at the input pin: Add an external RC filter (with attention to the source internal resistance). Comput the average value of different samples in the software routine.

For details, see the AN1538 "ST10F269/ST10F280 : Reducing Analog -Digital Conversion Error" application note.

6.5 - Varef Power-up / Down Sequence

Varef should always be lower than the 5V supply (maximum = V_{DD}+0.1v). This is especially true for power-up and power-down sequence when external devices are used to generate Varef.

7 - EXTERNAL MEMORY INTERFACE

ST10F269 external memory bus can easily interface with STMicroelectronics external Flash (M29Fxx series).

Please, refer to application note AN1155 "Connecting the ST10 Microcontroller to M29 Series Flash Memories."

8 - CONNECTING TO L4969

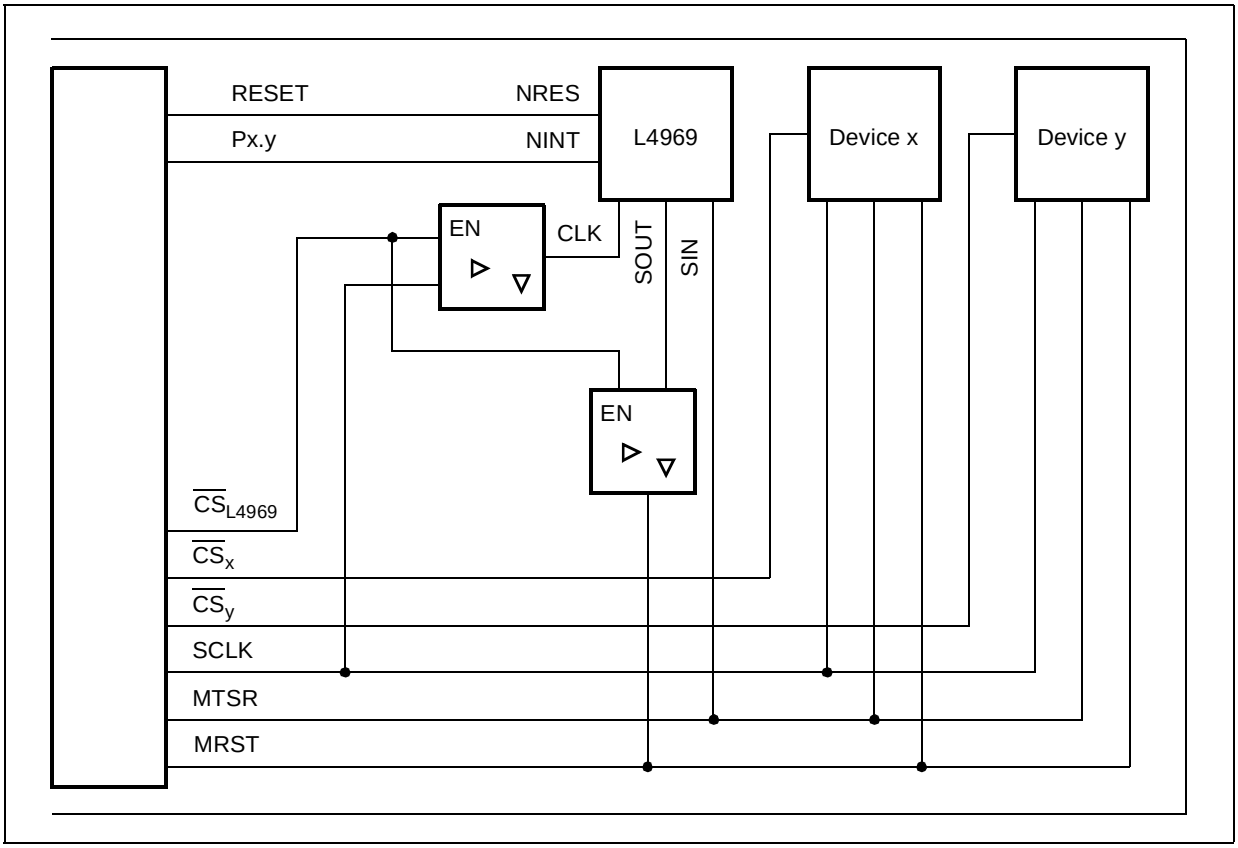
L4969 is a combined voltage regulator and low-speed CAN interface from STMicroelectronices.

The following figure shows how to connect the L4969 CAN interface to the ST10F269/ST10F280 microcontroller when working on a SPI bus with multiple peripherals.

Note: For further information to the L4969 please refer to the L4969 datasheet and the available application notes for this device.

When no other peripherals are connected to the SPI bus, the L4969 can be directly connected to the ST10 SPI lines without any further constraints.

Figure 8 : ST10F269 Connected to L4969 and other SPI Devices



9 - REVISION HISTORY

9.1 - Creation of the AN1544 on the 24th of May 2002

9.2 - Revision of the AN1544 on the 24th of June 2002

Modification of the 1st sentence of section 6.3 p12, "can result in increased conversion error:" .