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APPLICATION NOTE

A MOTOR DRIVES SYSTEM FOR WHEELCHAIR APPLICATIONS

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1. ABSTRACT

This paper deals with a new concept applied in designing low-voltage power MOSFETs that are suitable for high-current low-voltage converter applications. The layout of the proposed device family overcomes the traditional cell structure by a new strip-based geometry. They present interesting characteristics due to the advanced design rules typical of VLSI processes and strong reduction of the on-state resistance. Further, the technology process allows a significant simplification of the silicon fabrication steps, thus allowing to enhance the device ruggedness. The high current handling in switching conditions (up to 150A) with a breakdown voltage in the range between 20-50V in a convenient package solution give the correct answers to the low-voltage range switch applications. This paper starts with the description of the main technology issues in comparison with that of standard devices, particularly focusing on the innovations and the improved performances. Moreover, a detailed characterization of the MOSFET behavior in a traditional test circuit as well as in an actual AC motor drive for wheel chair applications are presented and discussed.

2. INTRODUCTION.

Higher efficiencies are expected nowadays in the field of power converters for battery-powered systems. As industrial and commercial applications of these systems are increasing more and more (laptops, portable equipment, home appliances, electric assisted bikes, electric scooters, wheel chairs, mobiles, etc.), higher efficiencies become of major interest in order to meet the user requirements of long-lasting behavior with the same battery charge. To do that, researchers have made dramatic efforts in designing new converter structures, in increasing the converter switching frequency and in conceiving innovative power devices.

Generally speaking, battery powered systems require low-voltage switching devices (<100V). Power MOSFET devices dominate in this voltage range due to their attractive characteristics of high switching speed and easy driving capability. On-state losses of MOSFETs are of major concern on their total power loss balance, especially in case of converters with low or medium switching frequency. Since on-state losses depend on the drain-source resistance (R_{on}), which is strictly related to the structure design, many modern MOSFETs are realized with a cell-based layout, which determines low on-state resistance. The increase of the cell density allows to further reduce the on-state resistance, thus increasing the current capability per device area-unit. However, for today' s state-of-the-art MOSFETs, ulterior reduction of the on-state resistance by this conventional layout is impeded since this approach is reaching its own physical limit [1]. The need of innovative approaches arises in order to overcome the limit of this technology.

The strip-based layout is a new approach [2], which allows using a simplified process for implanting the body and isolating the poly silicon gate from the source. The new technology is very effective in eliminating the limit of the cell-based layout, which relies on the capability to open smaller and smaller windows on the poly silicon area in order to obtain greater cell-density figures. With the strip-based layout, MOSFET devices show improved performances and a simpler manufacturing process. Moreover, they benefit of the well-established and advanced design rules typical of VLSI processes. On-state resistance values as low as 1.2mΩ can be reached, but the overall MOSFET design must account for the best trade-off of a merit figure, which is the product of the on-state resistance and the gate charge values (R_{on} Q_G).

In this paper the main issues of the new technology are briefly recalled, and the device structure is described and discussed. The static and dynamic characteristics of devices belonging to this new family of MOSFETs are presented and compared with those of more traditional ones. Conventional experimental tests have been carried out and are discussed aiming to determine the impact of turn on and turn off energy loss [3]. A low-voltage battery-powered converter for wheel chairs is used as a workbench for an application-oriented characterization. Some relevant tests are reported and discussed. A detailed analysis is done on the conduction and switching losses and the thermal behavior in the actual application.

3. MAIN TECHNOLOGY ISSUES OF STRIP-BASED MOSFET.

The structure of a strip-based MOSFET device overcomes the limit of a cell structure. In figure 1 the geometry of the two differently conceived devices are shown. The main differences between a standard square-cell layout and the strip implementation may be better understood by inspecting figure 2. In the conventional cell structure shown, all subsequent contacts and isolation openings must be confined and aligned inside the largest square windows opened on the poly silicon layer whose side is L in figure 2. That dimension depends on the alignment, the resolution, and the process tolerances and can be expressed as:

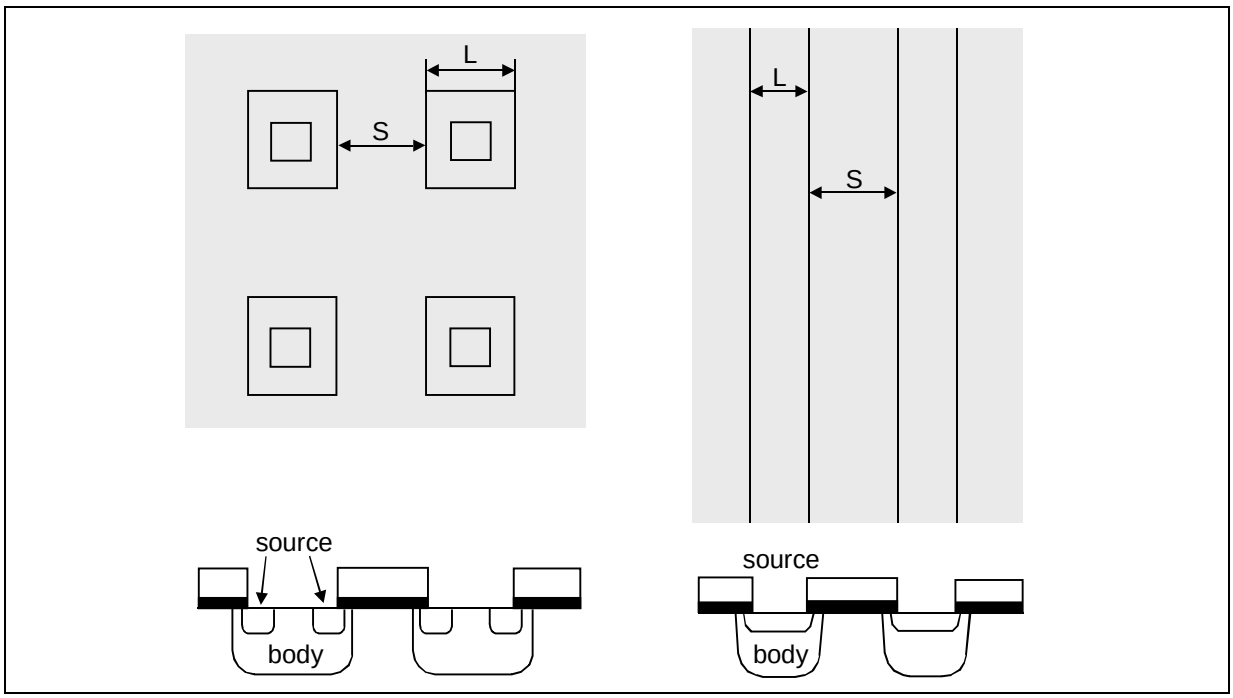
$$L = c + 2b + 2t \qquad (1)$$

where:

- c is the contact dimension for the body region imposed by the resolution of the photolithography equipment;
- b is the contact dimension for the source region which depends on the alignment capability and on the metallization process;
- t is the separation (isolation) between the poly and source metal and is controlled by the alignment feature.

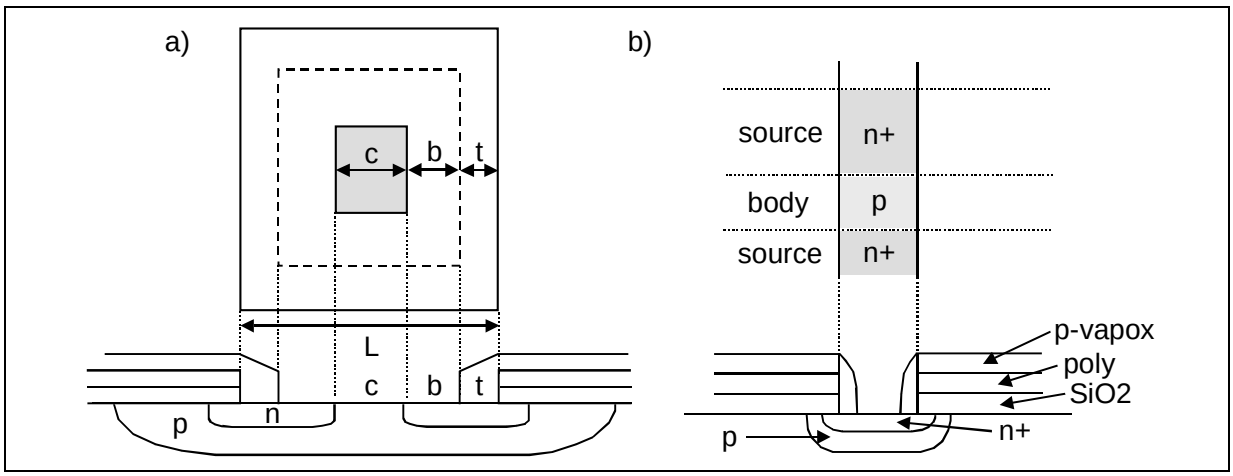
Consequently, the standard cell layout depends on three feature sizes.

Figure 1. Cell-based and strip-based structures of two Power MOSFETs



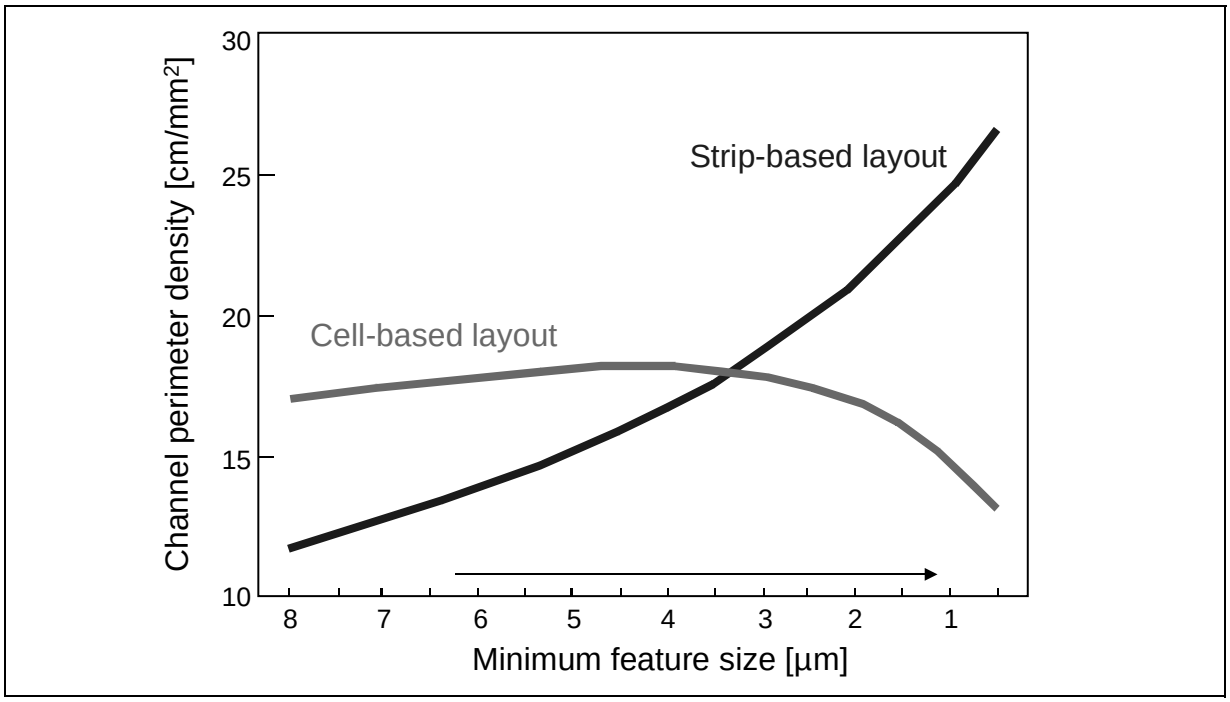
In the strip-based layout process an intermediate dielectric layer is obtained after growing the gate oxide and depositing the poly silicon. In such a sandwich structure parallel strips are opened through an appropriate photo masking process. After implanting the body, the source regions are created by using a sort of small rectangle (patches) masking. The longer sides of the patches are perpendicular to the strips in such a way that they do not need to be aligned within the strip but only along their spacing, which normally is larger than the opening, thus avoiding any alignment problem. The next step is to isolate the poly silicon along the stripe' s periphery thanks to the spacer process. Etching the dielectric material originally deposited and creating "hills"on the sides of the strips achieve this. Finally, Aluminum deposition is done in order to contact the strips, and the fabrication flow chart is completed.

Figure 2. Cell-based and strip-based structures of two Power MOSFETs showing the key parameters of the elemental component of the geometry



The source mask does not need to be aligned within the strip itself; the only critical parameter is the width of the strip (see figure 1), which depends on the equipment resolution. As can be argued from the above description, the process benefits in a reduced number of feature sizes since it is now only dependent on a single feature size, and higher packing densities can be obtained in comparison to the conventional cell-geometry process. The new process is also named Extremely High Density (EHD) referring to the possibility of getting devices with very high equivalent cell densities. Figure 3 compares the obtainable channel perimeter density and thus the current density of the two structures.

Figure 3. Channel perimeter density comparison of cell-based and strip-based structures



4. STATIC AND DYNAMIC BEHAVIOR OF THE NEW DEVICE.

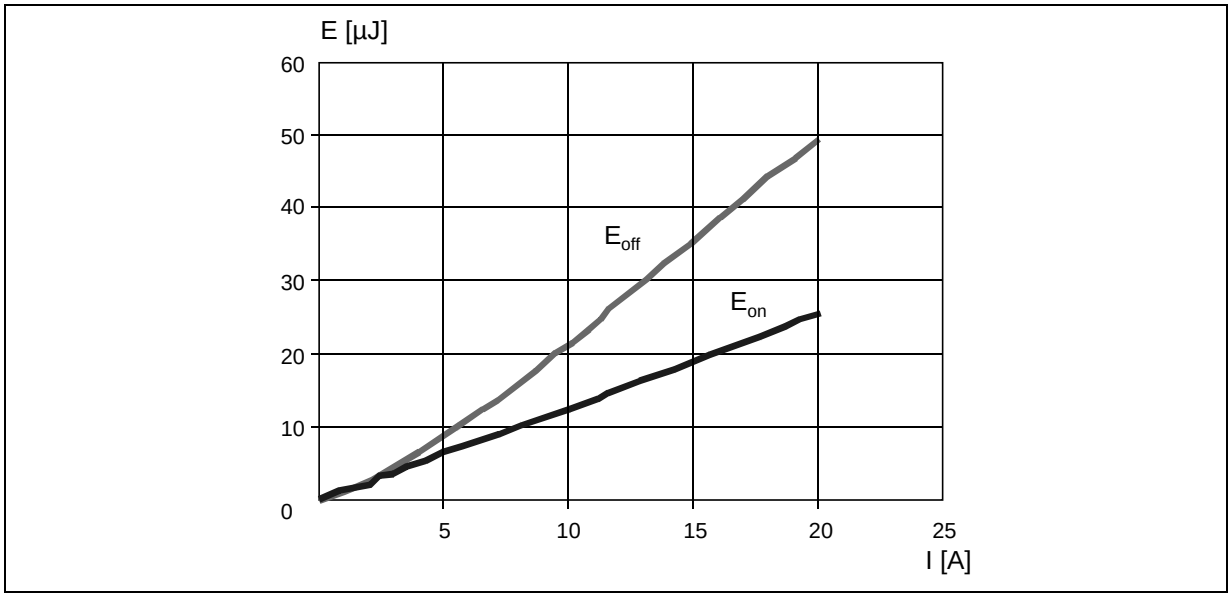
The resulting MOSFET device of the strip-based process shows very interesting characteristics: extremely high packing density and low on-state resistance, rugged avalanche characteristics, and less critical alignment steps. First of all we have selected the device STB80NF55, which was the candidate for the actual application in an AC drive. The drive is described with more details in the next section. The main electrical quantities of the component are summarized in Table 1.

Table 1. STB80NF55 Main Electrical Characteristics

R_{on} [mΩ]	BV_{DSS} [V]	Q_G [nC]	Qsw [nC]	Qgd [nC]	trr [nS]	Qrr [nC]	Irr [A]	Package
6.5	55	180	90	66	80	245	6.4	D^2PAK

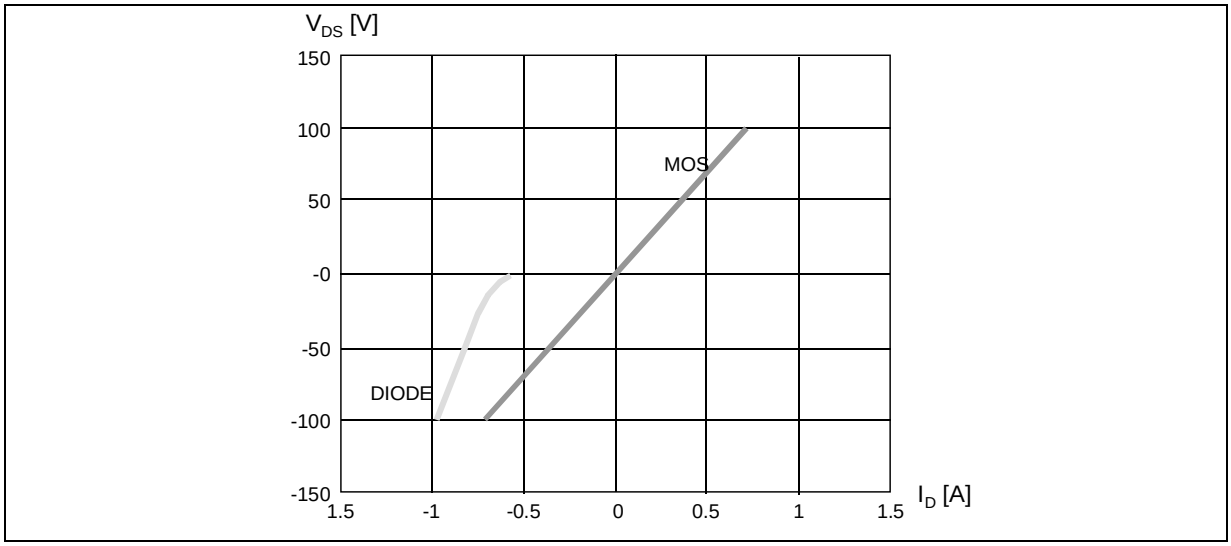
A preliminary characterization in a dc chopper working on inductive load has been done. Looking for the specific application supplied at a dc bus of 24V, several commutation tests (turn on and turn off) have been done at this voltage while the current assumed a variable value. The energy losses in such conditions are reported in figure 4. Linear dependence of the energy versus the switched current is evident both for the turn on and turn off transients.

Figure 4. Energy losses during turn off and turn on transients versus the drain current at V_{DS}=24V



Since the performances of the body-drain diode could be conveniently exploited in bridge topologies, the characteristics of this intrinsic diode have been tested. A favorable characteristic of this internal body-drain diode is its high d*v*/d*t* capability; crucial in all bridge topologies such as motor drives or uninterruptible power supply (UPS). For the used device the allowed limit is 10V/ns. Finally in figure 5 the static characteristics of the new MOSFET are reported. In forward conduction (positive drain voltage) the *I*/*V* characteristic of the MOSFET is traced. In reverse conduction two static characteristics are reported relative to the MOSFET and the intrinsic diode: at zero source-gate voltage the current will flow exclusively as a diode current; with a gate bias voltage the current will flow through the MOSFET as in the case of synchronous rectifier applications.

Figure 5. Static characteristics of the new MOSFET and its body-drain diode at a temperature of 125°C



5. THE LOW VOLTAGE AC MOTOR DRIVE APPLICATION.

In the frame of a funded program aiming to develop an innovative traction system for wheelchair application, a sinusoidal brushless motor drive has been developed. The system is powered by two lead-acid batteries, which are connected in series, and the rated voltage in the dc bus is 24V, while the rated capacity is 45Ah, thus the gross available energy to the traction system is about 1kWh. The innovativeness of such low voltage applications is represented by traction systems based on chopper converters feeding dc motors. Generally speaking, in the past such converters required paralleled operations of many MOSFETs, since the on-state resistance of a single device was unacceptably high. In the case study an injected current value of 80A in the motor will cause about 0.5 V-0.7V voltage drop in the used MOSFET, which is quite acceptable.

The mechanical actuators of the drives are two permanent magnet brushless motors specifically designed [4], rated speed 110 rpm, rated torque 20Nm, rated power 250W, rated current 15 A, number of rotor poles 16, and equipped with coaxial position transducers (absolute encoders). Two-separated three-phase current-regulated pulse-width modulated (CRPWM) inverters feed the motors. The two motors have separated torque references, which are simultaneously given by means of a joystick command; thus the steer action is automatically performed by control of the manipulator position. In particular cases the motors can be required to develop a peak torque, and consequently the current fed by the inverter should increase up to 70 A-80A for several tenth of seconds in order to obtain a torque five times greater than the rated one.

The inverter current is controlled by a tolerance band technique [1, 2], which allows supplying sinusoidal-shaped currents which amplitudes can be changed according to the load requirements. The devices in the full bridge inverter receive the command at a switching frequency f_S , which mainly depends on the width of the hysteresis band (between 2-4%). Figure 6 reports the block diagram of the application, figure 7 the schematic of the 3-phase full bridge inverter.

Figure 6. Block diagram of the traction system for wheelchair applications

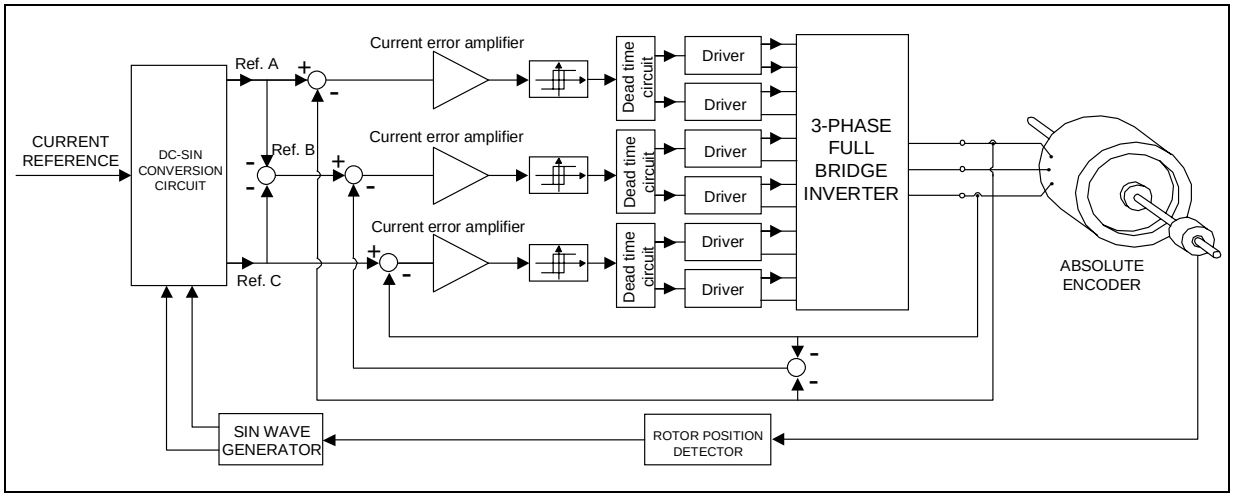
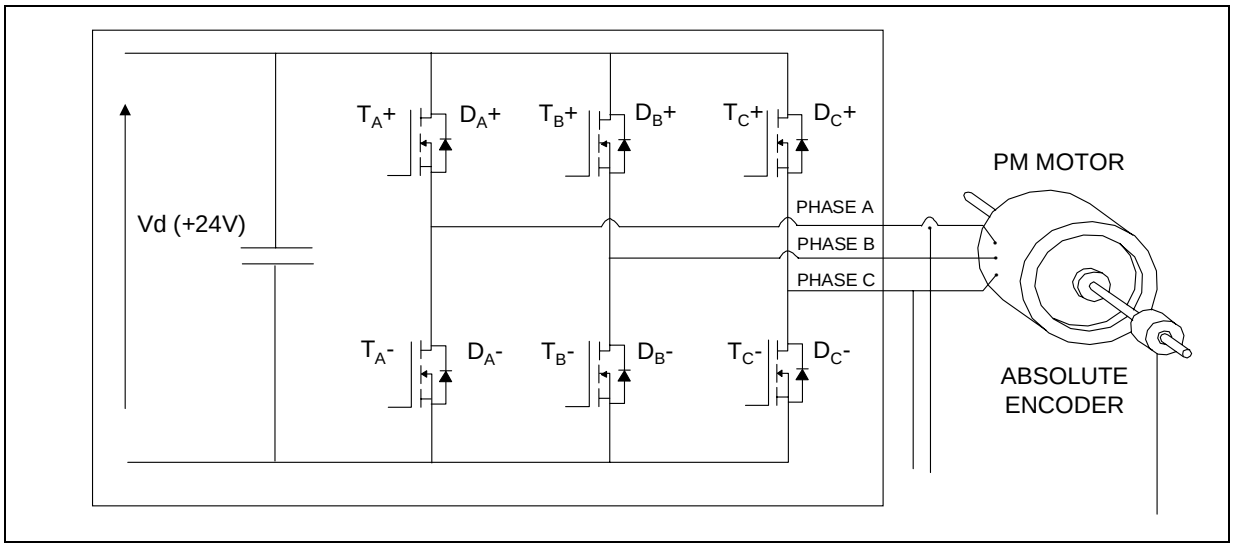
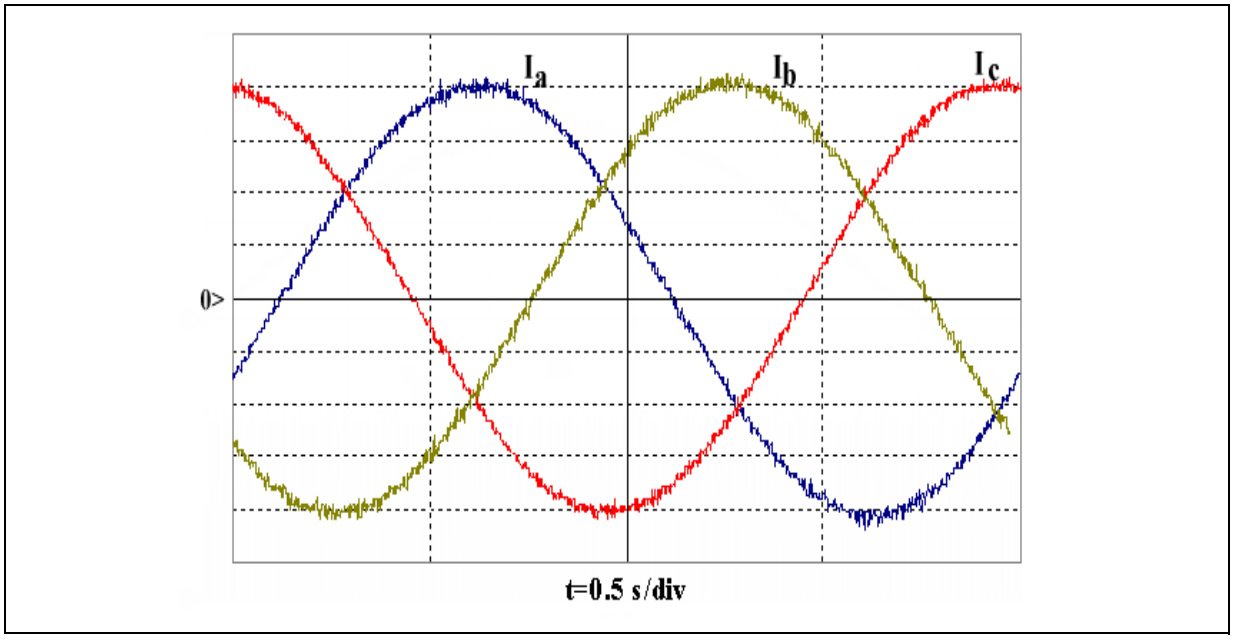


Figure 7. Schematic of the 3-phase full bridge inverter



In our case study with a figure of 4% a (quasi-constant) commutation frequency of 24.5kHz has been observed. Figure 8 shows the experimental traces of the three sinusoidal currents feeding the motor. The fundamental inverter frequency is 0.5Hz according to the need of the low speed on the wheel shaft.

Figure 8. Traces of the motor phase currents while the drive is operating at a fundamental frequency of 0.5Hz ($I_{a,b,c}$=5A/div, t=500ms/div)



5.1. Power Losses Estimation.

The device power losses are related to the switching behavior, and the on-state condition. In a generic *j*-th switching cycle the energy losses at turn-on, turn-off, and on-state condition are expressed respectively by:

$$E_{on \cdot j} = \int_0^{t_{on \cdot j}} V_{DS \cdot j} i_{D \cdot j} dt \qquad (2)$$

$$E_{off \cdot j} = \int_0^{t_{off \cdot j}} V_{DS \cdot j} i_{D \cdot j} dt \qquad (3)$$

$$E_{con \cdot j} = \int_0^{t_{con \cdot j}} V_{DS \cdot j} i_{D \cdot j} dt = \int_0^{t_{con \cdot j}} R_{on} i^2_{D \cdot j} dt \qquad (4)$$

At a constant switching frequency f_S, the turn on, turn off and conduction power losses in a device of an inverter leg (upper or lover device), working with sinusoidal shaped waveform of the current, are expressed respectively by:

$$P_{on} = \frac{1}{2} \sum_1^{f_s} j \int_0^{t_{on \cdot j}} V_{DS \cdot j} i_{D \cdot j} dt \qquad (5)$$

$$P_{off} = \frac{1}{2} \sum_1^{f_s} j \int_0^{t_{off \cdot j}} V_{DS \cdot j} i_{D \cdot j} dt \qquad (6)$$

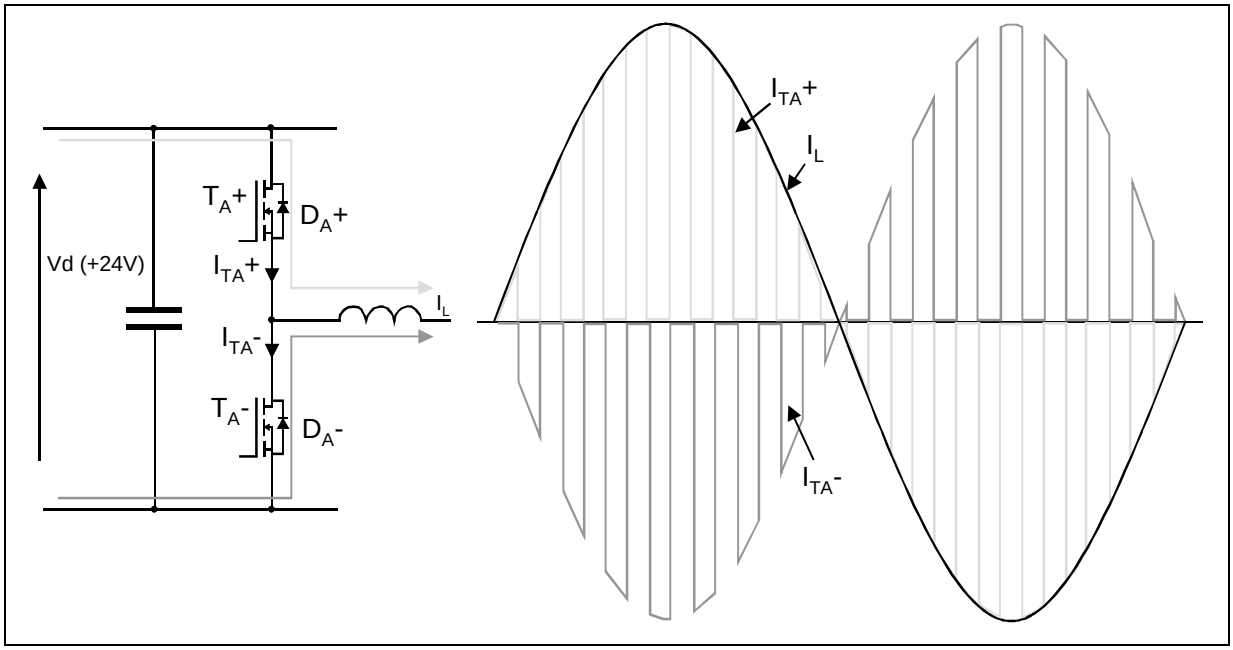
$$P_{con} = \frac{1}{2} \sum_1^{f_s} j \int_0^{t_{con \cdot j}} R_{on} i^2_{D \cdot j} dt \qquad (7)$$

where j is the variable accounting for the number of switching cycles per second, which in turn by definition means the switching frequency f_S. With reference to the used PWM technique, the current through the devices is sinusoidal-shaped, while the voltage across the device is the dc rail voltage maintained at constant amplitude.

The use of relations (5-7), which is very simple in the case of a chopper circuit operated at constant load current [3-7], is more complicated in this case. This is due to two main reasons: the non-linearity of both the instantaneous voltage V_{DS} and the instantaneous current i_D during the switching transient, and the sinusoidal variation of the load current. From inspection of the data reported in figure 4 we can observe the nonlinear trend of the switching losses as function of the amplitude of the drain current at a constant clamp voltage. Thus, obtaining any closed equation from relations (5-6) is practically prevented. Equation (7) can be evaluated straightforward by a simple formula according to the following consideration. With reference to the used PWM technique, the current through the devices is sinusoidal-shaped (figure 9), while the voltage across the devices is the constant dc rail. Due to the use of the body-drain diodes as antiparallel devices, while for example an upper device of the inverter leg is in turn off condition a positive current will flow through the body diode of the lower device [8-9]. This happens surely during the dead time of the inverter, but the current can switch in the channel of the lower MOSFET once its gate is positive biased. The same behavior applies for the lower device in blocking state and the upper device conducting firstly through the diode and then through the channel. Hence, that means from an effective point of view that the conduction losses of a switch during a fundamental period T_1 of the carrier are due to half sinusoidal waveform of the current. In fact, the current flows

through the MOSFET (forward conduction, positive current) or through the intrinsic diode (dead time, and reverse current), or through the MOSFET in reverse conduction and gate biased.

Figure 9. Sinusoidal-shaped current through the upper device and the lower device (first half period), and vice-versa in the second half period



The behavior of the MOSFET while it is in such a reverse conduction, via the intrinsic body diode or via the channel, is clearly shown in figure 10, where the time interval adopted as dead time of the inverter is also evident.

Accordingly, the conduction power loss can be calculated by:

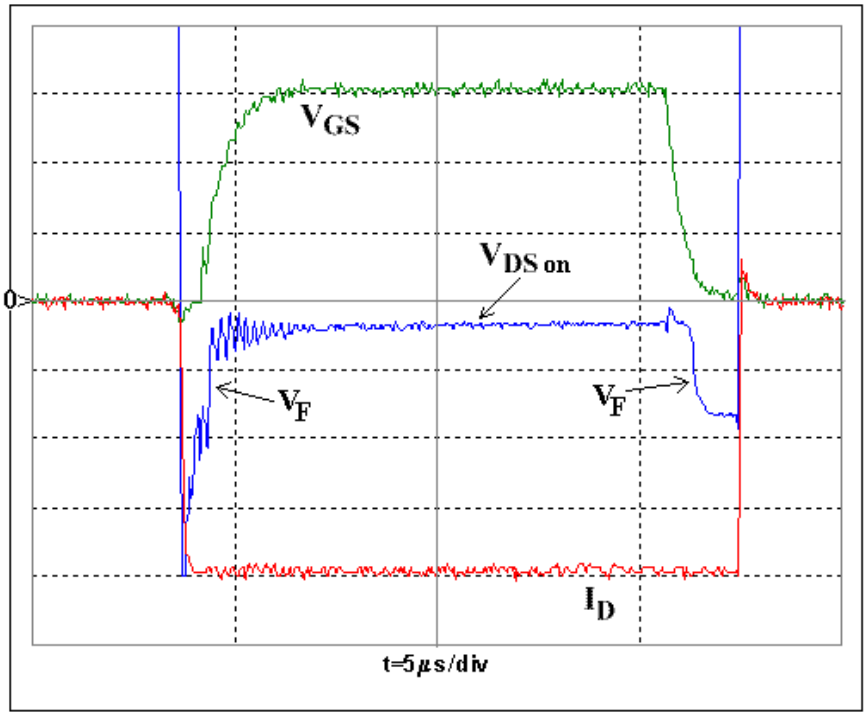
$$P_{con} = 0.5 R_{on} I^2_{rms} \qquad (8)$$

$$P_{con} = \sum_{1}^{f_s} j \int_{0}^{i_{con \cdot j}} R_{on} i^2_{D \cdot j} dt \cong R_{on} \frac{1}{T_1} \int_{0}^{T_{1/2}} \left(\sqrt{21}_{rms} \sin \frac{2\pi}{T_1} t \right) dt =$$

Finally the total power losses can be evaluated by:

$$P_{tot} = P_{on} + P_{off} + 0.5 R_{on} I^2_{rms} \qquad (9)$$

Figure 10. Reverse conduction of the power MOSFET through the intrinsic body diode or through the channel (I_D=5A/div, V_F=0.5V/div, V_{GS}=5 V/div, t=5ms/div)



5.2. Power Losses Measurement from the Thermal Behavior.

The total power losses P_{tot}, in the steady-state conditions as before described, are related to the actual heat sink temperature by relation:

$$P_{tot} = \frac{T_H - T_A}{R_{th,\,HA}} \qquad (10)$$

where T_H is the heat sink temperature, T_A is the ambient temperature (25°C), and $R_{th,\,HA}$ is the thermal resistance between the heat sink and the ambient. Relation (10) can be used to indirectly measure the total power losses, by measuring the ambient and heat sink temperatures and knowing the thermal resistance.

First of all the thermal resistance has been experimentally established, by means of a specific test with known power condition, at $R_{th,\,HA}$=15°C/W accounting for the actual layout. Hence, the total power losses expressed by relation (9) have been evaluated by (10) measuring the temperatures in the prototype in several loaded conditions. A separation in switching and conduction power losses has been carried out by calculating P_{con} through equation (8) and P_{sw} as difference of the total and the conduction power losses. The main results obtained are reported in the Table 2.

The same test procedure has been repeated with a different hysteresis band (about 18%), which implies a different ripple on the phase currents of the motor, in order to determine the influence of the switching frequency on the thermal behavior of the devices. In such a condition the switching frequency reduced to 1kHz. The traces of the motor currents for this new operating condition are reported in figure 11. The

ripple is increased but is still tolerable. In figure 12 the whole results of the two test conditions with different switching frequencies are given; the traces are relative to the total power losses and the conduction ones.

TABLE 2. THERMAL BEHAVIOR OF THE POWER MOSFET AT DIFFERENT LOAD CONDITIONS: HYSTERESIS BAND 4%

I [A]	T_H [C]	P_{tot} [W]	P_{con} [W]	P_{sw} [W]	$R_{DS(on)}$ [mΩ]
5.74	50.2	1.68	0.06	1.62	6.90
9.08	60.8	2.39	0.15	2.24	7.22
10.30	64.3	2.62	0.19	2.43	7.32
13.13	71.3	3.08	0.32	2.76	7.53
15.00	76.0	3.40	0.43	2.97	7.68
19.70	95.0	4.67	0.80	3.87	8.25

Figure 11. Experimental traces of the phase currents. The switching frequency of the inverter is 1kHz as consequence of the increased tolerance band of the hysteresis comparators (I_a=10A/div, t=50ms/div)

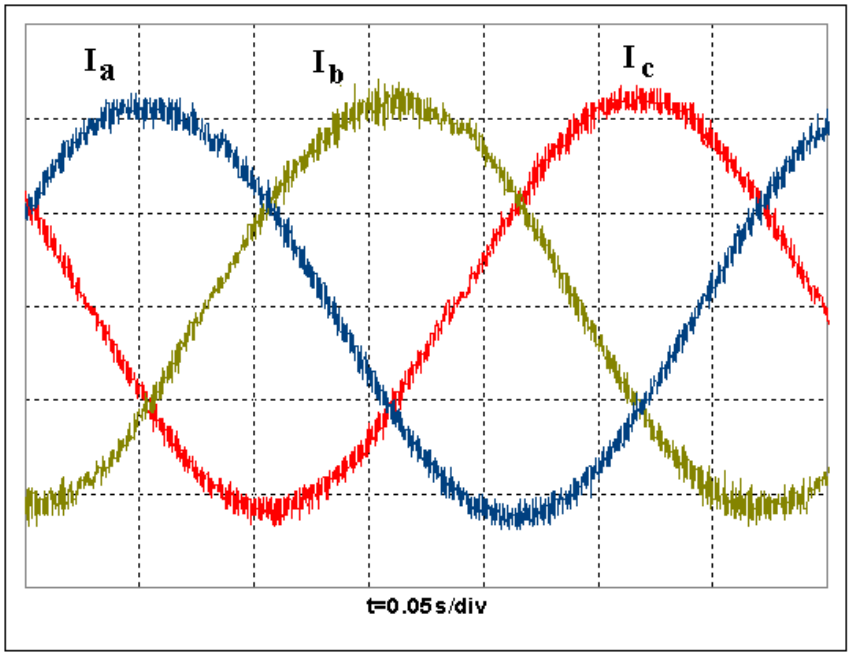
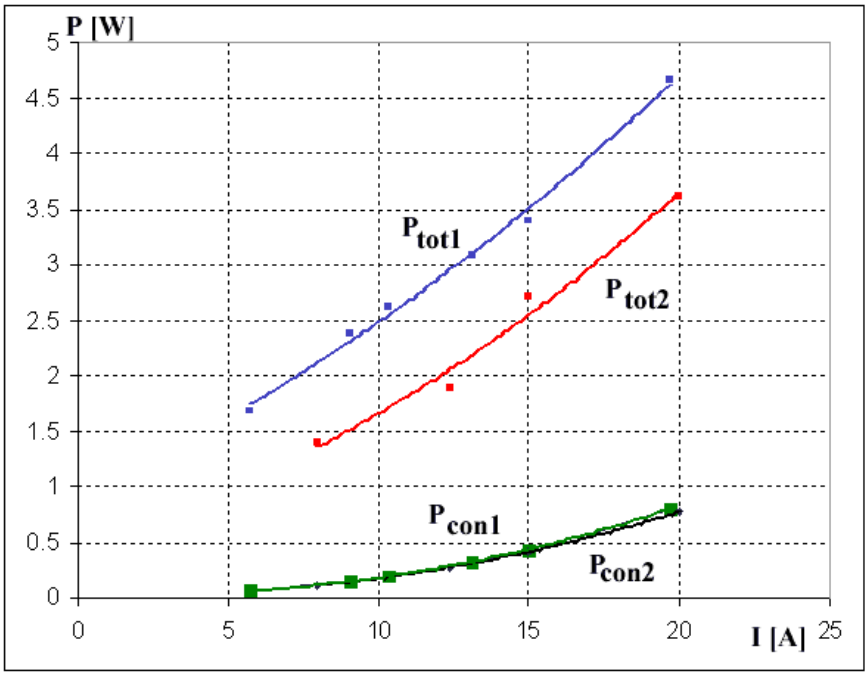


Figure 12. Total power losses at two switching frequencies (1kHz and 24.5kHz), and conduction losses in a power MOSFET of the inverter leg



6. CONCLUSION.

A full characterization of the device has been presented. First of all the MOSFET has been tested in order to evaluate the static and dynamic performances by traditional procedures. Then the device behavior has been investigated in a conventional chopper circuit, and several switching cycles have been performed in order to define, at constant clamp voltage, the trend of the energy losses as function of the drain current. A full characterization on a specific battery-powered converter has been presented and discussed. In particular, an analysis of the power losses has been previously carried out aiming to calculate and separate the switching and conduction contributions in such an application. Finally an experimental validation by a steady state thermal behavior has been performed to apply the analytical relations that have been determined. The results are interesting thus encouraging the use of the internal diode as antiparallel diode. In conclusion, the power MOSFETs presented has been demonstrated to be very suitable for inverter bridges in the field of commercial and industrial applications working at low voltage.

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