AN1365
APPLICATION NOTE

GUIDELINES FOR MIGRATING ST72C254 APPLICATIONS TO ST72F264

INTRODUCTION

This application note provides information on using ST72264 new series in an application originally designed for the ST72254, 215, 216, 104 series.

1 FEATURE OVERVIEW

Feature [1]	ST72104	ST72215	ST72216	ST72C254	ST72260	ST72262	ST72F264
Package	SDIP32/SO28 (no change)						
Program Memory	FLASH/ROM						
Operating Supply	3.2V to 5.5V				2.7V to 5.5V		
Register Map	128 bytes (no change)						
I/Os	28 pins (see Section 2.2 Pinout)						
Slow Mode	Yes						
Active-HALT	No				Yes (4096 t_{CPU} delay on wake-up)		
Nested Interrupts	No				Yes (not by default)		
Watchdog	Yes						
16-bit Timer	1	2	1	2	2 (minor change in PWM and One Pulse modes)		
SPI	Yes						
SCI	No						Yes
I^2C	No			Yes	No		Yes
ADC	No	Yes (8-bit)			No	Yes (10-bit)	
LVD	3 Levels (CFlash and XFlash levels may differ, refer to the datasheet)						
CSS	Yes (fixed frequency) -> CRSR				No		
Emulator	ST7MDT1-EMU2B and ST7MTD1-DVP2				ST7MDT10-EMU3		
Programming tools [2]	ST7MDT1-EPB2 and ST7MTD1-DVP2				ST7MDT10-EPB and ST7MDT10-DVP3		

Note 1: refer to the corresponding datasheets for more information on electrical characteristics.

Note 2: Go to http://www.st.com > Products > Product Support > Microcontrollers - Forum for information on third-party tools.

Rev. 2.0

2 PINOUT COMPATIBILITY

2.1 PACKAGE

All devices are available in SDIP32 and SO28 packages.

2.2 PINOUT

Some pins have been changed in the pinout of the ST72F264 (and subsets) device to add the SCI peripheral (see Table 1) and to move the ISP pins (which have become ICC pins) (see Table 2).

For more information about ICC (In-Circuit Communication) protocol, please refer to the ST7 FLASH Programming and ICC Reference Manuals available on Internet (http://www.st.com).

Table 1. Addition of SCI Pins

	ST72F264 only	
SDIP32 Package	TDO (pin 20)	RDI (pin 22)
SO28 Package	TDO (pin 18)	RDI (pin 20)

Table 2. Pin Changes

ST72C254 and Subsets		ST72F264 and Subsets	
SDIP32 Package	**SO28 Package**	**SDIP32 Package**	**SO28 Package**
ISPCLK (pin 5)	ISPCLK (pin 5)	ICCCLK (pin 29)	ICCCLK (pin 25)
ISPDATA (pin 6)	ISPDATA (pin 6)	ICCDATA (pin 28)	ICCDATA (pin 24)

TDO is the Transmit Data Output pin and RDI is the Receive Data Input pin of the SCI (Serial Communication Interface) peripheral.

3 TIMING

3.1 CYCLE ACCURACY

All timings are compatible between the ST72C254 and the ST72F264 devices except internal timings linked to the cycle accuracy. The ST72C254 is based on latches (gates) while the ST72F264 is based on RTL (flip-flop). Therefore, a difference of a half cycle may occur between those two devices.

This means that all software with timings based on fixed processor cycle times (a practice not recommended) must be verified in detail. An example of this would be a software wait loop implemented as a sequence of NOP instructions as opposed to polling a busy bit.

This internal difference does not affect the general timings.

3.2 CLOCK SECURITY SYSTEM (CSS)

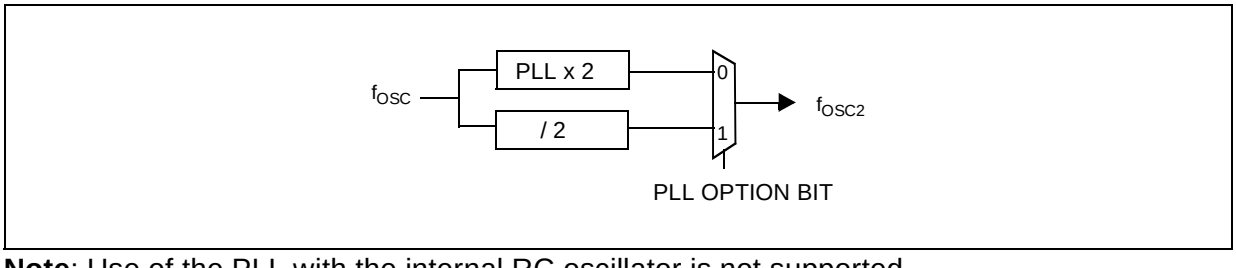
The backup oscillator of CSS available in the ST72C254 device (and subsets) has a fixed frequency between 250 kHz and 550 kHz in normal conditions (T=25° and Vdd=5V).

In the ST72F264 device (and subsets), there is no backup oscillator frequency.

3.3 PHASE LOCKED LOOP (PLL)

A PLL has been added in the ST72F264 in order to be able to multiply the oscillator frequency by 2 (for a f_{OSC} input frequency between 2 and 4 MHz). This PLL is activated through an option bit.

Figure 1. PLL Diagram

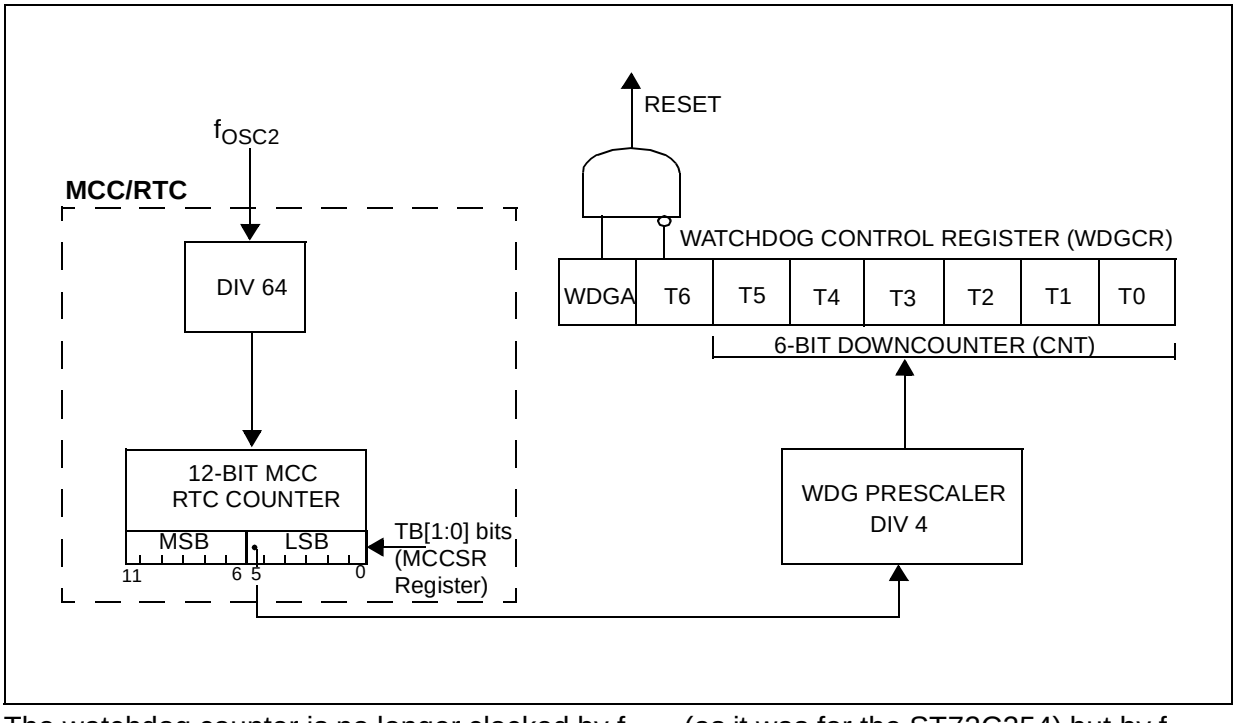


Note: Use of the PLL with the internal RC oscillator is not supported.

3.4 WATCHDOG TIMINGS

In the ST72F264, the watchdog timeout does not have an exact duration as in the ST72C254. It may vary between the min. and max. times specified in Figure 3.. To guarantee upward compatibility, you have to take this into account when you develop your software. The reason for this change is that the watchdog counter has been grouped with the Active-HALT counter and SLOW mode prescaler to enhance power consumption and EMC performance.

Figure 2. Watchdog Block Diagram



The watchdog counter is no longer clocked by f_{CPU} (as it was for the ST72C254) but by f_{OSC2} divided by 16384 (f_{OSC2} is the PLL output frequency when the PLL is activated or $f_{OSC}/2 = f_{CPU}$ if the PLL is disabled).

In the ST72F264 datasheet, the linear relationship between the 6-bit value to be loaded in the Watchdog Counter (CNT) and the resulting timeout duration in milliseconds is described. This can be used for a quick calculation without taking the timing variations into account.

If more precision is needed, use the formulae in Figure 3..

Figure 3. Exact Timeout Duration (t_{min} and t_{max}) (f_{OSC2}= 8 MHz)

t_{min0} = (LSB + 128) x 64 x t_{OSC2}
t_{max0} = 16384 x t_{OSC2}
t_{OSC2} = 125ns if f_{OSC2}=8 MHz

CNT = Value of T[5:0] bits in the WDGCR register (6 bits)
MSB and LSB are values from the table below depending on the timebase selected by the TB[1:0] bits in the MCCSR register

TB1 Bit (MCCSR Reg.)	TB0 Bit (MCCSR Reg.)	Selected MCCSR Timebase	MSB	LSB
0	0	2ms	4	59
0	1	4ms	8	53
1	0	10ms	20	35
1	1	25ms	49	54

To calculate the minimum Watchdog Timeout (t_{min}):

IF $CNT < \left[\frac{MSB}{4}\right]$ **THEN** $t_{min} = t_{min0} + 16384 \times CNT \times t_{osc2}$

ELSE $t_{min} = t_{min0} + \left[16384 \times \left(CNT - \left[\frac{4CNT}{MSB}\right]\right) + (192 + LSB) \times 64 \times \left[\frac{4CNT}{MSB}\right]\right] \times t_{osc2}$

To calculate the maximum Watchdog Timeout (t_{max}):

IF $CNT \leq \left[\frac{MSB}{4}\right]$ **THEN** $t_{max} = t_{max0} + 16384 \times CNT \times t_{osc2}$

ELSE $t_{max} = t_{max0} + \left[16384 \times \left(CNT - \left[\frac{4CNT}{MSB}\right]\right) + (192 + LSB) \times 64 \times \left[\frac{4CNT}{MSB}\right]\right] \times t_{osc2}$

Note: In the above formulae, division results must be rounded down to the next integer value.

Example:

With 2ms timeout selected in MCCSR register

Value of T[5:0] Bits in WDGCR Register (Hex.)	Min. Watchdog Timeout (ms) t_{min}	Max. Watchdog Timeout (ms) t_{max}
00	1.496	2.048
3F	128	128.552

Note: The timing variation shown in Figure 3. is due to the unknown status of the prescaler when writing to the CR register.

4 REGISTER MAP

In the ST72F264, some register addresses and bit locations are changed. These changes have made it possible to use the free locations to add new features.

Note: For easy software migration, two general rules have to be followed:

- All “reserved” byte memory areas must never be “read” or “write”.
- All “reserved” or “unused” bits must be left unchanged when accessing the byte.

4.1 REGISTER ADDRESS

These changes are classified in three groups:

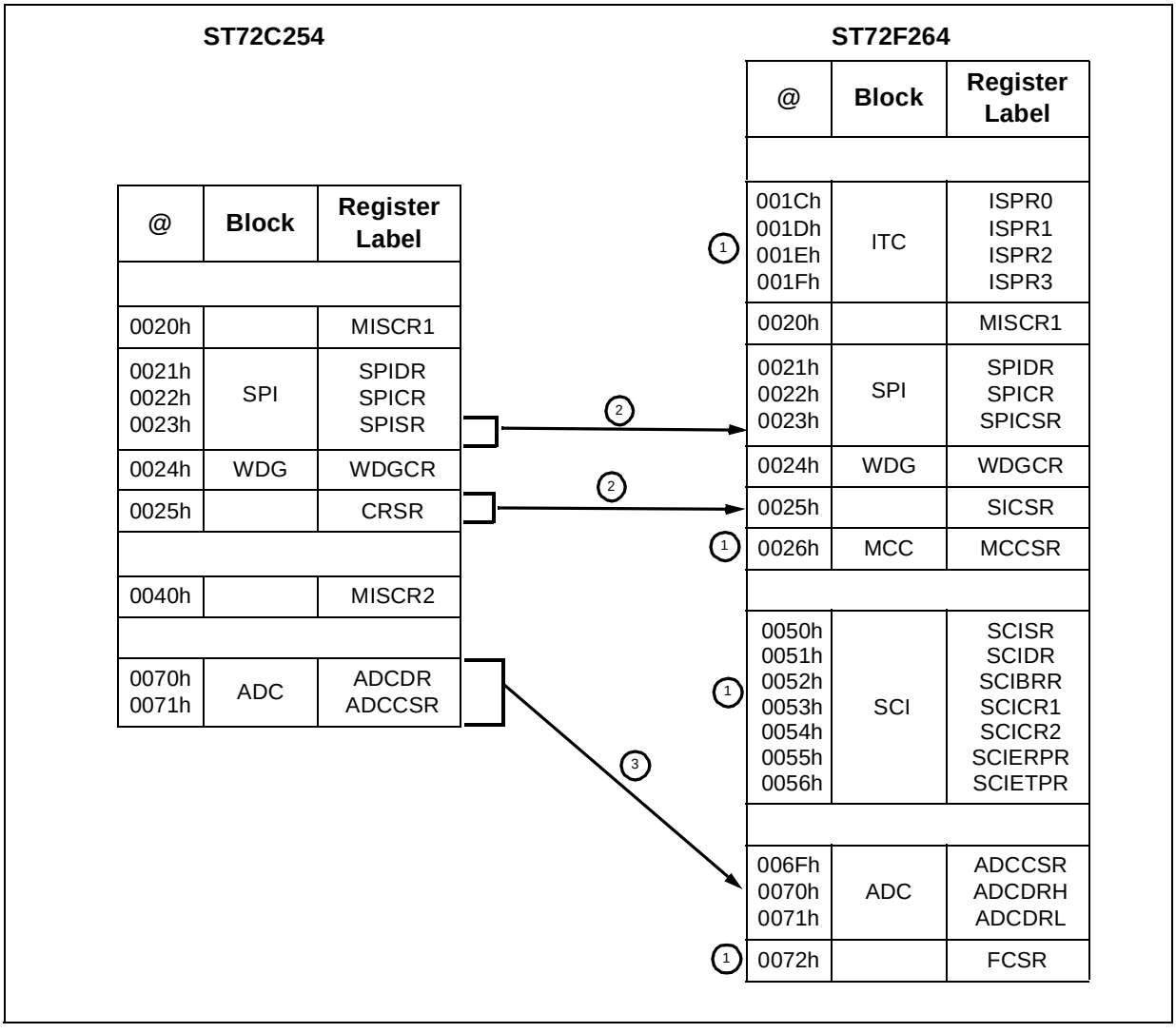
1. New features added: Interrupt Controller (ITC), Main Clock Controller (MCC), Serial Communications Interface (SCI), Flash Control/Status Register (FCSR).
2. CRSR (Clock, Reset, Supply Control/Status Register) has been replaced by the SICSR (System Integrity Control/Status Register). Two bits relative to the AVD (Auxiliary Voltage Detector) feature have been added into the SICSR register. Bits relative to the CSS are no longer used.

   SPISR (Serial Peripheral Interface Status Register) changed to SPICSR (Serial Peripheral Interface Control Status Register). Refer to the Section 5.3.1 for more information.
3. ADC registers changed.

Please, refer to the datasheet for the description of the new features.

Note: These register address changes can be easily performed if you group all the register definitions in a single header file.

Figure 4. Register Map Modifications

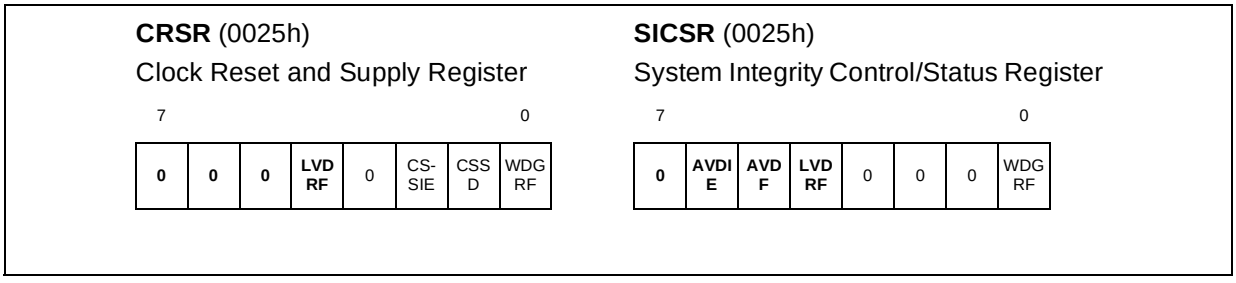


4.2 REGISTER MODIFICATIONS

4.2.1 CRSR Register

The CRSR (Clock, Reset and Supply Register) register has been replaced by the SICSR (System Integrity Control/Status Register) register (see Figure 5.). This SICSR register contains the bits related to the AVD feature.

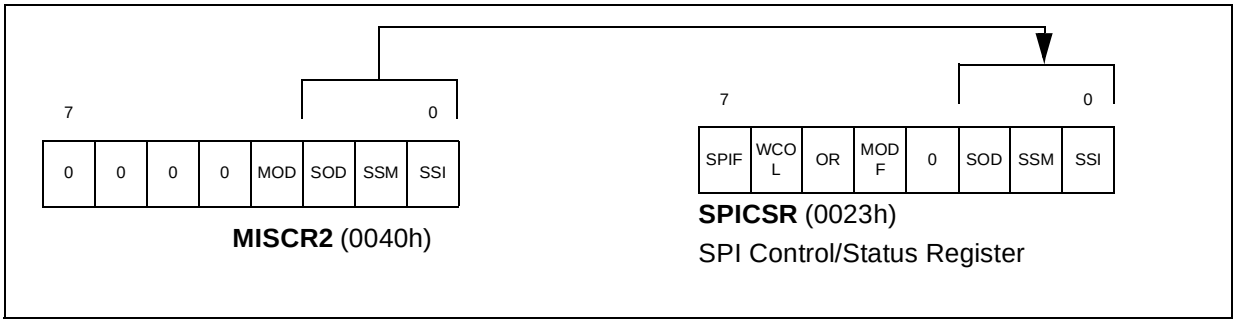
Figure 5. CRSR Register Changes



4.2.2 SPI/$\overline{SS}$ pin

The SPI $\overline{SS}$ pin alternate function is controlled from the MISCR2 like previously, but these control bits have also been duplicated into the SPICSR register in three unused locations.

Figure 6. $\overline{SS}$ pin control



Both registers can be used to control the $\overline{SS}$ pin.

5 NEW FEATURES AND PERIPHERALS

5.1 NESTED INTERRUPTS

A nested interrupt feature has been added to the ST72F264. By default, the interrupt management is concurrent. Some dedicated registers (ISPRx) make it possible for the user to configure the priority level (up to 4) for all the interrupts. Please refer to the datasheet for more information.

5.2 16-BIT TIMER PWM AND ONE PULSE MODE

The 16-bit timer of the ST72C254 has been modified in the ST72F264 to improve the PWM and One Pulse modes. If you use either of these two modes, you may need to change your software when transferring code from the ST72C254 to the ST72F264. All the other modes of the timer do not change.

5.2.1 PWM Mode

To avoid any uncontrolled status on the PWM output, a double buffering on the output compare registers (2 x 16 bits) is implemented in the ST72F264. This double buffering is not present in the ST72C254.

In the ST72F264 PWM mode, any new values written in the four OC1R and OC2R registers are taken into account only at the end of the PWM period (OC2 event) to avoid spikes on the PWM output.

Note: Any modification on the OC1R and OC2R registers must be done just after the OC2 event (using the ICF1 interrupt routine for example).

5.2.2 One Pulse Mode

When the ICAP1 event occurs (on falling or rising edge), the following sequence occurs:

1. IC1R is loaded with the value of the counter when the event occurred (not FFFDh as in the ST72C254)

2. The counter is immediately reset to FFFCh (not at the end like in the ST72C254)

3. OLVL2 is applied to OCMP1 pin if OC1E=1

4. ICF1 is set

5.3 SPI

5.3.1 Control/Status register bits

The SPISR in the ST72C254 has been replaced by the SPICSR in the ST72F264 (refer to Figure 4.). Their differences are the following ones:

- the SPI $\overline{SS}$ pin alternate function is controlled from the MISCR2 as previously, but these control bits have also been duplicated into the SPICSR register.
- the Overrun flag has been added into the ST72F264 (SPICSR register).

5.3.2 HALT mode

The ST72F264 is able to exit from HALT mode through an SPI interrupt. This is not the case in the ST72C254. To guarantee upward compatibility, if the SPI is used in slave mode, the SPI interrupt must be masked (via the SPE or SPIE bits) during HALT mode to avoid any unwanted wake-up events.

5.4 10-BIT ADC

To meet application requirements for increased resolution, the ST72F264 has a 10-bit ADC compared to the 8-bit ADC in the ST72C254. For upward compatibility, both ADCs have identical control registers and operating modes. The 8 most significant bits of the ST72F264 data register (ADCDRH) are used in place of the ADCDR register of the ST72C254. The 8 least significant bits of the ST72F264 data register (ADCDRL) have been added to reach a 10-bit conversion. If ADCDRL is read first, ADCDRH is locked until read (which means that no maximum time is imposed between an ADCDRL read and an ADCDRH read) and a 10-bit conversion will be performed. Then, ADCDRL and ADCDRH are ensured to correspond to the same conversion.

If ADCDRH is read first, ADCDRL is lost and an 8-bit conversion equivalent to the ST72C254 one will be performed.

5.5 MISCELLANEOUS

Many new features have been added in the ST72F264 (refer to Figure 4.):

- MCC (Main Clock Controller)
- ITC (Interrupt Controller)
- FSCR register (Flash Status Control Register)
- SCI (Serial Communication Interface) peripheral

Please, refer to the datasheet for more information concerning the operation of all these features and peripherals.

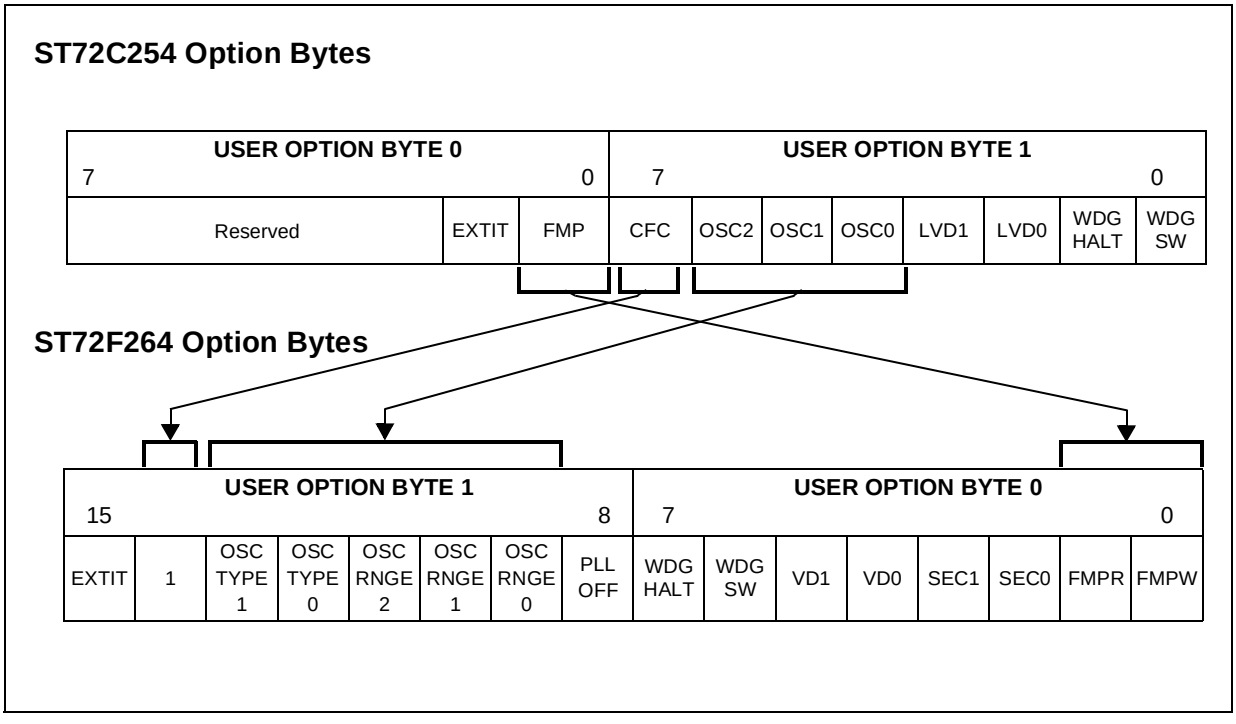
6 OPTION BYTES

Option bits have been added, split or replaced in the ST72F264 compared to the ST72C254 (see Figure 7.):

- Oscillator type bits have been added in order to select a best range of backup safe oscillator
- CFC (Clock Filter Control) bit has been removed
- FMP (Full Memory Protection) bit has been split into 2 bits: FMP_R (read protection) and FMP_W (write protection)
- SEC[1:0] bits have been added to select the ST72F264 sector 0 size
- PLL selection bit has been added
- External RC clock option is no longer supported with ST72F264 device.

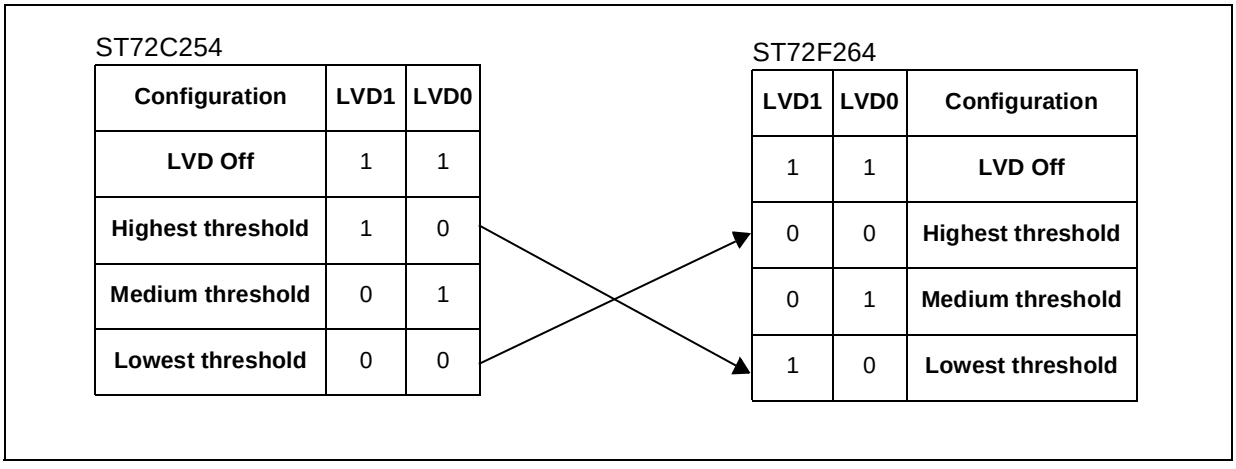
For more information concerning these option bits, please refer to the datasheet.

Figure 7. ST72C254 and ST72F264 Option Bytes



- LVD low and high configuration levels have been swapped:

Figure 8. ST72C254 and ST72F264 LVD Configuration Levels



Moreover, please take note that LVD levels values between the ST72C254 and the ST72F264 may differ a little bit. Please, refer to the datasheet of the respective devices (Electrical parameters part) to get them.

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