AN1094
Application note

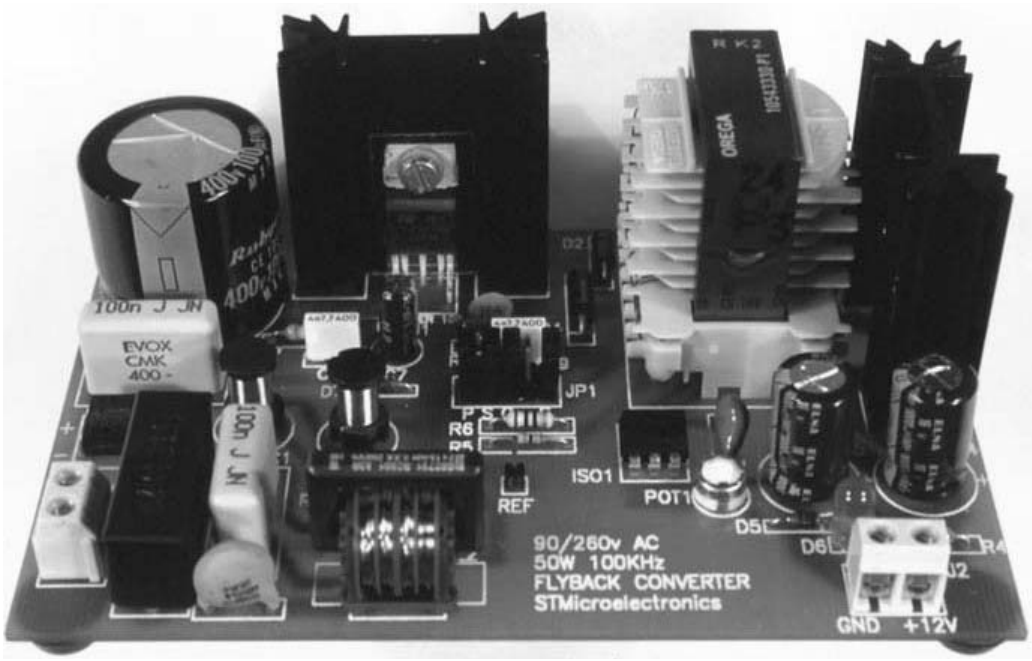
Solution for off-line SMPS using VIPer100-E

Introduction

The present board prototype is a wide-range input off-line 50 W single switch Flyback, working at 100 kHz. It is based on a new off-line smart switcher: the VIPer100-E.

The VIPer100-E is a current mode PWM with a 620 V / 2.5 Ω power switch, able to withstand an avalanche current during normal operation. The start-up of the circuit is done with an internal high voltage current source, which is switched off during steady state. It also includes a regulation function designed to minimize the pin count, while maintaining design flexibility. *Figure 2* presents the internal block diagram of this monolithic device. Such a device can be easily used in any off-line flyback SMPS, with a 100 W power capability for a single input voltage range, or 50 W with a wide input range. This stand-alone off-line Smart Switcher concept provides a cost effective solution for SMPS for many applications such as VCRs, TV sets, satellite receivers or decoders. The benefits for the customer are a simpler design phase and a reduced overall components count due to the optimization of the product configuration.

Figure 1. Standard evaluation board VIPerKITBD

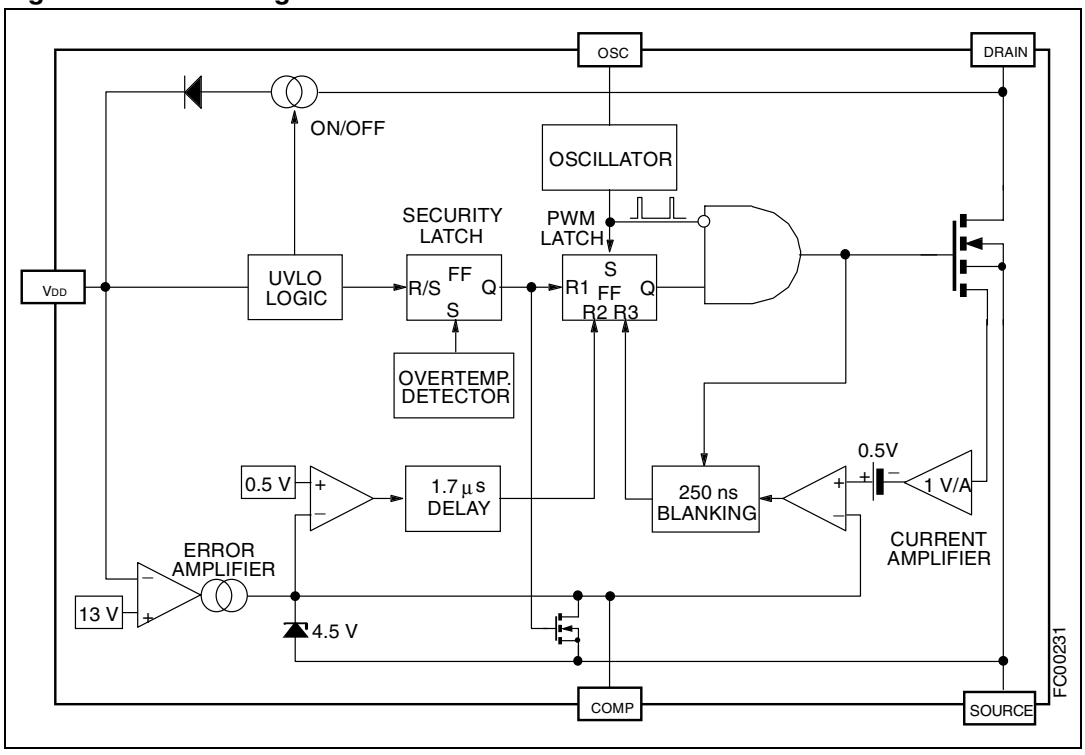


Contents

1 VIPer100-E major features

- Adjustable Switching Frequency up to 200 kHz
- Optimized for current mode control topology
- Inherent feedforward compensation
- Soft-start and enable functions
- Overcurrent protection
- Overtemperature protection
- Overvoltage protection
- Undervoltage lock-out with hysteresis
- Low standby current
- Integrated start-up supply
- Automatic burst mode operation in standby condition
- Internally trimmed BANDGAP reference

Figure 2. Block diagram



1.1 VIPer100-E pin description

- VDD: this is the low level supply pin of the device. At start-up, it delivers 2 mA of charging current. It is also connected to the inverted input of the error amplifier.
- Osc: to be connected to an external R-C network to fix the switching frequency.
- Comp: the control pin of the device. Its voltage sets the peak current of the power switch, and it is the output of the error amplifier. As this amplifier is transconductance, the compensation network on that pin is simply grounded.
- Drain & source: the two power pins of the device. The source is also the ground reference of the device for compensation and oscillation networks.

2 Board features

- AC input voltage: 90 ~ 265 V_{ac} maximum output power: 50 W
- DC output voltage / load: Vout = + 12 V, 4 A
- Operating frequency: 100 kHz
- Par. 3 gives the complete schematics of this off-line flyback converter.

2.1 Feedback loop

This evaluation board allows the user to choose between primary and secondary regulation. Primary regulation is done through the primary auxiliary winding which delivers the low level supply voltage on the Vdd pin of the device. This voltage represents also the secondary output voltage, if correctly filtered in order to avoid the spikes at the beginning of each off phase. This mode of running is achieved by putting one strap on JP1 in the "P" position. Secondary regulation is made with an optocoupler directly from secondary output voltage. It acts on the "COMP" pin, and the auxiliary winding is delivering the low level supply voltage at a lower value than when in primary regulation configuration, thanks to R6. The internal error amplifier is consequently saturated in high state, sourcing a constant current of about 0.5 mA on the "COMP" pin. To address this configuration, just put two straps on JP1 in the "S" position. In any case, a strap in "G" position must be always present.

2.2 Special operations

No limitation has been set on the VIPer device. This limitation can be implemented on the "COMP" pin with a zener or a Vbe multiplier, or whatever else able to clamp the voltage on this pin at about 3 V. When the voltage is clamped, the evaluation board is able to deliver up to 130 W of power, in continuous running. This operation must not last for more than 5 seconds. The evaluation board is fully protected against short circuits. This type of condition leads to a burst operation, with peak current of up to 25 A on the output. As the burst duty cycle is rather low, no risk exists and this situation can continue indefinitely. The board withstands the no-load condition. Notice that in primary regulation, the output voltage rises at about 20 V. Secondary regulation provides better behavior by maintaining the output voltage at about 12 V, and has also the lowest consumption on the main lines: less than 1 watt on a 325 VDC input voltage.

3 Schematics and board layout

Figure 3. Printed board - copper side (scale 1:1)

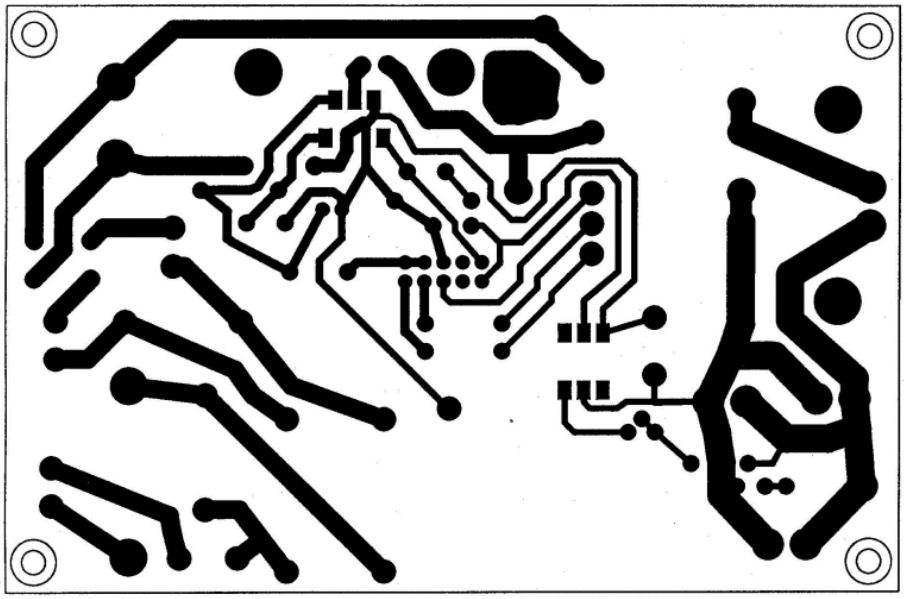


Figure 4. Printed board - components side (scale 1:1)

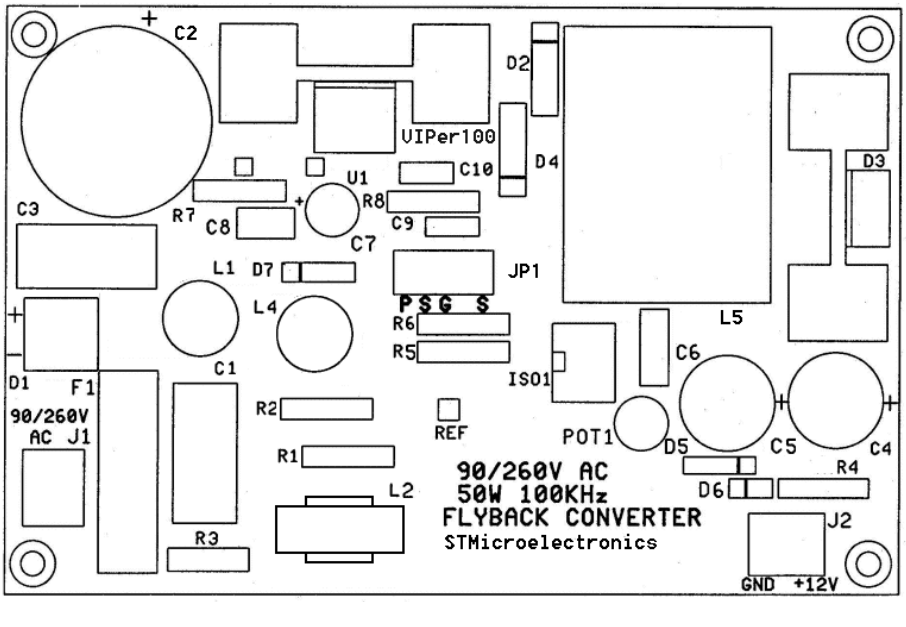
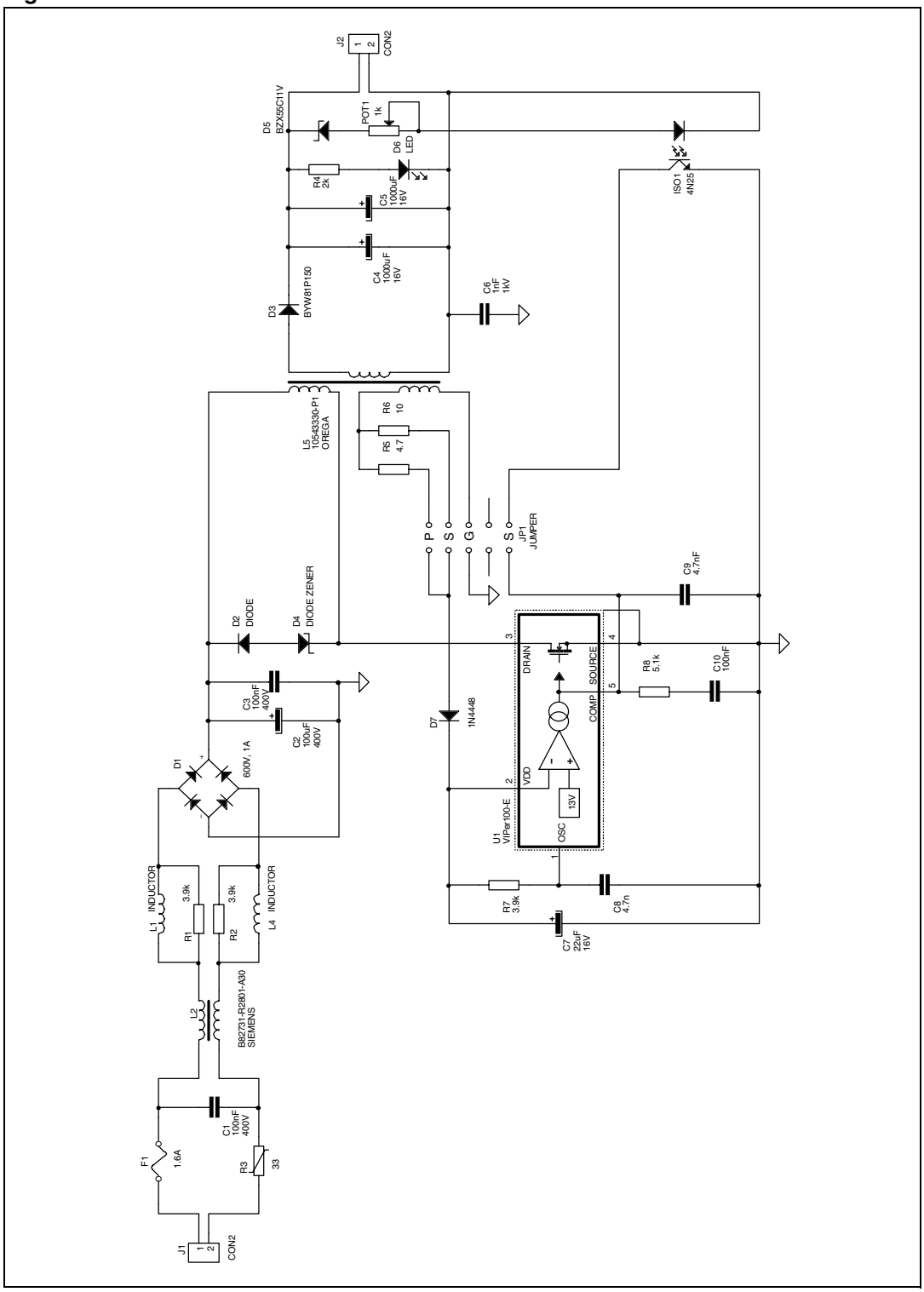


Figure 5. Board schematics



4 BOM

Table 1. Bill of material

Device	Pitch (mm)	Type	Description
C1	15	0.1 µF 400 V	Film
C2	10	100 µF 400 V	Electrolytic, high voltage, high temp
C3	15	0.1 µF 400 V	Film
C4	5	1000 µF 16 V	Electrolytic, low ESR
C5	5	1000 µF 16 V	Electrolytic, low ESR
C6	7.5	1 nF 400 V	Ceramic high voltage - classY
C7	2	22 µF 16 V	Electrolytic
C8	5	4.7 nF	Film, WYMA
C9	5	4.7 nF	Ceramic
C10	5	100 nF	Ceramic
D1	8x5	1 A/600 V	DIL diodes bridge
D2	9	BYT11-400	
D3	5	BYW81/100	
D4	9	BZW50-180	
D5	7	BZX55C10	Zener
D6	4	GREEN LED	
D7	7	1N4448	
F1	23	2 A FUSE	
ISO1	5x8	4N25	
J1	5	2contacts screw PCB connector	
J2	5	2contacts screw PCB connector	
L1	5	100 µH inductor	1 A rated
L2	(*)	B82731-R2801-A30	(1)
L4	5	100 µH inductor	1 A rated
POT1	4+3	1 kΩ POT	3/4 turn, horizontal, miniature
R1	10	3.9 kΩ	0.25 W
R2	10	3.9 kΩ	0.25 W
R3	7.5	33 Ω NTC	LCC
R4	10	2 kΩ	0.25 W
R5	10	4.7 kΩ	0.25 W
R6	10	10 Ω	0.25 W

Table 1. Bill of material (continued)

Device	Pitch (mm)	Type	Description
R7	10	3.9 kΩ	0.25 W
R8	10	5.1 kΩ	0.25 W
L5	(*)	OREGA 10543330-PI	(2)

1. L2 is a SIEMENS MATSUSHITA component.
2. L5 was specially developed by OREGA (THOMSON TELEVISION COMPONENT FRANCE) for this evaluation board.

5 Revision history

Table 2. Document revision history

Date	Revision	Changes
04-Jan-2005	1	Initial release
25-Oct-2007	2	– Document reformatted no content change – VIPer100 replaced by VIPer100-E