74V2G74

SINGLE D-TYPE FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED:
  f_{MAX} = 170 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION:
  I_{CC} = 1 µA (MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 8 mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC}(OPR) = 2V to 5.5V
- FUNCTION COMPATIBLE WITH
  74 SERIES 74
- IMPROVED LATCH-UP IMMUNITY

SOT23-8L

SOT323-8L

ORDER CODES

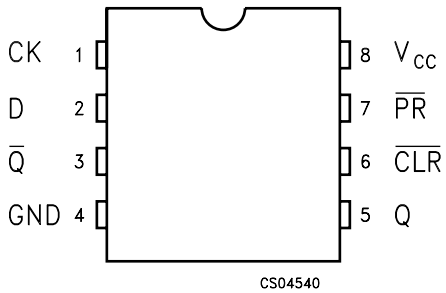
PACKAGE	T & R
SOT23-8L	74V2G70STR
SOT323-8L	74V2G70CTR

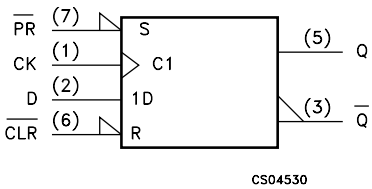
DESCRIPTION

The 74V2G74 is an advanced high-speed CMOS SINGLE D-TYPE FLIP FLOP WITH PRESET AND CLEAR fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS tecnology.
A signal on the D INPUT is transfered to the Q and $\overline{Q}$ OUTPUTS during the positive going transition of the clock pulse.

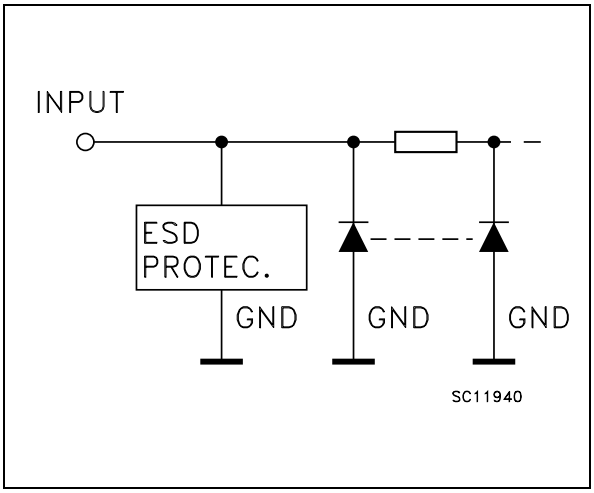
CLEAR and PRESET are independent of the clock and accomplished by a low setting on the appropriate input.
Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.
All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

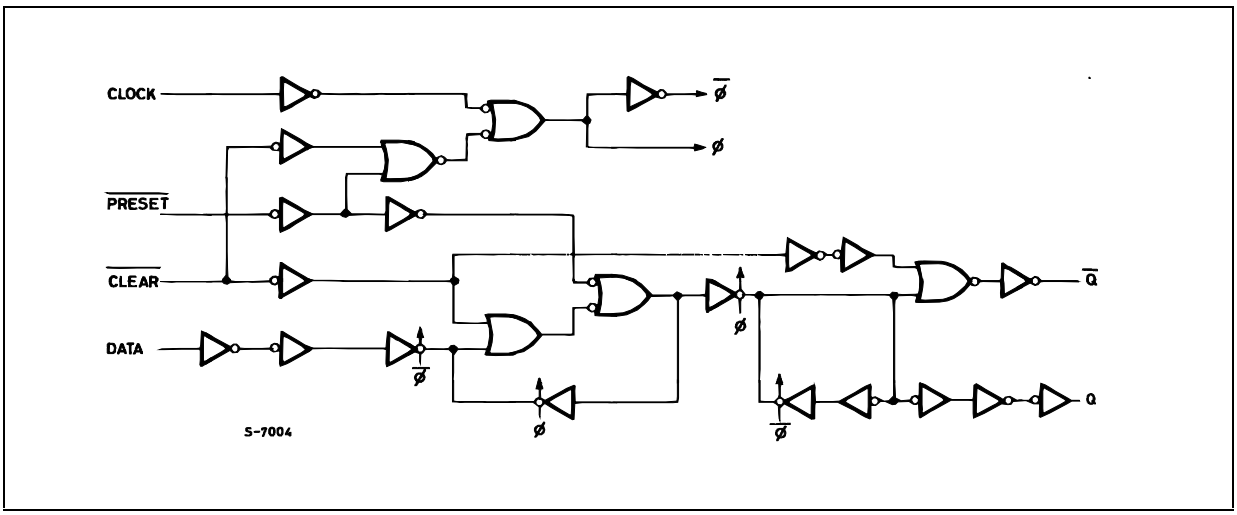
PIN No	SYMBOL	NAME AND FUNCTION
6	$\overline{CLR}$	Asyncronous Reset - Direct Input
2	D	Data Input
1	CK	Clock Input (LOW to HIGH, Edge Triggered)
7	$\overline{PR}$	Asyncronous Set - Direct Input
5	Q	True Flip-Flop Output
3	$\overline{Q}$	Complement Flip-Flop Output
4	GND	Ground (0V)
8	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	
H	H	L	⌐	L	H	
H	H	H	⌐	H	L	
H	H	X	¬	Q_n	$\overline{Q}_n$	NO CHANGE

X= Don't care

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	– 20	mA
I_{OK}	DC Output Diode Current	– 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 5.5	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 1) (V_{CC} = 3.3 ± 0.3V) (V_{CC} = 5.0 ± 0.5V)	0 to 100 0 to 20	ns/V

1) V_{IN} from 30% to 70% of V_{CC}

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		3.0 to 5.5		$0.7V_{CC}$			$0.7V_{CC}$		$0.7V_{CC}$		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		3.0 to 5.5				$0.3V_{CC}$		$0.3V_{CC}$		$0.3V_{CC}$	
V_{OH}	High Level Output Voltage	2.0	I_O=-50 µA	1.9	2.0		1.9		1.9		V
		3.0	I_O=-50 µA	2.9	3.0		2.9		2.9		
		4.5	I_O=-50 µA	4.4	4.5		4.4		4.4		
		3.0	I_O=-4 mA	2.58			2.48		2.4		
		4.5	I_O=-8 mA	3.94			3.8		3.7		
V_{OL}	Low Level Output Voltage	2.0	I_O=50 µA		0.0	0.1		0.1		0.1	V
		3.0	I_O=50 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=50 µA		0.0	0.1		0.1		0.1	
		3.0	I_O=4 mA			0.36		0.44		0.55	
		4.5	I_O=8 mA			0.36		0.44		0.55	
I_I	Input Leakage Current	0 to 5.5	V_I = 5.5V or GND			± 0.1		± 1		± 1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND			2		20		20	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time CK to Q or $\overline{Q}$	3.3(*)	15			6.7	11.9	1.0	14.0	1.0	14.0	ns
		3.3(*)	50			9.2	15.4	1.0	17.5	1.0	17.5	
		5.0(**)	15			4.6	7.3	1.0	8.5	1.0	8.5	
		5.0(**)	50			6.1	9.3	1.0	10.5	1.0	10.5	
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{PR}$ or $\overline{CLR}$ to Q or $\overline{Q}$	3.3(*)	15			7.6	12.3	1.0	14.5	1.0	14.5	ns
		3.3(*)	50			10.1	15.8	1.0	18.0	1.0	18.0	
		5.0(**)	15			4.8	7.7	1.0	9.0	1.0	9.0	
		5.0(**)	50			6.3	9.7	1.0	11.0	1.0	11.0	
t_W	CK Pulse Width HIGH or LOW	3.3(*)			6.0			7.0		7.0		ns
		5.0(**)			5.0			5.0		5.0		
t_W	PR or CLR Pulse Width LOW	3.3(*)			6.0			7.0		7.0		ns
		5.0(**)			5.0			5.0		5.0		
t_s	Setup Time D to CK HIGH or LOW	3.3(*)			6.0			7.0		7.0		ns
		5.0(**)			5.0			5.0		5.0		
t_h	Hold Time D to CK HIGH or LOW	3.3(*)			0.5			0.5		0.5		ns
		5.0(**)			0.5			0.5		0.5		
t_{REM}	Removal Time $\overline{PR}$ or $\overline{CLR}$ to CK	3.3(*)			5.0			5.0		5.0		ns
		5.0(**)			3.0			3.0		3.0		
f_{MAX}	Maximum Clock Frequency	3.3(*)	15		80	125		70		70		MHz
		3.3(*)	50		50	75		45		45		
		5.0(**)	15		130	170		110		110		
		5.0(**)	50		90	115		75		75		

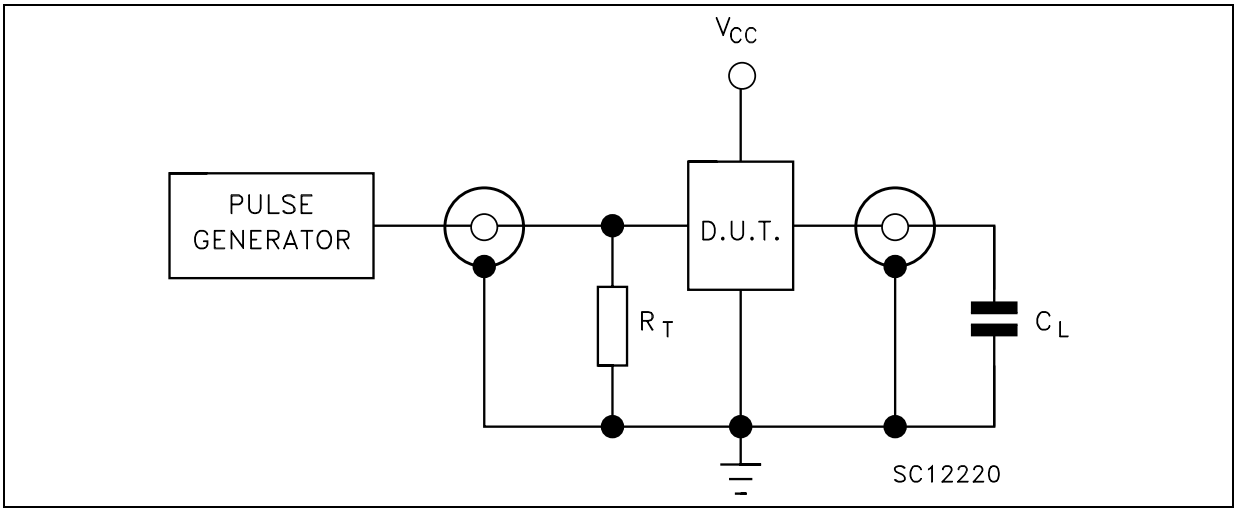
(*) Voltage range is 3.3V ± 0.3V
(**) Voltage range is 5.0V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	3.3			4	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	3.3	f_{IN} = 10MHz		22						pF

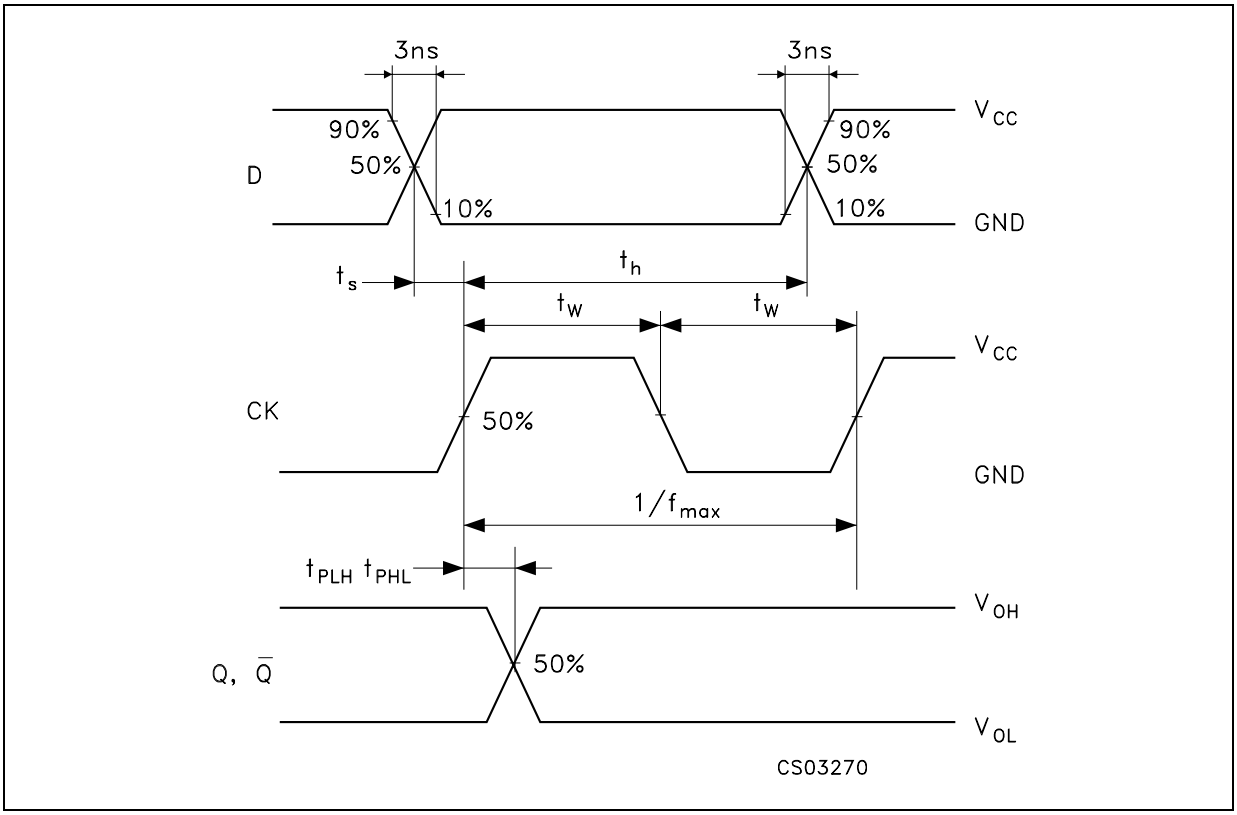
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

TEST CIRCUIT

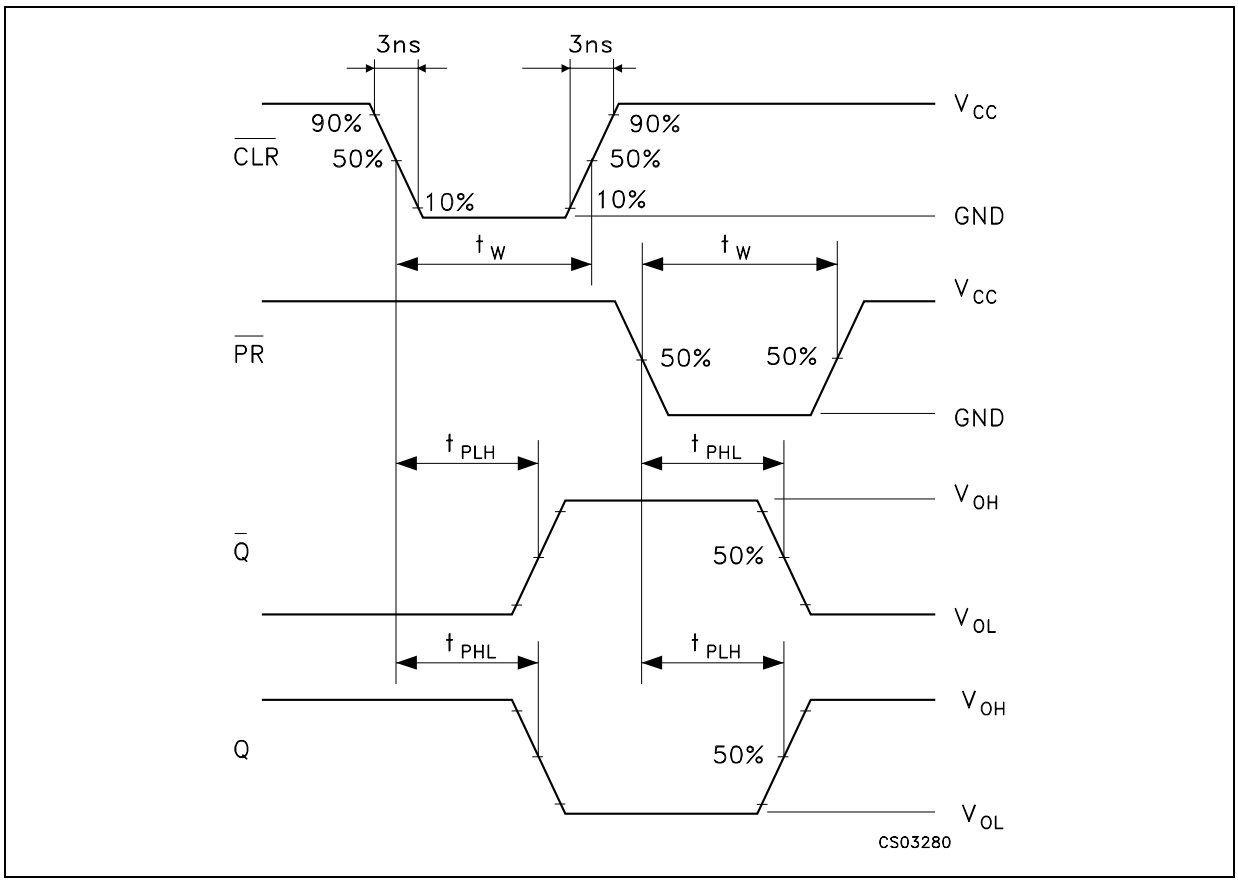


C_L =15/50pF or equivalent (includes jig and probe capacitance)
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

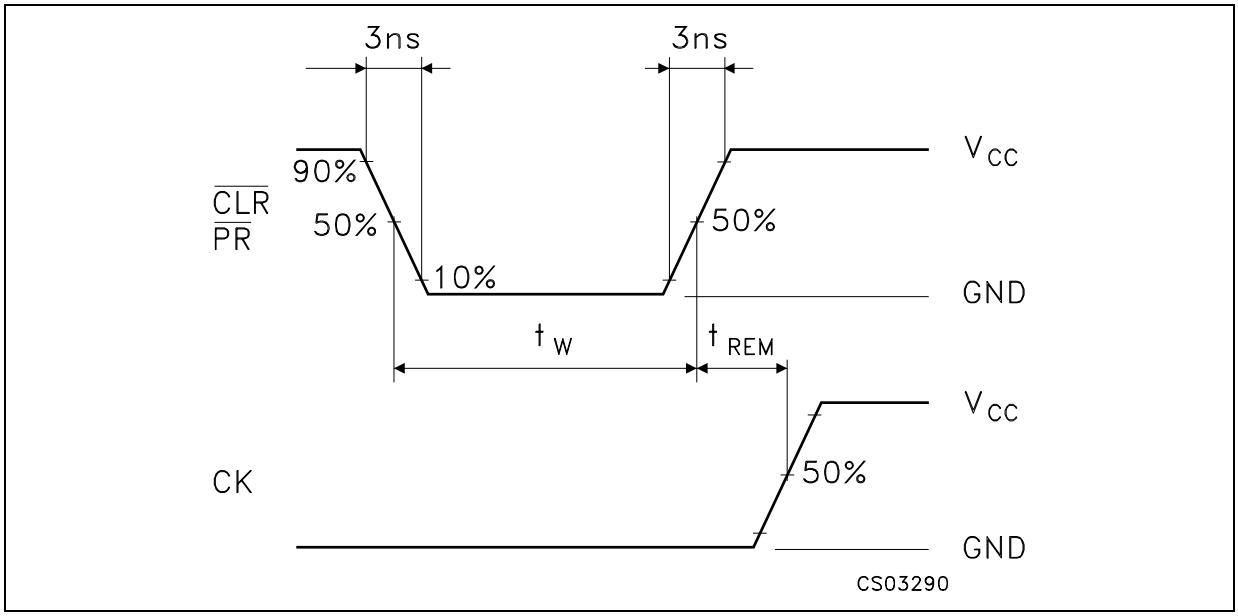
WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES (D TO CK), CK MAXIMUM FREQUENCY , CK MINIMUM PULSE WIDTH (f=1MHz; 50% duty cycle)



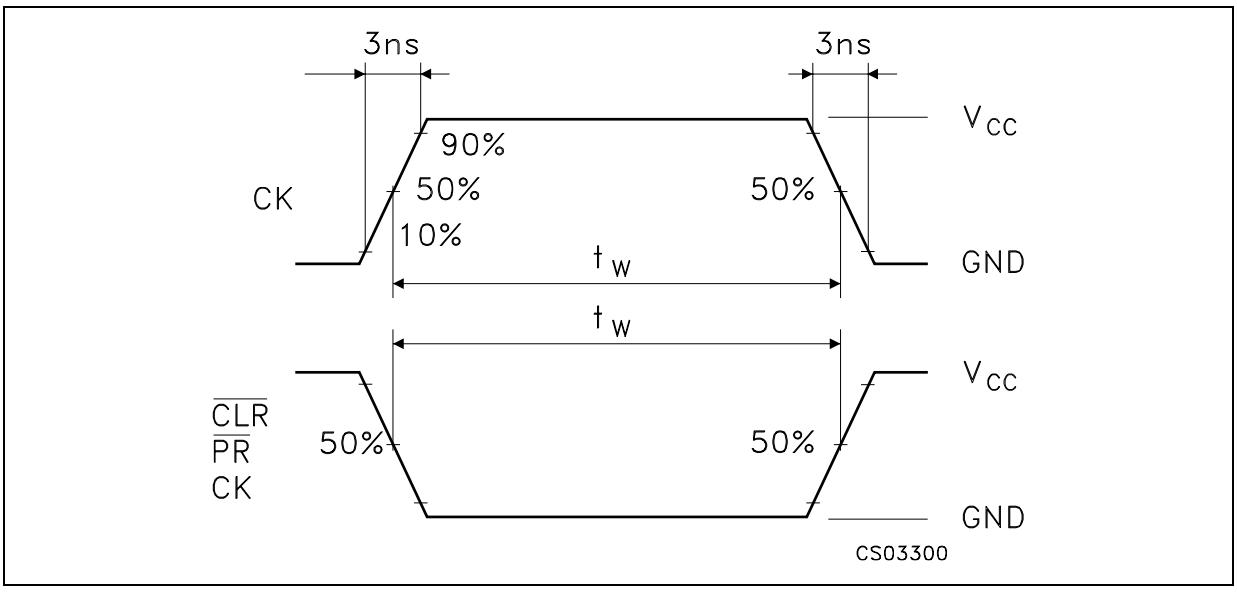
WAVEFORM 2: PROPAGATION DELAYS MINIMUM PULSE WIDTH ($\overline{CLR}$ AND $\overline{PR}$) (f=1MHz; 50% duty cycle)



WAVEFORM 3: RECOVERY TIME (f=1MHz; 50% duty cycle)

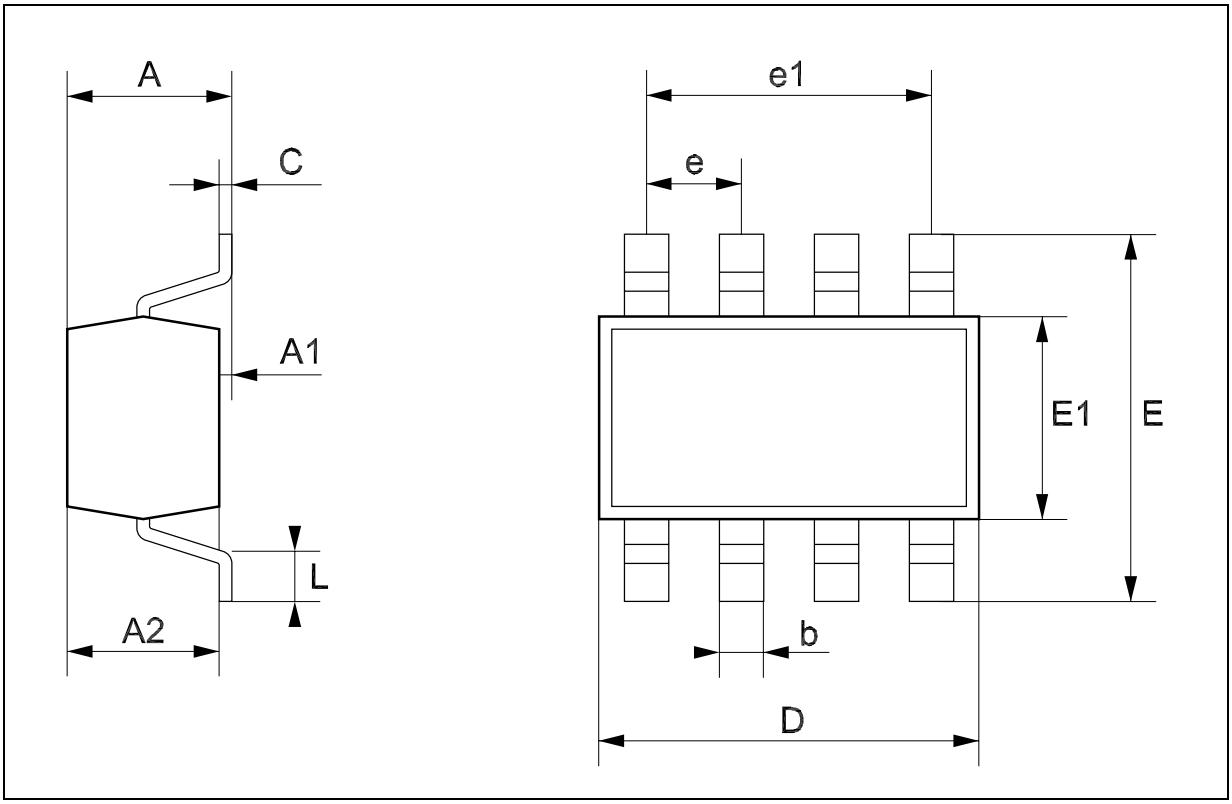


WAVEFORM 4: PULSE WIDTHS



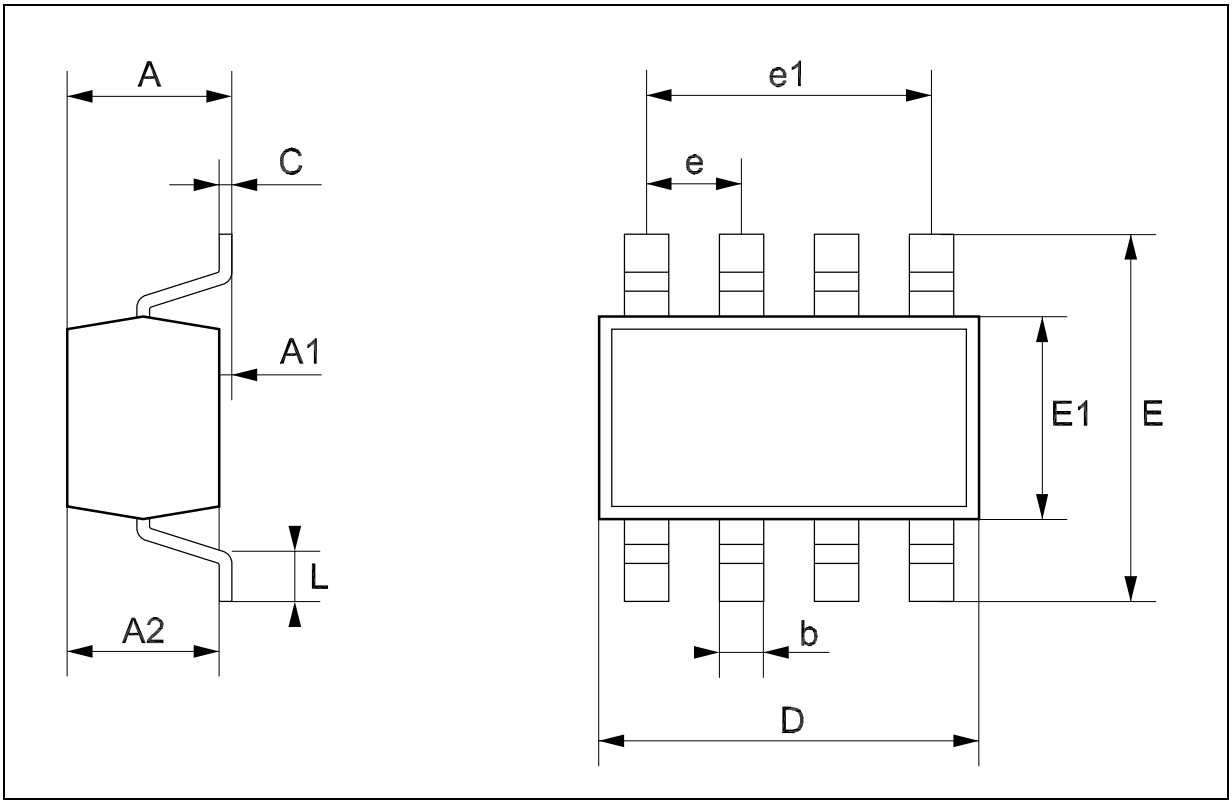
SOT23-8L MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	35.4		57.1
A1	0.00		0.15	0.0		5.9
A2	0.90		1.30	35.4		51.2
b	0.22		0.38	8.6		14.9
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	2.60		3.00	102.3		118.1
E1	1.50		1.75	59.0		68.8
e	0	.65			25.6	
e1		1.95			76.7	
L	0.35		0.55	13.7		21.6



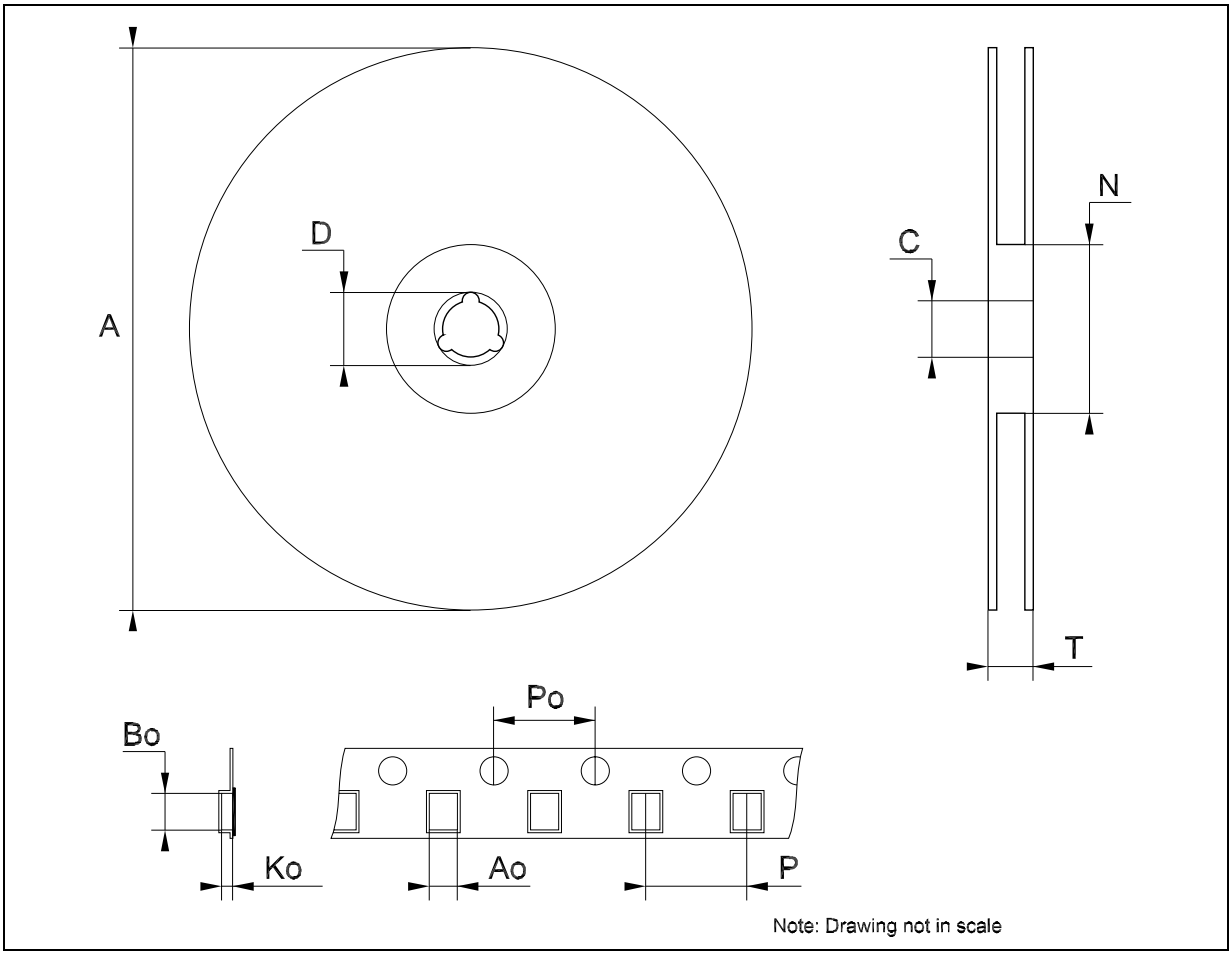
SOT323-8L MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80		1.10	31.5		43.3
A1	0.00		0.10	0.0		3.9
A2	0.80		1.00	31.5		34.9
b	0.13		0.28	5.1		11.0
C	0.10		0.18	3.9		7.1
D	1.80		2.20	70.9		86.6
E	1.80		2.40	70.9		94.5
E1	1.15		1.35	45.3		53.1
e		0.5			19.7	
e1		1.5			59.0	
L	0.10		0.30	3.9		11.8



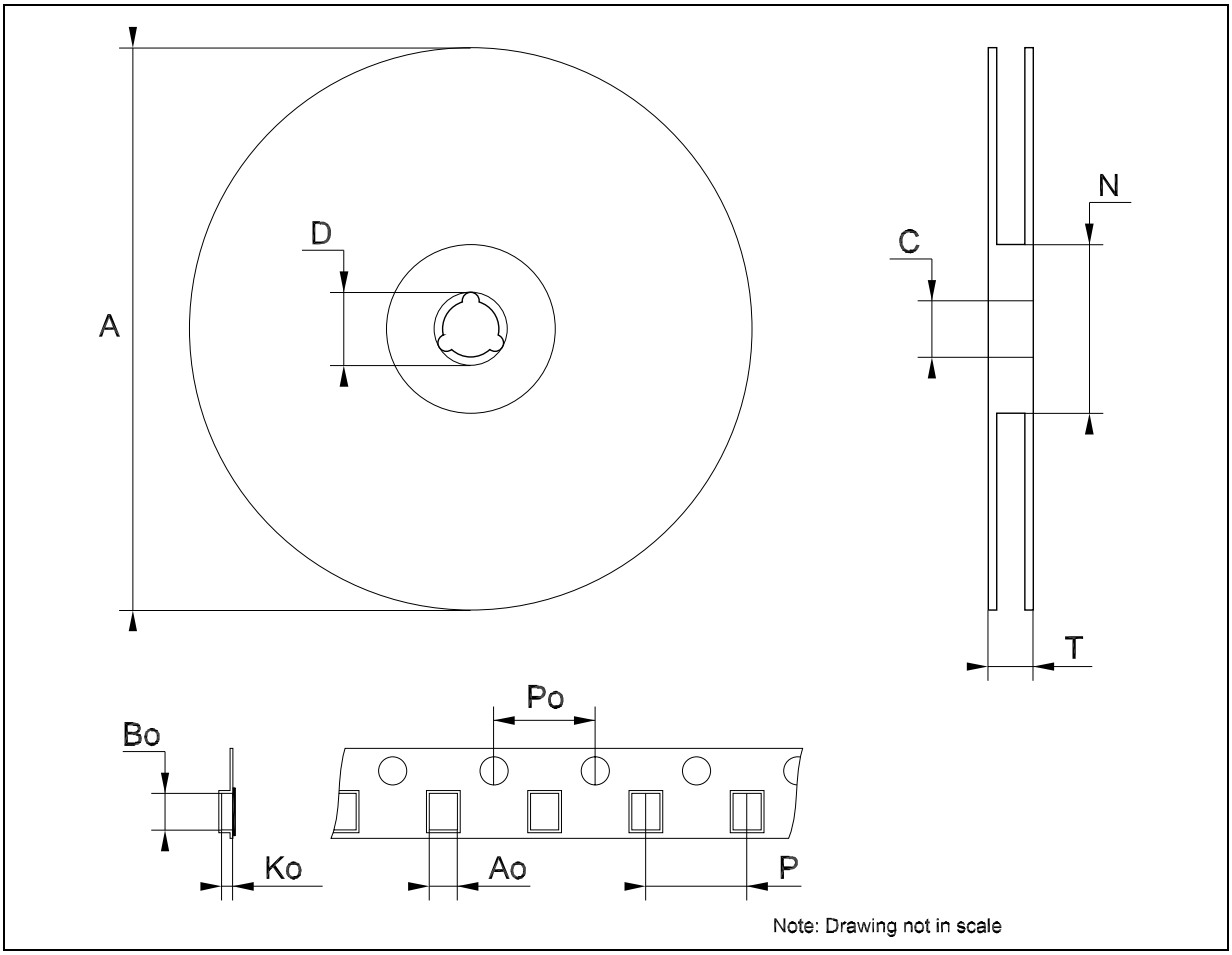
Tape & Reel SOT23-xL MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			180			7.086
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	3.13	3.23	3.33	0.123	0.127	0.131
Bo	3.07	3.17	3.27	0.120	0.124	0.128
Ko	1.27	1.37	1.47	0.050	0.054	0.0.58
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	3.9	4.0	4.1	0.153	0.157	0.161



Tape & Reel SOT323-xL MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	175	180	185	6.889	7.086	7.283
C	12.8	13	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	59.5	60	60.5		2.362	
T			14.4			0.567
Ao		2.25			0.088	
Bo		2.7			0.106	
Ko		1.2			0.047	
Po	3.98	4	4.2	0.156	0.157	0.165
P	3.98	4	4.2	0.156	0.157	0.165



Note: Drawing not in scale