RF3397

GENERAL PURPOSE AMPLIFIER

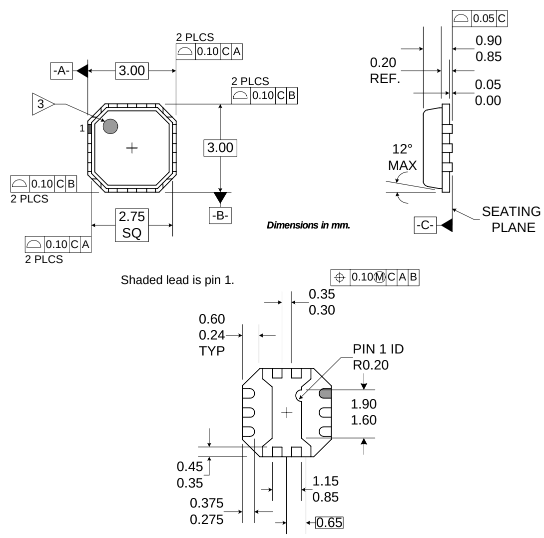
RoHS Compliant & Pb-Free Product

Typical Applications

- Basestation Applications
- Broadband, Low-Noise Gain Blocks
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Final PA for Low-Power Applications
- High Reliability Applications

Product Description

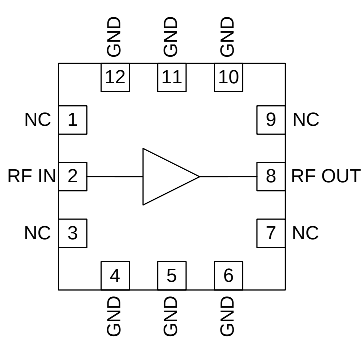
The RF3397 is a general purpose, low-cost RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily-cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 6000MHz. The device is self-contained with 50Ω input and output impedances and requires only two external DC-biasing elements to operate as specified. The device is designed for cost effective high reliability in a plastic package. The 3mmx3mm footprint is compatible with standard ceramic and plastic Micro-X packages.



Package Style: QFN, 12-Pin, 3x3

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS
- ☐ InGaP/HBT
- ☐ GaN HEMT
- ☐ SiGe Bi-CMOS



Functional Block Diagram

Features

- DC to >6000MHz Operation
- Internally Matched Input and Output
- 15.5dB Small Signal Gain
- +25.5dBm Output IP3
- +12.5dBm Output P1dB
- Footprint Compatible with Micro-X

Ordering Information

RF3397	General Purpose Amplifier
RF3397PCBA-41X	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

Parameter	Rating	Unit
Input RF Power	+13	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-60 to +150	°C
I_{CC}	60	mA

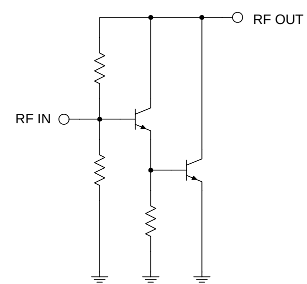
Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, I_{CC}=40mA (See Note 1.)
Frequency Range		DC to >6000		MHz	
3dB Bandwidth		4.4		GHz	
Gain	15.4	16.4		dB	Freq=500MHz
	15.3	16.3	17.3	dB	Freq=850MHz
	13.5	15.5	17.5	dB	Freq=2000MHz
		14.5		dB	Freq=3000MHz
		14.0			Freq=4000MHz
		13.5			Freq=6000MHz
Noise Figure		2.8		dB	Freq=2000MHz
Input VSWR		1.7:1			In a 50Ω system, DC to 6000MHz
Output VSWR		2:1			In a 50Ω system, DC to 6000MHz
Output IP3	24.5	25.5		dBm	Freq=850MHz
	+24.5	+25.5		dBm	Freq=2000MHz
Output P1dB	+12.0	+13.0		dBm	Freq=850MHz
	+11.5	+12.5		dBm	Freq=2000MHz
Reverse Isolation		19		dB	Freq=2000MHz
Thermal					I_{CC}=40mA, P_{DISS}=135mW. (See Note 3.)
$Theta_{JC}$		208		°C/W	V_{PIN}=3.38V
Maximum Measured Junction Temperature at DC Bias Conditions		113		°C	T_{AMB}=+85°C
Mean Time To Failures		51,709		years	T_{AMB}=+85°C
Power Supply					With 22Ω bias resistor
Device Operating Voltage	3.55	3.65	3.7	V	At pin 8 with I_{CC}=40mA
	4.2	4.5	4.8	V	At evaluation board connectors, I_{CC}=40mA
Operating Current		40	60	mA	See Note 2.

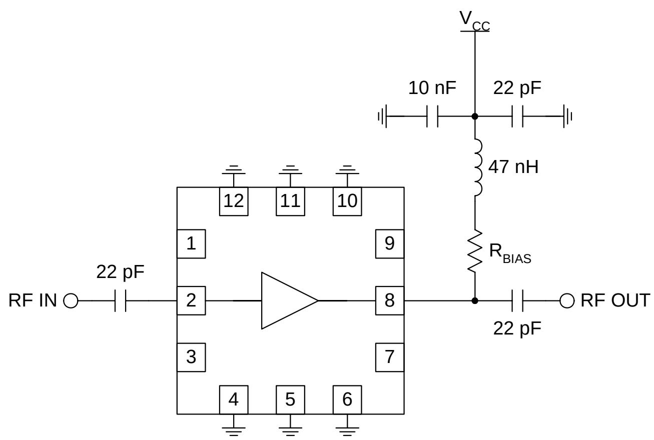
Note 1: All specification and characterization data has been gathered on standard FR-4 evaluation boards. These evaluation boards are not optimized for frequencies above 2.5GHz. Performance above 2.5GHz may improve if a high performance PCB is used.

Note 2: The RF3397 must be operated at or below 60mA in order to achieve the thermal performance stated above. Operating at 40mA will ensure the best possible combination of reliability and electrical performance.

Note 3: Because of process variations from part to part, the current resulting from a fixed bias voltage will vary. As a result, caution should be used in designing fixed voltage bias circuits to ensure the worst case bias current does not exceed 60mA over all intended operating conditions.

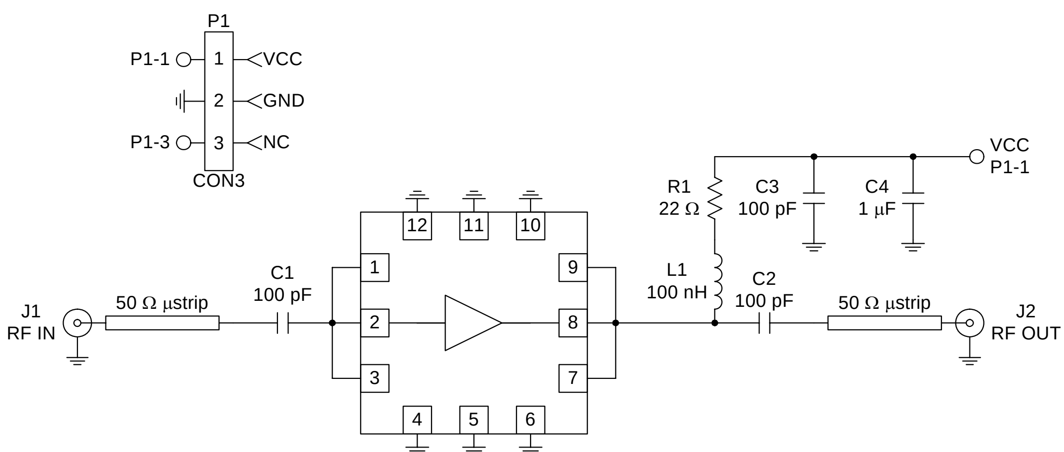
Pin	Function	Description	Interface Schematic
1	NC	No internal connections. It is not necessary to ground this pin.	
2	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
3	NC	No internal connections. It is not necessary to ground this pin.	
4	GND	Ground connection.	
5	GND	Ground connection.	
6	GND	Ground connection.	
7	NC	No internal connections. It is not necessary to ground this pin.	
8	RF OUT	RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC}. The resistor is selected to set the DC current into this pin to a desired level. The resistor value is determined by the following equation: $R = \frac{(V_{SUPPLY} - V_{DEVICE})}{I_{CC}}$ Care should also be taken in the resistor selection to **ensure that the current into the part never exceeds 60mA over the planned operating temperature**. This means that a resistor between the supply and this pin is always required, even if a supply near 3.6V is available, to provide DC feedback to prevent thermal runaway. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	
9	NC	No internal connections. It is not necessary to ground this pin.	
10	GND	Ground connection.	
11	GND	Ground connection.	
12	GND	Ground connection.	
Die Flag	GND	Ground connection. To ensure best performance, avoid placing ground vias directly beneath the part.	

Application Schematic



Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

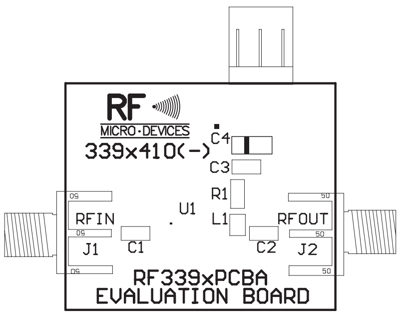


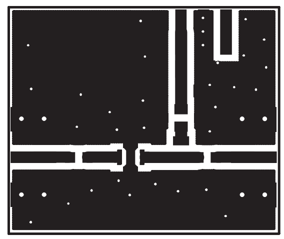
NOTE:
Evaluation board optimized for frequencies above 300 MHz and below 2.5 GHz. For operation below 300 MHz the value of inductor L1 and capcitors C1 and C2 should be increased.

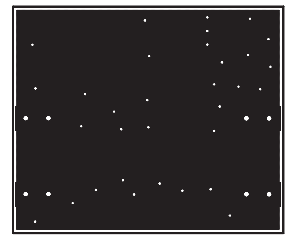
Evaluation Board Layout
Board Size 1.195" x 1.000"

Board Thickness 0.033”, Board Material FR-4

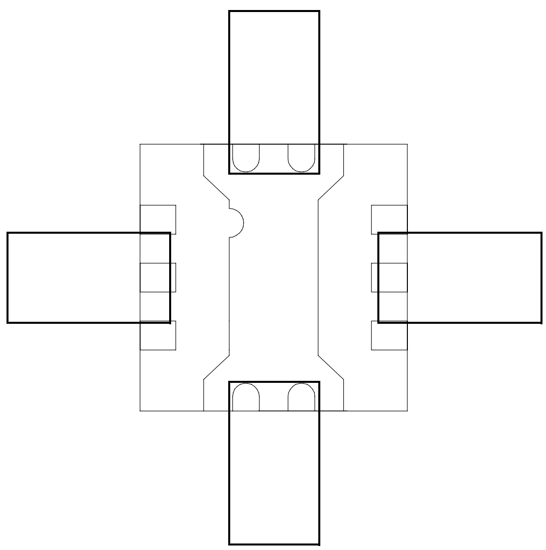
Note: A small amount of ground inductance is required to achieve datasheet performance. The necessary inductance may be generated by ensuring that no ground vias are placed directly below the footprint of the part.





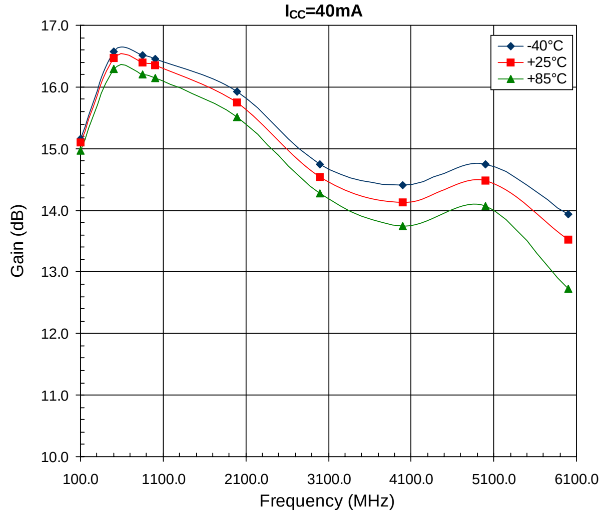


Overlay of Suggested Micro-X and 3mmx3mm Layouts Showing Compatibility



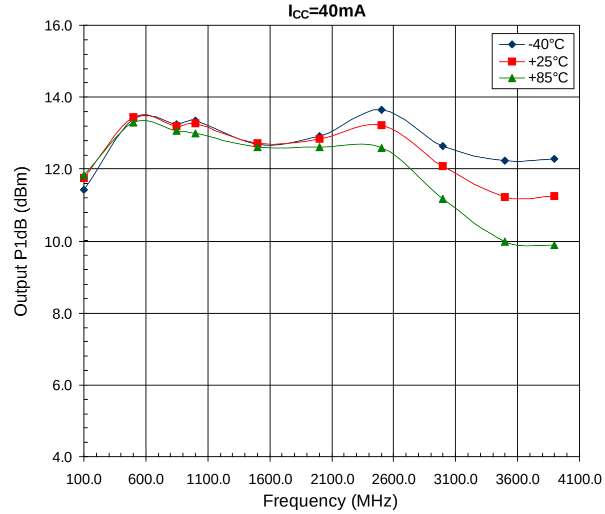
Gain versus Frequency Across Temperature

I_{CC}=40mA



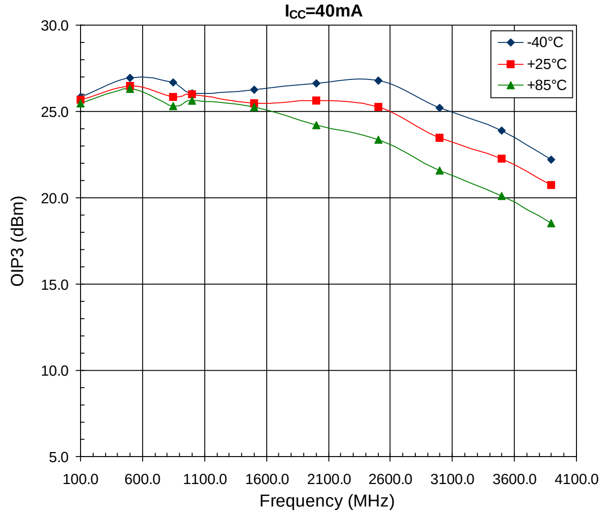
Output P1dB versus Frequency Across Temperature

I_{CC}=40mA



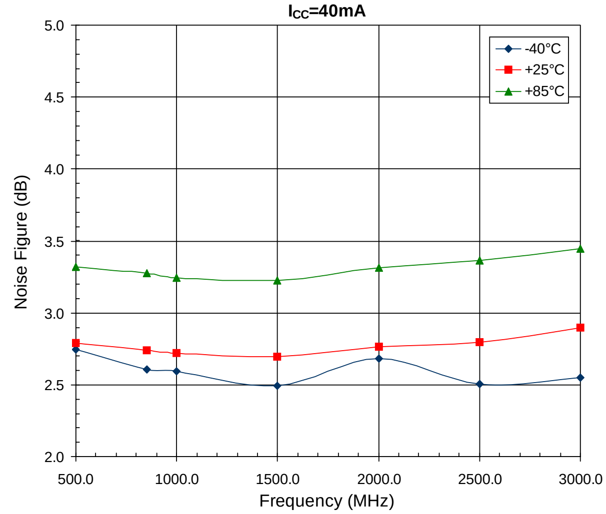
Output IP3 versus Frequency Across Temperature

I_{CC}=40mA



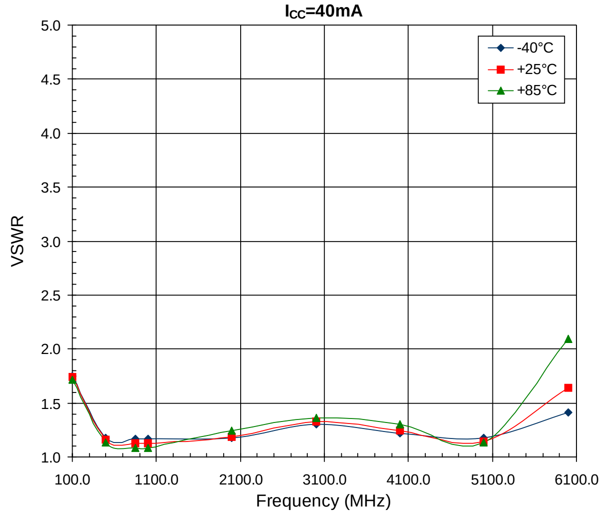
Noise Figure versus Frequency Over Temperature

I_{CC}=40mA



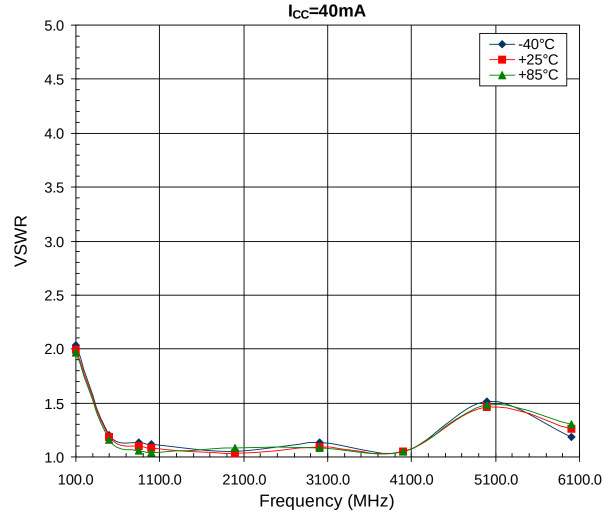
Input VSWR versus Frequency Across Temperature

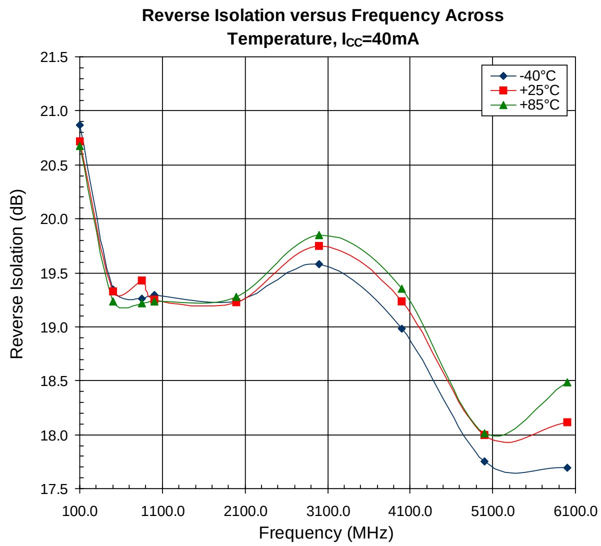
I_{CC}=40mA

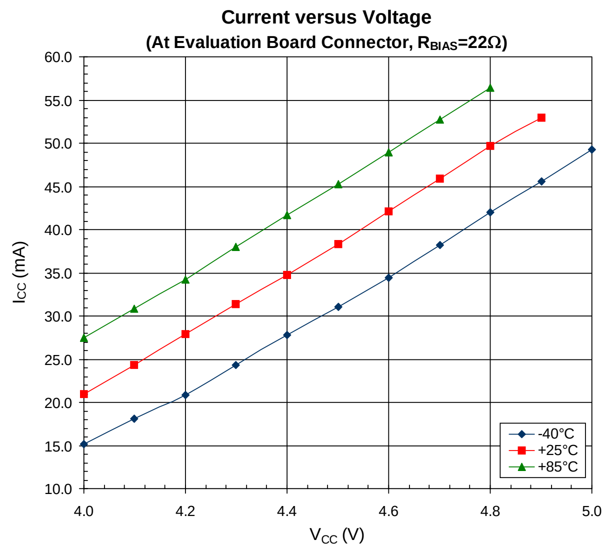


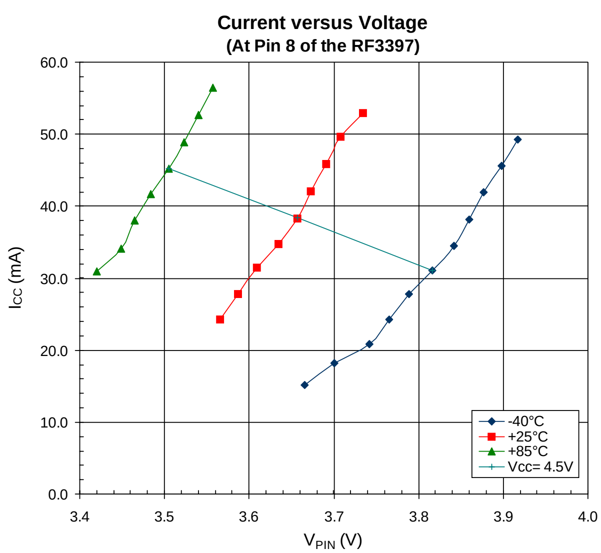
Output VSWR versus Frequency Across Temperature

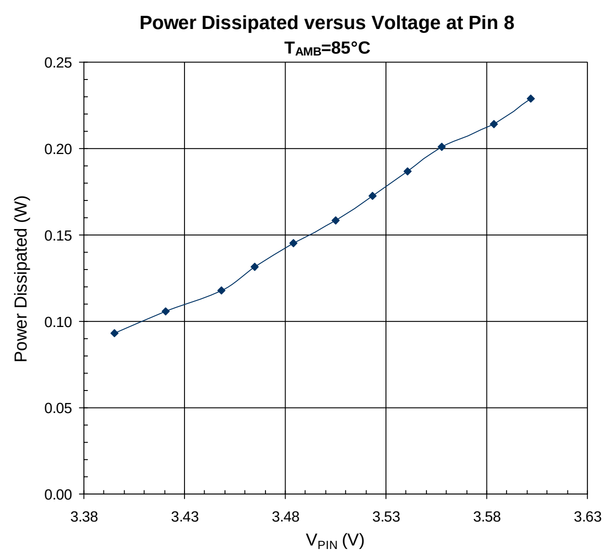
I_{CC}=40mA

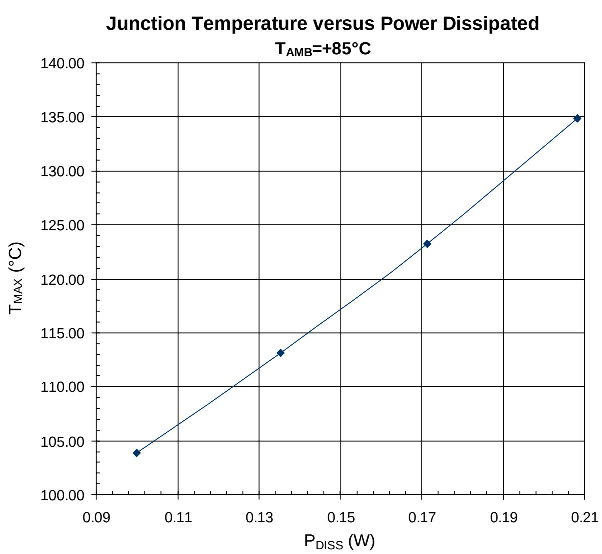



Reverse Isolation versus Frequency Across Temperature, I_{CC}=40mA
Reverse Isolation (dB)
Frequency (MHz)
-40°C
+25°C
+85°C


Current versus Voltage
(At Evaluation Board Connector, R_{BIAS}=22Ω)
I_{CC} (mA)
V_{CC} (V)
-40°C
+25°C
+85°C


Current versus Voltage
(At Pin 8 of the RF3397)
I_{CC} (mA)
V_{PIN} (V)
-40°C
+25°C
+85°C
Vcc= 4.5V


Power Dissipated versus Voltage at Pin 8
T_{AMB}=85°C
Power Dissipated (W)
V_{PIN} (V)


Junction Temperature versus Power Dissipated
T_{AMB}=+85°C
T_{MAX} (°C)
P_{DISS} (W)

PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is Electroless Nickel, immersion Gold. Typical thickness is 3μinch to 8μinch Gold over 180μinch Nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Mask Pattern

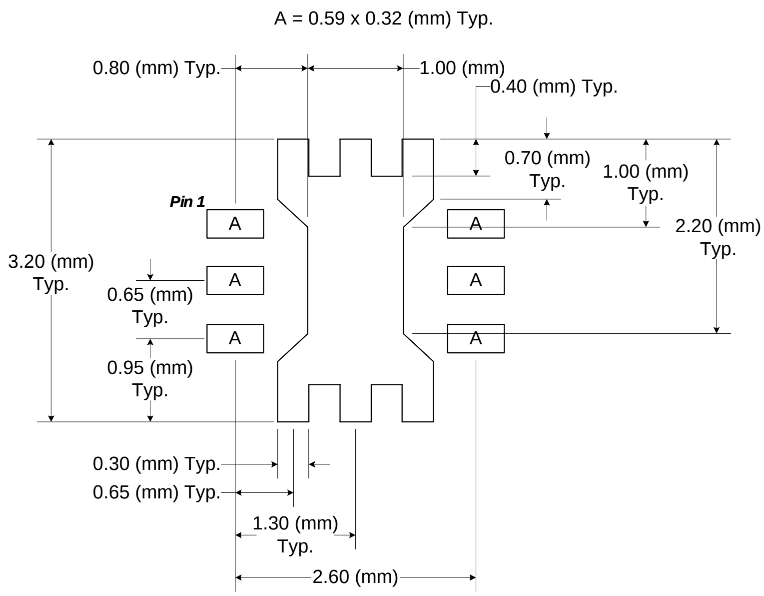


Figure 1. PCB Metal Land Pattern (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

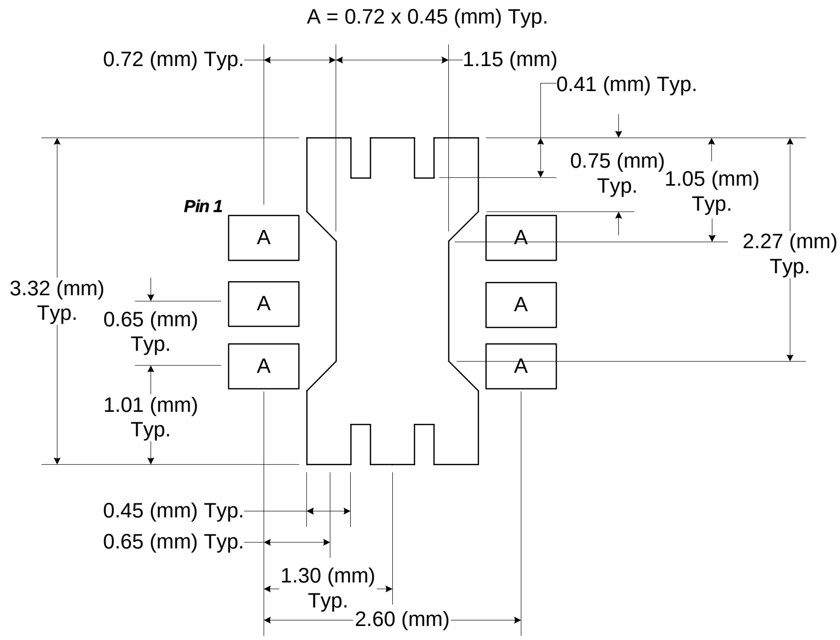


Figure 2. PCB Solder Mask (Top View)

Thermal Pad and Via Design

The PCB metal land pattern has been designed with a thermal pad that matches the exposed die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

NOTE: A small amount of ground inductance is required to achieve data sheet performance. The necessary inductance may be generated by ensuring that no ground vias are placed directly below the footprint of the part.