National Semiconductor

March 1988

MM54C89/MM74C89 64-Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C89/MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register latches the address information on the positive to negative transition of the memory enable input. The four TRI-STATE data output lines working in conjunction with the memory enable input provide for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note: The timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

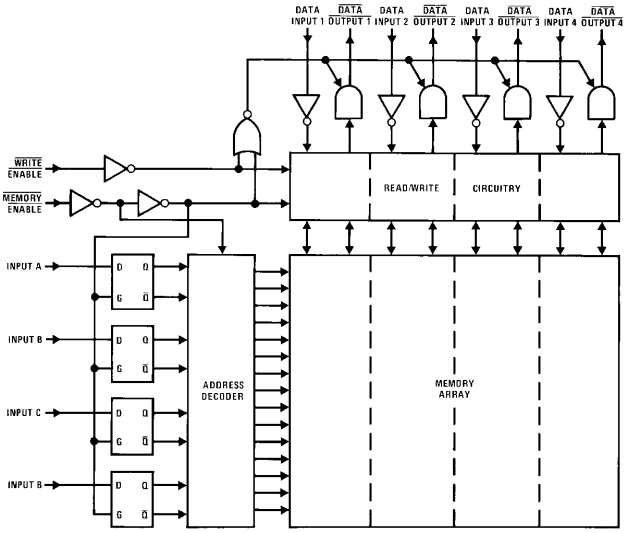
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

When the device is writing or disabled the output assumes a TRI-STATE (Hi-z) condition.

Features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L
- Low power consumption — 100 nW/package (typ.)
- Fast access time — 130 ns (typ.) at V_{CC} = 10V
- TRI-STATE output

Logic and Connection Diagrams



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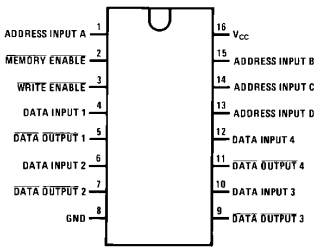
Dual-In-Line Package



Top View TL/F/5888–2

Order Number MM54C89 or MM74C89

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RRD-B30M105/Printed in U. S. A.

MM54C89/MM74C89 64-Bit TRI-STATE Random Access Read/Write Memory

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C89	−55°C to +125°C
MM74C89	−40°C to +85°C
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10 μA V_{CC} = 10V, I_O = −10 μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = +10 μA V_{CC} = 10V, I_O = +10 μA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		−0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{OZ}	Output Current in High Impedance State	V_{CC} = 15V, V = 15V V_{CC} = 15V, V_O = 0V	 −1.0	0.005 −0.005	1.0	μA μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −360 μA 74C, V_{CC} = 4.75V, I_O = −360 μA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = +360 μA 74C, V_{CC} = 4.75V, I_O = +360 μA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* T_A = 25°C, C_L = 50 pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay from Memory Enable	V_{CC} = 5V V_{CC} = 10V		270 100	500 220	ns ns
t_{ACC}	Access Time from Address Input	V_{CC} = 5V V_{CC} = 10V		350 130	650 280	ns ns
t_{SA}	Address Setup Time	V_{CC} = 5V V_{CC} = 10V	150 60			ns ns
t_{HA}	Address Hold Time	V_{CC} = 5V V_{CC} = 10V	60 40			ns ns
t_{ME}	Memory Enable Pulse Width	V_{CC} = 5V V_{CC} = 10V	400 150	250 90		ns ns

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{SR}	Write Enable Setup Time for a Read	$V_{CC} = 5V$ $V_{CC} = 10V$	0 0			ns ns
t_{WS}	Write Enable Setup Time for a Write	$V_{CC} = 5V$ $V_{CC} = 10V$			t_{ME} t_{ME}	ns ns
t_{WE}	Write Enable Pulse Width	$V_{CC} = 5V$, $t_{WS} = 0$ $V_{CC} = 10V$, $t_{WS} = 0$	300 100	160 60		ns ns
t_{HD}	Data Input Hold Time	$V_{CC} = 5V$ $V_{CC} = 10V$	50 25			ns ns
t_{SD}	Data Input Setup	$V_{CC} = 5V$ $V_{CC} = 10V$	50 25			ns ns
t_{1H}, t_{0H}	Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from Memory Enable	$V_{CC} = 5V$, $C_L = 5$ pF, $R_L = 10k$ $V_{CC} = 10V$, $C_L = 5$ pF, $R_L = 10k$		180 −85	300 120	ns ns
t_{1H}, t_{0H}	Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from Write Enable	$V_{CC} = 50V$, $C_L = 5$ pF, $R_L = 10k$ $V_{CC} = 10V$, $C_L = 5$ pF, $R_L = 10k$		180 85	300 120	ns ns
C_{IN}	Input Capacity	Any Input (Note 2)		5		pF
C_{OUT}	Output Capacity	Any Output (Note 2)		6.5		pF
C_{PD}	Power Dissipation Capacity	(Note 3)		230		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

AC Electrical Characteristics* Guaranteed across the specified temperature range, $C_L = 50$ pF

Parameter	Conditions	MM54C89 $T_A = -55°C$ to $+125°C$		MM74C89 $T_A = -40°C$ to $+85°C$		Units
		Min	Max	Min	Max	
t_{PD}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$		700 310 250		600 265 210	ns ns ns
t_{ACC}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$		910 400 320		780 345 270	ns ns ns
t_{SA}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	210 90 70		180 80 60		ns ns ns
t_{HA}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	80 55 45		70 50 40		ns ns ns
t_{ME}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	560 210 170		480 180 150		ns ns ns
t_{WE}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	420 140 110		360 120 100		ns ns ns
t_{HD}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	70 35 30		60 30 25		ns ns ns

*AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics*

Guaranteed across the specified temperature range, C_L = 50 pF (Continued)

Parameter	Conditions	MM54C89 T_A = −55°C to +125°C		MM74C89 T_A = −40°C to +85°C		Units
		Min	Max	Min	Max	
t_{SD}	V_{CC} = 5V	70		60		ns
	V_{CC} = 10V	35		30		ns
	V_{CC} = 15V	30		25		ns
t_{1H}, t_{0H}	V_{CC} = 5V		420		360	ns
	V_{CC} = 10V, C_L = 5 pF		170		145	ns
	V_{CC} = 15V, R_L = 10 kΩ		135		115	ns

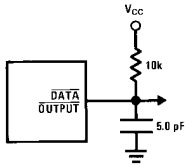
*AC Parameters are guaranteed by DC correlated testing.

Truth Table

ME	WE	Operation	Condition of Outputs
L	L	Write	TRI-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE
H	H	Inhibit, Storage	TRI-STATE

AC Test Circuits

t_{0H}



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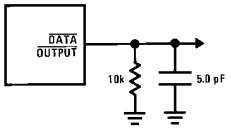
t_{1H}



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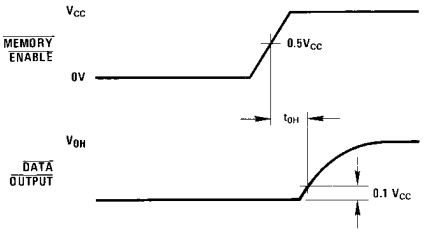
Switching Time Waveforms

t_{0H}



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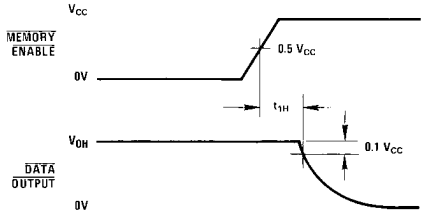
t_{1H}



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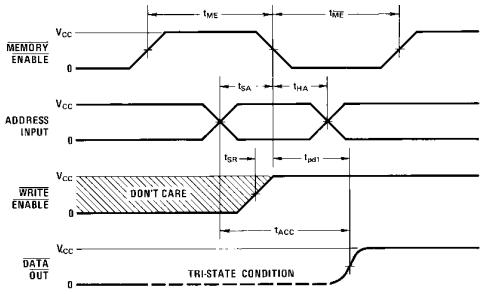
Read Cycle



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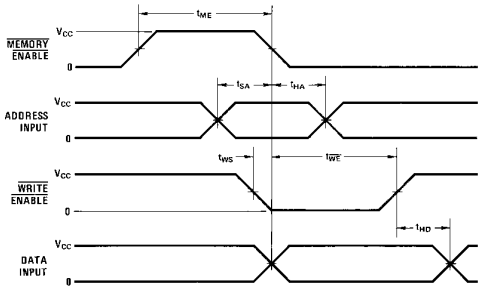
Write Cycle



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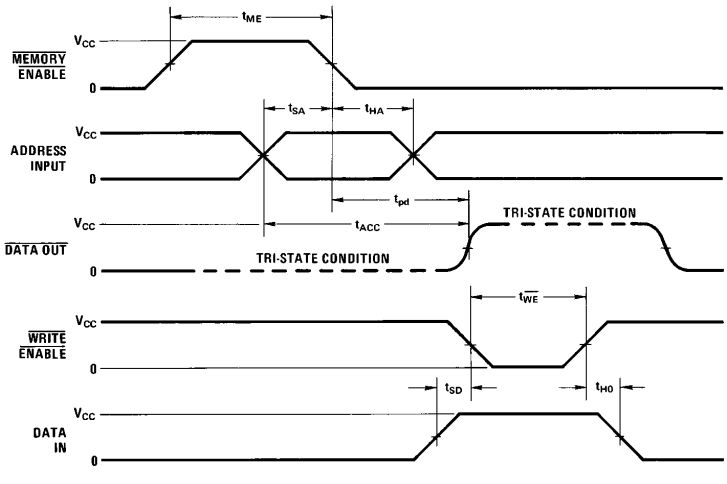
Switching Time Waveforms (Continued)

Read Modify Write Cycle



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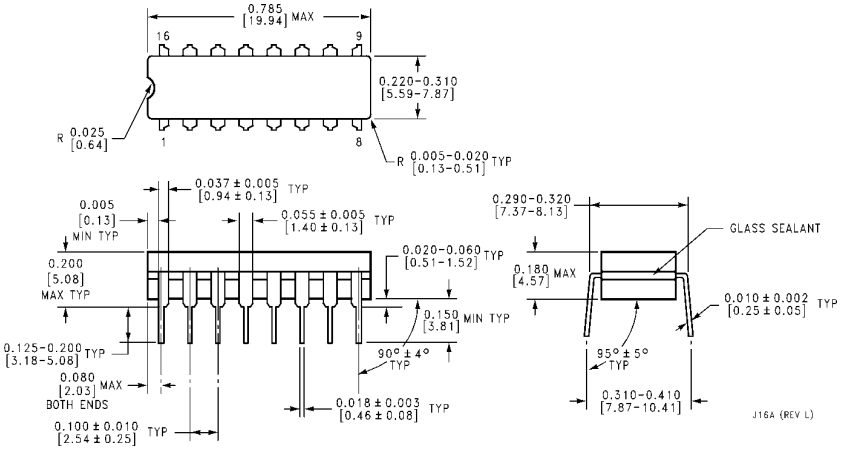
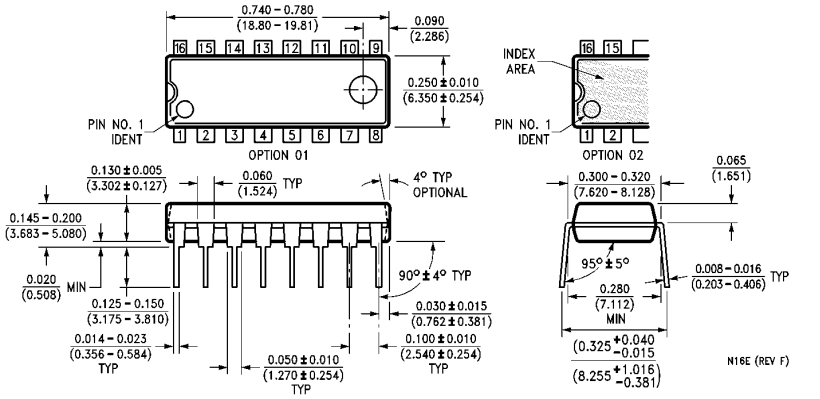
Note: t_r = 60 ns
t_f = 10 ns

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54C89J or MM74C89J
NS Package Number J16A



Molded Dual-In-Line Package (N)
Order Number MM54C89N or MM74C89N
NS Package Number N16E

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