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May 1997

HC-5504DLC

SLIC

Subscriber Line Interface Circuit

Features

- Pin for Pin Replacement for the HC-5504
- Capable of +5V or +12V (V_{B+}) Operation
- Monolithic Integrated Device
- DI High Voltage Process
- Compatible With Worldwide PBX Performance Requirements
- Controlled Supply of Battery Feed Current for Short Loops (41mA)
- Internal Ring Relay Driver
- Allows Interfacing With Negative Superimposed Ringing Systems
- Low Power Consumption During Standby
- Switch Hook Ground Key and Ring Trip Detection Functions
- Selective Denial of Power to Subscriber Loops

Applications

- Solid State Line Interface Circuit for Analog and Digital PBX Systems
- Direct Inward Dial (DID) Trunks
- Voice Messaging PBXs
- Allows Multi-Phone Operation

Description

The Intersil SLIC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents. Using the unique Intersil dielectric isolation process, the SLIC can operate directly with a wide range of station battery voltages.

The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

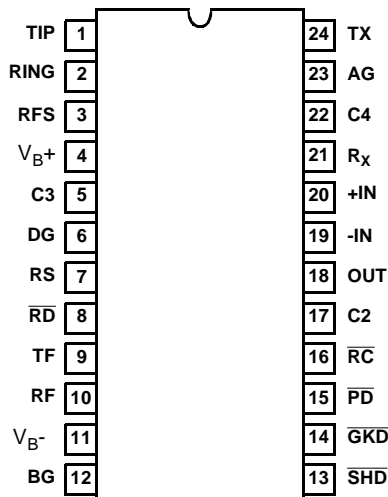
The Intersil SLIC is ideally suited for the design of new digital PBX systems by eliminating bulky hybrid transformers.

Ordering Information

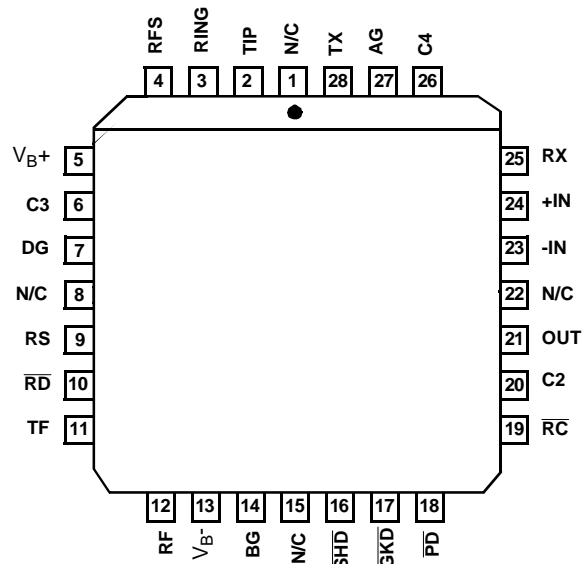
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HC1-5504DLC-5	0° to +75°C	24 Lead Ceramic DIP
HC1-5504DLC-9	-40° to +85°C	24 Lead Ceramic DIP
HC3-5504DLC-5	0° to +75°C	24 Lead Plastic DIP
HC3-5504DLC-9	-40° to +85°C	24 Lead Plastic DIP
HC4P5504DLC-5	0° to +75°C	28 Lead PLCC
HC4P5504DLC-9	-40° to +85°C	28 Lead PLCC
HC9P5504DLC-5	0° to +75°C	24 Lead SOIC
HC9P5504DLC-9	-40° to +85°C	24 Lead SOIC

Pinouts

HC-5504DLC (PDIP, CDIP, SOIC)
TOP VIEW



HC-5504DLC (PLCC)
TOP VIEW



Specifications HC-5504DLC

Absolute Maximum Ratings (Note 1)

Maximum Continuous Supply Voltages

(V _{B-})	-60 to +0.5 V
(V _{B+})	-0.5 to +15 V
(V _{B+} - V _{B-})	+75V
Relay Drive Voltage (V _{RD})	-0.5 to +15V
Junction Temperature Ceramic	+175°C
Junction Temperature Plastic	+150°C
Lead Temperature (Soldering 10 Sec.)	+300°C

Operating Conditions

Operating Temperature Range

HC-5504DLC-5	0°C to +75°C
HC-5504DLC-9	-40°C to +85°C
Storage Temperature Range	-65°C to 150°C
Relay Driver Voltage (V _{RD})	+5 to +12V
Positive Supply Voltage (V _{B+})	4.75 to 5.25 or 10.8 to 13.2V
Negative Supply Voltage (V _{B-})	-42 to -58V
High Level Logic Input Voltage	2.4V
Low Level Logic Input Voltage	0.6V
Loop Resistance (R _L)	200 to 1200Ω

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Unless Otherwise Specified, V_{B-} = -48V, V_{B+} = +12V and +5V, AG = BG = DG = 0V, Typical Parameters T_A = +25°C. Min-Max Parameters are Over Operating Temperature Range.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	I _{LONG} * = 0, V _{B+} = +12V	-	170	235	mW
Off Hook Power Dissipation	R _L = 600Ω, I _{LONG} * = 0, V _{B+} = +12V	-	425	550	mW
Off Hook IB+	R _L = 600Ω, I _{LONG} * = 0, T _A = -40°C	-	-	6.0	mA
Off Hook IB+	R _L = 600Ω, I _{LONG} * = 0, T _A = +25°C	-	-	5.3	mA
Off Hook IB-	R _L = 600Ω, I _{LONG} * = 0	-	35	41	mA
Off Hook Loop Current	R _L = 1200Ω, I _{LONG} * = 0	-	21	-	mA
Off Hook Loop Current	R _L = 1200Ω, V _{B-} = -42V, I _{LONG} * = 0 T _A = +25°C	17.5	-	-	mA
Off Hook Loop Current	R _L = 200Ω, I _{LONG} * = 0	36	41	48	mA
Fault Currents					
TIP to Ground		-	14	-	mA
RING to Ground		-	55	-	mA
TIP to RING		-	41	-	mA
TIP and RING to Ground		-	55	-	mA
Ring Relay Drive V _{OL}	I _{OL} = 62mA	-	0.2	0.5	V
Ring Relay Driver Off Leakage	V _{RD} = +12V, \overline{RC} = 1 = HIGH, T _A = +25°C	-	-	100	μA
Ring Trip Detection Period	R _L = 600Ω	-	2	3	Ring Cycles
On Hook Ringing Current		-	-	30	mApk
Switch Hook Detection Threshold	\overline{SHD} = V _{OL}	18	-	-	mA
	\overline{SHD} = V _{OH}	-	-	12	mA
Ground Key Detection Threshold	\overline{GKD} = V _{OL}	20	-	-	mA
	\overline{GKD} = V _{OH}	-	-	10	mA
Loop Current During Power Denial	R _L = 200Ω	-	±2	-	mA
Dial Pulse Distortion		0	-	5	ms
Receive Input Impedance	(Note 2)	-	110	-	kΩ
Transmit Output Impedance	(Note 2)	-	10	20	Ω
Two Wire Return Loss	(Referenced to 600Ω + 2.16μF), (Note 2)				
SR _L LO		-	15.5	-	dB
ER _L		-	24	-	dB
SR _L HI		-	31	-	dB
Longitudinal Balance	1V _{RMS} 200Hz - 3400Hz, (Note 2) IEEE Method				
2 Wire Off Hook		58	65	-	dB
2 Wire On Hook		60	63	-	dB
4 Wire Off Hook	0°C ≤ T _A ≤ +75°C	50	58	-	dB

Specifications HC-5504DLC

Electrical Specifications

Unless Otherwise Specified, $V_{B-} = -48V$, $V_{B+} = +12V$ and $+5V$, $AG = BG = DG = 0V$, Typical Parameters $T_A = +25^{\circ}C$. Min-Max Parameters are Over Operating Temperature Range. (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Low Frequency Longitudinal Balance	R.E.A. Method, (Note 2), $R_L = 600\Omega$ $0^{\circ}C \leq T_A \leq +75^{\circ}C$	-	-	23	dBrnC
		-	-	-67	dBmOp
Insertion Loss 2 Wire - 4 Wire, 4 Wire - 2 Wire	at 1kHz, 0dBm Input Level, Referenced 600 Ω	-	± 0.05	± 0.2	dB
Frequency Response	200 - 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level (Note 2)	-	± 0.02	± 0.05	dB
Idle Channel Noise 2 Wire - 4 Wire, 4 Wire - 2 Wire	(Note 2)	-	1	5	dBrnC
		-	-89	-85	dBmOp
Absolute Delay 2 Wire - 4 Wire, 4 Wire - 2 Wire	(Note 2)	-	-	2	ms
Trans Hybrid Loss	Balance Network Set Up for 600 Ω Termination at 1kHz	36	40	-	dB
Overload Level 2 Wire - 4 Wire, 4 Wire - 2 Wire	$V_{B+} = +5V$	1.5	-	-	Vpeak
	$V_{B+} = +12V$	1.75	-	-	Vpeak
Level Linearity 2 Wire - 4 Wire, 4 Wire - 2 Wire	At 1kHz, (Note 2) Referenced to 0dBm Level +3 to -40dBm	-	-	± 0.05	dB
	-40 to -50dBm	-	-	± 0.1	dB
	-50 to -55dBm	-	-	± 0.3	dB
Power Supply Rejection Ratio V_{B+} to 2 Wire V_{B+} to Transmit V_{B-} to 2 Wire V_{B-} to Transmit	(Note 2) 30 - 60Hz, $R_L = 600\Omega$	15	-	-	dB
		15	-	-	dB
		15	-	-	dB
		15	-	-	dB
V_{B+} to 2 Wire V_{B+} to Transmit V_{B-} to 2 Wire V_{B-} to Transmit	200 - 16kHz $R_L = 600\Omega$	30	-	-	dB
		30	-	-	dB
		30	-	-	dB
		30	-	-	dB
Logic Input Current (RS, \overline{RC} , \overline{PD})	$0V \leq V_{IN} \leq +5V$	-	-	± 100	μA
Logic Inputs Logic '0' V_{IL} Logic '1' V_{IH}		-	-	0.8	V
		2.0	-	5.5	V
Logic Outputs Logic '0' V_{OL} Logic '1' V_{OH}	$I_{LOAD} 800\mu A$, $V_{B+} = +12V$, $+5V$	-	0.1	0.5	V
		2.7	5.0	5.5	V
	$I_{LOAD} 40\mu A$, $V_{B+} = +5V$	2.7	-	5.0	V

* I_{LONG} = Longitudinal Current

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

Specifications HC-5504DLC

Uncommitted Op Amp Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		-	± 5	-	mV
Input Offset Current		-	± 10	-	nA
Input Bias Current		-	20	-	nA
Differential Input Resistance	(Note 2)	-	1	-	M Ω
Output Voltage Swing	$R_L = 10K, V_{B+} = +12V$	-	± 5	-	V_{PEAK}
	$R_L = 10K, V_{B+} = +5V$	-	± 3	-	V_{PEAK}
Output Resistance	$A_{VCL} = 1$ (Note 2)	-	10	-	Ω
Small Signal GBW	(Note 2)	-	1	-	MHz

Pin Descriptions

28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
2	1	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a 150 Ω feed resistor and a ring relay contact. Functions with the Ring terminal to receive voice signals from the telephone and for loop monitoring purposes.
3	2	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a 150 Ω feed resistor and a ring relay contact. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.
4	3	RFS	Senses ring side of loop for ground key and ring trip detection. During ringing, the ring signal is inserted into the line at this node and RF is isolated from RFS via a relay.
5	4	V_{B+}	Positive Voltage Source - Most positive supply. V_{B+} is typically 12V or 5V.
6	5	C3	Capacitor #3 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering V_{B-} . Typical value is 0.3 μ F, 30V.
7	6	DG	Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC microcircuit.
9	7	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock should be arranged such that a positive pulse transition occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring relay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to +5V.
10	8	RD	Relay Driver - A low active open collector logic output. When enabled, the external ring relay is energized.
11	9	TF	Tip Feed - A low impedance analog output connected to the TIP terminal through a 150 Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
12	10	RF	Ring Feed - A low impedance analog output connected to the RING terminal through a 150 Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
13	11	V_{B-}	Negative Voltage Source - Most negative supply. V_{B-} is typically -48V with an operational range of -42V to -58V. Frequently referred to as "battery".
14	12	BG	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
16	13	\overline{SHD}	Switch Hook Detection - A low active LS TTL - compatible logic output.
17	14	\overline{GKD}	Ground Key Detection - A low active LS TTL - compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA, and disabled if this current difference is below an internally set threshold.
18	15	\overline{PD}	Power Denial - A low active TTL - Compatible logic input. When enabled, the switch hook detect (\overline{SHD}) and ground key detect (\overline{GKD}) are not necessarily valid, and the relay driver (\overline{RD}) output is disabled.

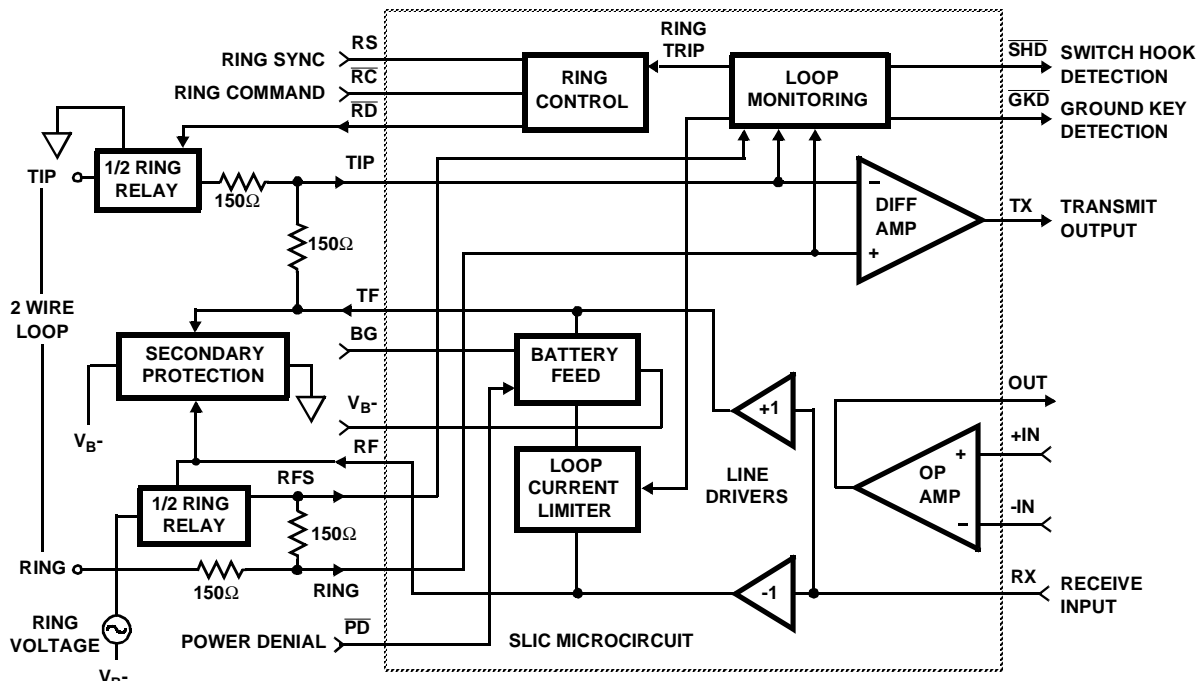
Specifications HC-5504DLC

Pin Descriptions (Continued)

28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
19	16	RC	Ring Command - A low active TTL - Compatible logic input. When enabled, the relay driver (RD) output goes low on the next high level of the ring sync (RS) input, as long as the SLIC is not in the power denial state ($\overline{PD} = 0$) or the subscriber is not already off-hook ($\overline{SHD} = 0$).
20	17	C2	Capacitor #2 - An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is $0.15\mu\text{F}$, 10V. This capacitor is not used if ground key function is not required and (Pin 17) may be left open or connected to digital ground.
21	18	OUT	The analog output of the spare operational amplifier. The output voltage swing is typically $\pm 5\text{V}$.
23	19	-IN	The inverting analog input of the spare operational amplifier.
24	20	+IN	The non-inverting analog input of the spare operational amplifier.
25	21	RX	Receive Input, Four Wire Side - A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed terminals, which in turn drive tip and ring through 300Ω of feed resistance on each side of the line.
26	22	C4	Capacitor #4 - An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from near by power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is $0.5\mu\text{F}$, to $1.0\mu\text{F}$, 20V. This capacitor should be nonpolarized.
27	23	AG	Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
28	24	TX	Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.
1,8,15,22		NC	No Internal Connection.

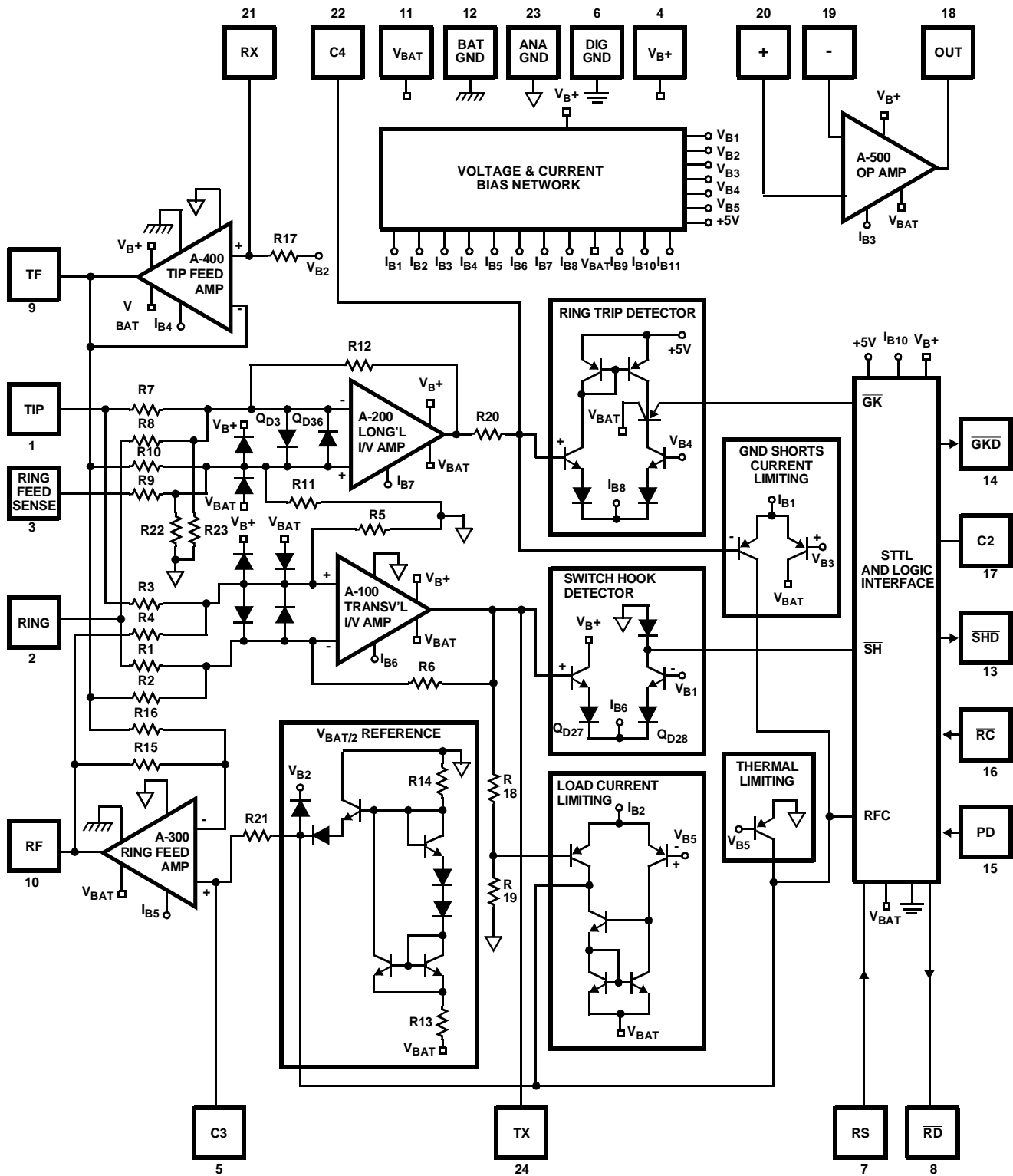
NOTE: All grounds (AG, BG, & DG) must be applied before V_{B+} or V_{B-} . Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Functional Diagram



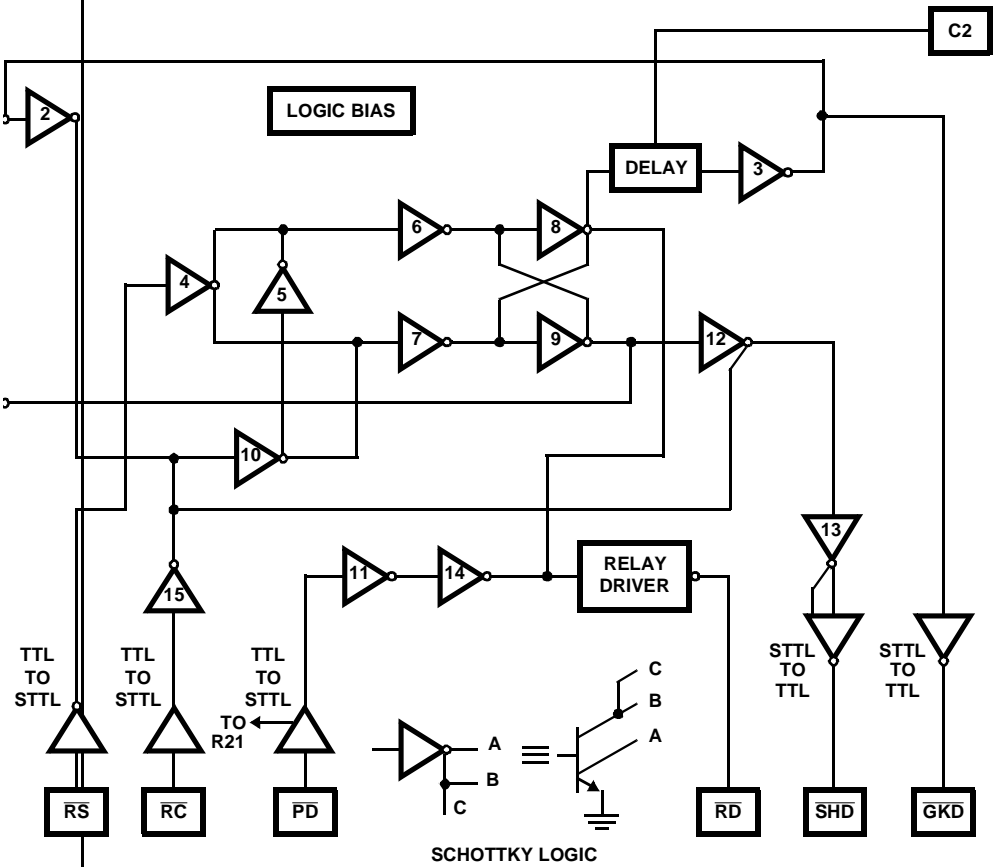
Schematic

SLIC FUNCTIONAL SCHEMATIC
(DIP/SOIC PIN NUMBERS SHOWN)



continued)

LOGIC GATE SCHEMATIC



Die Characteristics

Transistor Count	185	
Diode Count	36	
Die Dimensions	137 x 102	
Substrate Potential	Connected	
Process	Bipolar-DI	
Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	52	15
Plastic DIP	52	22
PLCC	67	29
SOIC	76	24

Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.
The SLIC will withstand longitudinal currents up to a maximum of 30mArms, 15mArms per leg, without any performance degradation.

TABLE 1

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/	±1000 (Plastic)	V _{PEAK}
	1000µs/Fall	±500 (Ceramic)	V _{PEAK}
Metallic Surge	10µs Rise/	±1000 (Plastic)	V _{PEAK}
	1000µ Fall	±500 (Ceramic)	V _{PEAK}
T/GND R/GND	10µs Rise/	±1000 (Plastic)	V _{PEAK}
	1000µs Fall	±500 (Ceramic)	V _{PEAK}
50/60Hz Current T/GND R/GND	11 Cycles	700 (Plastic)	V _{RMS}
	Limited to 10Arms	350 (Ceramic)	V _{RMS}

Applications Diagram

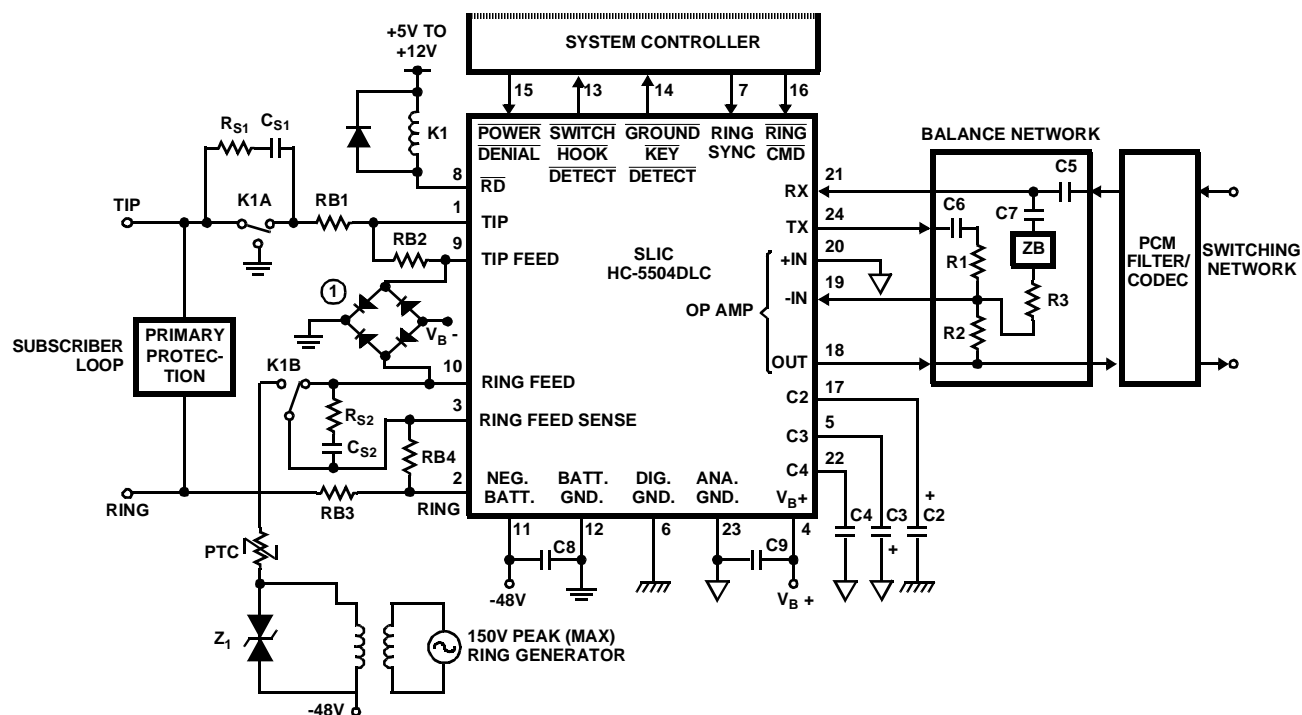


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

Typical Component Values

C2 = 0.15 μ F, 10V

C3 = 0.3 μ F, 30V

C4 = 0.5 μ F to 1.0 μ F, 10%, 20V (Should be nonpolarized)

C5 = 0.5 μ F, 20V

C6 = C7 = 0.5 μ F (10% Match Required) (Note 2)

C8 = 0.01 μ F, 100V

C9 = 0.01 μ F, 20V, \pm 20%

R1 = R2 = R3 = 100k (0.1% Match Required, 1% absolute value) ZB = 0 for 600 Ω Terminations (Note 2)

RB1 = RB2 = RB3 = RB4 = 150 Ω (0.1% Match Required, 1% absolute value)

RS1 = RS2 = 1k Ω , typically.

CS1 = CS2 = 0.1 μ F, 200V typically, depending on VRING and line length.

Z1 = 150V to 200V transient protection.

PTC used as ring generator ballast.

NOTES:

1. Secondary protection diode bridge recommended is a 2A, 200V type.
2. To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C6-R1 and R2 and C7-ZB-R3, to match in impedance to within 0.3%. Thus, if C6 and C7 are 1 μ F each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -22V step when the loop is closed. Too large a value for C6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.
A 0.5 μ F and 100k Ω gives a time constant of 50msec. The uncommitted op amp output is internally clamped to stay within \pm 5.5V and also has current limiting protection.
3. All grounds (AG, BG, & DG) must be applied before VB+ or VB-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.
4. To prevent saturation of longitudinal amplifier during ringing, the ringer current should be limited to less than 30mA peak.
5. Application shows Ring injected ringing, a Balanced or Tip injected configuration may be used.
6. Pin numbers given for DIP/SOIC package.

Additional information is contained in Application Note 549, "The HC-550X Telephone SLICs" By Geoff Phillips

