Virtex-4 ML450 Networking Interfaces Platform

User Guide

UG077 (v1.4) December 16, 2005

XILINX®

Virtex-4 ML450 Networking Interfaces Platform
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The following table shows the revision history for this document.

Date	Version	Revision
08/16/04	1.0	Initial Xilinx release.
11/02/04	1.1	Updated title of user guide. Removed references to System Monitor functions.
01/31/05	1.2	Removed references to XLVDSPro. Corrected clock descriptions in Table 3-2 to LVPECL. Removed duplicate pin entry in Table A-4.

Date	Version	Revision
08/19/05	1.3	Chapter 1 Revised Figure 1-1 Chapter 3 • Added Table 3-2, page 15 and Table 3-4, page 17. • Added text to "LVDS Loopback Cables," page 29. Chapter 4 • Added Table 4-4, page 41. Appendix A • Revised Table A-4, page 55 and Figure A-3, page 51. • Added Appendix E, "UCF File".
12/16/05	1.4	Updated Figure A-1 and Table A-3.

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Chapter 1

Introduction

About the Virtex-4 ML450 Source-Synchronous Interfaces Tool Kit

The Virtex™-4 ML450 Source-Synchronous Interfaces Tool Kit provides a complete development platform for designing and verifying applications based on the Virtex-4 LX FPGA family. This kit allows designers to implement high-speed applications with extreme flexibility using IP cores and customized modules. The Virtex-4 LX FPGA, with its column-based architecture, makes it possible to develop highly flexible networking applications.

The Virtex-4 ML450 Source-Synchronous Interfaces Tool Kit includes the following:

- Virtex-4 ML450 Networking Interfaces Development Board (XC4VLX25-FF668 FPGA)
- 5V/6.5 A DC power supply
- Country-specific power supply line cord
- RS-232 serial cable, DB9-F to DB9-F
- Four clock module daughter boards
- Two sets of precision interconnect "Blue Ribbon" loopback cables for Low Voltage Differential Signaling (LVDS) testing
- Documentation and reference design CD-ROM

Optional items that also support development efforts include:

- Xilinx ISE software
- JTAG cable, Xilinx Parallel Cable IV, or Xilinx Platform Cable USB

For assistance with any of these items, contact your local Xilinx distributor or visit the Xilinx online store at www.xilinx.com.

The heart of the Virtex-4 ML450 Source-Synchronous Interfaces Tool Kit is the ML450 Development Board. This manual provides comprehensive information on Rev 2 and later revisions of this board.

Virtex-4 ML450 Networking Interfaces Development Board

The ML450 Development Board includes the following:

- XC4VLX25-FF668 FPGA
- 32M x 16 DDR-1 SDRAM memory
- Eight clock sources:
  - 200-MHz and 250-MHz on-board oscillators
  - Four clock module connectors

  - Two sets of SMA differential clock input connectors
- One DB9-M RS-232 port
- One 64 x 128 pixel LCD
- A System ACE™ CompactFlash (CF) Configuration Controller that allows storing and downloading of up to eight FPGA configuration image files
- Four LVDS connectors (a total of 44 differential input and 44 differential output channels)
- One HyperTransport™ connector (HyperTransport Consortium DUT connector compliant)
- Onboard power regulators with ±5% output margin test capabilities

Figure 1-1 shows the ML450 Development Board.

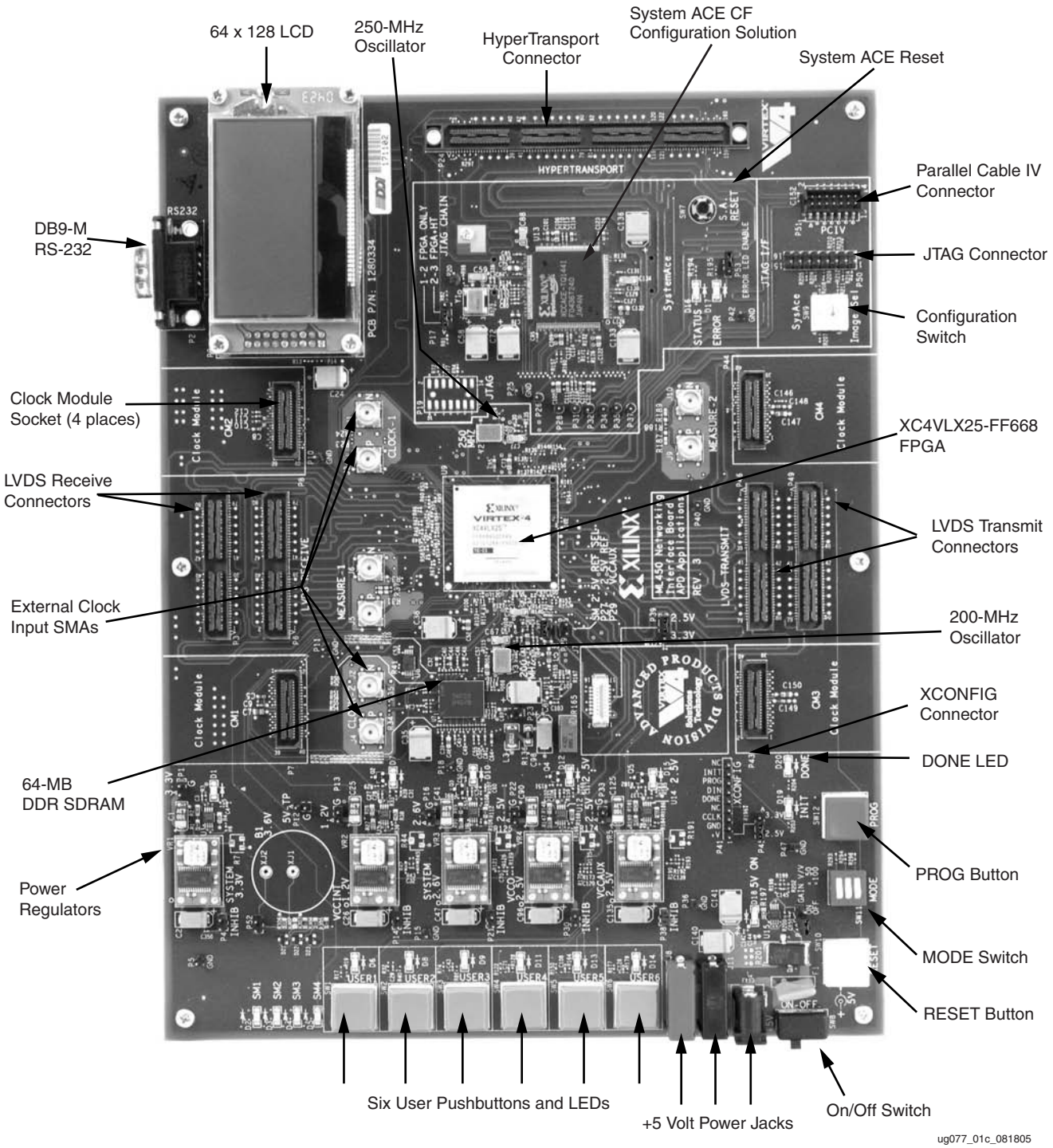


Figure 1-1: **Virtex-4 ML450 Networking Interfaces Development Board**

Chapter 2

Getting Started

This chapter describes the items needed to configure the Virtex-4 ML450 Networking Interfaces Development Board. The ML450 Development Board is tested at the factory after assembly and should be received in working condition. It is set up to load a bitstream from the CompactFlash card through the System ACE controller U13.

Documentation and Reference Design CD

The CD included in the Virtex-4 ML450 Source-Synchronous Interfaces Tool Kit contains the design files for the ML450 Development Board, including schematics, board layout, and reference design files. Open the `ReadMe.txt` file on the CD to review the list of contents.

Initial Board Checks Before Applying Power

Perform these steps before applying board power:

1. Set up the Configuration Mode Switch SW9.

   If the System ACE CF card is not used for FPGA configuration, then select one of the other modes (Master or Serial Slave modes, or JTAG mode) for device configuration using SW9. See "Configuration Modes" on page 35 for all available modes for the ML450 Development Board.

2. The JTAG chain jumper P17 must be configured to add the devices of interest to the chain, or the ISE iMPACT software will not find devices to configure. Connect P17 pins 1 and 2 to keep only the FPGA in the JTAG chain. To include the HyperTransport connector in the chain in addition to the FPGA, connect P17 pins 2 and 3. For more information see "JTAG Chain" on page 36.

3. The two ACE files (.ace) included on the Compact Flash card in the kit are:

   - DDR 400MHz Bert PRBS15 test (corresponding to SW9 position 0)
   - SDR 650MHz Bert PRBS15 test (corresponding to SW9 position 1)

In order to run the Bert GUI demonstration, please refer to documentation and files included on the kit CD. Find the UserGuide.doc in folder 3_ReferenceDesignsRev2.2. This document describes the loading of the Bert GUI files onto the host PC.

The Bert GUI should be launched and running with the DB9-M to DB9-M serial cable installed between the host PC and the ML450, before powering up the ML450 board with either SW9 position 0 or 1 selected.

4. No jumpers should be present on any of the power supply regulator modules. For more information, see "Voltage Regulators (TI PTH05000-WAH)" on page 29.

5. The ML450 Development Board has two onboard oscillators wired to the FPGA. They are available after configuration for the design to use for various system clocks. Table 3-2, page 15 lists the various clocking options.
6. Insert the CompactFlash card included in the kit into J13 on the bottom of the ML450 Development Board. To select the startup file, check that SW9 is set to position 0.

Applying Power to the Board

The ML450 Development Board is now ready to power on. The ML450 Development Board is shipped with a country-specific AC line cord for the universal input 5V desktop power supply. Follow these steps to power on the ML450 Development Board:

1. Confirm that the ON-OFF switch, SW8, is in the OFF position.
2. Plug the 5V desktop power supply into the 5V DC input barrel jack J12 on the ML450 Development Board. Plug the desktop power supply AC line cord into an electrical outlet supplying the appropriate voltage.
3. Turn ML450 Development Board SW8 to the ON position. The power indicators for all regulator modules should come on, indicating output from the regulators. The System ACE status LED D16 comes on as controller U13 extracts the .bit configuration file from the CompactFlash card to the FPGA. If no CompactFlash card is installed in the card socket J13 underneath the ML450 Development Board, the red System ACE error LED D17 flashes.
4. If a CompactFlash card is not installed in socket J13, a JTAG cable must be used to configure the FPGA. Confirm that the Mode switch SW11 is set to the JTAG configuration (101). Using a Parallel Cable IV or other JTAG pod, download the FPGA configuration bitstream into the FPGA. After the DONE LED (D20) comes on, the FPGA is configured and ready to use.

Chapter 3

Hardware Description

A high-level block diagram of the Virtex-4 ML450 Networking Interfaces Development Board is shown in Figure 3-1, followed by a brief description of each board section.

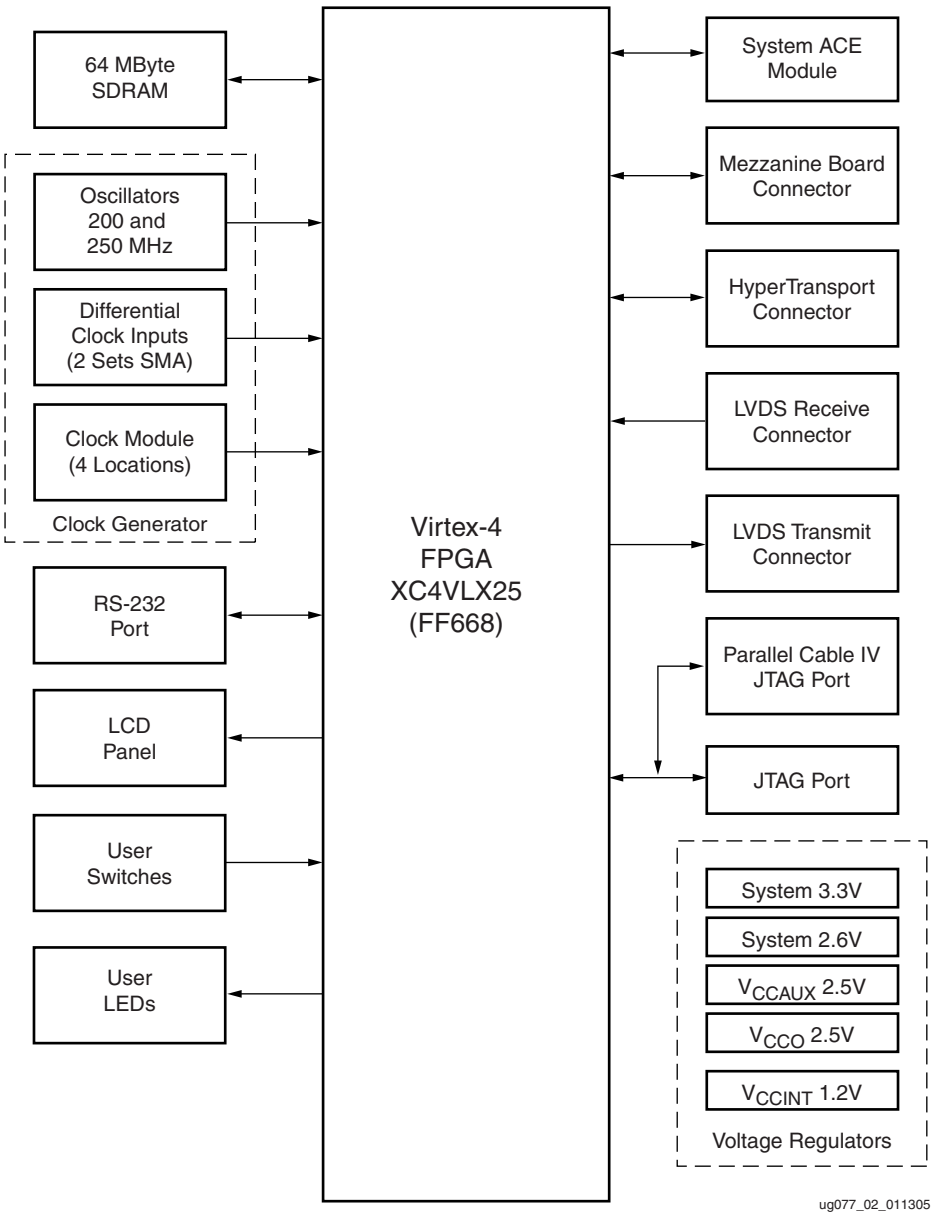


Figure 3-1: **Virtex-4 ML450 Networking Interfaces Development Board**

Clock Generation

The clock generation section of the ML450 Development Board provides all necessary clocks for the Virtex-4 FPGA. Eight clock sources are provided:

- Epson EG2121CA 2.5V 250-MHz Differential LVPECL oscillator (Y2) for HyperTransport support
- Epson EG2121CA 2.5V 200-MHz Differential LVPECL oscillator (Y3) for Virtex-4 bit delay tap support
- Two differential SMA clock inputs (CLOCK-1: J3, J1 and CLOCK-2: J4, J2)
- Four user clock sockets (CM-1: P7, CM-2: P8, CM-3: P43, CM-4:P44)

The differential SMA clock inputs are connected to the global clock inputs of the FPGA that access the upper and lower halves of the FPGA. An onboard 200-MHz oscillator calibrates the I/O delay, and an onboard 250-MHz oscillator is provided for use with the HyperTransport IP.

The four clock modules included in the kit are:

- Type A: Direct Balanced Differential SMA input
- Type B: Epson EG2121CA 2.5V 400-MHz Differential LVDS
- Type C: ICS Programmable 200 MHz to 700 MHz
- Type D: Unbalanced, Single-Ended Transformer Coupled into LVDS

The on-chip LVDS differential terminator is recommended for use in designs. The clock is received by an IBUFGDS module, and beneath that module instantiation, the synthesis attribute DIFF_TERM must be set to TRUE. Refer to the *Virtex-4 User Guide* (UG070) for information and examples using SelectIO primitives for LVDS inputs.

Note: All clock module output clocks are differential LVDS.

The clock module details are documented in Appendix C, "Clock Interfaces."

Table 3-1 shows the clock sources for the ML450 Rev 2 Board.

Table 3-1: **Clock Generation: ML450 Rev 2 Board**

	Signal Name	Pin Number	Direction	Description
Top of the Device (Bank3)	OSC1_250M_P	C13	Positive LVPECL Clock Input	Onboard 250-MHz LVPECL Oscillator
	OSC1_250M_N	C12	Negative LVPECL Clock Input	Onboard 250-MHz LVPECL Oscillator
	CLOCK-1_P	B15	Positive Differential Clock Input	SMA Connector J3
	CLOCK-1_N	B14	Negative Differential Clock Input	SMA Connector J1
	CM2_CLK_P	B13	Positive Clock Input	Dependent on Clock Module
	CM2_CLK_N	B12	Negative Clock Input	Dependent on Clock Module
	CM4_CLK_P	C15	Positive Clock Input	Dependent on Clock Module
	CM4_CLK_N	C14	Negative Clock Input	Dependent on Clock Module

Table 3-1: **Clock Generation: ML450 Rev 2 Board *(Continued)***

	Signal Name	Pin Number	Direction	Description
Bottom of the Device (Bank4)	OSC1_200M_P	AD12	Positive LVPECL Clock Input	Onboard 200-MHz LVPECL Oscillator
	OSC1_200M_N	AD11	Negative LVPECL Clock Input	Onboard 200-MHz LVPECL Oscillator
	CLOCK-2_P	AF12	Positive Differential Clock Input	SMA Connector J4
	CLOCK-2_N	AE12	Negative Differential Clock Input	SMA Connector J2
	CM1_CLK_P	AF11	Positive Clock Input	Dependent on Clock Module
	CM1_CLK_N	AF10	Negative Clock Input	Dependent on Clock Module
	CM3_CLK_P	AB17	Positive Clock Input	Dependent on Clock Module
	CM3_CLK_N	AC17	Negative Clock Input	Dependent on Clock Module

Table 3-2 shows the clock sources for the ML450 Rev 3 Board.

Table 3-2: **Clock Generation: ML450 Rev 3 Board**

	Signal Name	Pin Number	Direction	Description
Top of the Device (Bank3)	OSC1_250M_P	C13	Positive LVPECL Clock Input	Onboard 250-MHz LVPECL Oscillator
	OSC1_250M_N	C12	Negative LVPECL Clock Input	Onboard 250-MHz LVPECL Oscillator
	CLOCK-1_P	B15	Positive Differential Clock Input	SMA Connector J3
	CLOCK-1_N	B14	Negative Differential Clock Input	SMA Connector J1
	CM2_CLK_P	M19	Positive Clock Input	Dependent on Clock Module
	CM2_CLK_N	N19	Negative Clock Input	Dependent on Clock Module
	CM4_CLK_P	C15	Positive Clock Input	Dependent on Clock Module
	CM4_CLK_N	C14	Negative Clock Input	Dependent on Clock Module
Bottom of the Device (Bank4)	OSC1_200M_P	AD12	Positive LVPECL Clock Input	Onboard 200-MHz LVPECL Oscillator
	OSC1_200M_N	AD11	Negative LVPECL Clock Input	Onboard 200-MHz LVPECL Oscillator
	CLOCK-2_P	AF12	Positive Differential Clock Input	SMA Connector J4
	CLOCK-2_N	AE12	Negative Differential Clock Input	SMA Connector J2
	CM1_CLK_P	AF11	Positive Clock Input	Dependent on Clock Module
	CM1_CLK_N	AF10	Negative Clock Input	Dependent on Clock Module
	CM3_CLK_P	AB17	Positive Clock Input	Dependent on Clock Module
	CM3_CLK_N	AC17	Negative Clock Input	Dependent on Clock Module

Eight of the FPGA's clock inputs, bundled into four differential inputs, are routed to a set of small high-speed connectors. Each connector can carry a small board with a dedicated clock source.

Figure 3-2 shows the layout of the connector on the FPGA board.

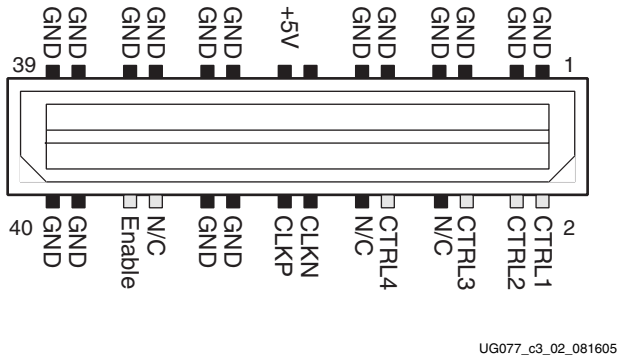


Figure 3-2: **Clock Connector (Top View)**

The connector on the small clock PCBs must be a Samtec QTE type.

Universal QTE and QSE connectors are on the ML450 Development Board schematics. The differential connectors are derived from these fully populated connectors.

Small clock device PCBs can be plugged into the connectors. When developed, each of these small boards requires a standard approach:

- The power supplied to the clock module connector is 5V. Each small clock board must contain its own local voltage regulators to supply any voltages needed by active devices on that board.
- Table 3-3 shows the non-GND signals of the clock module connectors for the ML450 Rev 2 Board.

Table 3-3: **Clock Module Non-GND Signals: ML450 Rev 2 Board**

Signal Name	Socket Pin#	FPGA Pin#	FPGA I or O	Description (Intended Usage)
CM1_CTRL1	P7.2	AE14	O	Clock Module control
CM1_CTRL2	P7.4	AE13	O	Clock Module control
CM1_CTRL3	P7.8	AE10	O	Clock Module control
CM1_CTRL4	P7.14	AD10	O	Clock Module control
VCC5	P7.19	N/A	N/A	+5V Power
VCC5	P7.21	N/A	N/A	+5V Power
CM1_CLK_N	P7.20	AF10	I	Clock Module differential N clock
CM1_CLK_P	P7.22	AF11	I	Clock Module differential P clock
CM1_EN	P7.34	AC10	O	Clock Module enable
CM2_CTRL1	P8.2	A16	O	Clock Module control
CM2_CTRL2	P8.4	A15	O	Clock Module control
CM2_CTRL3	P8.8	A10	O	Clock Module control
CM2_CTRL4	P8.14	B10	O	Clock Module control
VCC5	P8.19	N/A	N/A	+5V Power

Table 3-3: **Clock Module Non-GND Signals: ML450 Rev 2 Board *(Continued)***

Signal Name	Socket Pin#	FPGA Pin#	FPGA I or O	Description (Intended Usage)
VCC5	P8.21	N/A	N/A	+5V Power
CM2_CLK_N	P8.20	B12	I	Clock Module differential N clock
CM2_CLK_P	P8.22	B13	I	Clock Module differential P clock
CM2_EN	P8.34	A12	O	Clock Module enable
VCC5	P43.19	N/A	N/A	+5V Power
VCC5	P43.21	N/A	N/A	+5V Power
CM3_CLK_N	P43.20	AC17	I	Clock Module differential N clock
CM3_CLK_P	P43.22	AB17	I	Clock Module differential P clock
CM3_EN	P43.34	AB10	O	Clock Module enable
VCC5	P44.19	N/A	N/A	+5V Power
VCC5	P44.21	N/A	N/A	+5V Power
CM4_CLK_N	P44.20	C14	I	Clock Module differential N clock
CM4_CLK_P	P44.22	C15	I	Clock Module differential P clock
CM4_EN	P44.34	A11	O	Clock Module enable

The nomenclature in Table 3-3 reflects the intended signal usage compatible with the four clock modules included in the kit. The clock and control signals can be used as general-purpose I/O and are not dedicated. A different type of I/O board could replace the clock modules. Note that all clock module socket signals are wired to XC4VLX25 Banks 3 and 4, which contain only low capacitance (LC) pin types. Note that LC pins do not support the LVDS_25 transmit standard.

- As shown in Table 3-3, clock sockets CM-1 (P7) and CM-2 (P8) can support all clock module types. Clock sockets CM-3 (P43) and CM-4 (P44) can support clock module types A, B, and D.
- Table 3-4 shows the non-GND signals of the clock module connectors for the ML450 Rev 3 Board.

Table 3-4: **Clock Module Non-GND Signals: ML450 Rev 3 Board**

Signal Name	Socket Pin#	FPGA Pin#	FPGA I or O	Description (Intended Usage)
CM1_CTRL1	P7.2	AE14	O	Clock Module control
CM1_CTRL2	P7.4	AE13	O	Clock Module control
CM1_CTRL3	P7.8	AE10	O	Clock Module control
CM1_CTRL4	P7.14	AD10	O	Clock Module control
VCC5	P7.19	N/A	N/A	+5V Power
VCC5	P7.21	N/A	N/A	+5V Power
CM1_CLK_N	P7.20	AF10	I	Clock Module differential N clock

Table 3-4: **Clock Module Non-GND Signals: ML450 Rev 3 Board *(Continued)***

Signal Name	Socket Pin#	FPGA Pin#	FPGA I or O	Description (Intended Usage)
CM1_CLK_P	P7.22	AF11	I	Clock Module differential P clock
CM1_EN	P7.34	AC10	O	Clock Module enable
CM2_CTRL1	P8.2	A16	O	Clock Module control
CM2_CTRL2	P8.4	A15	O	Clock Module control
CM2_CTRL3	P8.8	A10	O	Clock Module control
CM2_CTRL4	P8.14	B10	O	Clock Module control
VCC5	P8.19	N/A	N/A	+5V Power
VCC5	P8.21	N/A	N/A	+5V Power
CM2_CLK_N	P8.20	N19	I	Clock Module differential N clock
CM2_CLK_P	P8.22	M19	I	Clock Module differential P clock
CM2_EN	P8.34	A12	O	Clock Module enable
VCC5	P43.19	N/A	N/A	+5V Power
VCC5	P43.21	N/A	N/A	+5V Power
CM3_CLK_N	P43.20	AC17	I	Clock Module differential N clock
CM3_CLK_P	P43.22	AB17	I	Clock Module differential P clock
CM3_EN	P43.34	AB10	O	Clock Module enable
VCC5	P44.19	N/A	N/A	+5V Power
VCC5	P44.21	N/A	N/A	+5V Power
CM4_CLK_N	P44.20	C14	I	Clock Module differential N clock
CM4_CLK_P	P44.22	C15	I	Clock Module differential P clock
CM4_EN	P44.34	A11	O	Clock Module enable

The nomenclature in Table 3-4 reflects the intended signal usage compatible with the four clock modules included in the kit. The clock and control signals can be used as general-purpose I/O and are not dedicated. A different type of I/O board could replace the clock modules. Note that all clock module socket signals are wired to XC4VLX25 Banks 3 and 4, which contain only low capacitance (LC) pin types. LC pins do not support the LVDS_25 transmit standard.

- As shown in Table 3-4, clock sockets CM-1 (P7) and CM-2 (P8) can support all clock module types. Clock sockets CM-3 (P43) and CM-4 (P44) can support clock module types A, B, and D.

Figure 3-3 shows the hardware schematic diagram for the clock board.

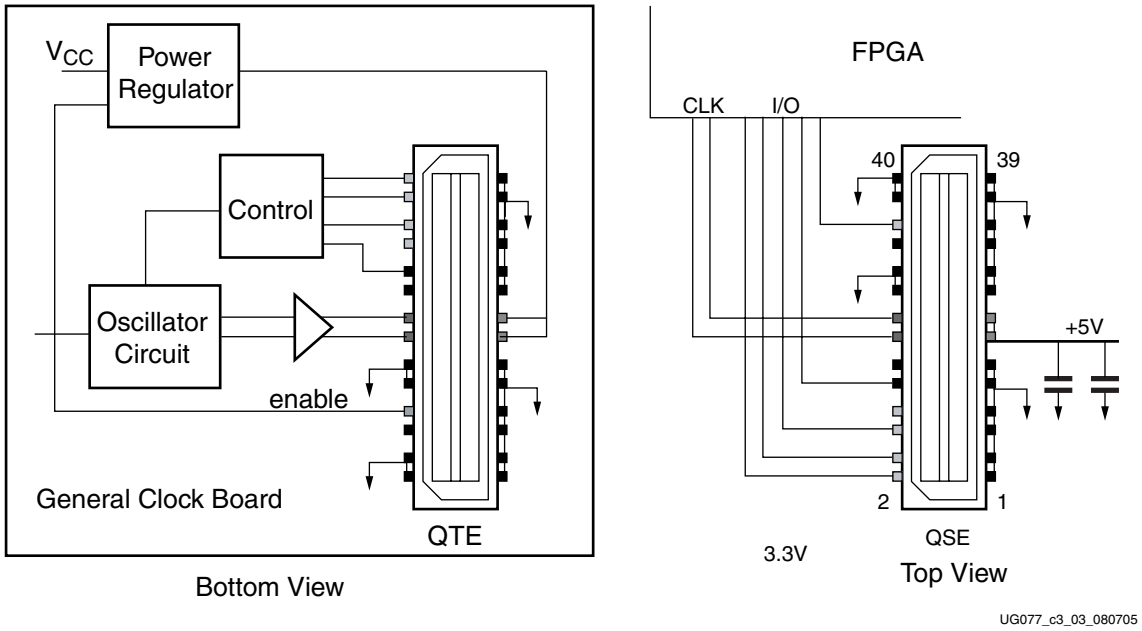


Figure 3-3: **Clock Board Schematic Diagram**

SDRAM Memory

The ML450 Development Board provides 64 MBytes of SDRAM memory (Micron Semiconductor MT46V32M16N-5B). The high-level block diagram of the SDRAM interface is shown in Figure 3-4. Table 3-5 lists the SDRAM memory interface signals for the FF668 package used on the ML450 Development Board.

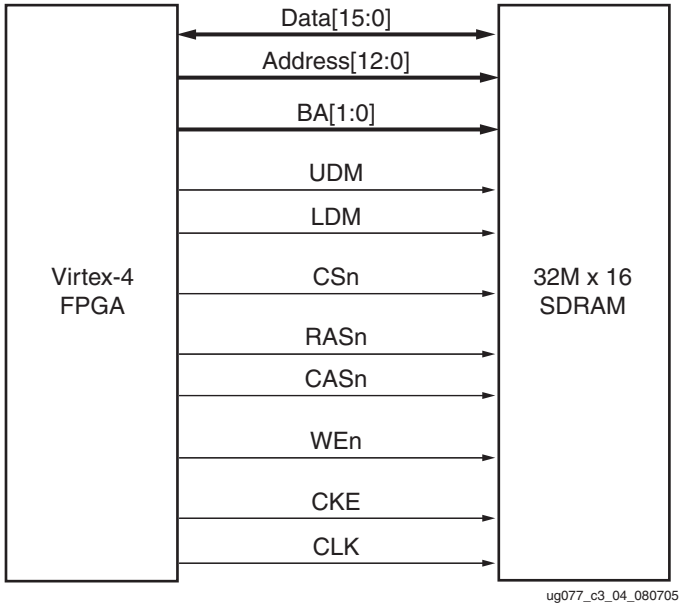


Figure 3-4: **Block Diagram of the SDRAM Interface**

Table 3-5: **SDRAM Memory Interface Signal Descriptions**

Signal Name	Description	FPGA Pin Number (FF668 Package)
A0	Address 0	AD2
A1	Address 1	AD1
A2	Address 2	Y10
A3	Address 3	AA10
A4	Address 4	AC7
A5	Address 5	AC9
A6	Address 6	AB9
A7	Address 7	AE6
A8	Address 8	AD6
A9	Address 9	AF9
A10	Address 10	AE9
A11	Address 11	AD8
A12	Address12	AC8
DQ0	Data 0	AB1
DQ1	Data 1	AA1
DQ2	Data 2	AC4
DQ3	Data 3	AB4
DQ4	Data 4	AC5
DQ5	Data 5	AB5
DQ6	Data 6	AC2
DQ7	Data 7	AC1
DQ8	Data 8	W7
DQ9	Data 9	V7
DQ10	Data 10	W6
DQ11	Data 11	W5
DQ12	Data 12	Y2
DQ13	Data 13	Y1
DQ14	Data 14	AA4
DQ15	Data 15	AA3
DQS0	DQ Strobe Lower Data Byte 0	Y6
DQS1	DQ Strobe Upper Data Byte 1	Y4

Table 3-5: **SDRAM Memory Interface Signal Descriptions *(Continued)***

Signal Name	Description	FPGA Pin Number (FF668 Package)
BA0	Bank Select 0	AF8
BA1	Bank Select 1	AF7
UDQM	Write Mask	W4
LDQM	Write Mask	AF3
CSn	Chip Select	AF4
RASn	Row Address Strobe	AA8
CASn	Column Address Strobe	Y8
WEn	Write Enable	Y9
CLK_P	Positive Clock	AD3
CLK_N	Negative Clock	AC3
CKE	Clock Enable	AA9

Liquid Crystal Display

The ML450 Development Board provides an 8-bit interface to a 64 x 128 LCD panel (DisplayTechQ 64128E-FC-BC-3LP, 64 x 128). This display was chosen because of its possible use in embedded systems. Appendix D, "LCD Interface," describes the LCD operation in detail.

Table 3-6 describes the LCD interface signal descriptions for the FF668 package used on the ML450 Development Board.

Table 3-6: **LCD Interface Signal Descriptions**

Signal Name	LCD Pin Number	Description	FPGA Pin Number (FF668 Package)
V_{SS}	1	GND	Ground
V_{DD}	2	3.3V DC	Logic Supply
MI	3	H = 6800 CPU, L = 8080 CPU	Pull-up resistor to 3.3V
DB7	4	LCD Data Bit 7	Y21
DB6	5	LCD Data Bit 6	Y20
DB5	6	LCD Data Bit 5	AE23
DB4	7	LCD Data Bit 4	AF23
DB3	8	LCD Data Bit 3	W19
DB2	9	LCD Data Bit 2	Y19
DB1	10	LCD Data Bit 1	AF20
DB0	11	LCD Data Bit 0	AF19
E	12	LCD Enable Signal	AF24
R/W	13	LCD Write Signal	Y18
RS	14	LCD Register Select Signal	AA18
RST	15	LCD Reset Signal	AD20
CS1B	16	LCD Chip Select Signal	AE20
LED +	17	LCD Back Light Anode	N/A
LED –	18	LCD Back Light Cathode	AE24 (Control)

A character-type display also can be connected because the graphical LCD has the same interface as many character-type LCD panels. The LCD can display alphanumeric (ASCII) information; however, a hardware character generator must be designed in the FPGA fabric in order to display the characters on the LCD screen.

Display Hardware Design

The I/Os of the FPGA function at 2.5V. The FPGA is connected to the graphic LCD display through a set of voltage-level converting devices. These switches translate the 2.5V I/O signals to the 3.3V signals that the LCD display requires.

Control for the LCD panel is based on the KS0713 controller from Samsung. The KS0713 is a 65-column, 132-segment driver-controller device for graphic dot matrix LCD display systems. The chip accepts serial or parallel display data. The 8-bit parallel interface is compatible with most LCD panel manufacturers. The serial connection mode is write only.

Extra features added to the interface in addition to the normal parallel signals are:

- Intel or Motorola compatible interface
- External reset of the chip
- External chip select

The interface also contains the following built-in options for the display and controller:

- On-chip oscillator circuitry
- On-chip voltage converter (x2, x3, x4, and x5)
- A 64-step electronic contrast control function

Table 3-7 summarizes the controller specifications.

Table 3-7: **Display Controller Specifications**

Parameter	Specification
Supply Voltage	2.4V to 3.6V (V_{DD})
LCD Driving Voltage	4V to 15V ($V_{LCD} = V_0 - V_{DD}$) Generated On-Chip
Power Consumption	70 µA typical (V_{DD} = 3V, x4 boost, V_0 = 11V, internal supply = ON)
Sleep Mode	2 µA
Standby Mode	10 µA

Hardware Schematic Diagrams

Figure 3-5 shows the schematic for connections to the display. Figure 3-6 shows a block diagram of the display, and Figure 3-7 shows the dimensions of the display.

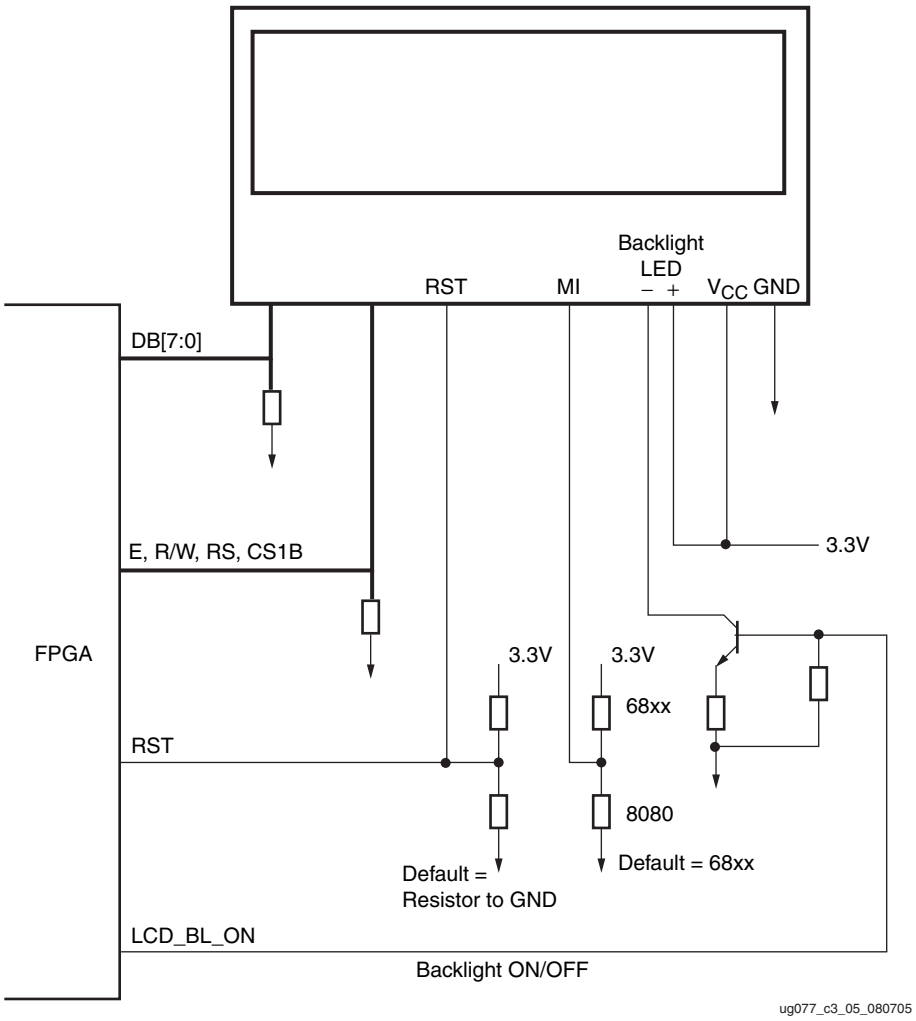


Figure 3-5: **Display Schematic Diagram**

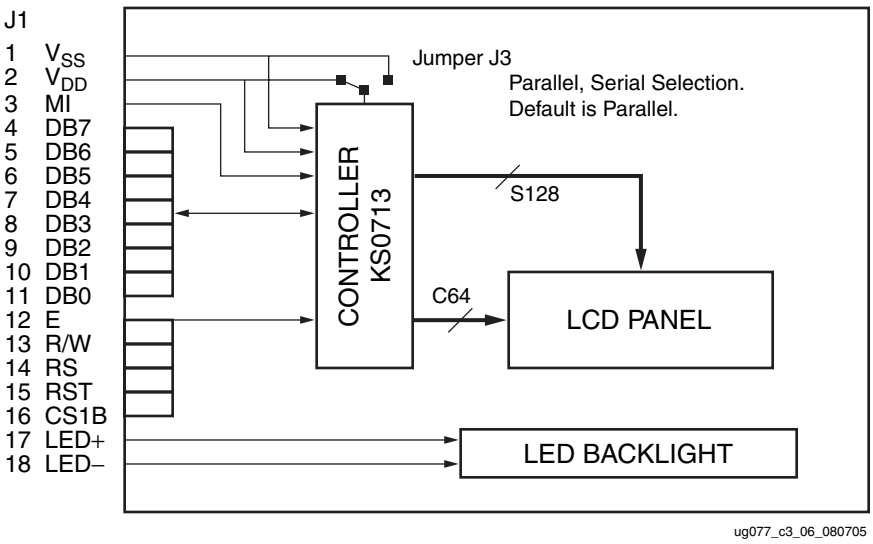


Figure 3-6: **64128EFCBC-3LP Block Diagram**

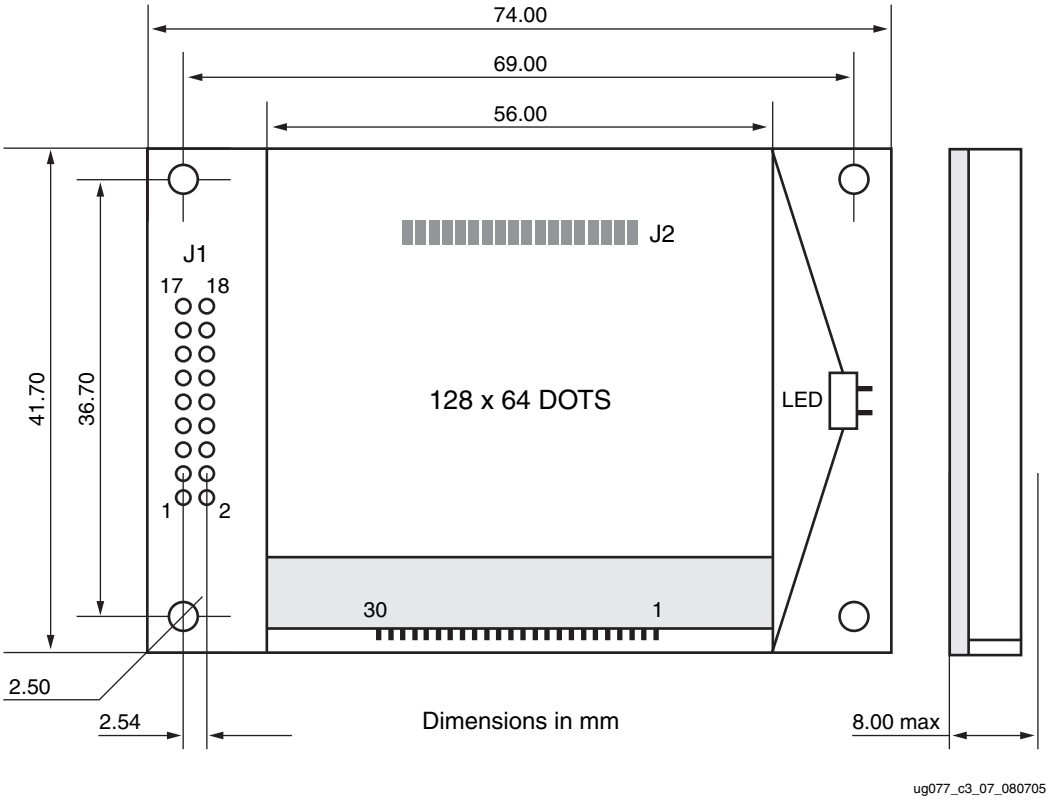


Figure 3-7: **64128EFCBC-3LP Dimensions**

User LED

The ML450 Development Board provides six user LEDs that can be turned ON by driving the LEDs signal Low. Table 3-8 describes the user LEDs and their associated pin assignments for the FF668 FPGA used on the ML450 Development Board.

Table 3-8: **User LED Pin Assignments**

LED	Designation	FPGA Pin Number (FF668 Package)
USER_LED0	USER1 D6	AB23
USER_LED1	USER2 D8	AA23
USER_LED2	USER3 D9	AD22
USER_LED3	USER4 D11	AD23
USER_LED4	USER5 D13	AC23
USER_LED5	USER6 D14	AC24

Configuration INIT and DONE LEDs

The ML450 Development Board provides an INIT LED and a DONE LED, which can be turned ON by driving the LEDs signal Low. Table 3-9 describes these LEDs and their associated pin assignments for the FF668 FPGA used on the ML450 Development Board.

Table 3-9: **Configuration INIT and DONE LED Pin Assignments**

LED	Designation	FPGA Pin Number (FF668 Package)
FPGA_INIT	INIT D19	G15
FPGA_DONE	DONE D20	H14

User Pushbutton Switches

The ML450 Development Board provides six user pushbutton switches that generate an active-Low signal when a given switch is pressed (see Table 3-10). There are pull-up resistors on the pushbutton switch signals on the ML450 Development Board. The internal FPGA pull-up resistors do not need to be used to force a given pushbutton switch signal High when its associated switch is not pressed. Switch contact debounce logic must be implemented inside the FPGA.

Table 3-10: **User Pushbutton Switch Assignments**

Signal Switch Designation	Description	FPGA Pin Number (FF668 Package)
USER_SW0 SW1	USER1	AC25
USER_SW1 SW2	USER2	AC26
USER_SW2 SW3	USER3	Y22

Table 3-10: **User Pushbutton Switch Assignments *(Continued)***

Signal Switch Designation	Description	FPGA Pin Number (FF668 Package)
USER_SW3 SW4	USER4	Y23
USER_SW4 SW5	USER5	AC22
USER_SW5 SW6	USER6	AB22
FPGA_RESETB SW10	RESET	D13

Program Switch

The ML450 Development Board provides a pushbutton program switch (SW12) for initiating the configuration of the Virtex-4 FPGA. This switch is used to force a reconfiguration of the FPGA from PROMs if they are present and enabled. The ML450 Development Board does not include PROMs.

The primary configuration device is the System ACE Controller (U13), which loads image files from a CompactFlash card. The mode switch (SW11) must be set to the proper mode for configuration to occur via the System ACE interface (refer to "Configuration Modes" on page 35 for further information regarding setting mode jumpers). The *PROG* pushbutton simply clears the FPGA configuration on this board.

RS-232 Port

The ML450 Development Board provides a DB9-M connection for a simple RS-232 port. The board uses the Maxim MAX3316 device to drive the RD, TD, RTS, and CTS signals. The user must provide a UART core internal to the FPGA to enable serial communication.

Table 3-11 describes the RS-232 interface signal names and their respective Virtex-4 FPGA pin assignments.

Table 3-11: **RS-232 Interface Signal Names and Pin Assignments**

Signal Name	Description	DB9-M Pin Number	Direction	FPGA Pin Number (FF668 Package)
RX	Receive Data RD	2	Input	AC20
TX	Transmit Data TD	3	Output	AB20
RTS	Request to Send RTS	7	Output	AD17
CTS	Clear to Send CTS	8	Input	AD16

A high-level block diagram of the RS-232 interface is shown in Figure 3-8.

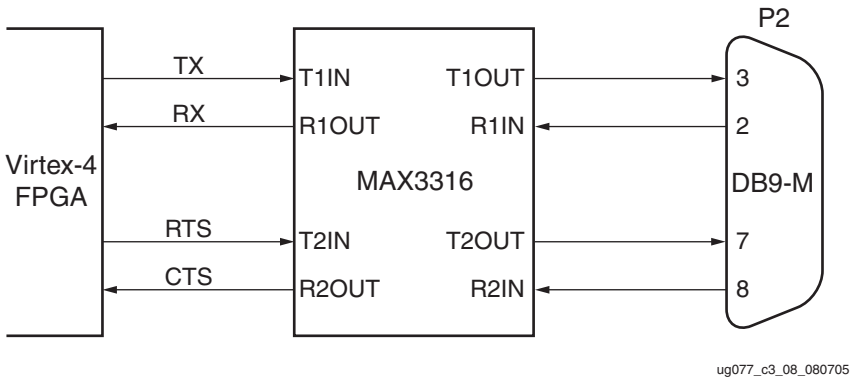


Figure 3-8: **RS-232 Interface Block Diagram**

The RS-232 DB9-F to DB9-F cable included in the kit mates with the P2 connector.

LVDS Connectors

The ML450 Development Board provides 44 channels of transmit signals and 44 channels of receive LVDS signals. These signals are distributed across two Samtec QSE-DP connectors for transmitting and another two connectors for receiving. Appendix A, "LVDS Connectors," lists the pin-outs and shows a graphical representation of each connector.

Transmit LVDS

The LVDS transmit differential pairs represent three different signal types:

- 40 data out pairs (LVDS_DATAOUT_P#/N#)
- Two clock out pairs (LVDS_CLKOUTn_P/N)
- Two frame out pairs (LVDS_FRAMEOUTn_P/N)

These signals are distributed across two Samtec QSE-DP connectors. The connector wiring is shown in the schematics on Sheet 10, as well as in Appendix A, "LVDS Connectors". Only one connector is fully populated.

Due to FPGA bank pin count limitations, the LVDS transmit pairs are driven from Banks 5, 7, and 9 (schematic Sheets 6, 8, and 10, respectively). Each Bank V_{CCO} is 2.5V, and the intended signalling standard for the LVDS interface is LVDS_25.

Figure A-1 shows LVDS transmit connector #1 (P46), and Figure A-2 shows LVDS transmit connector #2 (P49). Table A-2 lists the connections for LVDS transmit connector #1 (P46), and Table A-3 lists the connections for LVDS transmit connector #2 (P49).

Receive LVDS

The LVDS receive differential pairs represent three different signal types:

- 40 data-in pairs (LVDS_DATAIN_P#/N#)
- Two clock-in pairs (LVDS_CLKINn_P/N)
- Two frame-in pairs (LVDS_FRAMEINn_P/N)

These signals are distributed across two Samtec QSE-DP connectors. The connector wiring is shown in the schematics on Sheet 11, as well as in Appendix A, "LVDS Connectors". Only one connector is fully populated.

Due to FPGA bank pin count limitations, the LVDS receive pairs are terminated at Banks 1, 2, 6, and 10 (schematic Sheets 2, 3, 7, and 11 respectively). Each Bank V_{CCO} is 2.5V, and the intended signaling standard for the LVDS interface is LVDS_25.

Each LVDS receive differential pair has a discrete parallel termination resistor pad pair (size 0402) instantiated on the PCB as close to the FPGA as possible. The resistor (for LVDS, typically 100Ω) is NOT populated.

Figure A-3 shows LVDS receive connector #1 (P6), and Figure A-4 shows LVDS receive connector #2 (P3). Table A-3 lists the connections for LVDS receive connector #1 (P6), and Table A-4 lists the connections for LVDS receive connector #2 (P3).

LVDS Loopback Cables

The LVDS transmit and receive connectors can be connected to each other for loopback testing. The kit contains two Precision Interconnect *Blue Ribbon* mini-coax multiconductor cables, each terminated in a Samtec QTE-DP connector of the correct type.

The ML450 board LVDS transmit connectors are labelled P46 and P49. The ML450 board LVDS receive connectors are labelled P6 and P3. See Appendix A, "LVDS Connectors" for connector pinout details.

The TX and RX connectors are mounted in opposite orientations to allow the loopback cables to connect similarly named channel pairs to each other, i.e., TX P46 LVDS_DATAOUTP/N[25:00] pair are jumped to RX P6 LVDS_DATAINP/N[25:00] pair, etc. Each transmit TX_DATEOUT, FRAMEOUT and CLKOUT pair is jumped to its respective RX_DATAIN, FRAMEIN and CLKIN pair.

HyperTransport Connector (P24)

The ML450 Development Board provides 16 channels of transmit and receive data, along with miscellaneous control signals on the Samtec QSE HyperTransport connector P24.

Connections for the HyperTransport connector are described in detail in Appendix B, "HyperTransport Connector."

Information about HyperTransport technology is available on the web at:

http://www.hypertransport.org

The JTAG connections of P24 are included in the JTAG chain. Refer to Figure 4-2 for details of the JTAG chain jumper scheme (the default jumper selection bypasses the HyperTransport connector P24).

Voltage Regulators (TI PTH05000-WAH)

Figure 3-9 shows the voltage regulators used on ML450 Development Board to provide various on-board voltage sources. As shown in Figure 3-9, connector J12 provides the main 5.0V voltage to the board. This voltage source is provided to all on-board regulators to generate the 1.2V, 2.5V, 2.6V, and 3.3V voltages for the digital section of the board. All Bank V_{CCO} voltages are 2.5V.

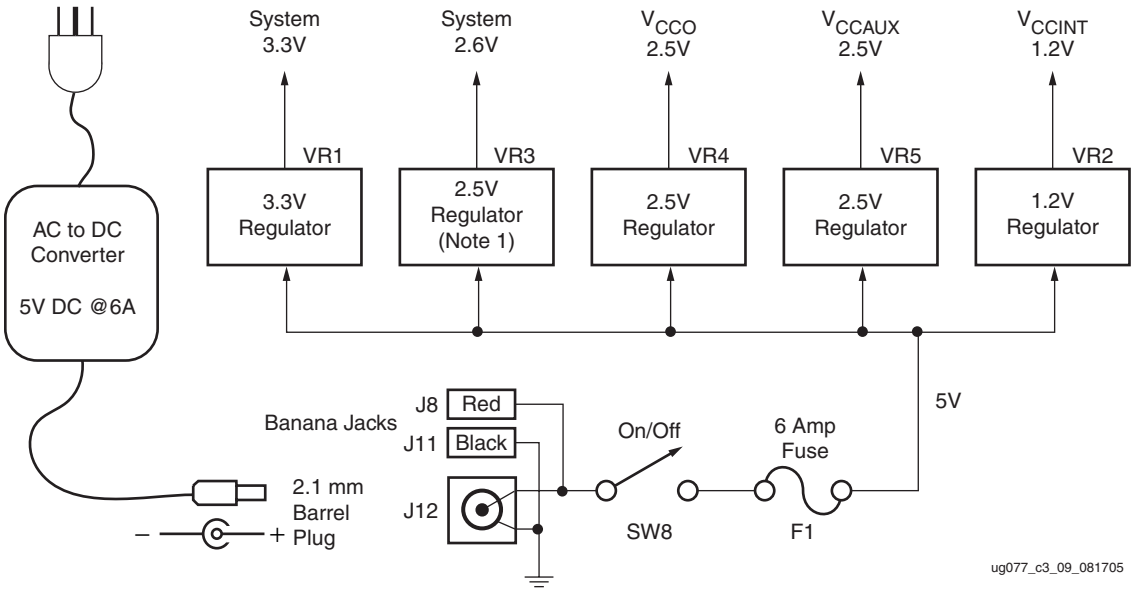


Figure 3-9: **Block Diagram of the Five Voltage Regulators**

Onboard digital voltages are as follows:

- 1.2V V_{CCINT} (VR2)
- 2.5V V_{CCAUX} (VR5)
- 2.5V V_{CCO} (VR4)
- 2.6V System (VR3)
- 3.3V System (VR1)

Note:

1. The 2.5V system adjustable output regulator is configured to generate a 2.6V output. The Micron DDR SDRAM device requires 2.6V to run at its full rated speed of 200 MHz.

Voltage Regulator ±5% Margin Adjustment

The regulators shown in Table 3-12 can have their outputs controlled over a ±5% range by the FPGA, or they can be enabled or inhibited through the use of on-board jumpers. The jumpers use the following conventions:

- Jumper OFF = Enabled
- Jumper ON = Inhibited

Table 3-12: **Voltage Regulators**

Regulator	Usage	Margin Control		Inhibit Jumper	Test Point Connector
		Channel 1	Channel 2		
VR1	System 3.3V	CTL11	CTL12	P4	P1
FPGA Pin		AA7	P3		
VR2	V_{CCINT} 1.2V	CTL7	CTL8	P14	P13
FPGA Pin		AF6	AF5		
VR3	System 2.6V	CTL1	CTL2	P21	P16
FPGA Pin		F14	F13		
VR4	V_{CCO} 2.5V	CTL5	CTL6	P30	P22
FPGA Pin		A17	AE4		
VR5	V_{CCAUX} 2.5V	CTL3	CTL4	P38	P33
FPGA Pin		F12	B17		

Notes:

1. Margin control signals CTL9 and CTL10 do not exist.

Figure 3-10 shows a typical schematic for voltage regulator control.

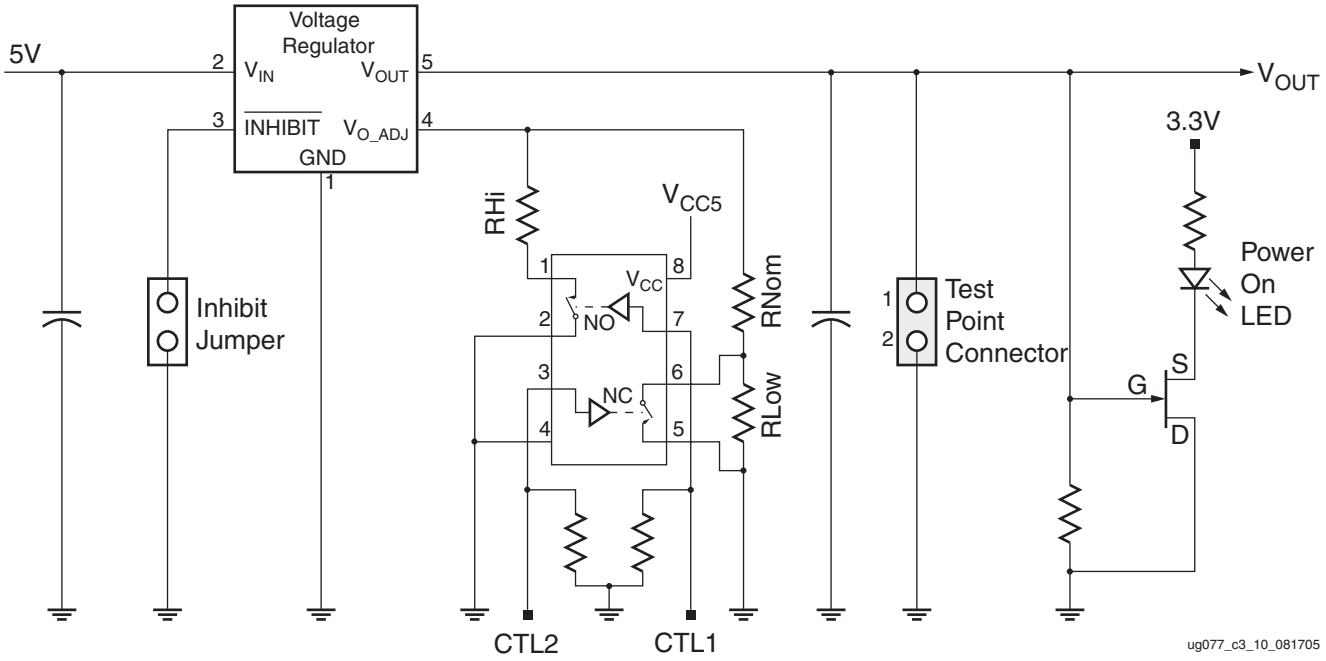


Figure 3-10: **Typical Voltage Regulator Configuration**

The TI PTH05000 regulator module requires a fixed 5V input. The output is adjustable over a range of 0.9V to 3.6V by changing the resistor tied between pin 4 and GND.

The ML450 Development Board implements the remote ±5% output adjustment using a Vishay Siliconix DG2005 two-channel analog switch. This switch has one normally closed channel, one normally open channel, and an analog switch resistance on the order of 5Ω. Each voltage regulator has its own independent margin control signals as shown in Figure 3-10.

Two pull-down resistors are tied to the channel control signals so that the default "nominal" regulator output value is selected at board power-up (before the FPGA has been configured). The normally closed Channel 2 selects the "nominal" output adjustment resistor (RNom) by shorting out a series resistor and connecting the "nominal" resistor to ground. Channel 1 is normally open, disconnecting the resistor tied to that channel.

To invoke the +5% output, the control signal for Channel 1 is driven High, causing the resistor (RHi) tied to Channel 1 to be switched in parallel with RNom. The parallel R value causes the regulator to adjust its output to the +5% margin.

To invoke the -5% output, the control signal for Channel 2 is driven High, causing the resistor (RLow) to be switched in series with RNom. The series R value causes the regulator to adjust its output to the -5% margin. Table 3-13 shows the switch selections used to control the voltage regulator output.

Table 3-13: **Voltage Regulator Control Signals**

Analog Switch Control Signals		V_{OUT} Regulator Output
Channel One (Normally Open)	Channel Two (Normally Closed)	
0	0	Nominal
0	1	–5%
1	0	+5%
1	1	Approximately +2%

Each regulator has a two-pin test point connector associated with it (pin 1 = V_{OUT} and pin 2 = GND). To apply other V_{OUT} values, first disable the on-board voltage regulator using the enable/disable jumpers shown in Table 3-12, and then connect a bench-top power supply to the two-pin test point connector for that voltage. This provides bench-top power to the power plane and also "back powers" the output pin of the inhibited voltage regulator.

Note: Do not turn OFF the 5V power to the ML450 Development Board while a bench-top power supply is ON and attached to the board in the manner described above. The voltage regulator can be damaged if the output is reverse powered and the 5V input is removed. Always turn the bench-top power supply OFF first, then turn the 5V power to the ML450 Development Board OFF.

Power Measurement SMA Pairs

The ML450 Development Board has two sets of power measurement “spy holes” wired into the XCV4LX25 FPGA. The *MEASURE-1* pair, J5(P) and J6(N), are connected to Bank 8 pins W2 and W1 respectively. A parallel 100Ω , 0402 resistor (R37) is installed between the two SMA connectors. There are also two 0603 resistor pad locations (unpopulated) wired between the SMA connectors and GND (R31 on J5, R30 on J6). These resistor locations are provided to allow varying configurations of clock in, clock out, and measurement connectivity.

The *MEASURE-2* pair, J9(P) and J10(N), are connected to Bank 9 pins J26 and J25 respectively. A parallel 100Ω , 0402 resistor (R188) is installed between the two SMA connectors. There are also two 0603 resistor pad locations (unpopulated) wired between the SMA connectors and GND (R187 on J9, R189 on J10). These resistor locations are provided to allow varying configurations of clock in, clock out, and measurement connectivity.

Chapter 4

Configuration

The Virtex-4 ML450 Networking Interfaces Development Board includes several options to configure the Virtex-4 FPGA. The configuration modes are:

- System ACE mode
- JTAG mode
- Slave Serial mode
- Master Serial mode

This chapter provides a brief description of the FPGA configuration methods used on the ML450 Development Board.

Configuration Modes

Table 4-1 shows the Virtex-4 configuration modes. The Master and Slave (Parallel) SelectMap configuration modes are not supported on the ML450 Development Board. Figure 4-1 shows the Configuration Mode switch (SW11).

Table 4-1: **Configuration Modes**

Mode	XCONFIG P41	JTAG P50 or P51	Mode SW11(2,3)		
			3 (M2)	2 (M1)	1 (M0)
Master Serial	X	—	0	0	0
Slave Serial	X	—	1	1	1
Master SelectMAP (1)	N/A	N/A	0	1	1
Slave SelectMAP (1)	N/A	N/A	1	1	0
JTAG	—	X	1	0	1
System ACE CF Card	—	—	1	1	1

Notes:

1. Not supported on the Virtex-4 ML450 Development Board.
2. 0 = SW11 switch position (n) is Closed.
3. 1 = SW11 switch position (n) is Open.

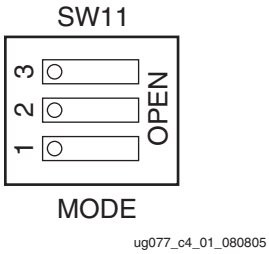


Figure 4-1: **Configuration Mode Switch**

JTAG Chain

Figure 4-2 shows the JTAG chain on the ML450 Development Board and illustrates how three different sources can be used to drive this JTAG chain. The chain can be driven by the following sources:

- System ACE controller
- Xilinx Parallel Cable IV
- Other JTAG cables

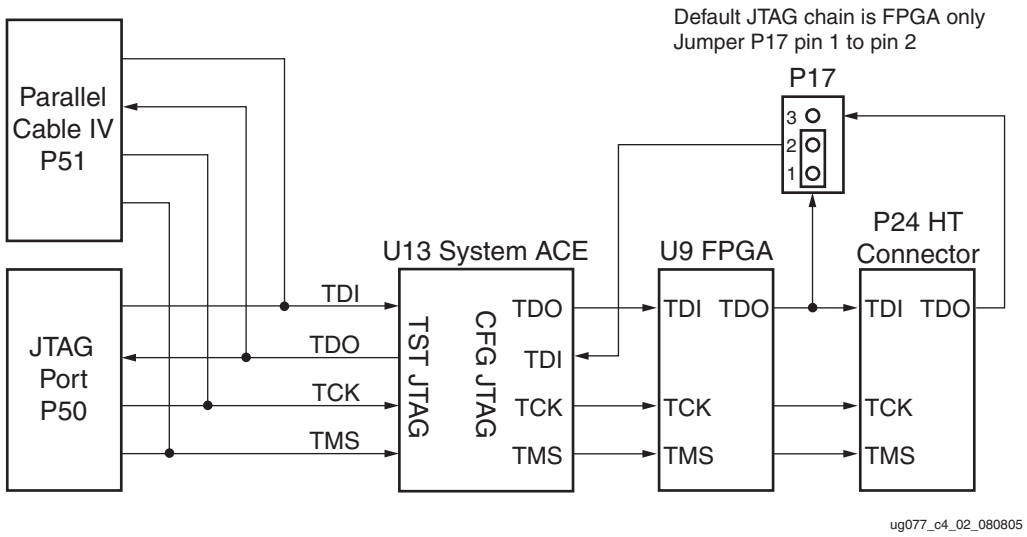


Figure 4-2: **JTAG Chain**

JTAG Port

The ML450 Development Board provides a JTAG connector (P50) that can be used to program the Virtex-4 FPGA and program and/or configure other JTAG devices in the

chain. Figure 4-3 shows the pin assignments for the JTAG connectors on the ML450 Development Board.

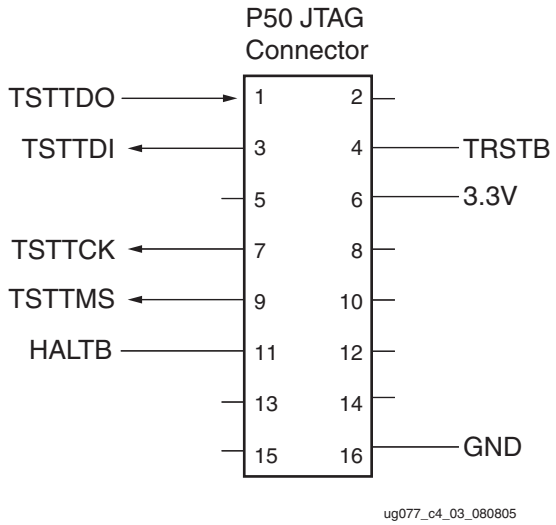


Figure 4-3: **JTAG Connectors P50 and P51**

Table 4-2 describes the P50 JTAG Header signal names, descriptions, and pin assignments.

Table 4-2: **P50 JTAG Header Signal Descriptions and Pin Assignments**

Signal Name	Description	P50 Pin Number	System ACE Pin Number
TSTTDO	JTAG TDO from System ACE Interface	1	97
TSTTDI	JTAG TDI to System ACE Interface	3	102
TSTTCK	JTAG TCK to System ACE Interface	7	101
TSTTMS	JTAG TMS to System ACE Interface	9	98
HALTB	User Defined	11	N/A; goes to FPGA pin V5
TRSTB	User Defined	4	N/A; goes to PFGA pin V6

Parallel Cable IV Port

The ML450 Development Board provides a Parallel Cable IV connector (P51) to configure the Virtex-4 FPGA and program JTAG devices located in the JTAG chain. Figure 4-4 shows the pin assignments for the Parallel Cable IV connector. The Parallel Cable IV can also be

used to configure the FPGA in Slave Serial configuration mode. The Parallel IV cable connects to P51 as shown in Figure 4-5.

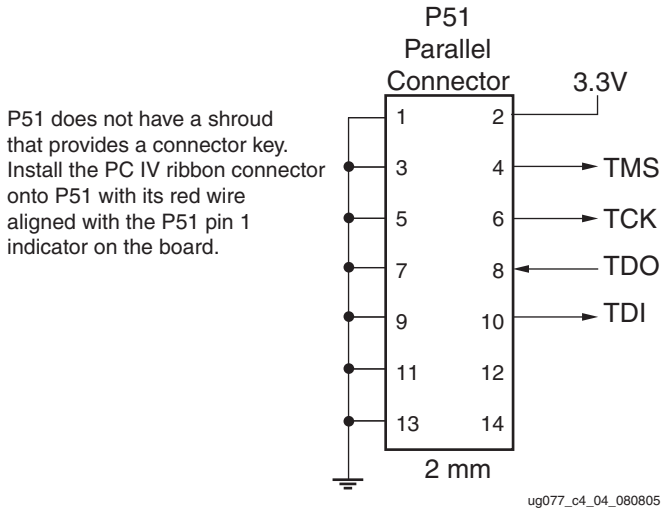


Figure 4-4: **Parallel IV Cable Hook-up**

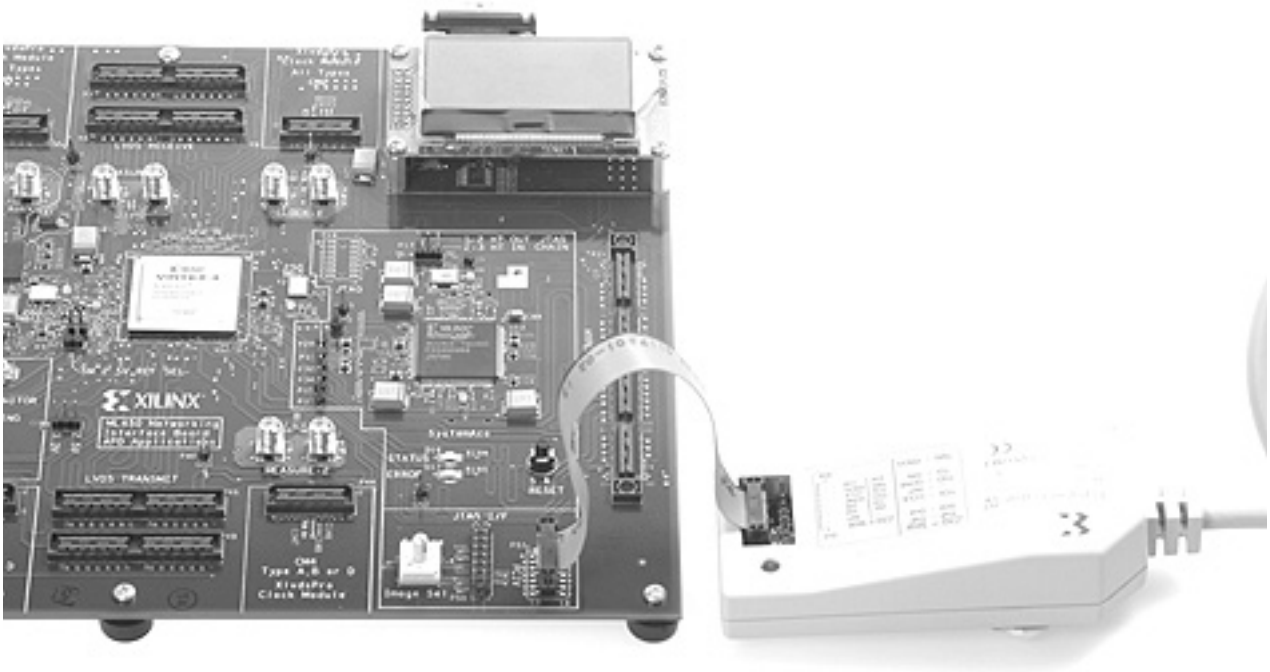


Figure 4-5: **Photo of ML450 Development Board and PC IV Pod Flat Cable Connection to P51**

System ACE Interface

The ML450 Development Board provides a System ACE interface to configure the Virtex-4 FPGA. The interface also gives software designers the ability to run code (for soft processor IP within the FPGA) from removable CompactFlash cards. Figure 4-6 shows the System ACE interface. When the MPU port of the System ACE Controller is used, the Virtex-4

FPGA and the System ACE Controller use the same clock source for interface synchronization.

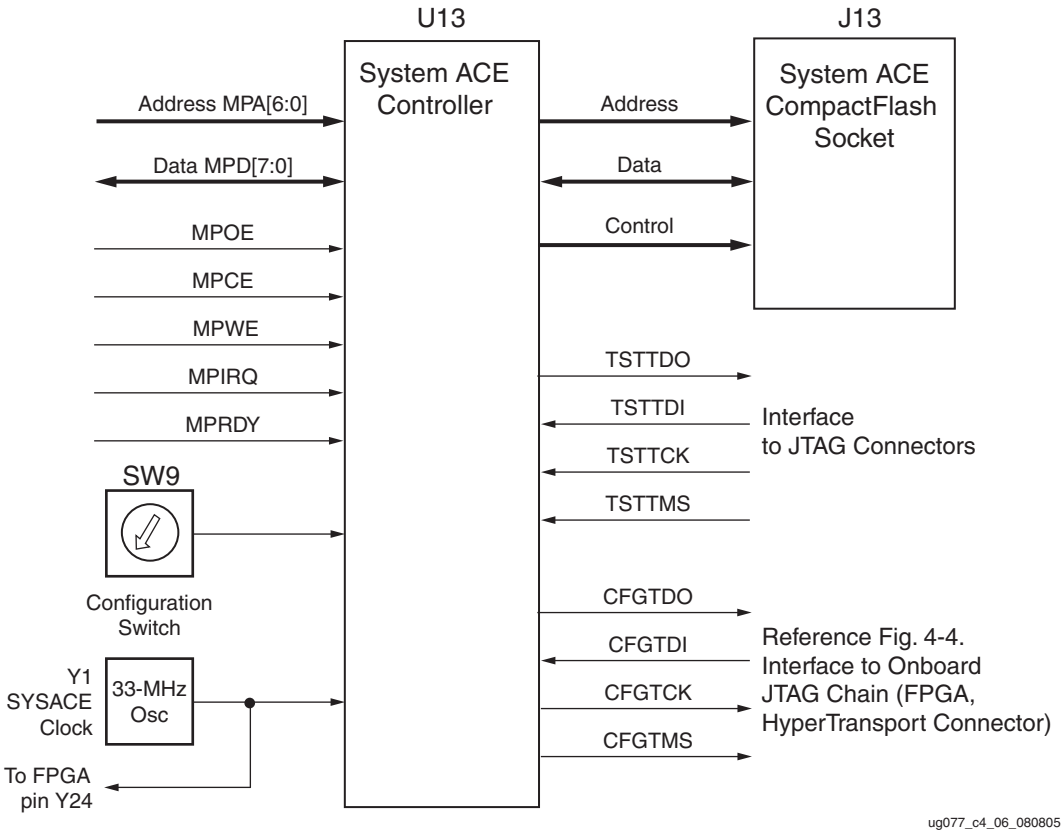


Figure 4-6: **System ACE Interface**

For detailed information on creation of System ACE compatible .ace files, formatting the CF card, and storing multiple design images, see the System ACE CompactFlash Solution Advance Product Specification (DS080). This data sheet is available at:

http://www.xilinx.com/isp/systemace/systemacecf.htm

Table 4-3 shows the System ACE interface signal names, descriptions, and pin assignments.

Table 4-3: **System ACE Interface Signal Descriptions**

System ACE Pin Number	Signal Name	FPGA Pin Number
70	SYSACE_MPA0	AA11
69	SYSACE_MPA1	AC16
68	SYSACE_MPA2	N19
67	SYSACE_MPA3	R19
45	SYSACE_MPA4	AD26
44	SYSACE_MPA5	T24
43	SYSACE_MPA6	AD25
66	SYSACE_MPD0	AC14
65	SYSACE_MPD1	AD14
63	SYSACE_MPD2	AA12
62	SYSACE_MPD3	AA24
61	SYSACE_MPD4	AB21
60	SYSACE_MPD5	AC21
59	SYSACE_MPD6	AB25
58	SYSACE_MPD7	AB24
77	SYSACE_CTRL0/MPOE	M19
76	SYSACE_CTRL1/MPWE	AC15
42	SYSACE_CTRL2/MPCE	AC13
41	SYSACE_CTRL3/MPIRQ	T23
39	SYSACE_CTRL4/MPBRDY	R20
93	SYSACE_CLK	Y24

Table 4-4 shows the System ACE interface signal names, descriptions, and pin assignmentsfor the ML450 Rev3 Board.

Table 4-4: **System ACE Interface Signal Descriptions for the ML450 Rev 3 Board**

System ACE Pin Number	Signal Name	FPGA Pin Number
70	SYSACE_MPA0	AA11
69	SYSACE_MPA1	AC16
68	SYSACE_MPA2	B12
67	SYSACE_MPA3	R19
45	SYSACE_MPA4	AD26
44	SYSACE_MPA5	T24
43	SYSACE_MPA6	AD25
66	SYSACE_MPD0	AC14
65	SYSACE_MPD1	AD14
63	SYSACE_MPD2	AA12
62	SYSACE_MPD3	AA24
61	SYSACE_MPD4	AB21
60	SYSACE_MPD5	AC21
59	SYSACE_MPD6	AB25
58	SYSACE_MPD7	AB24
77	SYSACE_CTRL0/MPOE	B13
76	SYSACE_CTRL1/MPWE	AC15
42	SYSACE_CTRL2/MPCE	AC13
41	SYSACE_CTRL3/MPIRQ	T23
39	SYSACE_CTRL4/MPBRDY	R20
93	SYSACE_CLK	Y24

Appendix A

LVDS Connectors

This appendix provides the pin-outs for the four LVDS Connectors.

LVDS Transmit Connectors

Figure A-1 shows LVDS transmit connector #1 (P46), and Figure A-2 shows LVDS transmit connector #2 (P49). Table A-1 lists the connections for LVDS transmit connector #1 (P46), and Table A-2 lists the connections for LVDS transmit connector #2 (P49).

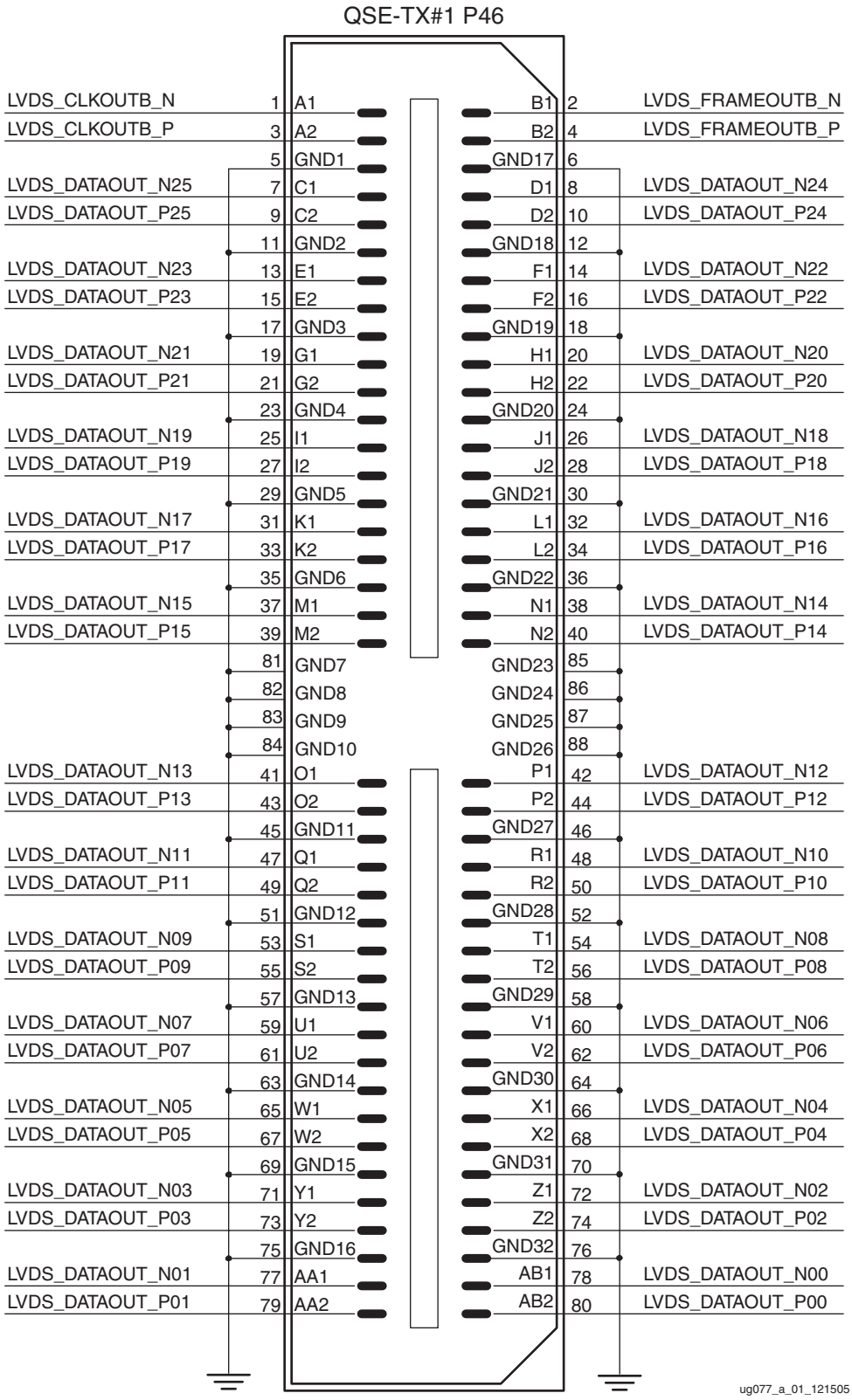


Figure A-1: **LVDS Transmit Connector #1**

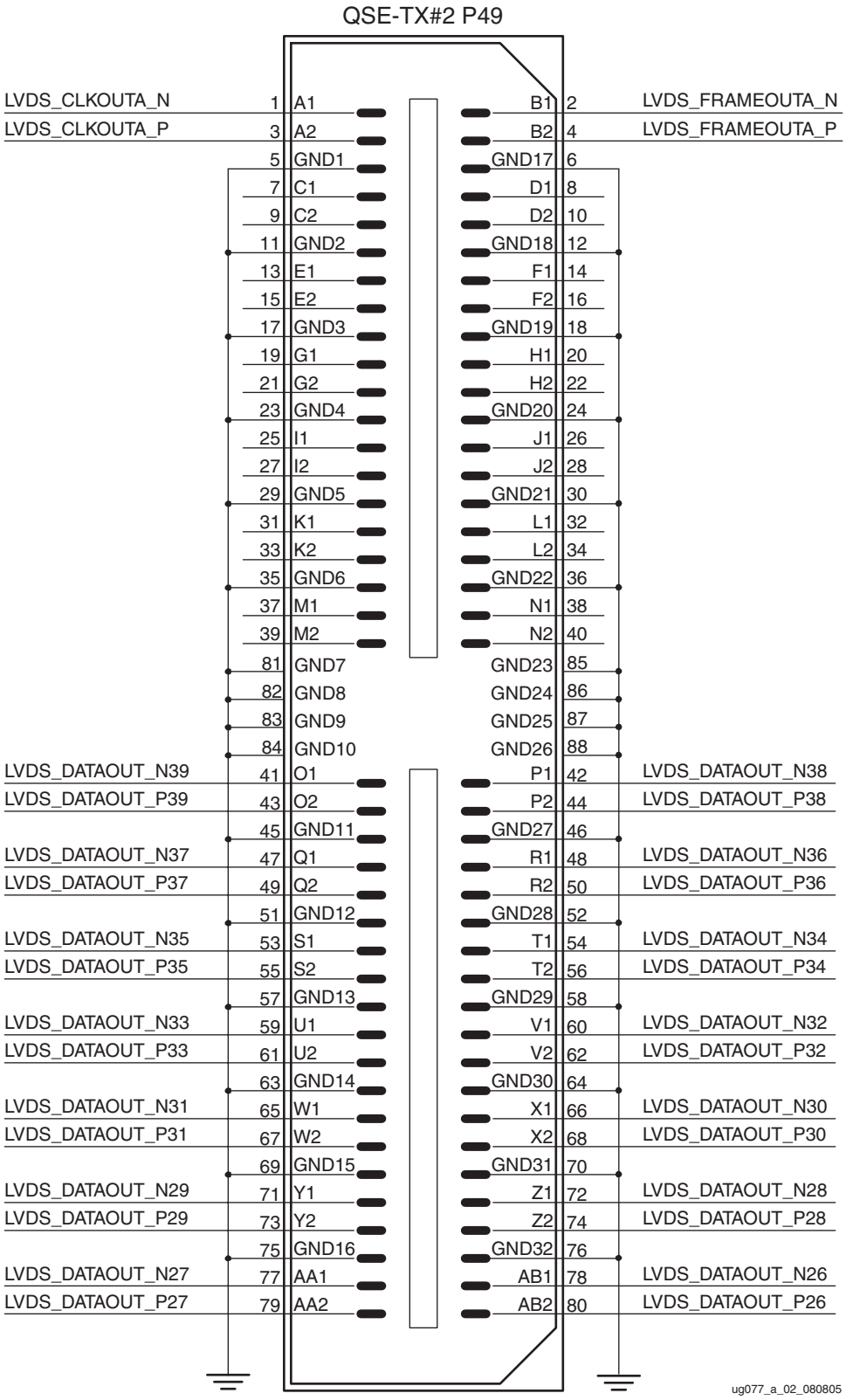


Figure A-2: **LVDS Transmit Connector #2**

Table A-1: **LVDS Transmit Connector #1 Pin-out (P46)**

P46	TX#1 Signal Name	U11 Pin#	Bank#	P46	TX#1 Signal Name	U11 Pin#	Bank#
1	LVDS_CLKOUTB_N	H21	5	37	LVDS_DATAOUT_N15	U26	9
2	LVDS_FRAMEOUTB_N	G21	5	38	LVDS_DATAOUT_N14	M22	9
3	LVDS_CLKOUTB_P	H22	5	39	LVDS_DATAOUT_P15	T26	9
4	LVDS_FRAMEOUTB_P	G22	5	40	LVDS_DATAOUT_P14	M23	9
5	GND			41	LVDS_DATAOUT_N13	V25	9
6	GND			42	LVDS_DATAOUT_N12	N24	9
7	LVDS_DATAOUT_N25	G25	5	43	LVDS_DATAOUT_P13	V26	9
8	LVDS_DATAOUT_N24	G23	5	44	LVDS_DATAOUT_P12	N25	9
9	LVDS_DATAOUT_P25	G26	5	45	GND		
10	LVDS_DATAOUT_P24	G24	5	46	GND		
11	GND			47	LVDS_DATAOUT_N11	K20	9
12	GND			48	LVDS_DATAOUT_N10	N22	9
13	LVDS_DATAOUT_N23	H25	5	49	LVDS_DATAOUT_P11	L19	9
14	LVDS_DATAOUT_N22	H23	5	50	LVDS_DATAOUT_P10	N23	9
15	LVDS_DATAOUT_P23	H26	5	51	GND		
16	LVDS_DATAOUT_P22	H24	5	52	GND		
17	GND			53	LVDS_DATAOUT_N09	P24	9
18	GND			54	LVDS_DATAOUT_N08	R21	9
19	LVDS_DATAOUT_N21	E22	5	55	LVDS_DATAOUT_P09	P25	9
20	LVDS_DATAOUT_N20	J22	9	56	LVDS_DATAOUT_P08	R22	9
21	LVDS_DATAOUT_P21	E23	5	57	GND		
22	LVDS_DATAOUT_P20	J23	9	58	GND		
23	GND			59	LVDS_DATAOUT_N07	V20	7
24	GND			60	LVDS_DATAOUT_N06	T20	9
25	LVDS_DATAOUT_N19	G20	5	61	LVDS_DATAOUT_P07	W20	7
26	LVDS_DATAOUT_N18	K23	9	62	LVDS_DATAOUT_P06	T21	9
27	LVDS_DATAOUT_P19	H20	5	63	GND		
28	LVDS_DATAOUT_P18	K24	9	64	GND		
29	GND			65	LVDS_DATAOUT_N05	U24	9
30	GND			66	LVDS_DATAOUT_N04	U21	9
31	LVDS_DATAOUT_N17	R25	9	67	LVDS_DATAOUT_P05	U25	9
32	LVDS_DATAOUT_N16	L23	9	68	LVDS_DATAOUT_P04	U22	9
33	LVDS_DATAOUT_P17	R26	9	69	GND		
34	LVDS_DATAOUT_P16	L24	9	70	GND		
35	GND			71	LVDS_DATAOUT_N03	V23	9
36	GND			72	LVDS_DATAOUT_N02	T19	9

Table A-1: **LVDS Transmit Connector #1 Pin-out (P46) *(Continued)***

P46	TX#1 Signal Name	U11 Pin#	Bank#	P46	TX#1 Signal Name	U11 Pin#	Bank#
73	LVDS_DATAOUT_P03	U23	9	81	GND		
74	LVDS_DATAOUT_P02	U20	9	82	GND		
75	GND			83	GND		
76	GND			84	GND		
77	LVDS_DATAOUT_N01	W26	7	85	GND		
78	LVDS_DATAOUT_N00	Y26	7	86	GND		
79	LVDS_DATAOUT_P01	W25	7	87	GND		
80	LVDS_DATAOUT_P00	Y25	7	88	GND		

Table A-2: **LVDS Transmit Connector #2 Pin-out (P49)**

P49	TX#2 Signal Name	U11 Pin#	Bank#	P49	TX#2 Signal Name	U11 Pin#	Bank#
1	LVDS_CLKOUTA_N	F19	5	37			
2	LVDS_FRAMEOUTA_N	E20	5	38			
3	LVDS_CLKOUTA_P	G19	5	39			
4	LVDS_FRAMEOUTA_P	F20	5	40			
5	GND			41	LVDS_DATAOUT_N39	J20	9
6	GND			42	LVDS_DATAOUT_N38	M24	9
7				43	LVDS_DATAOUT_P39	J21	9
8				44	LVDS_DATAOUT_P38	M25	9
9				45	GND		
10				46	GND		
11	GND			47	LVDS_DATAOUT_N37	K21	9
12	GND			48	LVDS_DATAOUT_N36	M26	9
13				49	LVDS_DATAOUT_P37	K22	9
14				50	LVDS_DATAOUT_P36	L26	9
15				51	GND		
16				52	GND		
17	GND			53	LVDS_DATAOUT_N35	L20	9
18	GND			54	LVDS_DATAOUT_N34	P22	9
19				55	LVDS_DATAOUT_P35	L21	9
20				56	LVDS_DATAOUT_P34	P23	9
21				57	GND		
22				58	GND		
23	GND			59	LVDS_DATAOUT_N33	M20	9
24	GND			60	LVDS_DATAOUT_N32	R23	9
25				61	LVDS_DATAOUT_P33	M21	9
26				62	LVDS_DATAOUT_P32	R24	9
27				63	GND		
28				64	GND		
29	GND			65	LVDS_DATAOUT_N31	V22	7
30	GND			66	LVDS_DATAOUT_N30	N20	9
31				67	LVDS_DATAOUT_P31	V21	7
32				68	LVDS_DATAOUT_P30	N21	9
33				69	GND		
34				70	GND		
35	GND			71	LVDS_DATAOUT_N29	P19	9
36	GND			72	LVDS_DATAOUT_N28	W22	7

Table A-2: **LVDS Transmit Connector #2 Pin-out *(Continued)* (P49)**

P49	TX#2 Signal Name	U11 Pin#	Bank#	P49	TX#2 Signal Name	U11 Pin#	Bank#
73	LVDS_DATAOUT_P29	P20	9	81	GND		
74	LVDS_DATAOUT_P28	W21	7	82	GND		
75	GND			83	GND		
76	GND			84	GND		
77	LVDS_DATAOUT_N27	AA26	7	85	GND		
78	LVDS_DATAOUT_N26	W24	7	86	GND		
79	LVDS_DATAOUT_P27	AB26	7	87	GND		
80	LVDS_DATAOUT_P26	W23	7	88	GND		

LVDS Receive Connectors

Figure A-3 shows LVDS receive connector #1 (P6), and Figure A-4 shows LVDS receive connector #2 (P3). Table A-3 lists the connections for LVDS receive connector #1 (P6), and Table A-4 lists the connections for LVDS receive connector #2 (P3).

The LVDS receive signal differential pairs each have a parallel 100Ω termination resistor location implemented on the ML450 Development Board. Refer to the schematic on page 11 for details. These resistors (0402 size) are optional and are not installed. They are removed to permit use of the FPGA on-die termination feature. The resistor pads are placed as close as possible to the FPGA and are not located at the connector.

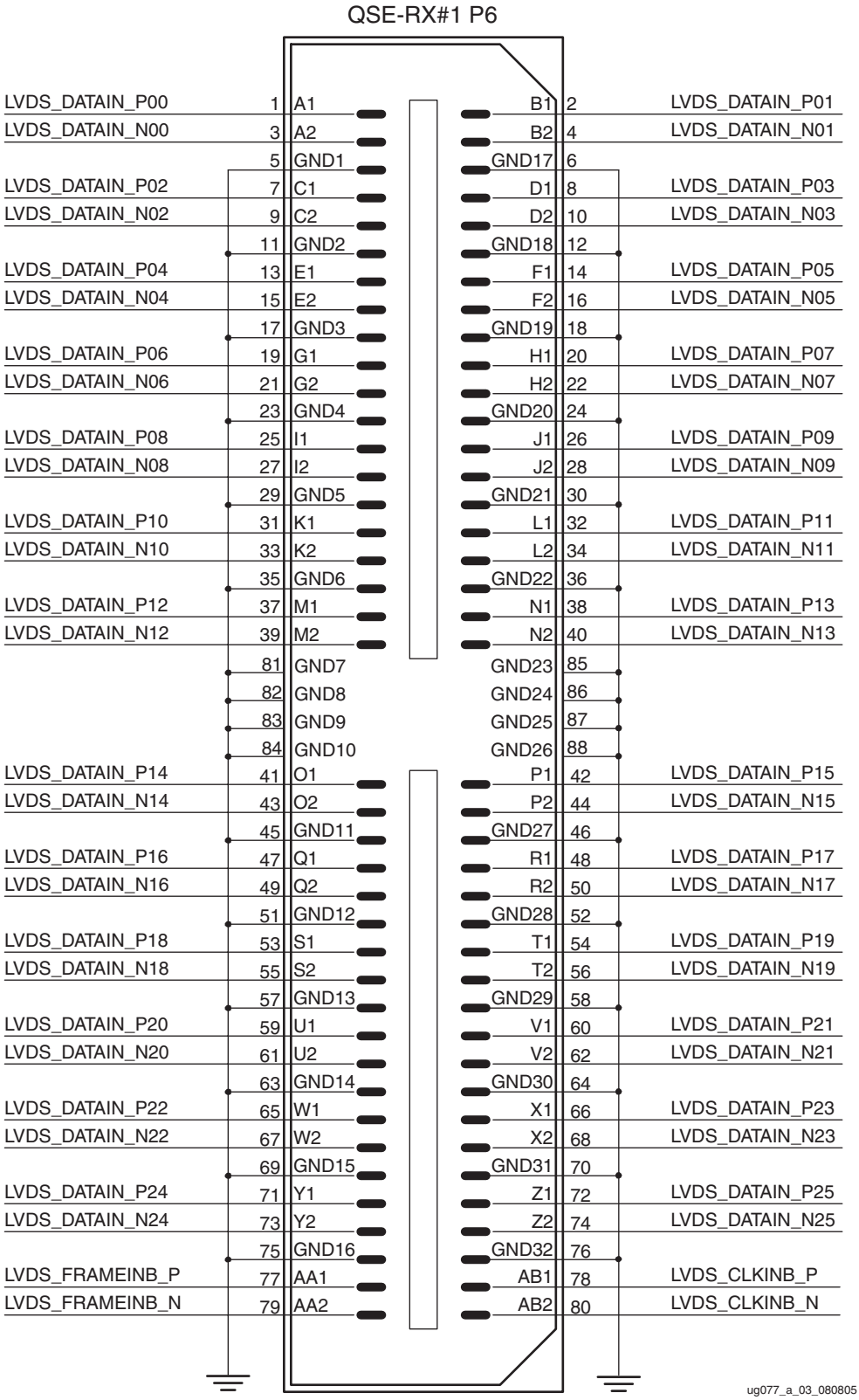


Figure A-3: **LVDS Receive Connector #1**

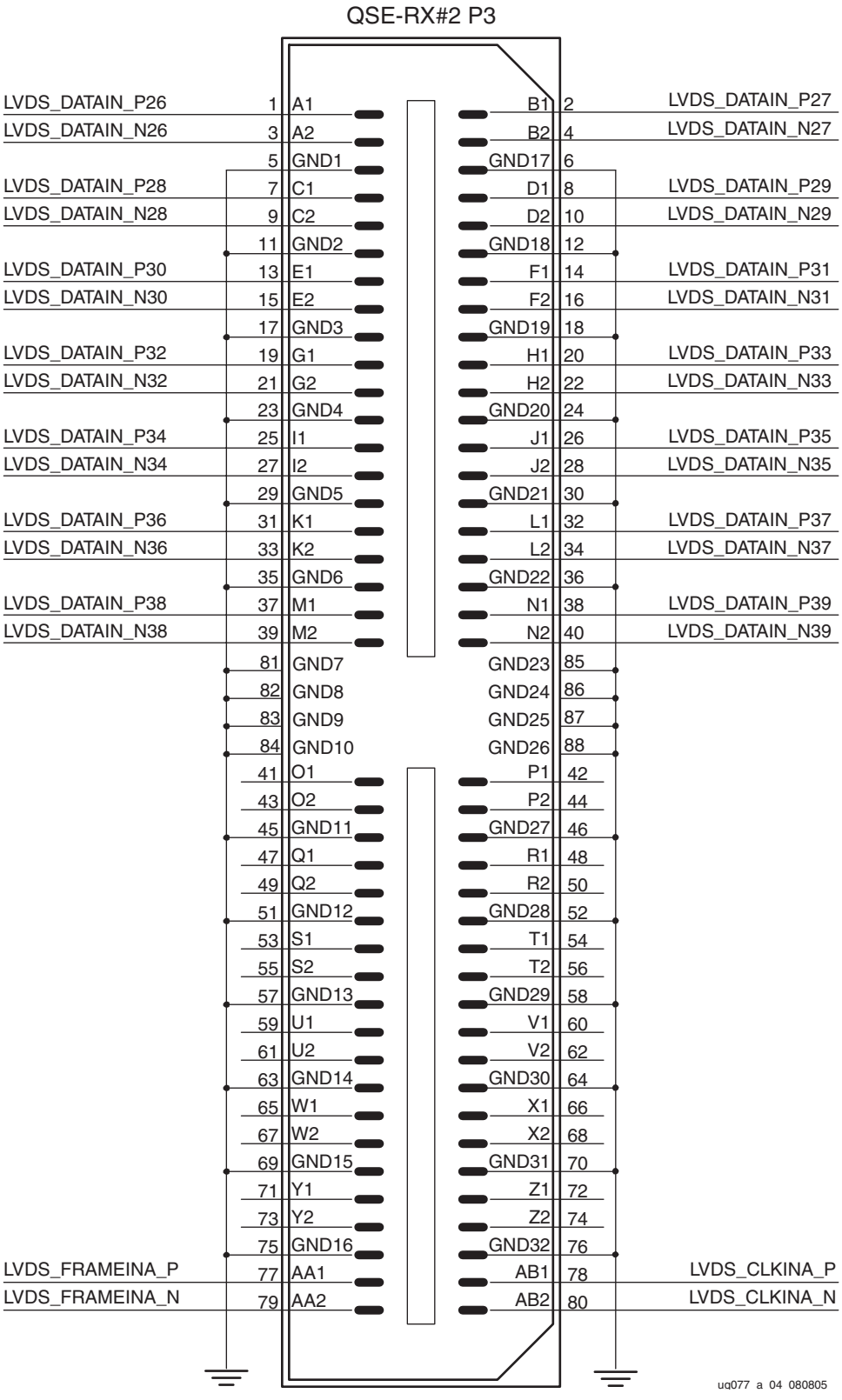


Figure A-4: **LVDS Receive Connector #2**

Table A-3: **LVDS Receive Connector #1 Pin-out (P6)**

P6	RX#1 Signal Name	U11 Pin#	Bank#	P6	RX#1 Signal Name	U11 Pin#	Bank#
1	LVDS_DATAIN_P00	AC12	2	37	LVDS_DATAIN_P12	P7	10
2	LVDS_DATAIN_P01	AB13	2	38	LVDS_DATAIN_P13	N5	10
3	LVDS_DATAIN_N00	AC11	2	39	LVDS_DATAIN_N12	P6	10
4	LVDS_DATAIN_N01	AA13	2	40	LVDS_DATAIN_N13	N4	10
5	GND			41	LVDS_DATAIN_P14	N7	10
6	GND			42	LVDS_DATAIN_P15	M4	10
7	LVDS_DATAIN_P02	U6	10	43	LVDS_DATAIN_N14	M7	10
8	LVDS_DATAIN_P03	V4	10	44	LVDS_DATAIN_N15	M3	10
9	LVDS_DATAIN_N02	U5	10	45	GND		
10	LVDS_DATAIN_N03	U4	10	46	GND		
11	GND			47	LVDS_DATAIN_P16	K7	10
12	GND			48	LVDS_DATAIN_P17	M6	10
13	LVDS_DATAIN_P04	T7	10	49	LVDS_DATAIN_N16	K6	10
14	LVDS_DATAIN_P05	U3	10	50	LVDS_DATAIN_N17	M5	10
15	LVDS_DATAIN_N04	T6	10	51	GND		
16	LVDS_DATAIN_N05	U2	10	52	GND		
17	GND			53	LVDS_DATAIN_P18	J7	10
18	GND			54	LVDS_DATAIN_P19	K5	10
19	LVDS_DATAIN_P06	R2	10	55	LVDS_DATAIN_N18	J6	10
20	LVDS_DATAIN_P07	T4	10	56	LVDS_DATAIN_N19	K4	10
21	LVDS_DATAIN_N06	R1	10	57	GND		
22	LVDS_DATAIN_N07	T3	10	58	GND		
23	GND			59	LVDS_DATAIN_P20	L4	10
24	GND			60	LVDS_DATAIN_P21	J5	10
25	LVDS_DATAIN_P08	N3	10	61	LVDS_DATAIN_N20	L3	10
26	LVDS_DATAIN_P09	R4	10	62	LVDS_DATAIN_N21	J4	10
27	LVDS_DATAIN_N08	N2	10	63	GND		
28	LVDS_DATAIN_N09	R3	10	64	GND		
29	GND			65	LVDS_DATAIN_P22	K3	10
30	GND			66	LVDS_DATAIN_P23	H6	6
31	LVDS_DATAIN_P10	M2	10	67	LVDS_DATAIN_N22	K2	10
32	LVDS_DATAIN_P11	P5	10	68	LVDS_DATAIN_N23	H5	6
33	LVDS_DATAIN_N10	M1	10	69	GND		
34	LVDS_DATAIN_N11	P4	10	70	GND		
35	GND			71	LVDS_DATAIN_P24	H4	6
36	GND			72	LVDS_DATAIN_P25	G6	6

Table A-3: **LVDS Receive Connector #1 Pin-out (P6) *(Continued)***

P6	RX#1 Signal Name	U11 Pin#	Bank#	P6	RX#1 Signal Name	U11 Pin#	Bank#
73	LVDS_DATAIN_N24	H3	6	81	GND		
74	LVDS_DATAIN_N25	G5	6	82	GND		
75	GND			83	GND		
76	GND			84	GND		
77	LVDS_FRAMEINB_P	G4	6	85	GND		
78	LVDS_CLKINB_P	E13	1	86	GND		
79	LVDS_FRAMEINB_N	G3	6	87	GND		
80	LVDS_CLKINB_N	D12	1	88	GND		

Table A-4: **LVDS Receive Connector #2 Pin-out (P3)**

P3	RX#2 Signal Name	U11 Pin#	Bank#	P3	RX#2 Signal Name	U11 Pin#	Bank#
1	LVDS_DATAIN_P26	AA14	2	37	LVDS_DATAIN_P38	H2	6
2	LVDS_DATAIN_P27	AA16	2	38	LVDS_DATAIN_P39	G2	6
3	LVDS_DATAIN_N26	AB14	2	39	LVDS_DATAIN_N38	H1	6
4	LVDS_DATAIN_N27	AA15	2	40	LVDS_DATAIN_N39	G1	6
5	GND			41			
6	GND			42			
7	LVDS_DATAIN_P28	V2	10	43			
8	LVDS_DATAIN_P29	T8	10	44			
9	LVDS_DATAIN_N28	V1	10	45	GND		
10	LVDS_DATAIN_N29	U7	10	46	GND		
11	GND			47			
12	GND			48			
13	LVDS_DATAIN_P30	U1	10	49			
14	LVDS_DATAIN_P31	R8	10	50			
15	LVDS_DATAIN_N30	T1	10	51	GND		
16	LVDS_DATAIN_N31	R7	10	52	GND		
17	GND			53			
18	GND			54			
19	LVDS_DATAIN_P32	R6	10	55			
20	LVDS_DATAIN_P33	P8	10	56			
21	LVDS_DATAIN_N32	R5	10	57	GND		
22	LVDS_DATAIN_N33	N8	10	58	GND		
23	GND			59			
24	GND			60			
25	LVDS_DATAIN_P34	L1	10	61			
26	LVDS_DATAIN_P35	M8	10	62			
27	LVDS_DATAIN_N34	K1	10	63	GND		
28	LVDS_DATAIN_N35	L8	10	64	GND		
29	GND			65			
30	GND			66			
31	LVDS_DATAIN_P36	J2	10	67			
32	LVDS_DATAIN_P37	L7	10	68			
33	LVDS_DATAIN_N36	J1	10	69	GND		
34	LVDS_DATAIN_N37	L6	10	70	GND		
35	GND			71			
36	GND			72			

Table A-4: **LVDS Receive Connector #2 Pin-out (P3) *(Continued)***

P3	RX#2 Signal Name	U11 Pin#	Bank#	P3	RX#2 Signal Name	U11 Pin#	Bank#
73				81	GND	81	GND
74				82	GND	82	GND
75	GND			83	GND	83	GND
76	GND			84	GND	84	GND
77	LVDS_FRAMEINA_P	H8	6	85	GND	85	GND
78	LVDS_CLKINA_P	B6	6	86	GND	86	GND
79	LVDS_FRAMEINA_N	H7	6	87	GND	87	GND
80	LVDS_CLKINA_N	C6	6	88	GND	88	GND

Appendix B

HyperTransport Connector

This appendix shows the pin-outs for the HyperTransport Connector (P24).

HyperTransport Connector

Figure B-1 shows the top half of the HyperTransport connector, and Figure B-2 shows the bottom half of the HyperTransport connector. Table B-1 lists the connections for the HyperTransport connector.

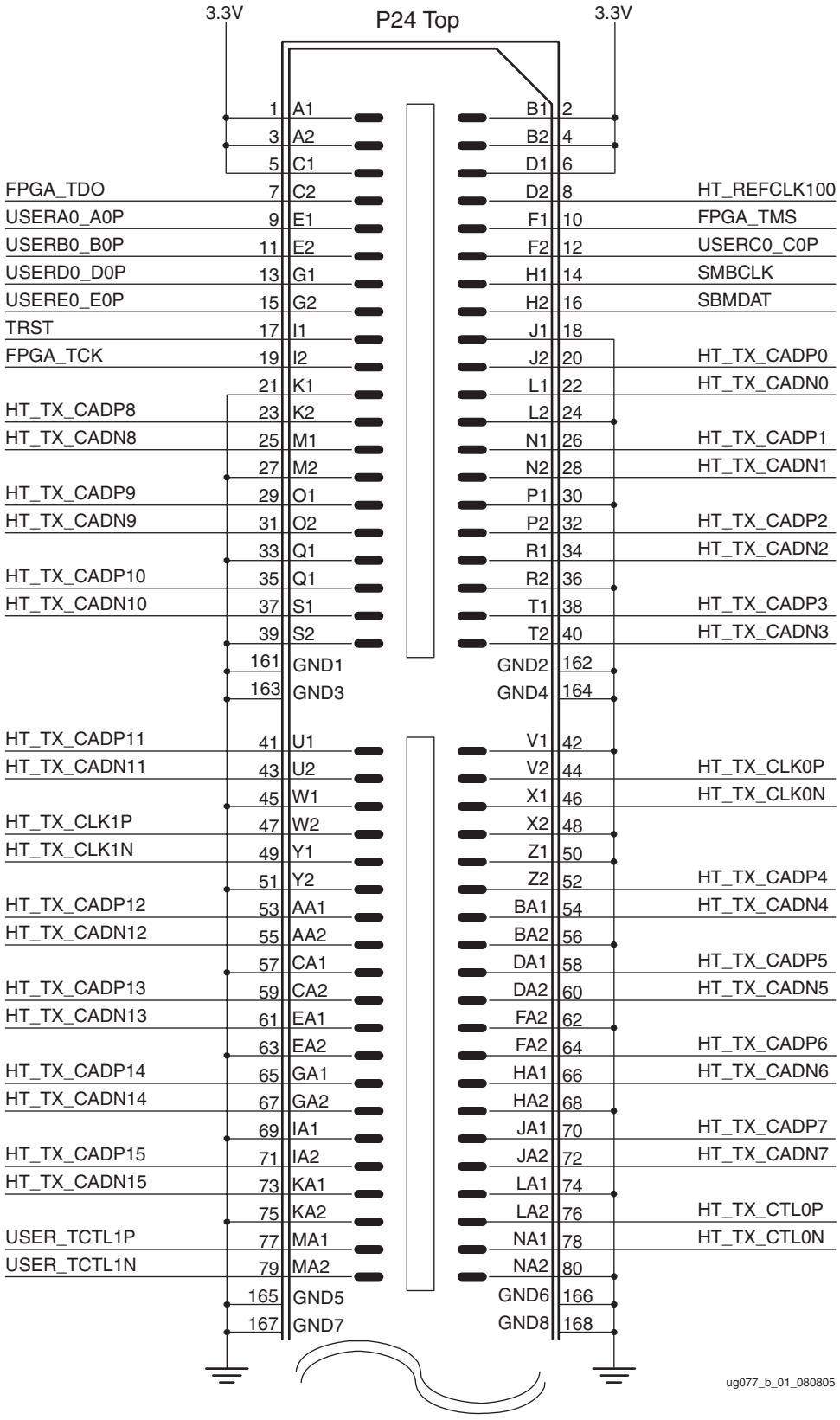


Figure B-1: **HyperTransport Connector Top**

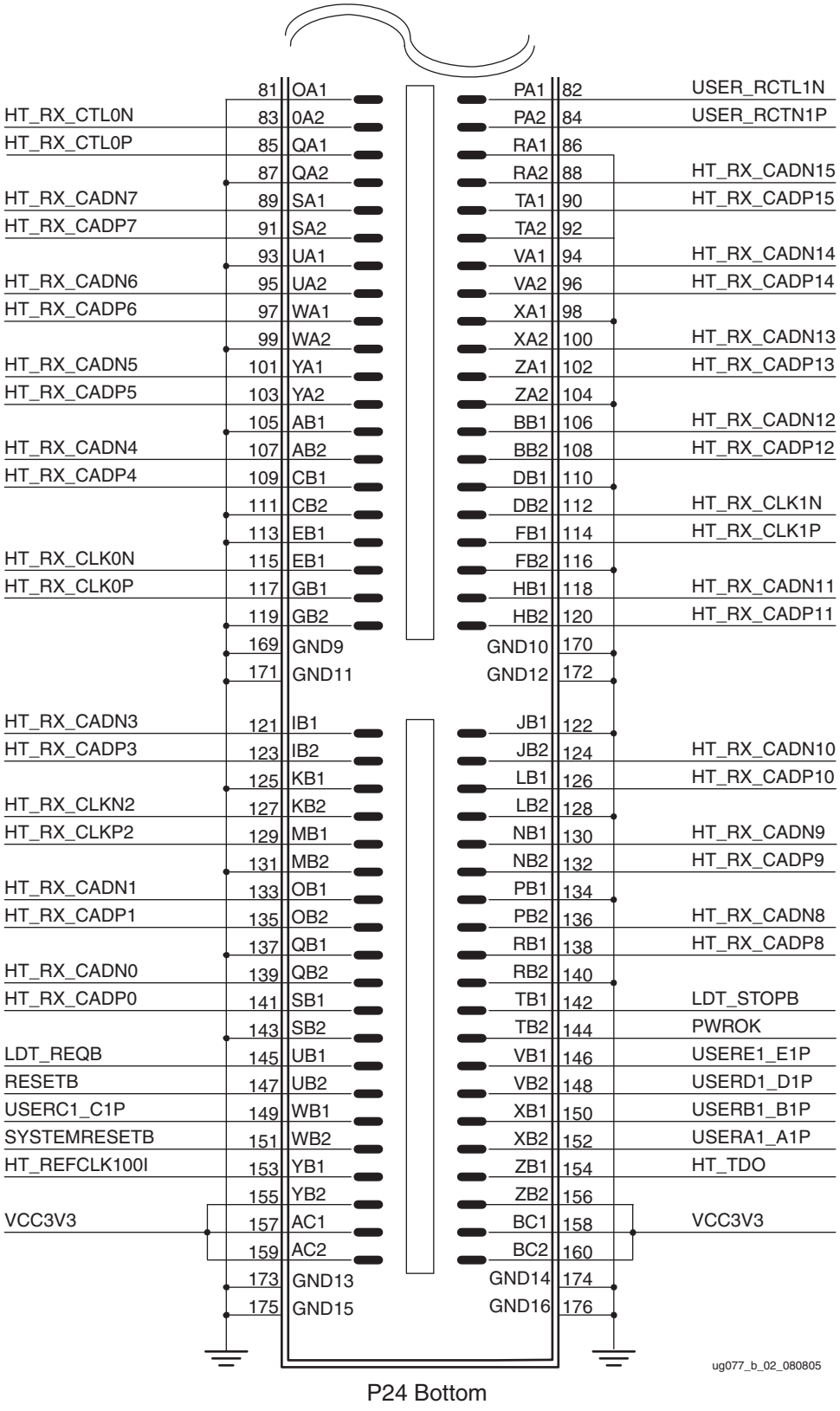


Figure B-2: **HyperTransport Connector Bottom**

HyperTransport Connector Connections

Table B-1 shows the connections for the HyperTransport connector.

Table B-1: **HyperTransport Connector Connections**

P24 Pin	HyperTransport Signal	U11 Pin#	Bank#
1	3.3V		
2	3.3V		
3	3.3V		
4	3.3V		
5	3.3V		
6	3.3V		
7	FPGA_TDO (HT_TDO)	P17.1	
8	HT_REFCLK100	D12	1
9	USERA0_A0P	D2	6
10	FPGA_TMS	Y11	0
11	USERB0_B0P	E1	6
12	USERC0_C0P	E3	6
13	USERD0_D0P	A9	6
14	SMBCLK	F1	6
15	USERE0_E0P	A3	6
16	SMBDAT	E2	6
17	TRST	D1	6
18	GND		
19	FPGA_TCK	W12	0
20	HT_TX_CADP0	F4	6
21	GND		
22	HT_TX_CADN0	F3	6
23	HT_TX_CADP8	A4	6
24	GND		
25	HT_TX_CADN8	B4	6
26	HT_TX_CADP1	A6	6
27	GND		
28	HT_TX_CADN1	A5	6
29	HT_TX_CADP9	A8	6
30	GND		

P24 Pin	HyperTransport Signal	U11 Pin#	Bank#
89	HT_RX_CADN7	A19	5
90	HT_RX_CADP15	C19	5
91	HT_RX_CADP7	A20	5
92	GND		
93	GND		
94	HT_RX_CADN14	B20	5
95	HT_RX_CADN6	A21	5
96	HT_RX_CADP14	C20	5
97	HT_RX_CADP6	A22	5
98	GND		
99	GND		
100	HT_RX_CADN13	B21	5
101	HT_RX_CADN5	A23	5
102	HT_RX_CADP13	C21	5
103	HT_RX_CADP5	A24	5
104	GND		
105	GND		
106	HT_RX_CADN12	C22	5
107	HT_RX_CADN4	C25	5
108	HT_RX_CADP12	D22	5
109	HT_RX_CADP4	C26	5
110	GND		
111	GND		
112	HT_RX_CLK1N	C23	5
113	GND		
114	HT_RX_CLK1P	D23	5
115	HT_RX_CLK0N	D25	5
116	GND		
117	HT_RX_CLK0P	D26	5
118	HT_RX_CADN11	C24	5

Table B-1: **HyperTransport Connector Connections *(Continued)***

P24 Pin	HyperTransport Signal	U11 Pin#	Bank#
31	HT_TX_CADN9	A7	6
32	HT_TX_CADP2	C2	6
33	GND		
34	HT_TX_CADN2	C1	6
35	HT_TX_CADP10	C4	6
36	GND		
37	HT_TX_CADN10	D4	6
38	HT_TX_CADP3	D10	6
39	GND		
40	HT_TX_CADN3	C10	6
41	HT_TX_CADP11	D3	6
42	GND		
43	HT_TX_CADN11	E4	6
44	HT_TX_CLK0P	C5	6
45	GND		
46	HT_TX_CLK0N	D5	6
47	HT_TX_CLK1P	B7	6
48	GND		
49	HT_TX_CLK1N	C7	6
50	GND		
51	GND		
52	HT_TX_CADP4	C17	5
53	HT_TX_CADP12	D9	6
54	HT_TX_CADN4	D17	5
55	HT_TX_CADN12	C8	6
56	GND		
57	GND		
58	HT_TX_CADP5	F10	6
59	HT_TX_CADP13	E6	6
60	HT_TX_CADN5	E10	6
61	HT_TX_CADN13	E5	6
62	GND		

P24 Pin	HyperTransport Signal	U11 Pin#	Bank#
119	GND		
120	HT_RX_CADP11	D24	5
121	HT_RX_CADN3	G9	6
122	GND		
123	HT_RX_CADP3	G10	6
124	HT_RX_CADN10	E18	5
125	GND		
126	HT_RX_CADP10	F18	5
127	HT_RX_CADN2	D19	5
128	GND		
129	HT_RX_CADP2	D20	5
130	HT_RX_CADN9	D21	5
131	GND		
132	HT_RX_CADP9	E21	5
133	HT_RX_CADN1	F23	5
134	GND		
135	HT_RX_CADP1	F24	5
136	HT_RX_CADN8	G17	5
137	GND		
138	HT_RX_CADP8	G18	5
139	HT_RX_CADN0	K25	9
140	GND		
141	HT_RX_CADP0	K26	9
142	LDT_STOPB	D16	1
143	GND		
144	PWROK	E13	1
145	LDT_REQB	C16	1
146	USERE1_E1P	B3	6
147	RESETB	E24	5
148	USERD1_D1P	B9	6
149	USERC1_C1P	E25	5
150	USERB1_B1P	B24	5

Table B-1: **HyperTransport Connector Connections *(Continued)***

P24 Pin	HyperTransport Signal	U11 Pin#	Bank#
63	GND		
64	HT_TX_CADP6	F8	6
65	HT_TX_CADP14	E7	6
66	HT_TX_CADN6	G8	6
67	HT_TX_CADN14	D6	6
68	GND		
69	GND		
70	HT_TX_CADP7	D8	6
71	HT_TX_CADP15	E9	6
72	HT_TX_CADN7	D7	6
73	HT_TX_CADN15	F9	6
74	GND		
75	GND		
76	HT_TX_CTL0P	E17	5
77	USER_TCTL1P	F7	6
78	HT_TX_CTL0N	F17	5
79	USER_TCTL1N	G7	6
80	GND		
81	GND		
82	USER_RCTL1N	E14	1
83	HT_RX_CTL0N	A18	5
84	USER_RCTL1P	D15	1
85	HT_RX_CTL0P	B18	5
86	GND		
87	GND		
88	HT_RX_CADN15	D18	5

P24 Pin	HyperTransport Signal	U11 Pin#	Bank#
151	SYSTEMRESETB	F26	5
152	USERA1_A1P	B23	5
153	HT_REFCLK100I	E26	5
154	HT_TDO	P17.3	
155	3.3V		
156	3.3V		
157	3.3V		
158	3.3V		
159	3.3V		
160	3.3V		
161	GND		
162	GND		
163	GND		
164	GND		
165	GND		
166	GND		
167	GND		
168	GND		
169	GND		
170	GND		
171	GND		
172	GND		
173	GND		
174	GND		
175	GND		
176	GND		

Appendix C

Clock Interfaces

This appendix is extracted from the *XLVDSPRO Demonstration Boards User Guide* (UG037). It describes the clock modules for the XLVDSPRO demonstration boards. These clock modules are identical to those used for the ML450 Development Board. The documentation is reproduced here for convenience.

General

A modular clock approach is implemented for maximum flexibility. Clock inputs have no fixed clock devices but are routed to a set of small high-speed connectors. Small boards, with all possible clocking devices, can be plugged onto these connectors.

Clock Hardware Design

Eight of the FPGA's clock inputs, bundled into four differential inputs, are routed to a set of small high-speed connectors. Each connector can carry a small board with a dedicated clock source.

Figure C-1 shows the layout of the connector on the FPGA board.

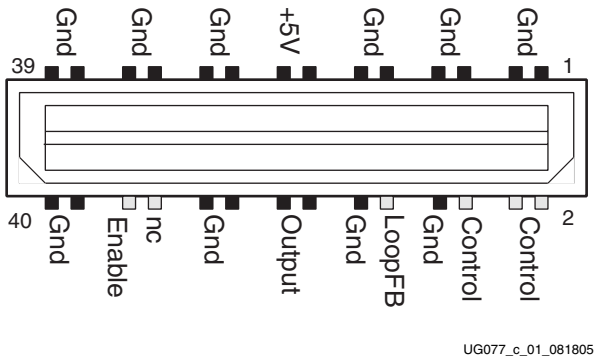


Figure C-1: **Clock Connector**

The connector on the small clock PCBs must be a Samtec QTE type.

Universal QTE and QSE connectors are on the board schematics. The differential connectors are derived from these fully populated connectors.

Small clock device PCBs can be plugged in the connectors. When developed, each of these small boards requires a standard approach:

- The board supply is 5V. Local voltage conversion is needed. A local, small power supply minimizes possible noise, giving better results. A small standard or adjustable very low noise regulator can be used.
- Four control lines, CTRL#[1 to 3]*A/B* and LoopF*A/B*, can be used to control a possible clocking device. These four control lines are shared with the second clock on that side of the FPGA. The level of these control signals is 2.5V LVTTL or LVCMOS.
- The clock signal to the FPGA is always differential. This choice is made because of good noise immunity. In order to get a good quality clock signal, the generated clock is best passed through a quality LVDS or LVPECL driver.
- A clock board enable pin is routed to a DIP switch set.

Figure C-2 shows the hardware schematic diagram for the Clock board.

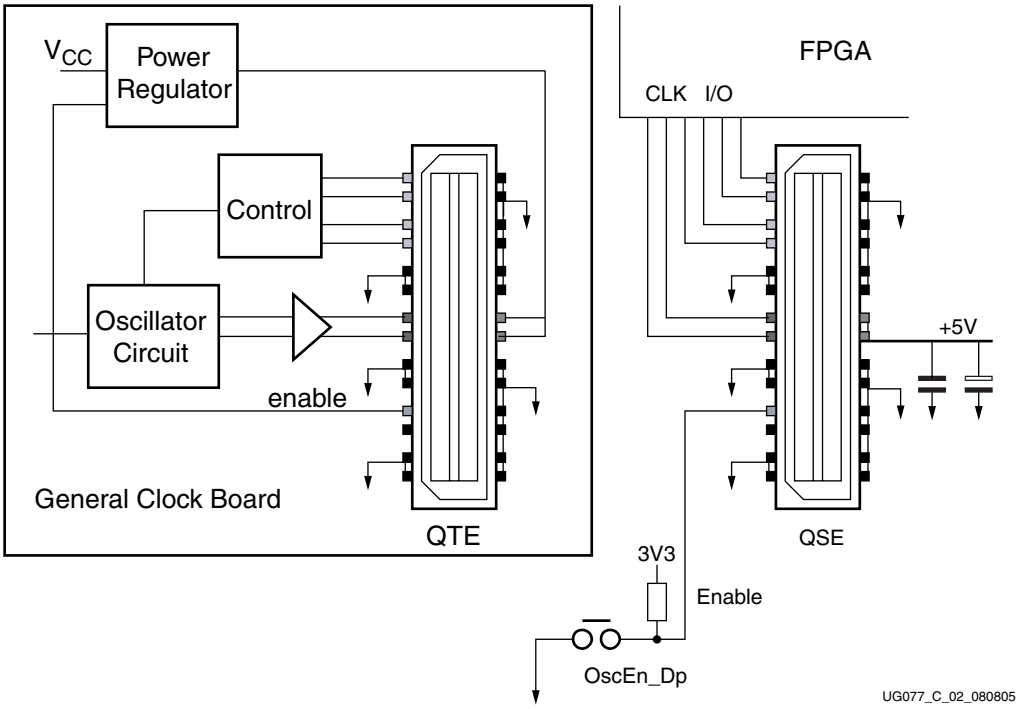


Figure C-2: **Clock Board Schematic Diagram**

Table C-1 lists the FPGA clock pin connections.

Table C-1: **FPGA Clock Connections**

Side	Bank	Pin Name	Pin #	Clock Type	Clock Source
Top	Bank_0	IO_L74N_0 / GCLK_7P	C16		
		IO_L74P_0 / GCLK_6S	B16		
		IO_L75N_0 / GCLK_5P	G16	BREFCLK	To Clock Connector
		IO_L75P_0 / GCLK_4S	F16		
	Bank_1	IO_L75N_1 / GCLK_3P	F15	BREFCLK2	To Clock Connector
		IO_L75P_1 / GCLK_2S	G15		
		IO_L74N_1 / GCLK_1P	B15		EXTOSC1 EXTOSC2
		IO_L74P_1 / GCLK_0S	C15		
Bottom	Bank_4	IO_L74N_4 / GCLK_3S	AF15		X_CLK1 X_CLK2
		IO_L74P_4 / GCLK_2P	AG15		
		IO_L75N_4 / GCLK_1S	AH15	BREFCLK2	To Clock Connector
		IO_L75P_4 / GCLK_0P	AJ15		
	Bank_5	IO_L75N_5 / GCLK_7S	AJ16	BREFCLK	To Clock Connector
		IO_L75P_5 / GCLK_6P	AH16		
		IO_L74N_5 / GCLK_5S	AG16		
		IO_L74P_5 / GCLK_4P	AF16		

Peripheral Devices

The following devices can be used as clock board components. Examples of these are listed in the next section.

- Epson EG-2101CA SAW oscillators
- Micrel SY89430V Programmable frequency generator
- Champion F17350B, F17355B VCXO
- Vite VCC1 Oscillators Oscillators
- Mini-Circuits Small transformers
- ICS Inc. ICS8430-11 700-MHz, low jitter, LVCMOS-to-3.3V LVPECL frequency synthesizer
- ICS Inc. ICS8442 700-MHz, crystal oscillator-to-differential LVDS frequency synthesizer

Design Examples

This section provides examples of different clock boards.

Normal Oscillator

Figure C-3 shows a possible design of a clock board containing a normal clock oscillator.

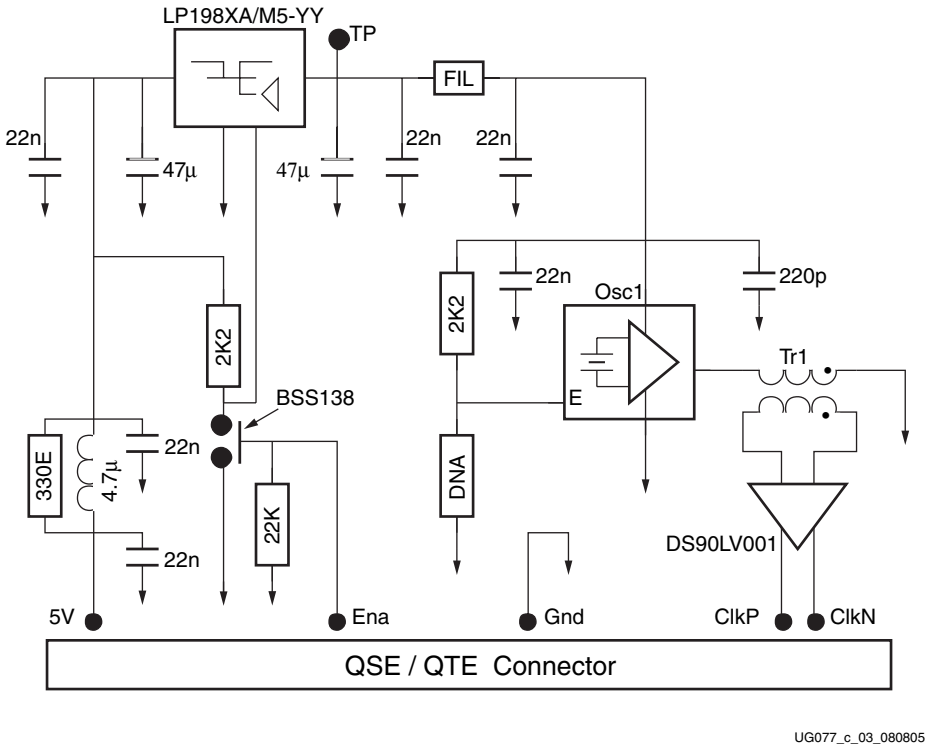


Figure C-3: **Single-Ended Oscillator**

It is possible to use the LVDS repeater device due to its very low jitter and skew levels and high-frequency possibilities.

SAW Oscillator

Figure C-4 shows a clock board with a SAW oscillator, such as the Epson EG2121CA. This design is nearly identical to the single-ended oscillator design.

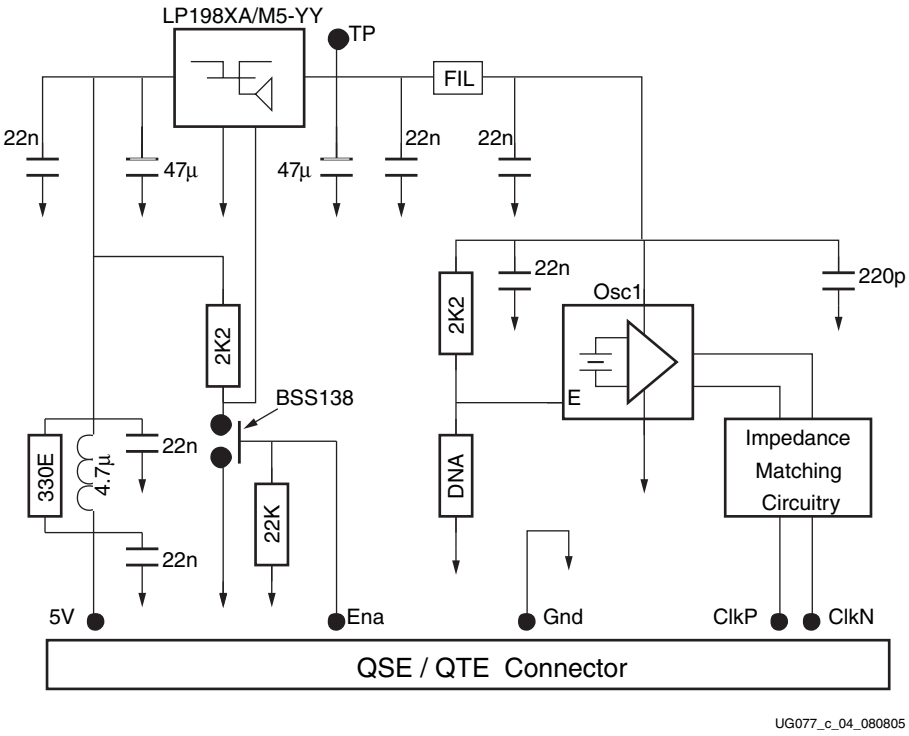


Figure C-4: **SAW Oscillator**

VCXO / VCO

Figure C-5 shows another basic oscillator board made with a VCXO or VCO device. Contrary to normal oscillators, this device needs feedback from the FPGA using one of the control lines.

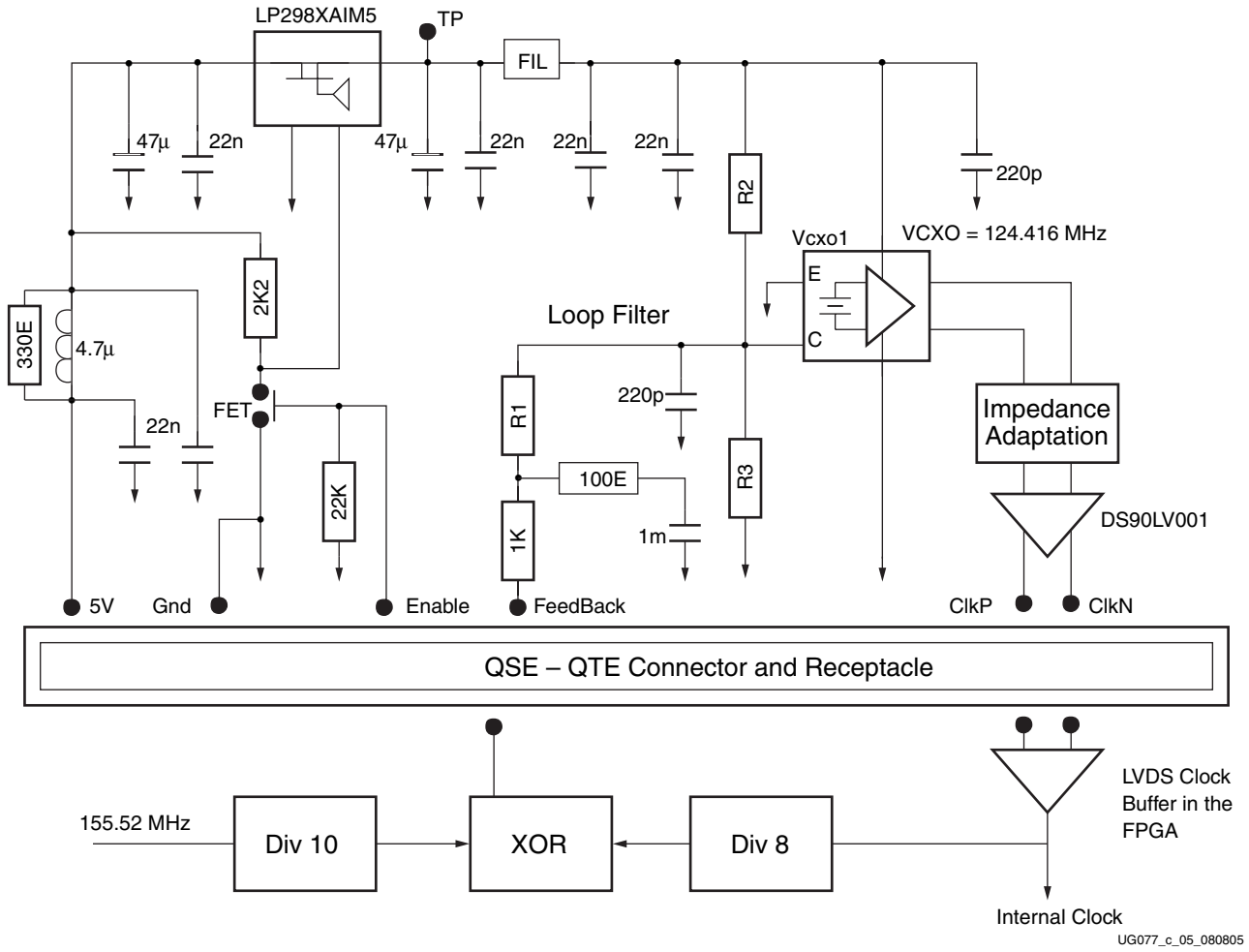


Figure C-5: **VCO/VCXO Oscillator (Example 1)**

The value and mounting of resistors R1, R2, and R3 depends on the VCXO type used (see Figure C-6).

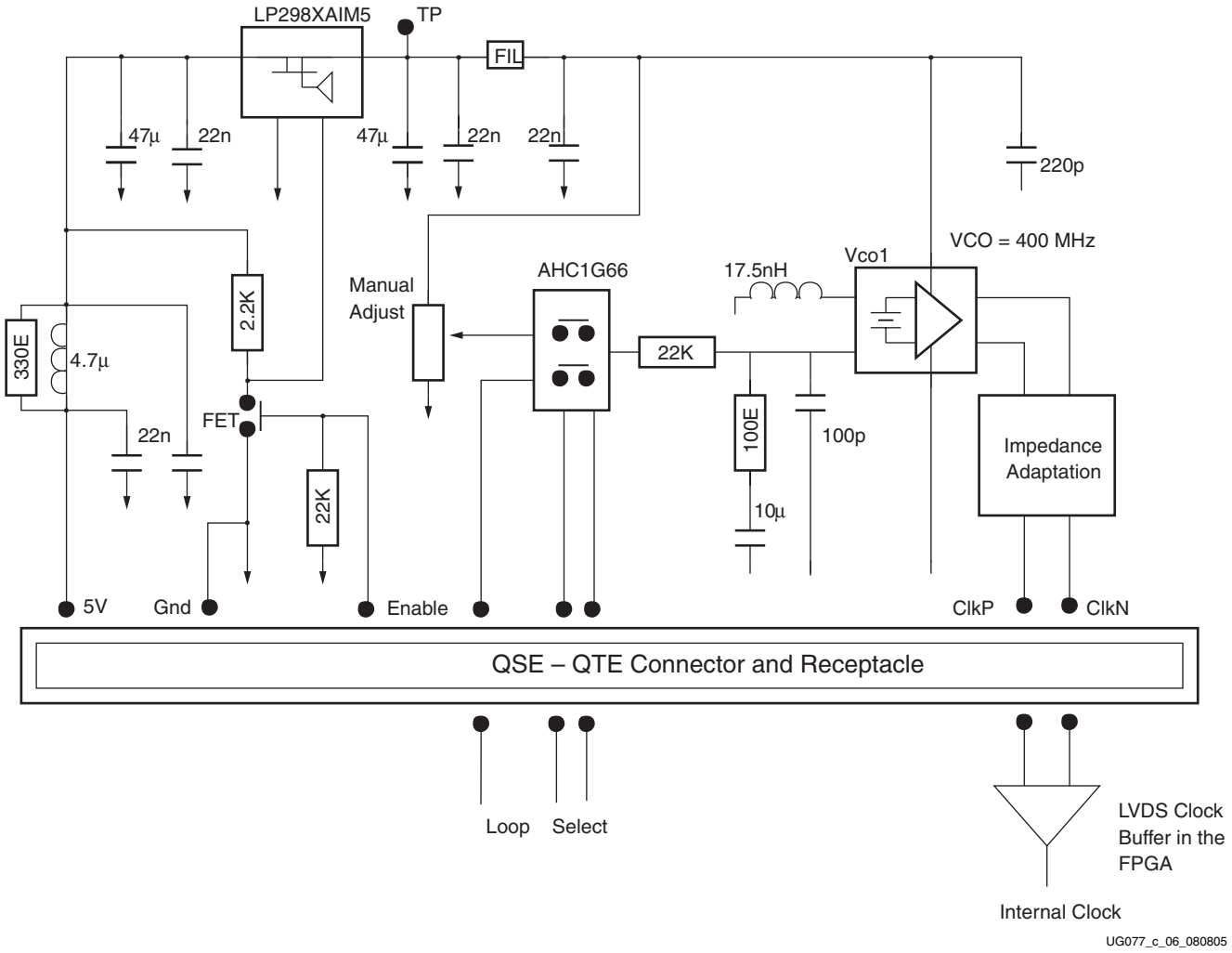


Figure C-6: **VCO/VCXO Oscillator (Example 2)**

Figure C-5 and Figure C-6 are shown for documentation purposes only. The real implementation of these solutions can be found in the schematics.

Programmable Frequency Synthesizer

Programmable frequency synthesizers can generate a wide range of frequencies between given minimum and maximum boundaries. ICS manufactures two synthesizers (ICS8430-11 and ICS8442). Their characteristics are summarized below:

- Output frequency up to 700 MHz
- Differential PECL outputs
- Crystal input frequency range: 14 MHz - 25 MHz
- VCO range: 200 MHz - 700 MHz
- Parallel or serial interface for programming counter and output dividers
  - RMS period jitter: between 2.5 ps and 2.7 ps (typical)
  - Cycle-to-cycle jitter: between 15 ps and 18 ps (typical)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature

Possible applications in which these devices are used are summarized below:

- Advanced communications
- High-end consumer
- High-performance computing
- RISC CPU clock
- Graphics pixel clock
- Test equipment
- Other high-performance processor-based applications

Figure C-7 shows an implementation using these devices.

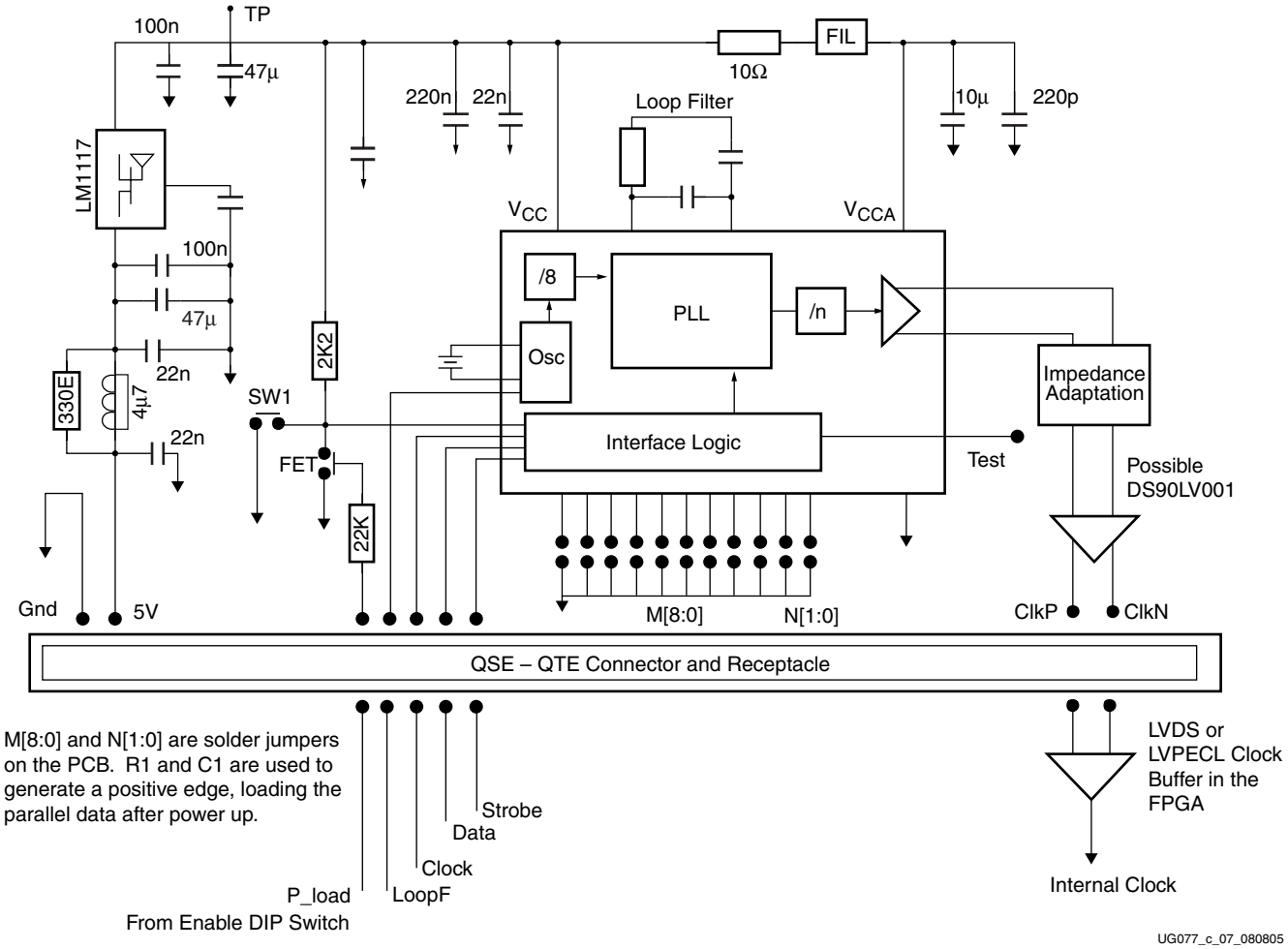


Figure C-7: **ICS Clock Board**

Depending on the device used, small device differences exist, resulting in a different layout of the PCB.

Figure C-7 is shown for documentation purposes only. The real implementation of this design can be found in the schematics.

Because these synthesizers are high-speed devices, the PCB must be made accordingly. Refer to the PCB layout specifications given by the manufacturer:

- ICS: Specifications are included in the data sheet.
- Micrel: Download Application Notes, AN-07 and AN-07 addendum.

The differences between the ICS and MICREL devices are listed in the following table.

Table C-2: **ICS and MICREL Synthesizer Comparison**

Micrel	ICS
M[8:0]	M[8:0]
N[1:0]	N[2:0]
Test	Test
F_{OUT}, $\overline{F}_{OUT}$	F_{OUT0}, $\overline{F}_{OUT0}$
	F_{OUT1}, $\overline{F}_{OUT1}$
Xtal1, Xtal2	Xtal1, Xtal2
	Xtal_Sel
	Test_Clk
	VCO_Sel
P_load	nP_load
S_load	S_load
S_data	S_data
S_clock	S_clock
V_{CC}	V_{CC}
	V_{EE}
V_{CC_QUIT}	V_{CCA}
28-pin PLCC	32-pin LQFP

For both devices, the value of N is the divider value of the output, while the M value is the PLL loop divider. Due to the differences in output frequency, both components have a slightly different range of settings.

The parallel inputs for the M-value simply can be connected to ground where needed, as indicated in Table C-3. Internal pull-up resistors are provided.

Table C-3: **M[8:0] Frequency Table**

VCO Frequency (MHz)	M div	256	128	64	32	16	8	4	2	1		
		M8	M7	M6	M5	M4	M3	M2	M1	M0		
200	100	0	0	1	1	0	0	1	0	0		ICS
202	101	0	0	1	1	0	0	1	0	1		
…….	…….	…….	…….	……	……	……	……	……	……	……		
…….	…….	…….	…….	……	……	……	……	……	……	……		
400	200	0	1	1	0	0	1	0	0	0	MICREL	
402	201	0	1	1	0	0	1	0	0	1		
…….	…….	…….	…….	……	……	……	……	……	……	……		
…….	…….	…….	…….	……	……	……	……	……	……	……		
696	348	1	0	1	0	1	1	1	0	0		
698	349	1	0	1	0	1	1	1	0	1		
700	350	1	0	1	0	1	1	1	1	0		
…….	…….	…….	…….	……	……	……	……	……	……	……		
…….	…….	…….	…….	……	……	……	……	……	……	……		
946	473	1	1	1	0	1	1	0	0	0		
948	474	1	1	1	0	1	1	0	0	1		
950	475	1	1	1	0	1	1	0	1	0		

The test output of both devices gives some insight to the internal component nodes. Due to the compact design of the Micrel component, its test output has more capabilities than the ICS device (see Table C-4), while ICS has provided extra inputs for testing purposes.

Table C-4: **Test Outputs**

MICREL				ICS		
T2	**T1**	**T0**	**Test**	**T1**	**T0**	**Test**
0	0	0	Data Out – LSB SR	0	0	Low
0	0	1	High	0	1	S-Data
0	1	0	Fref	1	0	M counter
0	1	1	M counter	1	1	CMOS F_{OUT}
1	0	0	F_{OUT}			
1	0	1	Low			
1	1	0	S-clock/M			
1	1	1	$F_{OUT}/4$			

At power up, a parallel load of the registers occurs when S_load is Low, and a Low-to-High transition occurs at P_load. A serial load of the registers happens as shown in Figure C-8.

Parallel loads have priority over serial loads.

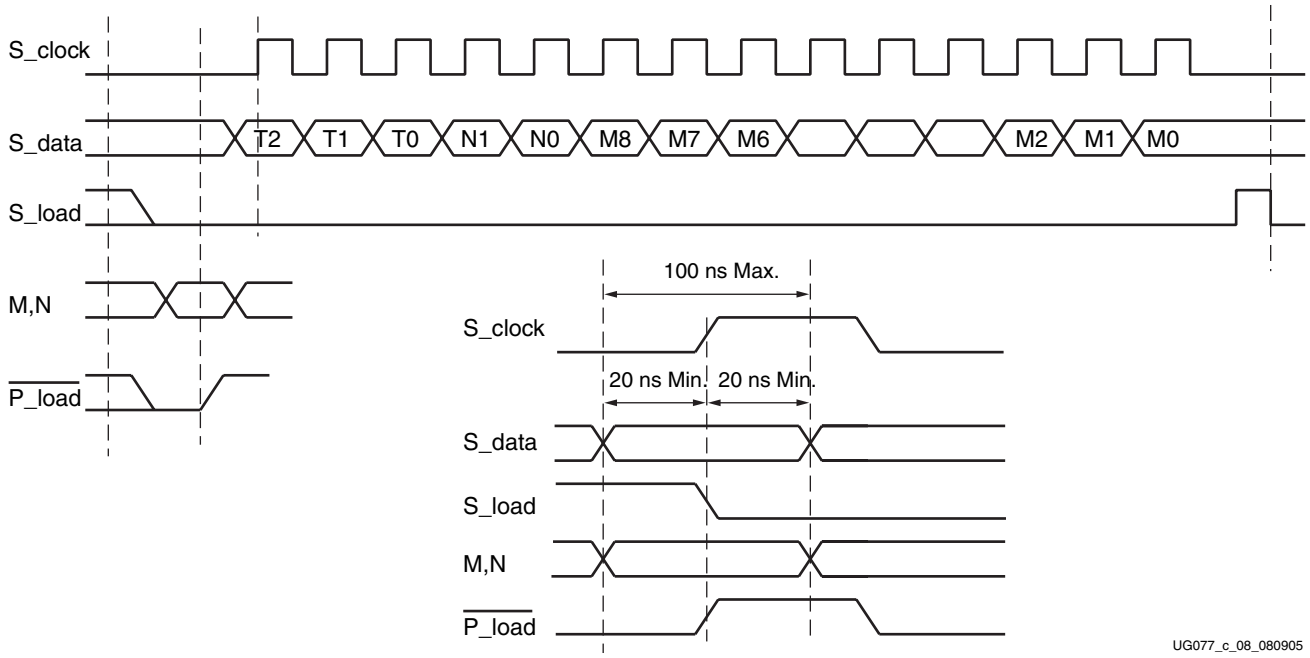


Figure C-8: **Serial Configuration Interface Timing**

Clock Feed Through

Two clock feed-through boards are available to take a clock from an external clock source such as a measurement oscillator device or even from a clock source of one of the MGTs.

One board converts a differential external input to LVDS signal levels (see Figure C-9). The other board accepts a single-ended clock and transforms it into a differential LVDS clock for the FPGA (see Figure C-10).

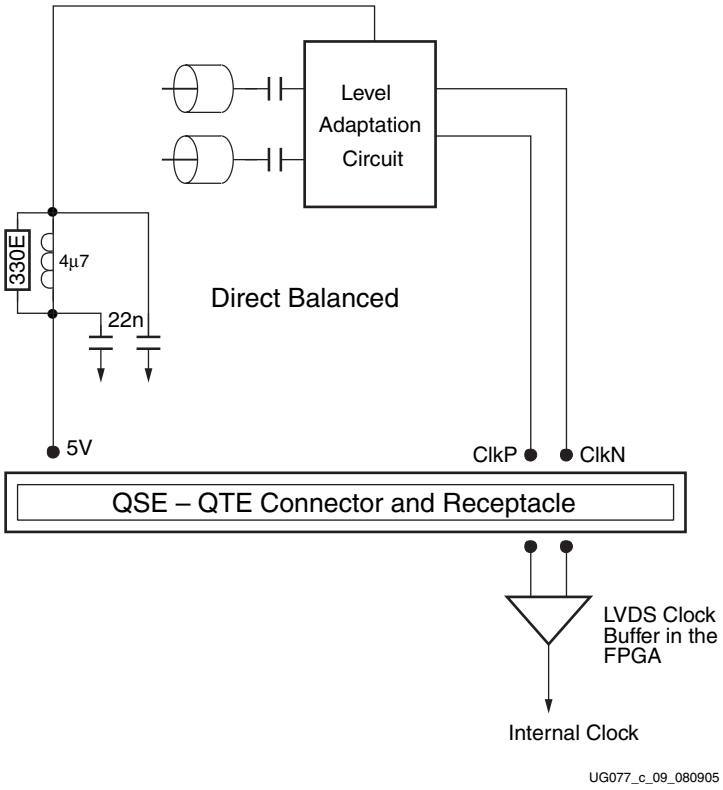


Figure C-9: **External Differential Clock**

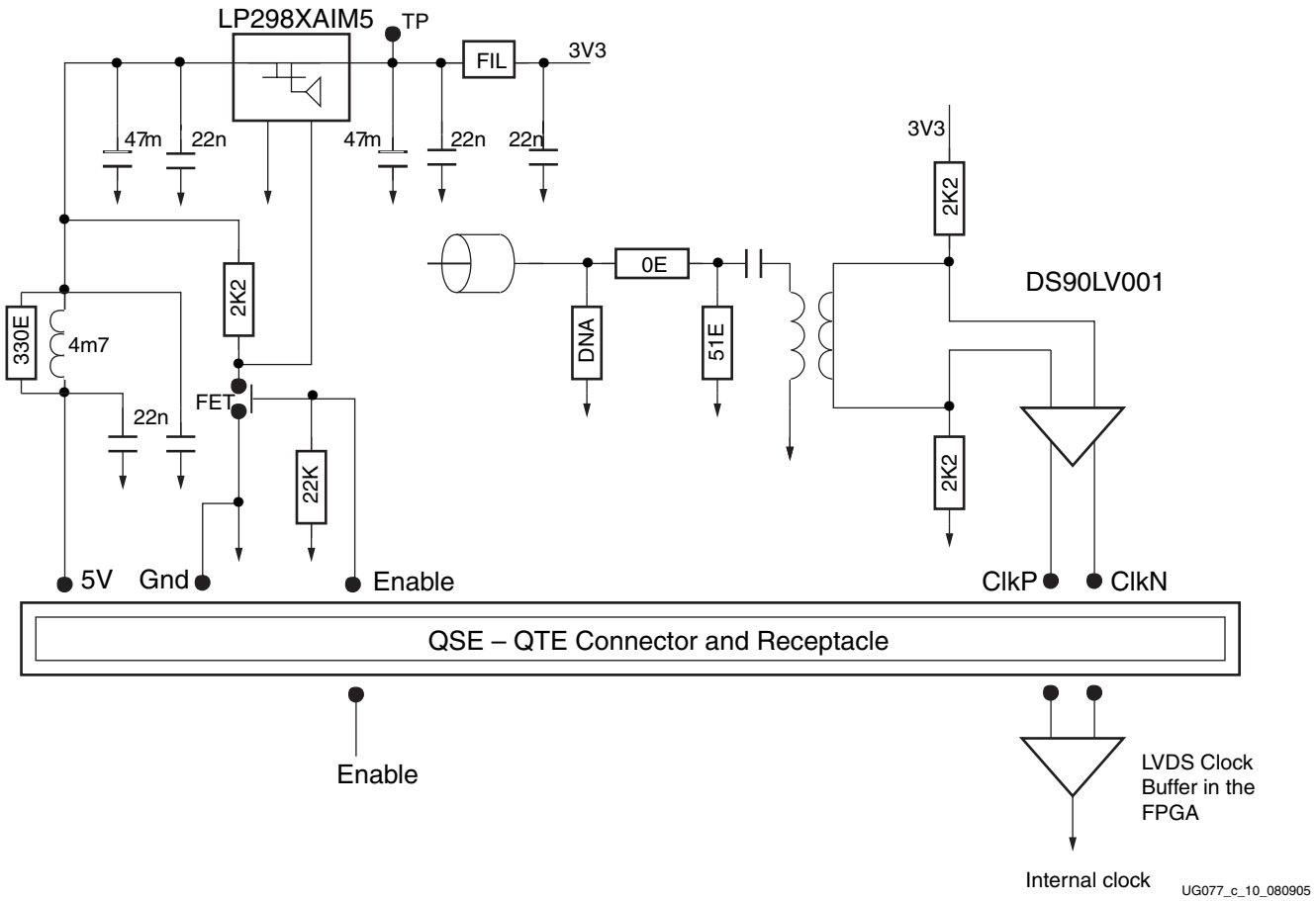


Figure C-10: **External Single-Ended Clock**

Design Solutions

Several boards use the same kind of circuits and design solutions. This section describes some of them.

LVDS Conversion

The LVDS DC specifications (LVDS_25) are listed in the *Virtex-4 Data Sheet*.

In order to guarantee that external clock signals as well as differential PECL outputs of oscillators comply to the LVDS specifications, a circuit with a micro-power voltage reference diode is used. This diode ensures that the common mode input voltage is held at 1.2V. The capacitive coupling of the input signals and the 2.2 KΩ resistors give a good signal quality within the requested Xilinx LVDS specifications.

In one of the designs, an external single-ended clock signal is taken and converted to a differential LVDS signal using a small transformer (UN_BAL). The signal level set there is ~1.5V. The small resistance of the transformer keeps the input of the LVDS transmitter device stable when no input signal is applied.

Power Supply Filtering

Every small clock board has an input low-pass PI filter. This filter cancels high-input noise from the 5V system power supply.

Frequencies above ~700 KHz are filtered. The parallel resistor on the coil kills the Q-factor of the small coil.

Linear 3.3V Regulator

On different boards, a fixed output voltage, low-noise, low-drop regulator is used to convert 5V to 3.3V.

In order to get the required low-noise and low-drop behavior, the linear regulator requires external capacitors for regulator stability. These capacitors must be selected carefully for good performance.

Input Capacitor

For excellent low-noise specifications, it is recommended that the input of the linear regulator has an input capacitor > 1µF placed within less than 1 cm.

A bulk 47µF tantalum capacitor, with sufficient surge current ratings, and a high-frequency ceramic capacitor are implemented in the different designs.

Output Capacitor

The linear regulator requires a low ESR output capacitor that meets the requirement for minimum amount of capacitance and also has an ESR value within the stable range. Manufacturers provide curves that show the stable ESR range as a function of load current. The capacitors used in these designs are 47µF low ESR (0.28 Ω), SMD tantalum capacitors supplied by Vishay or Nichicon.

Bypass Capacitor

To significantly reduce noise, a 10 nF capacitor should be connected at the Bypass pin of the regulator. The types of capacitors best suited for the noise bypass capacitor are ceramic

and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. Two 4.7 nF NPO capacitors are used here.

On/Off Operation

The regulator is turned off when the ON/OFF pin is Low. It is turned on when this pin is High. To satisfy the manufacturers specifications, the ON/OFF input must be able to swing above and below the specified turn-on and turn-off voltage thresholds listed in the Electrical Characteristics, and the turn-on (and turn-off) voltage signals applied to the ON/OFF input must have a slew rate which is >40mV/µs. A small MOSFET is used to turn the regulator on or off.

Web References

- http://www.viteonline.com
- http://www.vishay.com
- http://www.champtech.com
- http://www.micrel.com/product-info/products/SY89430V.html
- http://www.icst.com/products/summary/ics8430-11.htm
- http://products.analog.com/products/info.asp?product=ADP3338
- http://www.minicircuits.com/
- http://www.minicircuits.com/dg02-204.pdf
- http://www.national.com/search/search.cgi/main?keywords=DS90LV
- http://www.national.com/pf/LP/LP2985.html
- http://www.national.com/pf/LM/LM385.html

Array Connector Numbering

These clock sources are not routed to or through the Array connectors.

UCF Information

```
#
# Main Clock Inputs
#
# NET " " LOC "C16";       #LVDSCLKA_N see also in Receive Bank 7 section IO0L74N/GCLK7P
# NET " " LOC "B16";       #LVDSCLKA_P see also in Receive Bank 7 section IO0L74P/GCLK6S
# NET " " LOC "G16";       #CLKMODULE_0_N                                 IO0L75N/GCLK5P
# NET " " LOC "F16";       #CLKMODULE_0_P                                 IO0L75P/GCLK4S
# NET " " LOC "C15";       #EXTOSCP2                                      IO1L74P/GCLK0S
# NET " " LOC "B15";       #EXTOSCP1                                      IO1L74N/GCLK1P
# NET " " LOC "G15";       #CLKMODULE_1_P                                 IO1L75P/GCLK2S
# NET " " LOC "F15";       #CLKMODULE_1_N                                 IO1L75N/GCLK3P
# NET " " LOC "AF15";      #X_CLK1                                        IO4L74N/GCLK3S
# NET " " LOC "AG15";      #X_CLK2                                        IO4L74P/GCLK2P
# NET " " LOC "AH15";      #CLKMODULE_2_N                                 IO4L75N/GCLK1S
# NET " " LOC "AJ15";      #CLKMODULE_2_P                                 IO4L75P/GCLK0P
# NET " " LOC "AF16";      #LVDSCLKB_P see also in Receive Bank 6 section IO5L74P/GCLK4P
# NET " " LOC "AG16";      #LVDSCLKB_N see also in Receive Bank 6 section IO5L74N/GCLK5S
# NET " " LOC "AH16";      #CLKMODULE_3_P                                 IO5L75P/GCLK6P
# NET " " LOC "AJ16";      #CLKMODULE_3_N                                 IO5L75N/GCLK7S
#
# Clock Control Signals
#
# NET " " LOC "AB16";      # CTRL#1A                                      IO5L67P
# NET " " LOC "AC16";      # CTRL#2A                                      IO5L67N
# NET " " LOC "AD17";      # CTRL#3A                                      IO5L68P
# NET " " LOC "AE17";      # LOOPFA                                       IO5L68N
# NET " " LOC "AF17";      # CTRL#1B                                      IO5L69P
# NET " " LOC "AG17";      # CTRL#2B                                      IO5L69N
# NET " " LOC "AD16";      # CTRL#3B                                      IO5L73P
# NET " " LOC "AE16";      # LOOPFB                                       IO5L73N
#
```

Appendix D

LCD Interface

This appendix is extracted from the *XLVDSPRO Demonstration Boards User Guide* (UG037). It describes the LCD interface for the XLVDSPRO demonstration boards, which is identical to that used in the ML450 Development Board. The documentation is reproduced here for convenience.

General

The XlvdsPro_PwrIo board has a full graphical LCD display. This display has been chosen because of its possible use in embedded systems. A character-type display also can be connected because the graphical LCD used has the same interface as all character-type LCD panels.

A hardware character generator must be designed in order to display characters on the screen.

Display Hardware Design

The FPGA (I/O functioning at 2.5V) is connected to the graphic LCD display through a set of voltage-level converting devices. These switches translate the 2.5 I/O voltage to a 3.3V voltage for the LCD display.

To use the display, DIP switch 4 of the switch array DIP1 must be closed. When this switch is open, the I/O used for the LCD can be used for other applications through the SamArray connectors.

A graphics-based LCD panel from DisplayTech (64128EFCBC-XLP) is used on the Virtex-II Pro board. The control for this LCD panel is based on the KS0713 controller from Samsung. The KS0713 is a 65-column, 132-segment driver-controller device for graphic dot matrix LCD display systems. The chip accepts serial or parallel display data. The 8-bit parallel interface is compatible with most LCD panel manufacturers. The serial connection mode is write only.

Extra features added to the interface in addition to the normal parallel signals are:

- Intel or Motorola compatible interface
- External reset of the chip
- External chip select

The interface also contains the following built-in options for the display and controller:

- On-chip oscillator circuitry
- On-chip voltage converter (x2, x3, x4, and x5)
- A 64-step electronic contrast control function

Table D-1 summarizes the controller specifications.

Table D-1: **Display Controller Specifications**

Parameter	Specification
Supply voltage	2.4V to 3.6V (V_{DD})
LCD driving voltage	4V to 15V (V_{LCD} = V0 - V_{DD})
Power consumption	70µA typical (V_{DD} = 3V, x4 boost, V0 = 11V, internal supply = ON)
Sleep mode	2µA
Standby mode	10µA

The on-chip RAM size is 65x132 = 8580 bits.

Hardware Schematic Diagram

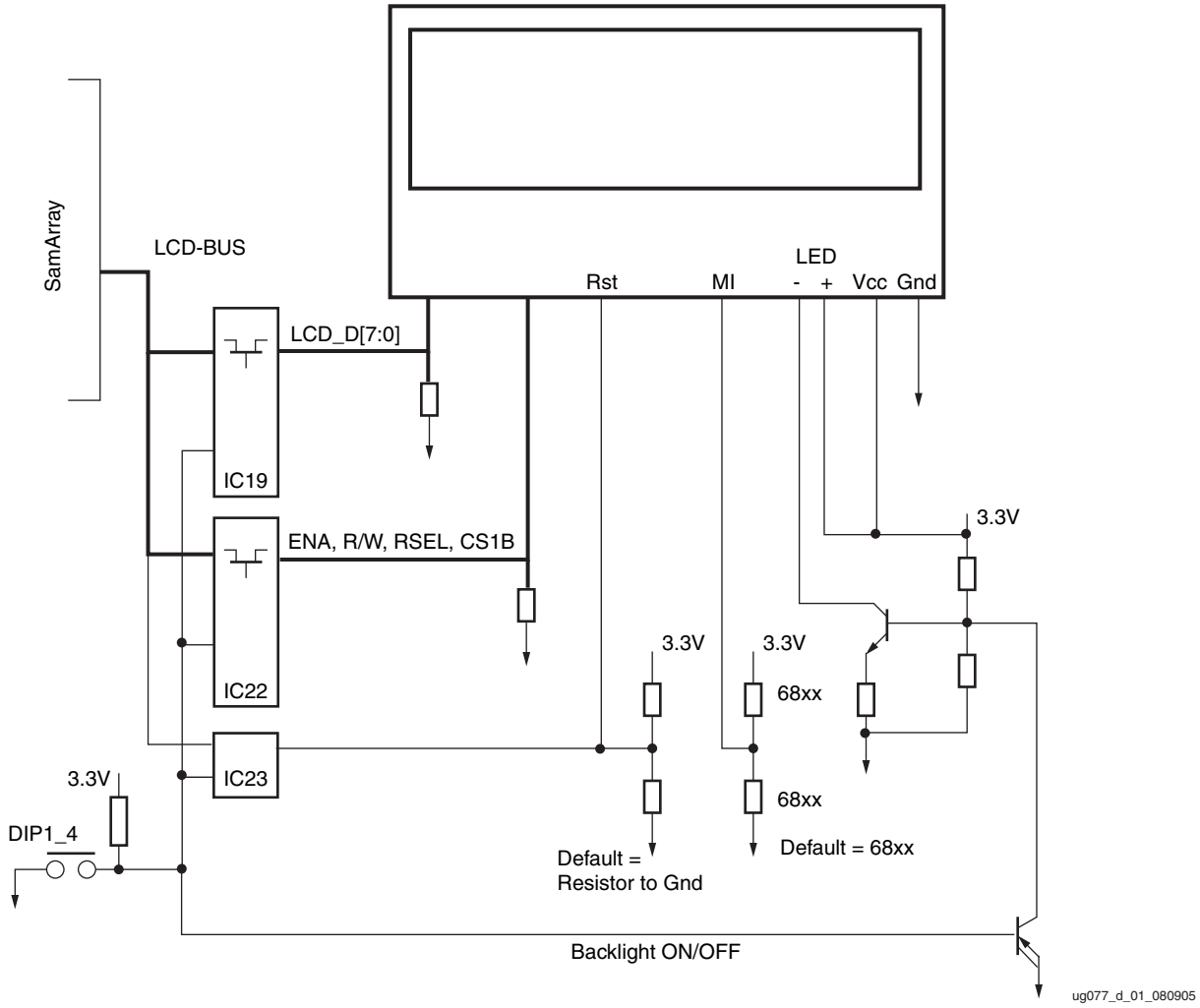


Figure D-1: **Display Schematic Diagram**

Peripheral Device KS0713

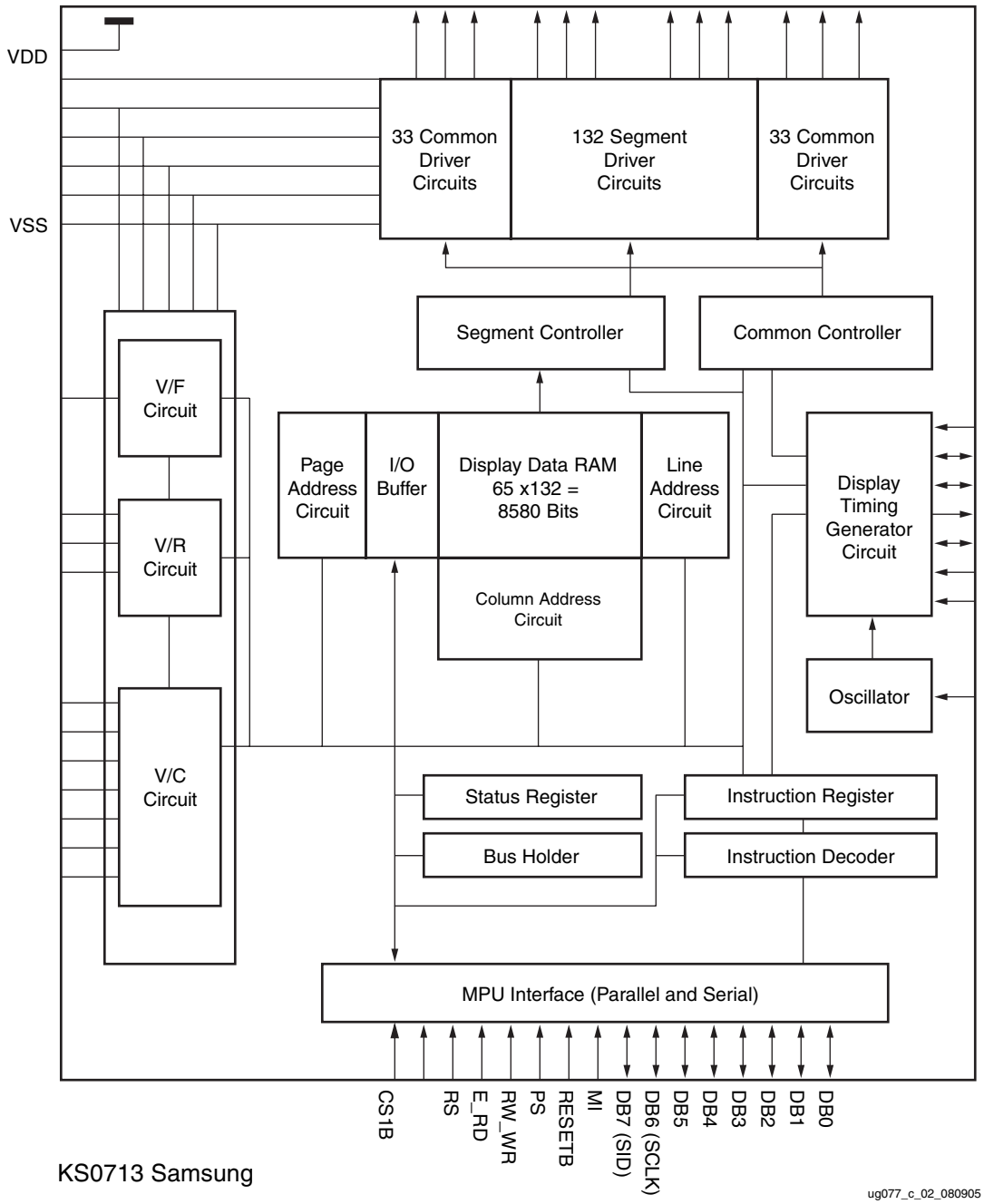


Figure D-2: **KS0713 Block Diagram**

Figure D-2 shows only the signals of interest for the LCD controller. Download the data sheet from the Samsung web pages for a complete signal listing.

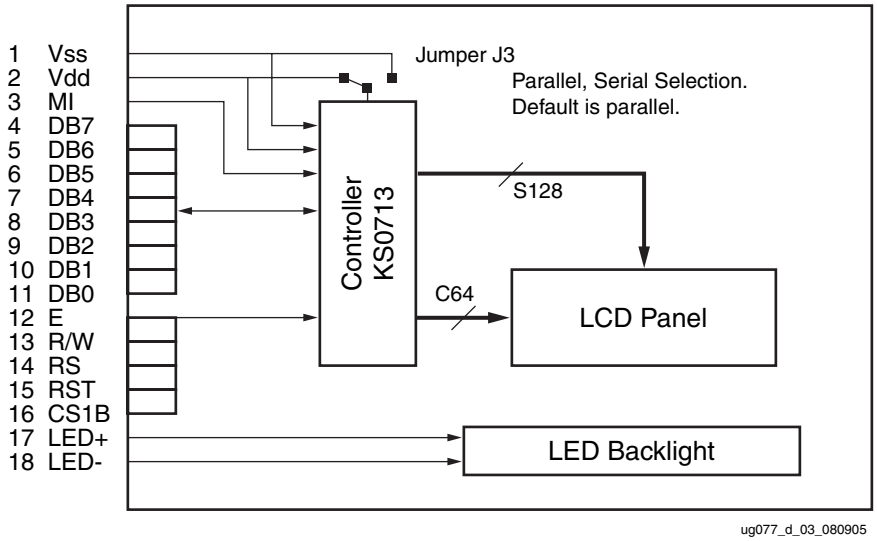


Figure D-3: **64128EFCBC-XLP Block Diagram**

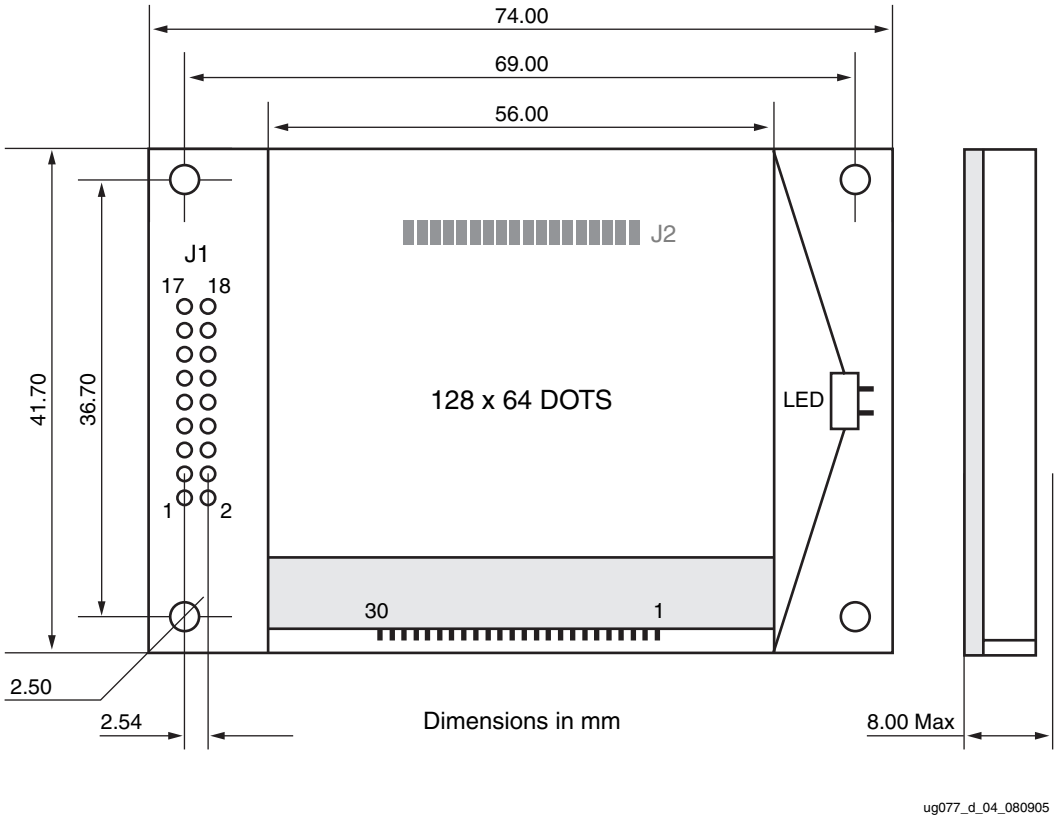


Figure D-4: **64128EFCBC-XLP Dimensions**

Controller – Operation

The pixels for the LCD panel are stored in the controller data RAM. This RAM is a 65-row by 132-column array. Each display pixel is represented by a single bit in the RAM array.

The interface to the RAM array goes through the 8-bit (DB0 – DB7) LCD interface. Therefore, the 65-bit rows are split into eight pages of eight lines. The ninth page is a single line page (DB0 only).

Interface designs can read from or write to the RAM array.

The display page is changed through the 4-bit page address register.

The column address (line address) is set with a two-byte register access. The line address corresponds to the first line that is going to be displayed on the LCD panel. This address is located in a 6-bit address register.

The RAM array is configured such that there are two characters per row (page), where each character pair uses eight rows of the display panel. Table D-2 shows the input data bytes, address lines, ADC control, and LCD outputs (segments).

Table D-2: **LCD Panel**

DB3	DB2	DB1	DB0	Data																			Line Address
0	0	0	0	DB0		■	■	■			■	■	■	■			Page 0							00H
				DB1	■				■		■				■									01H
				DB2	■				■		■				■									02H
				DB3	■				■		■	■	■	■										03H
				DB4	■	■	■	■	■		■				■									04H
				DB5	■				■		■				■									05H
				DB6	■				■		■	■	■	■										06H
				DB7																				07H
0	0	0	1	DB0		■	■	■			■	■	■				Page 1							08H
				DB1	■				■		■			■										09H
				DB2	■						■				■									0AH
				DB3	■						■				■									0BH
				DB4	■						■				■									0CH
				DB5	■				■		■			■										0DH
				DB6		■	■	■			■	■	■											0EH
				DB7																				0FH

Table D-2: **LCD Panel *(Continued)***

DB3	DB2	DB1	DB0	Data																			Line Address
0	0	1	0	DB0	■	■	■	■	■		■	■	■	■	■		Page 2							10H
				DB1	■						■													11H
				DB2	■						■													12H
				DB3	■	■	■	■			■	■	■	■										13H
				DB4	■						■													14H
				DB5	■						■													15H
				DB6	■	■	■	■	■		■													16H
				DB7																				17H
0	0	1	1	DB0		■	■	■			■				■		Page 3							18H
				DB1	■				■		■				■									19H
				DB2	■						■				■									1AH
				DB3	■		■	■	■		■	■	■	■	■									1BH
				DB4	■				■		■				■									1CH
				DB5	■				■		■				■									1DH
				DB6		■	■	■	■		■				■									1EH
				DB7																				1FH
0	1	0	0	DB0		■	■	■					■	■	■		Page 4							20H
				DB1			■							■										21H
				DB2			■							■										22H
				DB3			■							■										23H
				DB4			■							■										24H
				DB5			■				■			■										25H
				DB6		■	■	■				■	■											26H
				DB7																				27H
0	1	0	1	DB0	■				■		■						Page 5							28H
				DB1	■			■			■													29H
				DB2	■		■				■													2AH
				DB3	■	■					■													2BH
				DB4	■		■				■													2CH
				DB5	■			■			■													2DH
				DB6	■				■		■	■	■	■	■									2EH
				DB7																				2FH

Table D-2: **LCD Panel *(Continued)***

DB3	DB2	DB1	DB0	Data																			Line Address
0	1	1	0	DB0	■				■		■				■		Page 6							30H
				DB1	■	■		■	■		■				■									31H
				DB2	■		■		■		■	■			■									32H
				DB3	■		■		■		■		■		■									33H
				DB4	■				■		■			■	■									34H
				DB5	■				■		■				■									35H
				DB6	■				■		■				■									36H
				DB7																				37H
0	1	1	1	DB0		■	■	■			■	■	■	■			Page 7							38H
				DB1	■				■		■				■									39H
				DB2	■				■		■				■									3AH
				DB3	■				■		■	■	■	■										3BH
				DB4	■				■		■													3CH
				DB5	■				■		■													3DH
				DB6		■	■	■			■													3EH
				DB7																				3FH
1	0	0	0	DB0													Page 8							

Column Address																			
	ADC = 0	0	1	2	3	4	5	6	7	8	9	A	B		7E	7F	80	81	82	83
	ADC = 1	83	82	81	80	7F	7E	7D	7C	7B	7A	79	78		5	4	3	2	1	0
LCD Output		Seg 1	Seg 2	Seg 3	Seg 4	Seg 5	Seg 6	Seg 7	Seg 8	Seg 9	Seg 10	Seg 11	Seg 12		Seg 127	Seg 128	Seg 129	Seg 130	Seg 131	Seg 132

When a page is addressed, all the bits representing dots on the LCD panel can be accessed in that page. An array of 8x132 bits is available. The line address dictates what line of the RAM is going to be displayed on the first line of the glass panel.

Controller – LCD Panel Connections

The controller die, KS0713, connects to the LCD glass panel and user connection pins via a small PCB. Other necessary pins have default connections on the PCB. Table D-3 shows how all pins of the die are connected. The pins in blue connect to default values on the PCB, and the other pins connect to the user-accessible connectors.

Table D-3: **KS0713 Pin Connections**

Connector J1	Connector J2	PCB Connection	Connected to	Signal Name	Description
16	16	1		CS1B	Chip enable is active LOW.
15	15	2		RESETB	Initialize the LCD.
14	14	3		RS	Register select.
13	13	4		RW_WR	Read/Write.
12	12	5		E_RD	Enable/Read.
11	11	6		DB0	8-bit bidirectional data bus. In serial mode DB0-DB5 are high impedance, DB6 is the serial clock input, and DB7 is the serial data input.
10	10	7		DB1	
9	9	8		DB2	
8	8	9		DB3	
7	7	10		DB4	
6	6	11		DB5	
5	5	12		DB6	
4	4	13		DB7	
3	3	14		MI	Processor mode select.
		15		PS	Parallel or Serial.
1	1	16		VSS	Ground.
2	2	17		VDD	Power Supply.
LCD Control Pins					
			VDD	CS2	Active High chip enable.
			VDD	DUTY0	LCD driver duty ratio. Set to 1/65.
			VDD	DUTY1	
			VDD	MS	Master / Slave operation. Set to Master.
			VDD	CLS	Built-in oscillator enable.
			VSS	TEMPS	Set to -0.05%/°C
			VDD	INTRS	Internal resistors used.
			VSS	HPM	Normal mode set.
			VDD	BSTS	Voltage converter input is VDD (2.4<VDD<3.6).
			OPEN	DISP	Only used in Master/Slave.
			OPEN	CL	Display clock input.
			OPEN	M	Only used in Master/Slave.

Table D-3: **KS0713 Pin Connections *(Continued)***

Connector J1	Connector J2	PCB Connection	Connected to	Signal Name	Description
			OPEN	FRS	Only used in Master/Slave.
Voltage Converter and Control					
		18		VOUT	Voltage converter in or out.
		19		C3+	Voltage pump capacitors.
		20		C3-	
		21		C1+	
		22		C1-	
		23		C2+	
		24		C2-	
		25		V0	LCD driver supply. The relationship of the voltages is V0>V1>V2>V3>V4>VSS. When the internal power supply is active, these voltages are generated.
		26		V1	
		27		V2	
		28		V3	
		29		V4	
		30		VSS1	
			VSS	DCDC5B	Power Supply Control
			OPEN	VR	V0 Adjustment pin

Controller – Power Supply Circuits

Figure D-5 shows the power supply circuits. The power supply is used in the five times boost mode, where VDD is 3.3V and VOUT is 16.5V. VOUT is the operating voltage of the operational amplifier delivering the operating voltage, V0, for the LCD panel.

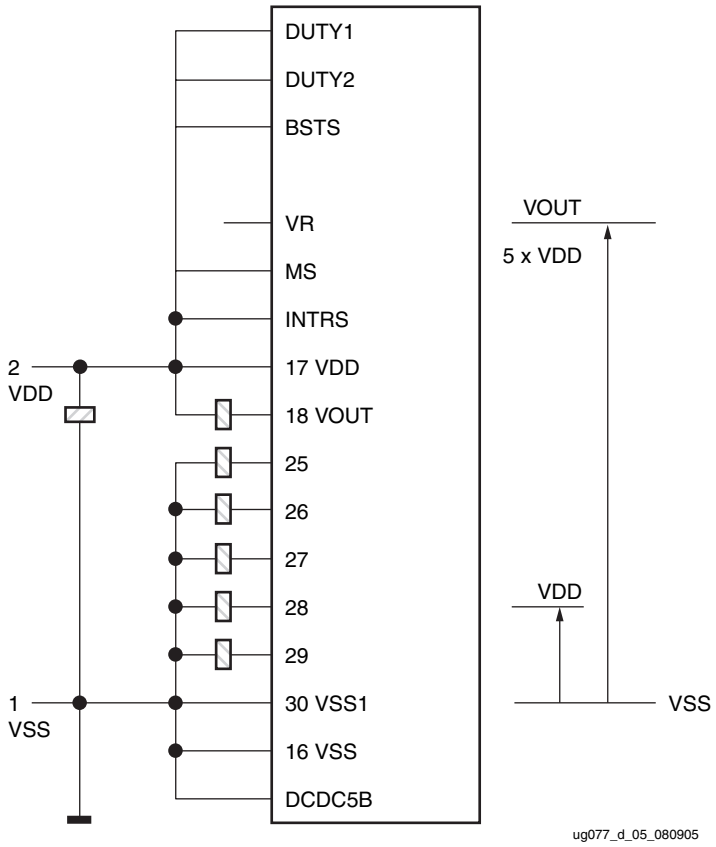


Figure D-5: **Power Supply Circuits**

The LCD operating voltage, V0, is set with two resistors, R_A and R_B. INTRS is driven Low when the resistors are external. INTRS is driven High when the resistors are internal. For the XlvdsPro_PwrIo board, internal resistors are selected.

The LCD operating voltage (V0) and the Electronic Volume Voltage (V_{EV}) can be calculated in units of V with these formulae:

Equation 1:

$$V0 = \left(1 + \frac{R_B}{R_A}\right) \times V_{EV}$$

Equation 2:

In Equation 2, V_{REF} is equal to 2.0V at 25 °C.

The values of the reference voltage parameter, α, and the ratio R_A/R_B are determined with bit settings in the LCD controller's instruction registers. Thus, it is possible to change physical operating parameters of the LCD through register bit settings, controlling the operating voltage, and the electronic volume level.

$$V_{EV} = \left(1 - \frac{63 - \alpha}{300}\right) \times V_{REF}$$

The voltage and contrast settings must be configured before the LCD panel is ready for operation. Figure D-6 shows the initialization procedure required to set up the LCD controller.

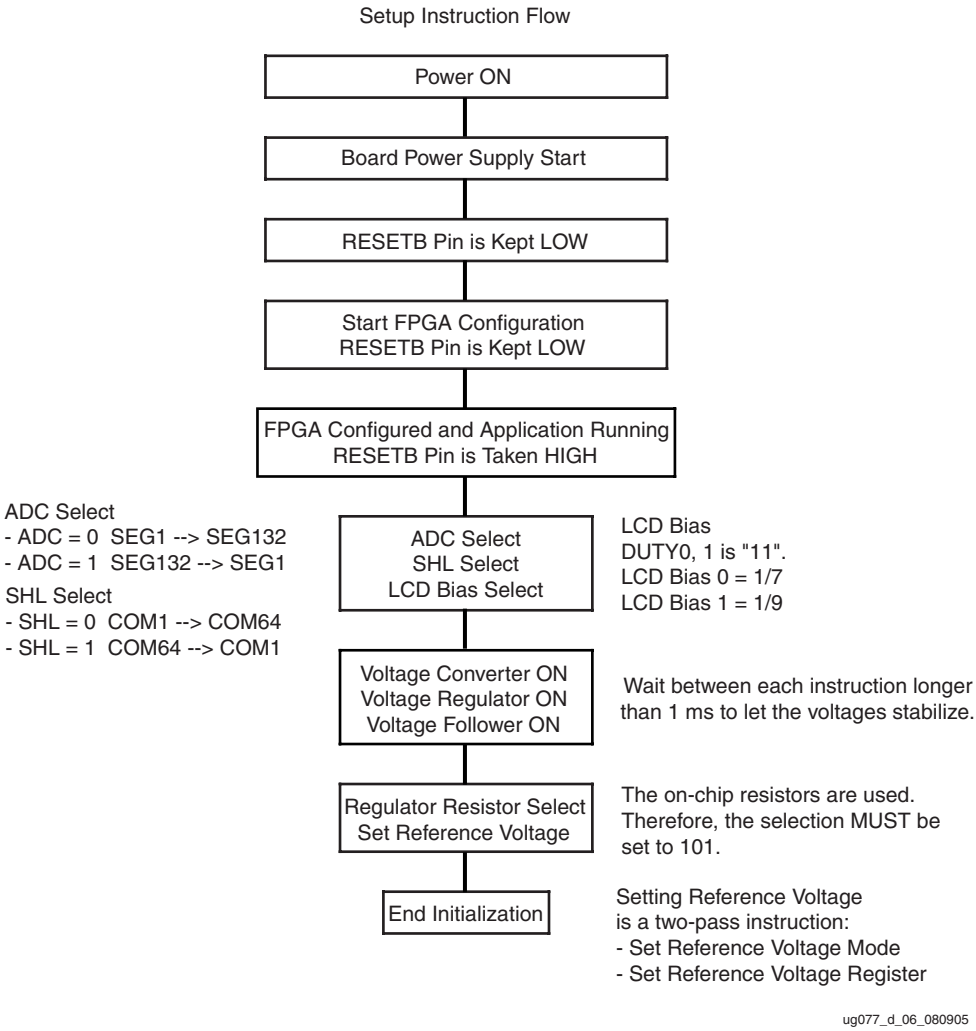


Figure D-6: **LCD Controller Initialization Flow**

Operation Example of the 64128EFCBC-3LP

The KS0713 LCD controller has several default settings of operation on the LCD panel display PCB. Some settings are forced through direct bonding on the chip. The default settings are:

- Master mode
- Parallel mode
- Internal oscillator
- Duty cycle ratio is set to 1/65
- Voltage converter input is between 2.4V ≤ VDD ≤ 3.6V, where VDD connects to 3.3V
- Internal voltage divider resistors
- Temperature coefficient is set to -0.05%/°C
- Normal power mode is set
- The voltage follower and voltage regulator are set to:
  - Five times boost mode
  - The V4, V3, V2, V1, and V0 outputs depend on the bias settings of 1/9 or 1/7.

Because of these default settings, the following display controller connections are not used:

- DISP: Turns into an output when Master mode is selected
- FRS: Static driver segment output
- M: Used in Master/Slave display configurations
- CL: Clock pin used in Master/Slave display configurations

When RESETB is Low, the display controller is initialized as indicated in Table D-4.

Table D-4: **Display Controller Initialization (RESETB is Low)**

Parameter	Initial Value
Display	OFF
Entire display	OFF
ADC select	OFF
Reverse display	OFF
Power control	0,0,0 (VC, VR, VF)
LCD bias	1/7
Read-modify-write	OFF
SHL select	OFF
Static indicator mode	OFF
Static indicator register	0,0 (S1, S0)
Display start	0 (First line)
Column address	0
Page address	0
Regulator select	0,0,0 (R2, R1, R0)
Reference voltage	OFF
Reference Voltage register	1,0,0,0,0,0 (SV5, SV4, SV3, SV2, SV1, SV0)

When RESETB is High, the display must be initialized. The first steps to be taken to guarantee correct operation of the display and the controller are:

- Configure the ADC bit. This bit determines the scanning direction of the segments.
  - When the RESETB signal is active, ADC is reset to *0*, meaning that the segments are scanned from SEG1 up to SEG132.
  - When ADC is set to *1*, the segments are scanned in opposite direction.
- Configure the SHL bit. This bit sets the scanning direction of the COM lines.
  - When the RESETB signal is active, SHL is reset to *0*, meaning that the segments are scanned from COM1 up to COM64.
  - When SHL is set to *1*, the common lines are scanned in opposite direction.

Once configured, these settings normally are not changed.

- Select the LCD bias settings.
  - The duty cycle is selected as 1/65 by hardwiring the controller IC pads on the display PCB.
  - The LCD bias is set to:
    - 1/7: when the BIAS bit is 0
    - 1/9: when the BIAS bit is 1

The following steps are performed next:

- Start the onboard converter, regulator, and follower
- Set the Regulator Resistor values (see Table D-5)
- Configure the reference voltage register parameters (see Table D-6)

Table D-5: **Resistor Value Settings**

	3-Bit Data Settings (R2 R1 R0)							
	000	001	010	011	100	**101**	110	111
1+(Rb/Ra)	1.90	2.19	2.55	3.02	3.61	**4.35**	5.29	6.48

Table D-6: **Reference Voltage Parameters**

SV5	SV4	SV3	SV2	SV1	SV0	Reference Voltage Parameter (α)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
..	..	…	..	..	..	..
..	..	..	..	..	..	..
1	1	1	1	1	0	62
1	1	1	1	1	1	63

At startup of the LCD controller (after RESETB operation), the resistor and reference voltage values are:

- Resistor selection is: 0,0,0
- Reference voltage is: 1,0,0,0,0,0

The Resistor selection value MUST be set to 101b when using this LCD panel.

After the display is brought to operational mode, it is best to wait at least 1 ms to ensure the stabilization of power supply levels. After this time, all other necessary display initializations can be performed.

Instruction Set

Table D-7 shows the instruction set for the LCD panel.

Table D-7: **Display Instructions**

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Read display data	1	1	Read Data							
8-bit data specified by the column and page address can be read from the Display Data RAM. The column address is increased automatically, thus data can be read continuously from the addressed page.										
Write display data	1	0	Write Data							
8-bit data can be written into a RAM location specified by the column and page address. The column address is increased automatically, thus data can be written continuously to the addressed page.										
Read status	0	1	BUSY	ADC	ONOFF	RESETB	0	0	0	0
BUSY: Device is BUSY when internal operation or reset. (0=active, 1 =busy). ADC: Indicates the relationship between RAM column address and segment driver. ONOFF: Indicates display ON or OFF status. RESETB: Indicates if initialization is in progress.										
Display ON/OFF	0	0	1	0	1	0	1	1	1	DON
Turn display ON or OFF. (1=ON, 0 = OFF)										
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

Sets the line address of the display RAM to determine the initial line of the LCD display.

ST5	ST4	ST3	ST2	ST1	ST0	
0	0	0	0	0	0	Line address 0
0	0	0	0	0	1	Line address 1
..	..	..	..	..	..	..
1	1	1	1	1	0	Line address 62
1	1	1	1	1	1	Line address 63

Table D-7: **Display Instructions *(Continued)***

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1
Set reference voltage register	0	0	x	x	SV5	SV4	SV3	SV2	SV1	SV0

This is a two-byte instruction. The first instruction sets the reference voltage mode. The second instruction sets the reference voltage parameter.

SV5	SV4	SV3	SV2	SV1	SV0	
0	0	0	0	0	0	0
0	0	0	0	0	1	1
..	..	..	..	..	..	..
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Set page address	0	0	1	0	1	1	P3	P2	P1	P0

This instruction sets the address of the display data page. Any RAM data bit can be accessed when its page address and column address are specified. Changing the Page Address does not affect the display status.

P3	P2	P1	P0	
0	0	0	0	page 0
0	0	0	1	page 1
..	..	..	..	...
0	1	1	1	page 7
1	0	0	0	page 8

Table D-7: **Display Instructions *(Continued)***

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Set column address MSB	0	0	0	0	0	1	Y7	Y6	Y5	Y4
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0

This instruction sets the address of the display data RAM. When a read or write to or from the display data RAM occurs, the addresses are automatically increased.

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	
0	0	0	0	0	0	0	0	Col Addr 0
0	0	0	0	0	0	0	1	Col Addr 1
..	..	..	..	..	..	..	..	...
1	1	1	1	1	1	1	0	Col Addr 130
1	1	1	1	1	1	1	1	Col Addr 131

ADC select	0	0	1	0	1	0	0	0	0	ADC

This instruction changes the relationship between RAM column address and segment driver.

ADC = 0, SEG1 --> SEG132 default mode
ADC = 1, SEG132 --> SEG1

Reverse display ON/OFF	0	0	1	0	1	0	0	1	1	REV

REV	RAM bit data = '1'	RAM bit data = '0'
0	Pixel ON	Pixel OFF
1	Pixel OFF	Pixel ON

Entire display ON/OFF	0	0	1	0	1	0	0	1	0	EON

This instruction forces the display to be turned on regardless of the contents of the display data RAM. The contents of the display data RAM are saved. This instruction has priority over reverse display.

LCD bias select	0	0	1	0	1	0	0	0	1	BIAS

This instruction selects the LCD bias.

Duty ratio	Bias = 0	Bias = 1
1/65	1/7	1/9

Table D-7: **Display Instructions *(Continued)***

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Set modify-read	0	0	1	1	1	0	0	0	0	0
This instruction stops the automatic incrementing of the column address by a read operation. The automatic increment is still done with a write operation.										
Reset modify-read	0	0	1	1	1	0	1	1	1	0
This instruction resets the changed modify-read to the normal.										
Reset	0	0	1	1	1	0	0	0	1	0
This instruction resets the LCD controller registers to the default values. The instruction CANNOT initialize the LCD power supply initialized with RESETB.										
SHL select	0	0	1	1	0	0	SHL	x	x	x
This instruction sets the COM output scanning direction. SHL = 0, COM1 ----> COM64 (default) SHL = 1, COM64 ----> COM1										
Power Control	0	0	0	0	1	0	1	VC	VR	VF
This instruction selects one of the eight power circuit functions. In the case of the DisplayTech 64128EFCBC display, these must be kept at "000."										
Regulator resistor select	0	0	0	0	1	0	0	R2	R1	R0
This instruction selects the resistor ratio Rb/Ra.										
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM
Set static indicator register	0	0	x	x	x	x	x	x	S1	S0
This is a two-byte instruction. The first instruction enables the second instruction. The second instruction update the contents of the static indicator register.										

Read/Write Characteristics (6800 Mode)

Table D-8: **Read/Write Characteristics in 6800 Mode**

Parameter	Signal	Symbol	Min	Typ	Max	Unit
Address setup time	RS	T_{AS}	13	-	-	ns
Address hold time		T_{AH}	17	-	-	ns
Data setup time	DB7 to DB0	T_{DS}	35	-	-	ns
Data hold time		T_{DH}	13	-	-	ns
Access time		T_{ACC}	-	-	125	ns
Output disable time		T_{OD}	10	-	90	ns
System cycle time	RS	T_{CYC}	400	-	-	ns
Enable pulse width	Read/write	E_RD	T_{PWR}	125	-	ns
			T_{PWW}	55	-	ns

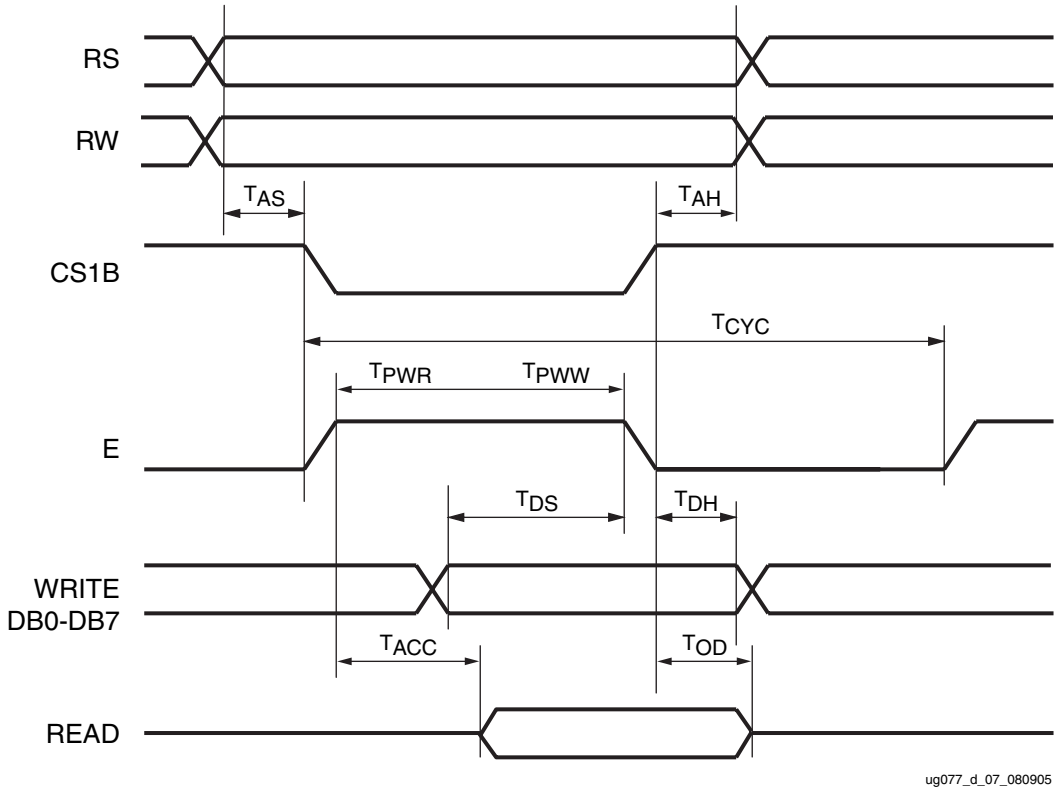


Figure D-7: **Read/Write Timing Waveforms (6800 Mode)**

Design Examples

LCD Panel Used in Full Graphics Mode

The LCD controller RAM has eight 132-byte pages (in fact, there are nine pages; page 9 is special). Each page is one-byte wide. If all the pages are put in one memory block, then the needed space is 8 pages x 8 bits x 132 pixels or 8448 bits (1056 bytes).

One Virtex-4 block RAM can be configured as 8+1 by 2048.

One block RAM can be used to store one complete pixel view of the LCD panel. There is enough space left for commands.

The ninth bit in the block RAM memory indicates whether the data in the block RAM is real data to be displayed or is a command for the controller.

The interface to the LCD panel is slow. The E signal can be used as the controller clock signal. This signal has a minimum cycle time of 400 ns for displaying 8 bits (equal to 8 dots) on the LCD. One full page of the display takes up to 132 x 400 ns = 52.8 µs. Updating the full display takes 52.8 µs x 8 = 423 µs.

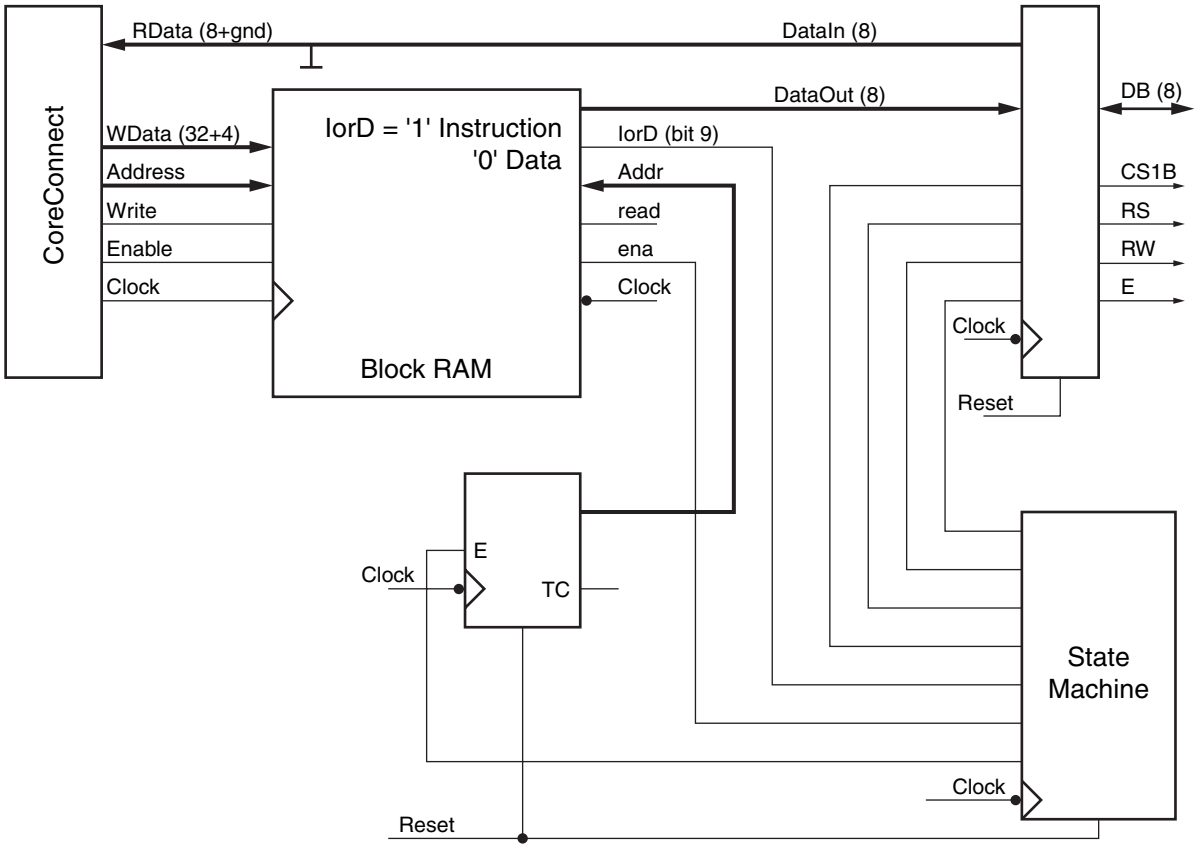
If using the dual port and data width capabilities of the block RAM, writes to the block RAM can be 32 bits (+4 control bits), and reads from the block RAM on the LCD side can be 8 bits (1 control bit). An entire LCD page is updated in 33 write operations.

The interface on the LCD panel side sequentially reads the block RAM and thus updates the screen contiguously (like a television screen). The controller (microcontroller or other) side of the block RAM can be written at any time.

The write operation happens on the rising edge of the clock, and the read (LCD update) happens on the falling edge of the clock. Normally, write and read operations at the same address give corrupt read data when the read and write clock edges do not respect the clock-to-clock setup timing. This problem is solved by using both edges of the clock.

A state machine is used to provide correct timing of the signals on the LCD panel side. The panel can be used in write-only mode or in read/write mode. Most of the time LCD panels operate in write-only mode.

At first the block RAM must be initialized with some data (instructions to the LCD) to make the LCD operate correctly.



Design for Full Graphics Interface, Attached to CoreConnect Bus

ug077_d_08_080905

Figure D-8: **General Block Diagram of Panel in Full Graphics Mode**

LCD Panel Used in Character Mode

This design example requires a byte representing a command or data to be displayed as input.

- When the Enable signal is Low, nothing happens. The display interface design is locked.

- When the Enable signal is High and the “data_or_command” control signal is Low, the byte written is a display command.
- When the Enable signal and the data_or_command control signal are High, the byte written is the ASCII character code of the character to be put on the display.

Display Command Byte

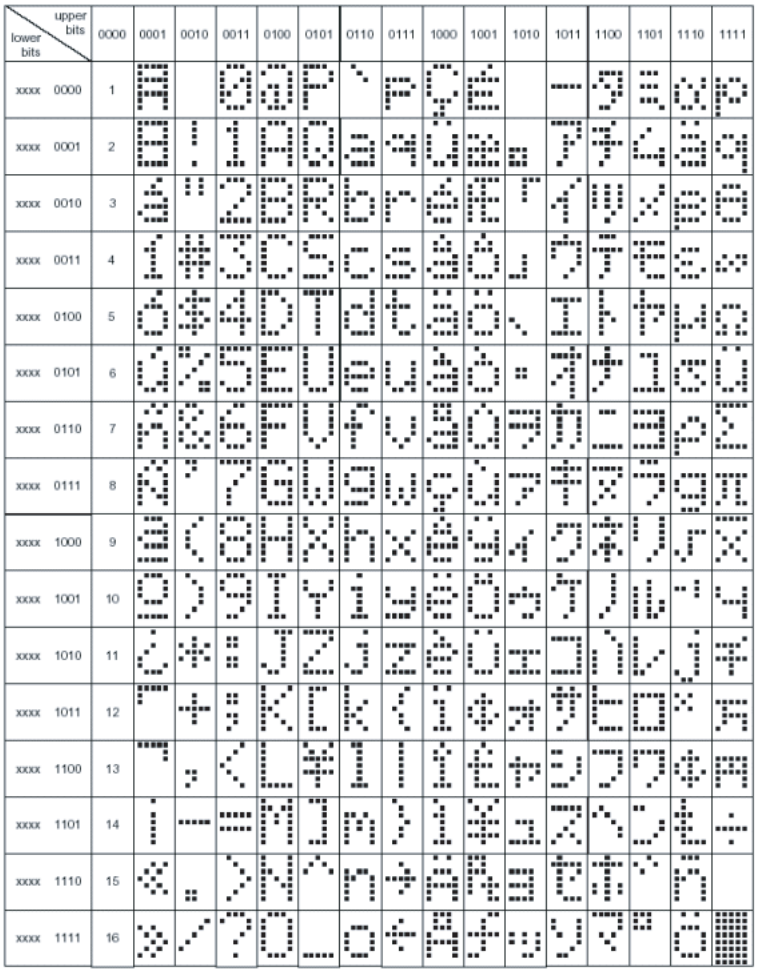
The command set of the display can be found in Table D-7.

When the LCD interface is enabled for the first time, a set of command bytes is sent to the LCD. This command set provides the basic initialization of the LCD display controller. When this initialization is done, the normal LCD display interface is freed for normal use. Command bytes from the valid command set can be sent to the display (controller).

A detailed description of the LCD controller interface can be found in the `Toplevel.vhd.txt` file.

Display Data Byte

The supplied byte must be a valid ASCII representation of a character as shown in Figure D-9.



ug077_d_09_080905

Figure D-9: **ASCII Character Representations**

The character set is stored in block RAM (used as ROM). For the layout of the block RAM character set, see the `CharacterSet.xls` file. The block RAM (see Figure D-10) is organized as small arrays of eight bytes, which is easy for address calculation.

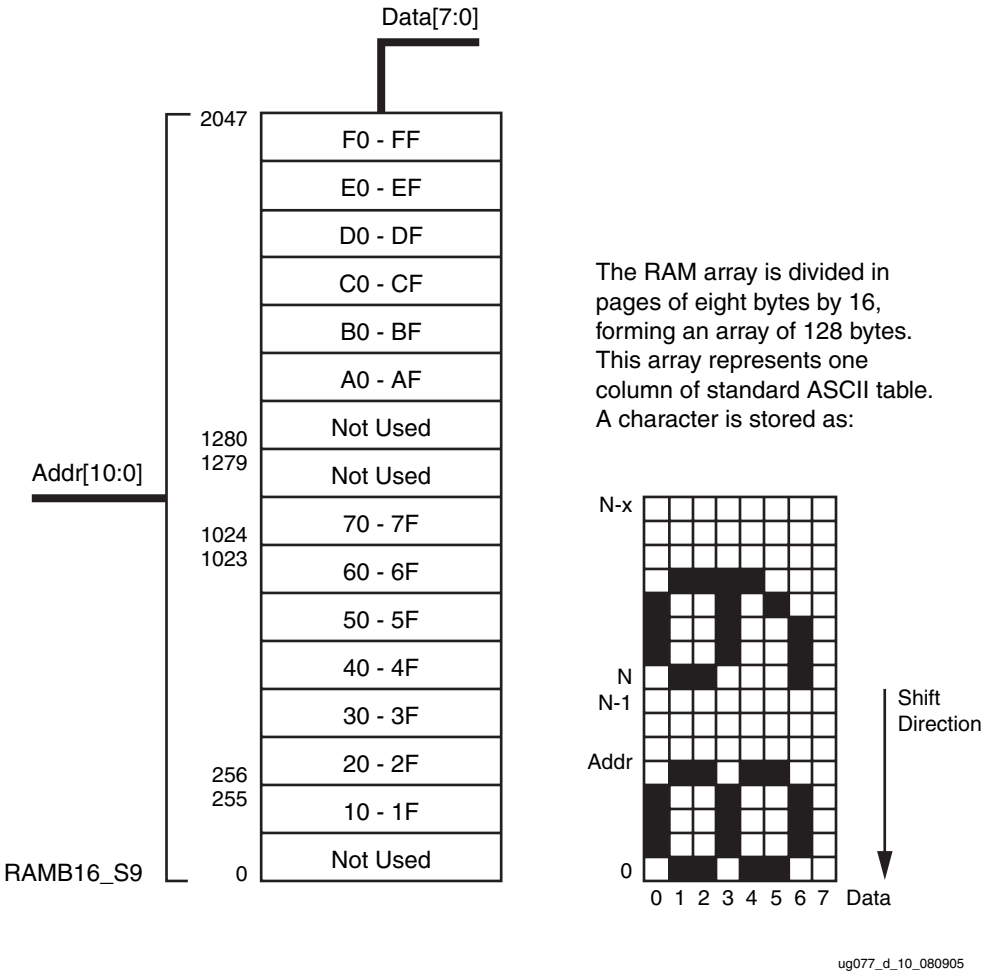


Figure D-10: **Block RAM Organization**

When presenting byte value 30 hex, character *0* must be displayed. Shifting the value 00110000b (30h) up three positions gives the value 180h or 348d.

Because each character uses eight byte locations, character *0* in the character set starts from memory location 348 decimal.

For example, character *X* has byte value 58h or 01011000b. Shifting this value three positions gives the value 2C0h or 704d.

Figure D-11 shows a block diagram of the LCD character generator controller. Character data is latched and then shifted left three positions. This shifted value is the start byte for a counter that outputs an address to the block RAM. The result is a stream of bytes representing a character for the display.

A small second counter determines when a new character is loaded into the block RAM address counter.

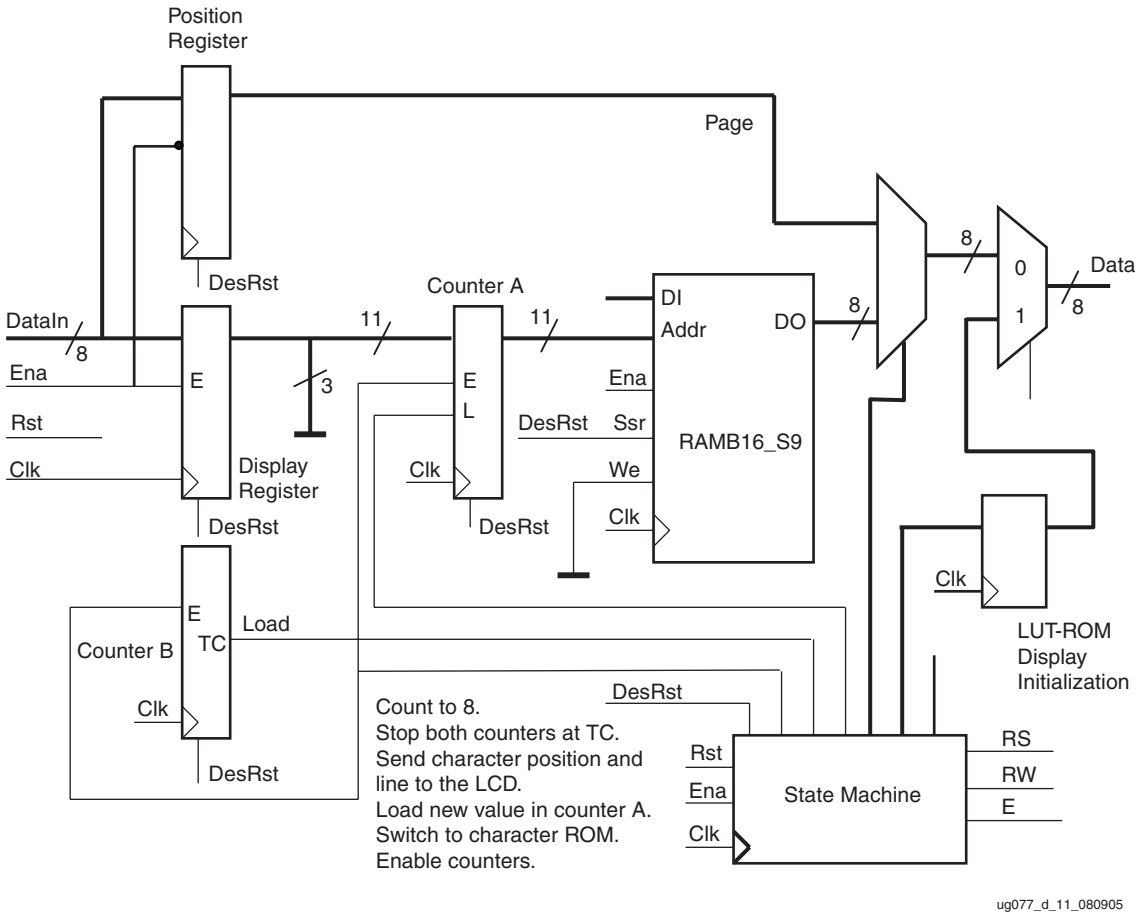


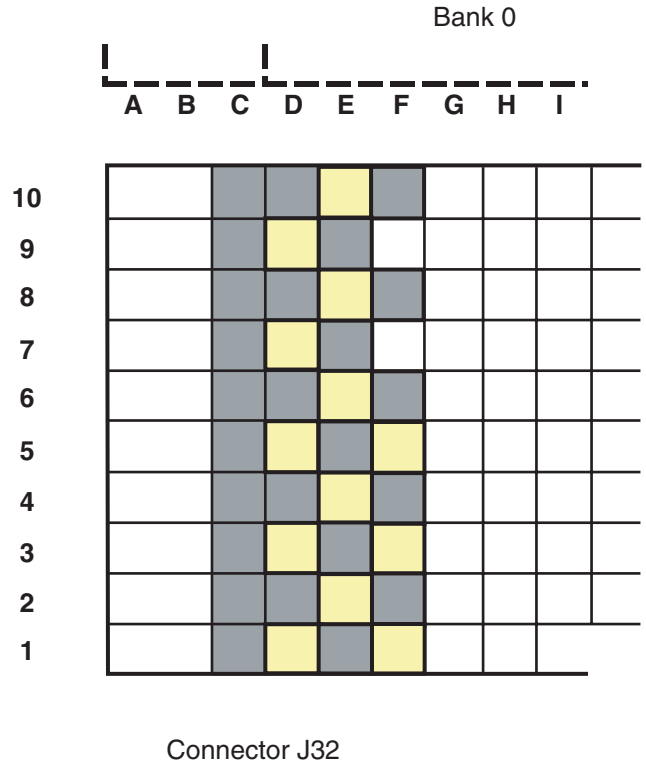
Figure D-11: **LCD Character Generator Controller**

A state machine takes care of the processing order.

A minimum cycle time of 400 ns on the E signal used as a reference. The 200 MHz system clock frequency is used as reference system clock. One E cycle uses at least 80 system clock cycles when the design is running at 200 MHz. The E pulse is part of the state machine, and the design only depends on the system clock. Timing is met as long as the system clock does not exceed 200 MHz.

This design can be adapted easily to fit the Microblaze or PPC405 core connect bus system.

Array Connector Numbering



Connector Pin		FPGA Pin
D9	LCD_D0	G23
D7	LCD_D4	E22
D5	LCD_D5	E23
D3	LCD_D6	F23
D1	LCD_D7	F24
E10	LCD_RST	D24
E8	LCD_D1	F21
E6	LCD_D2	F22
E4	LCD_D3	G22
E2	LCD_ENA	H22
F5	LCD_R/W	G21
F3	LCD_RSEL	H21
F1	LCD_CS1B	C24

ug077_d_12_080905

Figure D-12: **LCD Connections (Bank 0)**

UCF Information

```
#
# Bank 0 / LCD-BUS
#
# NET "     " LOC ="F24 ";    # LCD_D7                IO0L02N
# NET "     " LOC ="F23 ";    # LCD_D6                IO0L02P
# NET "     " LOC ="E23 ";    # LCD_D5                IO0L03N
# NET "     " LOC ="E22 ";    # LCD_D4                IO0L03P
# NET "     " LOC ="G22 ";    # LCD_D3                IO0L06P
# NET "     " LOC ="F22 ";    # LCD_D2                IO0L07N
# NET "     " LOC ="F21 ";    # LCD_D1                IO0L07P
# NET "     " LOC ="G23 ";    # LCD_D0                IO0L05
# NET "     " LOC ="D24 ";    # LCD_RST               IO0L08N
# NET "     " LOC ="C24 ";    # LCD_CS1B              IO0L08P
# NET "     " LOC ="H21 ";    # LCD_RSEL              IO0L09N
# NET "     " LOC ="G21 ";    # LCD_RW                IO0L09P
# NET "     " LOC ="H22 ";    # LCD_ENA               IO0L06N
#
```

UCF File

This appendix provides an example of a *starter* .UCF file that may be used with the ML450 Development Board. UCF File

```
#
# ************************************************************************
#
# ML450 constraints file
# XC4VLX25 FF668 FPGA pinout (U9) on ML450 board
# ************************************************************************#
#
# Power measurement "spy hole" pair #1,
# output pair within memory interface data
NET "B8_SPY1_SMA_N"      LOC = "W1";
NET "B8_SPY1_SMA_P"      LOC = "W2";
#
#
# Power measurement "spy hole" pair #2
NET "B9_SPY2_SMA_N"      LOC = "J25";
NET "B9_SPY2_SMA_P"      LOC = "J26";
#
#
# Clock Module, CM1
NET "CM1_CLK_N"          LOC = "AF10";
NET "CM1_CLK_P"          LOC = "AF11";
NET "CM1_CTRL1"          LOC = "AE14";
NET "CM1_CTRL2"          LOC = "AE13";
NET "CM1_CTRL3"          LOC = "AE10";
NET "CM1_CTRL4"          LOC = "AD10";
NET "CM1_EN"             LOC = "AC10";
#
#
# Clock Module, CM2
NET "CM2_CLK_N"          LOC = "N19";
NET "CM2_CLK_P"          LOC = "M19";
NET "CM2_CTRL1"          LOC = "A16";
NET "CM2_CTRL2"          LOC = "A15";
NET "CM2_CTRL3"          LOC = "A10";
NET "CM2_CTRL4"          LOC = "B10";
NET "CM2_EN"             LOC = "A12";
#
#
# Clock Module, CM3
NET "CM3_CLK_N"          LOC = "AC17";
NET "CM3_CLK_P"          LOC = "AB17";
NET "CM3_EN"             LOC = "AB10";
#
#
# Clock Module, CM4
```

```
NET "CM4_CLK_N"          LOC = "C14";
NET "CM4_CLK_P"          LOC = "C15";
NET "CM4_EN"             LOC = "A11";
#
#
# DDR 1 memory interface
NET "DDR1_A0"            LOC = "AD2";
NET "DDR1_A1"            LOC = "AD1";
NET "DDR1_A2"            LOC = "Y10";
NET "DDR1_A3"            LOC = "AA10";
NET "DDR1_A4"            LOC = "AC7";
NET "DDR1_A5"            LOC = "AC9";
NET "DDR1_A6"            LOC = "AB9";
NET "DDR1_A7"            LOC = "AE6";
NET "DDR1_A8"            LOC = "AD6";
NET "DDR1_A9"            LOC = "AF9";
NET "DDR1_A10"           LOC = "AE9";
NET "DDR1_A11"           LOC = "AD8";
NET "DDR1_A12"           LOC = "AC8";
NET "DDR1_BA0"           LOC = "AF8";
NET "DDR1_BA1"           LOC = "AF7";
NET "DDR1_CAS_N"         LOC = "Y8";
NET "DDR1_CK0_N"         LOC = "AC3";
NET "DDR1_CK0_P"         LOC = "AD3";
NET "DDR1_CKE"           LOC = "AA9";
NET "DDR1_CS0_N"         LOC = "AF4";
NET "DDR1_DM_BY0"        LOC = "AF3";
NET "DDR1_DM_BY1"        LOC = "W4";
NET "DDR1_DQ0"           LOC = "AB1";
NET "DDR1_DQ1"           LOC = "AA1";
NET "DDR1_DQ2"           LOC = "AC4";
NET "DDR1_DQ3"           LOC = "AB4";
NET "DDR1_DQ4"           LOC = "AC5";
NET "DDR1_DQ5"           LOC = "AB5";
NET "DDR1_DQ6"           LOC = "AC2";
NET "DDR1_DQ7"           LOC = "AC1";
NET "DDR1_DQ8"           LOC = "W7";
NET "DDR1_DQ9"           LOC = "V7";
NET "DDR1_DQ10"          LOC = "W6";
NET "DDR1_DQ11"          LOC = "W5";
NET "DDR1_DQ12"          LOC = "Y2";
NET "DDR1_DQ13"          LOC = "Y1";
NET "DDR1_DQ14"          LOC = "AA4";
NET "DDR1_DQ15"          LOC = "AA3";
NET "DDR1_DQS_BY0"       LOC = "Y6";
NET "DDR1_DQS_BY1"       LOC = "Y4";
NET "DDR1_RAS_N"         LOC = "AA8";
NET "DDR1_WE_N"          LOC = "Y9";
#
NET "READ_DATA_VALID_LOOPBACK" LOC = "AD4"; # one is ouput, the other is input
NET "READ_DATA_VALID_LOOPBACK"  LOC = "AD5"; # one is ouput, the other is input
#
#
# Serial EEPROM 24LC025, I2C interface
NET "EEPROM_SCL"         LOC = "AC6";
NET "EEPROM_SDA"         LOC = "AB6";
#
#
# Differential external source, input pair #1,
# within center column "GC" Global Clock inputs
NET "EXTCLK1_N"          LOC = "B14";
NET "EXTCLK1_P"          LOC = "B15";
#
#
# Differential external source, input pair #2,
```

```
# within center column "GC" Global Clock inputs
NET "EXTCLK2_N"          LOC = "AE12";
NET "EXTCLK2_P"          LOC = "AF12";
#
#
# Hyper Transport interface
NET "HT_REFCLK100"       LOC = "D12";
NET "HT_REFCLK100I"      LOC = "E26";
NET "HT_RX_CADN0"        LOC = "K25";
NET "HT_RX_CADN1"        LOC = "F23";
NET "HT_RX_CADN2"        LOC = "D19";
NET "HT_RX_CADN3"        LOC = "G9";
NET "HT_RX_CADN4"        LOC = "C25";
NET "HT_RX_CADN5"        LOC = "A23";
NET "HT_RX_CADN6"        LOC = "A21";
NET "HT_RX_CADN7"        LOC = "A19";
NET "HT_RX_CADN8"        LOC = "G17";
NET "HT_RX_CADN9"        LOC = "D21";
NET "HT_RX_CADN10"       LOC = "E18";
NET "HT_RX_CADN11"       LOC = "C24";
NET "HT_RX_CADN12"       LOC = "C22";
NET "HT_RX_CADN13"       LOC = "B21";
NET "HT_RX_CADN14"       LOC = "B20";
NET "HT_RX_CADN15"       LOC = "D18";
NET "HT_RX_CADP0"        LOC = "K26";
NET "HT_RX_CADP1"        LOC = "F24";
NET "HT_RX_CADP2"        LOC = "D20";
NET "HT_RX_CADP3"        LOC = "G10";
NET "HT_RX_CADP4"        LOC = "C26";
NET "HT_RX_CADP5"        LOC = "A24";
NET "HT_RX_CADP6"        LOC = "A22";
NET "HT_RX_CADP7"        LOC = "A20";
NET "HT_RX_CADP8"        LOC = "G18";
NET "HT_RX_CADP9"        LOC = "E21";
NET "HT_RX_CADP10"       LOC = "F18";
NET "HT_RX_CADP11"       LOC = "D24";
NET "HT_RX_CADP12"       LOC = "D22";
NET "HT_RX_CADP13"       LOC = "C21";
NET "HT_RX_CADP14"       LOC = "C20";
NET "HT_RX_CADP15"       LOC = "C19";
NET "HT_RX_CLK0N"        LOC = "D25";
NET "HT_RX_CLK0P"        LOC = "D26";
NET "HT_RX_CLK1N"        LOC = "C23";
NET "HT_RX_CLK1P"        LOC = "D23";
NET "HT_RX_CTL0N"        LOC = "A18";
NET "HT_RX_CTL0P"        LOC = "B18";
NET "HT_TX_CADN0"        LOC = "F3";
NET "HT_TX_CADN1"        LOC = "A5";
NET "HT_TX_CADN2"        LOC = "C1";
NET "HT_TX_CADN3"        LOC = "C10";
NET "HT_TX_CADN4"        LOC = "D17";
NET "HT_TX_CADN5"        LOC = "E10";
NET "HT_TX_CADN6"        LOC = "G8";
NET "HT_TX_CADN7"        LOC = "D7";
NET "HT_TX_CADN8"        LOC = "B4";
NET "HT_TX_CADN9"        LOC = "A7";
NET "HT_TX_CADN10"       LOC = "D4";
NET "HT_TX_CADN11"       LOC = "E4";
NET "HT_TX_CADN12"       LOC = "C8";
NET "HT_TX_CADN13"       LOC = "E5";
NET "HT_TX_CADN14"       LOC = "D6";
NET "HT_TX_CADN15"       LOC = "F9";
NET "HT_TX_CADP0"        LOC = "F4";
NET "HT_TX_CADP1"        LOC = "A6";
NET "HT_TX_CADP2"        LOC = "C2";
```

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NET "HT_TX_CADP3"         LOC = "D10";
NET "HT_TX_CADP4"         LOC = "C17";
NET "HT_TX_CADP5"         LOC = "F10";
NET "HT_TX_CADP6"         LOC = "F8";
NET "HT_TX_CADP7"         LOC = "D8";
NET "HT_TX_CADP8"         LOC = "A4";
NET "HT_TX_CADP9"         LOC = "A8";
NET "HT_TX_CADP10"        LOC = "C4";
NET "HT_TX_CADP11"        LOC = "D3";
NET "HT_TX_CADP12"        LOC = "D9";
NET "HT_TX_CADP13"        LOC = "E6";
NET "HT_TX_CADP14"        LOC = "E7";
NET "HT_TX_CADP15"        LOC = "E9";
NET "HT_TX_CLK0N"         LOC = "D5";
NET "HT_TX_CLK0P"         LOC = "C5";
NET "HT_TX_CLK1N"         LOC = "C7";
NET "HT_TX_CLK1P"         LOC = "B7";
NET "HT_TX_CTL0N"         LOC = "F17";
NET "HT_TX_CTL0P"         LOC = "E17";
#
NET "LDT_REQB"            LOC = "C16";
NET "LDT_STOPB"           LOC = "D16";
#
NET "SMBCLK"              LOC = "F1";
NET "SMBDAT"              LOC = "E2";
#
NET "TRST"                LOC = "D1";
NET "USERA0_A0P"          LOC = "D2";
NET "USERA1_A1P"          LOC = "B23";
NET "USERB1_B1P"          LOC = "B24";
NET "USERBO_BOP"          LOC = "E1";
NET "USERC1_C1P"          LOC = "E25";
NET "USERCO_COP"          LOC = "E3";
NET "USERD0_D0P"          LOC = "A9";
NET "USERD1_D1P"          LOC = "B9";
NET "USERE0_E0P"          LOC = "A3";
NET "USERE1_E1P"          LOC = "B3";
#
#
NET "USER_RCTL1N"         LOC = "E14"
NET "USER_RCTL1P"         LOC = "D15"
#
NET "USER_TCTL1N"         LOC = "G7";
NET "USER_TCTL1P"         LOC = "F7";
#
NET "PWROK"               LOC = "E13";
NET "SYSTEMRESETB"        LOC = "F26";
NET "RESETB"              LOC = "E24";
#
#
# LCD interface
NET "LCD_BL_ON"           LOC = "AE24";
NET "LCD_CSB"             LOC = "AE20";
NET "LCD_DB0"             LOC = "AF19";
NET "LCD_DB1"             LOC = "AF20";
NET "LCD_DB2"             LOC = "Y19";
NET "LCD_DB3"             LOC = "W19";
NET "LCD_DB4"             LOC = "AF23";
NET "LCD_DB5"             LOC = "AE23";
NET "LCD_DB6"             LOC = "Y20";
NET "LCD_DB7"             LOC = "Y21";
NET "LCD_E"               LOC = "AF24";
NET "LCD_RS"              LOC = "AA18";
NET "LCD_RSTB"            LOC = "AD20";
NET "LCD_R_WB"            LOC = "Y18";
```

```
#
#
# LVDS interface
NET "LVDS_CLKINA_N"      LOC = "C6";
NET "LVDS_CLKINA_P"      LOC = "B6";
NET "LVDS_CLKINB_N"      LOC = "D11";
NET "LVDS_CLKINB_P"      LOC = "C11";
NET "LVDS_CLKOUTA_N"     LOC = "F19";
NET "LVDS_CLKOUTA_P"     LOC = "G19";
NET "LVDS_CLKOUTB_N"     LOC = "H21";
NET "LVDS_CLKOUTB_P"     LOC = "H22";
NET "LVDS_DATAIN_N00"    LOC = "AC11";
NET "LVDS_DATAIN_N01"    LOC = "AA13";
NET "LVDS_DATAIN_N02"    LOC = "U5";
NET "LVDS_DATAIN_N03"    LOC = "U4";
NET "LVDS_DATAIN_N04"    LOC = "T6";
NET "LVDS_DATAIN_N05"    LOC = "U2";
NET "LVDS_DATAIN_N06"    LOC = "R1";
NET "LVDS_DATAIN_N07"    LOC = "T3";
NET "LVDS_DATAIN_N08"    LOC = "N2";
NET "LVDS_DATAIN_N09"    LOC = "R3";
NET "LVDS_DATAIN_N10"    LOC = "M1";
NET "LVDS_DATAIN_N11"    LOC = "P4";
NET "LVDS_DATAIN_N12"    LOC = "P6";
NET "LVDS_DATAIN_N13"    LOC = "N4";
NET "LVDS_DATAIN_N14"    LOC = "M7";
NET "LVDS_DATAIN_N15"    LOC = "M3";
NET "LVDS_DATAIN_N16"    LOC = "K6";
NET "LVDS_DATAIN_N17"    LOC = "M5";
NET "LVDS_DATAIN_N18"    LOC = "J6";
NET "LVDS_DATAIN_N19"    LOC = "K4";
NET "LVDS_DATAIN_N20"    LOC = "L3";
NET "LVDS_DATAIN_N21"    LOC = "J4";
NET "LVDS_DATAIN_N22"    LOC = "K2";
NET "LVDS_DATAIN_N23"    LOC = "H5";
NET "LVDS_DATAIN_N24"    LOC = "H3";
NET "LVDS_DATAIN_N25"    LOC = "G5";
NET "LVDS_DATAIN_N26"    LOC = "AB14";
NET "LVDS_DATAIN_N27"    LOC = "AA15";
NET "LVDS_DATAIN_N28"    LOC = "V1";
NET "LVDS_DATAIN_N29"    LOC = "U7";
NET "LVDS_DATAIN_N30"    LOC = "T1";
NET "LVDS_DATAIN_N31"    LOC = "R7";
NET "LVDS_DATAIN_N32"    LOC = "R5";
NET "LVDS_DATAIN_N33"    LOC = "N8";
NET "LVDS_DATAIN_N34"    LOC = "K1";
NET "LVDS_DATAIN_N35"    LOC = "L8";
NET "LVDS_DATAIN_N36"    LOC = "J1";
NET "LVDS_DATAIN_N37"    LOC = "L6";
NET "LVDS_DATAIN_N38"    LOC = "H1";
NET "LVDS_DATAIN_N39"    LOC = "G1";
NET "LVDS_DATAIN_P00"    LOC = "AC12";
NET "LVDS_DATAIN_P01"    LOC = "AB13";
NET "LVDS_DATAIN_P02"    LOC = "U6";
NET "LVDS_DATAIN_P03"    LOC = "V4";
NET "LVDS_DATAIN_P04"    LOC = "T7";
NET "LVDS_DATAIN_P05"    LOC = "U3";
NET "LVDS_DATAIN_P06"    LOC = "R2";
NET "LVDS_DATAIN_P07"    LOC = "T4";
NET "LVDS_DATAIN_P08"    LOC = "N3";
NET "LVDS_DATAIN_P09"    LOC = "R4";
NET "LVDS_DATAIN_P10"    LOC = "M2";
NET "LVDS_DATAIN_P11"    LOC = "P5";
NET "LVDS_DATAIN_P12"    LOC = "P7";
NET "LVDS_DATAIN_P13"    LOC = "N5";
```

```
NET "LVDS_DATAIN_P14"    LOC = "N7";
NET "LVDS_DATAIN_P15"    LOC = "M4";
NET "LVDS_DATAIN_P16"    LOC = "K7";
NET "LVDS_DATAIN_P17"    LOC = "M6";
NET "LVDS_DATAIN_P18"    LOC = "J7";
NET "LVDS_DATAIN_P19"    LOC = "K5";
NET "LVDS_DATAIN_P20"    LOC = "L4";
NET "LVDS_DATAIN_P21"    LOC = "J5";
NET "LVDS_DATAIN_P22"    LOC = "K3";
NET "LVDS_DATAIN_P23"    LOC = "H6";
NET "LVDS_DATAIN_P24"    LOC = "H4";
NET "LVDS_DATAIN_P25"    LOC = "G6";
NET "LVDS_DATAIN_P26"    LOC = "AA14";
NET "LVDS_DATAIN_P27"    LOC = "AA16";
NET "LVDS_DATAIN_P28"    LOC = "V2";
NET "LVDS_DATAIN_P29"    LOC = "T8";
NET "LVDS_DATAIN_P30"    LOC = "U1";
NET "LVDS_DATAIN_P31"    LOC = "R8";
NET "LVDS_DATAIN_P32"    LOC = "R6";
NET "LVDS_DATAIN_P33"    LOC = "P8";
NET "LVDS_DATAIN_P34"    LOC = "L1";
NET "LVDS_DATAIN_P35"    LOC = "M8";
NET "LVDS_DATAIN_P36"    LOC = "J2";
NET "LVDS_DATAIN_P37"    LOC = "L7";
NET "LVDS_DATAIN_P38"    LOC = "H2";
NET "LVDS_DATAIN_P39"    LOC = "G2";
NET "LVDS_DATAOUT_N00"   LOC = "Y26";
NET "LVDS_DATAOUT_N01"   LOC = "W26";
NET "LVDS_DATAOUT_N02"   LOC = "T19";
NET "LVDS_DATAOUT_N03"   LOC = "V23";
NET "LVDS_DATAOUT_N04"   LOC = "U21";
NET "LVDS_DATAOUT_N05"   LOC = "U24";
NET "LVDS_DATAOUT_N06"   LOC = "T20";
NET "LVDS_DATAOUT_N07"   LOC = "V20";
NET "LVDS_DATAOUT_N08"   LOC = "R21";
NET "LVDS_DATAOUT_N09"   LOC = "P24";
NET "LVDS_DATAOUT_N10"   LOC = "N22";
NET "LVDS_DATAOUT_N11"   LOC = "K20";
NET "LVDS_DATAOUT_N12"   LOC = "N24";
NET "LVDS_DATAOUT_N13"   LOC = "V25";
NET "LVDS_DATAOUT_N14"   LOC = "M22";
NET "LVDS_DATAOUT_N15"   LOC = "U26";
NET "LVDS_DATAOUT_N16"   LOC = "L23";
NET "LVDS_DATAOUT_N17"   LOC = "R25";
NET "LVDS_DATAOUT_N18"   LOC = "K23";
NET "LVDS_DATAOUT_N19"   LOC = "G20";
NET "LVDS_DATAOUT_N20"   LOC = "J22";
NET "LVDS_DATAOUT_N21"   LOC = "E22";
NET "LVDS_DATAOUT_N22"   LOC = "H23";
NET "LVDS_DATAOUT_N23"   LOC = "H25";
NET "LVDS_DATAOUT_N24"   LOC = "G23";
NET "LVDS_DATAOUT_N25"   LOC = "G25";
NET "LVDS_DATAOUT_N26"   LOC = "W24";
NET "LVDS_DATAOUT_N27"   LOC = "AA26";
NET "LVDS_DATAOUT_N28"   LOC = "W22";
NET "LVDS_DATAOUT_N29"   LOC = "P19";
NET "LVDS_DATAOUT_N30"   LOC = "N20";
NET "LVDS_DATAOUT_N31"   LOC = "V22";
NET "LVDS_DATAOUT_N32"   LOC = "R23";
NET "LVDS_DATAOUT_N33"   LOC = "M20";
NET "LVDS_DATAOUT_N34"   LOC = "P22";
NET "LVDS_DATAOUT_N35"   LOC = "L20";
NET "LVDS_DATAOUT_N36"   LOC = "M26";
NET "LVDS_DATAOUT_N37"   LOC = "K21";
NET "LVDS_DATAOUT_N38"   LOC = "M24";
```

```
NET "LVDS_DATAOUT_N39"   LOC = "J20";
NET "LVDS_DATAOUT_P00"   LOC = "Y25";
NET "LVDS_DATAOUT_P01"   LOC = "W25";
NET "LVDS_DATAOUT_P02"   LOC = "U20";
NET "LVDS_DATAOUT_P03"   LOC = "U23";
NET "LVDS_DATAOUT_P04"   LOC = "U22";
NET "LVDS_DATAOUT_P05"   LOC = "U25";
NET "LVDS_DATAOUT_P06"   LOC = "T21";
NET "LVDS_DATAOUT_P07"   LOC = "W20";
NET "LVDS_DATAOUT_P08"   LOC = "R22";
NET "LVDS_DATAOUT_P09"   LOC = "P25";
NET "LVDS_DATAOUT_P10"   LOC = "N23";
NET "LVDS_DATAOUT_P11"   LOC = "L19";
NET "LVDS_DATAOUT_P12"   LOC = "N25";
NET "LVDS_DATAOUT_P13"   LOC = "V26";
NET "LVDS_DATAOUT_P14"   LOC = "M23";
NET "LVDS_DATAOUT_P15"   LOC = "T26";
NET "LVDS_DATAOUT_P16"   LOC = "L24";
NET "LVDS_DATAOUT_P17"   LOC = "R26";
NET "LVDS_DATAOUT_P18"   LOC = "K24";
NET "LVDS_DATAOUT_P19"   LOC = "H20";
NET "LVDS_DATAOUT_P20"   LOC = "J23";
NET "LVDS_DATAOUT_P21"   LOC = "E23";
NET "LVDS_DATAOUT_P22"   LOC = "H24";
NET "LVDS_DATAOUT_P23"   LOC = "H26";
NET "LVDS_DATAOUT_P24"   LOC = "G24";
NET "LVDS_DATAOUT_P25"   LOC = "G26";
NET "LVDS_DATAOUT_P26"   LOC = "W23";
NET "LVDS_DATAOUT_P27"   LOC = "AB26";
NET "LVDS_DATAOUT_P28"   LOC = "W21";
NET "LVDS_DATAOUT_P29"   LOC = "P20";
NET "LVDS_DATAOUT_P30"   LOC = "N21";
NET "LVDS_DATAOUT_P31"   LOC = "V21";
NET "LVDS_DATAOUT_P32"   LOC = "R24";
NET "LVDS_DATAOUT_P33"   LOC = "M21";
NET "LVDS_DATAOUT_P34"   LOC = "P23";
NET "LVDS_DATAOUT_P35"   LOC = "L21";
NET "LVDS_DATAOUT_P36"   LOC = "L26";
NET "LVDS_DATAOUT_P37"   LOC = "K22";
NET "LVDS_DATAOUT_P38"   LOC = "M25";
NET "LVDS_DATAOUT_P39"   LOC = "J21";
NET "LVDS_FRAMEINA_N"    LOC = "H7";
NET "LVDS_FRAMEINA_P"    LOC = "H8";
NET "LVDS_FRAMEINB_N"    LOC = "G3";
NET "LVDS_FRAMEINB_P"    LOC = "G4";
NET "LVDS_FRAMEOUTA_N"   LOC = "E20";
NET "LVDS_FRAMEOUTA_P"   LOC = "F20";
NET "LVDS_FRAMEOUTB_N"   LOC = "G21";
NET "LVDS_FRAMEOUTB_P"   LOC = "G22";
#
#
# 200MHz Epson EG2121CA-200.0000M PHPAB,
# differential clock oscillator interface (LVDS 25)
NET "OSC1_200M_N"        LOC = "AD11";
NET "OSC1_200M_P"        LOC = "AD12";
#
#
# 250MHz Epson EG2121CA-250.0000M PHPAB,
# differential clock oscillator interface (LVDS 25)
NET "OSC1_250M_N"        LOC = "C12";
NET "OSC1_250M_P"        LOC = "C13";
#
#
# RS-232 interface, through Maxim MAX3316
NET "RS232_CTS"          LOC = "AD16";  # Clear to Send CTS,   input
```

```
NET "RS232_RTS"          LOC = "AD17";  # Request to Send RTS, output
NET "RS232_RX"           LOC = "AC20";  # Receive Data RD,     input
NET "RS232_TX"           LOC = "AB20";  # Transmit Data TD,    output
#
#
# System ACE interface
NET "SYSACE_CLK"         LOC = "Y24";
NET "SYSACE_CTRL0"       LOC = "B13";
NET "SYSACE_CTRL1"       LOC = "AC15";
NET "SYSACE_CTRL2"       LOC = "AC13";
NET "SYSACE_CTRL3"       LOC = "T23";
NET "SYSACE_CTRL4"       LOC = "R20";
NET "SYSACE_MPA0"        LOC = "AA11";
NET "SYSACE_MPA1"        LOC = "AC16";
NET "SYSACE_MPA2"        LOC = "B12";
NET "SYSACE_MPA3"        LOC = "R19";
NET "SYSACE_MPA4"        LOC = "AD26";
NET "SYSACE_MPA5"        LOC = "T24";
NET "SYSACE_MPA6"        LOC = "AD25";
NET "SYSACE_MPD0"        LOC = "AC14";
NET "SYSACE_MPD1"        LOC = "AD14";
NET "SYSACE_MPD2"        LOC = "AA12";
NET "SYSACE_MPD3"        LOC = "AA24";
NET "SYSACE_MPD4"        LOC = "AB21";
NET "SYSACE_MPD5"        LOC = "AC21";
NET "SYSACE_MPD6"        LOC = "AB25";
NET "SYSACE_MPD7"        LOC = "AB24";
# NET "SYSACE_TDO"         LOC = "Y12";
# dedicated config pin TDI_0; board net SYSACE_TDO
NET "TRSTB"              LOC = "V6";
NET "HALTB"              LOC = "V5";
#
#
# System Monitor (SysMon) interface
# Note: Designed onto ML450 Board but NOT supported in Virtex-4 devices
#
NET "SYSMON_ALARM1"      LOC = "Y3";    # controls blue LED D2, active LOW
NET "SYSMON_ALARM2"      LOC = "Y5";    # controls blue LED D3, active LOW
NET "SYSMON_ALARM3"      LOC = "AB3";   # controls blue LED D4, active LOW
NET "SYSMON_ALARM4"      LOC = "AE3";   # controls blue LED D5, active LOW
#
NET "TEMP_MON_VN7"       LOC = "AC19";
# [SM7] monitor Temp Measurement MAX6608 with Sysmon

# aka IO_L25N_CC_SM1_LC_7
NET "TEMP_MON_VP7"       LOC = "AD19";
# [SM7] monitor Temp Measurement MAX6608 with Sysmon

# aka IO_L25P_CC_SM1_LC_7
#
NET "VCC5_I_MEAS_VN6"    LOC = "AA20";
# [SM6] monitor "Current of 5V Vcc" with Sysmon

# aka IO_L26N_SM2_7
NET "VCC5_I_MEAS_VP6"    LOC = "AA19";
# [SM6] monitor "Current of 5V Vcc" with Sysmon

# aka IO_L26P_SM2_7
#
NET "VCC1V2_MON_VN5"     LOC = "AA17";
# [SM5] monitor voltage of "1.2V Vcc" with Sysmon

# aka IO_L27N_SM3_7
NET "VCC1V2_MON_VP5"     LOC = "Y17";
# [SM5] monitor voltage of "1.2V Vcc" with Sysmon
```

```
# aka IO_L27P_SM3_7
#
NET "VCC2V5_MON_VN4"     LOC = "AB18";
# [SM4] monitor voltage of "2.5V Vcc" with Sysmon

# aka IO_L29N_SM4_7
NET "VCC2V5_MON_VP4"     LOC = "AC18";
# [SM4] monitor voltage of "2.5V Vcc" with Sysmon

# aka IO_L29P_SM4_7
#
NET "VCCO2V5_MON_VN3"    LOC = "AF22";
# [SM3] monitor voltage of "2.5V Vcco" with Sysmon

# aka IO_L30N_SM5_7
NET "VCCO2V5_MON_VP3"    LOC = "AF21";
# [SM3] monitor voltage of "2.5V Vcco" with Sysmon

# aka IO_L30P_SM5_7
#
NET "VCCAUX2V5_MON_VN2"  LOC = "AE18";
# [SM2] monitor voltage of "2.5V Vccaux" with Sysmon

# aka IO_L31N_SM6_7
NET "VCCAUX2V5_MON_VP2"  LOC = "AF18";
# [SM2] monitor voltage of "2.5V Vccaux" with Sysmon

# aka IO_L31P_SM6_7
#
NET "VCC5V_MON_VN1"      LOC = "AD21";
# [SM1] monitor voltage of "5V Vcc" with Sysmon

# aka IO_L32N_SM7_7
NET "VCC5V_MON_VP1"      LOC = "AE21";
# [SM1] monitor voltage of "5V Vcc" with Sysmon

# aka IO_L32P_SM7_7
#
# Special System Monitor connector, access to dedicated analog input pair Vn/Vp
# only through external mezzanine board connector J7
# NET "SM_AVDD"            LOC = "AF17";  # dedicated pin AVDD_SM_0
# NET "GNDA"               LOC = "AE17";  # dedicated pin AVSS_SM_0
#
NET "SM_GPIO1"           LOC = "F11";
NET "SM_GPIO2"           LOC = "F16";
NET "SM_GPIO3"           LOC = "F15";
NET "SM_GPIO4"           LOC = "D14";
#
# NET "SM_VREF_P"          LOC = "AE16";  # dedicated pin VREFP_SM_0
# NET "GNDA"               LOC = "AE15";  # dedicated pin VREFN_SM_0
#
# NET "VN_SM"              LOC = "AF15";
# dedicated pin VN_SM_0, user defined with ext.

# Mezzanine Board connector (J7)
# NET "VP_SM"              LOC = "AF16";
# dedicated pin VP_SM_0, user defined with ext.

# Mezzanine Board connector (J7)
#
# Independent Power Supplies voltage control
#
# - controls an analog switch "Vishay DG2005"
#   >> CTL(x)   is pin 7 (IN1, normally open  NO1)
```

```
#   >> CTL(x+1) is pin 3 (IN2, normally close NC2)
#   ----------------------------
#    IN1 / IN2 ||  NO1  |  NC2
#   -----------||---------------
#        0     ||  off  |  on
#        1     ||  on   |  off
#   ----------------------------
#
# - select between -5%, nominal or +5%
#   ------------------------------------------
#    CTL(x+1) | CTL(x) || voltage control
#   ----------|--------||-----------------------
#       0     |   0    || nominal voltage
#       0     |   1    || +5% voltage
#       1     |   0    || -5% voltage
#       1     |   1    || (invalid) +1% or else
#   ------------------------------------------
#
NET "CTL1"               LOC = "F14";
# System 2.5V (analog switch  U8 pin 7, schem sht.21)
NET "CTL2"               LOC = "F13";
# System 2.5V (analog switch  U8 pin 3, schem sht.21)
#
NET "CTL3"               LOC = "F12";
# Vccaux 2.5V (analog switch U14 pin 7, schem sht.21)
NET "CTL4"               LOC = "B17";
# Vccaux 2.5V (analog switch U14 pin 3, schem sht.21)
#
NET "CTL5"               LOC = "A17";
# Vcco 2.5V   (analog switch U12 pin 7, schem sht.21)
NET "CTL6"               LOC = "AE4";
# Vcco 2.5V   (analog switch U12 pin 3, schem sht.21)
#
NET "CTL7"               LOC = "AF6";
# Vccint 1.2V (analog switch  U5 pin 7, schem sht.22)
NET "CTL8"               LOC = "AF5";
# Vccint 1.2V (analog switch  U5 pin 7, schem sht.22)
#
NET "CTL11"              LOC = "AA7";
# System 3.3V (analog switch  U1 pin 7, schem sht.22)
NET "CTL12"              LOC = "P3";
# System 3.3V (analog switch  U1 pin 7, schem sht.22)
#
#
# FPGA Configuration Interface
#
# NET "M0"                 LOC = "W15";
# dedicated configuration pin M_0_0
# NET "M1"                 LOC = "Y15";
# dedicated configuration pin M_1_0
# NET "M2"                 LOC = "W14";
# dedicated configuration pin M_2_0

NET "FPGA_DONE"          LOC = "AD13";
# NET "FPGA_DONE"          LOC = "H14";
# dedicated config. pin DONE_0; board net FPGA_DONE
# NET "FPGA_INIT"          LOC = "G15";
# dedicated config. pin INIT_0; board net FPGA_INIT
# NET "FPGA_PROGB"         LOC = "H15";
# dedicated config. pin PROGRAM_B_0; net FPGA_PROGB
NET "FPGA_RESETB"        LOC = "D13";  # active LOW reset
# NET "FPGA_TCK"           LOC = "W12";
# dedicated config. pin TCK_0; board net FPGA_TCK
# NET "FPGA_TDO"           LOC = "Y13";
# dedicated config. pin TDO_0; board net FPGA_TDO
```

```
# NET "FPGA_TMS"           LOC = "Y11";
# dedicated config. pin TMS_0; board net FPGA_TMS
#
# User LEDs interface: active LOW logic
NET "USER_LED0"          LOC = "AB23";  # controls blue LED D6,  active LOW
NET "USER_LED1"          LOC = "AA23";  # controls blue LED D8,  active LOW
NET "USER_LED2"          LOC = "AD22";  # controls blue LED D9,  active LOW
NET "USER_LED3"          LOC = "AD23";  # controls blue LED D11, active LOW
NET "USER_LED4"          LOC = "AC23";  # controls blue LED D13, active LOW
NET "USER_LED5"          LOC = "AC24";  # controls blue LED D14, active LOW
#
# User push button switch I/F: active LOW when switch closed,
# active HIGH when switch open
NET "USER_SW0"           LOC = "AC25";  # SW1 on schematic/PCB
NET "USER_SW1"           LOC = "AC26";  # SW2 on schematic/PCB
NET "USER_SW2"           LOC = "Y22";   # SW3 on schematic/PCB
NET "USER_SW3"           LOC = "Y23";   # SW4 on schematic/PCB
NET "USER_SW4"           LOC = "AC22";  # SW5 on schematic/PCB
NET "USER_SW5"           LOC = "AB22";  # SW6 on schematic/PCB
#
# FPGA Vref pins on Memory I/F Bank8
#
# NET "VREF_DDR_1V25"     LOC = "AB2";  # used as 1.25V DDR Vref; aka IO_L12N_VREF_8
# NET "VREF_DDR_1V25"     LOC = "AB7";  # used as 1.25V DDR Vref; aka IO_L28N_VREF_8
# NET "VREF_DDR_1V25"      LOC = "W3";   # used as 1.25V DDR Vref; aka IO_L4N_VREF_8
# NET "VREF_DDR_1V25"     LOC = "Y7";   # used as 1.25V DDR Vref; aka IO_L20N_VREF_8
#
# NET "GND"                LOC = "A2";   # dedicated pin GND1
# NET "GND"                LOC = "A13";  # dedicated pin GND2
# NET "GND"                LOC = "A14";  # dedicated pin GND3
# NET "GND"                LOC = "A25";  # dedicated pin GND4
#
# AA6  (GND5); AA21 (GND6); AB12 (GND7); AB15 (GND8); AD9 (GND9); AD18 (GND10);
# AD24 (GND11); AE1 (GND12); AE2 (GND13); AE25 GND14); AE26 (GND15); AF2 (GND16);
# AF13 (GND17); AF14 (GND18); AF25 (GND19); B1 (GND20); B2 (GND21); B25  (GND22);
# B26  (GND23);  C3   (GND24);  C9   (GND25);  C18  (GND26);  E12  (GND27);  E15
(GND28);
# F6 (GND29); F21 (GND30); J3 (GND31); J13 GND32); J14 (GND33); J24 (GND34);
# K11 (GND35); K12 (GND36); K13 (GND37); K14 (GND38); K15 (GND39); 16 (GND40);
# L12 (GND41); L13 GND42); L14 (GND43); L15 (GND44); M10 (GND45); M11 (GND46);
# M13 (GND47); M14 (GND48); M16 (GND49); M17 (GND50); N6 (GND51); N10 (GND52);
# N11 (GND53); N12 (GND54); N13 (GND55); N14 (GND56); N15 (GND57); N16 (GND58);
# N17 (GND59); N26 (GND60); P1 (GND61); P10 (GND62); P11 (GND63); P12 (GND64);
# P13 (GND65); P14 (GND66); P15 (GND67); P16 (GND68); P17 GND69); P21 (GND70);
# R10 (GND71); R11 (GND72); R13 (GND73); R14 (GND74); R16 (GND75); R17 (GND76);
# T12 (GND77); T13 (GND78); T14 (GND79); T15 (GND80); U11 (GND81); U12  (GND82);
# U13 (GND83); U14 (GND84); U15 (GND85); U16 (GND86); V3 (GND87); V13 (GND88);
#
# NET "GND"                LOC = "V14";  # dedicated pin GND89
# NET "GND"                LOC = "V24";  # dedicated pin GND90
#
# NET "GND"                LOC = "Y16";  # dedicated pin VBATT_0
#
# NET "VCC1V2"             LOC = "J10";
# ...J11   J16   J17   K9
# ...K10   K17   K18   L9    L10   L11
# ...L16   L17   L18   M12   M15   R12
# ...R15   T9    T10   T11   T16   T17
# ...T18   U9    U10   U17   U18   V10
# ...V11   V16
# NET "VCC1V2"             LOC = "V17";
#
# NET "VCC2V5_VAUX"        LOC = "H11";  # 2.5V Vccaux, LX60VCCAUX_1
# NET "VCC2V5_VAUX"        LOC = "H16";  # 2.5V Vccaux, LX60VCCAUX_2
# NET "VCC2V5_VAUX"        LOC = "H17";  # 2.5V Vccaux, LX60VCCAUX_3
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```
# NET "VCC2V5_VAUX"         LOC = "J12";  # 2.5V Vccaux, LX60VCCAUX_4
# NET "VCC2V5_VAUX"         LOC = "M9";   # 2.5V Vccaux, LX60VCCAUX_5
# NET "VCC2V5_VAUX"         LOC = "N9";   # 2.5V Vccaux, LX60VCCAUX_6
# NET "VCC2V5_VAUX"         LOC = "N18";  # 2.5V Vccaux, LX60VCCAUX_7
# NET "VCC2V5_VAUX"         LOC = "P9";   # 2.5V Vccaux, LX60VCCAUX_8
# NET "VCC2V5_VAUX"         LOC = "P18";  # 2.5V Vccaux, LX60VCCAUX_9
# NET "VCC2V5_VAUX"         LOC = "R18";  # 2.5V Vccaux, LX60VCCAUX_10
# NET "VCC2V5_VAUX"         LOC = "V15";  # 2.5V Vccaux, LX60VCCAUX_11
# NET "VCC2V5_VAUX"         LOC = "W10";  # 2.5V Vccaux, LX60VCCAUX_12
# NET "VCC2V5_VAUX"         LOC = "W11";  # 2.5V Vccaux, LX60VCCAUX_13
# NET "VCC2V5_VAUX"         LOC = "W16";  # 2.5V Vccaux, LX60VCCAUX_14
#
# NET "VCC2V5_VCCO"         LOC = "AA2";
# ...AA5    AA22   AA25   AB8    AB11   AB16    AB19
# ...AD15   AE5    AE8    AE11   AE19   AE22
# ...B5     B8     B11    B16    B19    B22
# ...E8     E11    E16    E19    F2     F5
# ...F22    F25    H9     H10    H18    H19
# ...J8     J15    J19    K8     K19    L2
# ...L5     L22    L25    M18    N1     P26
# ...R9     T2     T5     T22    T25    U8
# ...U19    V8     V12    V19    W8     W9      W17
# NET "VCC2V5_VCCO"         LOC = "W18";
#
#
```