

Thunder n3600M

///

**S2932** 

Version 1.1

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### Check the box contents!

Item	S2932WG2NR	S2932G2NR		
	1x Thunder n3600M S2932WG2NR motherboard	1x Thunder n3600M S2932G2NR motherboard		
	1x 34-Pin floppy drive cable	1x 34-Pin floppy drive cable		
3	6 x SATA cable	6 x SATA cable		
	3 x SATA Drive Power Adapter	3 x SATA Drive Power Adapter		
	2 x SAS Cable			
	1 x Ultra-DMA-100/66 IDE cable	1 x Ultra-DMA-100/66 IDE cable		
0	1 x USB2.0 cable	1 x USB2.0 cable		
	1 x Thunder n3600M user's manual	1 x Thunder n3600M user's manual		
	1 x Thunder n3600M Quick Reference guide	1 x Thunder n3600M Quick Reference guide		
•	1 x TYAN driver CD	1 x TYAN driver CD		
San	1 x I/O shield	1 x I/O shield		
TAIN FC	1 x SLI bridge	1 x SLI bridge		
J B	2 x CPU Retention Frame and Back Plate	2 x CPU Retention Frame and Back Plate		
	1 x COM Port cable	1 x COM Port cable		

# **NOTE**

# **Chapter 1: Introduction**

### 1.1 - Congratulations

You have purchased one of the most powerful server solutions. The Thunder n3600M (S2932) is a flexible AMD64 platform for multiple applications, based on NVIDIA nForce Pro3600 and SMSC DME5017 chipsets.

Designed to support AMD<sup>®</sup> uPGA 1207-pin ZIF L1 socket processors and 64GB DDRII-667 memory, the S2932 with integrated Dual Gigabit Ethernet LAN, built-in 32MB DDR video memory and six serial ATA ports, is ideal for CPU, memory, and video intensive applications such as CAD, Graphics Design, and High Bandwidth Video Editing, etc.

Remember to visit TYAN's Website at <a href="http://www.TYAN.com">http://www.TYAN.com</a>. There you can find information on all of TYAN's products with FAQs, online manuals and BIOS upgrades.

### 1.2 - Hardware Specifications

#### **Processor**

- •Two uPGA 1207-pin ZIF L1 sockets
- •Supports up to two AMD<sup>®</sup>
  Opteron<sup>™</sup> Rev. F 2000 Series
  Santa Rosa Dual core
  processors, and Barcelona Quad
  core processors
- Integrated 128-bit DDR memory controller

### **Expansion Slots**

- •Two (2) x16 PCI Express with x8 bandwidth
- •Three (3) PCI-X slots
- •One (1) 32-bit, 33MHz PCI v2.3 slots
- •Total six (6) usable expansion slots

#### Chipset

- •nVIDIA nForce Pro 3600
- ●NFC nPD720400
- •SMSC DME5017
- •LSI 1068E

### Integrated I/O Interfaces

- •One (1) floppy connector
- •One (1) IDE connector
- •Six (6) SATA ports
- •Eight (8) SAS ports
- •Four (4) USB2.0 ports (2 at rear, 2 via cable)
- •Two (2) COM port (1 at rear, 1 via cable)
- •Tyan 2x9 front-panel pin header
- •Tyan 2x7 pin header (2.0mm) for FAN tachometer and PWM
- •2x25 IPMI pin header

### Integrated 2D/3D PCI Graphics

- •ATI ES1000 PCI graphics controller
- •32MB DDR Frame Buffer of video memory

#### Integrated IDE

- One (1) ATA IDE slot for two IDE devices
- Support for ATA-133/100/66/33
   IDE drives and ATAPI compliant devices

### **System Management**

- SMSC DME5017 w/ hardware monitoring
- •Seven 4-pin fan header
- •Temperature and voltage monitoring
- Watchdog timer
- •Port 80 code display LED
- •TYAN IPMI support

#### Memory

- Dual memory channels
- •Supports up to 16 DDRII-667 DIMMs
- Up to 64GB of register ECC/non-ECC memory

### Integrated Serial ATA II

- •Serial ATA Host controllers embedded
- •Supports six serial ports running at 3.0Gb/s
- •NV RAID 0, 1, 0+1, 5 and JBOD support
- SATA activity LED connector

# Serial Attached SCSI(SAS)

- •LSI 1068E PCI-E SAS controller
- Supports 8 SAS ports running at 3.0Gb/s
- •RAID 0, 1 and JBOD support

#### **Back Panel I/O Ports**

- Stacked PS/2 mouse & keyboard ports
- •Two (2) USB 2.0 ports
- •One (1) COM1 connector
- •One (1) 15-pin VGA port
- Two RJ45 (Marvell 88E1121 PHy + nVIDIA MAC) 10/100/1000 Base-T port with link/activity LED

### **Integrated LAN Controllers**

- Two 10/100/1000 Base-T LAN (nForce Pro3600 integrated MAC with Marvell 88E1121Gigabit Ethernet PHY)
- •IEEE802.3 compliant, WOL/PXE support

#### **BIOS**

- •AMI BIOS 8Mbit Flash
- Supports ACPI 2.0
- PnP, DMI2.0, WfM2.0 power management

#### **Power**

- ATX12V support, on-board 4phase VRD
- Universal 24-pin + 8-pin power connectors
- •4-pin auxiliary power connector

#### Form Factor

- •Extended ATX (13" x 12")
- •8 layers PCB

### Regulatory

- •FCC Class B (Declaration of Conformity)
- •CE (Declaration of Conformity)

### **PCI-E Assignment**

- •X16 PCI Express with x8 bandwidth
- •X16 PCI Express with x8 bandwidth
- •NEC nPD720400 with x4 bandwidth
- •LSI 1068E with x8 bandwidth

# **Chapter 2: Board Installation**

You are now ready to install your motherboard. The mounting hole pattern of the Thunder n3600M S2932 matches the EATX specification. Before continuing with installation, confirm that your chassis supports an ATX motherboard.

### How to install our products right... the first time

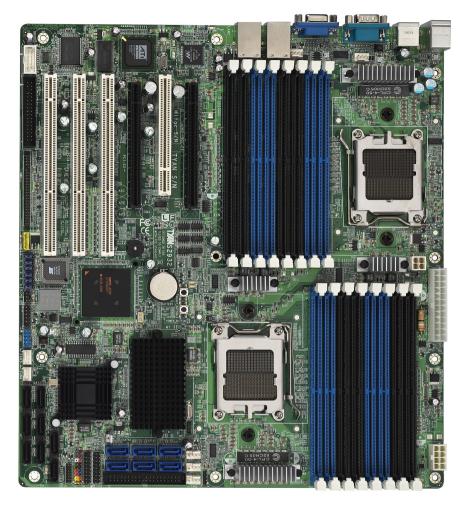
The first thing you should do is reading this user's manual. It contains important information that will make configuration and setup much easier. Here are some precautions you should take when installing your motherboard:

- (1) Ground yourself properly before removing your motherboard from the antistatic bag. Unplug the power from your computer power supply and then touch a safely grounded object to release static charge (i.e. power supply case). For the safest conditions, TYAN recommends wearing a static safety wrist strap.
- (2) Hold the motherboard by its edges and do not touch the bottom of the board, or flex the board in any way.
- (3) Avoid touching the motherboard components, IC chips, connectors, memory modules, and leads.
- (4) Place the motherboard on a grounded antistatic surface or on the antistatic bag that the board was shipped in.
- (5) Inspect the board for damage.

The following pages include details on how to install your motherboard into your chassis, as well as installing the processor, memory, disk drives and cables.

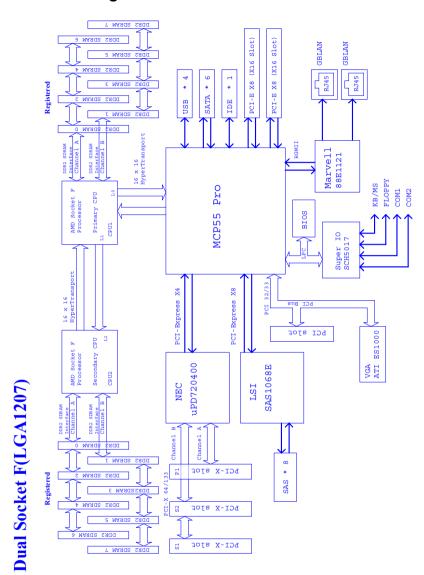
NOTE DO NOT APPLY POWER TO THE BOARD IF IT HAS BEEN DAMAGED.

# 2.1- Board Image



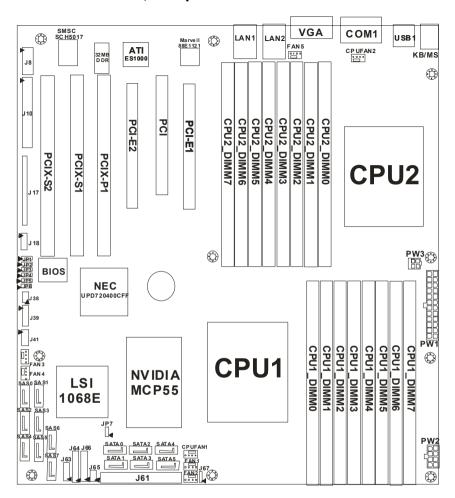
This picture is representative of the latest board revision available at the time of publishing. The board you receive may or may not look exactly like the above picture.

## 2.2 - Block Diagram



Thunder n3600M S2932 Block Diagram

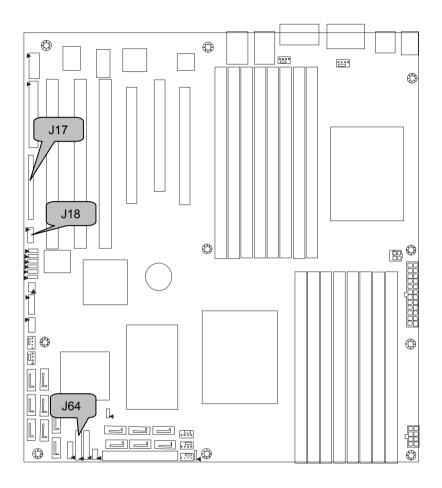
### 2.3 - Board Parts, Jumpers and Connectors



### **Jumper Legend**

OPEN - Jumper OFF, without jumper cover
CLOSED – Jumper ON, with jumper cover

Jumper/Connector	Function		
JP1/JP2	PCI-S1/ PCI-S2 Speed Setting Jumper		
JP3/JP4	SMDC Select Jumper		
JP5	VGA Enable/Disable Jumper		
JP6	SAS Enable/Disable Jumper		
JP7	Clear CMOS Jumper		
J1	Keyboard/Mouse Connectors		
J2	VGA Connector		
J3	COM Port Connector		
J4/J5	Gigabit LAN Port		
J7/J42/J43/J59/J62	Chassis Fan Connectors J59: FAN1, J62: FAN2, J42: FAN3, J43: FAN4 J7: FAN5		
J8	COM Port Pin Header		
J9/J55	J55: CPUFAN1; J9: CPUFAN2 connectors		
J10	Floppy Connector		
J17	SMDC Connector		
J18	IPMB Pin Header		
PW1/PW2/PW3	Power Connectors (see p.34 for details)		
J38	LCM Pin Header (for Barebone use only)		
J39/J63	TYAN Front Panel 2 Connector (for Barebone use only)		
J41	Front Panel USB2.0 Connectors		
J61	Primary IDE Connector		
J64	Front Panel Header		
J65	SGPIO Header (for Barebone use only)		
J66	SAS Fault LED Pin Header (for Barebone use only)		



#### J64: Front Panel Header

The Front Panel Header is used to connect some control or signal wires from motherboard to chassis, such as HDD LED, power LED, power button, and reset button.

HDD LED+	1 🔳	<b>2</b>	PWR LED+
HDD LED-	3■	<b>■</b> 4	PWR LED-
Reset Switch	5■	<b>6</b>	PWR Switch
Reset Switch	7 ■	■8	Power Switch
NMI	9■	<b>■</b> 10	Warning LED+
NMI	11 🔳	<b>■</b> 12	Warning LED-
5VsB	13 🔳	<b>■</b> 14	key
SMBus Data	15 ■	<b>■</b> 16	GND
SMBus Clock	17 ■	<b>■</b> 18	Chassis Intrusion

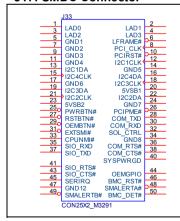
#### J18: IPMB Pin Header



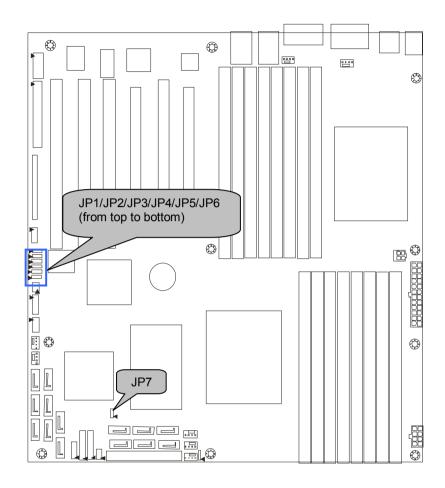
Use this header to connect to the IPMB device.

Pin 1	Pin 2	Pin 3	Pin 4
IPMB	GND	IPMB	NC
DATA		CLK	

#### J17: SMDC Connector



The SMDC connector allows you to connect with Tyan Server Management Daughter Card (SMDC). The S2932 supports Tyan SMDC M3291. See Appendix for more information on SMDC.



JP1/JP2: PCI-S1/PCI-S2 Speed Setting Jumper

of 1/of 2. I Of-01/1 Of-02 Opeed Cetting Sumper					
1 3	Max frequency is 133MHz				
1 3	Max frequency is 100MHz				

### JP3/JP4: SMDC Select Jumper

Support SMDC.  Please note that both JP3 and JP4 must closed to support SMDC.	: be Pin #2-3
---	---------------

JP5: VGA Enable/Disable Jumper

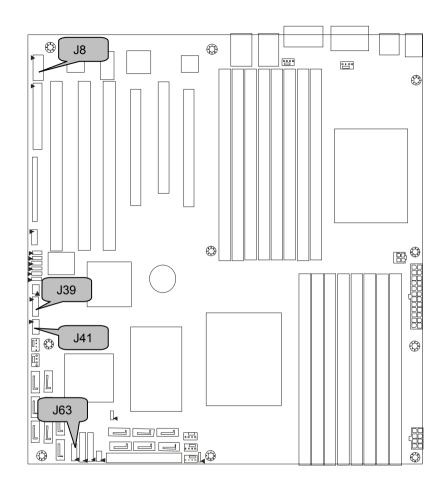
0. 0. 10.1 =				
1 3	Enable the onboard VGA function. (Default)			
1 3	Disable the onboard VGA function.			

JP6: SAS Enable/Disable Jumper

1 3	Enable the onboard SAS function. (Default)
1 3	Disable the onboard SAS function.

JP7: Clear CMOS Jumper

3	Use this jumper when you forgot your system/setup password or need to clear system BIOS setting.			
Normal (Default)	How to clear the CMOS data - Power off system and disconnect power supply from AC source			
a 3 a 1 Clear	Use jumper cap to close Pin_2 and 3 for several seconds to Clear CMOS     Replace jumper cap to close Pin_1 and 2 Reconnect power supply to AC source     Power on system			

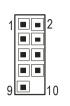


J41: Front Panel USB2.0 Connector

		Signal	Pin	Pin	Signal
1 2		USB PWR	1	2	USB PWR
		USB1-	3	4	USB2-
		USB1+	5	6	USB2+
		GND	7	8	GND
		Key	9	10	GND
9	U	se these heade	ers to	con	nect to the USE

Use these headers to connect to the USB devices via the enclosed USB cable.

### J8: COM Port Pin Header



Use these pin definitions to connect a port to COM2. \*TYAN does not provide cable for this header. It is designed for OEM use only.

Signal	Pin	Pin	Signal
DCD	1	2	DSR
RXD	3	4	RTS
TXD	5	6	CTS
DTR	7	8	RI
GND	9	10	Key

J39: TYAN Front Panel 2 Connector (for Barebone use only)

1	<b>9 9</b> 2	
1	<ul><li>12</li></ul>	

Signal	Signal Pin		Signal
LAN1 LED+	1	2	LAN1 LED-
LAN2 LED+	3	4	LAN2 LED-
NC	5	6	NC
ID LED+	7	8	ID LED-
ID S/W+	9	10	ID S/W-
Key	11	12	NC

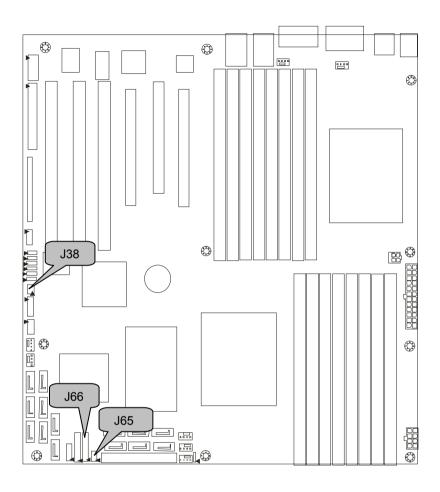
Use this header to connect to the front panel of barebone.

J63: TYAN Fron Panel 2 Connector (for Barebone use only)

14	13
2	1

z z z miester (i si z miesterie des z m.),			
Signal	Pin	Pin	Signal
TACH1	1	2	TACH6
TACH2	3	4	TACH7
TACH3	5	6	TACH8
TACH4	7	8	TACH9
TACH5	9	10	TACH10
GND	11	12	Key
GND	13	14	PWM

Use this header to connect to the front panel of barebone.



J38: LCM Pin Header (for Barebone use only)

6	<b>■</b> 5	)
2	╗╽╻	

Signal	Pin	Pin	Signal
VCC5V	1	2	RXD2
Key	3	4	GND
5VSB	5	6	TXD2

Use this header to connect the LCM module with system monitoring function. This header is reserved for barebone use.

J65: SGPIO Header (for Barebone use only)

8	7
2	1

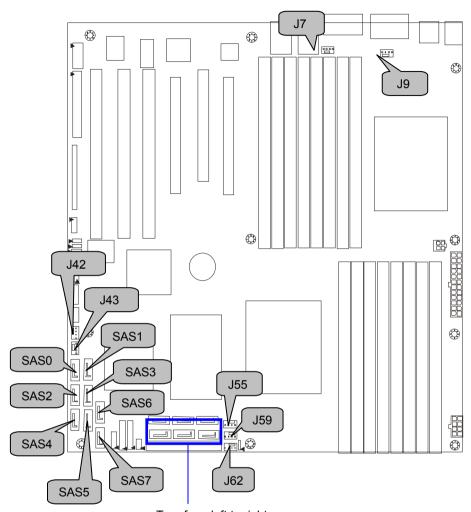
	Signal	Pin	Pin	Signal
SD	ATA_OUT0	1	2	SDATA_IN0
	SCLOCK	3	4	SLOAD
SD	ATA_OUT1	5	6	SDATA_IN1
	GND	7	8	Key

J66: SAS Fault LED Pin Header (for Barebone use only)

18	<b>■</b> ■1:	/
	■■	
2	<b>■ ■</b> 1	

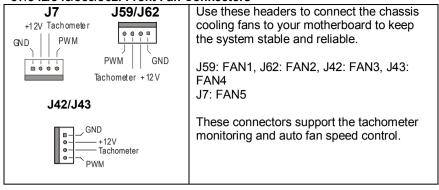
i neader (for Barebone use offiy)				
Signal	Pin	Pin	Signal	
SAS0+	1	2	SAS0-	
SAS1+	3	4	SAS1-	
SAS2+	5	6	SAS2-	
SAS3+	7	8	SAS3-	
Key	9	10	NC	
SAS4+	11	12	SAS4-	
SAS5+	13	14	SAS5-	
SAS6+	15	16	SAS6-	
SAS7+	17	18	SAS7-	

Use this header to connect to the SAS Fault LED on Barebone.

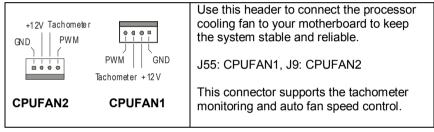


Top: from left to right SATA0, SATA2, SATA4 Bottom: from left to right SATA1, SATA3, SATA5

### J7/J42/J43/J59/J62: Front Fan Connectors



### J9/J55: CPU FAN Connector



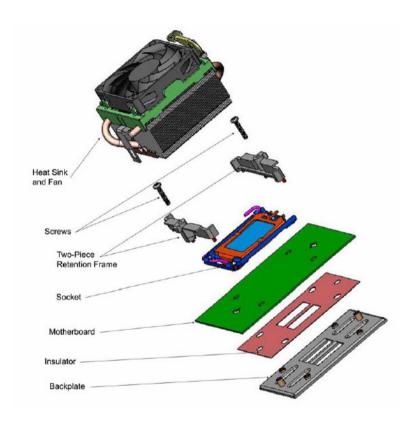
# SATA 0/1/2/3/4/5: Serial ATA RAID Connectors SAS 0/1/2/3/4/5/6/7 SAS Connectors

OAO OI IIZI	JI TI OI 1	on one	201111001013			
	7	GND	SATA 0/1/2/3/4/5 Connectors - Connects to the Serial ATA drives via the Serial			
	6	RXP	ATA cable - You may have the support of RAID 0, 1, 0+1,			
7	5	RXN	and 5 through the onboard MCP55 Pro chip.			
	4	GND	SAS 0/1/2/3/4/5/6/7 SAS Connectors - Connects to the Serial ATA or SAS HDD via t			
1 -	3	TXN	Serial ATA cable - You may have the support of NV RAID 0, 1 and			
	2	TXP	JBOD through the onboard LSI SAS1068E chip.			
	1	GND				

# 2.4 - Installing the Processor

Your Thunder n3600M S2932 supports the latest processor technologies from AMD. Check the TYAN website for latest processor support:

### http://www.tyan.com



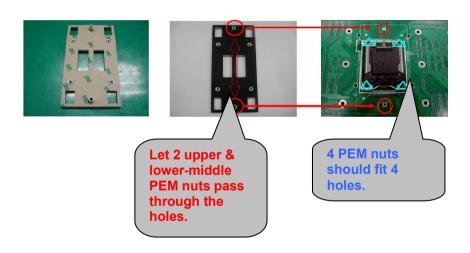
Exploded View of AMD PIB Platforms Thermal Solution based on AMD Socket F Processor

### **Back plate Assembly**

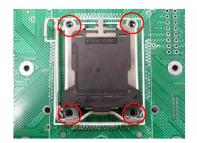
The back plate is mounted on the backside of the motherboard and enhances local stiffness to support shock and vibration loads acting on the heat sink. The back plate assembly prevents excessive motherboard warpage in the area near the processor. Without a back plate, excessive warpage could cause serious damage to electrical connections of the processor socket and integrated circuit packages surrounding the processor. The back plate also serves as a stiffener plate for the LGA socket.

While doing the installation, be careful in holding the components. Follow these instructions to install your back plate:

- 1. Remove the release liner from the back plate.
- Align the PEM nuts on the back plate to the holes on the reverse side of the PCB.
- First, insert the taller upper & lower middle PEM nuts through the holes of the PCB. The remaining four shorter PEM nuts should automatically fit the 4 holes on the PCB as shown in the following pictures.



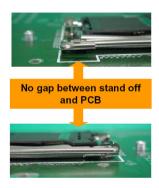
 Locate four screw holes on socket and screw the socket to the PCB board.





NOTE: Do not assemble CPU before securing socket with screws.

 Inspect Socket F assembly to PCB. The Socket F must be tightly attached onto the PCB. There must NOT be any gap between stand off the PCB.



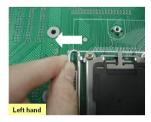


### **Processor Installation**

The processor should be installed carefully. Make sure you are wearing an antistatic strap and handle the processor as little as possible. Follow these instructions to install your processor:

- 1. Place the PCB such that the socket cam side faces you. Make sure the lever hook is on your top-left side.
- 2. Use your left thumb and forefinger to hold the lever hook, then pull it to the left side to clear the retention tab.
- 3. Rotate the lever to a fully open position.







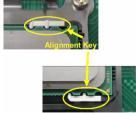
4. Lift the load plate to a fully open position.





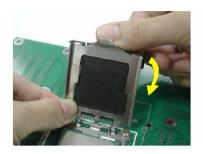
 Locate the Pin 1 indicator of the package. Align the package with the socket and carefully insert the package into the socket with vertical motion only. Vertically check if the CPU is seated well in the socket housing. If not, take out the CPU, with vertical motion only, and repeat the above steps.

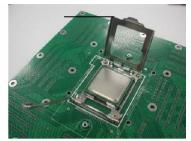




NOTE: The alignment keys must be located in the notches of the package.

Remove the PnP cap. Use your left hand to hold the load plate.
 Then use your right thumb to remove the PnP cap from the load plate.
 With the package in the socket, the PnP cap removal process will not damage the contacts.





7. Close the socket. Rotate the load plate onto the package lid.
Engage the load lever while pressing down lightly onto the load plate.
Secure the lever near the hook end under the retention tab.





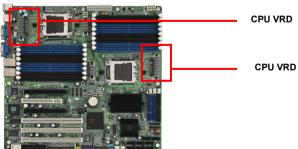


8. Repeat this procedure for the second processor if necessary.

### **CPU VRD Heat Dispersion Notice**

#### **INSTALL FAN INTO CHASSIS TO LET AIR FLOW IN!!!**

-To ensure that the board runs efficiently and does not overheat, make sure there is air flow around the CPU VRD (as shown) to help disperse the heat generated around the CPU.



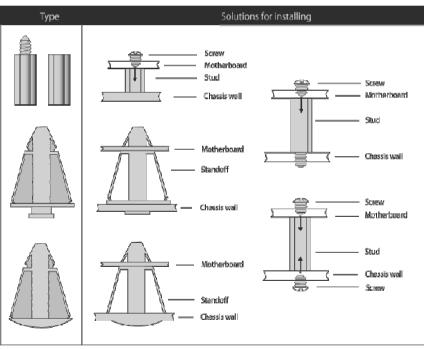
### 2.5 - Tips on Installing Motherboard in Chassis

Before installing your motherboard, make sure your chassis has the necessary motherboard support studs installed. These studs are usually metal and are gold in color. Usually, the chassis manufacturer will pre-install the support studs. If you are unsure of stud placement, simply lay the motherboard inside the chassis and align the screw holes of the motherboard to the studs inside the case. If there are any studs missing, you will know right away since the motherboard will not be able to be securely installed.

Some chassis' include plastic studs instead of metal. Although the plastic studs are usable, TYAN recommends using metal studs with screws that will fasten the motherboard more securely in place.

Below is a chart detailing what the most common motherboard studs look like and how they should be installed.

Mounting the Motherboard



### 2.6 - Installing the Memory

Before installing memory, ensure that the memory you have is compatible with the motherboard and processor. Only DDR2 register ECC/non-ECC memory modules are required. Check the TYAN Web site at <a href="https://www.tyan.com">www.tyan.com</a> for details of the type of memory recommended for your motherboard.

The following diagram shows common types of DDR2 memory modules.



- All installed memory will automatically be detected and no jumpers or settings need changing.
- The Thunder n3600M S2932 supports up to 64GB of memory.

# Memory Population Rule (Note: X indicates a populated DIMM Slot)

Single CPU Installed   Dual CPU installed								
		le CP			Dua	II CPL	J insta	alled
		(CPU1 only)			(CPU1 and CPU2)			
Population Option	1	2	3	4	5	6	7	8
CPU1_DIMM0				Х				Х
CPU1_DIMM1				Х				Х
CPU1_DIMM2			Х	Х			Х	Х
CPU1_DIMM3			Χ	Х			Х	Х
CPU1_DIMM4		Х	Χ	Х		Х	Х	Х
CPU1_DIMM5		Х	Χ	Х		Х	Х	Х
CPU1_DIMM6	Х	Х	Χ	Х	Х	Х	Х	Х
CPU1_DIMM7	Х	Х	Χ	Х	Х	Х	Х	Х
CPU2_DIMM0								Х
CPU2_DIMM1								Х
CPU2_DIMM2							Х	Х
CPU2_DIMM3							Х	Х
CPU2_DIMM4						Х	Х	Х
CPU2_DIMM5						Х	Х	Х
CPU2_DIMM6					Х	Х	Х	Х
CPU2_DIMM7					Х	Х	Х	Х

#### NOTE:

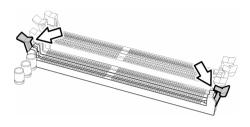
Symmetrical DIMMS must be identical

- Same DRAM technology, eg 128-bit, 256-bit, etc
- Same DRAM bus width, eg x8 or x16
- Matched Sided DIMMs (single-sided or double-sided)

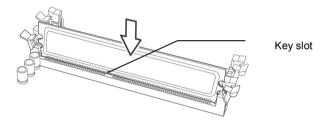
### **Memory Installation Procedure**

Follow these instructions to install memory modules into the Thunder n3600M.

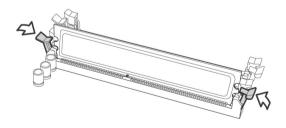
1. Press the locking levers in the direction shown in the following illustration.



2. Align the memory module with the socket. The memory module is keyed to fit only one way in the socket.



3. Seat the module firmly into the socket by gently pressing down until it sits flush with the socket. The locking levers pop up into place.

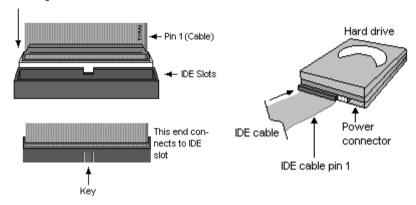


### 2.7 - Attaching Drive Cables

### **Attaching IDE Drive Cable**

Attaching the IDE drive cable is simple. These cables are "keyed" to only allow them to be connected in the correct manner. TYAN motherboards have two on-board IDE channels, each supporting two drives. The black connector designates the Primary channel, while the white connector designates the Secondary channel.

Attaching IDE cables to the IDE connectors is illustrated below:



Simply plug in the BLUE END of the IDE cable into the motherboard IDE connector, and the other end(s) into the drive(s). Each standard IDE cable has three connectors, two of which are closer together. The BLUE connector that is furthest away from the other two is the end that connects to the motherboard. The other two connectors are used to connect to drives.

**NOTE**: Always remember to properly set the drive jumpers. If only using one device on a channel, it must be set as Master for the BIOS to detect it.

TIP: Pin 1 on the IDE cable (usually designated by a colored wire) faces the drive's power connector.

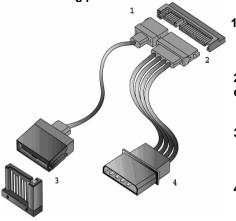
### **Attaching Serial ATA Cables**

The Thunder n3600M S2932 is equipped with **6** Serial ATA (SATA) channels. Connections for these drives are very simple.

There is no need to set Master/Slave jumpers on SATA drives.

Tyan has supplied two SATA cables and one SATA power adapter. If you are in need of other cables or power adapters please contact your place of purchase.

### The following pictures illustrate how to connect an SATA drive

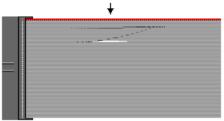


- 1.SATA drive cable connection
- 2. SATA drive power connection
- 3. SATA cable motherboard connector
- 4. SATA drive power adapter

### **Attaching Floppy Drive Cables**

Attaching floppy diskette drives are done in a similar manner to hard drives. See the picture below for an example of a floppy cable. Most of the current floppy drives on the market require that the cable be installed with the colored stripe positioned next to the power connector. In most cases, there will be a key pin on the cable which will force a proper connection of the cable.

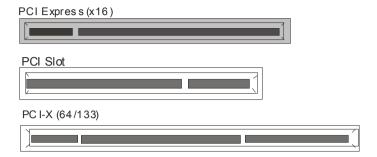
Twist at the end of the ribbon cable



Attach first floppy drive (drive **A:**) to the end of the cable with the twist in it. Drive **B:** is usually connected to the next possible connector on the cable (the second or third connector after you install Drive **A:**).

### 2.8 - Installing Add-in Cards

Before installing add-in cards, it's helpful to know if they are fully compatible with your motherboard. For this reason, we've provided the diagrams below, showing the most common slots that may appear on your motherboard. Not all of the slots shown will necessarily appear on your motherboard.



Simply find the appropriate slot for your add-in card and insert the card firmly. Do not force any add-in cards into any slots if they do not seat in place. It is better to try another slot or return the faulty card rather than damaging both the motherboard and the add-in card.

### PCI IDESELs and IRQ Assignments

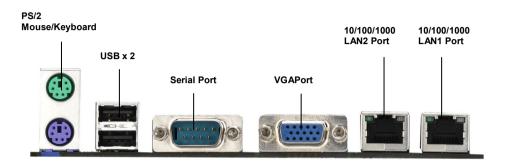
Slot or Device	IDSEL#	Bus#	PIRQ	PIRQ	PIRQ	PIRQ
PCI Slot	AD22	PCI	INT_W	INT_X	INT_Y	INT_Z
Onboard VGA	AD23	PCI	INT_Y			
PCI-X1 Slot #1 (32bit)	AD16	PCI- X1	INT_A	INT_B	INT_C	INT_D
PCI-X2 Slot #1 (32bit)	AD16	PCI- X2	INT_A	INT_B	INT_C	INT_D
PCI-X2 Slot #2 (32bit)	AD18	PCI- X2	INT_C	INT_D	INT_A	INT_B

NOTE

**YOU MUST ALWAYS** unplug the power connector from the motherboard before performing system hardware changes. Otherwise you may damage the board and/or expansion device.

### 2.9 - Connecting External Devices

Your motherboard supports a number of different interfaces through connecting peripherals. See the following diagrams for the details.



**NOTE**: Peripheral devices can be plugged straight into any of these ports but software may be required to complete the installation.

### Onboard LAN LED Color Definition

The three onboard Ethernet ports have green and yellow LEDs to indicate LAN status. The chart below illustrates the different LED states.

10/100/1000 Mbps LAN Link/Activity LED Scheme				
LEFT RIGHT		Left LED	Right LED	
10 Mbps	Link	Green	1 Blinking Yellow	
	Active	Blinking Green	1 Blinking Yellow	
100 Mbps	Link	Green	2 Blinking Yellow	
	Active	Blinking Green	2 Blinking Yellow	
1000 Mbps	Link	Green	3 Blinking Yellow	
	Active	Blinking Green	3 Blinking Yellow	
No Link		Off	Off	

**NOTE:** In 10 Mbps, the Right LED blinks yellow once in repeat and continuous action. In 100 Mbps, the Right LED blinks yellow twice in repeat and continuous action. So does the condition in 1000 Mbps.

## 2.10 - Installing the Power Supply

There are three power connectors on your Thunder n3600M S2932. The Thunder n3600M S2932 requires that you have an EPS12V power supply that has a 24-pin, an 8-pin and a 4-pin power connectors.

**NOTE**: Please be aware that ATX 2.x, ATX12V and ATXGES power supplies may <u>not</u> be compatible with the board and can damage the motherboard and/or CPU(s).

#### 24-Pin EPS/12V Power Connector

8-Pin 12V Power Connector



4-Pin 12V Power Connector



J28: PW1

12	+3.3V	24	GND
11	+12V2	23	+5V
10	+12V2	22	+5V
9	+5VSB	21	+5V
8	PWR OK	20	RESVD
7	GND	19	GND
6	+5V	18	GND
5	GND	17	GND
4	+5V	16	PSON#
3	GND	15	GND
2	+3.3V	14	-12V
1	+3.3V	13	+3.3V

.J49: PW2

0-10			
4	GND	8	+12V3
3	GND	7	+12V3
2	GND	6	+12V3
1	GND	5	+12V3

J27: PW3

<u></u>	
4	+12V
3	+12V
2	GND
1	GND

### Applying power to the board

- 1. Connect the 12V 8-pin power connector.
- 2. Connect the EPS/12V 24-pin power connector.
- 3. Connect the 4-pin power connector.
- 4. Connect power cable to power supply and power outlet



**YOU MUST** unplug the power supply before plugging the power cables to motherboard connectors.

### 2.11 - Finishing up

Congratulations on making it this far! You're finished setting up the hardware aspect of your computer. Before closing up your chassis, make sure that all cables and wires are connected properly, especially IDE cables and most importantly, jumpers. You may have difficulty powering on your system if the motherboard jumpers are not set correctly. In the rare circumstance that you have experienced difficulty, you can find help by asking your vendor for assistance. If they are not available for assistance, please find setup information and documentation online at our website or by calling your vendor's support line.

# **NOTE**

# **Chapter 3: BIOS Setup**

#### 3.1 About the BIOS

The BIOS is the basic input/output system, the firmware on the motherboard that enables your hardware to interface with your software. The BIOS determines what a computer can do without accessing programs from a disk. The BIOS contains all the code required to control the keyboard, display screen, disk drives, serial communications, and a number of miscellaneous functions. This chapter describes the various BIOS settings that can be used to configure your system.

The BIOS section of this manual is subject to change without notice and is provided for reference purposes only. The settings and configurations of the BIOS are current at the time of print and are subject to change, and therefore may not match exactly what is displayed on screen.

This section describes the BIOS setup program. The setup program lets you modify basic configuration settings. The settings are then stored in a dedicated, battery-backed memory (called NVRAM) that retains the information even when the power is turned off.

To start the BIOS setup utility:

- 1. Turn on or reboot your system.
- 2. Press <Del> during POST (<F4> on remote console) to start the BIOS setup utility.

#### 3.2 - BIOS Menu Bar

The menu bar at the top of the windows lists these selections:

Main	To configure basic system setups		
Advanced	To configure the advanced chipset features		
PCI/PnP	To configure legacy Plug & Play or PCI settings		
Boot	To configure system boot order		
Security	To configure user and supervisor passwords		
Chipset	To configure chipset management features		
Exit	To exit setup utility		

#### 3.3 Setup Basics

The table below shows how to navigate in the setup program using the

keyboard.
-----------

Key	Function			
<f1></f1>	General help window			
<esc></esc>	Exit current menu			
← → arrow keys	Select a different menu			
↑ or ↓ arrow keys	Move cursor up/down			
<tab> or <shift-tab></shift-tab></tab>	Cycle cursor up/down			
<home> or <end></end></home>	Move cursor to top/bottom of the window			
<pgup> or <pgdn></pgdn></pgup>	Move cursor to next/previous page			
<->	Select the previous value/setting of the field			
<+>	Select the next value/setting of the field			
<f8></f8>	Load Fail Safe default configuration values of the menu			
<f9></f9>	Load the Optimal default configuration values of the			
	menu			
<f10></f10>	Save and exit			
<enter></enter>	Execute command or select submenu			

### 3.4 Getting Help

Pressing [F1] will display a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window, press [ESC].

#### 3.5 In Case of Problems

If you have trouble booting your computer after making and saving the changes with the BIOS setup program, you can restart the computer by holding the power button down until the computer shuts off (usually within 4 seconds); resetting by pressing CTRL-ALT-DEL; or clearing the CMOS. The best advice is to only alter settings that you thoroughly understand. In

particular, do not change settings in the Chipset section unless you are absolutely sure of what you are doing. The Chipset defaults have been carefully chosen either by TYAN or your system manufacturer for best performance and reliability. Even a seemingly small change to the Chipset setup options may cause the system to become unstable or unusable.

NOTE: The following pages provide the details of BIOS menu. Please be noticed that the BIOS menu are continually changing due to the BIOS updating. The BIOS menu provided are the most updated when this manual is written. Please visit Tyan's website at <a href="http://www.tyan.com">http://www.tyan.com</a> for the information of BIOS updating.

#### 3.6 BIOS Main Menu

The Main BIOS Menu is the first screen that you can navigate. The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed-out" options cannot be configured, options in blue can be changed.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often, a text message will accompany it.

	BIOS Setup Utility					
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit
System Over	view				Use [ENTER [SHIFT-TAB]	
AMIBIOS Version : 0 Build Date : 0 ID : 0					field  Use [+] or [-] configure sys	
Processor Dual-Core Al Speed : Count :		Processor xx	хх		← → Select I	
System Mem Size :: System Time System Date	xxxx MB	[22:21:21] [Tue 01/01/2	2002]		Enter Go to S F1 Genera F10 Save a ESC Exit	al Help

Feature	Option	Description
Main		
System Time	HH: MM: SS	Set the system time
System Date	MM : DD : YYYY	Set the system date

#### 3.7 Advanced Menu

You can select any of the items in the left frame of the screen, such as Super I/O Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screen is shown below. The sub menus are described on the following pages.

BIOS Setup Utility						
Main	Advanced	PCI/PnP	Boot	Securi	ty Chipset	Exit
Advanced S	ettings					
					Options for CI	PU
	etting wrong va			s may		
С	ause system to	malfunction	١.			
➤ CPU Config ➤ IDE Config ➤ Floppy Co ➤ Super IO C ➤ ACPI Confi	guration nfiguration Configuration				← → Select S ↑ ↓ Select Ite Enter Go to S F1 General F10 Save an	em Sub Screen Help
	iguration Configuration Health Configu	ıration			ESC Exit	
	ccess Configur	ation				
▶ USB Confi	•					
	erNow Configu					
• Onboard L	Devices Config	uration				

Feature	Option	Description
Advanced Settings		
CPU Configuration	Menu Item	Options for CPU
IDE Configuration	Menu Item	Configure the IDE device(s)
Floppy Configuration	Menu Item	Configure the Floppy drive(s)
Super IO Configuration	Menu Item	Configures Super IO Chipset SCH5017
ACPI Configuration	Menu Item	Section for Advanced ACPI Configuration
APM Configuration	Menu Item	Section for APM configuration
Event Log Configuration	Menu Item	Mark as read, Clear or View Event Log statistics
Hardware Health Configuration	Menu Item	Configure/monitor the Hardware Health
Remote Access Configuration	Menu Item	Configure Remote Access

Feature	Option	Description			
Advanced Settings					
USB Configuration	Menu Item	Configure the USB support			
AMD PowerNow Configuration	Menu Item	Configure AMD PowerNow support			
Onboard Devices Configuration	Menu Item	Configure onboard devices			

#### 3.7.1 CPU Configuration

You can use this screen to view CPU Configuration Menu. Use the up and down arrow  $(\uparrow/\downarrow)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option. The settings are described on the following pages.

	BIOS Setup Utility				
Main	Advanced	PCI/PnP	Boot	Security	Chipset Exit
CPU Configu Module Versi AGESA Versi Physical Cou Logical Coun	on: XX.XX ion: XXXXX nt: X	x			This option should remain disabled for normal operation. The driver developer may disable it for testing
Revision: Cache L1: Cache L2: Cache L3: Speed: Current FSB Maximum FS Able to chang uCode Patch  GART Error F Microcode Up	B Multiplier: ge Freq.: Level: Reporting odate al Machine Mo		XX XXX XXX XXX XXX XXX XXX XXX XXX XXX	x x x x x	purpose.  ← → Select Screen  ↑ ↓ Select Item +/- Change Option F1 General Help F10 Save and Exit ESC Exit

Feature	Option	Description	
CPU Configuration			
Module Version			
AGESA Version	Read only	Displays information about CPU	
Physical Count	read only	Displays information about of o	
Logical Count			
Revision			
Cache L1			
Cache L2			
Cache L3			
Speed	Read only	Displays information about CPU	
Current FSB Multiplier			
Maximum FSB Multiplier			
Able to change Freq.			
uCode Patch Level			
GART Error Reporting	Disabled	This option should remain disabled for normal operation. The driver	
CART End Reporting	Enabled	developer may enable it for the purpose of testing.	
Microcode Update	Enabled	Enable CPU Microcode update	
Wildrocode Opdate	Disabled	Enable of O Microcode appeare	
Secure Virtual Machine	Enabled	Enable/disable Secure Virtual	
Mode	Disabled	Machine Mode (SVM)	
NMI Function	Enabled	Allow NMI button or SMDC to	
INIVITE UTICUOTI	Disabled	generate NMI	

### 3.7.2 IDE Configuration Sub-Menu

You can use this screen to select options for the IDE Configuration Settings. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option.

BIOS Setup Utility						
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit
IDE Configuration					While entering setup, BIOS auto detects the	
Onboard IDE Serial-ATA De	evices		[Enabl [Devic	ed] e 0/1/2]	presence of devices. Th the status of detection of devices.	is displays f auto
<ul> <li>Primary IDE Master</li> <li>Primary IDE Slave</li> <li>SATA0 (Dev5, Func0)</li> <li>SATA1 (Dev5, Func0)</li> <li>SATA2 (Dev5, Func1)</li> <li>SATA3 (Dev5, Func1)</li> <li>SATA4 (Dev5, Func2)</li> <li>SATA5 (Dev5, Func2)</li> </ul>				← → Select ↑ ↓ Select +/- Chang F1 Gene F10 Save ESC Exit	Item le Option ral Help	
Hard Disk Wri IDE Detect Tir			[Disab [35]	led]		

Feature	Option	Description
IDE Configuration		
Onboard IDE Controller	Enabled	Enable/Disable onboard IDE controller.
Official and the Controller	Disabled	Enable/Bladdle onboard IBE controller.
	Device 0/1/2	
Serial-ATA Devices	Disabled	Configure serial ATA devices.
	Device 0	Configure serial ATA devices.
	Device 0/1	
Hard Disk Write Protect	Disabled	Enable/Disable device write protection. This will be effective only if device is
Traire Blok Write Freder	Enabled	accessed through BIOS.
IDE Detect Time Out (Sec)	<b>0~35</b> (at 5 interval)	Select the time out value for detecting ATA/ATAPI device(s).

### 3.7.2.1 nVidia RAID Setup

	BIOS Setup Utility							
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit		
RAID Setup					While entering BIOS auto d			
nVidia RAID Function			[Disable	ed]	presence of IDE devices. This displays the status of auto detection of IDE devices.			
					← → Select ↑ ↓ Select I +/- Change F1 Genera F10 Save a ESC Exit	tem e Option al Help		

Feature	Option	Description
nVidia RAID Setup		
nVidia Function	Disabled	While entering setup, you can
	Enabled	choose enabled/disabled RAID mode for each ATA channel.

### 3.7.2.2 Primary IDE Master/Slave Sub-Menu

BIOS Setup Utility							
Main Advanced	PCI/PnP	Boot	Security	Chipset	Exit		
Primary IDE Master  Device: Not Detected				Selects the todevice connumbers system.			
Type LBA /Large Mode Block (Multi-Sector Transfer) PIO Mode DMA Mode S.M.A.R.T. 32 Bit Data Transfer		[Auto [Auto [Auto [Auto [Auto [Enal	) ] )] )] )]	Tab Select	Item le Option Field al Help		

Feature	Option	Description
Primary IDE Master		
Туре	Auto Not Installed CD/DVD ARMD	Selects the type of device connected to the system.
LBA/Large Mode	Auto	Auto: Enabled LBA Mode if the device supports it and the device is not already formatted with LBA
EBAY Large Wode	Disabled	Mode disabled. Disabled: Disabled LBA Mode.
Block (Multi-Sector Transfer)	Auto	Disabled: The Data transfer from and to the device occurs one sector at a time.
Block (Multi-occioi Transici)	Disabled	Auto: The Data transfer from and to the device occurs multiple sectors at a time if the device supports it.
PIO Mode	Auto	Selects the PIO Mode. Select Auto to enhance hard disk performance
T TO MOUD	0~4 (at 1 interval)	by optimizing the hard disk timing.
DMA Mode	Auto	Selects DMA Mode. Auto: Auto detected.
	Auto	S.M.A.R.T (Self-Monitoring Analysis
S.M.A.R.T.	Disabled	and Reporting Technology) is a utility that monitors your disk status
	Enabled	to predict hard disk failure.
32Bit Data Transfer	Enabled	Enables 32-bit to maximize the IDE
32DIL Data Transfel	Disabled	hard disk data transfer rate.

#### 3.7.2.3 SATA0/1/2/3/4/5 Sub-Menu

			Setup Utili	,		
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit
SATA0			·			
Device: Not De	etected	<ul> <li>← → Select Screen</li> <li>↑ ↓ Select Item</li> <li>+/- Change Option</li> </ul>	Item			
LBA /Large Mode Block (Multi-Sector Transfer) PIO Mode DMA Mode S.M.A.R.T. 32 Bit Data Transfer		[Auto [Auto [Auto [Auto [Auto	[] [] []	Tab Select	Field al Help	

Feature	Option	Description	
SATA 0			
LBA/Large Mode	Auto	Auto: Enabled LBA Mode if the device supports it and the device is not already formatted with LBA	
LBAVEarge Wode	Disabled	Mode disabled.  Disabled: Disabled LBA Mode.	
Diagle (Multi-Conton Transfer)	Auto	Disabled: The Data transfer from and to the device occurs one sector at a time.	
Block (Multi-Sector Transfer)	Disabled	Auto: The Data transfer from and to the device occurs multiple sectors at a time if the device supports it.	
PIO Mode	Auto	Selects the PIO Mode. Select Auto to enhance hard disk performance	
1 10 Mode	0~4 (at 1 interval)	by optimizing the hard disk timing.	
DMA Mode	Auto	Selects DMA Mode. Auto: Auto detected.	
	Auto	S.M.A.R.T (Self-Monitoring Analysis	
S.M.A.R.T.	Disabled	and Reporting Technology) is a utility that monitors your disk status	
	Enabled	to predict hard disk failure.	
32Bit Data Transfer	Enabled	Enables 32-bit to maximize the IDE	
SZDIL Data Transiei	Disabled	hard disk data transfer rate.	

### 3.7.3 Floppy Configuration Sub-Menu

You can use this screen to specify options for the Floppy Configuration Settings. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages.

	BIOS Setup Utility							
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit		
Floppy Configuration					connected			
					to the syste	em.		
Floppy A Floppy B		[1.44ME [Disable	-					
					←→ Select ↑ ↓ Select +/- Chang F1 Gene F10 Save ESC Exit	t Item e Option ral Help		

Feature	Option	Description
Floppy Configuration		
	Disabled	
	360 KB 51/4"	Selects the type of floppy drive
Floppy A	1.2 MB 51/4"	connected to the system.
	720 KB 31/2"	
	1.44 MB 31/2"	
	2.88 MB 31/2"	
	Disabled	
	360 KB 51/4"	Selects the type of floppy drive
	1.2 MB 51/4"	connected to the system.
Floppy B	720 KB 31/2"	
	1.44 MB 31/2"	
	2.88 MB 31/2"	

### 3.7.4 Super IO Configuration Sub-Menu

You can use this screen to select options for the Super I/O settings. Use the up and down arrow  $(\uparrow/\downarrow)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option

BIOS Setup Utility							
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit	
Configure S	CH5017 Super	or disable l	S to enable Floppy				
Onboard Flo Serial Port1 / Serial Port2 / Chassis Intru Watchdog M Watchdog Ti	Address usion Detect ode		[Enabl [3F8/IF [2F8/IF [Disab [Disab [2]	RQ4] RQ3] led]		t Item nge Option eral Help	

Feature	Option	Description
Configure SCH5017 Sup	oer IO Chipset	
Onboard Floppy	Disabled	Allow BIOS to enable or disable the floppy
Controller	Enabled	controller.
	3F8 IRQ4	
Serial Port1 Address	3E8 IRQ4	Allow BIOS to select Serial Port1 Base
	2E8 IRQ3	Addresses.
	Disabled	
	2F8 IRQ3	
Serial Port2 Address	3F8 IRQ4	Allow BIOS to select Serial Part2 Base
Condition 27 tadiose	2E8 IRQ3	Addresses.
	Disabled	
Chassis Intrusion	Disabled	Enable/Disable the function of chassis intrusion detection. When chassis open
Detect	Enabled	event is detected, BIOS will record the event.
	Disabled	POST: BIOS POST Watchdog timer
Watchdog Mode	POST	counting. Start at PowerON. Stop at OS boot.
	os	OS: OS boot Watchdog. Start at OS boot.
	Power ON	PowerON: Start at PowerON.
Watchdog Timer	2	
	4	Watchdog timer sets 2/4/6/8/10/12
	6	minutes. When WD time-out occurs,
	8	system will auto reboot.
	10	
	12	

### 3.7.5 ACPI Configuration Sub-Menu

Use this screen to select options for ACPI. Use the up and down arrow  $(\uparrow/\downarrow)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on this page. The screen is shown below.

	BIOS Setup Utility					
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit
ACPI Setting	js	Enable ACPI Configuration	settings			
	ACPI Configura PI Configuratio				←→ Select S  ↑ ↓ Select Is  +/- Change F1 Genera F10 Save ar  ESC Exit	em Option I Help

### 3.7.5.1 Advanced ACPI Configuration Sub-Menu

Main <b>Advanced</b>	BIOS PCI/PnP	Setup Utili Boot	ity Security	Chipset	Exit
Advanced ACPI Configura	ation				
ACPI Version Features ACPI APIC support AMI OEMB table Headless mode		[ACPI v2.0 [Enabled] [Enabled] [Disabled]	)]	←→ Select I ↑ ↓ Select I +/- Change F1 Genera F10 Save a ESC Exit	tem e Option al Help

Feature	Option	Description	
Advanced ACPI Configuration			
	ACPI v3.0	Set this value to allow or prevent	
ACPI Version Features	ACPI v2.0	the system to be complaint with	
	ACPI v1.0	the ACPI 2.0 specification.	
ACPI APIC Support	Enabled	This option allows you to define whether or not to enable APIC	
Aci i Ai io Support	Disabled	features.	
AMI OEMB table	Enabled	Set this value to allow the ACPI BIOS to add a pointer to an OEMB table in the Root System Description Table (RSDT) table.	
	Disabled	Note: OEMB table is used to pass POST data to the AMI code during ACPI O/S operations.	
Headless mode	Enabled	Enable or disable Headless	
Headless mode	Disabled	operation mode through ACPI.	

### 3.7.5.2 Chipset ACPI Configuration Sub-Menu

Main	Advanced	BIOS S PCI/PnP	etup Utili Boot	ty Security	Chipset	Exit
MCP55 ACP	I HPET TABLE		[Di	isabled]		
					←→ Select S ↑ ↓ Select It +/- Change F1 Genera F10 Save an ESC Exit	em e Option I Help

Feature	Option	Description
Chipset ACPI Configuration		
MCP55 ACPI HPET TABLE	Disabled	ACPI High Precision Event Timer
WICE 33 ACFITIFET TABLE	Enabled	description table.

# 3.7.6 APM Configuration

		BIOS	Setup Utilit	:y		
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit
Resume On F Resume On I Resume On I Resume On F	PCIE Wake# LAN (MAC)	] ]	[Disabled] [Disabled] [Disabled] [Disabled]		← → Select :  ↑ ↓ Select I: +/- Change	
Restore on A	C Power Loss	[Last State]		F1 Genera F10 Save a ESC Exit	al Help	

Feature	Option	Description
APM Configuration		
Resume On PME#	Disabled	Disable/Enable PME to generate a
	Enabled	wake event.
Resume On PCIE Wake#	Disabled	Disable/Enable PME to generate a
Nesume of Folk Wake#	Enabled	wake event.
Resume On LAN (MAC)	Disabled	Enable/Disable LAN (MAC) to
reseams on E at (wate)	Enabled	generate a wake event.
Resume On RTC Alarm	Disabled	Enable/Disable RTC event to wake
Resultie Off KTC Alaitti	Enabled	after a power failure.
	Last State	Configures how the system heard
Restore on AC Power Loss	Power on	Configures how the system board responds to a power failure.
	Power off	responds to a power failure.

### 3.7.7 Event Log Configuration Sub-Menu

You can use this screen to view the Event Log Control Menu. This logs system events (such as CMOS clear) and writes the log into NVRAM. Use the up and down arrow  $(\uparrow/\downarrow)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option. The settings are described on the following pages.

	BIOS Setup Utility					
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit
Event Loggir	ng details	View all unr				
View Event Lo Mark All Ever Clear Event L	its as Read				Enter Go to	Item ge Option Sub Screen ral Help

Feature	Option	Description
Event Logging details		
View Event Log	_	Views all unread events on the Event Log.
Mark All Events as Read	OK	Marks all unread events as
	Cancel	read.
Clear Event Log	OK	Erases all of events.
Clear Everit Log	Cancel	

### 3.7.8 Hardware Health Configuration Sub-Menu

You can use this screen to view the Hardware Health Configuration Settings. Use the up and down arrow  $(\uparrow / \downarrow)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option. The settings are described on the following pages.

BIOS Setup Utility						
Main <b>Advanced</b>	PCI/PnP	Boot	Security	Chipset	Exit	
Hardware Health Configurat	Enables Har Health Monit					
H/W Health Function CPUFAN1, 2 FAN1, 2 PWM C FAN3, FAN4, FAN5 PWM Cor FAN Fail LED Indicator		[Enabled] [Disabled] [Disabled] [Disabled]		Device.		
Hardware Health Event Mon	itoring			← → Select	Screen	
▶ Mainboard Voltages Report				↑ ↓ Select I +/- Chang Tab Select	e Option	
CPU1 Temperature CPU2 Temperature Ambient Temp (Near NEC) Ambient Temp (Near MCP55)		:xx C/ xxx :xx C/ xxx :xx C/ xxx :xx C/ xxx	F F	F1 Genera F10 Save a ESC Exit	al Help	
CPU1 FAN1 Speed (TACH1) CPU1 FAN2 Speed (TACH2) FAN 1 Speed (TACH3) FAN 2 Speed (TACH4) FAN 3 Speed (TACH5) FAN 4 Speed (TACH6) FAN 5 Speed (TACH7)		:xxxx RPM :xxxx RPM :xxxx RPM :xxxx RPM :xxxx RPM :xxxx RPM :xxxx RPM	 			

Feature	Option Description		
Hardware Health Confi	guration		
H/W Health Function	Enabled	Enables Hardware Health Monitoring Device.	
11/VV Ficaliti Function	Disabled	Enables Traidware Treater Monitoring Device.	
CPUFAN1, 2 FAN1, 2	Disabled	Fan Control Mode Disabled: Fan full speed	
PWM Control	Enabled	Enabled: Fan speed automatically adjusts according to specific temperature.	
FAN3, FAN4, FAN5	Disabled	Fan Control Mode Disabled: Fan full speed	
PWM Control	Enabled	Enabled: Fan speed automatically adjusts according to specific temperature.	
FAN Fail LED	Enabled	Enabled: Any FAN speed less than 800 RPM,	
Indicator	Disabled	the FAN Fail LED will be lighted.	

#### 3.7.8.1 Mainboard Voltages Report Sub-Menu

You can use this screen to monitor mainboard's voltages. Use the up and down arrow  $(\uparrow/\downarrow)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option.

Main <b>Advanced</b>	BIOS S PCI/PnP	Setup Util Boot	ity Security	Chipset	Exit
Board Voltages Event Monitorin		2001	Coounty	- Cimpost	
CPU1 Vdimm CPU2 Vidimm CPU1 Vcore CPU2 Vcore +V3.3 (SB) 3VDU +V5 (SB) VCC +12V (for cpu1 vcore) +12V (for cpu2 vcore)		: x.x : x.x : x.x : x.x : x.x : x.x : x.x	XXX V	↑ ↓ Sele +/- Cha Tab Sele F1 Ger	neral Help ve and Exit

### 3.7.9 Remote Access Configuration Sub-Menu

You can use this screen to view the Remote Access Configuration Menu. This feature allows access to the Server remotely via serial port. Use the up and down arrow  $(\uparrow/\downarrow)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option. The settings are described on the following pages.

	01: 1	<b>-</b> ::			
Main <b>Advanc</b>	ed PCI/PnP	Boot	Security	Chipset	Exit
Configure Remote A	Select remo	ote access			
Remote Access	]]	Enabled]			
Serial Port Number	[(	COM1]			
Base Address, IRQ	Ī	3F8h, 4]			
Serial Port Mode	į,	115200 <sup>-</sup> 8	, n, 1]	← → Selec	t Screen
Flow Control	11	None]		↑ ↓ Select	Item
Redirection After BIOS		Always]			ge Field
Terminal Type	Ţ	ANSÍ			ral Help
VT-UTF8 Combo Key	Support [	Enabled]		F10 Save	
Sredir Memory Display	Delay [۱	No Delay]		ESC Exit	and Exit

Feature	Option	Description
Configure Remote Access	type and paramet	ers
Remote Access	Enabled	Enables remote access to system through serial port.
	Disabled	tinough contai porti
Serial Port Number	COM1	Select Serial Port for console redirection. Make sure the
Ochari ortivamber	COM2	selected port is enabled.
Base Address, IRQ	Read only	Displays Com Port Base Address and IRQ number.
	115200 8,n,1	
Serial Port Mode	57600 8,n,1	Select Serial Port settings.
Serial Fort Wode	19200 8,n,1	Select Serial Fort Settings.
	9600 8,n,1	
	None	
Flow Control	Hardware	Select Flow Control for console redirection.
	Software	

Feature	Option	Description
Configure Remote Access	type and paramet	ers
	Disabled	Disable: Turns off the redirection after POST Boot Loader:
Redirection After BIOS POST	Boot Loader	Redirection is active during POST and during Boot Loader. Always:
	Always	Redirection is always active. <some always="" if="" may="" not="" oss="" set="" to="" work=""></some>
	ANSI	Select the target terminal type.
Terminal Type	VT100	
	VT-UTF8	
VT-UTF8 Combo Key	Enabled	Enable VT-UTF8 Combination key Support for ANSI/VT100 terminals.
Support	Disabled	Support for ANSI/VT 100 terminals.
	No Delay	Gives the delay in seconds to display memory information
Sredir Memory Display Delay	Delay 1 Sec	display memory miormation
	Delay 2 Sec	
	Delay 4 Sec	

### 3.7.10 USB Configuration Sub-Menu

You can use this screen to view the USB Configuration Menu. Use the up and down arrow  $(\uparrow / \downarrow)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option. The settings are described on the following pages.

		BIOS	Setup Ut	ility		
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit
USB Config	uration	Enables USB host controllers.				
Module Vers	ion – X.XX.X->	XX.X			← → Selec	
USB Devices	s Enabled: None		ge Option ral Help			
Legacy USB USB 2.0 Cor BIOS EHCI I	ntroller Mode	[Enal [HiS <sub>]</sub> [Enal	peed]		ESC Exit	anu Exit

Feature	Option	Description
USB Configuration		
Legacy USB Support	Disabled	Enables support for legacy USB.
Legacy COB Capport	Enabled	
	Hi Speed	Configure the USB 2.0
USB 2.0 Controller Mode	Full Speed	controller in Hi Speed (480Mbps) or Full Speed (12Mbps).
BIOS EHCI Hand-Off	Enabled	This is a work around for OSes without EHCI hand-off support.
BIOS ETICITIANU-OII	Disabled	The EHCI ownership change should claim by EHCI driver.

### 3.7.11 AMD PowerNow Configuration Sub-Menu

You can use this screen to view the AMD PowerNow Configuration Menu. Use the up and down arrow  $(\uparrow/\lor)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option. The settings are described on the following pages.

		BIOS	Setup Ut	ility		
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit
AMD Power Power Now	Now Configu		bled]			t Item nge Option eral Help

Feature	Option	Description			
AMD PowerNow Configuration					
Power Now	Enabled	Enable/Disable PowerNow			
1 OWEI NOW	Disabled	Litable/Disable Fowerhow			

### 3.7.12 Onboard Devices Configuration Sub-Menu

You can use this screen to view the Onboard Devices Configuration Menu. Use the up and down arrow  $(\uparrow / \downarrow)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option. The settings are described on the following pages.

		Setup Ut	ility	-
Main <b>Advanced</b>	PCI/PnP	Boot	Security	Chipset Exit
Onboard Device and PCI S	Select remote access type.			
Onboard VGA Onboard SAS Primary Graphics Adapter  USB 1.1 Controller USB 2.0 Controller LAN1 LAN2	[Er [PC [Er [At	nabled] nabled] CI Expres nabled] nabled] nabled] uto]	ss → PCI]	←→ Select Screen ↑↓ Select Item +/- Change Field F1 General Help F10 Save and Exit ESC Exit

Feature	Option	Description			
MPS Configuration					
Onboard VGA/SAS	Disabled	Enabled/Disabled VGA/SAS controller			
Chibdara V CAVOAC	Enabled	Enabled/Disabled VOA/OAC Controlled			
Primary Graphics	PCI Express → PCI	Configure primary graphics adapter.			
Adapter	PCI → PCI Express				
USB 1.1/2.0	Disabled	Enabled/Disabled LAN controller			
Controller	Enabled	Enabled Bloadied Entry Controller			
LAN1/LAN2	Auto Disabled	Configure LAN1/LAN2			

# 3.8 PCI PnP Menu

You can use this screen to view PnP (Plug & Play) BIOS Configuration Menu. This menu allows the user to configure how the BIOS assigns resources & resolves conflicts. Use the up and down arrow ( $\uparrow / \downarrow$ ) keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option. The settings are described on the following pages.

BIOS Setup Utility						
Main	Advanced	PCI/PnP	Boot	Security	y Chipset	Exit
Advanced Po	CI/PnP Settin	Clear NVRAM System Boot.	l during			
WARING: Sei cause system		s may				
Clear NVRAM Plug & Play C PCI Latency T Allocate IRQ of Palette Snoop PCI IDE BusM	D/S Fimer to PCI VGA bing		[No] [No] [64] [Yes] [Disable [Enable		← → Select S ↑ ↓ Select Ite +/- Change F1 General F10 Save an ESC Exit	em Option Help

Feature	Option	Description					
Advanced PCI/PnP Settings	Advanced PCI/PnP Settings						
Clear NVRAM	No	Clears NVRAM during system					
Olean TVT G (IV)	Yes	Boot.					
Plug & Play OS	Yes	No: lets the BIOS configure all the devices in the system. Yes: lets the operating system configure Plug and Play (PnP)					
Thug at hay 00	No	devices not required for boot if your system has a Plug and Play operating system.					
	32	This setting controls how many					
	64	PCI clocks each PCI device can					
	96	hold the bus before another PCI device takes over. When set to					
DCI Latanay Timor	128	higher values, every PCI device					
PCI Latency Timer	160	can conduct transactions for a					
	192	longer time and thus improve the effective PCI bandwidth.					
	224	Values in units of PCI clocks for					
	248	PCI device latency timer register.					
Allocate IRQ to PCI VGA	Yes	Yes: assigns IRQ to PCI VGA card if card requests IRQ.					
7 modulo mag to 1 on vort	No	oa. a . oquosto (Q.					
Palette Snooping	Disabled	This is the default setting and should not be changed unless the VGA card manufacturer requires Palette Snooping to be Enabled.					
T dioles of looping	Enabled	Enabled: informs the PCI devices that an ISA graphics device is installed in the system so the card will function correctly.					
DCLIDE DuaMastar	Disabled	Enabled: BIOS uses PCI bus					
PCI IDE BusMaster	Enabled	mastering for reading / writing to IDE drives.					

#### 3.9 Boot Menu

You can display Boot Setup option by highlighting it using the Arrow  $(\uparrow / \downarrow)$  keys and pressing Enter. The settings are described on the following pages.

		BIOS	Setup Ut	ility		
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit
Boot Settings	5	Configures during Syst	U			
▶ Boot Settin	gs Configurati	on				
➤ Boot Devic ➤ Removable ➤ Network Dr	Drives		Item Sub Screen ral Help			

#### 3.9.1 Boot Settings Configuration Sub-Menu

Use this screen to select options for the Boot Settings Configuration. Use the up and down arrow  $(\uparrow / \downarrow)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option.

Feature	Option	Description				
Boot Settings Configuration						
Quick Boot	Enabled	This option allows user bypass BIOS				
	Disabled	self test during POST.				
Quiet Boot	Disabled	Disabled: displays normal POST messages.				
Quiot Boot	Enabled	Enabled: displays OEM log instead of POST messages.				
Add On ROM Display	Force BIOS	Allows user to force BIOS/Option ROM of add-on cards to be displayed during				
Mode	Keep Current	quiet boot.				
Boot up Num-Lock	On Off	Selects Power-on state for Numlock.				
	Enabled					
PS/2 Mouse Support	Disabled	Selects support for PS/2 Mouse.				
	Auto					
Wait for 'F1' If Error	Enabled	Waits for F1 key to be present if error				
	Disabled	occurs.				
Hit 'DEL' Message Display	Enabled	Displays "Press DEL to run Setup" in				
The DEE Message Display	Disabled	POST.				
Interrupt 19 Capture	Disabled	Enabled: allows option ROMs to trap				
ппенирі тә Саріше	Enabled	interrupt 19.				
Endless Boot	Enabled	Enable/Disable endless loop boot from				
Lifutess Boot	Disabled	BBS table.				

# 3.9.2 Boot Device Priority

Use this screen to select options for the Boot Device Priority. Use the up and down arrow  $(\uparrow/\downarrow)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option.

	BIOS Setup Utility						
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit	
Boot Device	Priority				Specifies sequence		
1st Boot Dev 2nd Boot De			[xx,xxx-xx) [xx,xxx-xx)		A device of parenthes	devices. enclosed in is has bled in the	
					↑ ↓ Selection ↑ ↓ Selection ↑ ↓ Selection ↑ ↓ Selection ↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑	nge Option eral Help e and Exit	

Feature	Option	Description
Boot Device Priority		
1st Boot Device	xx,xxx-xxxxx:xxx	Settings for boot priority.
2nd Boot Device	XX,XXX-XXXXX:XXX	These can be customized depending on your
	Disabled	preference.

#### 3.9.3 Removable Drives

Use this screen to select options for the Removable Drives. Use the up and down arrow  $(\uparrow/\downarrow)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option.

		BIOS	Setup Util	lity		
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit
Removable	Drives					
1st Drive		[	1 <sup>st</sup> FLOPF	PY DRIVE]		
					← → Sele	ect Screen
					↑ ↓ Sele	
						inge Option ieral Help
					F10 Sav	e and Exit
					ESC Exit	

Feature	Option	Description
Removable Drives		
1st Drive	xx,xxx-xxxxx:xxx	Specifies the boot seguence from the available
	Disabled	devices.

#### 3.9.4 Network Drives

Use this screen to select options for the Network Drives. Use the up and down arrow  $(\uparrow/\downarrow)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option.

		BIOS	Setup Uti	lity		
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit
Network Dri	ves					
1st Drive		[Ne	twrok: NV	'IDIA Boo]		
2nd Drive		[Ne	twork:2-N	IVIDIA B]		
					↑ ↓ Sele +/- Cha F1 Ger	inge Option ieral Help e and Exit

Feature	Option	Description	
Network Drives			
1st /2nd Drive	xx,xxx-xxxxx:xxx	Specifies the boot	
	Disabled	sequence from the available devices.	

### 3.10 Security Menu

The system can be configured so that all users must enter a password every time the system boots or when BIOS Setup is entered, using either the Supervisor password or User password. The Supervisor and User passwords activate two different levels of password security. If you select password support, you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed. Make sure you write it down. If you forget it, you must clear CMOS and reconfigure.

		BIOS	Setup U	tility		
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit
Security Set	tings	Install or ch	nange the			
	assword : N				← → Selec	
Change Super Change User	ervisor Passw Password	rord			F1 Gene	ge Option ral Help
Boot Sector \	√irus Protectio	on [	[Disabled]		F10 Save ESC Exit	and Exit

Feature Option		Description				
Security Settings						
Supervisor Password:	Not Installed	If the password has been set,				
Supervisor r assword.	Installed	Installed displays. If no password is set, Not Installed displays.				
User Password:	Not Installed	If the password has been set, Installed displays. If no password				
OSCI I assword.	Installed	is set, Not Installed displays.				
Change Supervisor Password	1	Selects this option to change or install Supervisor Password.				
Change User Password	1	Selects this option to change or install User Password.				
Boot Sector Virus Protection	Disabled	When it is set to [Enabled], BIOS will issue a virus warning				
Boot Sector virus Protection	Enabled	message and beep if a write to the boot sector or the partition table of the HDD is attempted.				

# 3.11 Chipset Menu

BIOS Setup Utility						
Main Advanced PCI/PnP Boot Security	<b>Chipset</b> Exit					
Advanced Chipset Settings Options for NB						
WARNING: Setting wrong values in below sections may	← → Select Screen					
cause system to malfunction.	↑ ↓ Select Item					
▶ Northbridge Configuration	Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit					

### 3.11.1 Northbridge Configuration Sub-Menu

This menu gives options for customizing memory & Hypertransport settings. Select a menu by highlighting it using the Arrow  $(\uparrow / \downarrow)$  keys and pressing Enter. The settings are described on the following pages.

	BIOS Setup Utility					
Main Advanced PCI/F	PηP	Boot	Security	Chipset	Exit	
NorthBridge Chipset Configura	tion					
<ul> <li>Memory Configuration</li> <li>ECC Configuration</li> <li>DRAM Timing Confirugation</li> <li>IOMMU Option Menu</li> </ul>						
Alternate VID Memory Timing Parameters		uto] PU Node	0]			
Memory CLK CAS latency (Tcl) RAS/CAS Delay (Trcd) Min Active RAS (Tras) Row Precharge Time (Trp) RAS/RAS Delay (Trrd) Row Cycle (Trc)	:XX :X :X :X	XX MHz X CLK CLK CLK CLK X CLK		←→ Select ↑ ↓ Select I Enter Go to 5 F1 Genera F10 Save a ESC Exit	tem Sub Screen al Help	

Feature	Option	Description
NorthBridge Chipset Co	onfiguration	
	Auto	
	0.850V	
	1.050V	
Alternate VID	1.025V	
	1.000V	
	0.975V	Specify the alternate VID while in low
	0.950V	power status.
	0.925V	
	0.900V	
	0.875V	
	0.825V	
	0.800V	
Memory Timing	CPU Node 0	Select which node's timing parameters
Parameters	CPU Node 1	to display

Feature	Option	Description				
NorthBridge Chipset Configuration						
Memory CLK	Read only	It shows the clock frequency of the installed SDRAM.				
CAS Latency (Tcl)	Read only	This controls the timing delay (in clock cycles) before SDRAM starts a read command after receiving it.				
RAS/CAS Delay (Trcd)	Read only	When DRAM is refreshed, both rows and columns are addressed separately. This setup item allows you to determine the timing of the transition from RAS (row address strobe) to CAS (column address strobe). The less the clock cycles, the faster the DRAM performance.				
Min Active RAS (Tras)	Read only	This setting allows you to select the number of clock cycles allotted for the RAS pulse width, according to DRAM specifications. The less the clock cycles, the faster the DRAM performance.				
Row Precharge Time (Trp)	Read only	This item controls the number of cycles for Row Address Strobe (RAS) to be allowed to precharge. If insufficient time is allowed for the RAS to accumulate its chage before DRAM refresh, refresh may be incomplete and DRAM may fail to retain data. This item applies only when synchronous DRAM is installed in the system.				
RAS/RAS Delay (Trrd)	Read only	Auto uses hardware compensation values. Other values add to or subtract from hardware generated value. Recommended setting is Auto.				
Row Cycle (Trc)	Read only	Bits 7-4. RAS#-active to RAS#-active or auto refresh of the same bank.				

## 3.11.1.1 Memory Configuration Sub-Menu

This menu has options for memory speed & latency. Use the up and down arrow  $(\uparrow/\downarrow)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option.

BIOS Setup Utility						
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit
Memory Con	figuration	MEMCLK can be set by the code using AUTO, o				
Bank Interlea Node Interlea Channel Inter Enable Clock MemClk Trist Memory Hole CS Sparing E Unganged Mo Power Down Power Down	ving leaving to All DIMMs ate C3/ATLVIE Remapping nable ode Support Enable	)	[Aut [Dis: [Dis: [Ena [Dis: [Ena	abled]	set one of the values.  ← → Select ↑ ↓ Select +/- Chang	ne standard  t Screen Item ge Option ral Help

Feature	Option	Description
Memory Configuration		
Bank / Channel Interleaving	Disabled	Enable Bank / Channel Memory
Dank / Chamile interleaving	Auto	Interleaving
Node Interleaving	Disabled	Enable Node Interleaving
Node interieaving	Auto	Enable Node Interleaving
Enable Clock to All DIMMs	Disabled	Enable unused clocks to DIMMs
Eliable Clock to All Dilvilvis	Enabled	Even Memory slots are not populated.
MemClk Tristate	Disabled	Enable/Disable MemClk Tri-Stating
C3/ATLVID	Enabled	during C3 and Alt VID
Memory Hole Remapping	Enabled	Enable Memory Remapping around
Memory Hole Remapping	Disabled	Memory Hole
CS Sparing Enable	Disabled	Reserve a spare memory rank in
CS Sparing Enable	Enabled	each node.
Unganged Mode Support	Enabled	Enabled: Configured to two single- channel DRAM Controllers
onganged wode Support	Disabled	Disabled : Configured to a single dual-channel DRAM Controller

Power Down Enable	Enabled	Enable or disable DDR power down	
Tower Down Linable	Disabled	mode	
Power Down Mode	Channel	Set DDR power down mode	
1 ower bowit mode	Chip Select	Set DDK power down mode	

## 3.11.1.2 ECC Configuration Sub-Menu

This menu allows the user to configure ECC setup for system & DRAM. Use the up and down arrow  $(\uparrow/\downarrow)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option.

	BIOS	Setup Ut	tility		
Main Advance	ed PCI/PnP	Boot	Security	Chipset	Exit
ECC Configuration	Select the level of ECC protection. Note: The "Super" ECC				
ECC Mode DRAM ECC Enable DRAM SCRUB REDIF 4-Bit ECC Mode DRAM BG Scrub Data Cache BG Scrub L2 Cache BG Scrub L3 Cache BG Scrub		Ena [Ena [1.31 [Disa [Disa	bled] bled] bled]	the DRÁM: so all of me scrubbed ir  ← → Select ↑ ↓ Select +/- Chan F1 Gene	emory is a 8 hours. t Screen

Feature	Option	Description				
ECC Configuration						
	Disabled					
	Basic	Select the level of ECC protection.				
ECC Mode	Good	Note: The "Super" ECC mode dynamically sets the DRAM scrub				
Loc wode	Super	rate so all of memory is scrubbed in				
	Max	8 hours.				
	User					
DRAM ECC Enable	Enabled	DRAM ECC allows hardware to report and correct memory errors				
DIVAM EGG Ellable	Disabled	automatically maintaining system integrity.				
DRAM SCRUB	Disabled	DRAM SCRUB REDIRECT allows the system to correct DRAM ECC				
REDIRECT	Enabled	errors immediately when they occur, even if background scrubbing is on.				
4-Bit ECC Mode	Disabled	Enable 4-Bit ECC Mode. Note: Also known as CHIPKILL ECC				
4-Bit LOO Midde	Enabled	Mode Mode				

	Disabled	<u> </u>	
	40ns		
	80ns		
	160ns		
	320ns		
	640ns		
	1.28us		
	2.56us		
	5.12us	DRAM scrubbing corrects memory	
	10.2us	errors so later reads are correct.	
	20.5us	Doing this while memory is not being	
DRAM BG Scrub	41.0us	used improves performance.	
	81.9us	Note: When AMD's node interleave	
	163.8us	feature is enabled, BIOS will force DRAM scrub off.	
	327.7us	DRAW SCIUD OII.	
	655.4us		
	1.31ms		
	2.62ms		
	5.24ms		
	10.49ms		
	20.97ms		
	42.00ms		
	84.00ms		
	Disabled		
	40ns		
	80ns		
	160ns		
	320ns		
	640ns		
	1.28us		
Data Cache BG Scrub	2.56us	Allows the L1 Data Cache RAM to	
Data Cache BG Scrub	5.12us	be corrected while idle.	
	10.2us		
	20.5us		
	41.0us		
	81.9us		
	163.8us		
	327.7us		
	655.4us		

	Disabled	
	40ns	
	80ns	
	160ns	
	320ns	
	640ns	
	1.28us	Allows the L2/L3 Data Cache RAM
L2 /L3 Cache BG Scrub	2.56us	to be corrected while idle.
LZ /L3 Cache BO Scrub	5.12us	
	10.2us	
	20.5us	
	41.0us	
	81.9us	
	163.8us	
	327.7us	
	655.4us	

## 3.11.1.3 DRAM Timing Configuration Sub-Menu

This menu allows the user to configure DRAM Timing. Use the up and down arrow  $(\uparrow/\psi)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option.

		tility			
Main	Advanced	PCI/PnP	Boot	Security	Chipset Exit
DRAM Timii	ng Configura	tion			Auto Limit Manual
Memory Cloc DRAM Timir			[Auto	4	←→ Select Screen  ↑ ↓ Select Item  +/- Change Option F1 General Help F10 Save and Exit ESC Exit

Feature	Option	Description					
DRAM Timing Configuration							
	Auto	Select the DRAM Frequency programming method. If Auto, the					
Memory Clock Mode	Limit	DRAM speed will be based on SPDs. If Limit, the DRAM speed will not exceed the specified value. If					
	Manual	Manual, the DRAM speed specified will be programmed by users.					
	Auto						
DRAM Timing Mode	DCT 0	Allow users to configure the DRAM					
DIVANI FILITING Mode	DCT 1	Timing manually.					
	Both						

## 3.11.1.4 IOMMU Option Sub-Menu

This menu has options for IOMMU. Use the up and down arrow  $(\uparrow/\downarrow)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option.

	BIOS Setup Utility						
Main	Advanced	PCI/PnP	Boot	Śecurity	Chipset	Exit	
IOMMU Mode			[128MB]		or disable Some OSo valid GAR operation, present, s	vithout AGP, altogether. es require T for proper If AGP is elect e option to	
					← → Selectory → Selectory ← Charactery ← Ch	ct Item nge Option eral Help	

Feature	Option	Description	
IOMMU Option			
	AGP Present		
	Disabled	Set GART size in systems without	
	32 MB	AGP, or disable altogether. Some	
IOMMU Mode	64 MB	OSes require valid GART for proper operation. If AGP is present, select	
IOMINO Mode	128 MB	appropriate option to ensure proper	
	256 MB	AGP operation.	
	512 MB	·	
	1 GB		

#### 3.12 Exit Menu

You can display an Exit BIOS Setup option by highlighting it Arrow  $(\uparrow/\downarrow)$  keys and pressing Enter.

Main	Advanced	BIOS PCI/PnP	Setup U	tility Securit	y Chipset <b>Exit</b>
Exit Options	S				Exit system setup after saving the changes.
Save Chang Discard Cha Discard Cha Load Optima Load Failsaf	nges and Exit rges al Defaults				F10 key can be used for this operation.  ← → Select Screen  ↑ ↓ Select Item  Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit

#### Save Changes and Exit

Use this option to exit setup utility and re-boot. All new selections you have made are stored into CMOS.

System will use the new settings to boot up.

#### **Discard Changes and Exit**

Use this option to exit setup utility and re-boot.

All new selections you have made are not stored into CMOS.

System will use the old settings to boot up.

### **Discard Changes**

Use this option to restore all new setup values that you have made but not saved into CMOS.

### **Load Optimal Defaults**

Use this option to load default performance setup values.

Use this option when system CMOS values have been corrupted or modified incorrectly.

#### Load Failsafe Defaults

Use this option to load all default failsafe setup values.

Use this option when troubleshooting.

## **Chapter 4: Diagnostics**

**NOTE**: if you experience problems with setting up your system, always check the following things in the following order:

### Memory, Video, CPU

By checking these items, you will most likely find out what the problem might have been when setting up your system. For more information on troubleshooting, check the TYAN website at: <a href="http://www.tyan.com">http://www.tyan.com</a>.

### 4.1 Beep Codes

Fatal errors, which halt the boot process, are communicated through two kinds of audible beeps.

- •Eight short beeps: It indicates that a video error has occurred.
- •A single long beep repeatedly: It indicates that a DRAM error has occurred.

The most common type of error is a memory error.

Before contacting your vendor or TYAN Technical Support, be sure that you note as much as you can about the beep code length and order that you experience. Also, be ready with information regarding add-in cards, drives and O/S to speed the support process and come to a quicker solution.

### 4.2 Flash Utility

Every BIOS file is unique for the motherboard it was designed for. For Flash Utilities, BIOS downloads, and information on how to properly use the Flash Utility with your motherboard, please check the TYAN web site: <a href="http://www.tyan.com/">http://www.tyan.com/</a>

**NOTE:** Please be aware that by flashing your BIOS, you agree that in the event of a BIOS flash failure, you must contact your dealer for a replacement BIOS. There are no exceptions. TYAN does not have a policy for replacing BIOS chips directly with end users. In no event will TYAN be held responsible for damages done by the end user.

## **4.3 AMIBIOS Post Code**

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize
	BIOS, POST, Runtime data area. Also initialize BIOS modules on
	POST entry and GPNV area. Initialized CMOS as mentioned in the
	Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and
	CMOS checksum is OK. Verify CMOS checksum manually by
	reading storage area. If the CMOS checksum is bad, update CMOS
	with power-on default values and clear passwords. Initialize status
	register A.
	Initializes data variables that are based on CMOS setup questions.
	Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and
	interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer.Install
	the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer
	interrupt.
00	Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
08	Initializes the CPU. The BAT test is being done on KBC. Program
	the keyboard controller command byte is being done after Auto
04	detection of KB/MS using AMI KB-5.
0A 0B	Initializes the 8042 compatible Key Board Controller.  Detects the presence of PS/2 mouse.
OC OC	·
0E	Detects the presence of Keyboard in KBC port.  Testing and initialization of different Input Devices. Also, update the
OL.	Kernel Variables.
	Traps the INT09h vector, so that the POST INT09h handler gets
	control for IRQ1. Uncompress all available language, BIOS logo, and
	Silent logo modules.
13	Early POST initialization of chipset registers.
24	Uncompress and initialize any platform specific BIOS modules.
30	Initialize System Management Interrupt.
2A	Initializes different devices through DIM.
	See DIM Code Checkpoints section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter
	installed in the system that have optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to
	ADM module for initialization. Initialize language and font modules for
	ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text
	information.
37	Displaying sign-on message, CPU information, setup key message,
	and any OEM specific information.

Checkpoint	Description
38	Initializes different devices through DIM. See DIM Code Checkpoints
	section of document for more information.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, etc.) successfully installed in the system and update the BDA, EBDAetc.
50	Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7A	Initializes remaining option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested.
8C	Late POST initialization of chipset registers.
8E	Program the peripheral parameters. Enable/Disable NMI as selected
90	Late POST initialization of system management interrupt.
A0	Check boot password if installed.
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A8	Prepare CPU for OS boot including final MTRR values.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector. Deinitializes the ADM module.
AB	Prepare BBS for Int 19 boot.
AC	End of POST initialization of chipset registers.
B1	Save system context for ACPI.
00	Passes control to OS Loader (typically INT19h).

# **NOTE**

# **Appendix: SMDC Information**

#### Overview

Tyan Server Management Daughter Card (SMDC) is a powerful yet costefficient solution for high-end server management hardware packages. Tyan's goal is to provide remote system monitoring and control even when the operating system is absence or simply fails. This empowers Tyan's server board with advanced industrial-standard features.

Tyan SMDC is a snap-in card that provides essential server management solution. It enables any IT Manager by providing multi-interfaces to access the hardware remotely and perform **monitor**, **control** and **diagnose** activities effectively.

Tyan SMDC is not a peripheral card. Unlike regular peripheral card such as AGP card, Network card or SCSI card, SMDC does not require any hardware specific driver. As long as a standby power comes into the system, SMDC will begin looking after the system.

Tyan SMDC provides diversified methods to communicate with the hardware. IT manager has the flexibility to choose among *Keyboard Controller Style* (KCS), *Block Transfer* (BT) style, Intelligent Chassis Management Bus (ICMB), Intelligent Platform Management Bus (IPMB), Emergency Management Port (EMP) and standard IPMI-Over-LAN communication as defined in latest IPMI 1.5 specification.

Tyan SMDC is compatible with all IPMI-compliance software as well as Tyan System Operator<sup>TM</sup> (TSO) software package.

By adding SMDC, Tyan's server board becomes a highly manageable and IPMI compatible system with all the advanced features suggesting in IPMI Spec.

More detailed information on Tyan's SMDC card can be found on our website: <a href="http://www.tyan.com">http://www.tyan.com</a>

### **Features of Tyan Server Management**



Monitor various system components remotely -such as fans, processor temperature, and more



Remote power on and power off



Console redirect -the ability to view system remotely



Alert and error actions -such as audible beep, e-mail, power down and reboot



SMDC runs on stand-by power -the SMDC will continue to function, even if the system is not powered on

#### How SMDC and TSO Work

The brief descriptions below will help explain how these items function.

<b>→</b>	Agent – a system with SMDC installed The SMDC is installed in the Agent system that uses a compatible/supported Tyan motherboard.
THE CONTRACT OF THE CONTRACT O	Manager – manages the Agent The Manger is set up to manage the Agent that has the SMDC. The Manager and Agent should be located in the same place.
	Console – communicates with Manager The Console is used to monitor and control the Agent through the Manager.

## **Glossary**

**ACPI (Advanced Configuration and Power Interface):** a power management specification that allows the operating system to control the amount of power distributed to the computer's devices. Devices not in use can be turned off, reducing unnecessary power expenditure.

**AGP** (Accelerated Graphics Port): a PCI-based interface which was designed specifically for demands of 3D graphics applications. The 32-bit AGP channel directly links the graphics controller to the main memory. While the channel runs only at 66 MHz, it supports data transmission during both the rising and falling ends of the clock cycle, yielding an effective speed of 133 MHz.

**ATAPI (AT Attachment Packet Interface):** also known as IDE or ATA; a drive implementation that includes the disk controller on the device itself. It allows CD-ROMs and tape drives to be configured as master or slave devices, just like HDDs.

**ATX:** the form factor designed to replace the AT form factor. It improves on the AT design by rotating the board 90 degrees, so that the IDE connectors are closer to the drive bays, and the CPU is closer to the power supply and cooling fan. The keyboard, mouse, USB, serial, and parallel ports are built-in.

**Bandwidth:** refers to carrying capacity. The greater the bandwidth, the more data the bus, phone line, or other electrical path can carry. Greater bandwidth results in greater speed.

BBS (BIOS Boot Specification): a feature within the BIOS that creates, prioritizes, and maintains a list of all Initial Program Load (IPL) devices, and then stores that list in NVRAM. IPL devices have the ability to load and execute an OS, as well as provide the ability to return to the BIOS if the OS load process fails. At that point, the next IPL device is called upon to attempt loading of the OS.

**BIOS (Basic Input/Output System):** the program that resides in the ROM chip, which provides the basic instructions for controlling your computer's hardware. Both the operating system and application software use BIOS routines to ensure compatibility.

**Buffer:** a portion of RAM which is used to temporarily store data; usually from an application though it is also used when printing and in most keyboard drivers. The CPU can manipulate data in a buffer before copying it to a disk drive. While this improves system performance (reading to or writing from a disk drive a single time is much faster than doing so repeatedly) there is the possibility of

losing your data should the system crash. Information in a buffer is temporarily stored, not permanently saved.

**Bus:** a data pathway. The term is used especially to refer to the connection between the processor and system memory, and between the processor and PCI or ISA local buses.

**Bus mastering:** allows peripheral devices and IDEs to access the system memory without going through the CPU (similar to DMA channels).

**Cache:** a temporary storage area for data that will be needed often by an application. Using a cache lowers data access times since the information is stored in SRAM instead of slower DRAM. Note that the cache is also much smaller than your regular memory: a typical cache size is 512KB, while you may have as much as 4GB of regular memory.

**Closed and open jumpers:** jumpers and jumper pins are active when they are "on" or "closed", and inactive when they are "off" or "open".

**CMOS (Complementary Metal-Oxide Semiconductors):** chips that hold the basic startup information for the BIOS.

**COM port:** another name for the serial port, which is called as such because it transmits the eight bits of a byte of data along one wire, and receives data on another single wire (that is, the data is transmitted in serial form, one bit after another). Parallel ports transmit the bits of a byte on eight different wires at the same time (that is, in parallel form, eight bits at the same time).

**DDR (Double Data Rate):** a technology designed to double the clock speed of the memory. It activates output on both the rising and falling edge of the system clock rather than on just the rising edge, potentially doubling output.

**DIMM (Dual In-line Memory Module):** faster and more capacious form of RAM than SIMMs, and do not need to be installed in pairs.

**DIMM bank:** sometimes called DIMM socket because the physical slot and the logical unit are the same. That is, one DIMM module fits into one DIMM socket, which is capable of acting as a memory bank.

**DMA (Direct Memory Access):** channels that are similar to IRQs. DMA channels allow hardware devices (like soundcards or keyboards) to access the main memory without involving the CPU. This frees up CPU resources for other tasks. As with IRQs, it is vital that you do not double up devices on a single line. Plug-n-Play devices will take care of this for you.

**DRAM (Dynamic RAM):** widely available, very affordable form of RAM which looses data if it is not recharged regularly (every few milliseconds). This refresh requirement makes DRAM three to ten times slower than non-recharged RAM such as SRAM.

**ECC (Error Correction Code or Error Checking and Correcting):** allows data to be checked for errors during run-time. Errors can subsequently be corrected at the same time that they're found.

**EEPROM** (Electrically Erasable Programmable ROM): also called Flash BIOS, it is a ROM chip which can, unlike normal ROM, be updated. This allows you to keep up with changes in the BIOS programs without having to buy a new chip. TYAN's BIOS updates can be found at http://www.tyan.com

**ESCD (Extended System Configuration Data):** a format for storing information about Plug-n-Play devices in the system BIOS. This information helps properly configure the system each time it boots.

**Firmware:** low-level software that controls the system hardware.

**Form factor:** an industry term for the size, shape, power supply type, and external connector type of the Personal Computer Board (PCB) or motherboard. The standard form factors are the AT and ATX.

Global timer: onboard hardware timer, such as the Real-Time Clock (RTC).

**HDD:** stands for Hard Disk Drive, a type of fixed drive.

**H-SYNC:** controls the horizontal synchronization/properties of the monitor.

HyperTransport<sup>™</sup>: a high speed, low latency, scalable point-to-point link for interconnecting ICs on boards. It can be significantly faster than a PCI bus for an equivalent number of pins. It provides the bandwidth and flexibility critical for today's networking and computing platforms while retaining the fundamental programming model of PCI.

IC (Integrated Circuit): the formal name for the computer chip.

**IDE** (Integrated Device/Drive Electronics): a simple, self-contained HDD interface. It can handle drives up to 8.4 GB in size. Almost all IDEs sold now are in fact Enhanced IDEs (EIDEs), with maximum capacity determined by the hardware controller.

**IDE INT (IDE Interrupt):** a hardware interrupt signal that goes to the IDE.

**I/O (Input/Output):** the connection between your computer and another piece of hardware (mouse, keyboard, etc.)

**IRQ** (Interrupt Request): an electronic request that runs from a hardware device to the CPU. The interrupt controller assigns priorities to incoming requests and delivers them to the CPU. It is important that there is only one device hooked up to each IRQ line; doubling up devices on IRQ lines can lock

up your system. Plug-n-Play operating systems can take care of these details for you.

**Latency:** the amount of time that one part of a system spends waiting for another part to catch up. This occurs most commonly when the system sends data out to a peripheral device and has to wait for the peripheral to spread (peripherals tend to be slower than onboard system components).

**NVRAM:** ROM and EEPROM are both examples of Non-Volatile RAM, memory that holds its data without power. DRAM, in contrast, is volatile.

**Parallel port:** transmits the bits of a byte on eight different wires at the same time.

**PCI** (Peripheral Component Interconnect): a 32 or 64-bit local bus (data pathway) which is faster than the ISA bus. Local buses are those which operate within a single system (as opposed to a network bus, which connects multiple systems).

**PCI PIO (PCI Programmable Input/Output) modes:** the data transfer modes used by IDE drives. These modes use the CPU for data transfer (in contrast, DMA channels do not). PCI refers to the type of bus used by these modes to communicate with the CPU.

**PCI-to-PCI bridge:** allows you to connect multiple PCI devices onto one PCI slot.

**Pipeline burst SRAM:** a fast secondary cache. It is used as a secondary cache because SRAM is slower than SDRAM, but usually larger. Data is cached first to the faster primary cache, and then, when the primary cache is full, to the slower secondary cache.

**PnP** (Plug-n-Play): a design standard that has become ascendant in the industry. Plug-n-Play devices require little set-up to use. Devices and operating systems that are not Plug-n-Play require you to reconfigure your system each time you add or change any part of your hardware.

**PXE** (**Preboot Execution Environment**): one of four components that together make up the Wired for Management 2.0 baseline specification. PXE was designed to define a standard set of preboot protocol services within a client with the goal of allowing networked-based booting to boot using industry standard protocols.

**RAID** (Redundant Array of Independent Disks): a way for the same data to be stored in different places on many hard drives. By using this method, the data is stored redundantly and multiple hard drives will appear as a single drive to the operating system. RAID level 0 is known as striping, where data is striped (or overlapped) across multiple hard drives, but offers no fault-tolerance. RAID

level 1 is known as mirroring, which stores the data within at least two hard drives, but does not stripe. RAID level 1 also allows for faster access time and fault-tolerance, since either hard drive can be read at the same time. RAID level 0+1 is both striping and mirroring, providing fault-tolerance, striping, and faster access all at the same time.

RAIDIOS: RAID I/O Steering (Intel)

**RAM (Random Access Memory):** technically refers to a type of memory where any byte can be accessed without touching the adjacent data and is often referred to the system's main memory. This memory is available to any program running on the computer.

**ROM (Read-Only Memory):** a storage chip which contains the BIOS; the basic instructions required to boot the computer and start up the operating system.

**SDRAM (Synchronous Dynamic RAM):** called as such because it can keep two sets of memory addresses open simultaneously. By transferring data alternately from one set of addresses and then the other, SDRAM cuts down on the delays associated with non-synchronous RAM, which must close one address bank before opening the next.

**Serial port:** called as such because it transmits the eight bits of a byte of data along one wire, and receives data on another single wire (that is, the data is transmitted in serial form, one bit after another).

Sleep/Suspend mode: in this mode, all devices except the CPU shut down.

**SDRAM** (Static RAM): unlike DRAM, this type of RAM does not need to be refreshed in order to prevent data loss. Thus, it is faster and more expensive.

**SLI (Scalable Link Interface)**: NVIDIA SLI technology links two graphics cards together to provide scalability and increased performance. NVIDIA SLI takes advantage of the increased bandwidth of the PCI Express bus architecture, and features hardware and software innovations within NVIDIA GPUs (graphics processing units) and NVIDIA MCPs (media and communications processors). Depending on the application, NVIDIA SLI can deliver as much as two times the performance of a single GPU configuration.

**Standby mode:** in this mode, the video and hard drives shut down; all other devices continue to operate normally.

**UltraDMA-33/66/100:** a fast version of the old DMA channel. UltraDMA is also called UltraATA. Without a proper UltraDMA controller, your system cannot take advantage of higher data transfer rates of the new UltraDMA/UltraATA hard drives.

**USB (Universal Serial Bus):** a versatile port. This one port type can function as a serial, parallel, mouse, keyboard or joystick port. It is fast enough to support video transfer, and is capable of supporting up to 127 daisy-chained peripheral devices.

VGA (Video Graphics Array): the PC video display standard

**V-SYNC:** controls the vertical scanning properties of the monitor.

**ZCR (Zero Channel RAID):** PCI card that allows a RAID card to use the onboard SCSI chip, thus lowering cost of RAID solution

**ZIF Socket (Zero Insertion Force socket):** these sockets make it possible to insert CPUs without damaging the sensitive CPU pins. The CPU is lightly placed in an open ZIF socket, and a lever is pulled down. This shifts the processor over and down, guiding it into the board and locking it into place.

# **Technical Support**

If a problem arises with your system, you should turn to your dealer for help first. Your system has most likely been configured by them, and they should have the best idea of what hardware and software your system contains. Furthermore, if you purchased your system from a dealer near you, you can bring your system to them to have it serviced instead of attempting to do so yourself (which can have expensive consequences).

#### Help Resources:

- 1. See the beep codes section of this manual.
- 2. See the TYAN website for FAQ's, bulletins, driver updates, and other information: http://www.tyan.com
- 3. Contact your dealer for help BEFORE calling TYAN.
- 4. Check the TYAN user group: alt.comp.periphs.mainboard.TYAN

### **Returning Merchandise for Service**

During the warranty period, contact your distributor or system vendor FIRST for any product problems. This warranty only covers normal customer use and does not cover damages incurred during shipping or failure due to the alteration, misuse, abuse, or improper maintenance of products.

NOTE: A receipt or copy of your invoice marked with the date of purchase is required before any warranty service can be rendered. You may obtain service by calling the manufacturer for a Return Merchandise Authorization (RMA) number. The RMA number should be prominently displayed on the outside of the shipping carton and the package should be mailed prepaid. TYAN will pay to have the board shipped back to you.



#### Notice for the USA

Compliance Information Statement (Declaration of Conformity Procedure) DoC FCC Part 15: This device complies with part 15 of the FCC Rules

Operation is subject to the following conditions:

This device may not cause harmful interference, and
This device must accept any interference received including interference that
may cause undesired operation. If this equipment does cause harmful
interference to radio or television reception, which can be determined by turning
the equipment off and on, the user is encouraged to try one or more of the
following measures:

Reorient or relocate the receiving antenna.

Increase the separation between the equipment and the receiver. Plug the equipment into an outlet on a circuit different from that of the receiver. Consult the dealer on an experienced radio/television technician for help.

#### Notice for Canada

This apparatus complies with the Class B limits for radio interference as specified in the Canadian Department of Communications Radio Interference Regulations. (Cet appareil est conforme aux norms de Classe B d'interference radio tel que specifie par le Ministere Canadien des Communications dans les reglements d'ineteference radio.)



Notice for Europe (CE Mark)
This product is in conformity with the Council Directive
89/336/EEC, 92/31/EEC (EMC).

CAUTION: Lithium battery included with this board. Do not puncture, mutilate, or dispose of battery in fire. Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by manufacturer. Dispose of used battery according to manufacturer instructions and in accordance with your local regulations.

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