

TC74VHC153F, TC74VHC153FN, TC74VHC153FT, TC74VHC153FK

Dual 4-Channel Multiplexer

The TC74VHC153 is an advanced high speed CMOS DUAL 4-CHANNEL MULTIPLEXERS fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Each of these data (1C0-1C3, 2C0-2C3) is selected by the two address inputs A and B.

Separate strobe inputs ($\overline{1G}$, $\overline{2G}$) are provided for each of the two four-line sections.

The strobe input (\overline{G}) can be used to inhibit the data output; the output is fixed in low level while the strobe input is held high.

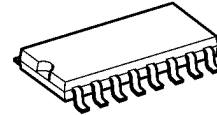
An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High speed: $t_{pd} = 5.0 \text{ ns}$ (typ.) at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 4 \mu\text{A}$ (max) at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC}(\text{opr}) = 2 \text{ to } 5.5 \text{ V}$
- Pin and function compatible with 74ALS153

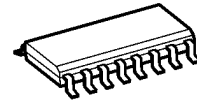
Note: xxxFN (JEDEC SOP) is not available in Japan.

TC74VHC153F



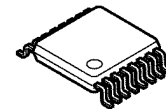
SOP16-P-300-1.27A

TC74VHC153FN



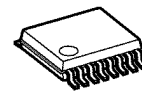
SOL16-P-150-1.27

TC74VHC153FT



TSSOP16-P-0044-0.65A

TC74VHC153FK

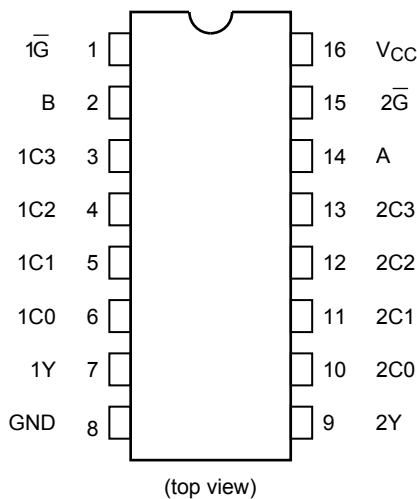


VSSOP16-P-0030-0.50

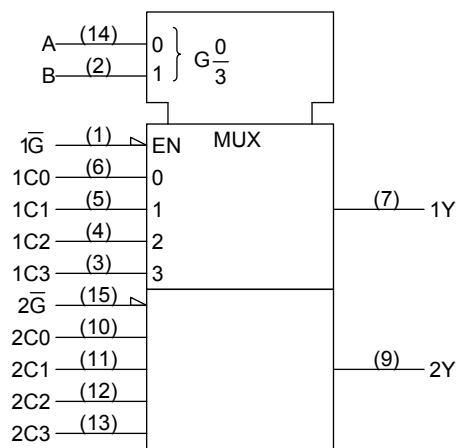
Weight

SOP16-P-300-1.27A	: 0.18 g (typ.)
SOL16-P-150-1.27	: 0.13 g (typ.)
TSSOP16-P-0044-0.65A	: 0.06 g (typ.)
VSSOP16-P-0030-0.50	: 0.02 g (typ.)

Pin Assignment



IEC Logic Symbol

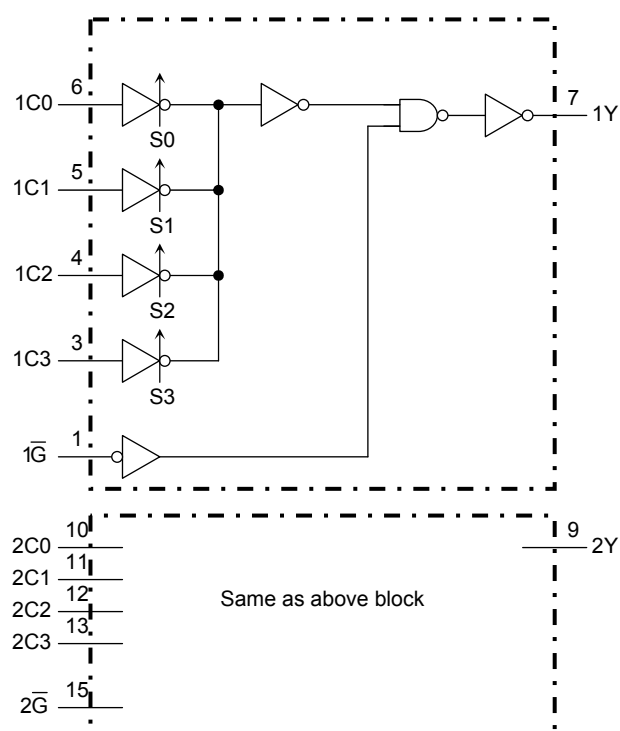
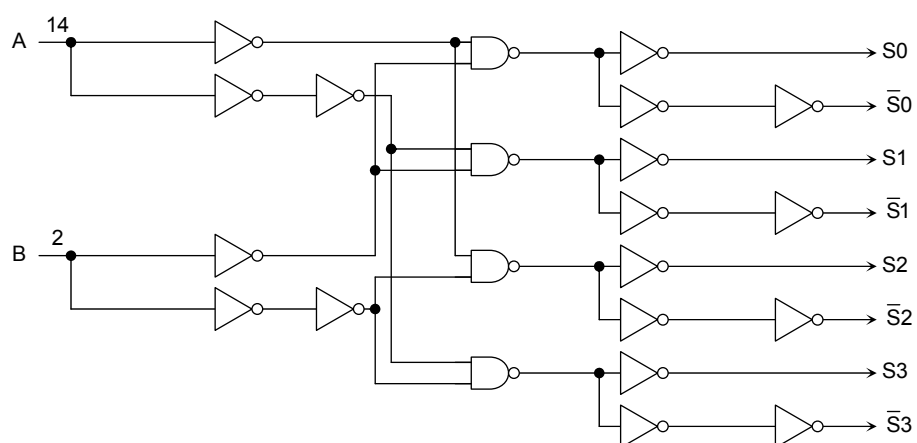


Truth Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	\overline{G}	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

X: Don't care

System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to 7.0	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Operating Range (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V)	ns/V

Note : The operating range must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V _{CC} (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V _{IH}	—		2.0 3.0 to 5.5	1.50 V _{CC} × 0.7	— —	— —	1.50 V _{CC} × 0.7	— —	V
Low-level input voltage	V _{IL}	—		2.0 3.0 to 5.5	— —	— —	0.50 V _{CC} × 0.3	— —	0.50 V _{CC} × 0.3	V
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I _{OH} = -4 mA	3.0	2.58	—	—	2.48	—	
I _{OH} = -8 mA	4.5	3.94		—	—	3.80	—			
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I _{OL} = 4 mA	3.0	—	—	0.36	—	0.44	
I _{OL} = 8 mA	4.5	—		—	0.36	—	0.44			
Input leakage current	I _{IN}	V _{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	4.0	—	40.0	μA

AC Characteristics (input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
			V _{CC} (V)	C _L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (Cn-Y)	t _{pLH} t _{pHL}	—	3.3 ± 0.3	15	—	7.7	11.9	1.0	14.0	ns
				50	—	10.2	15.4	1.0	17.5	
			5.0 ± 0.5	15	—	5.0	7.7	1.0	9.0	
				50	—	6.5	9.7	1.0	11.0	
Propagation delay time (A, B-Y)	t _{pLH} t _{pHL}	—	3.3 ± 0.3	15	—	10.8	16.7	1.0	19.5	ns
				50	—	13.3	20.2	1.0	23.0	
			5.0 ± 0.5	15	—	6.8	9.9	1.0	11.5	
				50	—	8.3	11.9	1.0	13.5	
Propagation delay time (\overline{G} -Y)	t _{pLH} t _{pHL}	—	3.3 ± 0.3	15	—	6.3	10.1	1.0	12.0	ns
				50	—	8.8	13.6	1.0	15.5	
			5.0 ± 0.5	15	—	4.4	6.4	1.0	7.5	
				50	—	5.9	8.4	1.0	9.5	
Input capacitance	C _{IN}	—			—	4	10	—	10	pF
Power dissipation capacitance	C _{PD}	(Note)			—	20	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

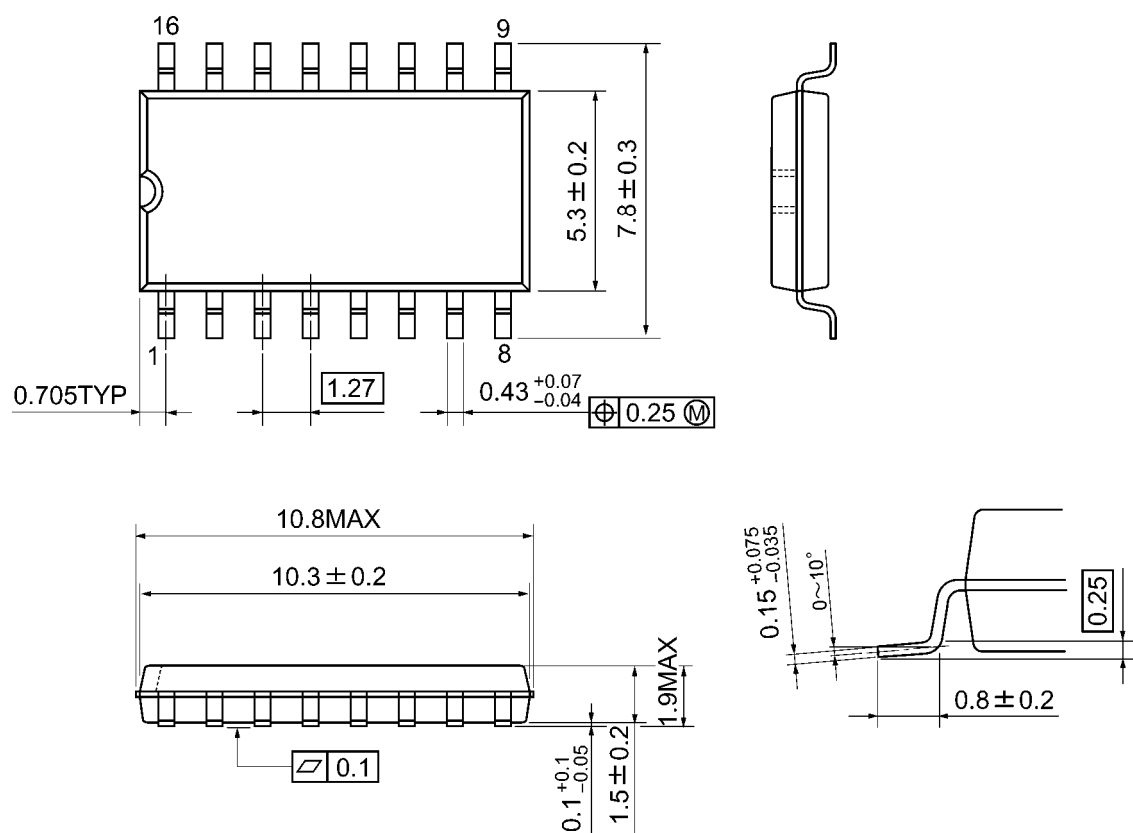
$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

The diagram shows a CMOS inverter circuit. An input signal, labeled "INPUT", is connected to the input of a CMOS inverter. The inverter consists of an NMOS transistor (bottom) and a PMOS transistor (top). The gates of both transistors are connected to the input. The source of the NMOS is connected to ground, and the source of the PMOS is connected to a pull-up resistor, which is in turn connected to a switch. The output of the inverter is taken from the common drain connection of the two transistors. The output line is shown with a dashed line indicating it continues.

Package Dimensions

SOP16-P-300-1.27A

Unit: mm

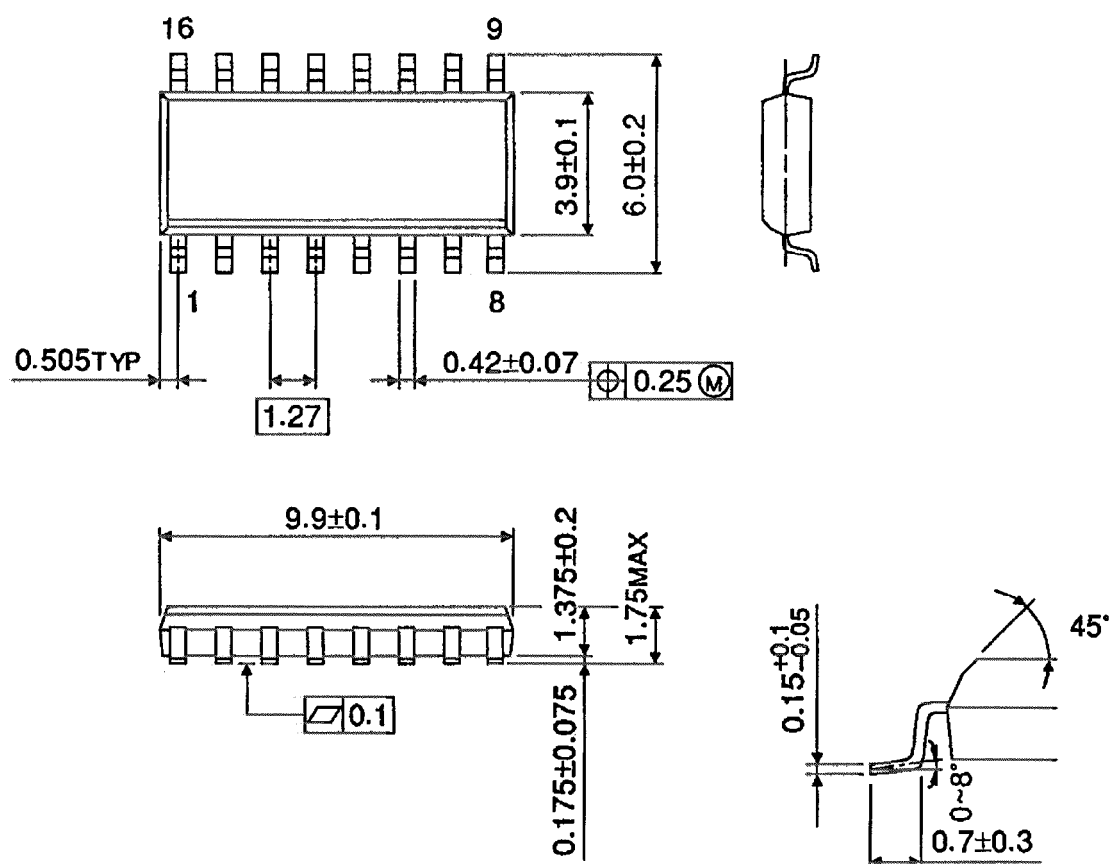


Weight: 0.18 g (typ.)

Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



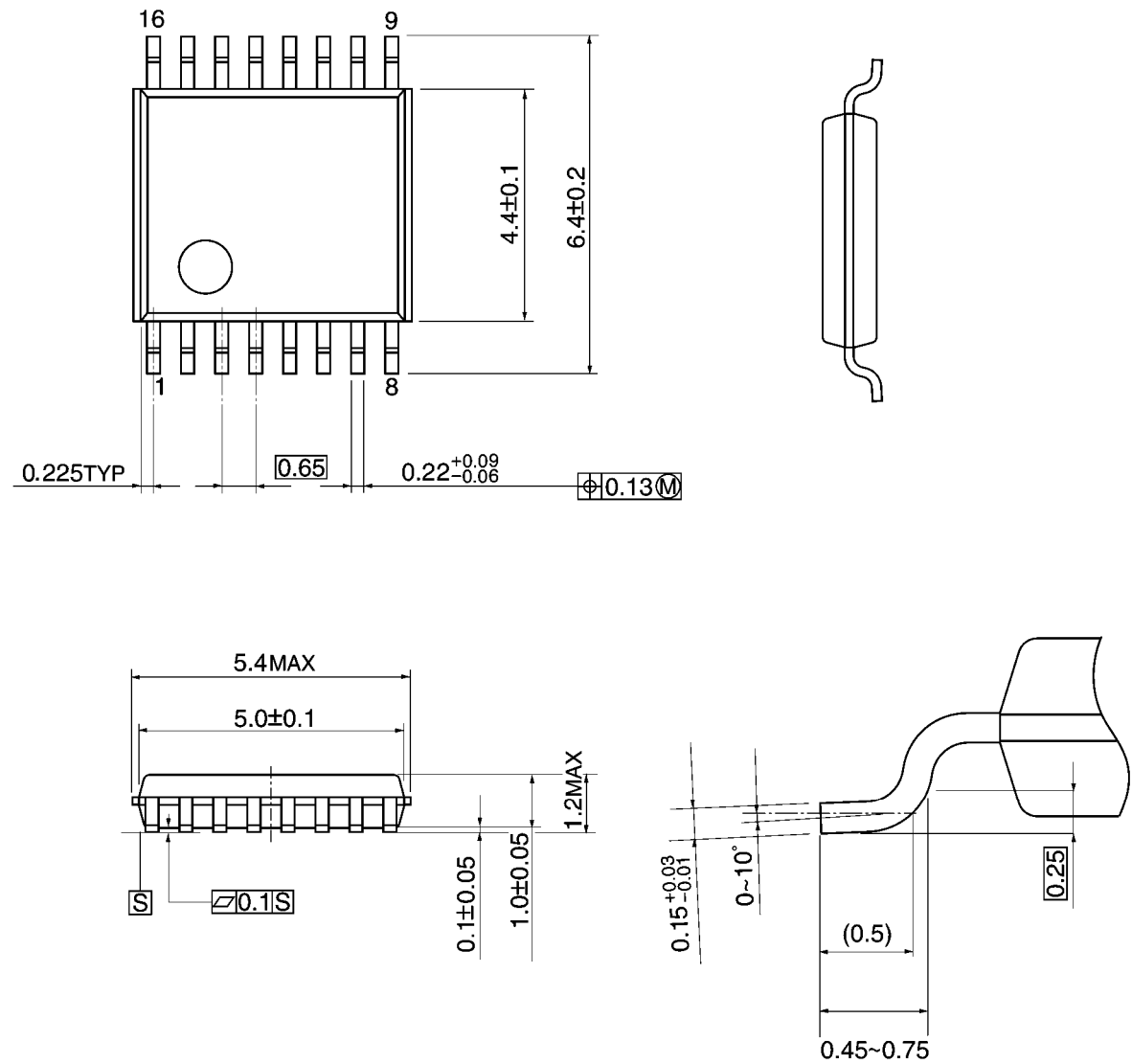
Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

Package Dimensions

TSSOP16-P-0044-0.65A

Unit: mm

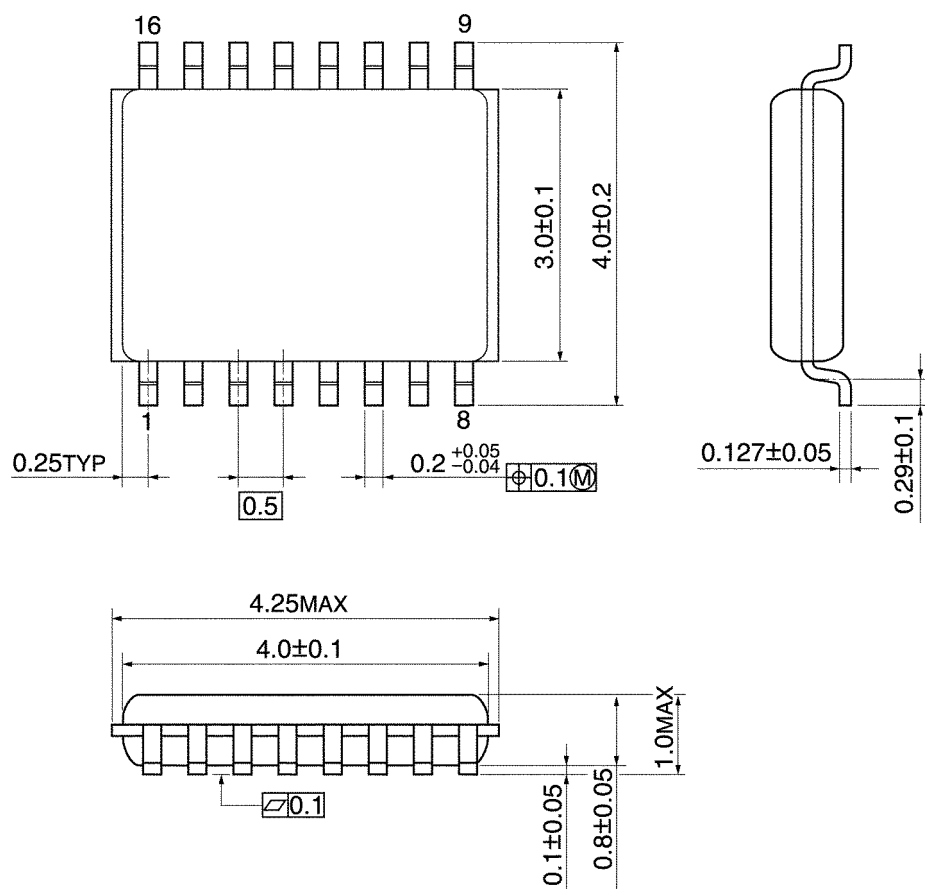


Weight: 0.06 g (typ.)

Package Dimensions

VSSOP16-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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