TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74AC166P,TC74AC166F,TC74AC166FN

8-Bit Shift Register (P-IN, S-OUT)

Note: xxxFN (JEDEC SOP) is not available in Japan.

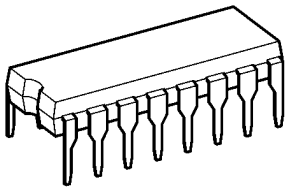
The TC74AC166 is an advanced high speed CMOS 8-BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of parallel-in or serial-in, serial-out 8-bit shift register with a gated clock input and an overriding clear input. The parallel-in or serial-in modes are controlled by the SHIFT/$\overline{\text{LOAD}}$ input. When the SHIFT/$\overline{\text{LOAD}}$ input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting on each clock pulse. When held low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. Clocking is accomplished on the low-to-high transition of the clock pulse. The CLOCK-INHIBIT input should be shifted high only while the CLOCK input is held high. A direct clear input overrides all other inputs, including the clock, and sets all the flip-flops to zero. Functional details are shown in the truth table and the timing charts.

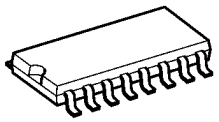
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TC74AC166P



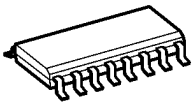
DIP16-P-300-2.54A

TC74AC166F



SOP16-P-300-1.27A

TC74AC166FN



SOL16-P-150-1.27

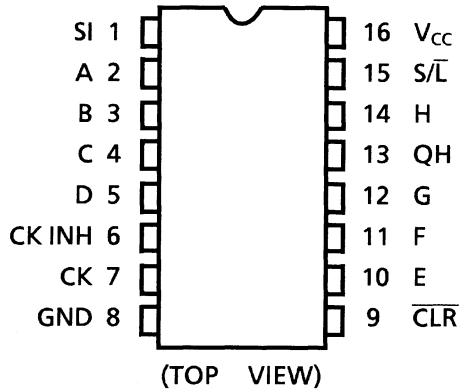
Weight

DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)
SOL16-P-150-1.27	: 0.13 g (typ.)

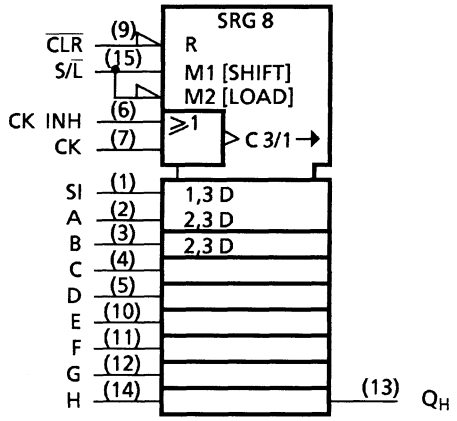
Features

- High speed: f_{max} = 170 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 8 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 24 mA (min)
  Capability of driving 50 Ω transmission lines.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 5.5 V
- Pin and function compatible with 74HC166

Pin Assignment



IEC Logic Symbol



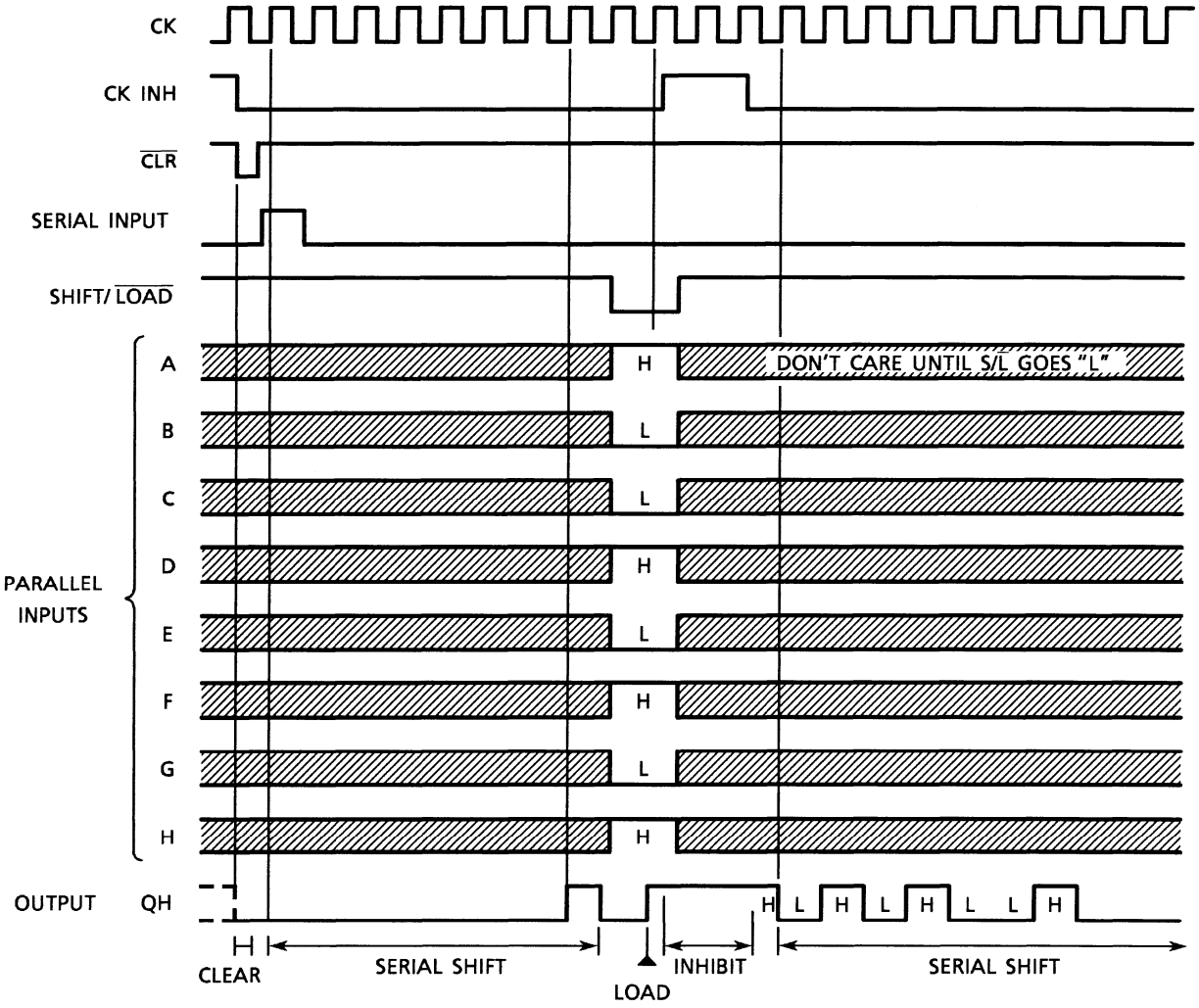
Truth Table

Inputs						Internal Output		Output
$\overline{CLR}$	SHIFT/ $\overline{LOAD}$	CK INH.	CK	SERIAL IN	PARALLEL A·····H	QA	QB	QH
L	X	X	X	X	X	L	L	L
H	X	X	↓	X	X	No Change		
H	L	L	↑	X	a·····h	a	b	h
H	H	L	↑	H	X	H	QAn	QGn
H	H	L	↑	L	X	L	QAn	QGn
H	X	H	X	X	X	No Change		

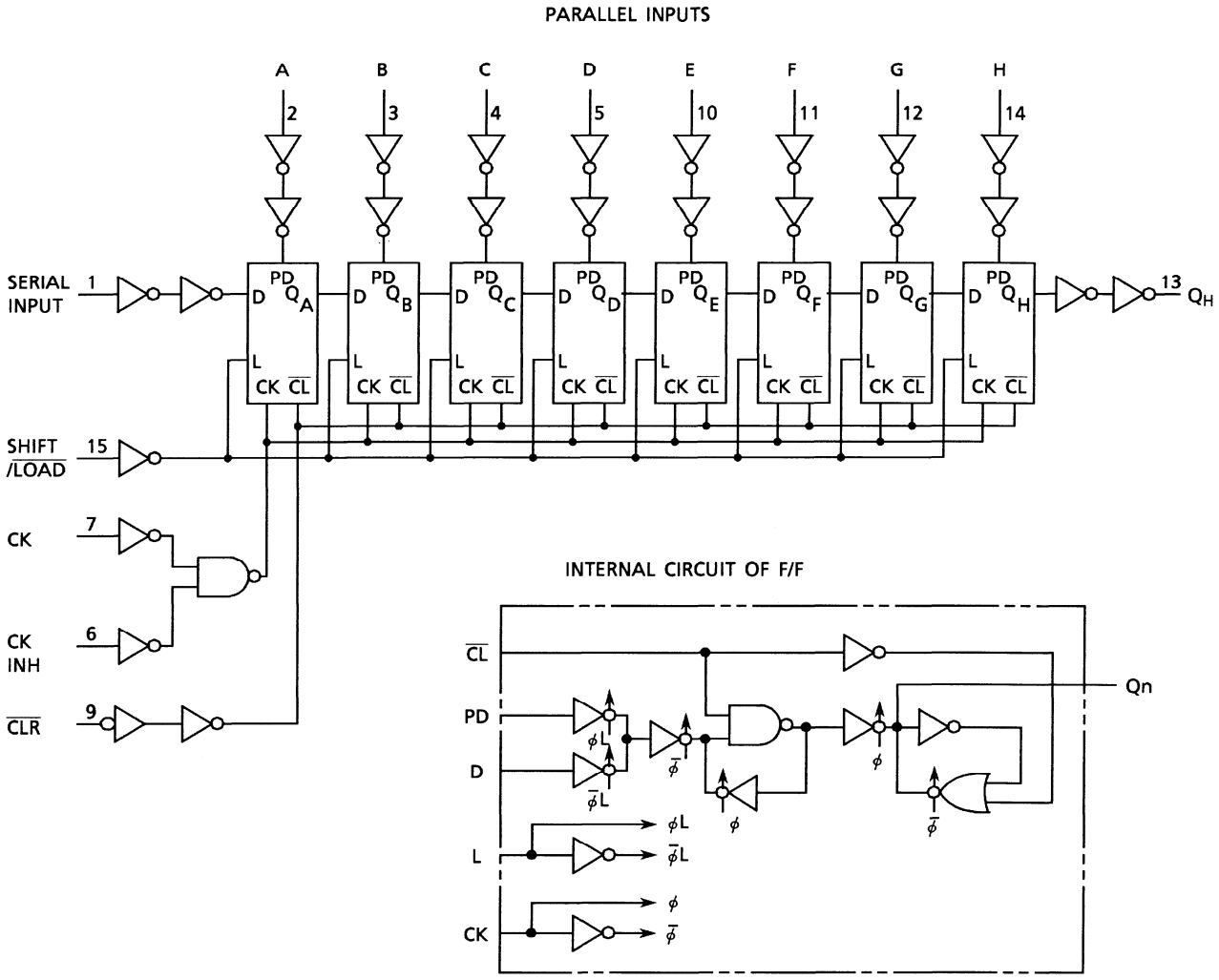
X: Don't care

a·····h: The level of steady state input voltage at inputs A through H respectively

Timing Chart



System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±50	mA
DC output current	I_{OUT}	±50	mA
DC V_{CC}/ground current	I_{CC}	±100	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C should be applied up to 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dV	0 to 100 (V_{CC} = 3.3 ± 0.3 V) 0 to 20 (V_{CC} = 5 ± 0.5 V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				3.0	2.10	—	—	2.10	—	
				5.5	3.85	—	—	3.85	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				3.0	—	—	0.90	—	0.90	
				5.5	—	—	1.65	—	1.65	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = −4 mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = −24 mA	4.5	3.94	—	—	3.80	—	
			I_{OH} = −75 mA (Note)	5.5	—	—	—	3.85	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 12 mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 24 mA	4.5	—	—	0.36	—	0.44	
			I_{OL} = 75 mA (Note)	5.5	—	—	—	—	1.65	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	8.0	—	80.0	μA

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

Timing Requirements (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C	Ta = −40 to 85°C	Unit
			V_{CC} (V)	Limit	Limit	
Minimum pulse width (CK)	$t_{W(H)}$ $t_{W(L)}$	—	3.3 ± 0.3 5.0 ± 0.5	7.0 5.0	7.0 5.0	ns
Minimum pulse width ($\overline{CLR}$)	$t_{W(L)}$	—	3.3 ± 0.3 5.0 ± 0.5	8.0 5.0	8.0 5.0	ns
Minimum set-up time (SI, PI)	t_s	—	3.3 ± 0.3 5.0 ± 0.5	8.0 4.0	8.0 4.0	ns
Minimum set-up time ($S/\overline{L}$)	t_s	—	3.3 ± 0.3 5.0 ± 0.5	7.0 4.0	7.0 4.0	ns
Minimum hold time (SI, PI)	t_h	—	3.3 ± 0.3 5.0 ± 0.5	0.5 0.5	0.5 0.5	ns
Minimum hold time ($S/\overline{L}$)	t_h	—	3.3 ± 0.3 5.0 ± 0.5	1.0 1.0	1.0 1.0	ns
Minimum removal time ($\overline{CLR}$)	t_{rem}	—	3.3 ± 0.3 5.0 ± 0.5	4.0 1.5	4.0 1.5	ns

AC Characteristics ($C_L = 50$ pF, $R_L = 500\ \Omega$, input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-QH)	t_{pLH} t_{pHL}	—	3.3 ± 0.3 5.0 ± 0.5	— —	9.4 6.6	16.1 10.0	1.0 1.0	18.3 11.4	ns
Propagation delay time ($\overline{CLR}$-QH)	t_{pHL}	—	3.3 ± 0.3 5.0 ± 0.5	— —	9.2 6.4	15.2 9.6	1.0 1.0	17.4 10.9	ns
Maximum clock frequency	f_{max}	—	3.3 ± 0.3 5.0 ± 0.5	55 90	105 150	— —	55 90	— —	MHz
Input capacitance	C_{IN}	—		—	5	10	—	10	pF
Power dissipation capacitance	C_{PD} (Note)	—		—	67	—	—	—	pF

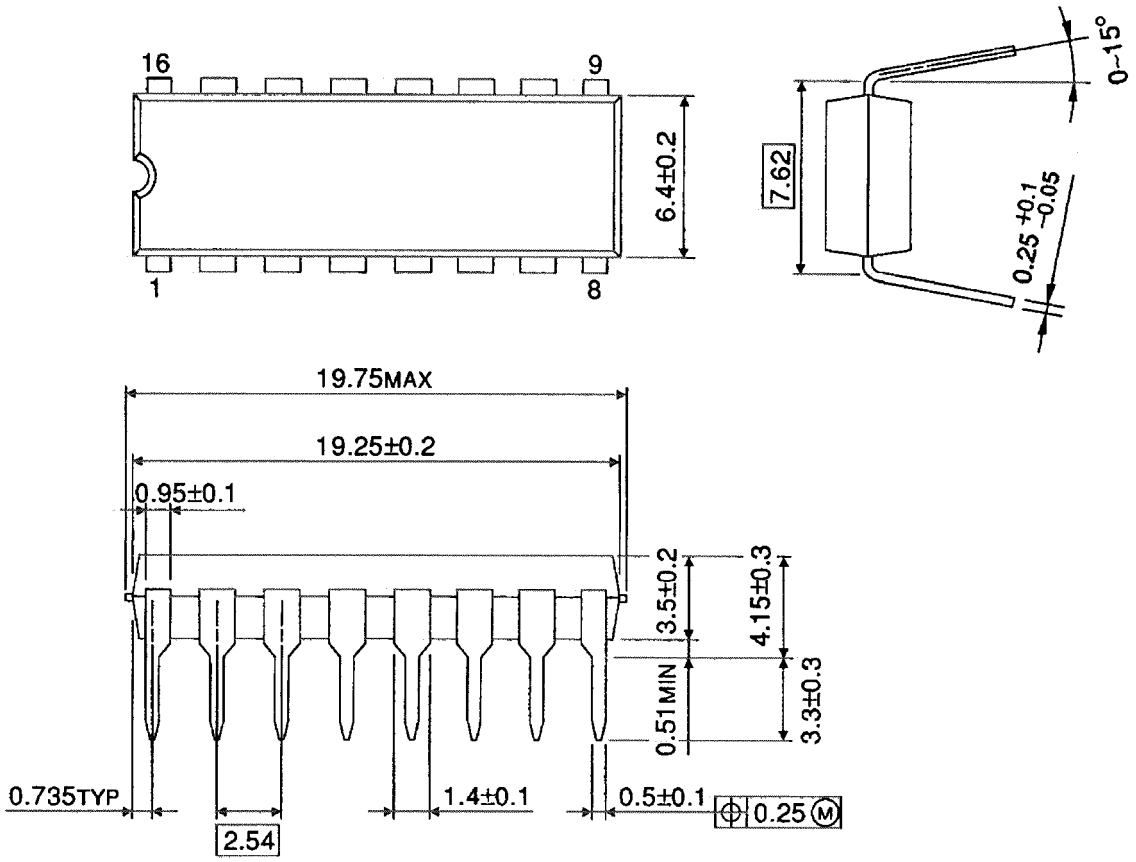
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}\ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions

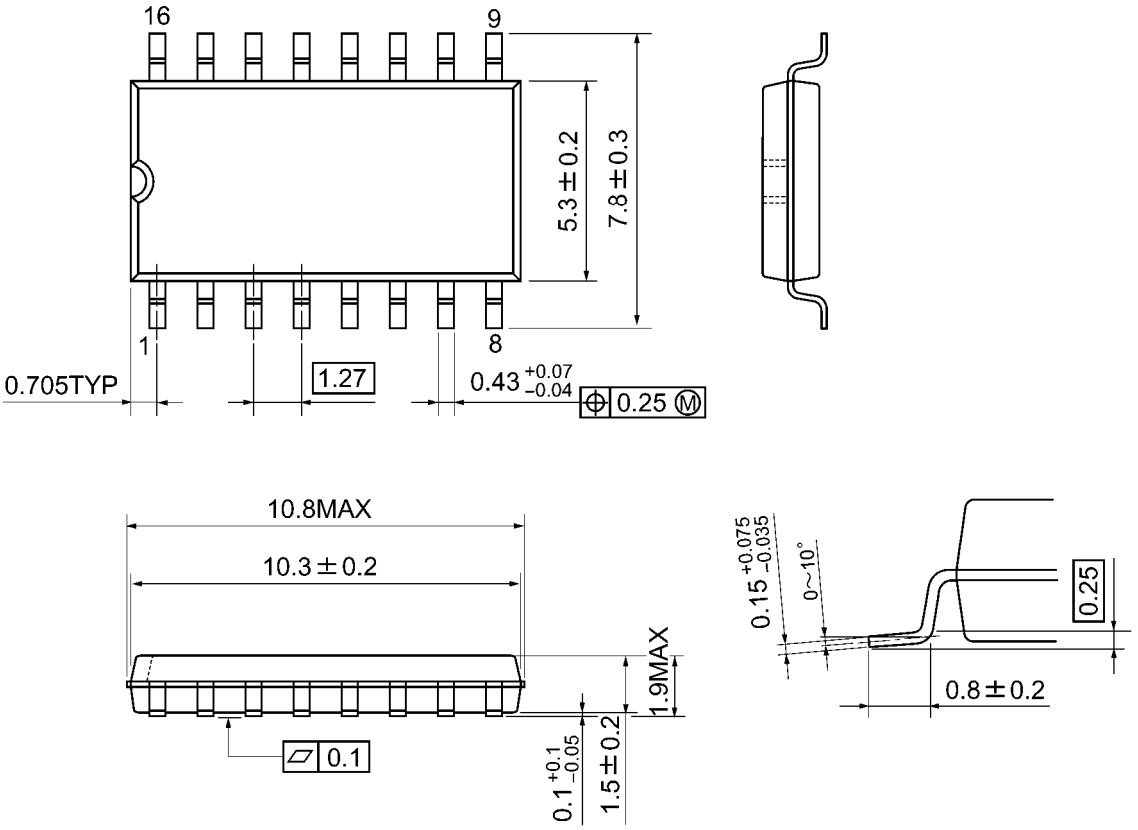
DIP16-P-300-2.54A Unit : mm



Weight: 1.00 g (typ.)

Package Dimensions

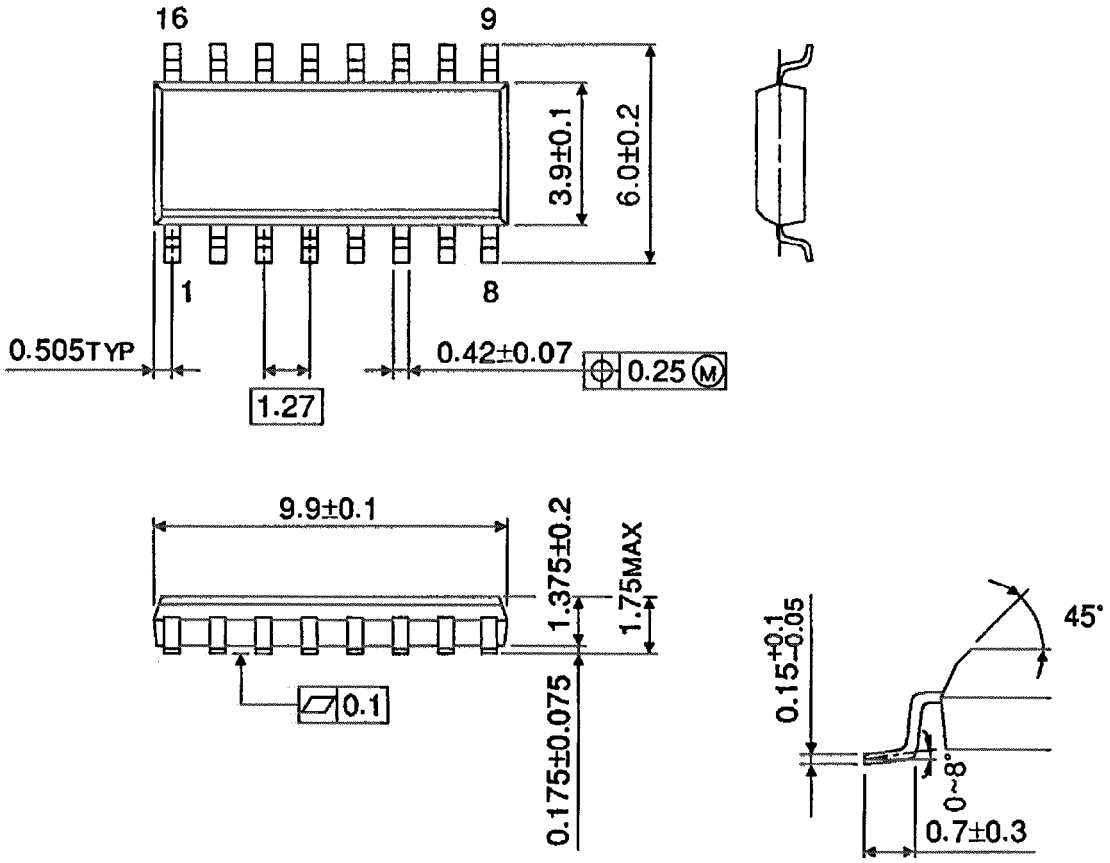
SOP16-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)

Package Dimensions (Note)

SOL16-P-150-1.27 Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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