ET(e)-XSC

XScale ET(e) Module
User's Manual
HW Revision
V4.0/5.0/6.0

Version 1.1

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MSC Vertriebs GmbH
Design Center Eching

Copyright Notice

☝ Important Information

This product is not an end user product. It was developed and manufactured for further processing by trained personnel.

EMC Rules

This unit has to be installed in a shielded housing. If not installed in a properly shielded enclosure, and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his or her own expense.

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1. General Information

1.1. Introduction

The ET(e)-XSC is a highly integrated Intel XScale PXA255 CPU Module. The module provides a subset of the functionality specified by the ETX standard as shown in the table below.

Feature	ETX-Standard	ET(e) XSC	Comment
PCI-Bus	yes	no	
ISA-Bus	yes	Subset	No DMA, several limitations
USB Host	yes	2 Ports	
USB Function (Client)	no	1 Port	
PS2 Mouse/Keyboard	yes	no	
Ethernet 10/100	yes	yes	
UART	yes	1x Full 1x Subset	RXD/TXD/RTS/CTS only
IrDA	yes	yes	
Audio	yes	yes	Stereo Line In/Out, Mic
I²/SMB	yes	yes	
LPT	yes	yes	
Floppy Controller	yes	no	
LCD Controller	yes	yes	TTL or LVDS available
2nd Graphics Controller	no	yes	Optional, dual display possible
CRT Controller (analog)	yes	optional	Only with 2nd controller.

Table 1: Functional range

In order to achieve full cost optimization most features can be adjusted to customer requirements:

Feature	Scalability
CPU	200 / 400 MHz
On-Board SDRAM	4 - 64 MByte
On-Board Linear or Boot Flash	1 - 64 MByte (depends on flash type)
USB Host	yes / no
Ethernet	yes / no
Audio	yes / no
LPT	yes / no
LCD	TTL / LVDS / no
2nd I²C data EEPROM	yes / no (1 – 16 kBit)
RTC	yes / no
2nd Graphics Controller	yes / no
2nd Compact Flash Socket	yes / no

Table 2: Features

2. Technical Information

2.1. Specifications

CPU:
Intel Embedded XScale PXA255 (mBGA, soldered)

Memory:
Up to 64 MByte on-board SDRAM (soldered)

Flash:
Up to 64 MByte on-board flash (soldered)

ISA-Bus:
8/16 bit, no DMA, several limitation
ET(e) connector X2

PCI-Bus:
Not available
ET(e) connector X1

LCD / Video:
Flat Panel Interface (TTL or LVDS, 18 bit)
2nd Flat Panel Interface (TTL, 18 bit, optional)
CRT out (optional)

Ethernet :

SMSC LAN91C111 or LAN91C113
10/100 MBit Ethernet controller

Audio:
National LM4548 or compatible: AC97 Codec
Stereo Line IN, Stereo Line OUT, Mono Microphone IN

USB:
integrated in PXA255 (Port 3)
1 USB 1.1 client / device (1.5MBit/s or 12MBit/s half duplex)
Cypress CY7C67200 (Port 1 + 2)
Dual USB 2.0 compatible host controller (1.5MBit/s or 12MBit/s)

Compact Flash:
integrated in PXA255
2 Ports/Slots

Serial:
integrated in PXA255
UART1: Full functional UART (TTL, 230.4 kbps)
UART2: Bluetooth or normal function UART (TTL, 921.6 kbps)
IrDA (TTL, 4 Mbps)

Parallel:
EXAR ST78C36
1 Parallel Port (Centronics, IBM PS2, EPP, ECP)

Keyboard, Mouse:
Mouse or Keyboard via USB available (no PS2)

Real time Clock (external battery required):
Seiko-Epson RTC-8563 or RTC-8564

Watchdog
integrated in PXA255

I²C Bus:
integrated in PXA255
I²C1: Standard I²C Bus (100kbps or 400kbps)
I²C2: Software emulated Bus

EEPROM:

One universal EEPROM for board specific information at I²C Bus 1 (UspEPC)
One universal EEPROM for vendor specific information at I²C Bus 2 (optional)

Power supply:

Supply Voltage	Tolerance
+5V	±5%

Table 3: Supply voltage

Supply current:

Supply voltage	Supply current	CPU status
+5V	0,40A	PXA255 @ 200MHz
+5V	0,43A	PXA255 @ 400MHz
+5V	0,34A	PXA255 @ Sleep Mode

Table 4: Supply current

Note: The values are measured with a fully equipped module. The current consumption varies in dependence of the equipped options on the board.

Environment:

Temperature	Module status
0 .. + 70°C	operating
- 40 .. + 85°C	operating (extended temperature)
- 40 .. + 85°C	non operating (storage)

Table 5: Temperature

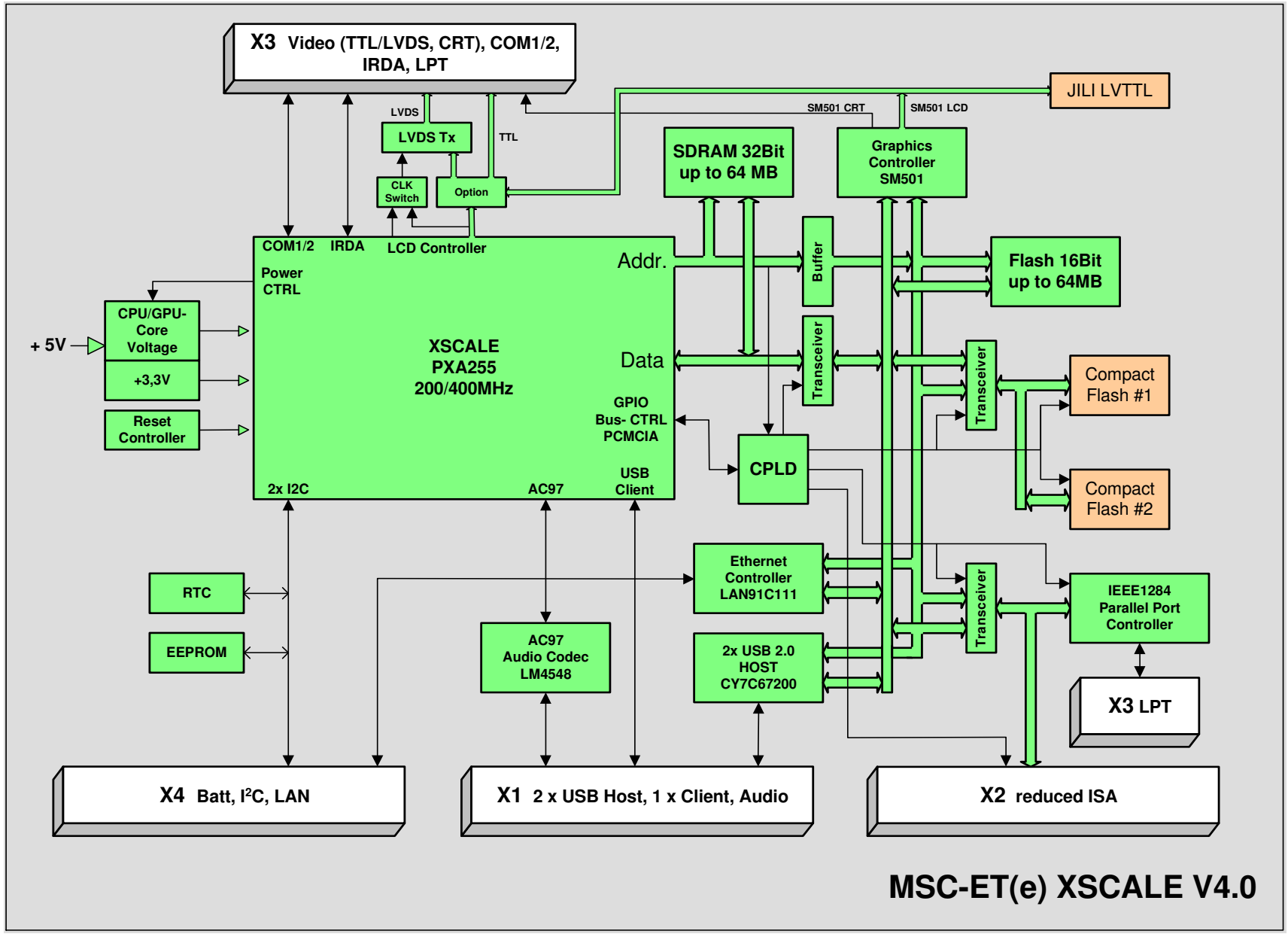
Humidity (rel.)	Module status
10 .. 95%	operating
5 .. 95%	non operating (storage)

Table 6: Humidity

Dimensions:

95 x 114 x 12 mm

2.2. Block Diagram



2.3. Watchdog

The XScale Processor has a watchdog function implemented using a timer / counter register set. It is assumed that watchdog resets are generated only when software is not executing properly and has potentially destroyed data. During a watchdog reset, all units are reset except of the Clocks and Power Manager.
OS-timer 3 is used as watchdog timer. The watchdog can be enabled, disabled and configured via software.
If the watchdog is enabled a counter is started which creates a reset if it is not retriggered within a programmable time window. The programmable time ranges up to about 19 minutes.

Watchdog Control Registers:

Register	Bit(s)	Function
OWER	WME	0 = Watchdog is disabled (default) 1 = Watchdog is enabled
OSMR3	OSMV[31:0]	OS Timer Match Value. The value compared against the OS timer counter.

Table 7: Watchdog registers

2.4. Interrupts, DMA channels, memory map

Interrupts

GPIO	used for	comment
0	PX_POWER#	Power button, wake up IRQ / power down
1	RTC_IRQ#	RTC wake up
2	GPU_IRQ	Graphics controller IRQ
3	USB_OVCR#	USB Host over current IRQ
4	USBH1_IRQ	USB Host IRQ
5	CF1_CD#	Compact Flash socket 1 card detect IRQ
6	CF2_CD#	Compact Flash socket 2 card detect IRQ
8	ISA_IRQ	ISA IRQ (1)
9	CF2_IRQ#	Compact Flash socket 2 IRQ
10	CF1_IRQ#	Compact Flash socket 1 IRQ
11	PX_LPT_IRQ7	LPT IRQ
12	LAN_IRQ	LAN IRQ

Table 8: Interrupts

Note: (1) ISA IRQ 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, 15 are concatenated to this interrupt

DMA channels

DMA	used for	comment
0	--	Not implemented
1	--	Not implemented

Table 9: DMA channels

Memory map

CS#	Device	PXA memory base address	Comment
0	Linear Flash	0x0000 0000	256kByte to 64MByte
1	USB-Host	0x0400 0000	A1, A2 used
2	ISA-Subset	0x0800 0000	See 2.5 ISA Bus
3	LPT-Controller	0x0C00 0000	A0, A1, A2, A10 used
4	LAN-Controller	0x1000 0000	A1, A2, A3 used
5	Ext. Graphics	0x1400 0000	A2 - A25 used

Table 10: Memory map

2.5. ISA Bus

2.5.1. Signal description

The ET(e) XScale Module provides only a subset of the standard ISA bus. The timing equals the ISA specification. DMA is not available.

ISA Signal	Comment
AEN	Address Enable, not used, Pull down
BCLK#	Bus clock, 8,3 MHz, generated by hardware using SDRAM Memory Clock
BALE	Bus Address Latch Enable, generated by hardware
SA0 … SA19	Small address, output together with LAx
LA17 … LA23	Large address, output together with SAx
SD0 … SD15	16-bit data
SBHE#	System Bus High Enable generated by hardware
IOCHRDY	I/O Channel Ready, used to generate WAIT#/READY for the PXA255
IOW#, IOR#,MEMW#, MEMR#,SMEMW#, SMEMR#	Read- and write-signals, generated from bus control and address signals
RESET	Connected to system reset
MEMCS16#	Memory Chip Select 16 Bit, not used, Pull up
IOCS16#	I/O Chip Select 16 Bit, not used, Pull up
IOCHCK#	I/O Channel Check, not used, Pull up
DRQ0 … DRQ7 DACK0# … DACK7#	DMA-Request, DMA Acknowledge, not used, DRQ0 … DRQ7 Pull down
TC	Terminal Count, not used, Pull down
MASTER#	Bus Master, not used, Pull up
REFSH#	Refresh, not used, Pull up
IRQ3 … IRQ7, IRQ9 … IRQ12, IRQ14, IRQ15	Interrupt Request, IRQ 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, 15 are combined (or'ed) by hardware, all IRQs Pull down; Note: IRQ2 (ISA Documentation) is labeled IRQ9 in the ETX documentation from Jumptec/Kontron
OSC	Oscillator 14,31818 MHz, not used, Pull down
NOWS#	No Wait States, not used, Pull up

Table 11: ISA signals

2.5.2. ISA address space

The ISA address space is used in I/O or memory access mode. With X86-compatible processors the distinction between the I/O and the memory domain is implemented by using different opcodes. The XScale/ARM architecture however does not support this architecture. In order to differentiate between the I/O and the memory mode accesses on the XScale the I/O and the memory domain have simply been mapped into different memory areas.
A25 of the PXA255 is used to decode I/O and memory accesses. A25 = low initiates an ISA I/O cycle, while A25 = high selects an ISA memory cycle.

PXA Memory Address	Physical Address		ISA-Control-Signals		Comment
	PXA (A25, A23 – A0)	ISA (A23 – A0)			
0x0800 0000 0x08FF FFFF	0x0000 0000 0x00FF FFFF	0x0000 0000 0x00FF FFFF	IOR# IOW#		I/O-Space A25 = 0
0x0A00 0000 0x0A0F FFFF	0x0200 0000 0x020F FFFF	0x0000 0000 0x000F FFFF	SMEMR# SMEMW#	MEMR# MEMW#	Memory-Space A25 = 1
0x0A10 0000 0x0AFF FFFF	0x0210 0000 0x02FF FFFF	0x0010 0000 0x00FF FFFF			

Table 12: ISA address map

2.6. I²C Busses

The Inter-Integrated Circuit (I²C) bus interface unit of the PXA255 processor can serve only as a master for the I²C bus. The I²C bus is a serial bus developed by Philips Corporation consisting of a two-pin interface. SDA is the serial data line and SCL is the serial clock line.

2.6.1. PXA integrated I²C bus (primary I²C bus)

The integrated I²C bus is controlled by a set of dedicated registers. For further information on this registers please refer to the PXA 255 documentation available on the Intel website.
The I²C unit supports a fast mode operation at 400 kbits/sec and a standard mode at 100 kbits/sec.

This I²C bus is connected to the RTC, the ID-EEPROM and the external I²C bus provided at ET(e) connector X4 SCL on pin X4.16, SDA on pin X4.22.

The ID-EEPROM connected to this bus contains the board specific data of the module.

The module is regularly equipped with a 2kBit EEPROM from Atmel (Type 24C02). As an option the size of the EEPROM can be increased up to 16kBit. If the standard type is not used special consideration to the address space must be taken. See capture 2.6.3.

Addressing of the ID-EEPROM.

Standard device	Address	Address (available)
ID-EEPROM (UspEPC)	1010_000x (0xA0)	only 0xA0

Table 13: ID-EEPROM

2.6.2. Software emulated I²C bus (secondary I²C bus)

The secondary I²C bus is a SW emulated I²C bus using standard GPIO-Pins of the PXA255. SCL is available on GPIO17 and SDA is available on GPIO16. The I²C bus is connected to the optional on-board user EEPROM, the JILI and the SMB I²C bus. The JILI and the SMB I²C bus are available on connector X3 and X4 using the following pins:

JILI: SCL on pin X3.43, SDA on pin X3.41
SMB: SCL on pin X4.23, SDA on pin X4.24

The addressing of the optional on-board user EEPROM depends on the size of the EEPROM. See capture 2.6.3.

Optional device	Address (default)	Addresses available
User EEPROM	1010_000x (0xA0)	0xA0 to 0xAE

Table 14: Emulated I2C

2.6.3. I²C Device Address Map (on-board devices)

ETX I2C Bus	UspEpc Bus ID	Address	Device
I2CLK X4.16 / I2DAT X4.22	1	0xA2	Seiko Epson RTC8563
I2CLK X4.16 / I2DAT X4.22	1	0xA0	24C02 UspEpc EEPROM
SMBCLK X4.23 SMBDATA X4.24 JILI_CLK X3.43 JILI_DAT X3.41	0/2 (*)	0xAx	Optional 24C02 EEPROM

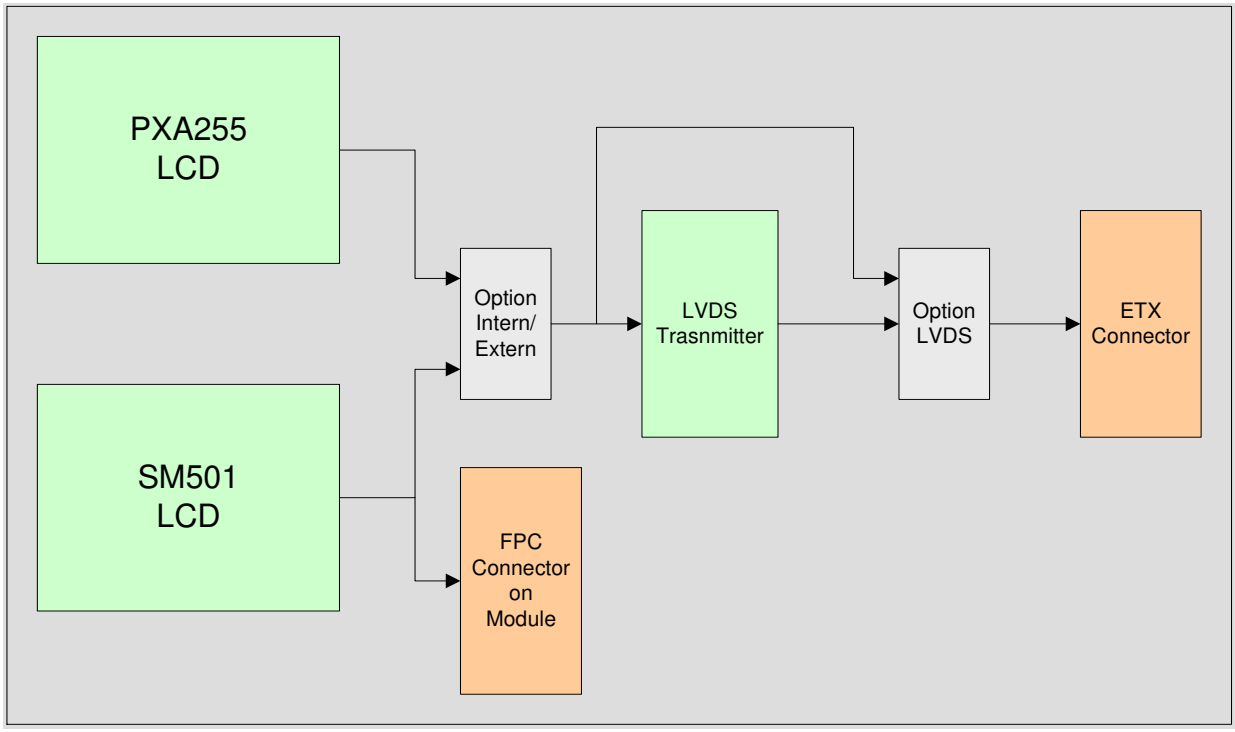
(*) The SMB and the JILI-Bus are tied together

Table 15: I²C addressing

2.7. Graphics Subsystem

The ET(e) XScale Module can be equipped with a 2nd graphics controller. The first is always present as it is integrated in the PXA-255 CPU. The other one is an optional SiliconMotion SM501 discrete graphics controller with 8 MByte integrated frame buffer memory operating on the 32-bit wide bus. The integrated graphics controller has got the disadvantage that it uses the global program memory (SDRAM) as frame buffer (UMA) and it hasn't got significant hardware acceleration. The additional bus traffic which is generated by the continuous DMA accesses from the LCD controller limits the usable display resolutions to max. 640x480 pixel @ 16bpp and of course reduces total system performance. With the SM501 graphics controller much higher resolutions up to 1024x768 pixel can be used with little impact on system performance and graphics speed due to hardware acceleration.

Both graphics controllers can even be used in parallel, because the LCD interface of the SM501 is always accessible directly via an additional FPC-Connector on the module, while the integrated graphics controller uses the ETX connectors. It is also possible to route the signals of the external graphics controller to the ETX connectors. The PXA-255 integrated graphics controller is not used in this case. For more flexibility the signals are routed to the ETX connector directly with LVTTL level or through an LVDS converter.



2.7.1. Onboard FPC-Connector

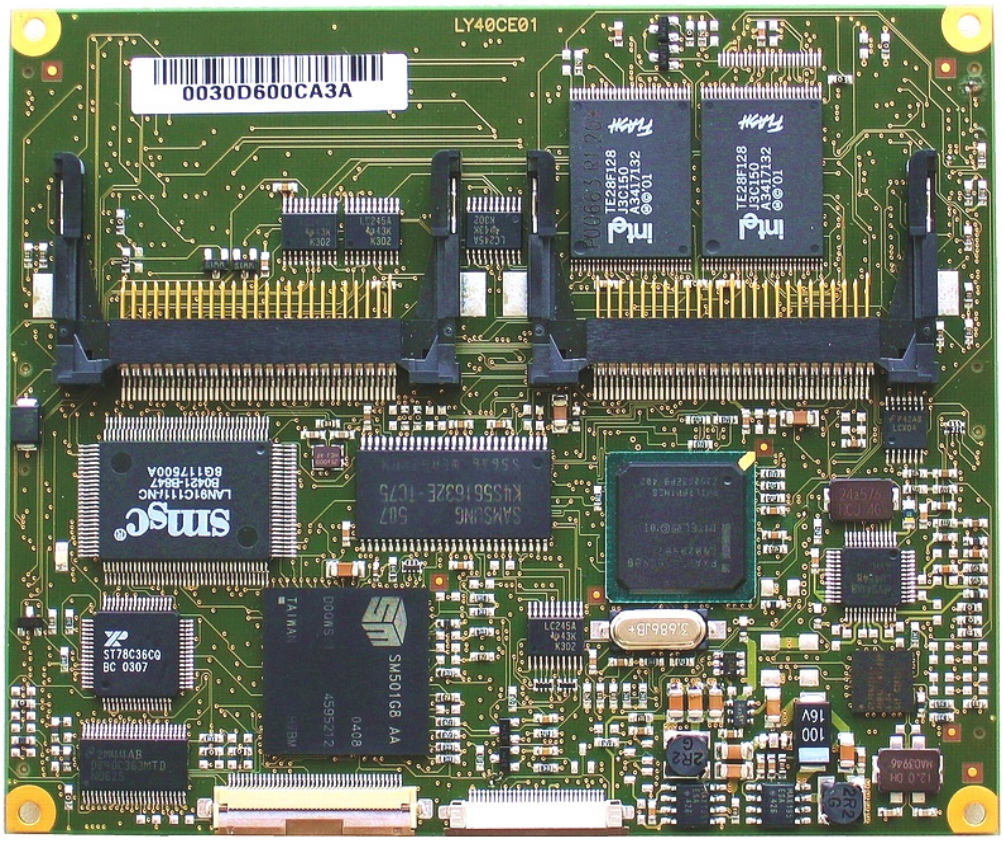
Pin	Signal	Description	I/O	Note
1	VSYNC	Vertical Sync	O	VSYNC, LVTTL
2	RED0	RED LSB	O	LVTTL
3	RED1	RED	O	LVTTL
4	DIGON	Display Power ON	O	LVTTL
5	RED2	RED	O	LVTTL
6	RED3	RED	O	LVTTL
7	HSYNC	Horizontal Sync	O	HSYNC, LVTTL
8	RED4	RED	O	LVTTL
9	RED5	RED MSB	O	LVTTL
10	GND	Power Ground	O	display power supply
11	GREEN0	GREEN LSB	O	LVTTL
12	GREEN1	GREEN	O	LVTTL
13	GND	Power Ground	O	display power supply
14	GREEN2	GREEN	O	LVTTL
15	GREEN3	GREEN	O	LVTTL
16	JILI_I2C_DAT	I2C data: Read data from Display	O	LVTTL
17	GREEN4	GREEN	O	LVTTL
18	GREEN5	GREEN MSB	O	LVTTL
19	JILI_I2C_CLK	I2C clock: Read data from Display	O	LVTTL
20	BLUE0	BLUE	O	LVTTL
21	BLUE1	BLUE	O	LVTTL
22	n.c.			
23	BLUE2	BLUE	O	LVTTL
24	BLUE3	BLUE	O	LVTTL
25	GND	Power Ground	O	display power supply
26	BLUE4	BLUE	O	LVTTL
27	BLUE5	BLUE MSB	O	LVTTL
28	GND	Power Ground	O	display power supply
29	SHIFT_CLK	Shift Clock	O	SHFCLK, LVTTL
30	DATA_ENABLE	Data Enable	O	EN, LVTTL
31	VCC5V0	Power Supply +5V, +/-5%	O	display power supply
32	VCC5V0	Power Supply +5V, +/-5%	O	display power supply
33	VCC5V0	Power Supply +5V, +/-5%	O	display power supply
34	VCC5V0	Power Supply +5V, +/-5%	O	display power supply
35	BLON#	Display Backlight ON	O	LVTTL
36	GND	Power Ground	O	display power supply
37	GND	Power Ground	O	display power supply
38	n.c.			
39	n.c.			
40	n.c.			

Table 16: Debug connector Note: n.c. : Not connected

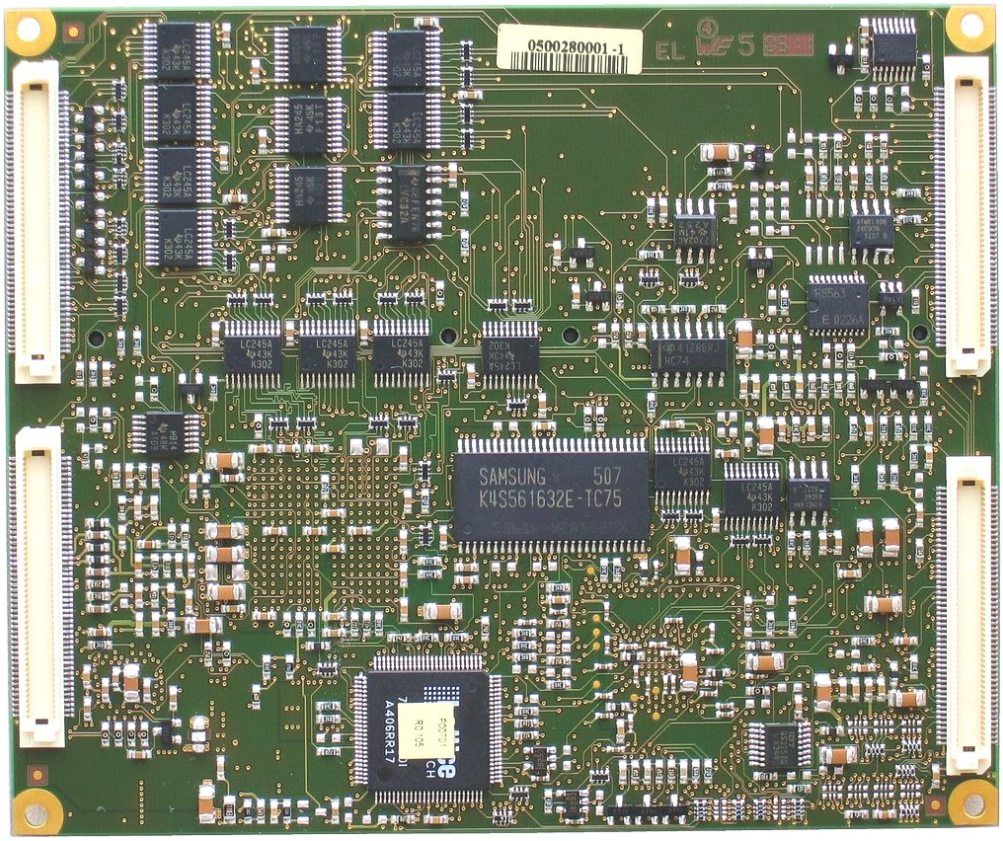
3. Mechanical Specification

3.1. Pictures

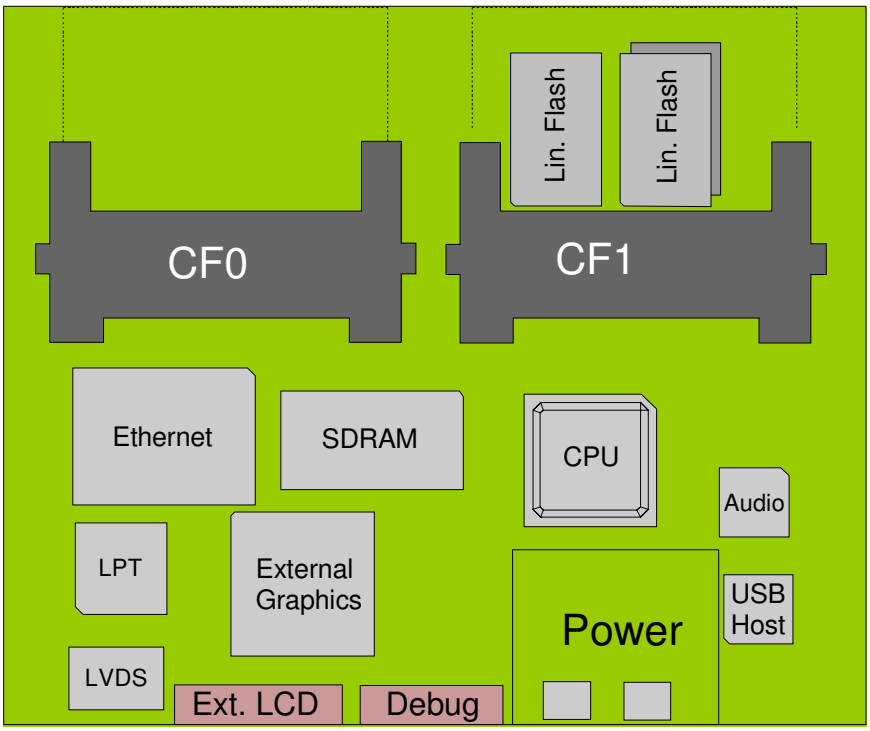
3.1.1. Top view:



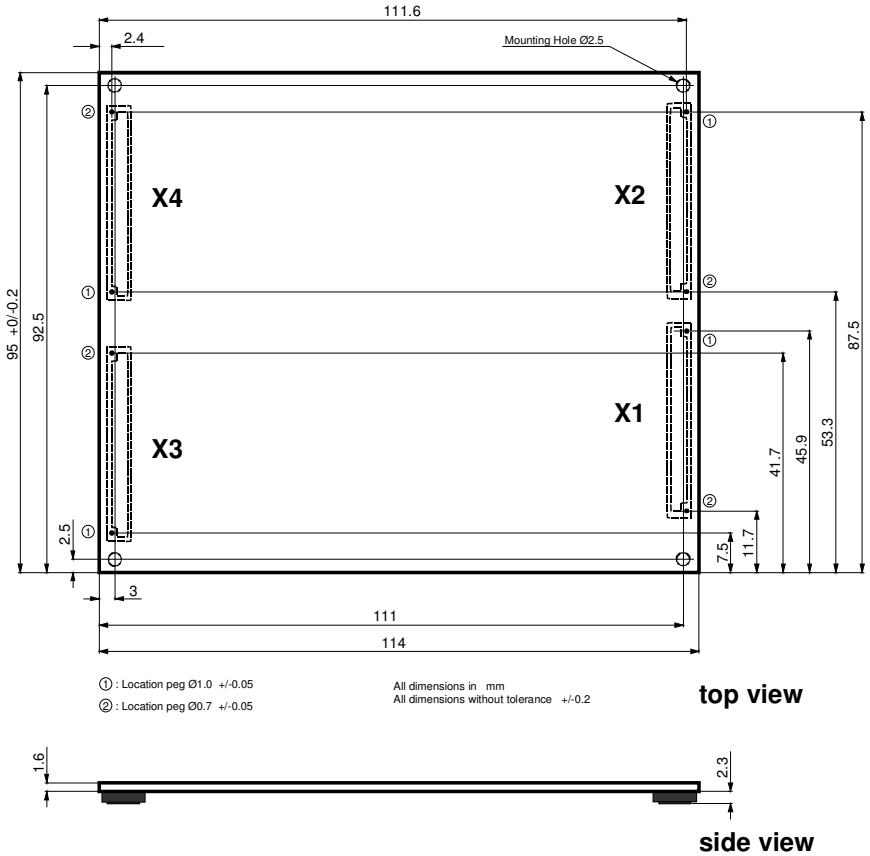
3.1.2. Bottom view:



3.2. Board overview (Rev. V4.0)



3.3. Mechanical drawing



Heat spreader options for ET(e)-XSC:

No fan, heat spreader or heat sink is required.

4. ET(e) Connectors

4.1. Connector X1 (PCI, USB, Audio)

Pin	Signal	Function	Pin	Signal	Function
1	GND		2	GND	
3	PCICLK3	Pull up	4	PCICLK4	Pull up
5	GND		6	GND	
7	PCICLK1	Pull up	8	PCICLK2	Pull up
9	REQ3#	n.c.	10	GNT3#	n.c.
11	GNT2#	n.c.	12	3.3V	
13	REQ2#	n.c.	14	GNT1#	n.c.
15	REQ1#	n.c.	16	3.3V	
17	GNT0#	n.c.	18	Res.	n.c.
19	VCC		20	VCC	
21	SERIRQ	n.c.	22	REQ0#	n.c.
23	AD0	n.c.	24	3.3V	
25	AD1	n.c.	26	AD2	n.c.
27	AD4	n.c.	28	AD3	n.c.
29	AD6	n.c.	30	AD5	n.c.
31	CBE0#	n.c.	32	AD7	n.c.
33	AD8	n.c.	34	AD9	n.c.
35	GND		36	GND	
37	AD10	n.c.	38	AUXAL	Audio
39	AD11	n.c.	40	MIC	Audio
41	AD12	n.c.	42	AUXAR	Audio
43	AD13	n.c.	44	ASVCC	Audio
45	AD14	n.c.	46	SNDL	Audio
47	AD15	n.c.	48	ASGND	Audio
49	CBE1#	n.c.	50	SNDR	Audio
51	VCC		52	VCC	
53	PAR	n.c.	54	SERR#	n.c.
55	GPERR#	n.c.	56	Res.	n.c.
57	PME#	n.c.	58	USB2#	USB Client N
59	LOCK#	n.c.	60	DEVSEL#	n.c.
61	TRDY#	n.c.	62	USB3#	n.c.
63	IRDY#	n.c.	64	STOP#	n.c.
65	FRAME#	n.c.	66	USB2	USB Client P
67	GND		68	GND	
69	AD16	n.c.	70	CBE2#	n.c.
71	AD17	n.c.	72	USB3	n.c.
73	AD19	n.c.	74	AD18	n.c.
75	AD20	n.c.	76	USB0#	USB Host Port0 N
77	AD22	n.c.	78	AD21	n.c.
79	AD23	n.c.	80	USB1#	USB Host Port1 N
81	AD24	n.c.	82	CBE3#	n.c.

Pin	Signal	Function	Pin	Signal	Function
83	VCC		84	VCC	
85	AD25	n.c.	86	AD26	n.c.
87	AD28	n.c.	88	USB0	USB Host Port0 P
89	AD27	n.c.	90	AD29	n.c.
91	AD30	n.c.	92	USB1	USB Host Port1 P
93	PCIRST#	n.c.	94	AD31	n.c.
95	INTC#	n.c.	96	INTD#	n.c.
97	INTA#	n.c.	98	INTB#	n.c.
99	GND		100	GND	

Table 17: ET(e) ´Connector X1

Note: n.c. = not connected

Signal	Description	I/O	Note
VCC	Power Supply +5V, +/-5%	I	external supply
GND	Power Ground	I	external supply
3V3	Power Supply +3.3V	O	Do not use as power-supply
RESERVED	Not connected	n.a.	Do not connect

Table 18: X1 Power

Note: n.a. = not available

Signal	Description of PCI Bus Signals	I/O	Note
PCICLK1..4.	PCI clock output	O	Pull up
REQ0..3#	PCI bus request	n.c.	n.a.
GNT0..3#	PCI bus grant	n.c.	n.a.
AD0..31	PCI Address-/ Data bus	n.c.	n.a.
CBE0..3#	PCI bus command / byte enables	n.c.	n.a.
PAR	PCI bus parity	n.c.	n.a.
SERR#	PCI bus system error	n.c.	n.a.
GPERR#	PCI bus grant parity error	n.c.	n.a.
PME#	PCI bus power management event	n.c.	n.a.
LOCK#	PCI bus lock	n.c.	n.a.
DEVSEL#	PCI bus device select	n.c.	n.a.
TRDY#	PCI bus target ready	n.c.	n.a.
IRDY#	PCI bus initiator ready	n.c.	n.a.
STOP#	PCI bus stop	n.c.	n.a.
FRAME#	PCI bus frame	n.c.	n.a.
PCIRST#	PCI bus reset	n.c.	n.a.
INTA#	PCI bus interrupt A	n.c.	n.a.
INTB#	PCI bus interrupt B	n.c.	n.a.
INTC#	PCI bus interrupt C	n.c.	n.a.
INTD#	PCI bus interrupt D	n.c.	n.a.
SERIRQ	Serial interrupt request	n.c.	n.a.

Table 19: PCI bus

Note: n.a. = not available

n.c. = not connected

Signal	Description of USB Signals	I/O	Note
USB0, USB0#	USB Port 0	I/O	Host 1 / USB Controller
USB1, USB1#	USB Port 1	I/O	Host 2 / USB Controller
USB2, USB2#	USB Port 2	I/O	Client / device / XScale
USB3, USB3#	USB Port 3	n.c.	n.a.

Table 20: USB

Signal	Description of Audio Signals	I/O	Note
SNDL	Line-Level stereo output left	O	
SNDR	Line-Level stereo output right	O	
AUXAL	Auxiliary Line-Level input left	I	max. 1Vrms
AUXAR	Auxiliary Line-Level input right	I	max. 1Vrms
MIC	Microphone input	I	max. 1Vrms
ASGND	Analog ground of audio controller		
ASVCC	Analog supply of audio controller		5.0V

Table 21: Audio

4.2. Connector X2 (ISA)

Pin	Signal	Function	Pin	Signal	Function
1	GND		2	GND	
3	SD14	ISA-Bus	4	SD15	ISA-Bus
5	SD13	ISA-Bus	6	MASTER#	Pull up / not used
7	SD12	ISA-Bus	8	DREQ7	Pull down / not used
9	SD11	ISA-Bus	10	DACK7#	Pull up / not used
11	SD10	ISA-Bus	12	DREQ6	Pull down / not used
13	SD9	ISA-Bus	14	DACK6#	Pull up / not used
15	SD8	ISA-Bus	16	DREQ5	Pull down / not used
17	MEMW#	ISA-Bus	18	DACK5#	Pull up / not used
19	MEMR#	ISA-Bus	20	DREQ0	Pull down / not used
21	LA17	ISA-Bus	22	DACK0#	Pull up / not used
23	LA18	ISA-Bus	24	IRQ14	ISA-Bus
25	LA19	ISA-Bus	26	IRQ15	ISA-Bus
27	LA20	ISA-Bus	28	IRQ12	ISA-Bus
29	LA21	ISA-Bus	30	IRQ11	ISA-Bus
31	LA22	ISA-Bus	32	IRQ10	ISA-Bus
33	LA23	ISA-Bus	34	IO16#	Pull up / not used
35	GND		36	GND	
37	SBHE#	ISA-Bus	38	M16#	Pull up / not used
39	SA0	ISA-Bus	40	OSC	Pull down / not used
41	SA1	ISA-Bus	42	BALE	ISA-Bus
43	SA2	ISA-Bus	44	TC	Pull down / not used
45	SA3	ISA-Bus	46	DACK2#	Pull up / not used
47	SA4	ISA-Bus	48	IRQ3	ISA-Bus
49	SA5	ISA-Bus	50	IRQ4	ISA-Bus
51	VCC		52	VCC	
53	SA6	ISA-Bus	54	IRQ5	ISA-Bus
55	SA7	ISA-Bus	56	IRQ6	ISA-Bus
57	SA8	ISA-Bus	58	IRQ7	ISA-Bus
59	SA9	ISA-Bus	60	SYSCLK	ISA-Bus
61	SA10	ISA-Bus	62	REFSH#	Pull up / not used
63	SA11	ISA-Bus	64	DREQ1	Pull down / not used
65	SA12	ISA-Bus	66	DACK1#	Pull up / not used
67	GND		68	GND	
69	SA13	ISA-Bus	70	DREQ3	Pull down / not used
71	SA14	ISA-Bus	72	DACK3#	Pull up / not used
73	SA15	ISA-Bus	74	IOR#	ISA-Bus
75	SA16	ISA-Bus	76	IOW#	ISA-Bus
77	SA18	ISA-Bus	78	SA17	ISA-Bus
79	SA19	ISA-Bus	80	SMEMR#	ISA-Bus
81	IOCHRDY	ISA-Bus	82	AEN	Pull down / not used
83	VCC		84	VCC	

85	SD0	ISA-Bus	86	SMEMW#	ISA-Bus
87	SD2	ISA-Bus	88	SD1	ISA-Bus
89	SD3	ISA-Bus	90	NOWS#	Pull up / not used
91	DREQ2	Pull down / not used	92	SD4	ISA-Bus
93	SD5	ISA-Bus	94	IRQ9	ISA-Bus
95	SD6	ISA-Bus	96	SD7	ISA-Bus
97	IOCHK#	Pull up / not used	98	RSTDRV	ISA-Bus
99	GND		100	GND	

Table 22: ET(e) connector X2

Signal	Description	I/O	Note
VCC	Power Supply +5V, +/-5%	I	external supply
GND	Power Ground	I	external supply

Table 23: X2 Power

Signal	Description of ISA Bus Signals	I/O	Note
SD0..15	ISA Data bus	I/ O	3.3V signal levels all ISA inputs 5V tolerant
SA0..19	ISA Small Address bus	O	3.3V signal levels
LA17..23	ISA Large Address bus	O	3.3V signal level
SBHE#	ISA System Byte High Enable	O	
BALE	ISA Address Latch Enable	O	
AEN	ISA Address Enable	n.a.	Pull down
MEMR#	ISA memory read	O	
SMEMR#	ISA memory read	O	
MEMW#	ISA memory write	O	
SMEMW#	ISA memory write	O	
IOR#	ISA IO read	O	
IOW#	ISA IO write	O	
IOCHK#	ISA IO check	n.a.	Pull up
IOCHRDY	ISA IO channel ready	I	5V tolerant
M16#	ISA 16Bit memory device	n.a.	Pull up
IO16#	ISA 16Bit IO device	n.a.	Pull up
REFSH#	ISA memory refresh cycle pending	n.a.	Pull up
NOWS#	ISA No wait states	n.a.	Pull up
MASTER#	ISA Master	n.a.	Pull up
SYSCLK	ISA System clock (8,3 MHz)	O	
OSC	ISA Oscillator (14,31818 MHz)	n.a.	Pull down
RSTDRV	ISA Reset signal	O	System reset (5V levels)
DREQ0..7	ISA DMA request	n.a.	Pull down
DACK0#..7#	ISA DMA acknowledge	n.a.	Pull up
TC	ISA DMA end / terminal count	n.a.	Pull down
IRQ3..15	ISA Interrupt request	I	5V tolerant Interrupt table see 2.4

Table 24: ISA bus Note: n.a. = not available

4.3. Connector X3 (CRT, Display, Serial, Parallel)

Standard pin out with LVDS and LPT

Pin	Signal	Function	Pin	Signal	Function
1	GND		2	GND	
3	R	CRT	4	B	CRT
5	HSY	CRT	6	G	CRT
7	VSY	CRT	8	DDCK	I2C SCK
9	DETECT#	n.c.	10	DDDA	I2C SDA
11	LCDDO16	LCD	12	LCDDO18	LCD
13	LCDDO17	LCD	14	LCDDO19	LCD
15	GND		16	GND	
17	LCDDO13	LCD	18	LCDDO15	LCD
19	LCDDO12	LCD	20	LCDDO14	LCD
21	GND		22	GND	
23	LCDDO8	LCD	24	LCDDO11	LCD
25	LCDDO9	LCD	26	LCDDO10	LCD
27	GND		28	GND	
29	LCDDO4	LCD	30	LCDDO7	LCD
31	LCDDO5	LCD	32	LCDDO6	LCD
33	GND		34	GND	
35	LCDDO1	LCD	36	LCDDO3	LCD
37	LCDDO0	LCD	38	LCDDO2	LCD
39	VCC		40	VCC	
41	JILI_DAT	LCD JILI	42	LTGIO0 / VSYNC	LCD
43	JILI_CLK	LCD JILI	44	BLON#	LCD
45	BIASON / HSYNC	LCD	46	DIGON	LCD
47	COMP	n.c.	48	Y	n.c.
49	SYNC	n.c.	50	C	n.c.
51	LPT / FLPY#	n.c.	52	RESERVED	n.c.
53	VCC		54	GND	
55	STB# / RES	LPT	56	AFD# / DENSEL	LPT
57	RESERVED	n.c.	58	PD7 / RESERVED	LPT
59	IRRX	IrDA	60	ERR# / HDSEL#	LPT
61	IRTX	IrDA	62	PD6 / RESERVED	LPT
63	RXD2	UART2	64	INIT# / DIR#	LPT
65	GND		66	GND	
67	RTS2#	UART2	68	PD5 / RESERVED	LPT
69	DTR2#	n.c.	70	SLIN# / STEP#	LPT
71	DCD2#	n.c.	72	PD4 / DSKCHG#	LPT
73	DSR2#	n.c.	74	PD3 / RDATA#	LPT
75	CTS2#	UART2	76	PD2 / WP#	LPT
77	TXD2#	UART2	78	PD1 / TRK0#	LPT
79	RI2#	n.c.	80	PD0 / INDEX#	LPT

Pin	Signal	Function	Pin	Signal	Function
81	VCC		82	VCC	
83	RXD1	UART1	84	ACK / DRV1	LPT
85	RTS1#	UART1	86	BUSY# / MOT1#	LPT
87	DTR1#	UART1	88	PE / WDATA#	LPT
89	DCD1#	UART1	90	SLCT# / WGATE#	LPT
91	DSR1#	UART1	92	MSCLK	n.c.
93	CTS1#	UART1	94	MSDAT	n.c.
95	TXD1	UART1	96	KBCLK	n.c.
97	RI1#	UART1	98	KBDAT	n.c.
99	GND		100	GND	

Table 25: ET(e) connector X3

Note: n.c. = not connected

Signal	Description	I/O	Note
VCC	Power Supply +5VDC, 5%	I	external supply
GND	Power Ground	I	external supply

Table 26: X3 Power

Signal	Description of analog CRT signals (optional)	I/O	Note
HSYNC	Horizontal Sync	O	CRT
VSYNC	Vertical Sync	O	CRT
R	Red channel	O	CRT
G	Green channel	O	CRT
B	Blue channel	O	CRT
DDCK	Display Data Channel Clock	O	GPU I²C clock
DDDA	Display Data Channel Data	I/O	GPU I²C data

Table 27: CRT

Signal	Description of TV signals (option)	I/O	Note
SYNC	Composite sync	n.a.	n.c.
Y	Luminance for S-Video	n.a.	n.c.
C	Chrominance for S-Video	n.a.	n.c.
Comp	Composite Video	n.a.	n.c.

Table 28: Video

Note: n.a. = not available
n.c. = not connected

Signal	Description of UART1 signals	I/O	Note
DTR1#	Data terminal ready of COM1	I	5V tolerant
RI1#	Ring indicator of COM1	I	5V tolerant
TXD1	Data transmit of COM1	O	3.3V out
RXD1	Data receive of COM1	I	5V tolerant
CTS1#	Clear to send of COM1	I	5V tolerant
RTS1#	Request to send of COM1	O	3.3V out
DCD1#	Data carrier detect of COM1	O	3.3V out
DSR1#	Data set ready of COM1	I	5V tolerant

Signal	Description of UART2 (BlueTooth) signals	I/O	Note
DTR2#	Data terminal ready	n.a.	Pull up
RI2#	Ring indicator	n.c.	n.a.
TXD2	Data transmit of Bluetooth	O	3.3V out
RXD2	Data receive of Bluetooth	I	5V tolerant
CTS2#	Clear to send of Bluetooth	I	5V tolerant
RTS2#	Request to send of Bluetooth	O	3.3V out
DCD2#	Data carrier detect	n.c.	n.a.
DSR2#	Data set ready	n.c.	n.a.

Signal	Description of IrDA signals	I/O	Note
IRTX	Infrared Transmit	O	3.3V out
IRRX	Infrared Receive	I	5V tolerant

Table 29: UART1/2, IrDA

Note: n.a. = not available
n.c. = not connected

Signal	Description of PS/2 signals	I/O	Note
KBDAT	Keyboard Data	n.c.	n.a.
KBCLK	Keyboard Clock	n.c.	n.a.
MSDAT	Mouse Data	n.c.	n.a.
MSCLK	Mouse Clock	n.c.	n.a.

Table 30: PS/2

Note: n.a. = not available
n.c. = not connected

Signal	Description of LPT signals	I/O	Note
LPT / FLPY#	LPT or Floppy Interface configuration input	n.a.	n.c. LPT only
STB# / RESERVED	Strobe signal	O	
AFD# / DENSEL	Automatic feed	O	
PD0 / INDEX#	Data bus D0	I/O	
PD1 / TRK0#	Data bus D1	I/O	
PD2 / WP#	Data bus D2	I/O	
PD3 / RDATA#	Data bus D3	I/O	
PD4 / DSKCHG#	Data bus D4	I/O	
PD5 / RESERVED	Data bus D5	I/O	
PD6 / RESERVED	Data bus D6	I/O	
PD7 / RES	Data bus D7	I/O	
ERR# / HDSEL#	LPT error	I	
INIT# / DIR#	Initiate	O	
SLIN# / STEP#	Select	O	
ACK / DRV1	Acknowledge	I	
BUSY# / MOT1#	Busy	I	
PE / WDATA#	Paper empty	I	
SLCT# / WGATE#	Power ON	I	

Table 31: LPT

Note: Floppy disk drive function is not available
n.a. = not available
n.c. = not connected

Signal	Description of LVDS flat panel signals	I/O	Note
BIASON	n.a.	n.c.	
DIGON	Display Power ON	O	
BLON#	Display Backlight ON	O	
LCDDO0	Channel0-	O	LVDS
LCDDO1	Channel0+	O	LVDS
LCDDO2	Channel1-	O	LVDS
LCDDO3	Channel1+	O	LVDS
LCDDO4	Channel2-	O	LVDS
LCDDO5	Channel2+	O	LVDS
LCDDO6	Clock-	O	LVDS
LCDDO7	Clock+	O	LVDS
LCDDO8	n.a.	n.c.	
LCDDO9	n.a.	n.c.	
LCDDO10	n.a.	n.c.	
LCDDO11	n.a.	n.c.	
LCDDO12	n.a.	n.c.	
LCDDO13	n.a.	n.c.	
LCDDO14	n.a.	n.c.	
LCDDO15	n.a.	n.c.	
LCDDO16	n.a.	n.c.	
LCDDO17	n.a.	n.c.	
LCDDO18	n.a.	n.c.	
LCDDO19	n.a.	n.c.	

Table 32: LCD Display (LVDS assignment)

Note: n.a. = not available
n.c. = not connected

Signal	Description of LVTTL flat panel signals	I/O	Note
DIGON	Display Power ON	O	LVTTL
BLON#	Display Backlight ON	O	LVTTL
LCDDO0	RED0	O	LVTTL
LCDDO1	RED1	O	LVTTL
LCDDO2	RED2	O	LVTTL
LCDDO3	RED3	O	LVTTL
LCDDO4	RED4	O	LVTTL
LCDDO5	RED5	O	LVTTL
LCDDO6	GREEN0	O	LVTTL
LCDDO7	GREEN1	O	LVTTL
LCDDO8	GREEN2	O	LVTTL
LCDDO9	GREEN3	O	LVTTL
LCDDO10	GREEN4	O	LVTTL
LCDDO11	GREEN5	O	LVTTL
LCDDO12	BLUE0	O	LVTTL
LCDDO13	BLUE1	O	LVTTL
LCDDO14	BLUE2	O	LVTTL
LCDDO15	BLUE3	O	LVTTL
LCDDO16	BLUE4	O	LVTTL
LCDDO17	BLUE5	O	LVTTL
LCDDO18	Shift Clock	O	SHFCLK, LVTTL
LCDDO19	Data Enable	O	EN, LVTTL
HSYNC	Horizontal Sync	O	HSYNC, LVTTL
VSYNC	Vertical Sync	O	VSYNC, LVTTL

Table 33: LCD Display (TTL assignment)

Note**:** Displays with 2 pixels/clock are not supported

4.4. Connector X4 (IDE, Ethernet, Speaker, Battery, I²C, SMB, etc.)

Pin	Signal	Function	Pin	Signal	Function
1	GND		2	GND	
3	5V_SB	ATX PWR	4	PWGIN	ATX PWR
5	PS_ON	ATX PWR	6	SPEAKER	Beeper TTL
7	PWRBTN#	PWR	8	BATT	RTC Battery
9	KBINH	n.c.	10	LILED	Ethernet
11	RSMRST#	n.c.	12	ACTLED	Ethernet
13	ROMKBCS#	n.c.	14	SPEEDLED	Ethernet
15	EXT_PRG	n.c.	16	I2CLK	I2C
17	VCC		18	VCC	
19	OVCR#	USB	20	GPCS#	n.c.
21	EXTSMI#	n.c.	22	I2DAT	I2C
23	SMBCLK	I2C/SMB	24	SMBDATA	I2C/SMB
25	SIDE_CS3#	n.c.	26	SMBALRT#	n.c.
27	SIDE_CS1#	n.c.	28	DASP_S	n.c.
29	SIDE_A2	n.c.	30	PIDE_CS3#	n.c.
31	SIDE_A0	n.c.	32	PIDE_CS1#	n.c.
33	GND		34	GND	
35	PDIAG_S	n.c.	36	PIDE_A2	n.c.
37	SIDE_A1	n.c.	38	PIDE_A0	n.c.
39	SIDE_INTRQ	n.c.	40	PIDE_A1	n.c.
41	BATLOW#	PWR	42	GPE1#	n.c.
43	SIDE_AK#	n.c.	44	PIDE_INTRQ	n.c.
45	SIDE_RDY	n.c.	46	PIDE_AK#	n.c.
47	SIDE_IOR#	n.c.	48	PIDE_RDY	n.c.
49	VCC		50	VCC	
51	SIDE_IOW#	n.c.	52	PIDE_IOR#	n.c.
53	SIDE_DRQ	n.c.	54	PIDE_IOW#	n.c.
55	SIDE_D15	n.c.	56	PIDE_DRQ	n.c.
57	SIDE_D0	n.c.	58	PIDE_D15	n.c.
59	SIDE_D14	n.c.	60	PIDE_D0	n.c.
61	SIDE_D1	n.c.	62	PIDE_D14	n.c.
63	SIDE_D13	n.c.	64	PIDE_D1	n.c.
65	GND		66	GND	
67	SIDE_D2	n.c.	68	PIDE_D13	n.c.
69	SIDE_D12	n.c.	70	PIDE_D2	n.c.
71	SIDE_D3	n.c.	72	PIDE_D12	n.c.
73	SIDE_D11	n.c.	74	PIDE_D3	n.c.
75	SIDE_D4	n.c.	76	PIDE_D11	n.c.
77	SIDE_D10	n.c.	78	PIDE_D4	n.c.
79	SIDE_D5	n.c.	80	PIDE_D10	n.c.
81	VCC		82	VCC	
83	SIDE_D9	n.c.	84	PIDE_D5	n.c.

85	SIDE_D6	n.c.	86	PIDE_D9	n.c.
87	SIDE_D8	n.c.	88	PIDE_D6	n.c.
89	GPE2#	n.c.	90	CBLID_P#	
91	RXD#	Ethernet	92	PIDE_D8	n.c.
93	RXD	Ethernet	94	SIDE_D7	n.c.
95	TXD#	Ethernet	96	PIDE_D7	n.c.
97	TXD	Ethernet	98	HDRST#	Reset out
99	GND		100	GND	

Table 34: ET(e) connector X4

Note: n.c. = not connected

Signal	Description	I/O	Note
VCC	Power Supply +5VDC, 5%	I	external supply
GND	Power Ground	I	external supply
N.C.	Not connected	n.a.	Do not connect

Table 35: X4 Power

Note: n.a. = not available

Signal	Description of IDE signals	I/O	Note
PIDE_D0..15	Primary IDE Data bus	n.a.	n.c.
PIDE_A0..2	Primary IDE Address bus	n.a.	n.c.
PIDE_CS1#	Primary IDE CS# ch.0	n.a.	n.c.
PIDE_CS3#	Primary IDE CS# ch.1	n.a.	n.c.
PIDE_DRQ	Primary IDE DMA request	n.a.	n.c.
PIDED_AK#	Primary IDE DMA acknowledge	n.a.	n.c.
PIDE_RDY	Primary IDE ready	n.a.	n.c.
PIDE_IOR#	Primary IDE IO read	n.a.	n.c.
PIDE_IOW#	Primary IDE IO write	n.a.	n.c.
PIDE_INTRQ	Primary IDE interrupt request	n.a.	n.c.
CBLID_P#	Cable ID primary	n.a.	n.c.
SIDE_D0..15	Secondary IDE Data bus	n.a.	n.c.
SIDE_A0..2	Secondary IDE Address bus	n.a.	n.c.
SIDE_CS1#	Secondary IDE CS# ch.0	n.a.	n.c.
SIDE_CS3#	Secondary IDE CS# ch.1	n.a.	n.c.
SIDE_DRQ	Secondary IDE dma request	n.a.	n.c.
SIDED_AK#	Secondary IDE dma acknowledge	n.a.	n.c.
SIDE_RDY	Secondary IDE ready	n.a.	n.c.
SIDE_IOR#	Secondary IDE IO read	n.a.	n.c.
SIDE_IOW#	Secondary IDE IO write	n.a.	n.c.
SIDE_INTRQ	Secondary IDE interrupt request	n.a.	n.c.
DASP_S	Secondary IDE Drive active	n.a.	n.c.
PDIAG_S	Secondary IDE Master/Slave	n.a.	n.c.
HDRST#	Hard Disk reset	O	Reset, 5V signal level

Table 36: IDE

Note: n.a. = not available
n.c. = not connected

Signal	Description of Ethernet signals	I/O	Note
TXD, TXD#	Ethernet Twisted Pair transmit signal pair	O	
RXD, RXD#	Ethernet Twisted Pair receive signal pair	I	
ACTLED	Ethernet ACTivity LED	O	
LILED	Ethernet LInk LED	O	
SPEEDLED	Ethernet SPEED LED, ON at 100Mb/s	O	n.c. optional instead of LInk LED

Table 37: Ethernet

Note: n.c. = not connected

Signal	Description of Misc. signals	I/O	Note
SPEAKER	Speaker output	O	XScale GPIO with 3.3V signal level. Do not connect directly to speaker.
BATT	Battery supply for RTC	I	2.0..5.5V
PWGIN	Power good input	I	Connected to system reset
I2CLK	I2C Bus clock	O	5V out
I2DAT	I2C Bus Data	I/O	5V tolerant input
SMBCLK	SM Bus Clock	O	5V out
SMBDAT	SM Bus Data	I/O	5V tolerant input
SMBALRT#	Not supported	n.a.	n.c.
KBINH	Keyboard inhibit	n.a.	n.c.
5V_SB	Supply of internal suspend circuit	I	used for RTC
PS_ON#	Power Supply ON	O	5V signal level
PWRBTN#	Power Button On / Off / Suspend	I	5V tolerant input
OVCR#	Over current detect for USB	I	5V tolerant input
ROMKBCS#	Do not connect	n.a.	n.c.
EXT_PRG#	Do not connect	n.a.	n.c.
GPCS#	General purpose chip select	n.a.	n.c.
GPE1#	LID input	n.a.	n.c.
GPE2#	Ring Input	n.a.	n.c.
BATLOW#	Battery low	I	5V tolerant input
EXTSMI#	External SMI	n.a.	n.c.
RSMRST#	Resume Reset	n.a.	n.c.

Table 38: X4 Miscellaneous

Note: n.a. = not available
n.c. = not connected

5. Software / Windows CE .NET support

The ET(e) XScale Module comes with full Windows CE 4.2 .NET & WinCE 5.0 support. Please note that the XScale CPU is NOT compatible to the X86-PC processors used in PCs. Applications and drivers (!) running on WinCE on other processor architectures (like Pentium, SH-4, MIPS etc.) at least need to be recompiled for the XScale processor. Windows CE - while having a very similar look-and-feel - is not Windows (98, NT, XP..) with e.g. an entirely different driver model. Applications running on 32-Bit PC Windows often require considerable porting effort, which is especially true if they make use of high-end features like DirectX, 3D acceleration etc.
Windows CE is targeted to embedded applications with limited hardware resources. It offers a drastically reduced system overhead at the price of a very different environment in comparison to standard PC Windows

The differences begin immediately after powering up the system.

5.1. Bootloader

Windows CE Platforms with non-X86 Processors do NOT have a BIOS, but a Bootloader. The Bootloader performs similar functions as a BIOS – with a few important differences.

After power-up or reset the XScale jumps into the Bootloader, which always resides in the on-board flash memory device.
In the first step the Bootloader initializes the hardware (bus-controller, timings etc.), so that all internal and external devices (SDRAM, GPIO, peripherals etc.) are correctly mapped into the address space.
After that the Bootloader copies itself from Linear Flash into SDRAM and continues operation from there because executing code from SDRAM is much faster than from Flash Memory.
At this point the Bootloader behaves very much like a BIOS, which allows to do hardware specific settings using it's own menu. In the case of the ET(e) XScale however this is not done via the system display (useless on headless systems), but with an ASCII-Terminal.
The ASCII Terminal uses the COM1-Port of the ET(e)-Module, which is directly accessible on the ATX-Formfactor EVA-Baseboard available from MSC. Only an RS-232 Zero-Modem Cable (9-Pin SubD) and a Computer running an ASCII-Terminal Emulation like HyperTerminal with the following settings is needed:

38400 Bps, **8** Data Bits, **N**o Parity, **1** Stop Bit; Flow-Control: **OFF**

With the terminal setup properly the "**Bootlader Menu"** or one of the following messages is displayed on the Terminal after Power-Up or Reset :

a) "Press [Enter] to boot image stored on CompactFlash or [SPACE] to cancel
b) "Press [Enter] to download now or [SPACE] to cancel
c) "Press [Enter] to launch image stored in flash or [SPACE] to cancel

A stroke to the space key prompts the Bootloader to enter the **"Bootlader Menu"** rather than booting the operating system.

5.2. Bootloader Menu

```
-------------------------------------------------
Boot Loader Menu:

 1: Network Settings
 2: Boot Settings
 3: Display Settings
 4: Miscellaneous Settings

 B: Boot existing CompactFlash image (nk.bin) now

 D: Download new image via ethernet now

 L: Launch existing flash resident image now

 U: Update Bootloader with eboot.bin from CompactFlash
-------------------------------------------------

Enter your selection:
```

```
-------------------------------------------------
Network settings:

  1: DHCP: Enabled
  2: IP address: 192.168.80.2
  3: Subnet mask: 255.255.0.0
  4: Default Gateway: 192.168.80.1
  5: DNS: 192.168.80.1
  6: WINS: 192.168.80.1
  7: SMSC speed selection: Auto Negotiation
  8: Pass network settings to WinCE network driver (SMSC): Disabled
  9: Number of bootme's: 25
  A: Download device search order: CF0 -> CF1 -> SMSC
-------------------------------------------------

Enter your selection or press [Esc] to cancel:
```

1. Enable/disable DHCP (it's recommended to enable DHCP if possible).
2. Enter a fixed IP-Number for the system if DHCP is not possible.
3. Enter the Subnet Mask if DHCP is not possible.
4. Enter the IP-Number of the default gateway if DHCP is not possible.
5. Enter the IP-Number of the DNS server if DHCP is not possible.
6. Enter the IP-Number of the WINS server if DHCP is not possible.
7. Set Ethernet Speed Negotiation (change not recommended).
8. Enable/disable posting of the above network settings to WinCE (for SMSC network driver only).
This facilitates the user to use the same WinCE image for several target systems in a network environment without a DHCP server (using an unique IP address for each system).
Note: These settings will **NOT** be used for a debug connection between WinCE image and Platformbuilder.
For this the corresponding registry settings (VMINI) must be adapted.
9. Set max. Number of "Bootme" Broadcast Messages for Platformbuilder.
A. Sets from where first to download an image via Ethernet & Platformbuilder. The "CF" setting requires an NE2000-compatible CF-Ethernet Card to be installed in the respective CF-Slot on the module.

```
-------------------------------------------------
Boot settings:

 1: Boot delay: 5 seconds
 2: Boot device search order: CF0 -> CF1
 3: Default startup mode: Display Boot Loader Menu
 4: Boot Logo Settings
-------------------------------------------------

Enter your selection or press [Esc] to cancel:
```

1: Sets the time the Bootloader waits for a keystroke to enter the Bootloader Menu if an image should be started automatically.

2: Sets the search order for a bootable image on the CF slots.

3: The Default startup mode defines the behavior of the bootloader after a Power-Up or Reset:
0: "Display Boot Loader Menu at startup", enter the Bootloader menu
1: "Boot Existing CompactFlash Image (nk.bin) at startup", boot WinCE (nk.bin) from CompactFlash
2: "Download new image via ethernet at startup", requires "Platformbuilder" to send the image
3: "Launch existing flash resident image at startup", boot WinCE from the On-Board LinearFlash

4: Options for showing a boot logo at startup
1: Selects whether a boot logo should be displayed and defines the location from which it should be loaded.
2: Selects the position of the boot logo on the boot screen.
3: Selects if the progress bar should be shown if a boot logo has been loaded.
4: Loads a boot logo bitmap file (bootlogo.bmp) from CompactFlash and programs it into the On-Board LinearFlash.
5: Removes a boot logo bitmap from the On-Board LinearFlash.

```
-------------------------------------------------
Display settings:

 1: Display boot progress: Disabled
 2: Pass display type info to WinCE display driver: Disabled
 3: Video display type: NO DISPLAY
 4: Base Address of EDID Structure: 0xA0
 5: User defined display timings
-------------------------------------------------

Enter your selection or press [Esc] to cancel:
```

1: Enables/disables a graphical boot progress display on the LCD display.

2: Enable posting of the display type selection to WinCE (XScale integrated LCD Controller only).

3: Select LCD Display Type:
0: "NO DISPLAY"
1: "LG_LP064V1 (640x480x16)"
2: "LQ10D421 (640x480x16)"
3: "NEC_NL3224BC35_20 (320x240x16)"
4: "NEC_NL6448AC33_18 (640x480x16)"
5: "HLM8620_DP (dual panel) (640x480x16)
6: "NEC_NL6448BC26_01 (640x480x16)"
7: "LQ121S1DG31 (800x600x16)"
8: "NEC_NL8060BC26_17 (800x600x16)"
9: "LQ150X1LW71 (1024x768x16)"
A: "SX14Q001 (320x240x16)"
B: "LQ057Q3DC02 (320x240x16)"
C: "VL_DD320240 (320x240x16)"
D: "EDID DISPLAY (only for INTERNAL display controller !)" via EDID I²C-EEPROM
E: "USER DEFINED TIMINGS (only for INTERNAL display controller !)"

4: Selects the base address of the EDID I²C-EEPROM which contains the according LCD display string for “display auto detection” **or** a valid EDID Structure Version 2 (EDID 2.0) with an “18-byte detailed timing format” block.

1: “0xA0“
2: “0xA2“
3: “0xA4“
4: “0xA6“
5: “0xA8“
6: “0xAA“
7: “0xAC“
8: “0xAE“
9: “SEARCH MODE”

If “SEARCH MODE” has been selected the complete range (0xA0 … 0xAE) will be searched for a valid EDID structure.

Display auto detection:

Bootloader: Video display type	**EDID: Manufacturer/product ID string (offset 08h)**
LG_LP064V1	LP064V1
LQ10D421	LQ10D421
NEC_NL3224BC35_20	NL3224BC35-20
NEC_NL6448AC33_18	NL6448AC33-18
HLM8620_DP (dual panel)	HLM8620_DP
NEC_NL6448BC26_01	NL6448BC26-01
LQ121S1DG31	LQ121S1DG31
NEC_NL8060BC26_17	NL8060BC26-17
LQ150X1LW71	LQ150X1LW71
SX14Q001	SX14Q001
LQ057Q3DC02	LQ057Q3DC02
VL_DD320240	DD320240

Table 39: EDID display information

5: Selects display timing settings for a LCD display without an EDID I²C-EEPROM.
The requested information is based on the “18-byte detailed timing format” block of an EDID 2.0 structure.
Note:
The requested value for the “Flags” differs from the EDID 2.0 structure and is bootloader specific:

Bit 0:	DE polarity	0: active low	1: active high
Bit 1:	Clock edge selection	0: falling edge	1: rising edge
Bit 2:	Double pixel data	0: disabled	1: enabled (both edges used)
Bit 3:	V-Sync polarity	0: active low	1: active high
Bit 4:	H-Sync polarity	0: active low	1: active high
Bit 5:	Active/Passive display	0: active display (TFT)	1: passive display (STN)
Bit 6:	Color/Monochrome display	0: color display	1: monochrome display
Bit 7:	Single/Dual panel mode	0: single panel	1: double panel

```
------------------------------------------------
Miscellaneous settings:

 1: Core Frequency: 200 MHz
 2: Program loaded RAM image into FLASH: Disabled
 3: Remove existing flash resident image
 4: Debug outputs: Bootloader only
 5: Power button: Power off
 6: Automatic update of bootloader settings: Enabled
 7: Reserved FLASH memory size for FLASH DISK: 0 kByte
 8: Erase FLASH DISK area in FLASH memory
 9: 32.768kHz from external RTC: Enabled

 L: Load bootloader settings from file
 R: Reset bootloader settings to factory defaults

 S: Substitute Bootloader with 'bootldr.bin' from CompactFlash
          (no checks will be done!)
------------------------------------------------

Enter your selection or press [Esc] to cancel:
```

1: Sets CPU core frequency. 200 MHz CPUs can be run at 400 MHz without risking damages, however operation is not guaranteed under all conditions.
2: Enables an update of the LinearFlash with the image resident in SDRAM. The image has to be downloaded or booted from CompactFlash before programming.
3: Removes an existing flash resident image and frees this area of the LinearFlash.
4: Sets which messages are output to the terminal: None, Bootloader only, Bootloader and + WinCE Debug Messages.
5: Select operation mode of the ATX Power Button: Switch power supply off or enter WinCE Suspend Mode.
6: Selects if the bootloader settings should be updated automatically at startup (with data from “autoconf.cfg” on CompactFlash).
7: Select the size of reserved memory from the LinearFlash for a flash media device (flash disk) under WinCE (only for StrataFlash compatible LinearFlash devices).
Note:
All data in an existing flash disk will be lost if the size of the reserved memory for the flash disk has been changed.
8: Erases the area of reserved LinearFlash memory for a flash media device (flash disk).
9: Selects if the 32.768kHz output of the external RTC should be enabled and used as input for the internal RTC and Power Manager.
If it is disabled the 3.6864MHz oscillator will be used as input for the internal RTC and Power Manager.

L: Load bootloader settings from a file on the CompactFlash.
R: Reset bootloader settings to factory defaults.

S: Substitute existing bootloader with a binary bootloader file ('bootldr.bin') from CompactFlash. The format of the file must be a raw binary image of the bootloader (as it appears in the memory).

Warning : Make sure that the Bootloader file you are using matches the hardware revision of the ET(e) XScale Module (Board Rev 4 and 5 ONLY). Loading the wrong Bootloader or a wrong file format will most likely disable the board. Recovery can only be done by MSC in this case.

```
B: Boot existing CompactFlash image (nk.bin) now
```

B: Exit Booloader Menu and boot WinCE Image from CompactFlash Card.

```
D: Download new image via ethernet now
```

D: Exit Booloader Menu and initiate download of a WinCE Image via Ethernet using Platformbuilder.

```
L: Launch existing flash resident image now
```

L: Exit Booloader Menu and boot WinCE Image form on-board linear flash.

```
U: Update Bootloader with eboot.bin from CompactFlash
```

U: Updates the Bootloader with an eboot.bin file from Compact Flash

Warning : Make sure that the Bootloader file you are using matches the hardware revision of the ET(e) XScale Module (Board Rev 4 and 5 ONLY). Bootloader files are available as binary files from MSC, only. Loading the wrong Bootloader will most likely disable the board. Recovery can only be done by MSC in this case.

5.3. WinCE 4.2 .NET BSP

The ET(e) XSC Module comes with a complete WinCE 4.2 .NET BSP with driver support for the following devices:

Feature	Device	Comment
LCD Controller	PXA255	max. 640x480 TFT/LVDS/STN
Graphics Controller	Silicon Motion SM501	320x240, 640x480,800x600,1024x768 TFT/LVDS/STN
Ethernet	SMSC 91C111/113	Full WinCE support
USB Host	Cypress CY7C67200	HID Mouse, Keyboard, Memory Stick / Mass Storage
USB Function	PXA255	ActiveSync
LPT Controller	EXAR ST78C36	WinCE Standard Printer
Compact Flash	PXA255	2 Slots: Memory & I/O Cards (NE2000)
Audio AC97	National LM4548	Full WinCE support
I2C/SMB	PXA255 HW/Emulation	UspEPC Vesa EDID Display Data
UART	PXA255	Full support
IRDA	PXA255	TXD and RXD
Bluetooth	PXA255	TXD, RXD, CTS and RTS

Table 40: WinCE.net support

The following general WinCE features are supported / can be included in an image if required by the customer:

Power management: WinCE power management using the extended features of the PXA-255 CPU including reduction of the core voltage, suspend mode, sleep & idle mode.

Debugging: Download & debugging of WinCE Images via Ethernet using MS Platformbuilder. Either the on-board Ethernet Controller or an NE2000 compatible CF-Ethernet-Card can be used.
Download & debugging of Applications (C, C++, C#, VB.NET) using Embedded Visual C++ or Visual Studio.NET & Compact Framework (where required) via Ethernet.
Debugging via RS232 is possible, while not recommended

Hive-based registry

ActiveSync: Access to system resources using USB or RS-232 connections.

Bootloader and drivers are provided as binary/compiled only.

6. Low Level / JTAG Debugging

It is possible to debug the XScale Module using a JTAG debugger like the ARM-MultiICE and the integrated ARM-compatible debug interface of the PXA-255.

The major advantage of this method is that it is entirely independent of the operating system or any other software running on the XScale and that it does not make use of interfaces that could be required by the actual application.
It is actually possible – while not recommended because of the very limited speed of the JTAG interface - to debug WinCE applications with the JTAG debugger and a SW-PlugIn for Platformbuilder

The JTAG Debugger is connected to the ET(e) module using the “DEBUG” connector (FPC-type). There is a debug adapter available from MSC which converts the standard ARM debug connector into the FPC interface.

Pin	Signal
1	3,3V
2	3,3V
3	d.n.u.
4	d.n.u.
5	d.n.u.
6	d.n.u.
7	d.n.u.
8	RESET#
9	GND
10	TCK
11	TRSL#
12	TDI
13	TDO
14	TMS
15	d.n.u.
16	GND
17	d.n.u.
18	d.n.u.
19	GND
20	d.n.u.
21	d.n.u.
22	d.n.u.
23	d.n.u.
24	d.n.u.
25	d.n.u.
26	d.n.u.
27	d.n.u.
28	GND
29	n.c.
30	n.c.
31	n.c.

Table 41: Debug connector

Note: d.n.u. : Do Not Use
n.c. : Not connected