1:4 LVPECL/CML FANOUT BUFFER WITH INTERNAL TERMINATION

Precision Edge® SY58020/21/22U EVALUATION BOARD

FEATURES

- **Precision, fully differential 1:4 fanout buffer family**
  - **SY58020U—6GHz any diff. input-to-CML outputs (4)**
  - **SY58021U—4GHz any diff. input-to-800mV LVPECL outputs (4)**
  - **SY58022U—5.5GHz any diff. input-to-400mV LVPECL outputs (4)**
- **Low jitter performance:**
  - **< 10ps$_{PP}$ total jitter (clock)**
  - **< 1ps$_{RMS}$ random jitter (data)**
  - **< 10ps$_{PP}$ deterministic jitter (data)**
- **Accepts an input signal as low as 100mV**
- **Unique input termination and V_T pin accepts DC- and AC-coupled differential inputs: LVPECL, LVDS, and CML**
- **Power supply 2.5V ±5% and 3.3V ±10%**
- **Industrial –40°C to +85°C temperature range**
- **Available in 16-pin (3mm × 3mm) MLF® package**

APPLICATIONS

- **All SONET and all GigE clock distribution**
- **Fibre Channel clock and data distribution**
- **Backplanes**
- **Data distribution: OC-48, OC-48+FEC, XAUI**
- **High-end, low skew, multiprocessor synchronous clock distribution**

DESCRIPTION

The SY58020U, SY58021U, and SY58022U are 2.5V/3.3V precision, high-speed, fully differential 1:4 fanout buffers with CML, LVPECL, and 400mV LVPECL outputs. The SY58020U and SY58022U can process clock signals as fast as 6GHz and 5.5GHz respectively, whereas, the SY58021U (800mV LVPECL) can process clock signals as fast as 4GHz.

The 1:4 fanout buffers include Micrel's unique, 3-pin input termination architecture that allows the devices to directly interface to LVPECL, CML, and LVDS differential signals (AC-coupled or DC-coupled) without any level-shifting or termination resistor network in the signal path.

This documentation provides design and implementation information, and a detailed description of the SY58020U, SY58021U, and SY58022U evaluation boards. The evaluation boards are intended to provide a convenient test and evaluation platform.

All data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

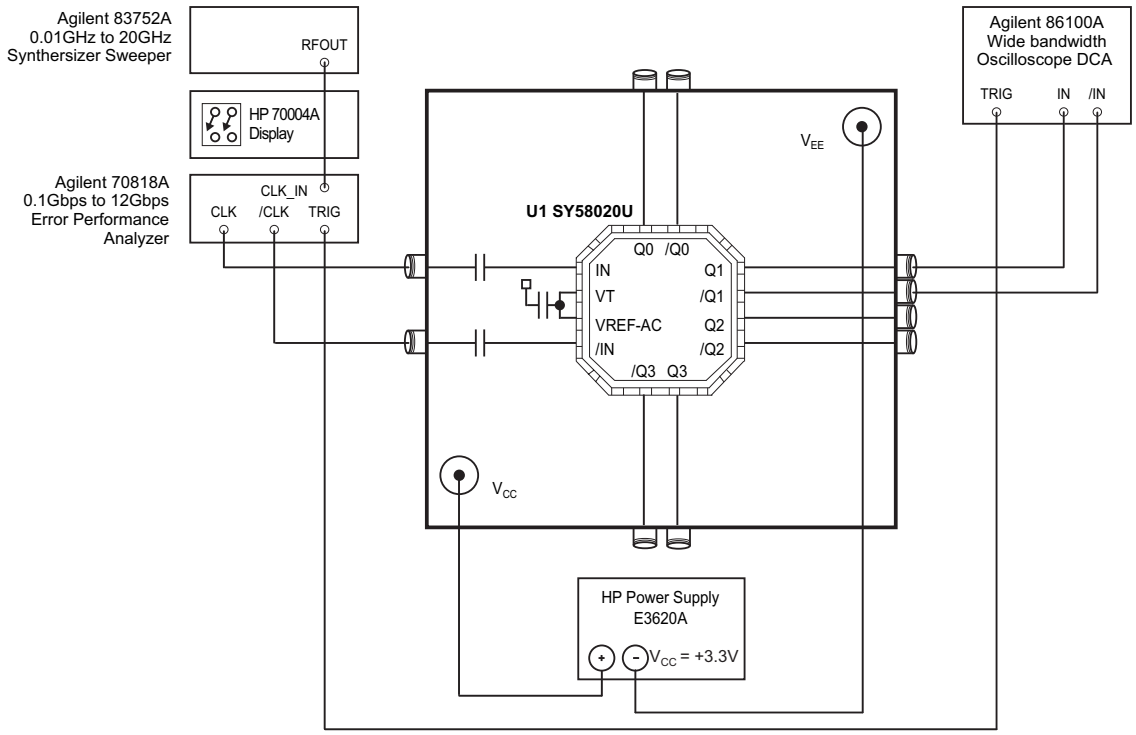


Figure 1. SY58020U Evaluation Board and DC-Coupled Test Setup (Eye Diagram and t_r/t_f Setup)

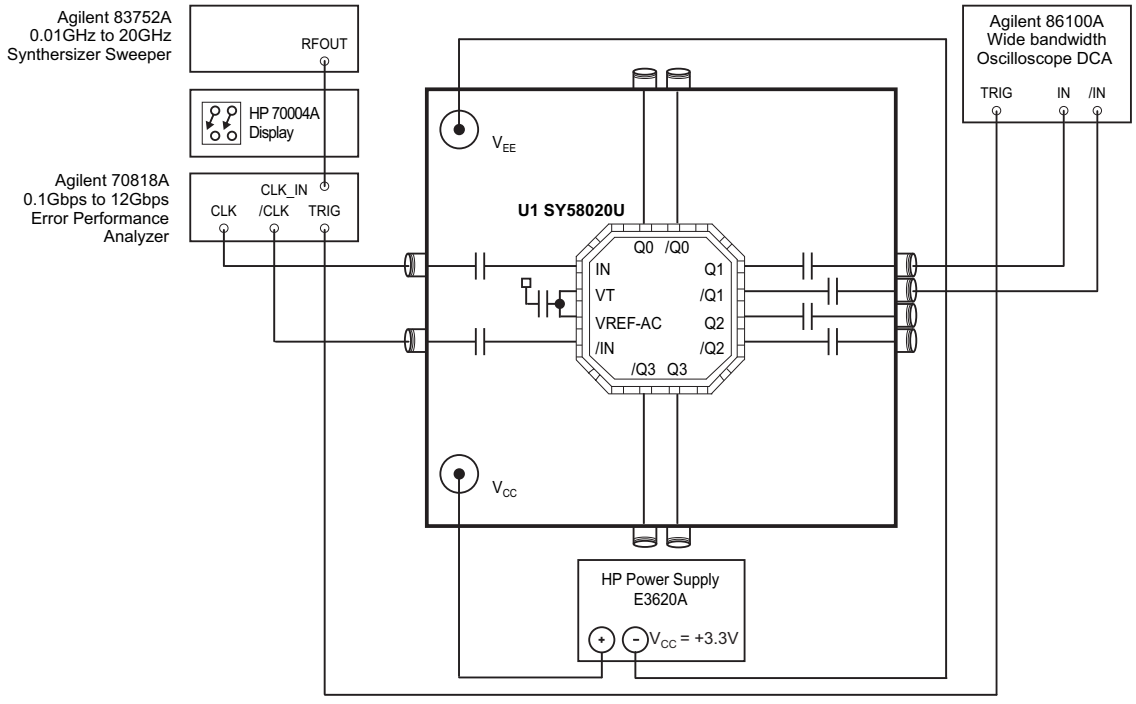


Figure 2. SY58020U Evaluation Board and AC-Coupled Test Setup (Eye Diagram and t_r/t_f Setup)

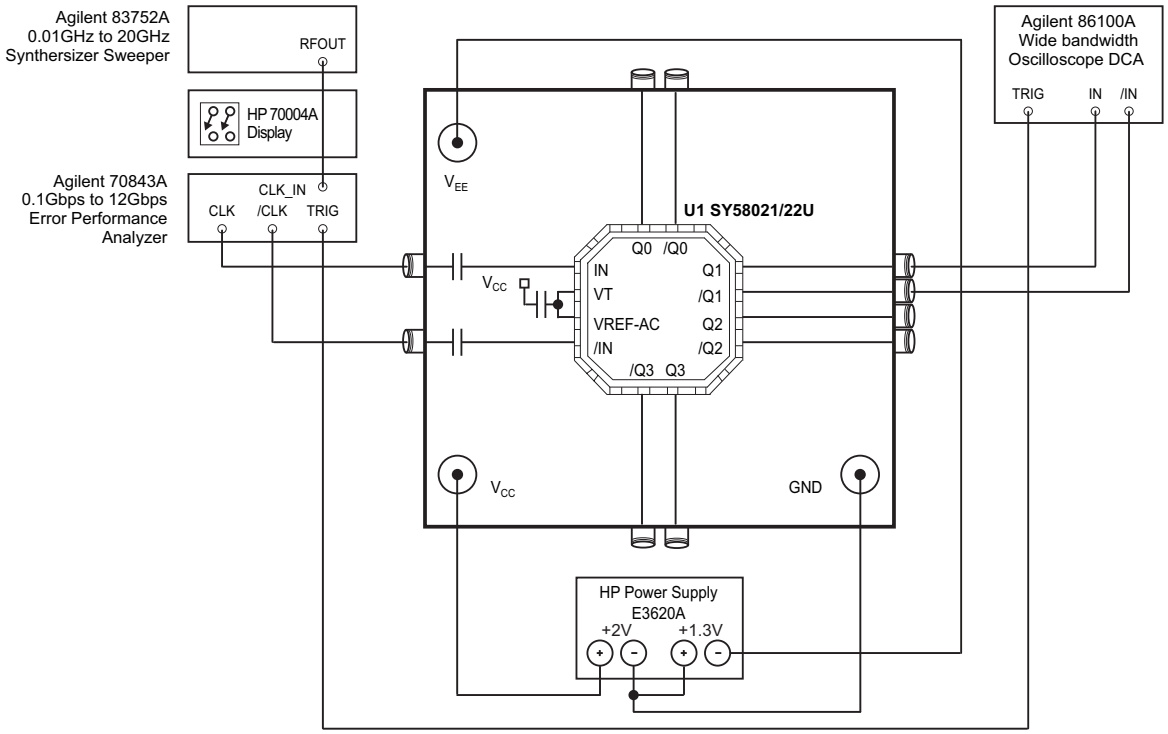


Figure 3. SY58021/22U Evaluation Board and DC-Coupled Test Setup (Eye Diagram and t_r/t_f Setup)

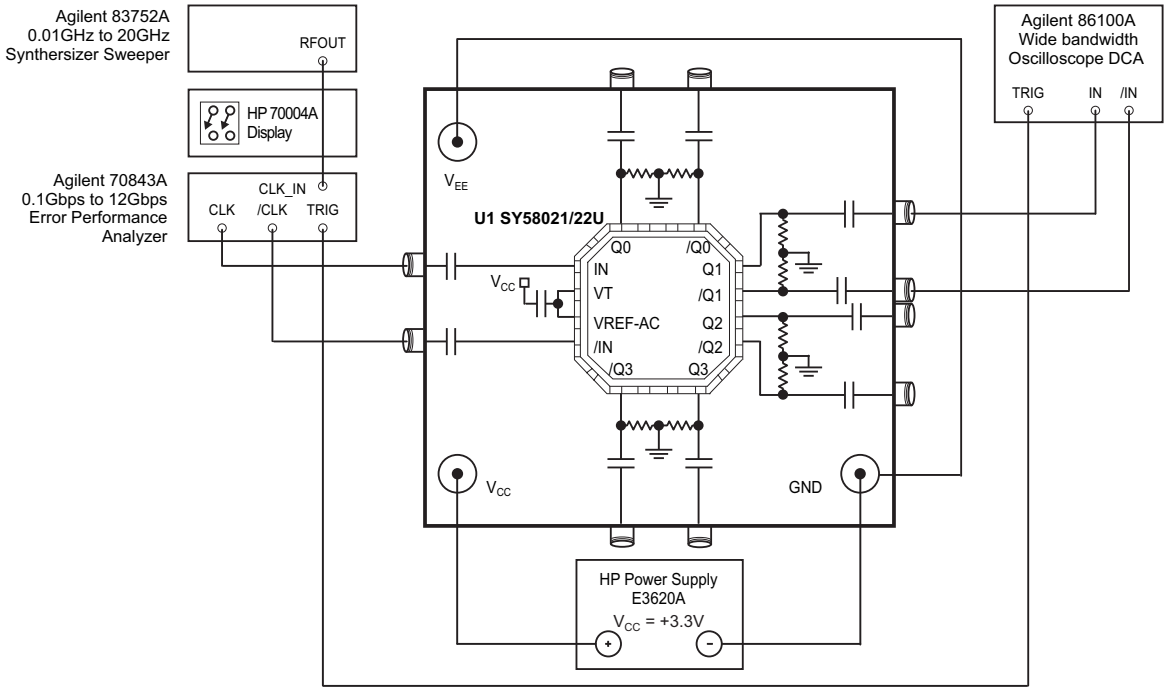


Figure 4. SY58021/22U Evaluation Board and AC-Coupled Test Setup (Eye Diagram and t_r/t_f Setup)

FUNCTIONAL DESCRIPTION

The SY58020U, SY58021U and SY58022U evaluation boards simplify test and measurement of jitter and AC-performance and have been preconfigured to function at both 2.5 ±5% and 3.3V ±10% supply voltage.

Signal Inputs/Outputs

The SY58020/21/22U evaluation boards have been designed and shipped with AC-coupled inputs, and DC-coupled outputs. The SY58020U, SY58021U and SY58022U require a 100mV minimum input signal to guarantee operation. The SY58020U CML outputs deliver 400mV swing into 50Ω. The SY58021U outputs provide 800mV swing (100k compatible), and the SY58022U outputs provide a faster, 400mV LVPECL swing (100k compatible). Unused output pairs maybe left floating with no impact on jitter.

Power Supply

The SY58020U, SY58021U and SY58022U are 2.5V ±5% and 3.3V ±10% devices. The SY58020U CML evaluation board has been configured for positive power supply, see Figure 1, meaning V_{CC} = +3.3V, and GND = 0V. Further, the SY58021U and SY58022U LVPECL evaluation boards have been configured for split power supply, meaning V_{CC} = 2V, GND = 0V, and V_{EE} = (–0.5V or –1.3) see Figure 3. Therefore, the SY58021/22U are shipped with split power supply, so that the output can directly interface with a 50Ω load.

SY58020U AC-Coupled Output Configuration

The SY58020U can be configured for AC-coupled output by following the next few steps.

1. Add AC-coupling capacitors, which normally is 0.1μF, to C6-C7, C8-C11 and C12-C13, see Figure 5 and 6. (The value of the AC-coupling capacitor depends on the frequency of the application.)

SY58021/22U AC-Coupled Output Configuration

The SY58021/22U can be configured for normal power supply or V_{CC} = 2.5V/3.3V and GND = V_{EE} = 0 by following the next few steps.

1. Add AC-coupling capacitors, which normally is 0.1μF to C6-C7, C8-C11 and C7-C8, see Figure 7 and 8. (The value of the AC-coupling capacitor depends on the frequency of the application.)
2. Add resistor pull-downs R1-R8. The resistor pull-downs, are normally 50Ω for V_{CC} = 2.5V or 100Ω for V_{CC} = 3.3V.

Board Layout

The evaluation boards are constructed with Rogers 4003 material and is co-planer designed to minimize noise, and achieve high bandwidth, and minimize crosstalk.

Layer Stack SY58020U

L1	Signal/V_{CC}
L2	Impedance V_{CC}
L3	GND
L4	Signal/V_{CC}

Layer Stack SY58021/22U

L1	Signal/GND
L2	Impedance GND
L3	V_{CC}
L4	Signal/GND

Test Description

This section contains step-by-step instructions for evaluating the SY58020U, SY58021U, and SY58022U. There are several evaluation tests that can be performed on the devices. First, the devices can be tested functionally for AC-performance including eye-diagram generation, and second, the devices can be tested for jitter.

Functionality AC-Testing

Equipment

1. HP8133A Function Generator
2. HP E3620A Power Supply
3. Agilent 86100A Widebandwidth Oscilloscope DCA
4. Agilent 83752A 0.01GHz to 20GHz Synthesizer Sweeper
5. HP70004A Display
6. Agilent 70843A 0.1Gbps to 12Gbps Error Performance Analyzer
7. Harbour Industries Stiff Cables Model 2748 SB-142

AC-Testing

SY58020U

1. Connect V_{CC} to +3.3V, and GND to 0V.
2. Using Agilent BERT Stack (see Figure 1) connect OUT and /OUT to IN and /IN of the SY58020U.
3. Set the desired frequency of operation, and make sure that V_{IL} and V_{IH} and f_{MAX} are within data sheet limits. The SY58020U can accept LVPECL, LVDS, and CML input compatible signals. In addition, if an eye-diagram is desired, set the Agilent BERT Stack to 2^{23}–1 PRBS pattern, if a clock pattern is desired, set the Agilent BERT Stack accordingly.
4. Connect OUT and /OUT of the evaluation board to an oscilloscope.
5. Connect the trigger out connection of the Agilent BERT Stack to the input trigger of the oscilloscope and make measurement.

SY58021U and SY58022U

1. Connect V_{CC} to 2V, GND to 0V, and V_{EE} = (–0.5V or –1.3V) for DC-coupled outputs shown in Figure 3 and connect V_{CC} = 3.3V, GND and V_{EE} to 0V for AC-coupled outputs as shown in Figure 1.
2. Using Agilent BERT Stack (see Figure 1) connect OUT and /OUT to IN and /IN of the SY58021U and SY58022U.
3. Set the desired frequency of operation, and make sure that V_{IL} and V_{IH} and f_{MAX} are within data sheet limits. The SY58021U and SY58022U can accept LVPECL, LVDS, and CML input compatible signals. In addition, if an eye-diagram is desired, set the Agilent BERT Stack to 2^{23}–1 PRBS pattern, if a clock pattern is desired, set the Agilent BERT Stack accordingly.
4. Connect OUT and /OUT of the evaluation board to an oscilloscope.
5. Connect the trigger out connection of the Agilent BERT Stack to the input trigger of the oscilloscope and make measurement.

Jitter Test

Measuring jitter is a relative process and involves establishing a base line. Measure the generated jitter from a pulse generator used to drive the SY58020U, SY58021U, or SY58022U. Once this is established, jitter generated from the part is compared against the jitter generated from the pulse generator, and the difference is the jitter generated from the DUT.

Deterministic Jitter

Configure a HP8133A Pulse Generator to a PRBS K28.5 data pattern at 3E8CC173'H and set the HP8133A to a desired frequency with LVPECL, 400mV LVPECL, or CML levels and connect the outputs to a Wavecrest DTS-2079. Remember that the level set should correspond to the output level expected from the device under test. In other words, if it's the SY58020U that is being tested, the output of the HP8133A should be set to CML and the V_{OH} and V_{OL} levels should correspond to the outputs of the device. If the level is not set at the same level generated from the device, the measurement will be off. In addition, if it's the SY58021U that is to be tested, the LVPECL should be programmed level generated from the HP8133A, and likewise for the SY58022U, set the output of the HP8133A to 400mV LVPECL. The next few steps involves performing a learn operation which measures the amount of jitter generated from the HP8133A which will be stored and the results compared against the jitter generated by the devices when driven by a HP8133A.

Wavecrest Setup

1. Connect the HP8133A to the Wavecrest instruments. The output OUT of the HP8133A should connect to the input CH1 of the Wavecrest instrument, and the trigger output of the HP8133A should connect to the ARM input of the Wavecrest instrument.
2. On the HP8133A, select bit 0 as trigger start, in addition, configure the HP8133A to the desired data-rate and NRZ data pattern.
3. On the Wavecrest instruments menu, select datacom tool.
4. Then click on known pattern w/marker on the menu.
5. Under the View Tab, select –DCD+DDJ vs. SPA.
6. Make sure that the following settings are configured:
   a. Quick Mode = On
   b. Tail Fit = Off
   c. Advanced Options = Off
7. Hit the pulse find button and make sure that the appropriate levels are being read on the Wavecrest. For example, if the device is LVPECL, 800mV should be read from the Wavecrest with correct V_{OH} and V_{OL} levels.
8. Click on the display bottom and select values on plot to be view all.
9. Then on the advanced options button select on and go to page 2 of the Wavecrest menu, select learn pattern option and include DCD+DDJ calibration. Additionally, set the total number of bits to be 32, and set the appropriate bit rate then click on learn.
10. The Wavecrest will then plot the K28.5 bit sequence and determine the deterministic jitter, random jitter, and total jitter of the HP8133A.
11. At this point save the results, and reload the results into the Wavecrest.
12. Next, drive the SY58020U, or SY58021U, or SY58022U with the HP8133A, and connect the outputs of the Wavecrest.
13. Repeat #3 and #10 and compare the results of the generated jitter to the jitter generated by the HP8133A. The difference between the two measurements will determine the deterministic jitter being generated by the device.

Random Jitter

Random jitter can be measured two different ways. One way is similar to measuring the deterministic jitter which uses a Wavecrest DTS instrument, but with a K28.7 1010... (clock pattern) using the same concept of measuring the jitter generated by the Agilent 8133A, then comparing it to the jitter generated from the device while being driven by the Agilent 8133A. Another way is to drive the device using a clock pattern and measuring the histogram at the output using a Tektronic scope and directly measuring the random jitter.

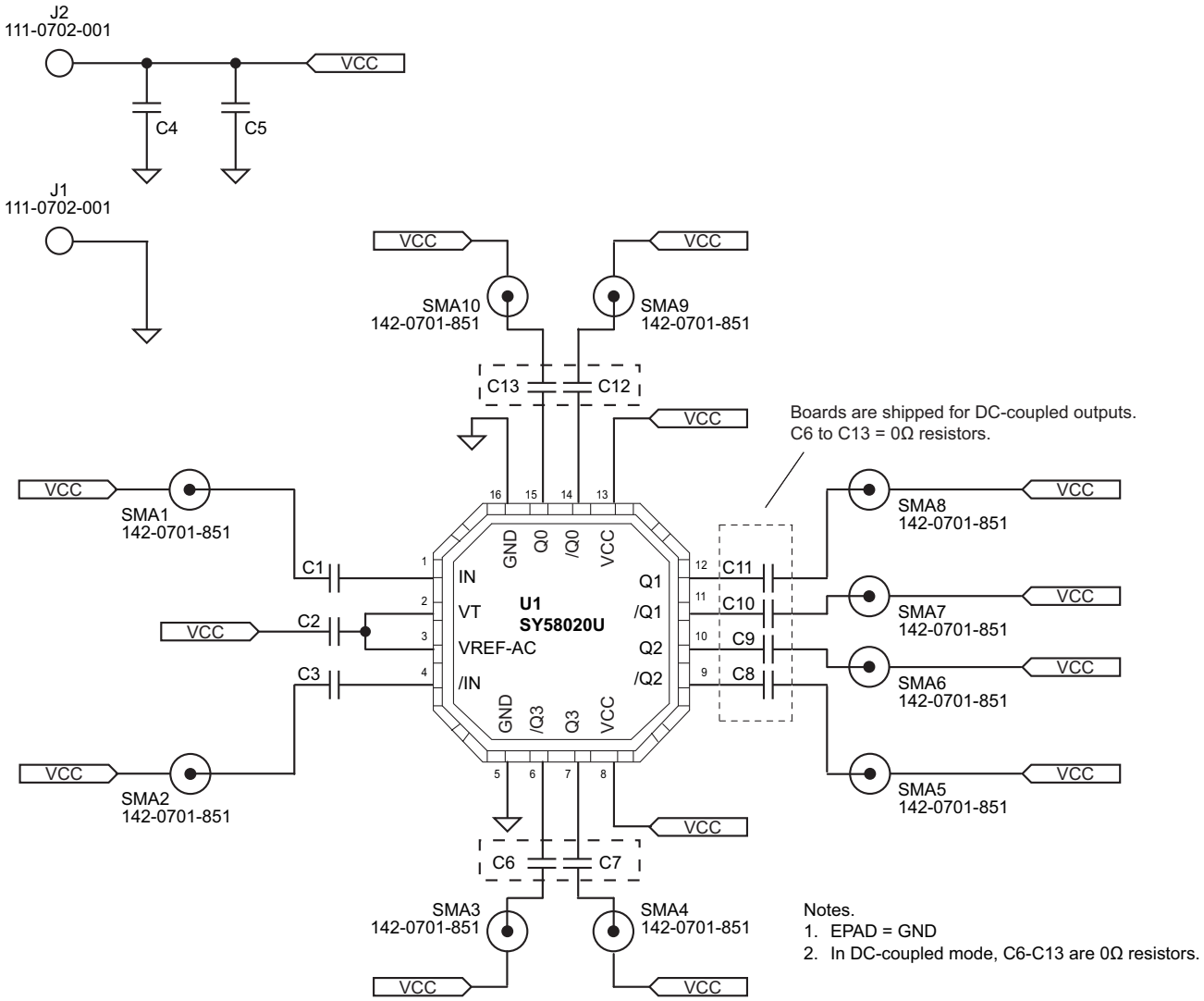
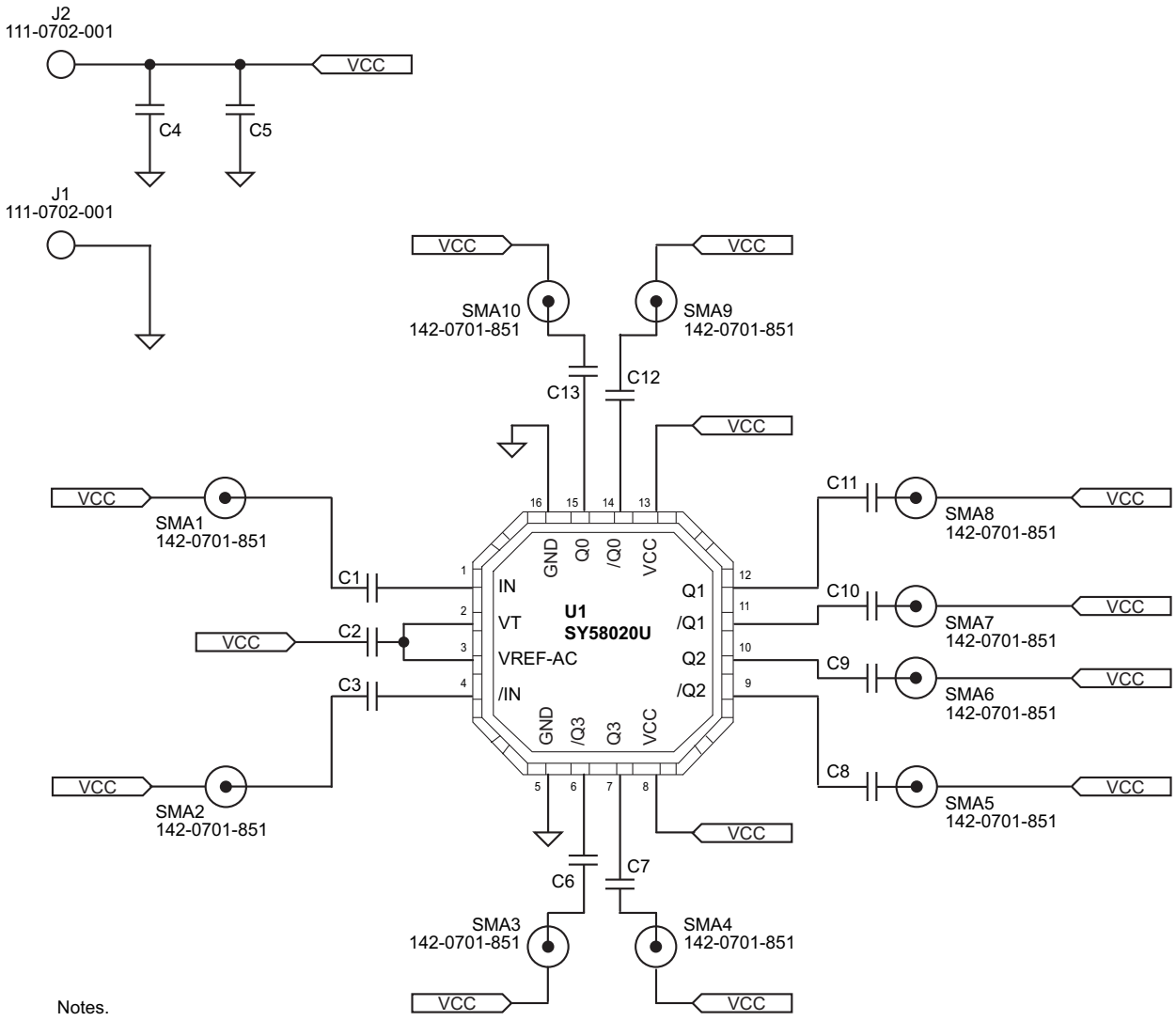
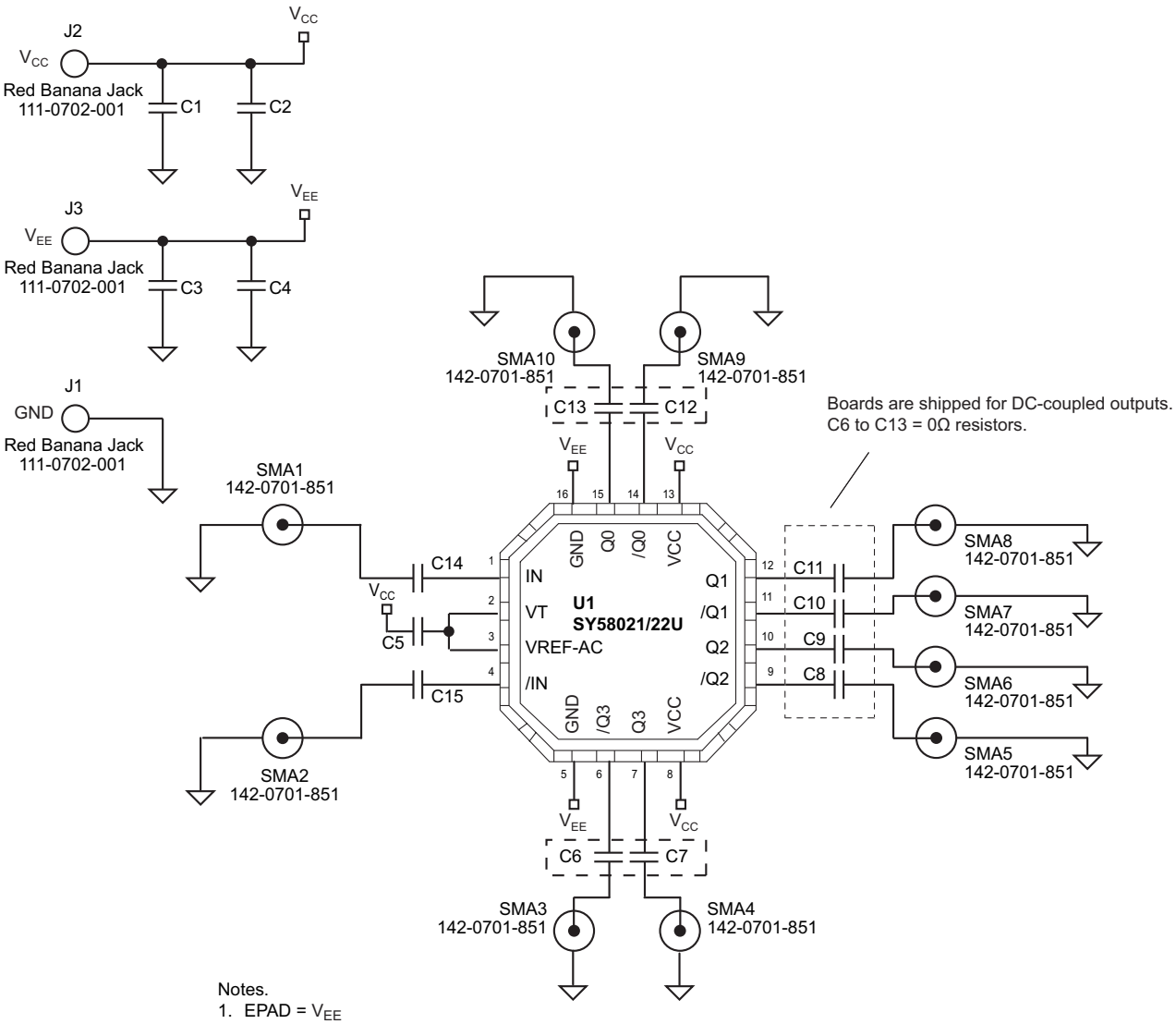


Figure 5. SY58020U DC-Coupled Evaluation Board Schematic



Notes.
1. EPAD = GND
2. In AC-coupled mode, C6-C13 are 0.1µF capacitors, (actual value depends on the frequency of interest.)

Figure 6. SY58020U AC-Coupled Evaluation Board Schematic



Notes.
1. EPAD = V_{EE}
2. In DC-coupled mode, C6-C13 are 0Ω resistors, and R3-R6 are not mounted, see Figure 8.

Figure 7. SY58021/22U DC-Coupled Evaluation Board Schematic

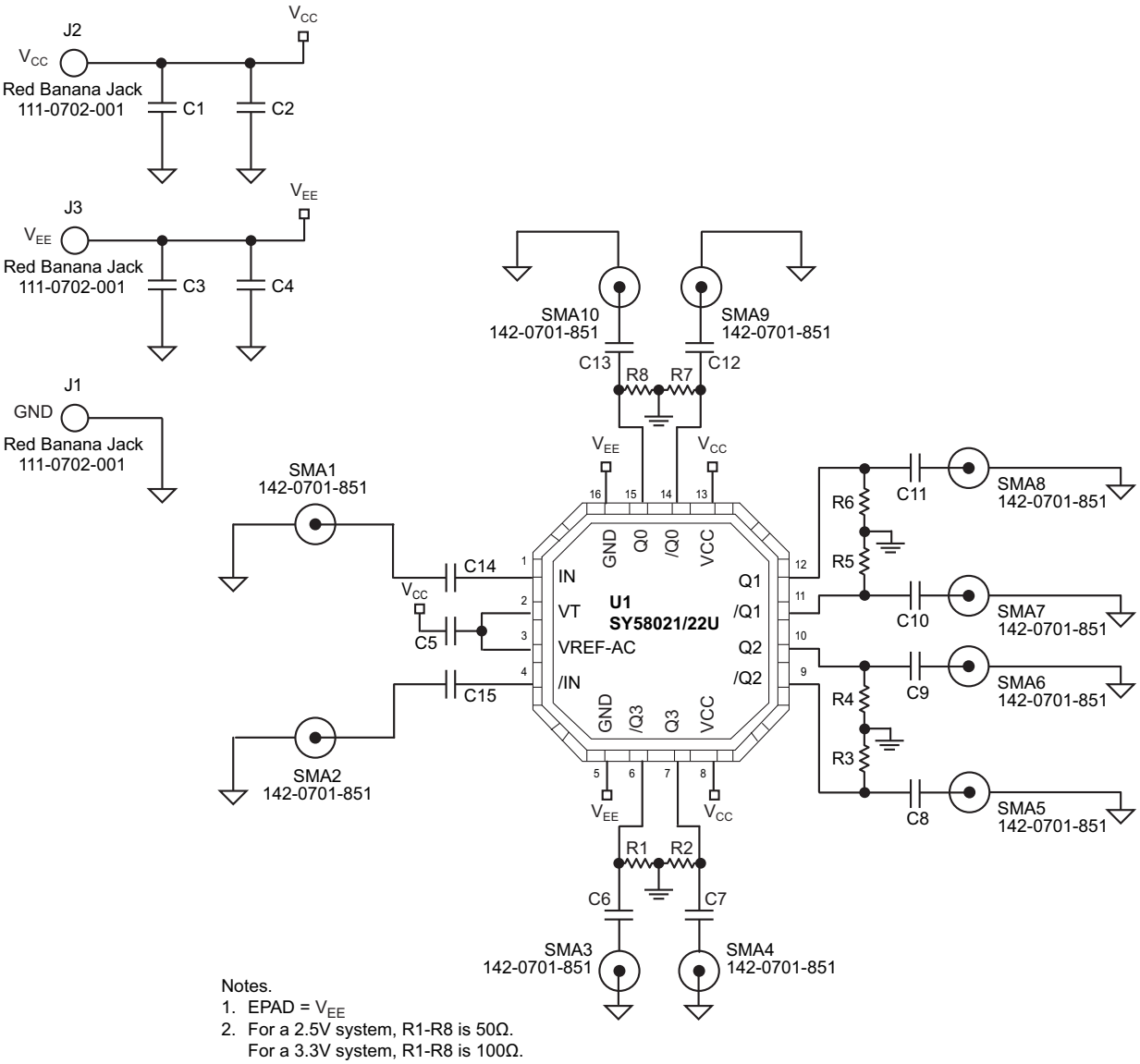


Figure 8. SY58021/22U AC-Coupled Evaluation Board Schematic

BILL OF MATERIALS

SY58020U

Item	Part Number	Manufacturer	Description	Qty.
C1-C4, C6-C13	VJ0402Y104KXXAT	Vishay[1,4]	0.1μF, 10%, Ceramic Capacitor, Size 0402 Dielectric, Size 0402	12
C5	293D685X0025C2T	Vishay[1]	6.8μF, 20V, Tantalum Electrolytic, Capacitor, Size C	1
J1	111-0703-001	Johnson Components[2]	Black Banana Jack	1
J2	111-0703-001	Johnson Components[2]	Red Banana Jack	1
SMA1–SMA10	142-0701-851	Johnson Components[2]	Jack Assembly End Launch SMA	10
U1	**SY58020U**	**Micrel, Inc.**[3]	6GHz 1:4 Fanout Buffer w/CML Outputs and Internal Termination	1

SY58021/22U

Item	Part Number	Manufacturer	Description	Qty.
C1, C3, C5-C15	VJ0402Y104KXXAT	Panasonic[1, 4]	0.1μF, 25V, 10%, Ceramic Capacitor, X5R Dielectric, Size 0402	13
C2, C4	293D685X0025C2T	Panasonic[1]	6.8μF, 20V, Tantalum Electrolytic, Capacitor, Size C	2
J1	111-0703-001	Johnson Components[2]	Black Banana Jack	1
J2, J3	111-0703-001	Johnson Components[2]	Red Banana Jack	2
R1-R8		Panasonic[1, 5]	Chip Resistors, size 0403	8
SMA1–SMA10	142-0701-851	Johnson Components[2]	Jack Assembly End Launch SMA	10
U1	**SY58021/22U**	**Micrel, Inc.**[3]	4GHz to 5.5GHz 1:4 Fanout Buffer w/LVPECL Outputs and Internal Termination	1

Notes:

1. Vishay: www.vishay.comm.
2. Johnson Components: www.johnsoncomponents.com.
3. Micrel, Inc.: www.micrel.com.
4. In DC-coupled mode, C6-C13 are 0Ω resistors.
5. In AC-coupled mode, R1-R8 are 50Ω for a 2.5V system, and 100Ω for a 3.3V system. In addition, in DC-coupled mode R1-R8 are unmounted.

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