SV6P6418 series

64M Sync Burst CCRAM

Version 1.1

Mar. 29, 2005

Revision History	Date	Revision Items
Rev 1.0	2004.11.25	Initial
Rev 1.1	2005.03.29	- Improved the TTL standby current from 0.5mA to 0.3mA - Changed the Standby current from 150uA to 250uA

Contents

64M(4M x 16bit) Asynchronous Page / Synchronous Burst Mode
CompactCell™ SRAM for cost sensitive, mobile applications

1. Description

The SV6P6418 is a 64Mb high speed, low power Pseudo SRAM organized as 4,194,304 words by 16bits and supports synchronous burst read/write, asynchronous page mode, and deep power down. In addition, the SV6P6418 family of PSRAM are available for both 1.8V and 3.0V supply voltage and I/O voltage applications. The SV6P6418 is a Pseudo SRAM based on successfully proven *Silicon7 CompactCell® SRAM* which was specifically developed for cost sensitive, low power computing and communication applications such as mobile cellular phone handsets, personal digital assistants and other battery-operated consumer products.

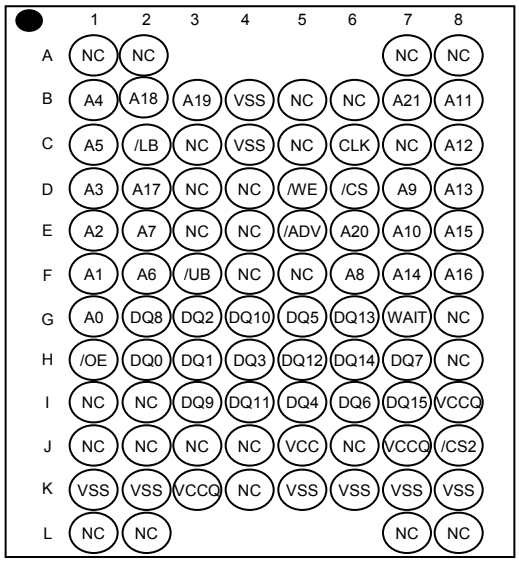
1.1 PRODUCT Features

- 4M X 16 Bit organization
- Selective operation of asynchronous and synchronous access
- High performance asynchronous access
  - 70/85ns Random Access Speed
  - 25/30ns Page Mode Read Speed
  - 16 words Page Mode Read
- Configuration Register set
  - Bus Configuration Register(**BCR**)
  - Refresh Configuration Register(**RCR**)
- High performance Synchronous access
  - Burst frequency at 104/80/66MHz
  - 36ns Initial Access Read / Write Speed at 104MHz
  - 4,8,16 word and continuous Burst Mode Read / Write
  - Burst Suspend feature
- 8, 16, and 32Mbit Partial Refresh Density
- Supply Voltage (1.8V/3.0V)
- Deep Power Down
- Tri-state Output and TTL Compatible
- 8, 16, and 32Mbit Partial Refresh Density
- Pb-free

PRODUCT FAMILY

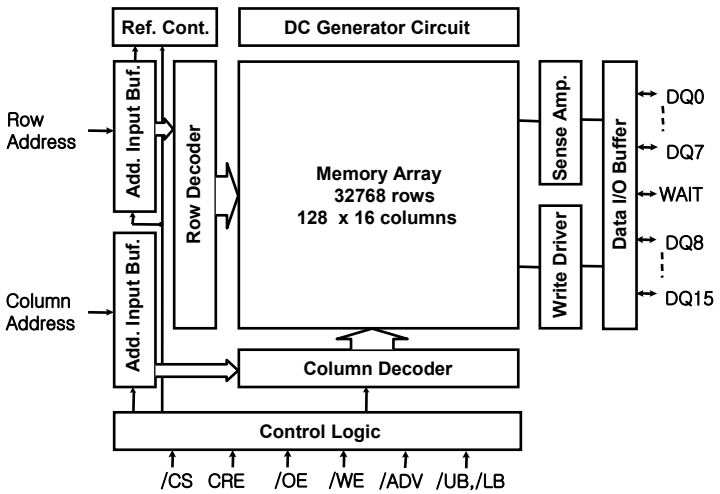
Product Family	Operating Temperature	Operating Voltage		Speed		Standby Current (Isb),Max	Operating Current (Icc),Max
		Core Voltage (VCC)	I/O voltage (VCCQ)	Async. Access Time	Sync. Frequency		
SV6P6418UFA-703P	-25 ~ 85 ℃	2.7V ~ 3.1V	2.7V ~ 3.1V	70ns	104/80MHz	250uA	3mA
SV6P6418UFA-851P				85ns	66MHz		
SV6P6418RFA-703P		1.7 ~ 1.95V	1.7 ~ 1.95V	70ns	104/80MHz		
SV6P6418RFA-851P				85ns	66MHz		

Fig.1 Ball Assignments 88-Ball FBGA (Top view)



Note: See table 1 for Pin Description Tables.
See figure 41 for 88-ball mech

Fig.2 Functional Block Diagram



1.2 Pin Descriptions

Table 1 : Pin Descriptions

Symbol	Type	Name and Function
A[21:0]	I	**ADDRESS INPUTS** : For memory address. The address lines are also used to define the value to be loaded into the Bus Configuration Register or the Refresh Configuration Register.
D[15:0]	I/O	**DATA INPUTS / OUTPUTS** : Input data during write cycles; output data during reads; tri-state when chip is deselected.
/ADV	I	**ADDRESS VALID** : /ADV indicates valid address presence on address inputs. During synchronous operations, all addresses are latched on /ADV's rising edge or CLK's rising(or falling) edge, whichever occurs first.
/CS	I	**CHIP ENABLE** : Asserting /CS activates internal control logic, I/O buffers, decoders, and sense amps. De-asserting /CS deselects the device, places it in standby mode, and tri-state all outputs
CLK	I	**CLOCK** : CLK synchronizes the device to the system bus frequency during synchronous operations and increments an internal address generator.
/WE	I	**WRITE ENABLE** : Determines if a given cycle is a write cycle. If /WE is low, The cycle is a write to either a control register or the memory array.
/OE	I	**OUTPUT ENABLE** : When asserted . /OE enables the device's output data buffers during a read cycle. When /OE is deasserted, data outputs are placed in a high-impedance state. /OE pin only have an effect on data outputs asynchronously. It has no effect of the device internal functions.
CRE	I	**CONFIGURATION REGISTER ENABLE** : When CRE is high, write operations load the refresh control register or bus control register.
/UB,/LB	I	**Byte Control** : When only /LB is in select mode, DQ0-DQ7 are affected. When /UB is in select mode, DQ8-DQ15 are affected.
WAIT	O	**WAIT** : Provides data valid feedback during burst read and write operations. The signal is gated by /CS. WAIT is used to arbitrate collisions between refresh and read/write operations. WAIT is asserted when a burst crosses a row boundary. WAIT is also used to max the delay associated with opening a new internal page. WAIT asserted and should be ignored during asynchronous and page mode operations.
VCC	Pwr	**DEVICE POWER SUPPLY**
VCCQ	Pwr	**I / O POWER SUPPLY**
VSS	Pwr	**GROUND**
VSSQ	Pwr	**I / O GROUND**
DNU		**Do not use**

1.3 TRUTH TABLE

Table 2 : Asynchronous Mode

CRE	/CS	/WE	/OE[7]	/UB&/LB	CLK	/ADV	WAIT	I/O 0~15	MODE	Power
L	L	H	L	L[1]	X	X	High-Z	Data-out	Async. read	Active[3]
L	L	L	X	L[1]	X	X	High-Z	Data-in	Async. write	Active[3]
L	H	X	X	X	X	X	High-Z	High-Z	Standby[2]	Standby
H	L	L	X	X	X	X	High-Z	High-Z	Async. Register set	Active[3]
X	H	X	X	X	X	X	High-Z	High-Z	Deep power down	DPD[8]

Table 3 : Synchronous Mode

CRE	/CS	/WE	/OE[7]	/UB&/LB	CLK	/ADV	WAIT	I/O 0~15	MODE	Power
L	L	H	L	L[1]	L	L	V	Data-out	Async. read	Active[3]
L	L	L	X	L[1]	L	L	V	Data-in	Async. write	Active[3]
L	H	X	X	X	X	X	High-Z	High-Z	Standby[2]	Standby
L	L	H	L	L[1]	T	L	V[9]	Data-out	Init burst read	Active[3]
L	L	L	H	X	T	L	V[9]	Data-in	Init burst write	Active[3]
L	L	X	L	L	T	H	V[9]	Data-in or Data-out	Burst continue	Active[4]
L	L	X	X	X	L	X	V[9]	Maintain prior state or High-Z	Burst suspend[5]	Active[6]
H	L	L	X	X	T	L	High-Z	High-Z	Sync. Register set	Active[3]
X	H	X	X	X	L	X	High-Z	High-Z	Deep power down	DPD[8]

** : X means don't care. (Must be low or high state). T means Toggle of CLK pin.
V means Valid output.

Note.

1. *When /UB and /LB are selected (LOW), DQ0-DQ15 are affected as shown. When only /LB is selected, DQ0-DQ7 are affected as shown. When only /UB is selected, DQ8-DQ15 are affected as shown.*
2. *When device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.*
3. *The device will consume active power in this mode.*
4. *The device will consume synchronous burst operation power in this mode.*
5. *The device will maintain prior state in this mode. If the clock is not toggled during the burst operation, the device will not execute any internal operations until the clock resumes. Even in burst suspend mode, Data outputs can be controlled by /OE pin since /OE control is asynchronous.*
6. *The device will consume synchronous active standby power in this mode.*
7. */OE pin have only an effect on the data outputs asynchronously. It has no effect of the device internal functions.*
8. *Deep Power Down is entered by the register setting and maintained until control register is reprogrammed to disable DPD control register(RCR A4)*
9. *The WAIT state is become high-Z state when the device is operated in fixed latency mode.*

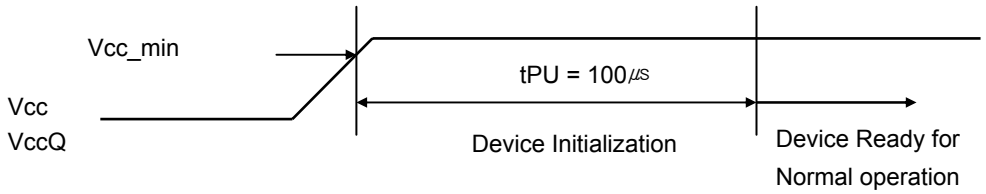
2. Functional Description

The SV6P6418x device contains 67,108,864 bits organized as 4,194,304 address X 16 bits. The 64M Compact Cell SRAM bus interface supports both asynchronous and synchronous mode transfers. Page mode accesses are also included for a high speed operation of asynchronous mode.

2.1 Power-up Sequence

The SV6P6418x products include an on-chip voltage sensor used to launch the power-up initialization process. Initialization will configure the Bus Configuration Register (BCR) and Refresh Configuration Register (RCR) with their default settings. VCC and VCCQ must be applied simultaneously. Once they reach a stable level above Vcc_min, the device will require 100us to complete its self-initialization process. Immediately after device power-up, the SV6P6418x is set to asynchronous mode by default so asynchronous mode timing should be used to set the Configuration Registers following successful power-up. Refer to figure 3,4.

Figure 3: Power-Up initialization Timing



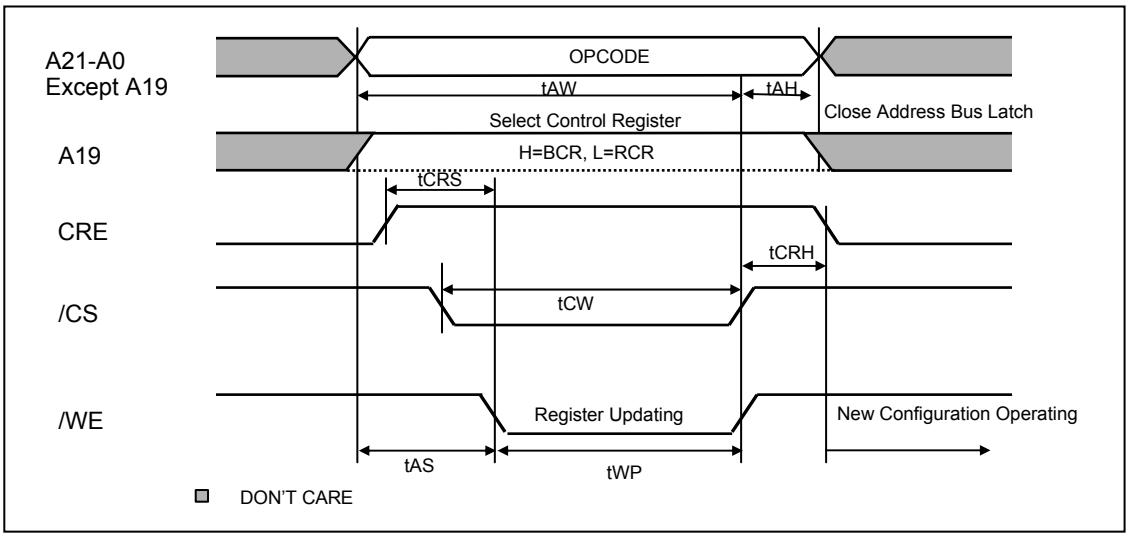
Note : VCC and VCCQ must be applied simultaneously. In case of 3V version device, an Initialization is started from 2.7V.

2.2 Configuration Register Setting Modes

The SV6P6418x products supports Asynchronous, Page Mode and Synchronous Burst Mode Bus Interface. In synchronous bus interface mode, the device also supports both Burst and Asynchronous bus interface incorporated CLK state. The specific interface supported is defined by the value loaded into the Configuration Register. Burst Mode is controlled by the Bus Configuration Register (BCR), and Page Mode is controlled by Refresh Configuration Register (RCR). The Configuration Register set can be only updated when the device is in idle state and no burst accesses are in progress.

Configuration Register Setting Timing

Fig. 4 Asynchronous Type Register Setting Timing (In Asynchronous Mode)

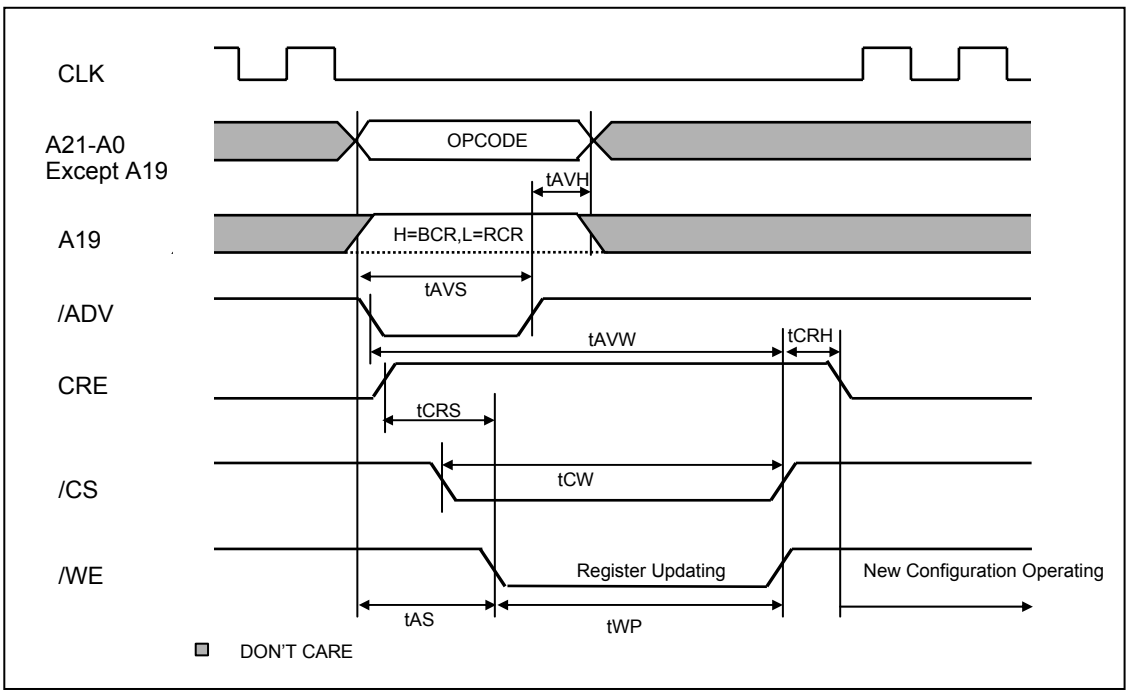


Note :

1. Prior to setting, Device must be set to the asynchronous mode(default).

2. All parameters have to meet conventional Write timing values.

Fig. 5 Asynchronous Type Register Setting Timing (Without Clock In Synchronous Mode)

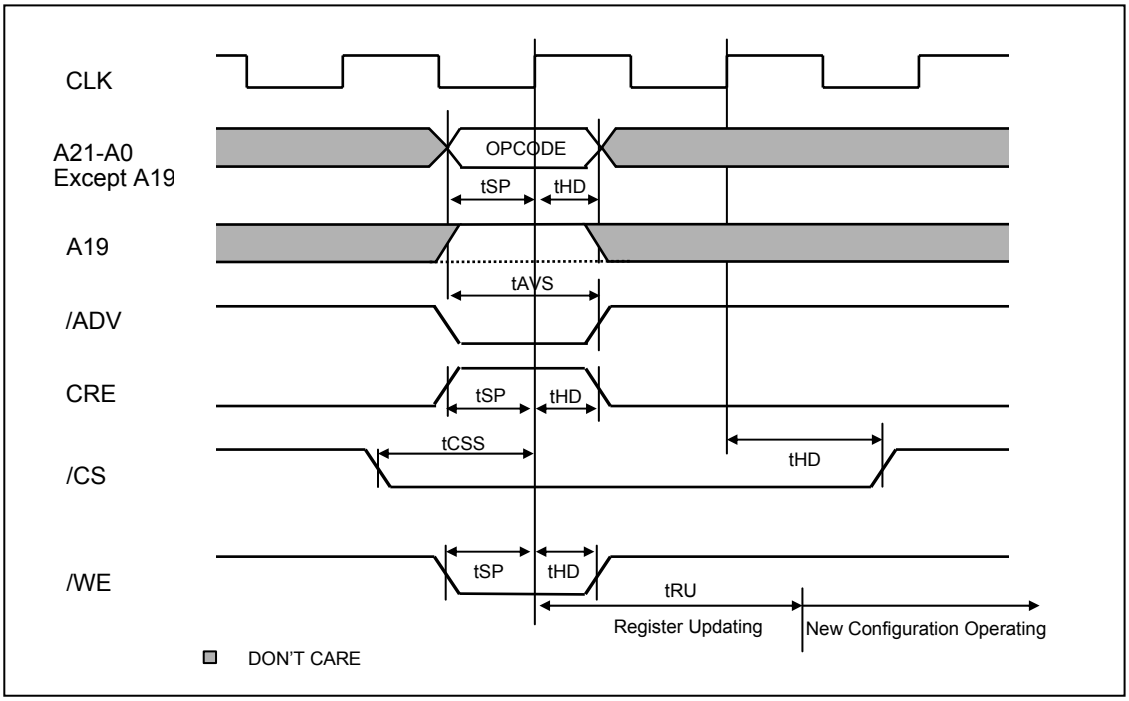


Note :

1. Prior to setting, Device must be set to the synchronous mode .

2. All parameters have to meet conventional Write timing values.

Fig. 6 Synchronous Type Register Setting Timing(With Clock)



Note :

1. Prior to setting, Device must be set to the synchronous mode .

2. All parameters have to meet conventional Write timing values.

Configuration Register Setting AC Characteristics (T = -25 to 85℃)

Table 4 : Timing Parameters –Configuration Register Setting

Parameter	Symbol	Speed 104/80/66MHz		Units
		Min	Max	
CRE setup time (to /WE=/CS=low)	tCRS	5		ns
CRE hold time (from /WE or /CS=high)	tCRH	0		ns
/ADV low setup to Write End	tAVW	65		ns
/CS low setup to CLK	tCSS	5	20	ns
Register Update time	tRU	20		ns

Note :

1. Prior to setting, Device must be in idle state.

2. Unspecified parameters have to meet conventional Write timing values.

Software Access Mode for Configuration Register Setting

Software access of the configuration registers used a sequence of asynchronous READ and WRITE operations. The contents of the configuration registers can be read or modified using the software access sequence.The configuration registers are loaded using a four step sequence consisting of two asynchronous READ operations followed by two asynchronous WRITE operations (refer to figure 7). The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (refer to figure 8). The address used during all READ and WRITE operations is the highest address of the device(3FFFFFh). The contents of this address are not changed by using this sequence. The data value presented during the third operation(WRITE) in the sequence defines whether the BCR or the RCR is to be accessed. The use of the software access sequence does not affect the ability to perform the standard (CRE-controlled) method of loading the configuration registers. However, the software nature of this access mechanism eliminates the need for the control register enable(CRE) pin. If the software mechanism is used, the CRE pin can simply be tied to Vss.

Fig. 7 Write Configuration Register CRE, /UB,/LB & /OE = V_{IL}

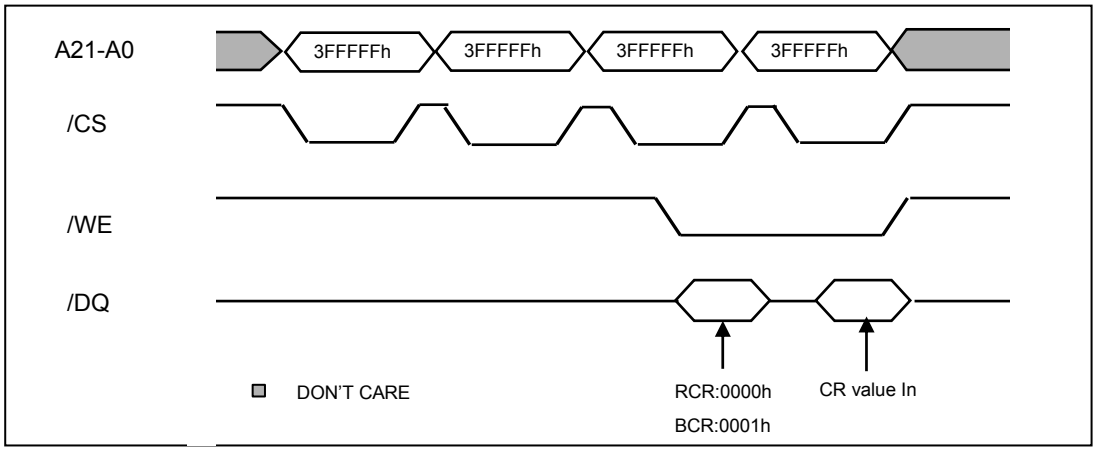
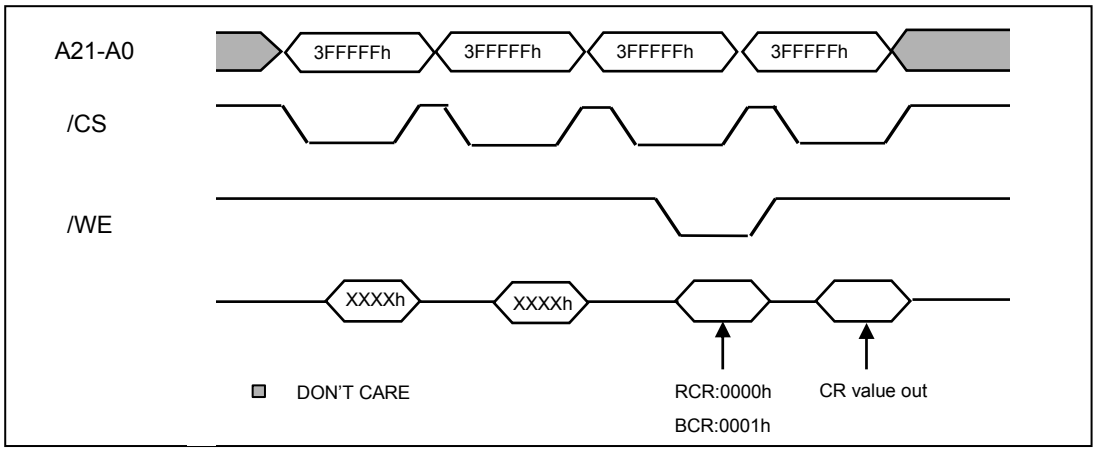


Fig. 8 Read Configuration Register CRE, /UB,/LB & /OE = V_{IL}



Note :

1. If the device is operating in synchronous mode, the CLK and /ADV pins must be held in V_{IL} level.

2.3 Asynchronous Modes

The SV6P6418x products power-up in the asynchronous operating mode by default. This mode uses the standard SRAM control bus (/CS, /WE, /OE, /UB, /LB, CRE). During asynchronous operation, the CLK and /ADV inputs have no effect of the device operation, and the WAIT pin is maintained in high-Z state. READ operations are initiated by bringing /CS low while keeping /WE high. Address Control READ operations are also initiated by changing addresses. Valid data will be driven out of the I/O pins after the specified access time has elapsed(refer to fig.9). WRITE operations are initiated by /CS,/UB,/LB and /WE low and terminated by /CS,/UB,/LB or /WE high (whichever occurs first). Refer to figure 10.

Single Asynchronous Read/Write Modes

Fig. 9 Read Operation Timing(/WE=V_{IH},CRE=V_{IL}**)**

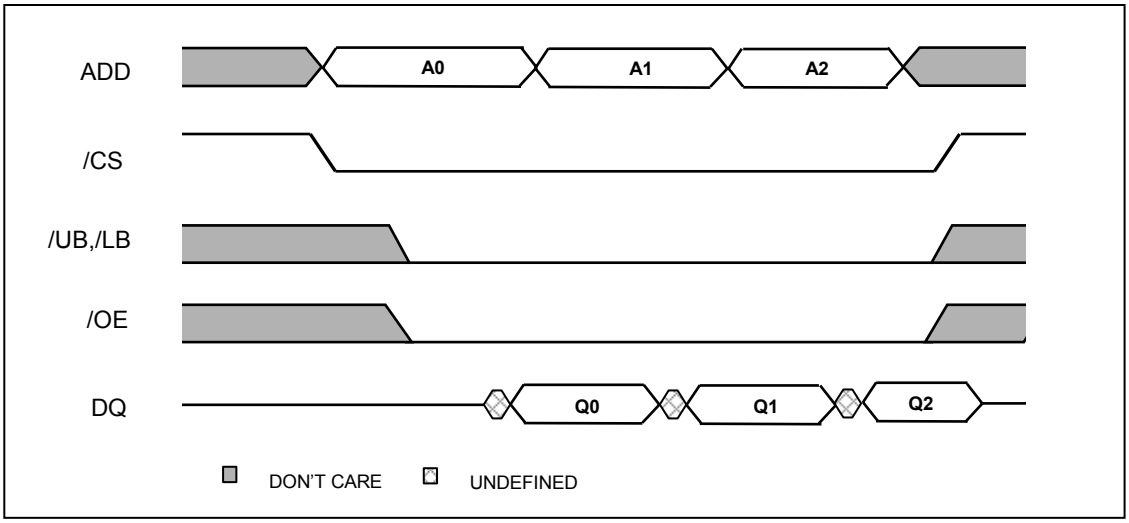
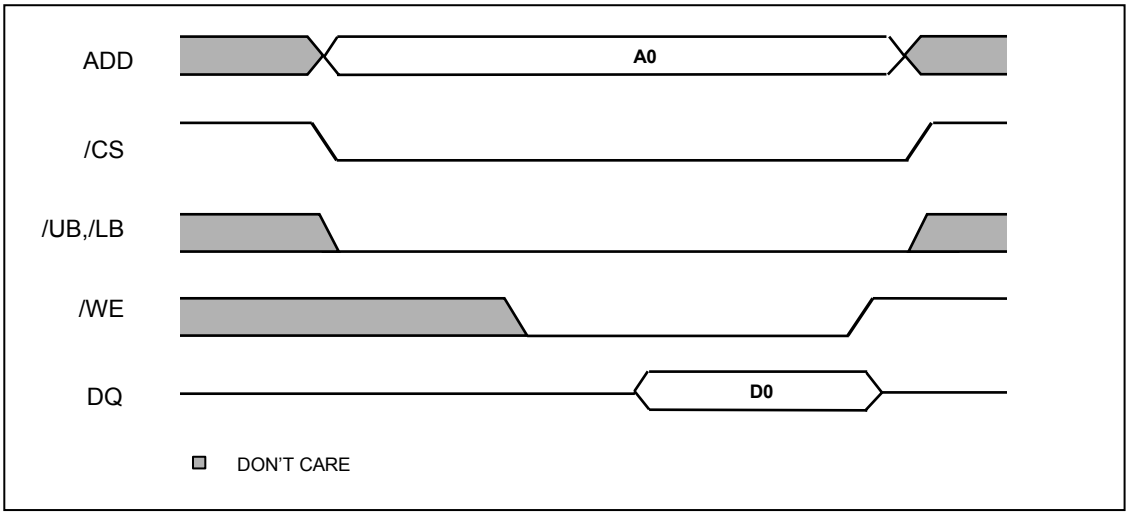


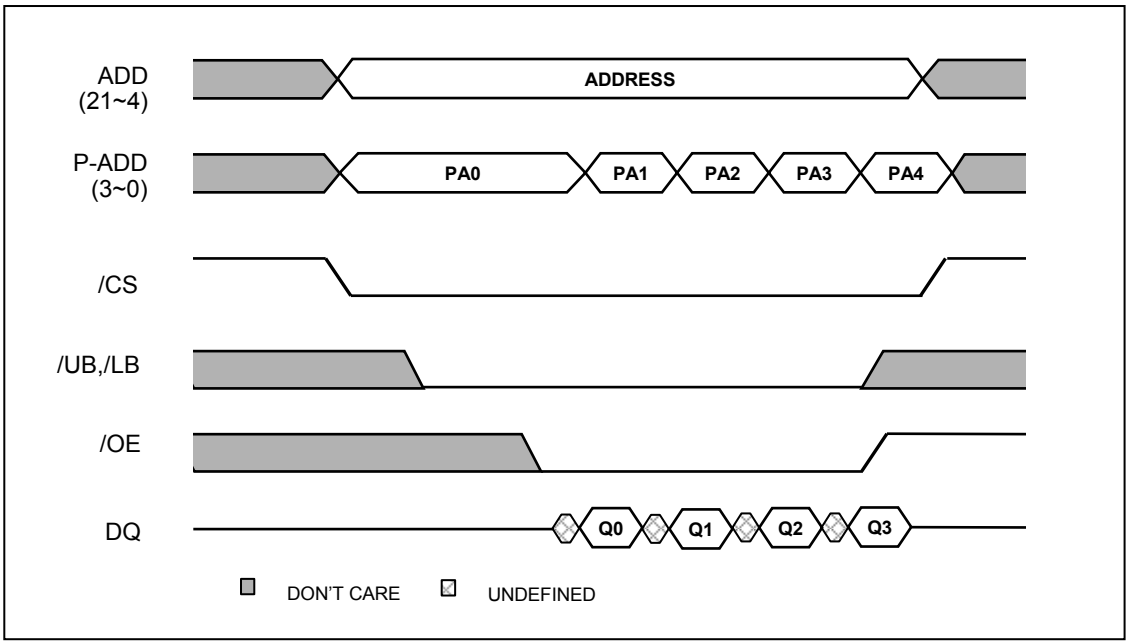
Fig. 10 Write Operation Timing (/OE=V_{IH},CRE=V_{IL}**)**



2.4 Page Modes (Read Only)

Page mode support 16-word page length and is only issued in asynchronous mode setting. The A0-A3 inputs are used to determine the members of the 16-address products. Addresses higher than A3 must remain fixed during the entire page address access. Page mode takes advantage of the fact that adjacent address can be read in a shorter period of time than random addresses access. During asynchronous page mode operation, the CLK and /ADV inputs have no effect of the device operation. And the WAIT pin is retained in High-Z state. Refer to figure 11.

Fig. 11 Page Read Operation Timing (/WE=V_{IH},CRE=V_{IL})



Note :

1. *Page mode operation supports only read access.*
2. *The /CS pin must not be kept low longer than 10us. Otherwise ADD(4~21) must change at least once within 10us.*
3. *The register settings for page mode are ignored in synchronous mode.*
4. *If the page access crosses any 16-word boundary (any change in A4~A21), then a new random access cycle is initiated.*

2.5 Synchronous Modes

The device also supports synchronous operations for high rate data transactions. By appropriately setting the Configuration Register set (see section 2.2), the device can be operated in the synchronous mode. In synchronous mode, CLK, /ADV and WAIT pin are used to control synchronous operation such as burst read/write and burst suspend mode. The latency and burst length for read and write operations are programmable. Please note that the burst length of read and write can be different according to Configuration Register settings (see figure 19).

Burst Modes

Burst mode operations allow high speed synchronous READ and WRITE transactions. Burst mode is initiated when the device is set for Synchronous Mode by the Bus Configuration Register. Burst operations consist of a multi-clock sequence that must be performed in an ordered fashion. In contrast to Asynchronous Mode and Page Mode operation, CLK and /ADV inputs control the device, and the WAIT pin is driven while the device is enabled to indicate the availability of the device for valid data input or data output. When the device is deselected, the WAIT pin is kept at high-Z. Burst mode supports various burst lengths 4, 8 and 16 words and full address which can be set by the BCR. The latency cycles stored in the BCR defines how many clock cycles elapse before the initial data are transferred between the processor and this device in READ and WRITE operations. Two burst wrapping modes are supported. If the Wrap option is not enabled, the device inputs or outputs data from sequential addresses without regard to burst boundaries. When the Wrap option is enabled, the device inputs or outputs data within burst boundaries. Refer to figure 19 and table 5. Please note that the device outputs will not be at high-Z after end of the burst sequence. To put the device outputs at high-Z, /OE, /CS or UB,/LB control signals should be used.

Fig. 12 Burst Read Operation Timing(BL=4)

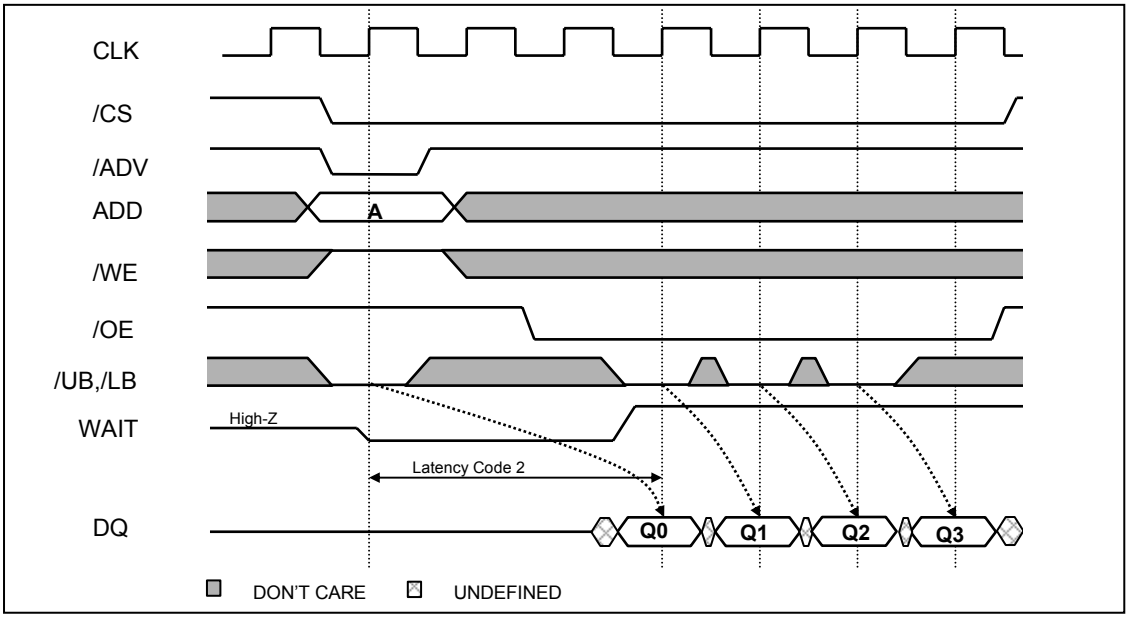
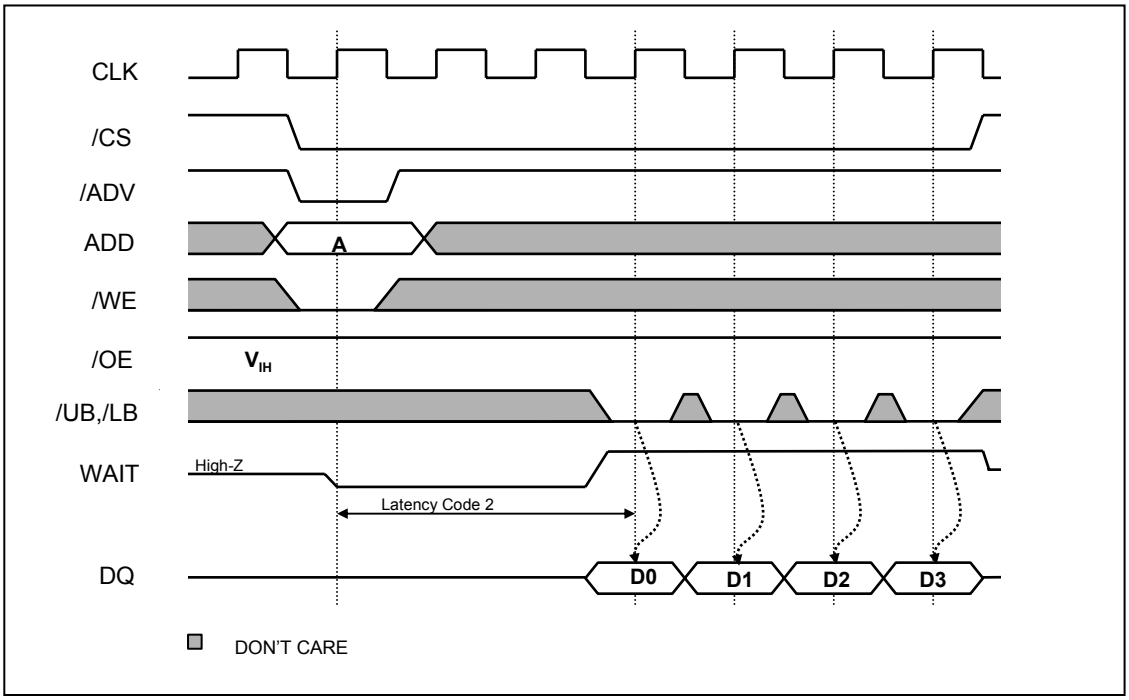


Fig. 13 Burst Write Operation Timing(BL=4)



Burst Suspend

The Burst suspend feature allows the system to temporarily suspend a synchronous burst sequence if the system needs to access the device or data bus for other purpose. This mode can suspend the burst operation during the initial latency (before the data is received) and after the device has output the data. While the burst access is suspended, internal array sensing still continues and any previously latched internal data is retained in read mode. Burst Suspend occurs when CLK is halted after /CS is asserted, the current address has been latched (either /ADV rising edge or valid CLK edge). Burst Suspend is released when CLK is resumed and the burst sequence continues where it left off with subsequent CLK edges (see figure 14,15).

Fig. 14 Burst Read Suspend Operation Timing(BL=4)

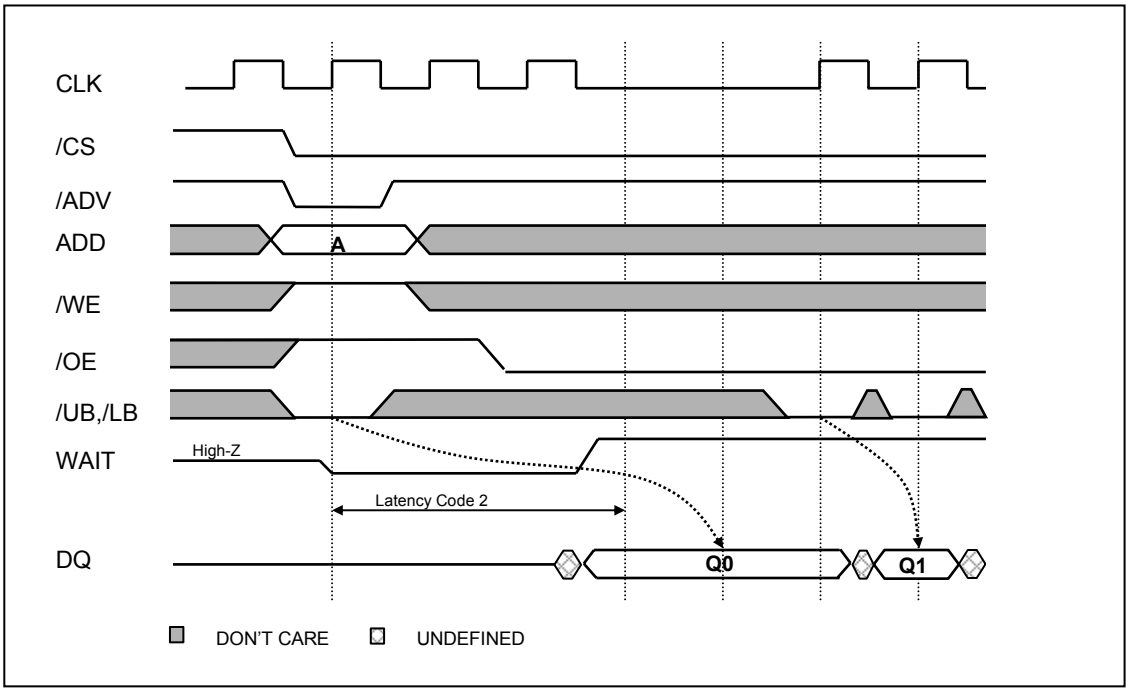
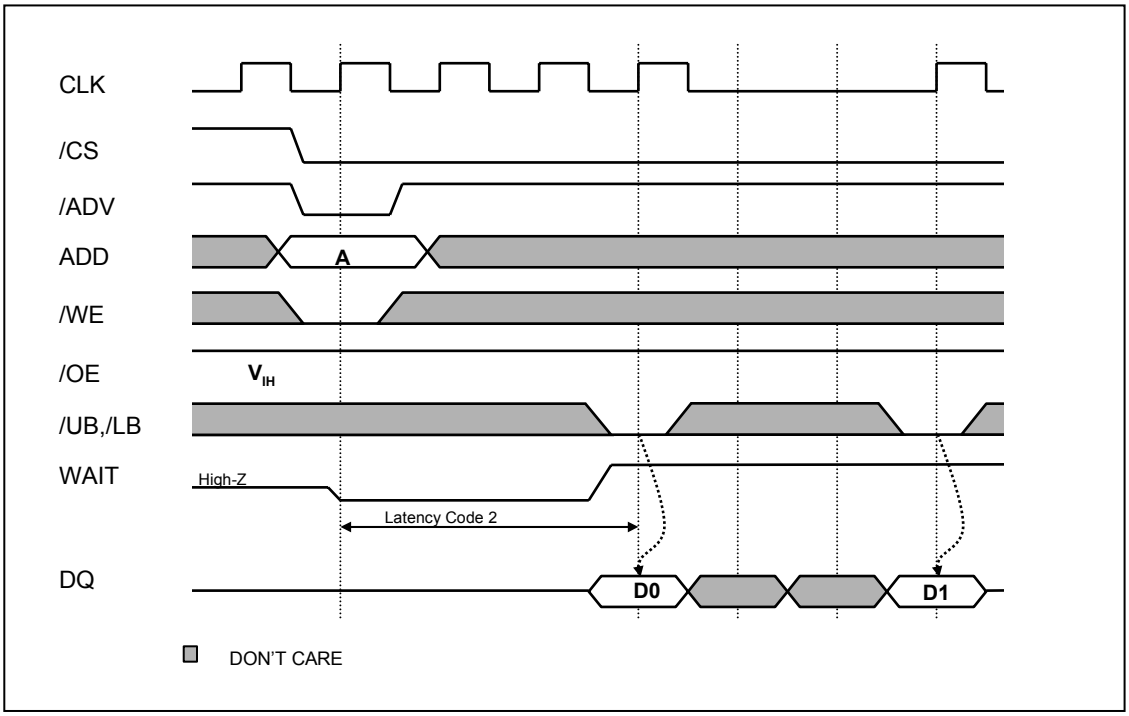


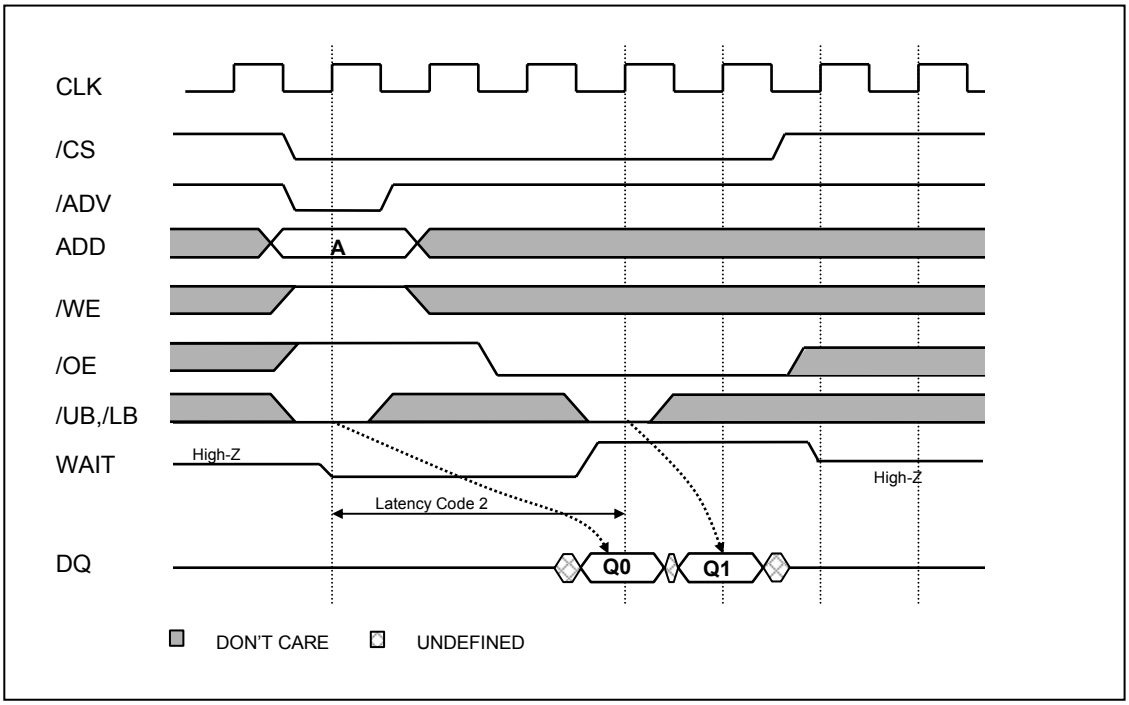
Fig. 15 Burst Write Suspend Operation Timing(BL=4)



Burst Stop

The Burst operations are only stopped by /CS high transition (any burst length). Refer to figure 16.

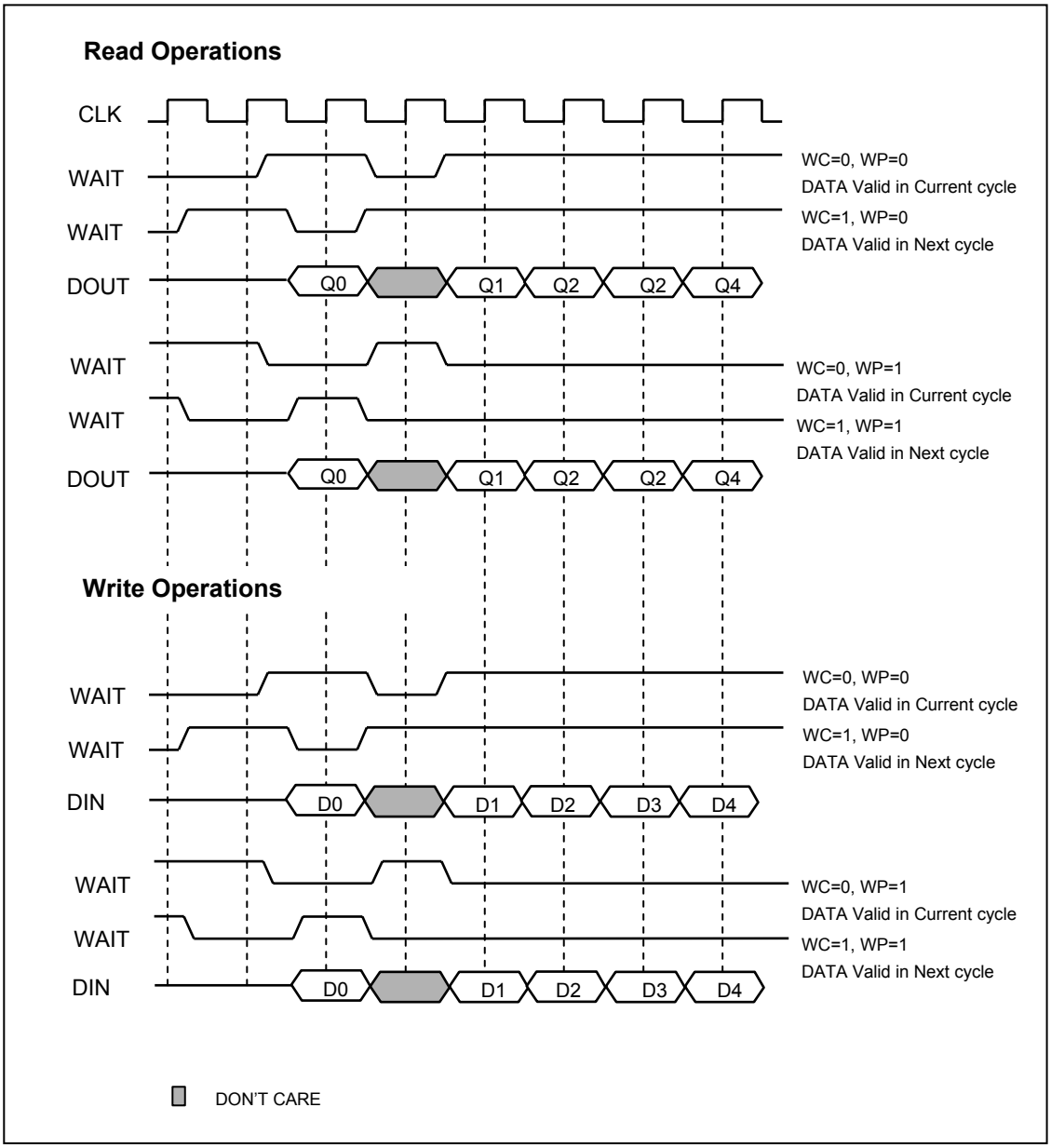
Fig. 16 Burst Stop Operation Timing(BL=Continuous)



WAIT

The WAIT pin on the products is connected to a shared system-level WAIT signal. The shared WAIT signal is used by the processor to coordinate transactions with multiple memories on the synchronous bus. When the device is set to Asynchronous Mode by the Configuration Register, the WAIT pin will be kept at high-Z. If the device is set to Synchronous Mode, the WAIT pin performs an arbitration role when the device requires additional time before data can be transferred or when a READ or WRITE operation is launched while an on-chip refresh is in progress. For READ operations, the WAIT pin will remain active until valid data is output from the device. For WRITE operations, WAIT will indicate to the memory controller when data will be accepted into the device. Once WAIT transitions to an inactive state, the data burst will progress on successive clock edge (refer to figure 17). If the device is used with Asynchronous timing (CLK halted) in Synchronous Mode, the WAIT pin will be driven asynchronously active when data is ready to be transferred. But If the device is set to fixed latency mode, the state of WAIT is always maintained the high-Z state.

Fig. 17 WAIT Operation Timing(BL=Continuous)



Standby Mode

Standby Operation occurs when the /CS pin is high and CRE pin is low and there are no transactions in progress. During Standby Mode, the device current consumption is reduced to the level necessary to perform the self refresh operation.

Deep Power Down Mode

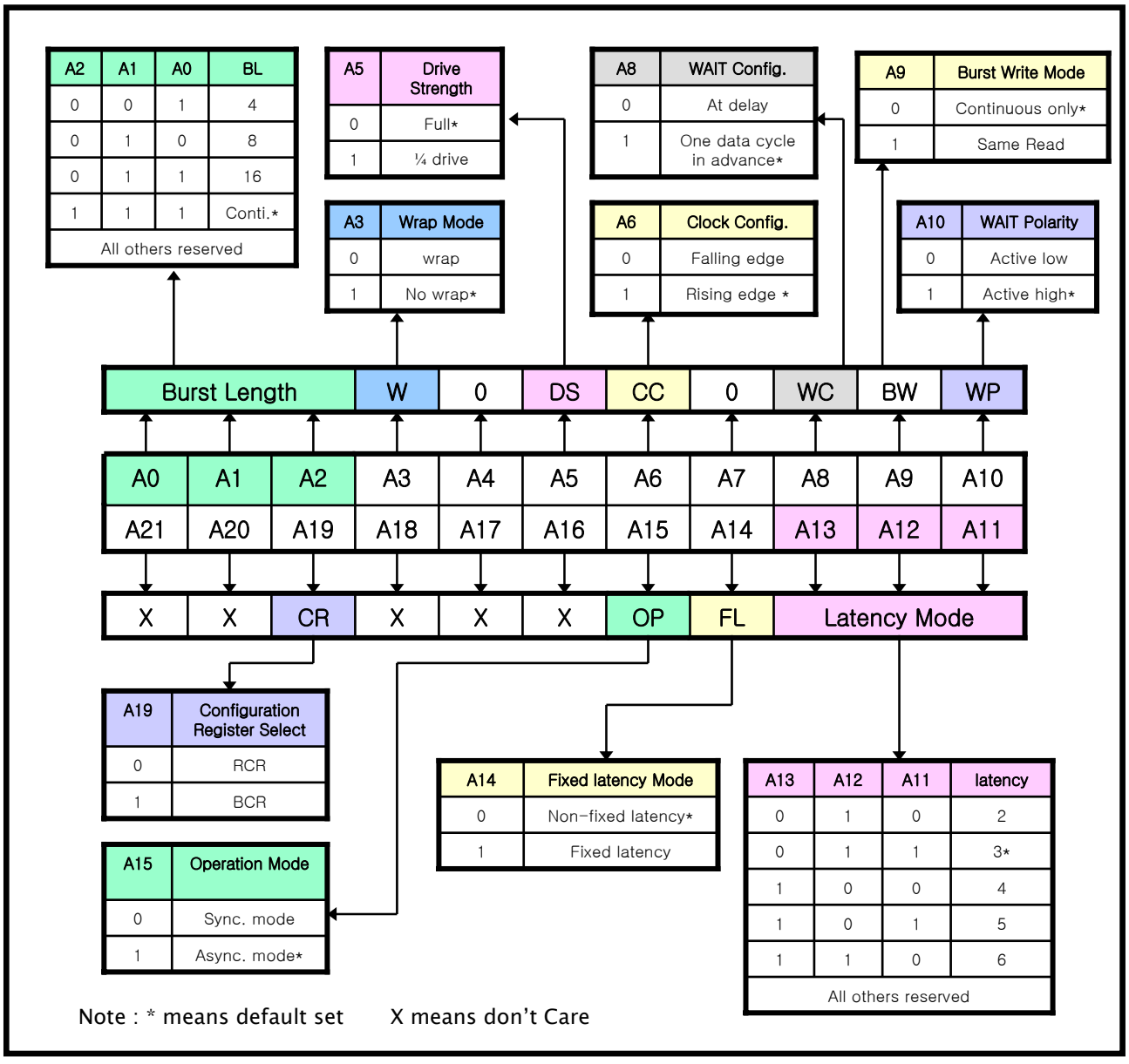
Deep Power Down (DPD) operation disables all refresh-related activity. Any stored data will become corrupted once the DPD is enabled. Only the register value of BCR and RCR are kept during DPD. This mode should only be used if the system does not require the storage provided by this device. Deep Power Down is entered by setting the Configuration Register and maintained until Control Register is reprogramming to disable DPD control register (RCR A4). Refer to figure 18.

2.6 The Configuration Register

There are two kinds of Configuration Register set. The first is the Bus Configuration Register (BCR) set. The second is the Refresh Configuration Register(RCR) set. The BCR is specifies the interface configurations. The RCR permits additional saving of standby power by making use of Temperature Compensated Self-Refresh (TCSR), Partial Array Self-Refresh (PASR) and Deep Power Down (DPD) features. In case of setting the device by software access, the data(D0~D15) substitute for the address(A0~A15) except A19. Refer to figure 7,8.

2.6.1 Bus Configuration Register Mapping

Fig.18 Bus Configuration Register Map



Burst Length

Via the burst length field the user can select between fixed burst lengths of 4, 8, 16 and any arbitrary burst length by choosing the continuous mode option. In continuous mode the burst length is controlled by the active period of the /CS low. The burst length of the write cycle is different from the read cycle when the BW(A9) register is set to 0(default). In this case the burst write mode is always continuous independent of the burst length setting. If the BW(A9) register is set to 1, the burst lengths of the write cycle are same as the read cycle(refer to figure 18). And the continuous mode is not supported during the device is operating in fixed latency mode. In asynchronous mode, BW(A9) has no effect on device operations.

Wrap Mode

Wrap mode defines whether there is a wrap around within a burst access or not (default no wrap). Refer to table 4. In asynchronous mode, wrap mode has no effect on device operation.

Table 4 : Sequence and Burst Length

Starting Address (Decimal)	Wrap (A3)	BL=4	BL=8	BL=16	BL=Continuous
0	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7- 8-9-10-11-12-13-14-15	0-1-2-3-4-------
1	0	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8- 9-10-11-12-13-14-15-0	1-2-3-4--------
2	0	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9- 10-11-12-13-14-15-0-1	2-3-4-5-6-------
3	0	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10- 11-12-13-14-15-0-1-2	3-4-5-6-7-------
5	0	5-6-7-4	5-6-7-0-1-2-3-4	5-6-7-8-9-10-11-12- 13-14-15-0-1-2-3-4	5-6-7-8-9-------
9	0	9-10-11-8	9-10-11-12-13-14-15-8	9-10-11-12-13-14-15-0- 1-2-3-4-5-6-7-8	9-10-11-12------
0	1	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7- 8-9-10-11-12-13-14-15	0-1-2-3-4-------
1	1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5-6-7-8- 9-10-11-12-13-14-15-16	1-2-3-4--------
2	1	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6-7-8-9- 10-11-12-13-14-15-16-17	2-3-4-5-6-------
3	1	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7-8-9-10- 11-12-13-14-15-16-17-18	3-4-5-6-7-------
5	1	5-6-7-8	5-6-7-8-9-10-11-12	5-6-7-8-9-10-11-12- 13-14-15-16-17-18-19-20	5-6-7-8-9-------
9	1	9-10-11-12	9-10-11-12-13-14-15-16	9-10-11-12-13-14-15-16- 17-18-19-20-21-22-23-24	9-10-11-12------

Note : In mode of continuous burst length, device doesn't stop the burst operation until /CS disable.

Driver Strength

For adaptation to different system characteristics the output driver strength can be configured (default full strength).

Clock Configuration

The clock configuration means if the device operations are synchronized and referenced to the rising or falling edge of clock (default rising edge). In asynchronous mode, this has no effect of device operations.

WAIT Configuration

The WAIT Configuration specifies whether the WAIT signal is asserted at the time of the delay or whether it is asserted one clock cycle in advance (default is one clock in advance). Refer to figure 17. In asynchronous mode, this has no effect on device operations.

WAIT Polarity

The WAIT Polarity allows the user to define the polarity of the WAIT output signal. The WAIT output is only used for a synchronous mode. Refer to figure 17. In asynchronous mode, the WAIT signal is always kept in high-Z state.

Latency Mode

The Latency Mode determines how many clocks occur between the beginning of a read or write operation and the first data value transferred. For higher frequency device operation needs larger latency setting since the core internal operation of device is independent of the value of latency setting (default latency 3). Only latencies of two or three clocks are allowed. Refer to figure 19. In asynchronous mode, this has no effect on device operations.

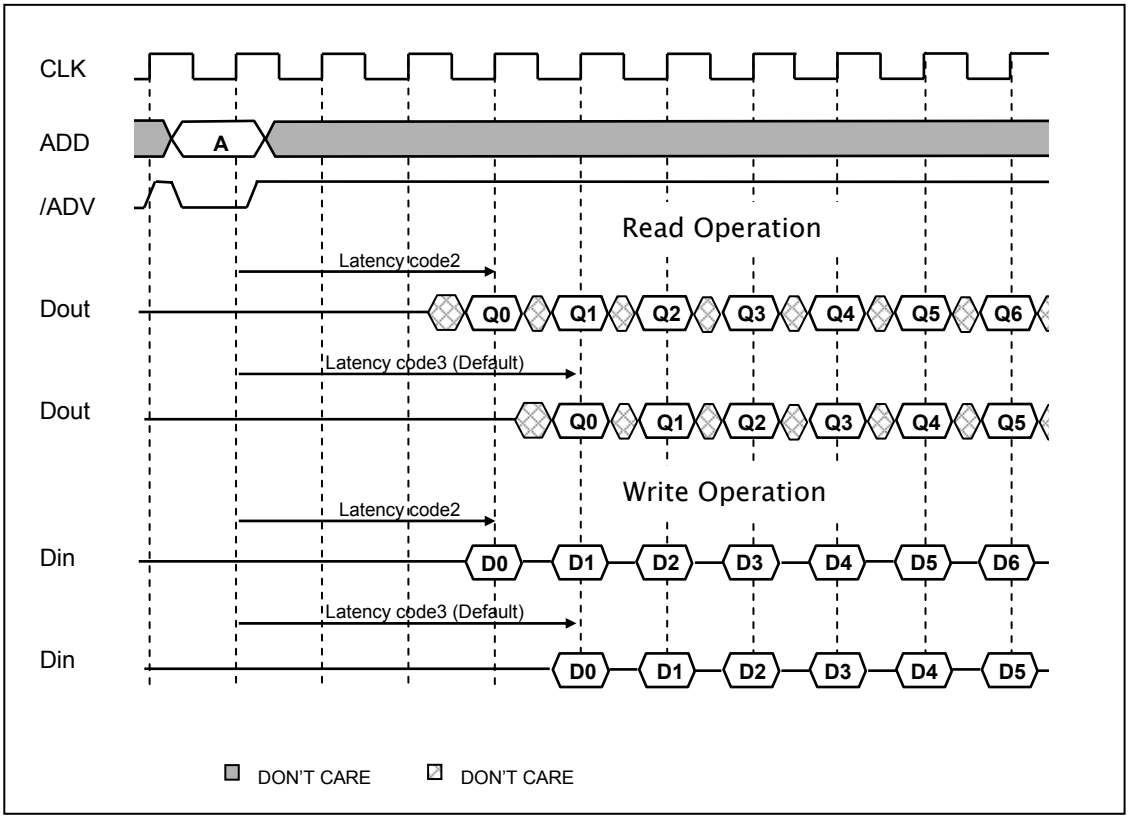
Fixed Latency Mode

The Fixed Latency Mode determines whether the device is controlled by WAIT pin state or not. In non-fixed mode, the device is operating with variable WAIT method (refer to figure 17). But in fixed latency mode, the device is always needed the fixed number of elapsed clock between the beginning of a read or write operation and the first data value transferred. The number of elapsed clock is depend on the number of set of Latency mode. In fixed latency mode, the state of WAIT pin will be kept at high-Z state. This mode is useful for simple controlling the device. But this mode support slower clock speed compare to the non-fixed latency mode. Refer to table 12. In asynchronous mode, this mode has no effect on device operations.

Burst Write Mode

The Burst Write Mode determines whether the burst sequences of write cycle are same as a read cycle or fixed at continuous sequence (default continuous). If the BL register is set to 8 and the BW register is set to 1, the write burst length will be eight words as the read cycle. In asynchronous mode, this has no effect on device operations.

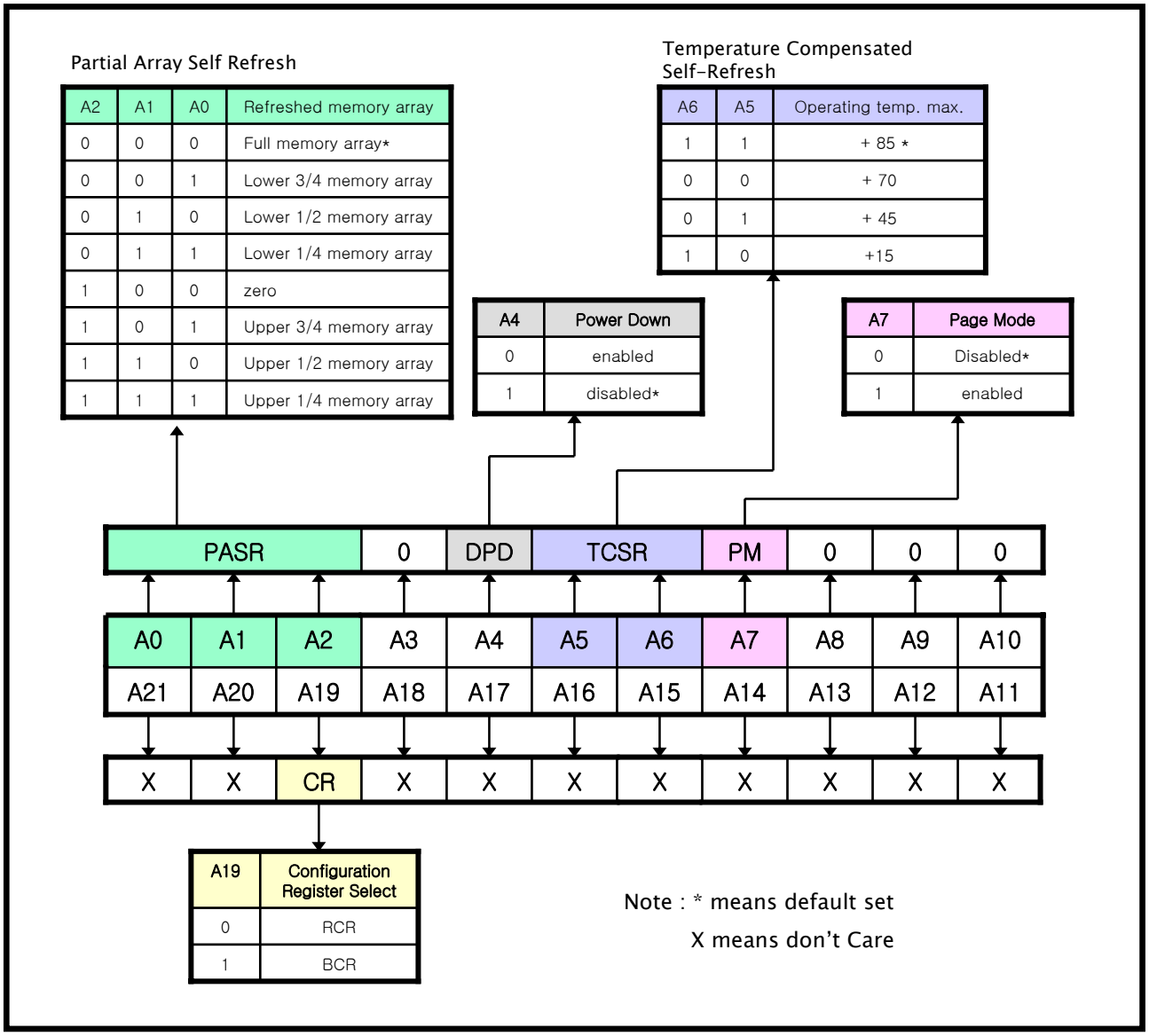
Fig.19 Latency Counter



2.6.2 Refresh Configuration Register Mapping

The Refresh Configuration Register (RCR) permits additional saving of standby power by making use of the TCSR, PASR, DPD features. RCR can only be set when the device is in idle state.

Fig.20 Refresh Configuration Register Map



Partial Array Self-Refresh

Partial Array Self-Refresh (PASR) restricts refresh operation to a portion of the total memory. Only the active portion of the memory array will be periodically refreshed whereas the disabled parts will be excluded from refresh and previously stored data will be lost. Normal operation of disabled portions of the memory array are possible, but stored data are not guaranteed. Refer to table 5.

Table 5 : Memory Array Patterns for PASR

A2	A1	A0	Active array	Address space(h)	Organization	Density
0	0	0	Full array	000000-3FFFFF	4Mb X 16	64Mb
0	0	1	Lower 3/4 of memory array	000000-2FFFFF	3Mb X 16	48Mb
0	1	0	Lower 1/2 of memory array	000000-1FFFFF	2Mb X 16	32Mb
0	1	1	Lower 1/4 of memory array	000000-0FFFFF	1Mb X 16	16Mb
1	0	0	zero	0	0	
1	0	1	Upper 3/4 of memory array	100000-3FFFFF	3Mb X 16	48Mb
1	1	0	Upper 1/2 of memory array	200000-3FFFFF	2Mb X 16	32Mb
1	1	1	Upper 1/4 of memory array	300000-3FFFFF	1Mb X 16	16Mb

Deep Power Down Mode

The DPD mode puts the device in an extreme low power mode by stopping all internal device operations. Stored memory data is not retained in this mode.

Temperature Compensated Self-Refresh (TCSR)

The TCSR mode adjusts the refresh period internally to the actual environment temperature. DRAM cells require more frequent refresh rates at higher temperature. To guarantee data integrity over the full operating temperature range, the device has to be set higher refresh rate. Actually it waste system power on useless thing for normal range of operating temperatures. The TCSR is method to lower power consumption in case of low or medium temperatures.

Page Mode

The Page mode is only evoked in asynchronous mode. The device does not support an asynchronous page write mode in every mode and also does not support an asynchronous page read mode in synchronous mode. Although the device can be set for page mode and operated an asynchronous read mode (CLK fixed in low) in synchronous mode, the device will only access single words in asynchronous mode. During synchronous mode operation, the value of register (A7) is ignored. In asynchronous page mode, the user has the option to toggle A0-A3 in any way at a higher rate (20ns vs. 70ns) compared to initial access latency. However in page mode operation, the /CS pin must not be kept in low longer than 10us.

3. Electrical Characteristics

Absolute Maximum Ratings

Table 6 : Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}	−0.2 to V_{CC} +0.3 V	V
Voltage on V_{CC} supply relative to Vss	V_{CC}	−0.2 to 3.3	V
Voltage on V_{CCQ} supply relative to Vss	V_{CCQ}	−0.2 to 3.3	V
Soldering peak temperature (10s)		260	℃
Power dissipation	P_D	180	mW
Storage temperature	T_{STG}	−55 to 150	℃
Operating temperature	T_C	−25 ~ 85	℃
Short circuit output current	I_{OUT}	−50 ~ 50	mA

Note : Stresses greater than those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These rating are for stress only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS [1]

Table 7 : Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (1.8V version) [5]	V_{CC}	1.7	1.8	1.95	V
Supply Voltage(3.0V version) [5]	V_{CC}	2.7	2.9	3.1	V
Supply Voltage, 1.8 I/Os	V_{CCQ}	1.7	1.8	1.95	V
Supply Voltage, 3.0 I/Os	V_{CCQ}	2.7	2.9	3.1	V
Ground	Vss& Vssq	0	0	0	V
Input High Voltage	V_{IH}	1.4	-	Vcc+0.2 [2]	V
Input Low Voltage	V_{IL}	-0.2 [3]	-	0.4	V

Note :
1. TA = -25 ℃ to 85 ℃, otherwise specified.
2. Overshoot : Vcc + 0.5V in case of pulse width ≤ 10 ns.
3. Undershoot : -0.5V in case of pulse width ≤ 10 ns.
4. Overshoot and undershoot are sampled, not 100% tested.
5. Stable power supply required 100 us before device operation.

Pin Capacitances (T_A = 25 ℃, f = 1.0MHz)

Table 8 : Pin Capacitance

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} =0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} =0V	6	pF

Note : This parameter is sampled and not 100% tested

3.1 DC Characteristics and Test Conditions

Table 9 : DC and Operating Characteristics

Parameter	Symbol	Operation & Test Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc	-1	1	uA
Output Leakage Current	I_{LO}	/CS = V_{IH},CRE = V_{IL} or /OE=V_{IH} or /WE=V_{IL}, V_{IO}=Vss to Vcc	-1	1	uA
Asynchronous Operating Current	I_{CC}	Active Standby IIO=0mA, /CS = V_{IL}, V_{IN}=V_{IH} or V_{IL}		3	mA
	I_{CC2}	Active or Initial Page Access Cycle time=Min, I_{IO}=0mA, 100% duty /CS = V_{IL}, V_{IN}=V_{IL} or V_{IH}		20	mA
	I_{CCP}	Page Continuous Access Cycle time=Min, I_{IO}=0mA, 100% duty /CS = V_{IL}, V_{IN}=V_{IL} or V_{IH}		20	mA
Synchronous Operating Current	I_{CC3}	Active Standby I_{IO}=0mA, /CS = V_{IL}, V_{IN}=V_{IH} or V_{IL}		5	mA
	I_{CC4}	Initial Burst Access Cycle time=Min, I_{IO}=0mA, 100% duty /CS = V_{IL}, V_{IN}=V_{IL} or V_{IH}		35	mA
	I_{CC5}	Burst Continuous Access Cycle time=Min, I_{IO}=0mA, 100% duty /CS = V_{IL}, V_{IN}=VIL or V_{IH}		25	mA
Output Low Voltage	V_{OL}	I_{OL} = 0.2 mA		V_{DDQ}X0.2	V
Output High Voltage	V_{OH}	I_{OH} = -0.2 mA	V_{DDQ}X0.8		V
Standby Current(TTL)	I_{SB}	/CS=V_{IH} Other inputs = V_{IH} or V_{IL}		0.3	mA
Standby Current(CMOS)	I_{SB1}	/CS ≥ Vcc-0.2V Other inputs =V_{CC} or V_{SS}		250	uA
Deep Power Down Current	I_{DPD}	/CS ≥ Vcc-0.2V Other inputs=V_{CC} or V_{SS}		10	uA

Note : The specification assumes the output disabled.

Output Test Conditions

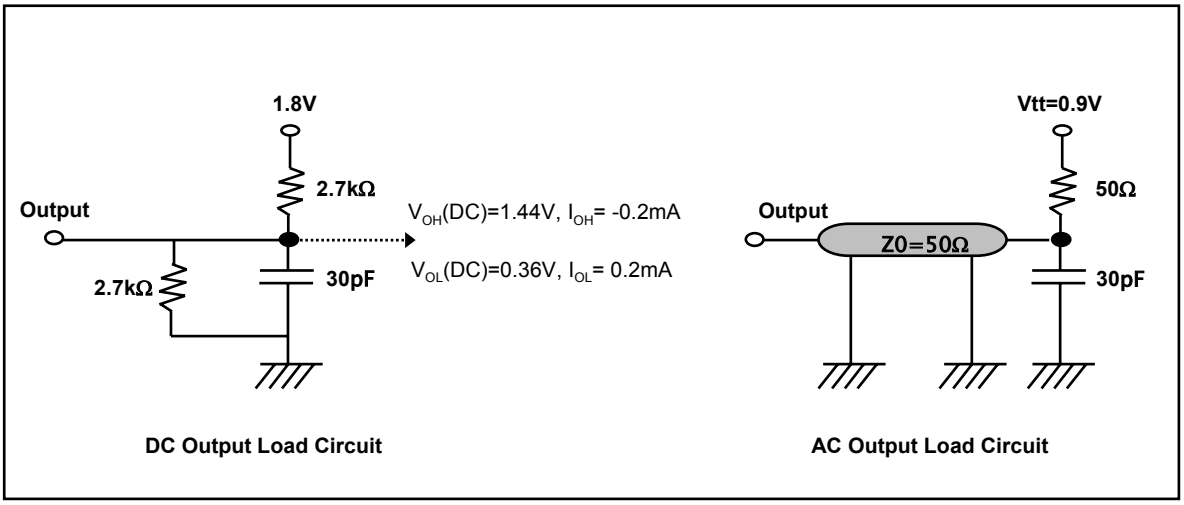
Table 10 : AC Output Test Conditions

PARAMETER	Value
Input Pulse Level	0.4V to 1.4V
Input Rise and Fall Time	1ns
Input and Output Measurement Reference Level	0.9V
Output Load Condition	See Fig.21

T_A = -25℃ to 85℃ (Normal), unless otherwise specified

Output Test Loads

Fig.21 Output Test Loads and conditions



Note :

1. Including jig and scope capacitance

2. AC inputs are driven at Vcc for a logic 1 and Vss for a logic 0. Input timing begins at Vcc/2, and output timing ends at VccQ/2.

3.2 Asynchronous AC Characteristics (T_A = -25 to 85℃)

Table 11 : Asynchronous AC Characteristics

Parameter List		Symbol	Speed Bins				Units
			70 ns(104/80Mhz)		85 ns(66Mhz)		
			Min	Max	Min	Max	
R E A D	Read cycle time	tRC	70		85		ns
	Address access time	tAA		70		85	ns
	Chip select access time	tCO		70		85	ns
	Output enable to valid output	tOE		20		25	ns
	/UB,/LB access time	tBA		20		25	ns
	/CS low to output Low-Z	tLZ	5		5		ns
	/UB, /LB low to output Low-Z	tBLZ	5		5		ns
	Output enable to output Low-Z	tOLZ	5		5		ns
	/CS high to output High-Z	tHZ	0	20	0	25	ns
	/UB, /LB high to output High-Z	tBHZ	0	20	0	25	ns
	Output disable to output High-Z	tOHZ	0	20	0	25	ns
	Output hold from address change	tOH	5		5		ns
	/CS pre-charge time	tCPH	5		5		ns
	Page read cycle time	tPRC	25		30		ns
	Page read address access time	tPAA		25		30	ns
W R I T E	Write cycle time	tWC	70		85		ns
	Chip select to end of write	tCW	65		80		ns
	Address valid to end of write	tAW	65		80		ns
	/UB, /LB valid to end of write	tBW	65		80		ns
	Write pulse width	tWP	50		60		ns
	Address set-up time	tAS	0		0		ns
	Write to output High-Z	tWHZ	0	20	0	25	ns
	Data to write time overlap	tDW	25		30		ns
	Data Hold from Write Time	tDH	0		0		ns
	End of Write to Output Low-Z	tOW	5		5		ns
	/CS pre-charge time	tCPH	5		5		ns

3.3 Asynchronous Timing Diagram

Fig.22 Single Read Cycle 1 (Address Controlled, /CS, /OE,/UB,/LB and CRE = VIL, /WE = VIH)

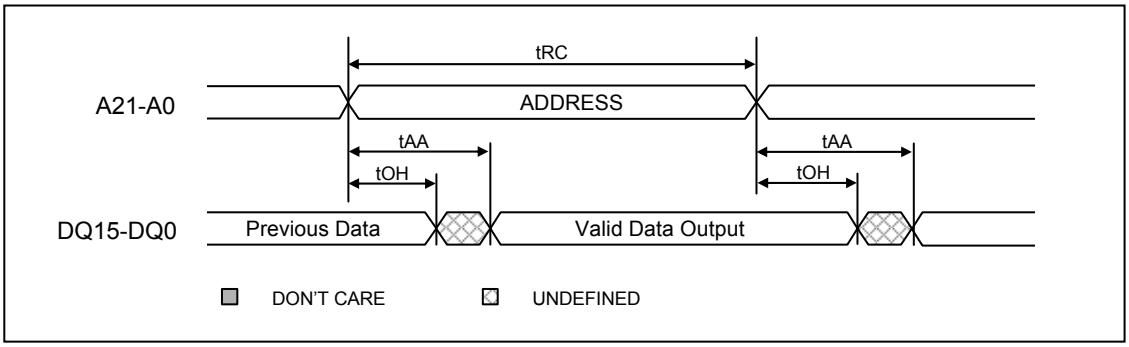
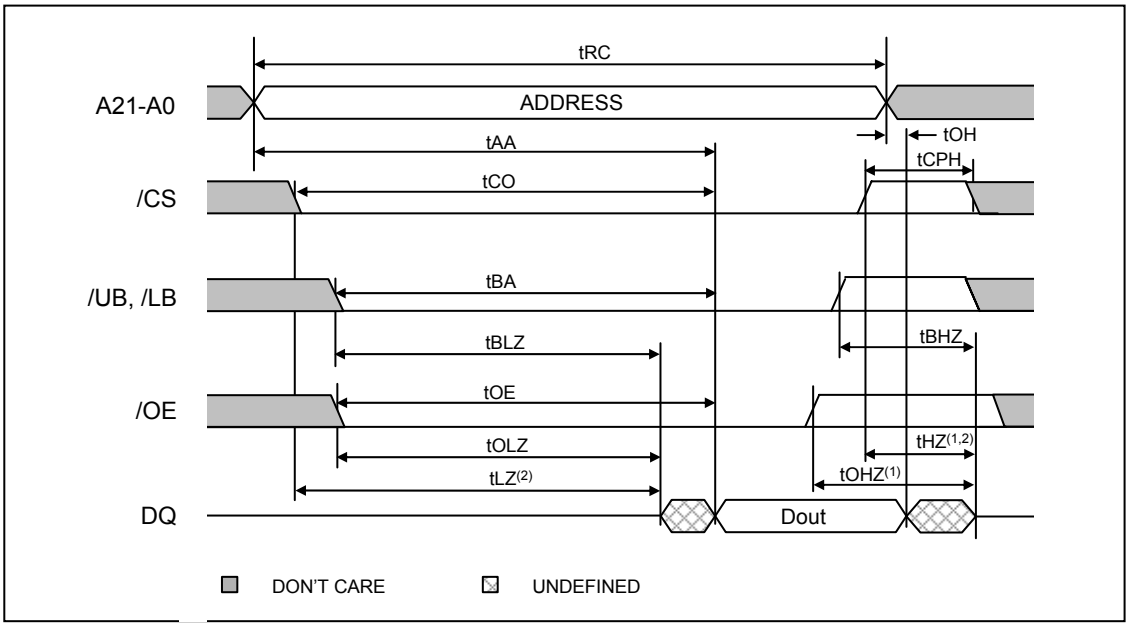


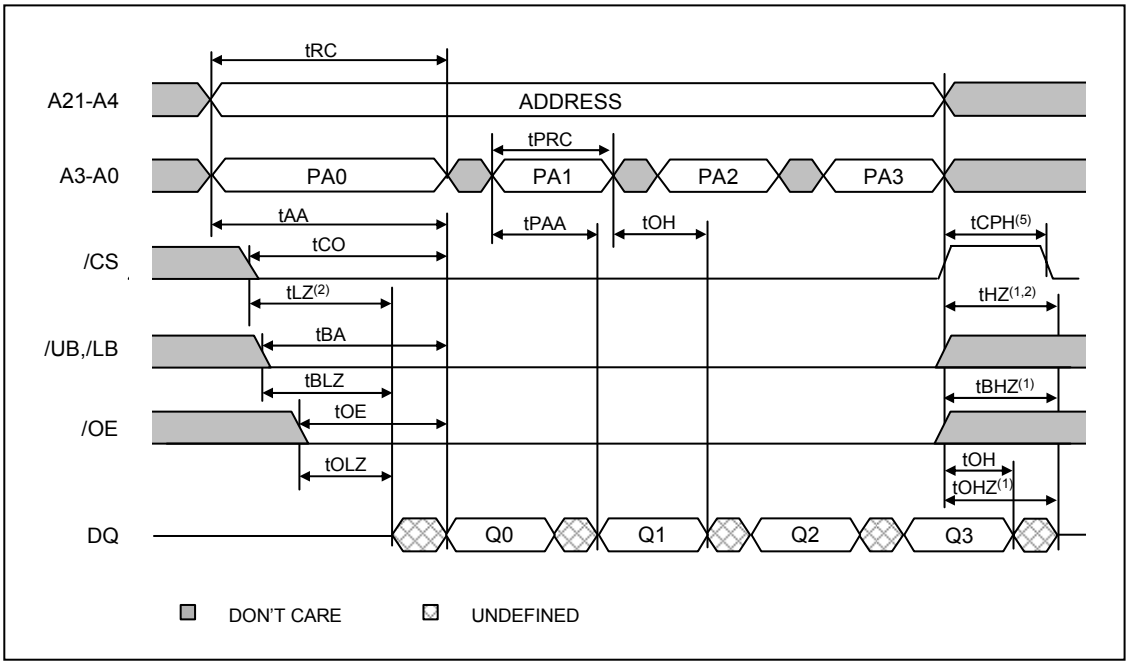
Fig.23 Single Read Cycle 2 (CRE = VIL , /WE = VIH)



Note (READ CYCLE) :

1. *tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced output voltage levels*
2. *At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.*
3. */WE is high for the read cycle.*
4. *Do not access device with cycle timing shorter than tRC for continuous periods > 10us.*
5. */ADV, CLK have no effect of the device operations.*
6. *WAIT pin is always kept in high-Z.*

Fig.24 Page Mode Read Cycle (CRE = VIL , /WE = VIH)



Note (PAGE MODE READ CYCLE) :

1. *tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels*
2. *At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.*
3. */WE is high for the read cycle.*
4. *Do not access device with cycle timing shorter than tRC for continuous periods > 10us.*
5. *tCPH (precharge time) should be guaranteed for new Address.*
6. *After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page.*
7. */ADV, CLK have no effect of the device operations.*
8. *WAIT pin is always kept in high-Z.*

Fig.25 Asynchronous Write Cycle 1 (/CS Controlled, CRE = VIL, /OE = don't care)

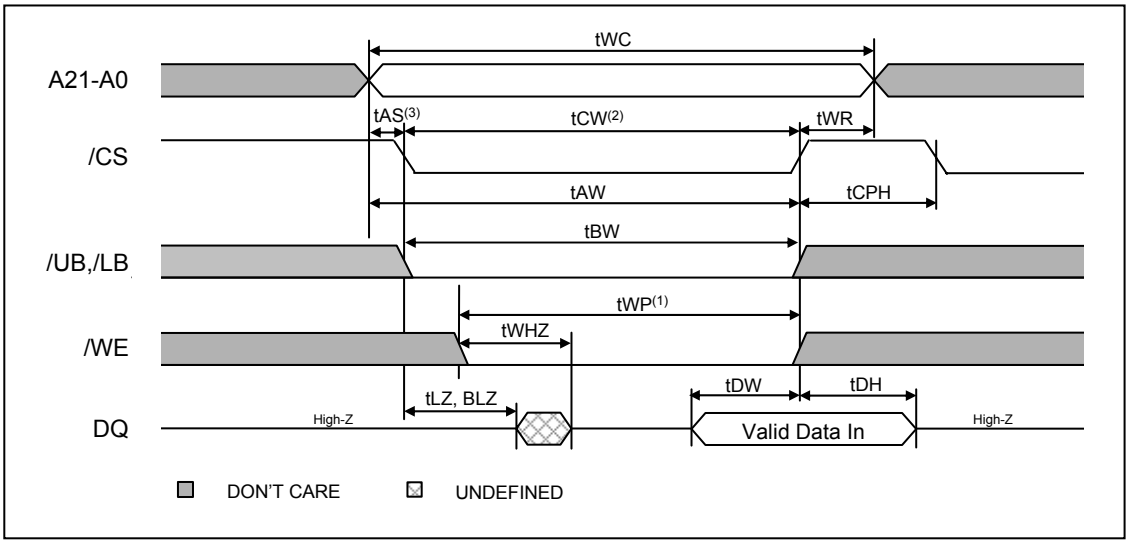


Fig.26 Asynchronous Write Cycle 2 (/UB, /LB Controlled, CRE = VIL, /OE = don't care)

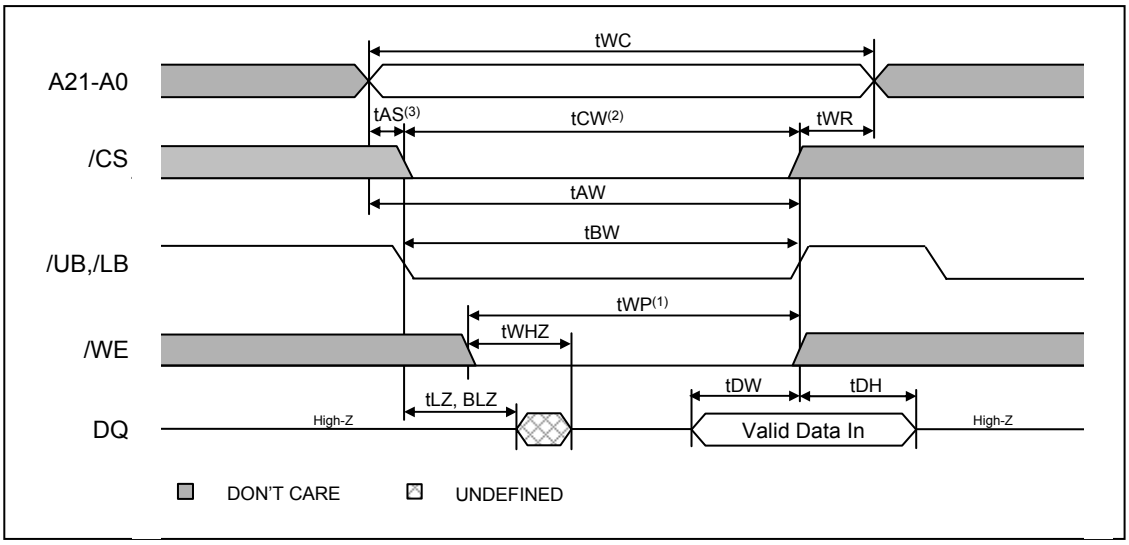
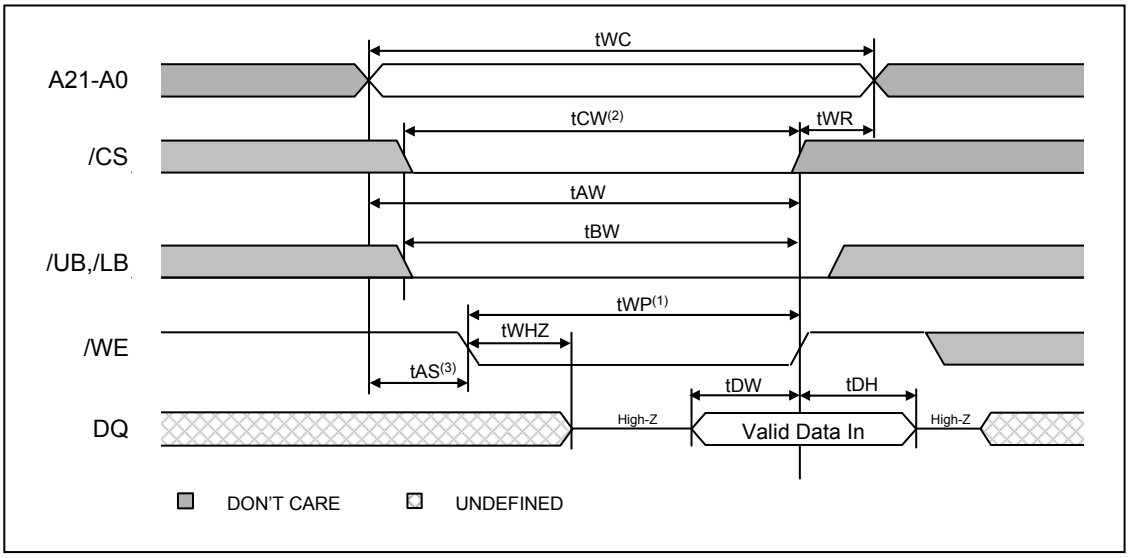


Fig.27 Asynchronous Write Cycle 3 (/WE Controlled, CRE = VIL, /OE = don't care)



Note (WRITE CYCLE) :

1. *A write occurs during the overlap of a low /CS and low /WE. A write begins at the latest transition among /CS going low and /WE going low: A write end at the earliest transition among /CS going high and /WE going high. tWP is measured from the beginning of write to the end of write.*
2. *tCW is measured from the later of /CS going low to the end of write.*
3. *tAS is measured from the address valid to the beginning of write.*
4. *tWR is measured from the end of write to the address change. tWR is applied in case a write ends as /CS.*
5. *Do not access device with cycle timing shorter than tRC for continuous periods > 10us.*
6. */ADV, CLK have no effect of the device operations.*
7. *WAIT pin is always kept in high-Z.*

3.4 Synchronous AC Characteristics[1,2] (T_A = -25 to 85℃)

Table 12 : Synchronous CLK Characteristics

Parameter		Symbol	Speed Bins				Units
			104/80Mhz(70ns)		66Mhz(85ns)		
			Min	Max	Min	Max	
CLK period	Latency Code=3	tCLK3	9.62/12.5		15		ns
	Latency Code=2	tCLK2	15		25		ns
CLK period[3]	Latency Code=6	tCLK6	9.62/12.5		15		ns
	Latency Code=5	tCLK5	13.3		19.2		ns
	Latency Code=4	tCLK4	15		25		ns
	Latency Code=3	tCLK3	19.2		30		ns
	Latency Code=2	tCLK2	30		50		ns
CLK high or low time		tCKP	3		5		ns
CLK rise or fall time		tT		1		1.5	ns

Note :
1. Assume tT (Clock rise and fall time) is 1ns
2. Access time to be measured with input signals of 1v/ns edge rate
3. This is the value when the device is operating in fixed latency mode

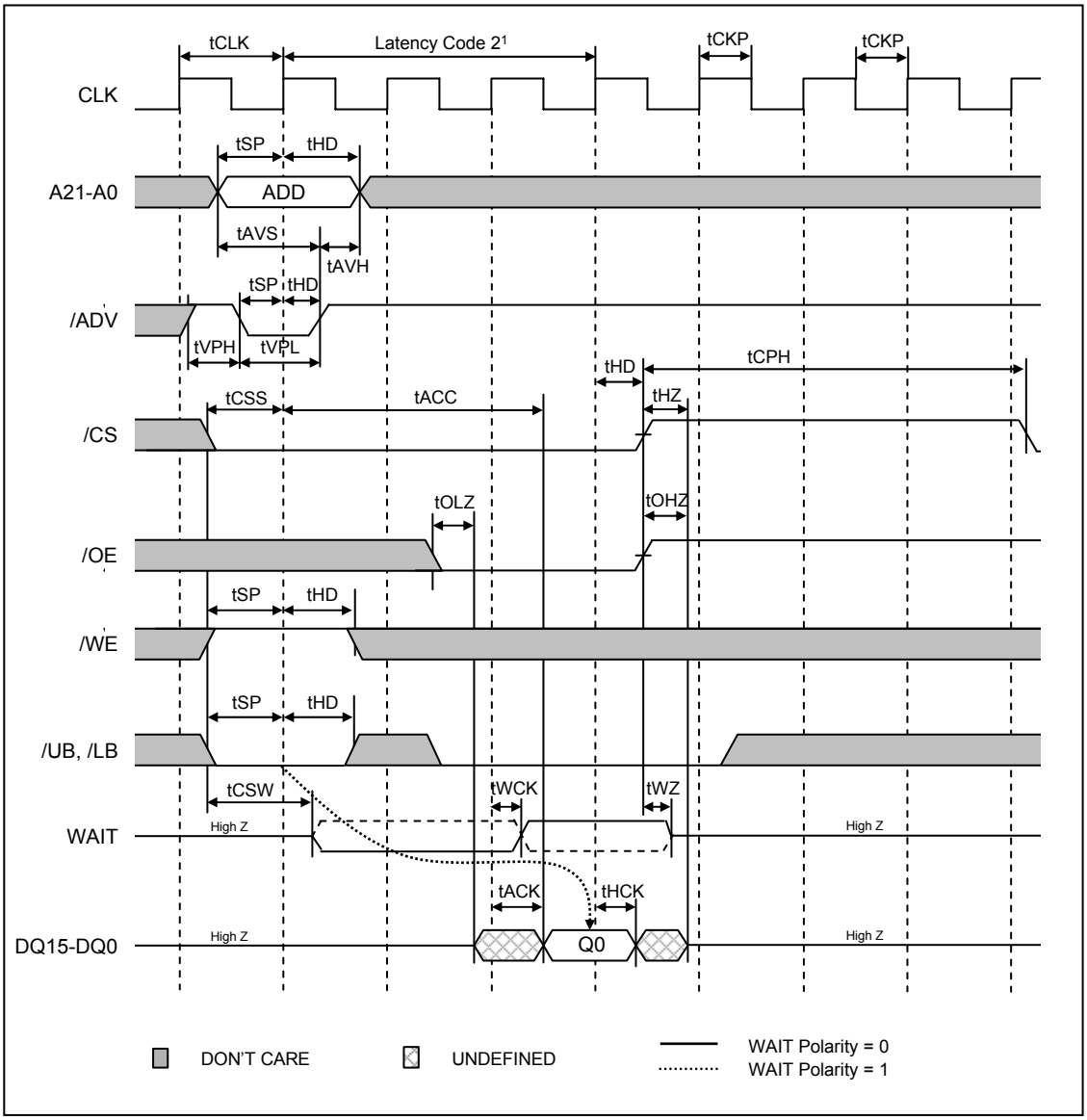
Table 13 : Synchronous AC Characteristics

Parameter	Symbol	Speed Bins				Units
		104/80Mhz(70ns)		66Mhz(85ns)		
		Min	Max	Min	Max	
Setup time to active CLK edge	tSP	3		4		ns
Hold time from active CLK edge	tHD	2		2		ns
CLK to output delay	tACK		7		10	ns
Output hold from CLK	tHCK	2		3		ns
CLK to WAIT delay	tWCK		7		10	ns
Burst read first access time	tACC		36		55	ns
/CS low setup to start CLK edge	tCSS	5	20	6	20	ns
/CS or /UB,/LB high to output High-Z	tHZ	0	6	0	10	ns
Output disable to output High-Z	tOHZ	0	6	0	10	ns
Output enable to output low-Z	tOLZ	5		5		ns
/CS pre-charge time	tCPH	5		5		ns
Address setup to /ADV high	tAVS	3		4		ns
Address hold from /ADV high	tAVH	2		2		ns
/ADV pulse width high	tVPH	5		5		ns
/ADV pulse width low	tVPL	4		4		ns
/OE low to output delay	tOE	20		25		ns
/CS low to WAIT valid	tCSW	1	7	1	10	ns
/CS high to WAIT high-Z	tWZ	1	8	1	10	ns
/WE high pulse width	tWPH[3]	5		5		ns
/CS low to /ADV high time	tCVH[3]	10		15		ns
/ADV low to write end time	tVS[3]	70		85		ns
/ADV low to output delay	tVO[3]	70		85		ns

Note :
1. Assume tT (Clock rise and fall time) is 1ns
2. Access time to be measured with input signals of 1v/ns edge rate
3. tWPH, tCVH, tVS and tVO are only restricted in asynchronous operation

3.5 Synchronous Timing Diagram

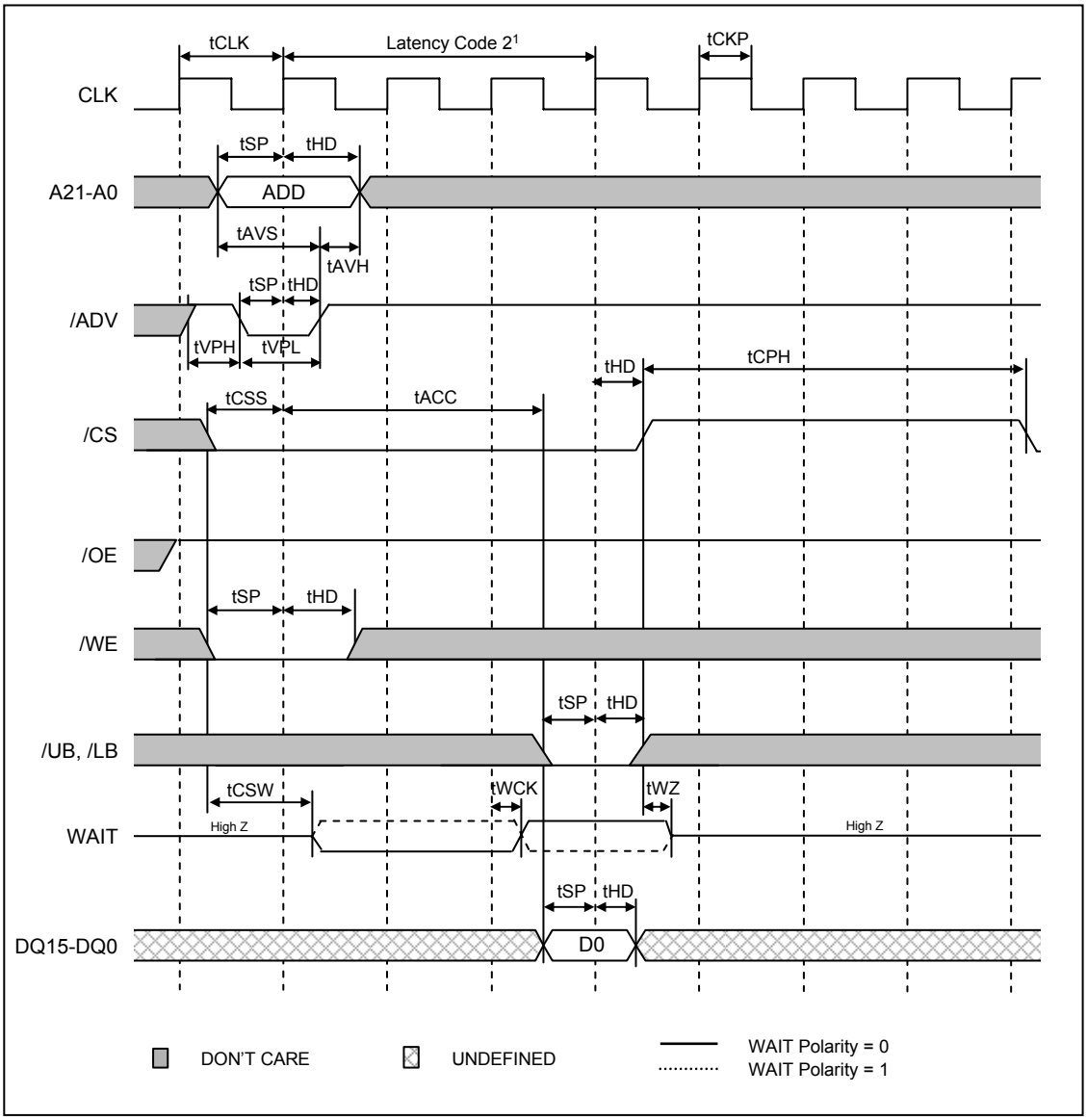
Fig.28 Synchronous Single Read Operation (BL= don't care, CRE = VIL)



Note :

1. *Configuration register setting " First Access Latency Count " describes how to insert clock cycles during initial access*
2. *WAIT Polarity is set by Bus Configuration Register setting Mode*
3. *Once determined mode(Sync. or Async.) via tCSS is maintained until /CS disable regardless of clock*

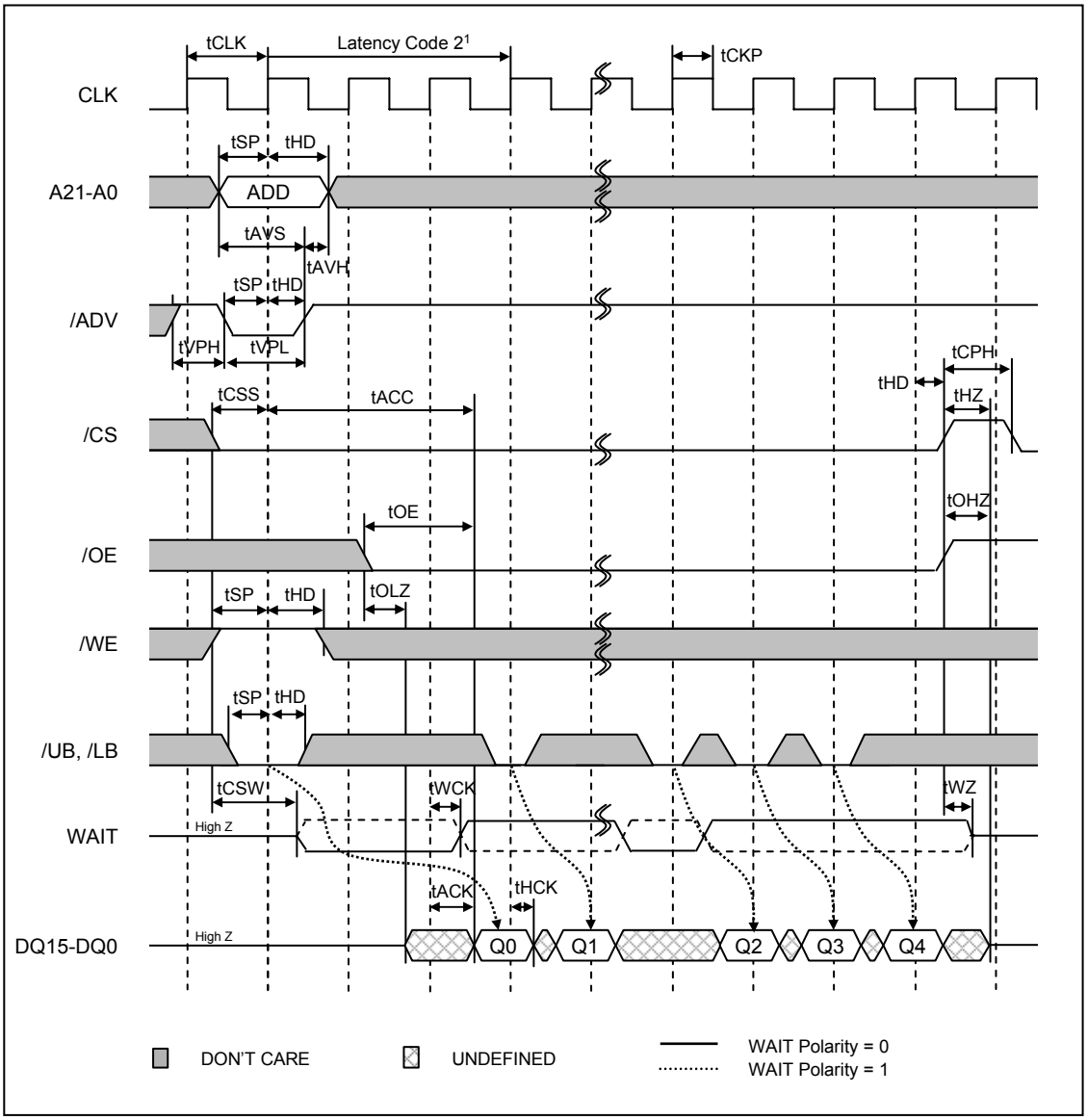
Fig.29 Synchronous Single Write Operation (BL= don't care, CRE = VIL)



Note :

1. *Configuration register setting " First Access Latency Count " describes how to insert clock cycles during initial access*
2. *WAIT Polarity is set by Bus Configuration Register setting Mode*
3. *Once determined mode(Sync. or Async.) via tCSS is maintained until /CS disable regardless of clock*

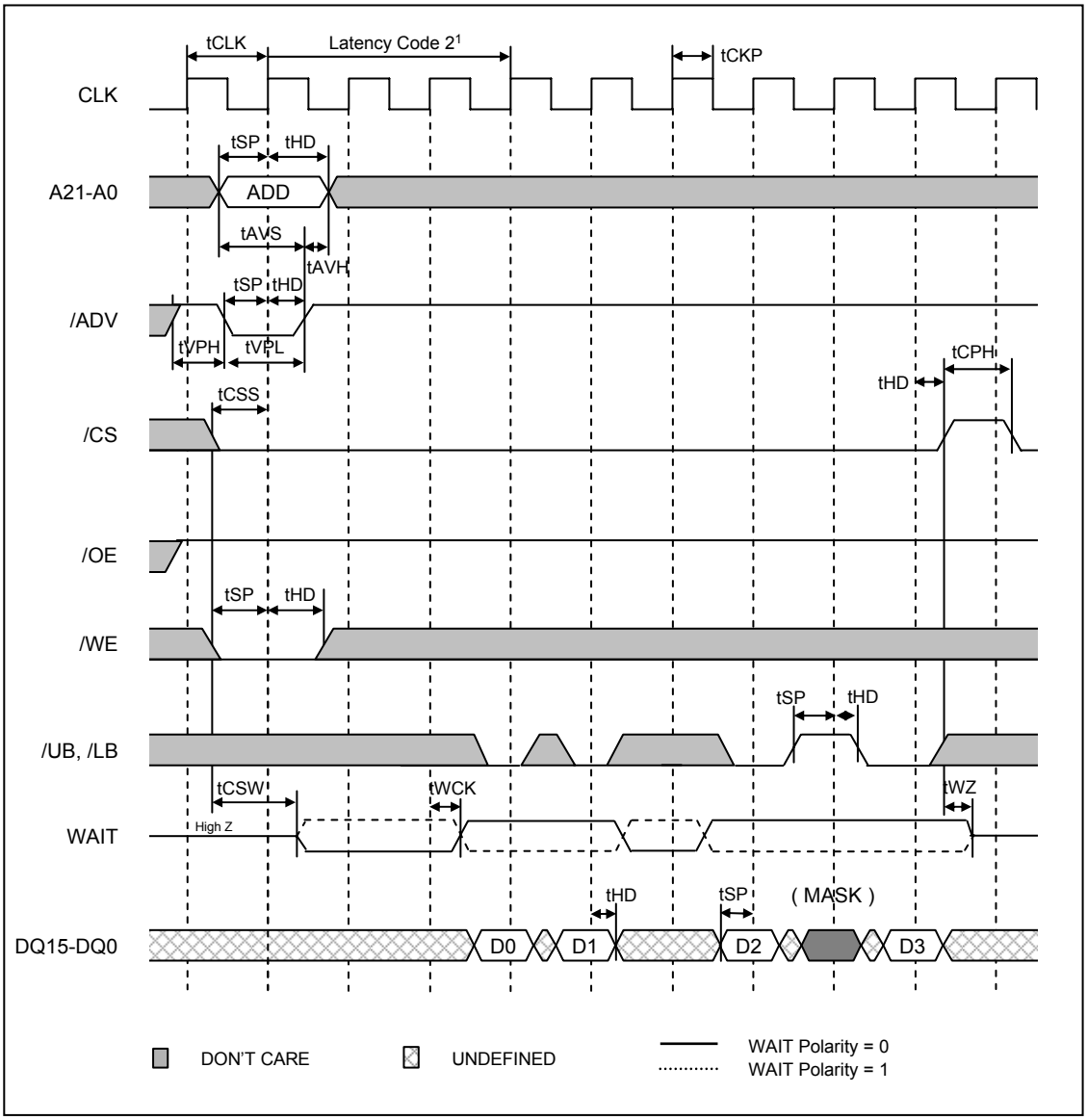
Fig.30 Synchronous Burst Read Operation (BL= continuous, CRE = VIL)



Note :

1. *Configuration register setting " First Access Latency Count " describes how to insert clock cycles during initial access*
2. *Only /CS disable can stopped the continuous burst operations*
3. WAIT is asserted when a burst crosses a row boundary or an internal refresh is needed
4. *Once determined mode(Sync. or Async.) via tCSS is maintained until /CS disable regardless of clock*

Fig.31 Synchronous Burst Write Operation (BL= continuous, CRE = VIL)



Note :

1.Configuration register setting " First Access Latency Count " describes how to insert clock cycles during initial access

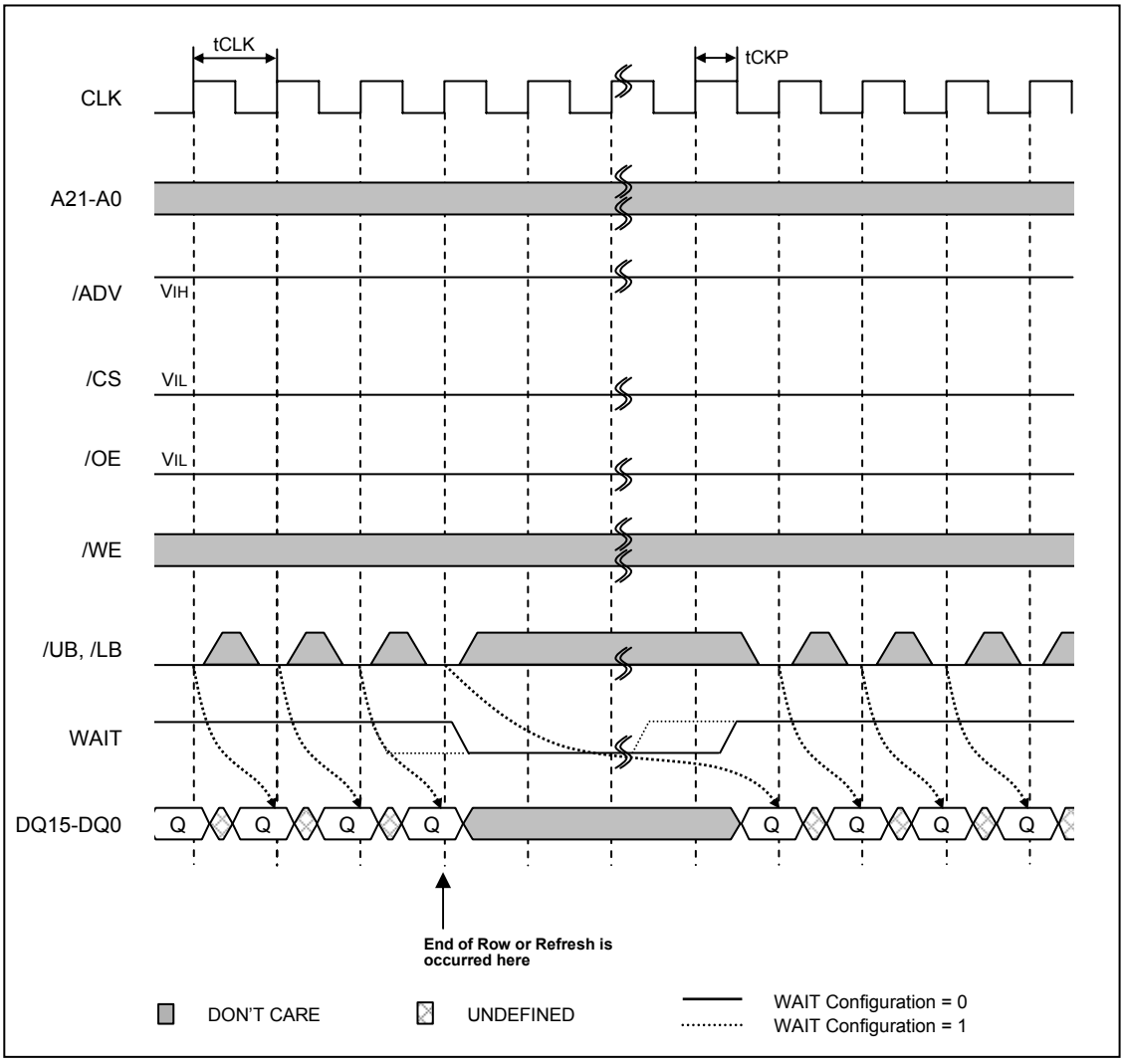
2. Only /CS disable can stopped the continuous burst operations

3. WAIT is asserted when a burst crosses a row boundary or an internal refresh is needed

4. /UB,/LB state determine whether the data of current clock is written or not during write operations

5. Once determined mode(Sync. or Async.) via tCSS is maintained until /CS disable regardless of clock

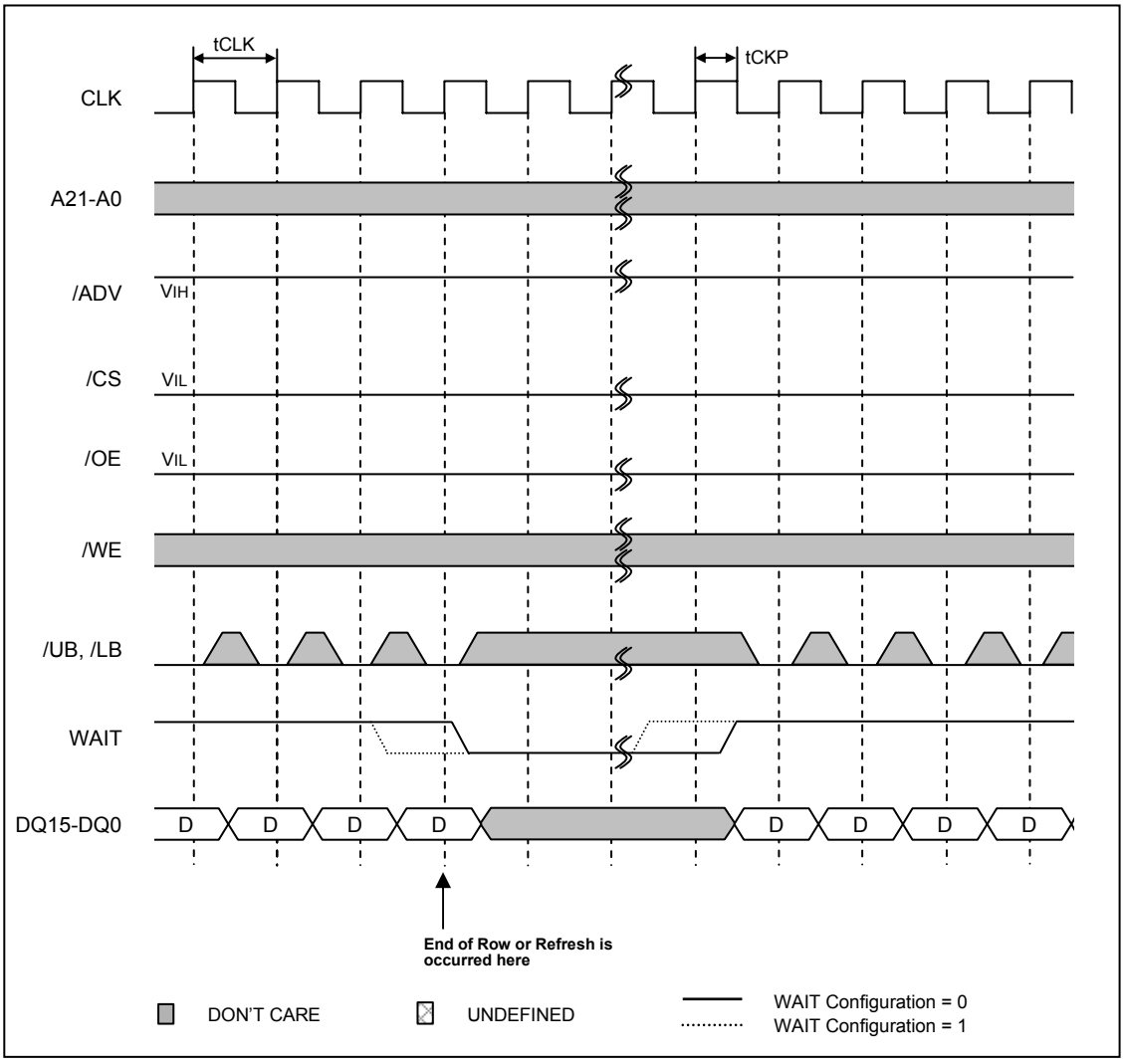
Fig.32 Burst Read Showing an Output Delay for Abnormal[1] Condition (BL= continuous, CRE = VIL)



Note :

1. *The abnormal condition means that current access is either Cross the Row Boundary or in Collisions with Refresh.*
2. *Configuration register setting " First Access Latency Count " describes how to insert clock cycles during initial access*
3. *WAIT Configuration is set by Bus Configuration Register setting Mode*

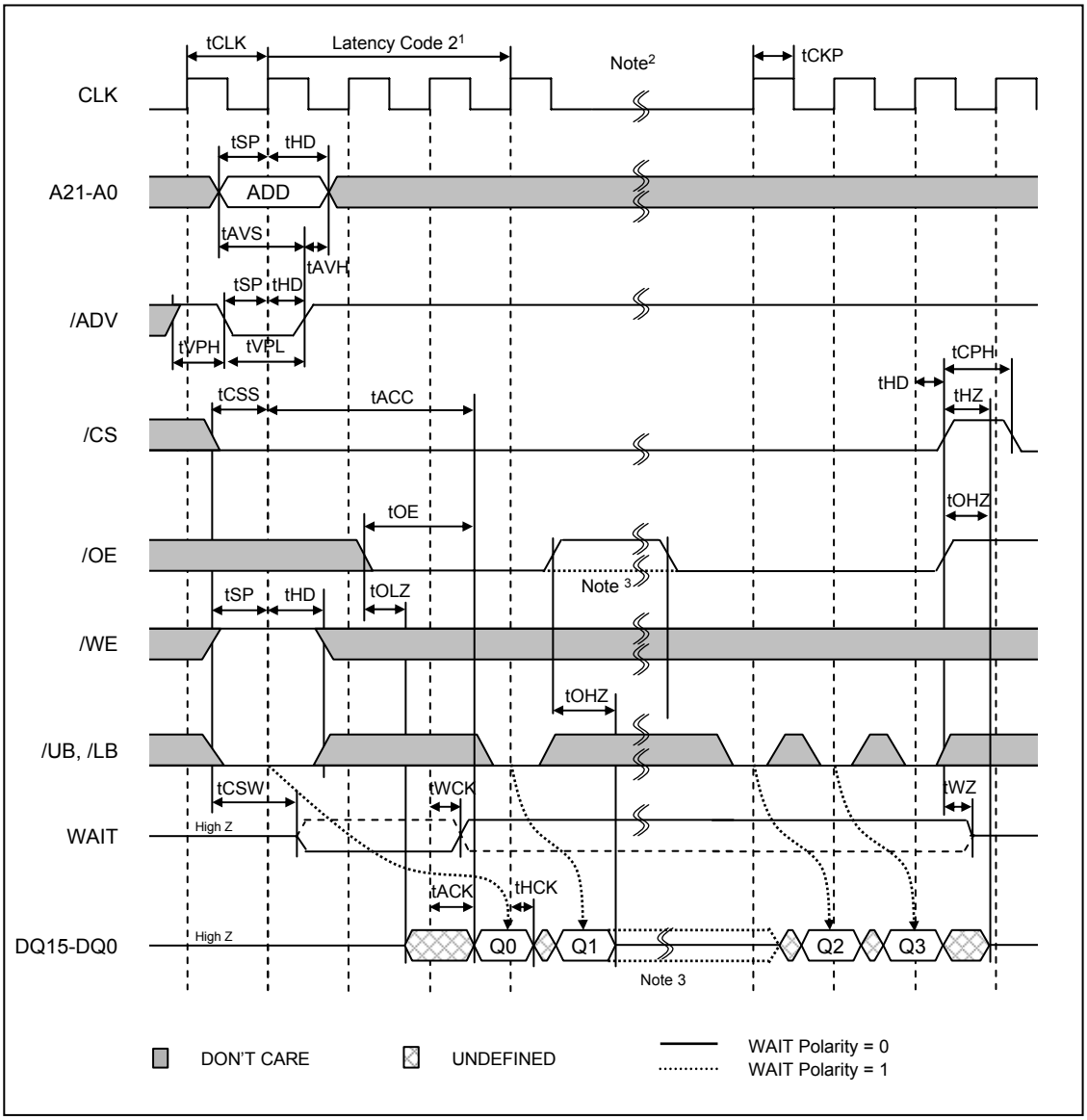
Fig.33 Burst Write Showing an Input Delay for Abnormal[1] Condition (BL= continuous, CRE = VIL)



Note :

1. *The abnormal condition means that current access is either Cross the Row Boundary or in Collisions with Refresh.*
2. *Configuration register setting " First Access Latency Count " describes how to insert clock cycles during initial access*

Fig.34 Burst Read Suspend Operation (BL= continuous, CRE = VIL)



Note :

1. *Configuration register setting " First Access Latency Count " describes how to insert clock cycles during initial access*
2. *In order to burst read/write suspend, Clock signal should be held high or low.*
3. *Data in/out bus lines could be high-Z state by means of ,/OE disable during burst suspend*
4. *Once determined mode(Sync. or Async.) via tCSS is maintained until /CS disable regardless of clock*

Fig.35 Burst Write Followed by Burst Read (BL= 4, CRE = VIL)

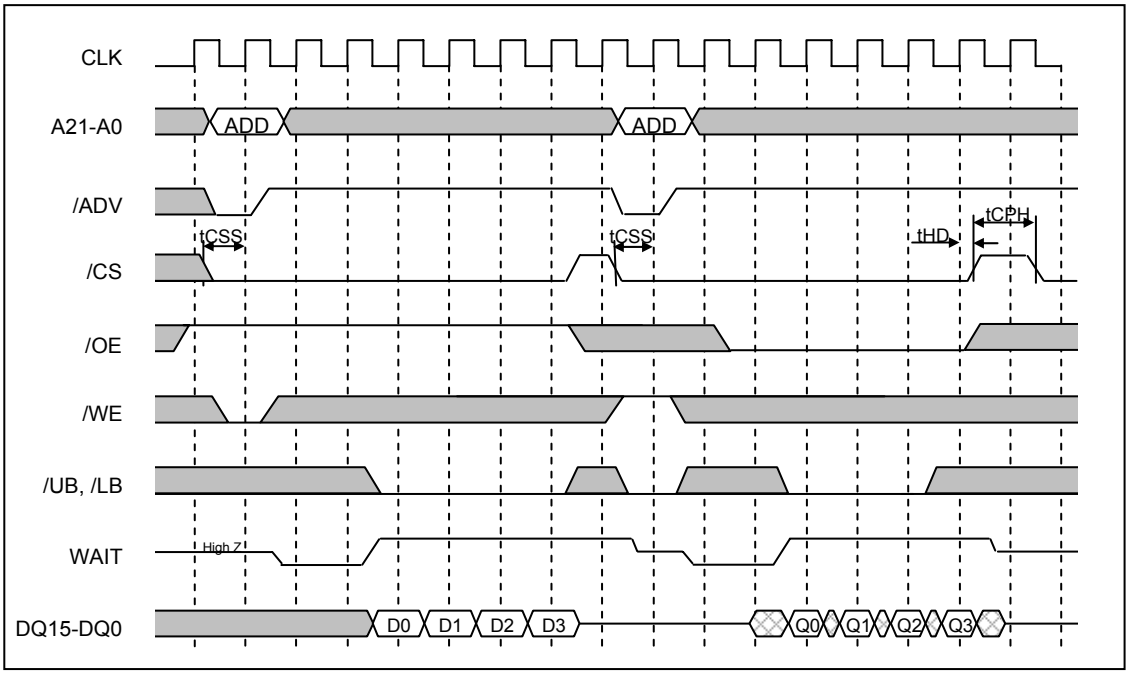
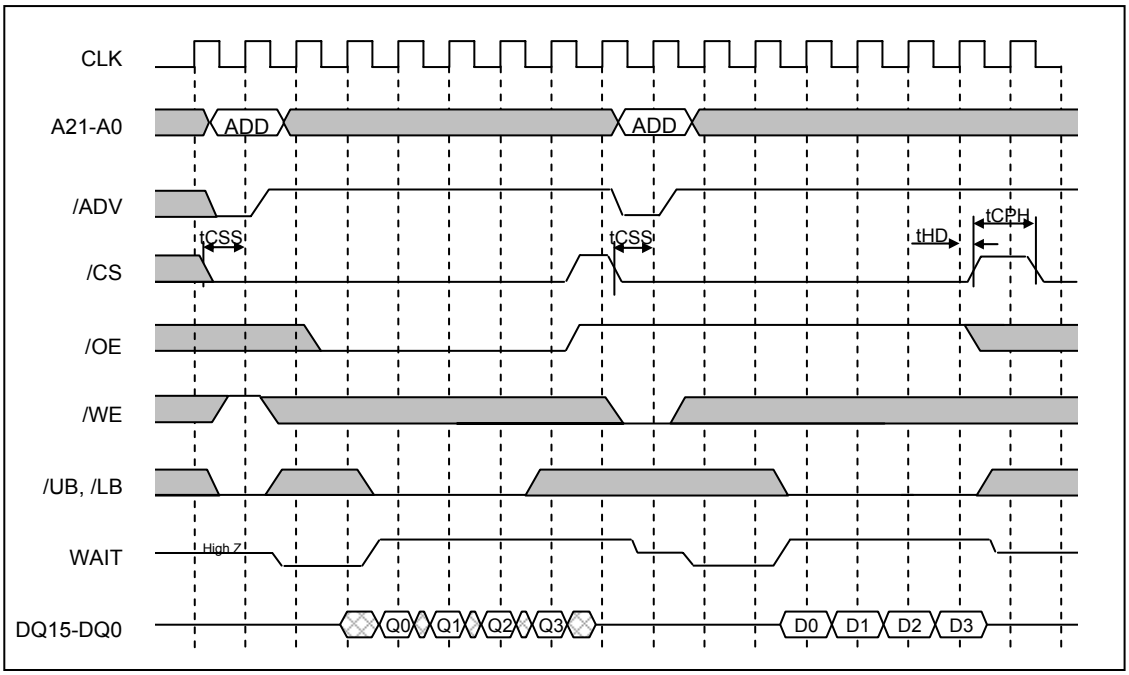


Fig.36 Burst Read Followed by Burst Write (BL= 4, CRE = VIL)



Note :

1. *To allow self-refresh operations to occur between transactions, /CS must retain HIGH for at least 5ns(tCPH) to schedule the appropriate internal refresh operation*
2. *Once determined mode(Sync. or Async.) via tCSS is maintained until /CS disable regardless of clock*

Fig.37 Burst Read Followed by Asynchronous Write with /ADV Control (BL= 4, CRE = VIL)

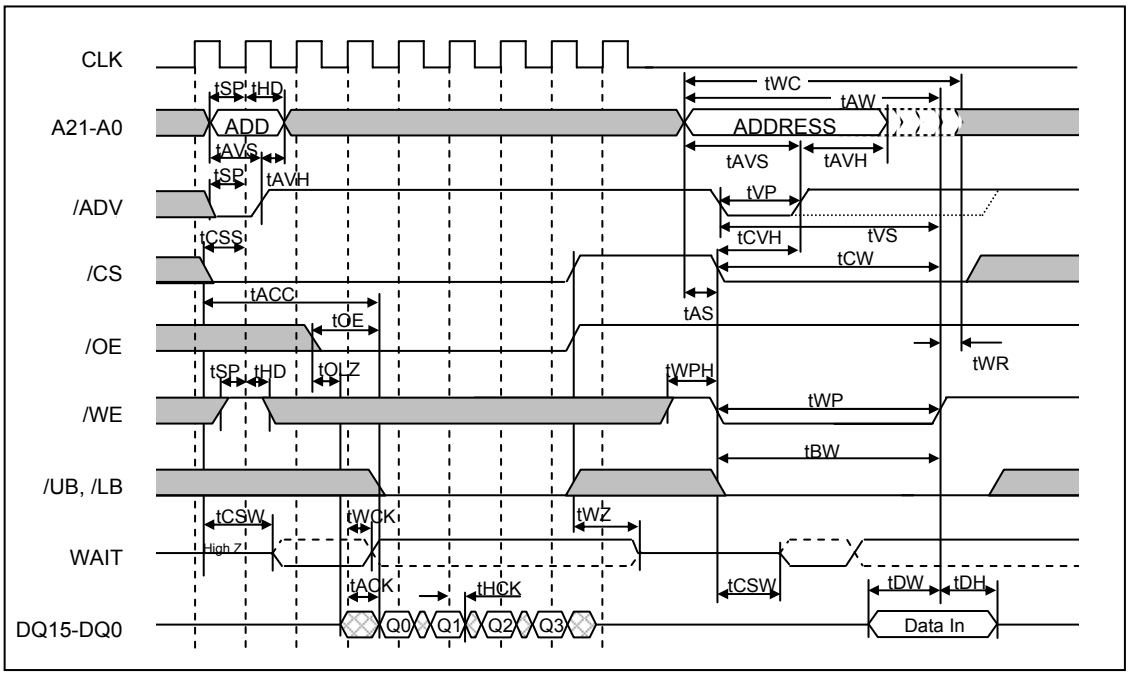
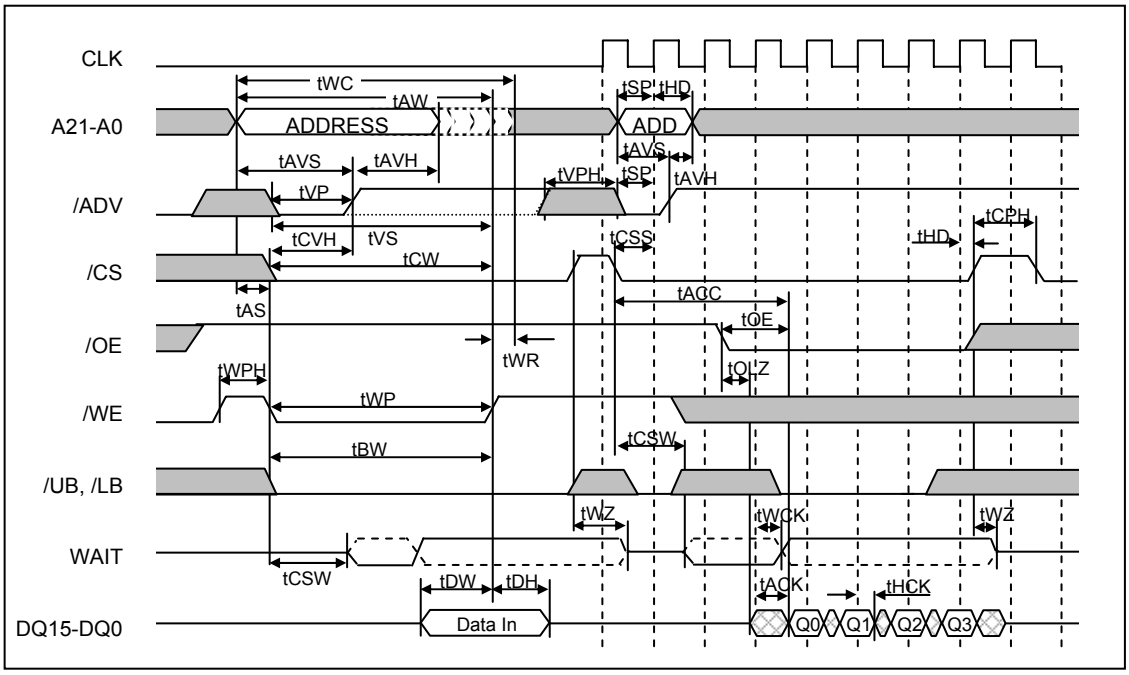


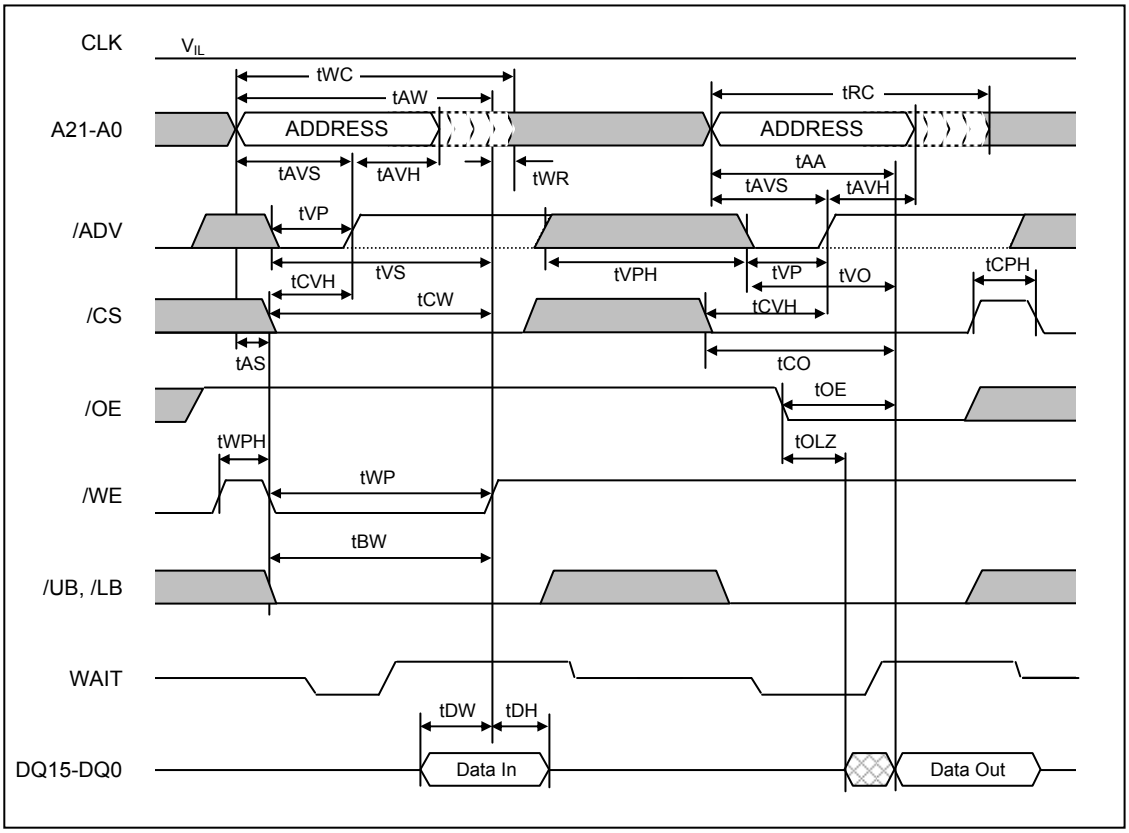
Fig.38 Asynchronous Write with /ADV Control Followed by Burst Read(BL= 4, CRE = VIL)



Note :

1. *To change the operation mode from Sync. to Async. or in opposition, /CS must be HIGH for at least 5ns(tCPH) to altered operation mode*
2. *Once determined mode(Sync. or Async.) via tCSS is maintained until /CS disable regardless of clock*
3. *Unspecified parameters in Synchronous AC characteristics have to meet the value of Asynchronous AC characteristics*

Fig.39 Asynchronous Write Followed by Asynchronous Read (BL= don't care, CRE = VIL)

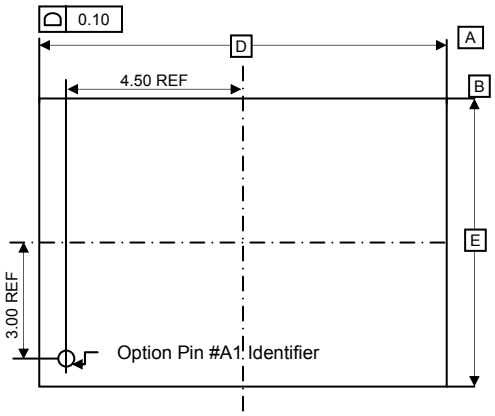


Note :

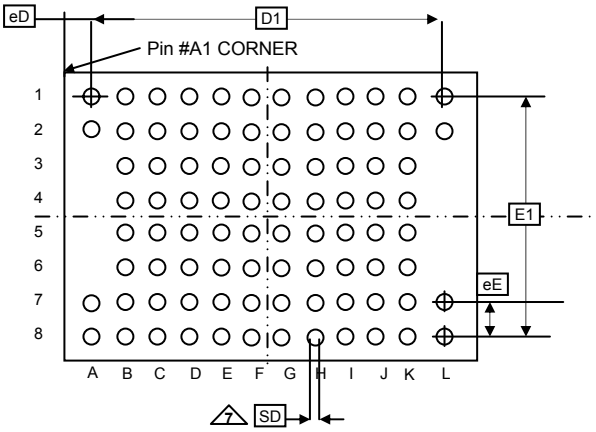
1. *Page mode is ignored in synchronous mode setting*
2. *Once determined mode(Sync. or Async.) via tCSS is maintained until /CS disable regardless of clock*
3. *Unspecified parameters in Synchronous AC characteristics have to meet the value of Asynchronous AC characteristics*

PHYSICAL DIMENSIONS

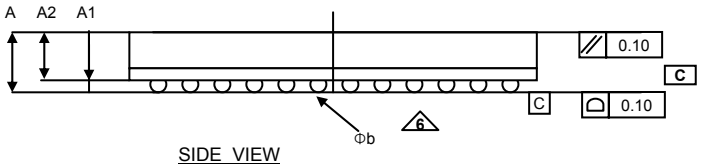
— 88 Ball Fine-Pitch Grid Array 8 x 10 mm



TOP VIEW



BOTTOM VIEW



SIDE VIEW

PACKAGE	88 Ball FBGA			NOTE
JEDEC	N/A			
	8.00mm X 10.00mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	
A	-	-	1.40	PROFILE
A1	0.15	-	0.20	BALL HEIGHT
A2	0.91	-	1.01	BODY THICKNESS
D	10.00 BSC			BODY SIZE
E	8.00 BSC			BODY SIZE
D1	8.80 BSC			MATRIX FOOTPRINT
E1	5.60 BSC			MATRIX FOOTPRINT
MD	10			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
n	72			BALL COUNT
Φb	0.35	0.4	0.45	BALL DIAMETER
eD	0.80 BSC			BALL PITCH
eE	0.80 BSC			BALL PITCH
SD/SE	0.40 BSC			SOLDER BALL PLACEMENT

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

△6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

△7 SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DFFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

4. Part-Numbering Information

Fig.42 Part Number Chart