SONY

CXD2401R

Electronic Iris Control IC

Description

The CXD2401R is an IC which performs electronic iris control by applying a CCD electronic shutter.

Features

- Electronic iris control drive
- Generates system clocks in response to the CXA1390AR series
- Generates timing pulses to drive the 510H system CCD image sensor
- H driver for CCD (5V direct drive for Type 1/3 CCD)

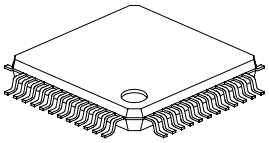
Absolute Maximum Ratings

• Supply voltage	V_{DD}	V_{SS} – 0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.75 to 5.25	V
• Operating temperature	Topr	–20 to +75	°C

48 pin LQFP (Plastic)



Applications

CCD monitoring cameras

Structure

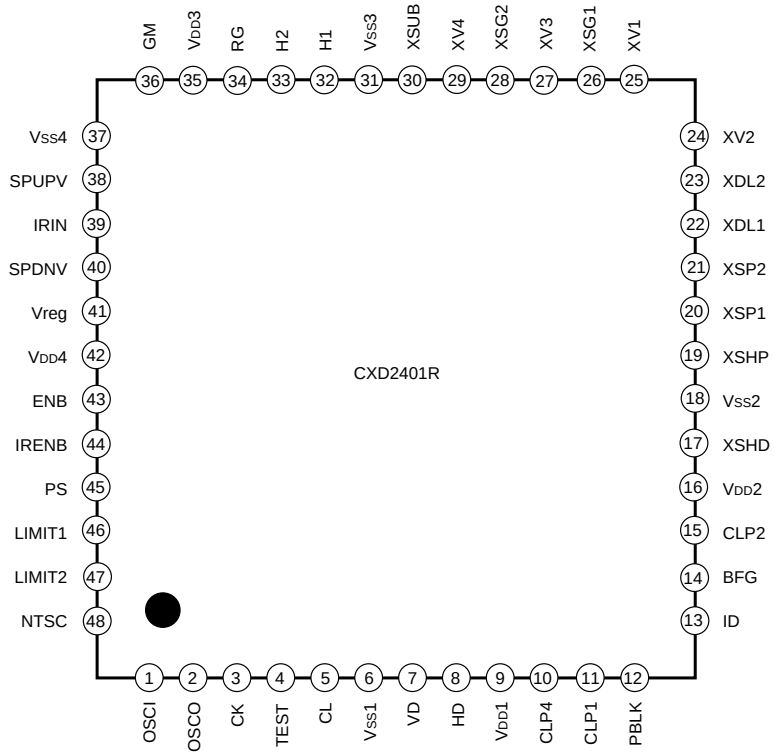
Silicon gate CMOS IC

Applicable CCD Image Sensors

510H system SONY CCD

- ICX054BK (Type 1/3 NTSC CCD)
- ICX055BK (Type 1/3 PAL CCD)

Pin Configuration



E94620E11-TE

Pin Description

Pin No.	Symbol	I/O	Description
1	OSCI	I	Inverter input for oscillation. (NTSC: 1820fH, PAL: 1816fH)
2	OSCO	O	Inverter output for oscillation. (NTSC: 1820fH, PAL: 1816fH)
3	CK	I	Input for main clock in IC. (NTSC: 1820fH, PAL: 1816fH)
4	TEST	I	IC test input. Fixed at GND in normal operation. (With pull-down resistor)
5	CL	O	CK/2 clock output. NTSC: 910fH = 4fsc, PAL: 908fH
6	$V_{SS}1$	—	GND
7	VD	I	Vertical sync signal input.
8	HD	I	Horizontal sync signal input.
9	$V_{DD}1$	—	5V power supply.
10	CLP4	O	Clamping pulse for CCD dummy output.
11	CLP1	O	Clamping pulse for CCD optical black.
12	PBLK	O	Cleaning pulse for vertical/horizontal blanking.
13	ID	O	Vertical direction line identification signal.
14	BFG	O	Burst flag gate pulse.
15	CLP2	O	Clamping pulse in horizontal blanking.
16	$V_{DD}2$	—	5V power supply.
17	XSHD	O	CCD data level sample-and-hold pulse output.
18	$V_{SS}2$	—	GND
19	XSHP	O	CCD precharge level sample-and-hold pulse output.
20	XSP1	O	Color separation sample-and-hold pulse output.
21	XSP2	O	Color separation sample-and-hold pulse output.
22	XDL1	O	Clock output for CCD DL (Delay Line).
23	XDL2	O	Clock output for CCD DL (Delay Line).
24	XV2	O	CCD vertical clock output.
25	XV1	O	CCD vertical clock output.
26	XSG1	O	Clock output for CCD sensor readout.
27	XV3	O	CCD vertical clock output.
28	XSG2	O	Clock output for CCD sensor readout.
29	XV4	O	CCD vertical clock output.
30	XSUB	O	Clock output for CCD electronic shutter.
31	$V_{SS}3$	—	GND
32	H1	O	CCD horizontal clock output.
33	H2	O	CCD horizontal clock output.
34	RG	O	CCD reset gate pulse output.

Pin No.	Symbol	I/O	Description
35	$V_{DD}3$	—	5V power supply.
36	GM	I	Used for GND connection.
37	$V_{SS}4$	—	GND
38	SPUPV	I	When set in electronic iris mode: Shutter speedup reference voltage input When set in serial mode of electronic shutter: Strobe input
39	IRIN	I	When set in electronic iris mode: Iris signal input When set in serial mode of electronic shutter: Clock input
40	SPDNV	I	When set in electronic iris mode: Shutter speed-down reference voltage input When set in serial mode of electronic shutter: Data input
41	Vreg	—	Current source for comparator. Connected to 5V power supply via 33kΩ resistor.
42	$V_{DD}4$	—	5V power supply.
43	ENB	I	Generation/halt switching of electronic shutter pulse (Pin 30). (With pull-up resistor)
44	IRENB	I	Electronic iris/electronic shutter switching. (With pull-up resistor)
45	PS	I	Parallel/serial input switching of electronic shutter speed data. (With pull-up resistor)
46	LIMIT1	I	Selecting limit value of max. shutter speed. (With pull-down resistor)
47	LIMIT2	I	Selecting limit value of max. shutter speed. (With pull-down resistor)
48	NTSC	I	NTSC/PAL switching. (With pull-down resistor)

Electrical Characteristics

DC Characteristics (Within recommended operating range)

Item	Pin No.	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage 1	9, 16, 35, 42	V_{DD}		4.75	5.0	5.25	V
Input voltage 1	38, 40 (Electronic iris mode)	$V_{IN}1$		1.9		V_{DD}	V
Input voltage 2	39 (Electronic iris mode)	$V_{IN}2$		V_{SS}		V_{DD}	V
Input voltage 3*	4, 7, 8, 36, 38, 39, 40, 43, 44, 45, 46, 47, 48 (Pins 38, 39 and 40 are when set in electronic shutter mode)	$V_{IH}3$		$0.7V_{DD}$			V
		$V_{IL}3$				$0.3V_{DD}$	V
Output voltage 1	5, 10, 11	$V_{OH}1$	I_{OH} = –4mA	V_{DD} – 0.8			V
		$V_{OL}1$	I_{OL} = 8mA			0.4	V
Output voltage 2	15, 17, 19, 20, 21, 22, 23, 34	$V_{OH}2$	I_{OH} = –8mA	V_{DD} – 0.8			V
		$V_{OL}2$	I_{OL} = 8mA			0.4	V
Output voltage 3	32, 33	$V_{OH}3$	I_{OH} = –20mA	V_{DD} – 0.8			V
		$V_{OL}3$	I_{OL} = 20mA			0.4	V
Output voltage 4	12, 13, 14, 24, 25, 26, 27, 28, 29, 30	$V_{OH}4$	I_{OH} = –2mA	V_{DD} – 0.8			V
		$V_{OL}4$	I_{OL} = 4mA			0.4	V
Pull-up resistance value	43, 44, 45	R_{PU}	V_{IL} = 0V	25	50	75	kΩ
Pull-down resistance value	4, 36, 46, 47, 48	R_{PD}	$V_{IH} = V_{DD}$	25	50	75	kΩ

* Pins 7 and 8 do not have a protective diode at the power supply side.

Comparator Characteristics (Within recommended operating range)

Item		Pin No.	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input offset voltage		38, 39, 40	Vos			1.1	50	mV
Response time	Rise		tpd +	Response time when a step input of 100mV amplitude/ 5mV overdrive is applied.		140		ns
	Fall		tpd –			190		ns
Current consumption			IDD			98	140	µA
In-phase input voltage range			VICR		1.9 to 5			V
Indefinite region			Vf				±10	mW

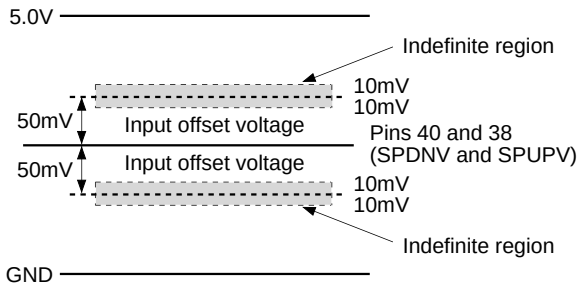
Bias current source for comparator. Pin No.: 41. Connected to power supply via 33kΩ resistor.

Note) 1. Input offset voltage and indefinite region

Input offset voltage and indefintie region are existed in the comparator which builds in this IC as shown right figure. Note that this when designing external circuit.

2. Pins 40 and 38 for electronic iris mode

Use it in this state of Pin 40 (SPDNV) > Pin 38 (SPUPV).



Oscillating Inverter I/O Characteristics (Within recommended operating range)

Item	Pin No.	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	1	LVth			VDD/2		V
Input voltage		VIH		0.7VDD			V
		VIL				0.3VDD	V
Output voltage	2	VOH	IOH = –12mA	VDD/2			V
		VOL	IOL = 12mA			VDD/2	V
Feedback resistor	1 to 2	RFE	VIN = VDD or Vss	250k	1M	2.5M	Ω
Oscillator frequency		f		20		30	MHz

Duty Control Inverter Input Characteristics (Within recommended operating range)

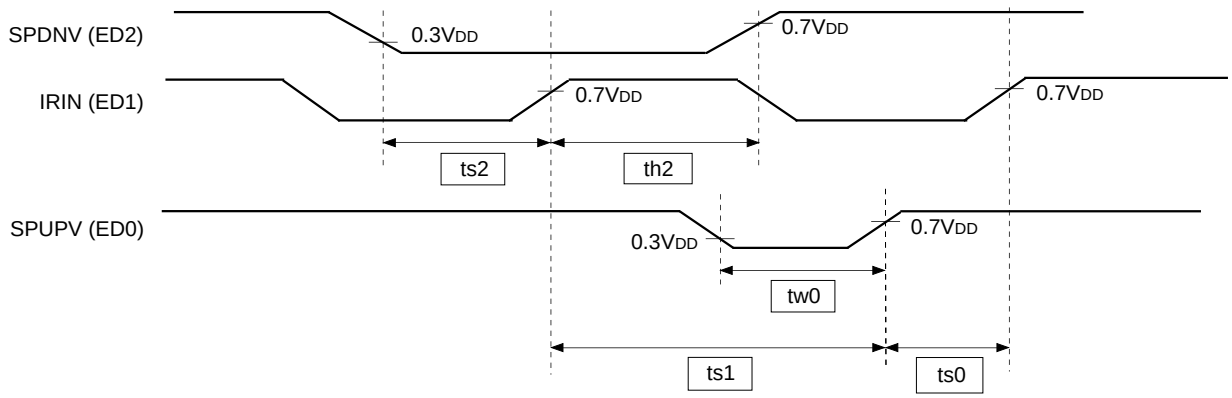
Item	Pin No.	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	3	LVth			VDD/2		V
Input voltage		VIH		0.7VDD			V
		VIL				0.3VDD	V
Input amplification		VIN	fmax = 50MHz sine wave	0.5			Vpp
Feedback resistor		RFE	VIN = VDD or Vss	250k	1M	2.5M	Ω

Note) The input voltage is the input voltage characteristics for an external direct power input, and input amplification is the input amplification characteristics for input through capacitor.

Electrical Characteristics

AC Characteristics

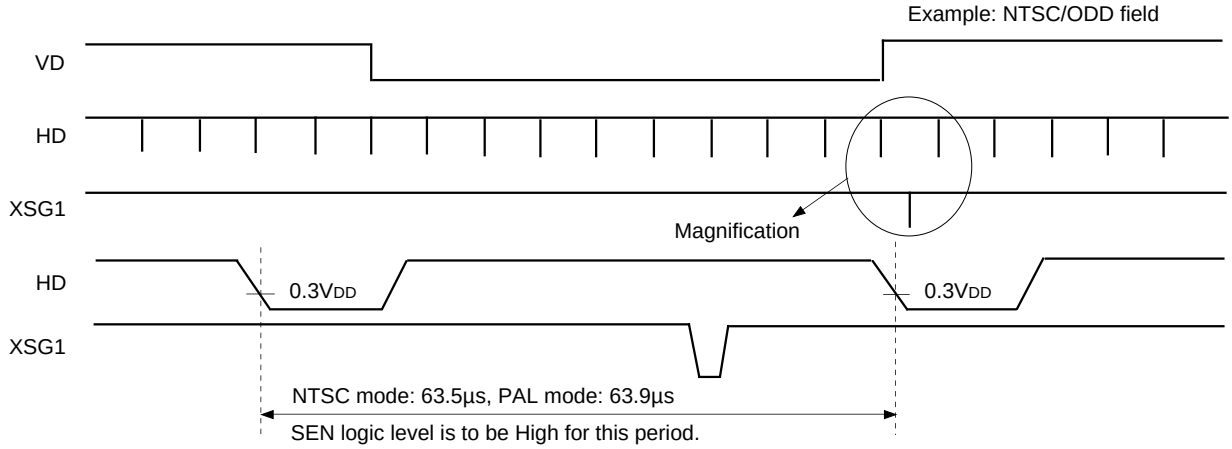
1) AC characteristics among serial communication clocks (SPDNV (ED2), IRIN (ED1), SPUPV (ED0))



(Within recommended operating range)

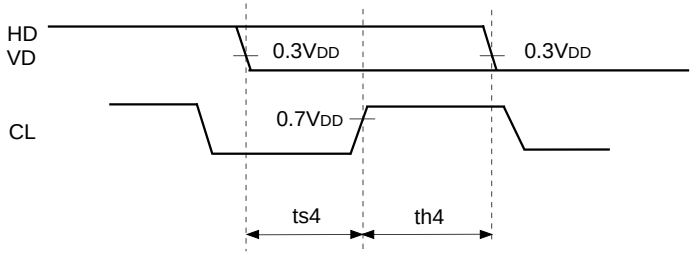
Symbol	Definition	Min.	Typ.	Max.
ts2	SPDNV (ED2) set-up time, activated by the rising edge of IRIN (ED1)	20ns		
th2	SPDNV (ED2) hold time, activated by the rising edge of IRIN (ED1)	20ns		
ts1	IRIN (ED1) rising set-up time, activated by the rising edge of SPUPV (ED0)	20ns		
tw0	SPUPV (ED0) pulse width	20ns		50µs
ts0	SPUPV (ED0) rising set-up time, activated by the rising edge of IRIN (ED1)	20ns		

2) Microcomputer communication clock → IC take-in characteristics



Note) During the 1H period for generating XSG1, the phase against AVD differs according to each mode. Please always maintain the SEN logic level at High for "the 1H period when XSG1 varies."

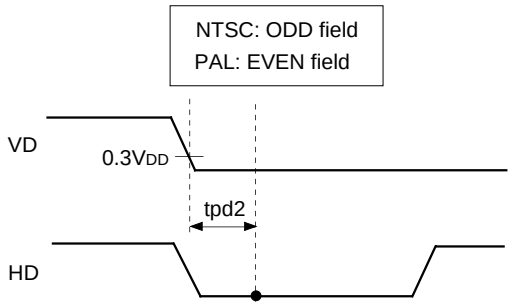
3) HD/VD take-in characteristics



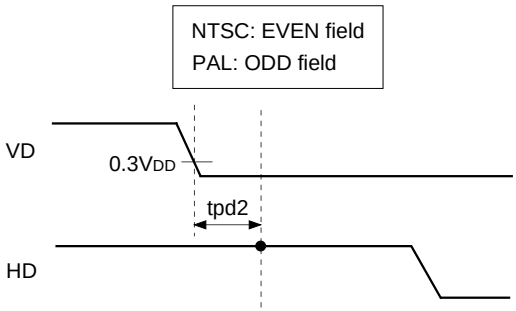
(Within recommended operating range, Load capacity of CL = 30pF)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts4	HD/VD set-up time, activated by CL	5			ns
th4	HD/VD hold time, activated by CL	7			ns

4) Phase discrimination characteristics by VD/HD input



When the HD logic level is Low tpd2 after VD falls, the phase is discriminated as an ODD field (NTSC).

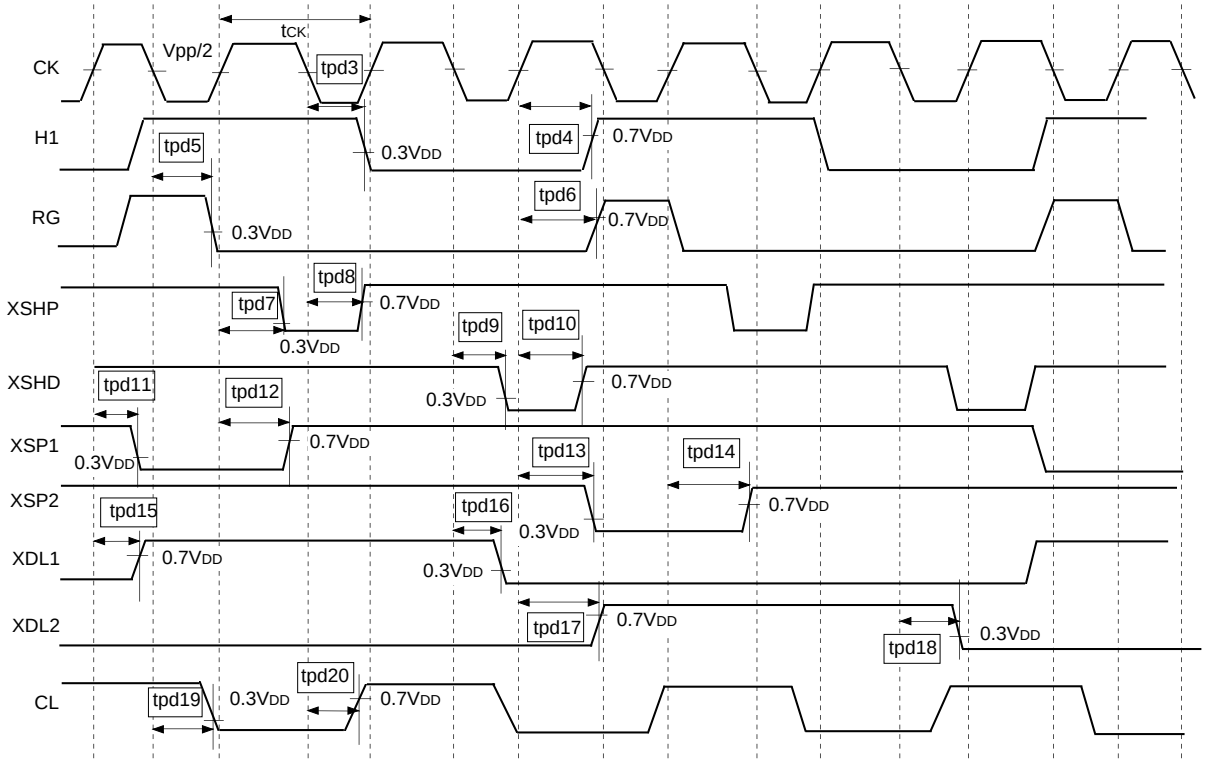


When the HD logic level is High tpd2 after VD falls, the phase is discriminated as an EVEN field (NTSC).

(Within recommended operating range)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpd2	Field discriminating clock phase, activated by the falling edge of VD	700		1000	ns

5) Phase characteristics of H1, RG, XSHP, XSHD, XSP1, XSP2, XDL1, XDL2, and CL

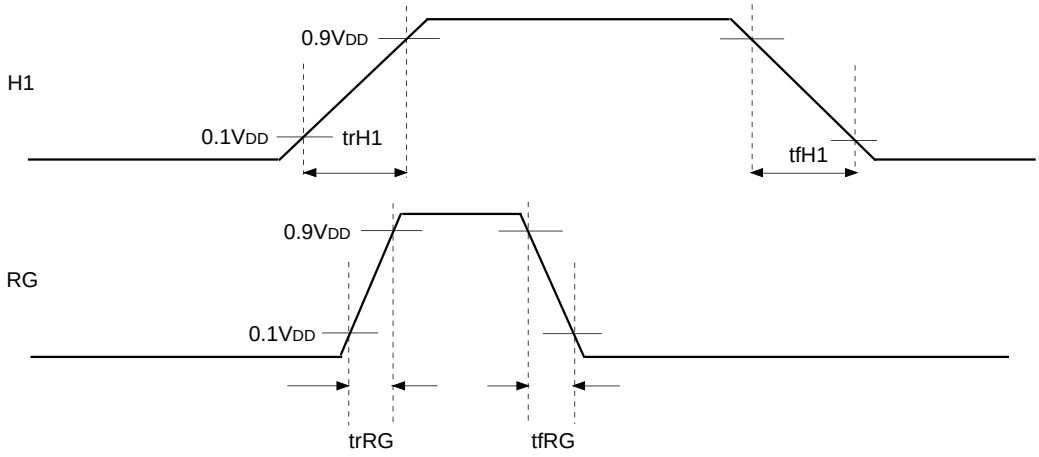


(Within recommended operating range)

CK-duty = within 50 ± 4%, Load capacity of H1 = 150pF, Load capacity of CL = 30pF, Load capacity of RG, XSHP, XSHD, XSP1, XSP2, XDL1, and XDL2 = 10pF

Symbol	Definition	Min.	Typ.	Max.	Unit
t_{CK}	CK cycle		35		ns
tpd3	H1 falling delay, activated by the falling edge of CK	16.22	29	56.9	ns
tpd4	H1 rising delay, activated by the rising edge of CK	17.25	31	60.38	ns
tpd5	RG falling delay, activated by the falling edge of CK	20.18	36	70.58	ns
tpd6	RG rising delay, activated by the rising edge of CK	18.61	33	65.32	ns
tpd7	XSHP falling delay, activated by the rising edge of CK	15.86	28	55.59	ns
tpd8	XSHP rising delay, activated by the falling edge of CK	15.76	28	55.32	ns
tpd9	XSHD falling delay, activated by the falling edge of CK	14.92	27	52.26	ns
tpd10	XSHD rising delay, activated by the rising edge of CK	14.76	26	51.62	ns
tpd11	XSP1 falling delay, activated by the rising edge of CK	14.79	26	51.74	ns
tpd12	XSP1 rising delay, activated by the rising edge of CK	15.05	27	52.58	ns
tpd13	XSP2 falling delay, activated by the rising edge of CK	15.09	27	52.82	ns
tpd14	XSP2 rising delay, activated by the rising edge of CK	15.29	27	53.54	ns
tpd15	XDL1 rising delay, activated by the rising edge of CK	14.49	26	50.79	ns
tpd16	XDL1 falling delay, activated by the falling edge of CK	15.05	27	52.67	ns
tpd17	XDL2 rising delay, activated by the rising edge of CK	14.46	26	50.65	ns
tpd18	XDL2 falling delay, activated by the falling edge of CK	14.92	27	52.47	ns
tpd19	CL falling delay, activated by the falling edge of CK	15.33	27	53.01	ns
tpd20	CL rising delay, activated by the falling edge of CK	14.71	26	51.58	ns

6) Waveform characteristics of H1 and RG



V_{DD} = 5.0V, Topr = 25°C, Load capacity of H1 = 150pF, Load capacity of RG = 10pF

Symbol	Definition	Min.	Typ.	Max.	Unit
t_{rH1}	H1 rise time		7		ns
t_{fH1}	H1 fall time		7		ns
t_{rRG}	RG rise time		3		ns
t_{fRG}	RG fall time		3		ns

I/O Pin Capacitances

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C_{IN}			9	pF
Output pin capacitance	C_{OUT}			11	pF
I/O pin capacitance	$C_{I/O}$			11	pF

Description of Operation

The operations of the CXD2401R are described below.

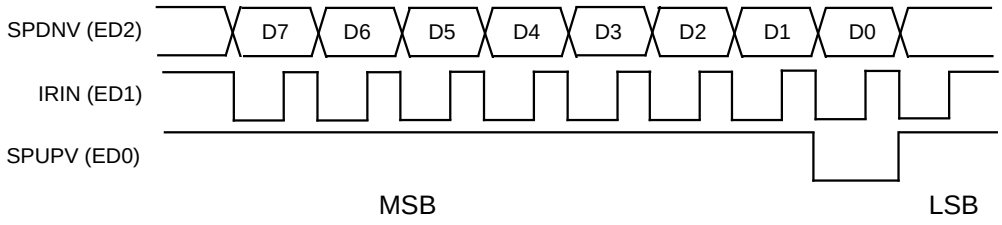
Control pin	Detailed description
NTSC (Pin 48)	Low: The CXD2401R performs control drive in accordance with NTSC. In this case, the CXD2401R operates by assuming the signals input to Pin 7 (VD) and Pin 8 (HD) are NTSC sync signals. High: The CXD2401R performs control drive in accordance with PAL. In this case, the CXD2401R operates by assuming the signals input to Pin 7 (VD) and Pin 8 (HD) are PAL sync signals. Refer to the "Timing Chart" for the control drive pulse for either NTSC or PAL.
ENB (Pin 43)	Low: Pin 30 (XSUB) is always High. That is, the electronic iris and electronic shutter to which XSUB pulses are applied suspend operation (electronic iris and electronic shutter OFF). High: Pin 30 (XSUB) outputs control pulses for the electronic iris and electronic shutter. (electronic iris and electronic shutter ON).
IRENB (Pin 44)	Low: Realizes the electronic shutter control. High: Realizes the electronic iris control. The control pins (SPUPV, IRIN, and SPDNV) are used in common for both electronic shutter control and electronic iris control. The operations of these pins differ depending on the state of IRENB pin.
PS (Pin 45)	This pin is valid when the operation of electronic shutter is assigned (IRENB = Low). Low: Electronic shutter speed can be controlled by inputting serial data into SPUPV, IRIN, and SPDNV pins. High: Electronic shutter speed can be controlled by inputting parallel data into SPUPV, IRIN, and SPDNV pins. **Note)** The PS pin is invalid when IRENB = High, and the CXD2401R does not accept data, whether PS is Low or High.

Control pin	Detailed description
SPUPV (Pin 38) IRIN (Pin 39) SPDNV (Pin 40)	The operations of SPUPV, IRIN, and SPDNV pins differ according to the mode (IRENB control) of the electronic iris and electronic shutter. The operations are described below for each case.

IRENB = Low: When the operation of electronic shutter is assigned

PS = Low: When inputting serial data is assigned

SPUPV : Strobe input pin
IRIN : Clock input pin
SPDNV : Data input pin



MSB LSB

	D7	D6	D5	D4	D3	D2	D1	D0
Ld : Shutter speed data Ex.: Ld = 100 [decimal]	0	1	1	0	0	1	0	0

<Shutter speed calculation formula> Shutter speed = 1/n [s]

Ld (decimal)	NTSC: NTSC (Pin 48) = L $n = 1/m \times 10^6$ m	Ld (decimal)	PAL: NTSC (Pin 48) = H $n = 1/m \times 10^6$ m
255 to 248	$[261 - \{(255 - Ld) \times 7 + 2\}] \times 63.56 + 31$	255 to 251	$[311 - \{(255 - Ld) \times 10 + 2\}] \times 64 + 30.77$
247 to 241	$[261 - \{(247 - Ld) \times 5 + 58\}] \times 63.56 + 31$	250 to 243	$[311 - \{(250 - Ld) \times 7 + 52\}] \times 64 + 30.77$
240 to 232	$[261 - \{(240 - Ld0 \times 4 + 93\}] \times 63.56 + 31$	242 to 236	$[311 - \{(242 - Ld) \times 5 + 108\}] \times 64 + 30.77$
231 to 220	$[261 - \{(231 - Ld) \times 3 + 129\}] \times 63.56 + 31$	235 to 227	$[311 - \{(235 - Ld) \times 4 + 143\}] \times 64 + 30.77$
219 to 202	$[261 - \{(219 - Ld) \times 2 + 165\}] \times 63.56 + 31$	226 to 215	$[311 - \{(226 - Ld) \times 3 + 179\}] \times 64 + 30.77$
201 to 151	$[261 - \{(201 - Ld) \times 1 + 201\}] \times 63.56 + 31$	214 to 197	$[311 - \{(214 - Ld) \times 2 + 215\}] \times 64 + 30.77$
150 to 114	$[875 - \{(150 - Ld) \times 11 + 253\}] \times 0.978 + 0.047$	196 to 146	$[311 - \{(196 - Ld) \times 1 + 251\}] \times 64 + 30.77$
113 to 107	$[875 - \{(113 - Ld) \times 5 + 660\}] \times 0.978 + 0.047$	145 to 109	$[923 - \{(145 - Ld) \times 11 + 303\}] \times 0.987 + 0.721$
106 to 98	$[875 - \{(106 - Ld) \times 4 + 695\}] \times 0.978 + 0.047$	108 to 102	$[923 - \{(108 - Ld) \times 5 + 710\}] \times 0.987 + 0.721$
97 to 86	$[875 - \{(97 - Ld) \times 3 + 731\}] \times 0.978 + 0.047$	101 to 93	$[923 - \{(101 - Ld) \times 4 + 745\}] \times 0.987 + 0.721$
85 to 69	$[875 - \{(85 - Ld) \times 2 + 767\}] \times 0.978 + 0.047$	92 to 81	$[923 - \{(92 - Ld) \times 3 + 781\}] \times 0.987 + 0.721$
68 to 0	$[875 - \{(68 - Ld) \times 1 + 801\}] \times 0.978 + 0.047$	80 to 64	$[923 - \{(80 - Ld) \times 2 + 817\}] \times 0.987 + 0.721$
		63 to 0	$[923 - \{(63 - Ld) \times 1 + 851\}] \times 0.987 + 0.721$

Control pin	Detailed description

IRENB = Low: When the operation of electronic shutter is assigned

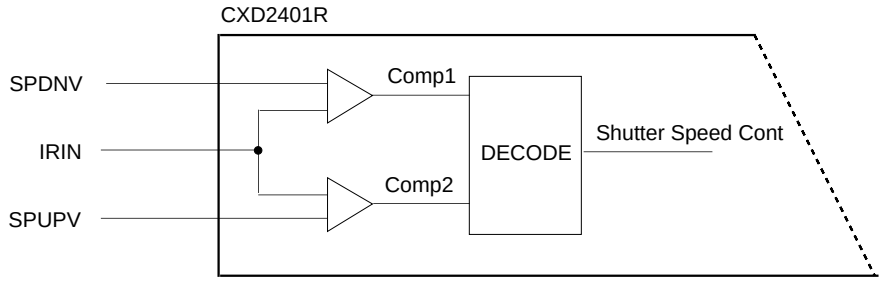
PS = High: When inputting parallel data is assigned

Shutter Speed Compatibility Chart

SPUPV	IRIN	SPDNV	Shutter speed (s)	
			NTSC(Pin 48) = L	NTSC(Pin 48) = H
H	H	H	1/100	1/120
L	H	H	1/250	1/250
H	L	H	1/500	1/500
L	L	H	1/1000	1/1000
H	H	L	1/2000	1/2000
L	H	L	1/5000	1/5000
H	L	L	1/10000	1/10000
L	L	L	1/100000	1/110000

SPUPV (Pin 38)
IRIN (Pin 39)
SPDNV (40Pin)

IRENB = High: When the operation of electronic iris is assigned



Comp 1 Truth Table

SPDNV	IRIN	Comp1
L	H	H
H	L	L

Comp 2 Truth Table

IRIN	SPUPV	Comp2
L	H	L
H	L	H

DECODE Truth Table

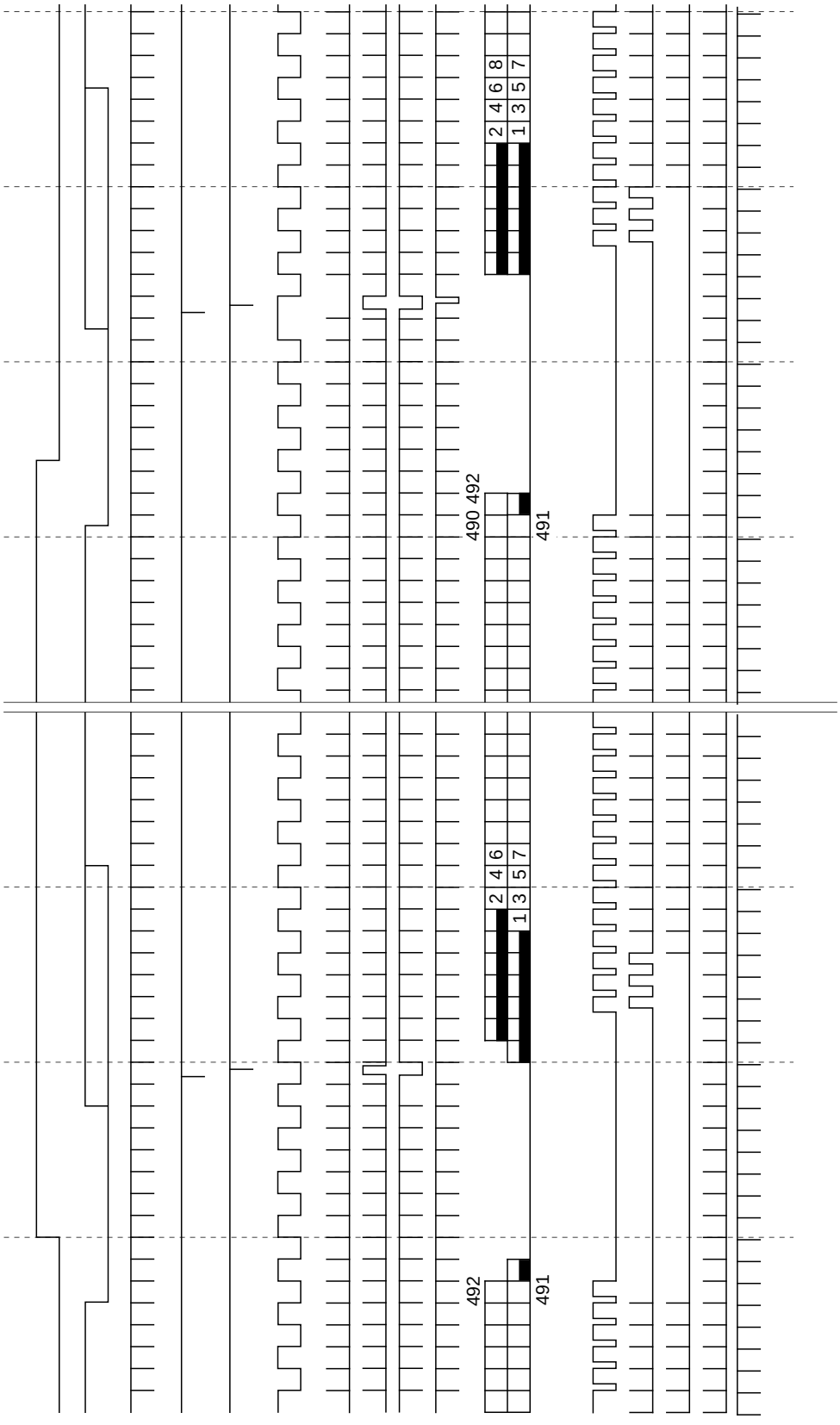
Comp1	Comp2	Shutter Speed Cont
L	L	Shutter speed; Faster
L	H	Shutter speed; Hold
H	L	Shutter speed; Hold
H	H	Shutter speed; Slower

In the electronic iris control operation, the electronic shutter speed is controlled according to the logic above. The variations of shutter speed by each control are the same as those shown in <Shutter speed calculation formula> for "electronic shutter; inputting serial data".

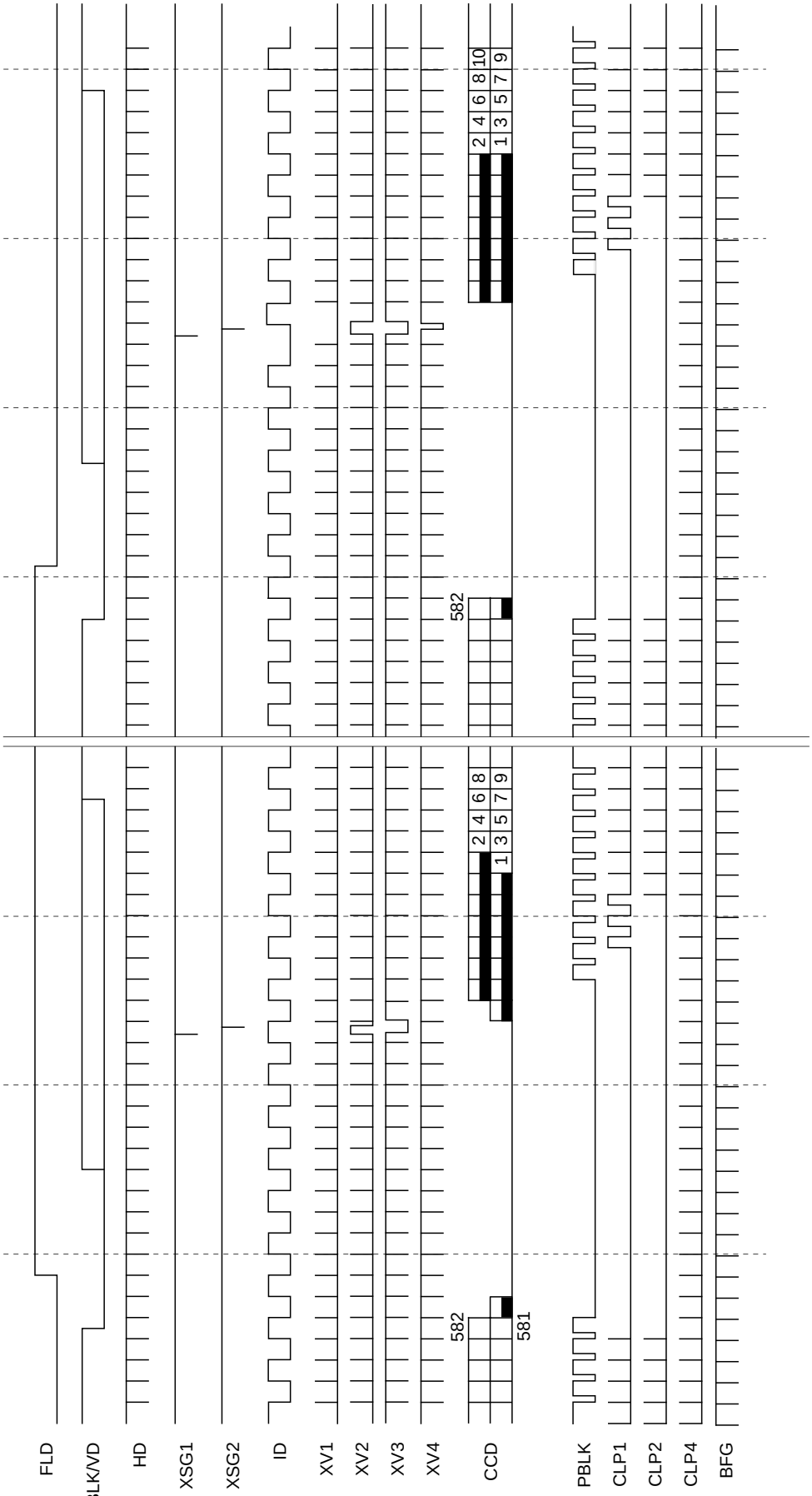
<table>
<tr><th>Control pin</th><th>Detailed description</th></tr>
<tr><td>LIMIT1
(Pin 46)
LIMIT2
(Pin 47)</td><td>
LIMIT1 and LIMIT2 pins function only when IRENB = High (when the operation of electronic iris is assigned).
(Inputs from LIMIT1 and LIMIT2 are not accepted when IRENB = Low: when the operation of electronic shutter is assigned.)

Maximum Electronic Shutter Speed
<table>
<tr><th rowspan="2">LIMIT1</th><th rowspan="2">LIMIT2</th><th colspan="2">Max. shutter speed (s)</th><th rowspan="2">Purpose</th></tr>
<tr><th>NTSC (Pin 48) = L</th><th>NTSC (Pin 48) = H</th></tr>
<tr><td>L</td><td>L</td><td>1/200</td><td>1/200</td><td>Reduces flickers caused by an indoor fluorescent lamp.</td></tr>
<tr><td>L</td><td>H</td><td>1/2000</td><td>1/2000</td><td>Intermediate mode between indoor and outdoor applications.</td></tr>
<tr><td>H</td><td>L</td><td>1/20000</td><td>1/20000</td><td>Reduces CCD smear outdoors.</td></tr>
<tr><td>H</td><td>H</td><td>1/90000</td><td>1/100000</td><td>Secures dynamic range of iris.</td></tr>
</table>
Electronic iris control of the CXD2401R is realized by applying functions of the electronic shutter. The electronic shutter has a dynamic range from 1/60s when Pin 48 (NTSC) = Low or from 1/50s when Pin 48 (NTSC) = High up to the maximum shutter speed in the table above.
Select one of the four dynamic ranges of the electronic iris, according to the application conditions of the CXD2401R. The dynamic range is also determined by also taking into consideration the influence of the electronic shutter on image quality, as shown in the table above.
</td></tr>
</table>

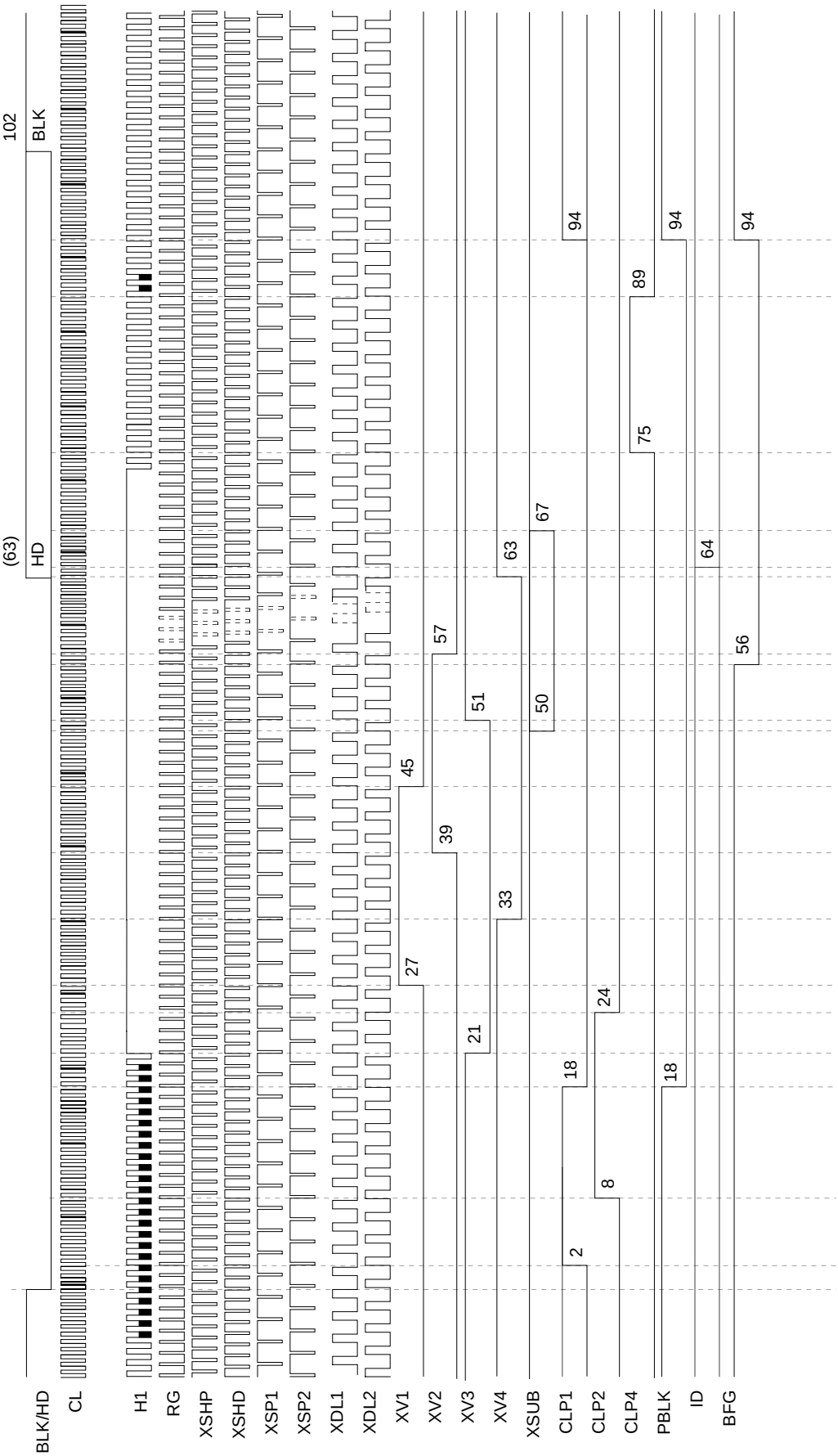
NTSC Vertical Direction Timing Chart



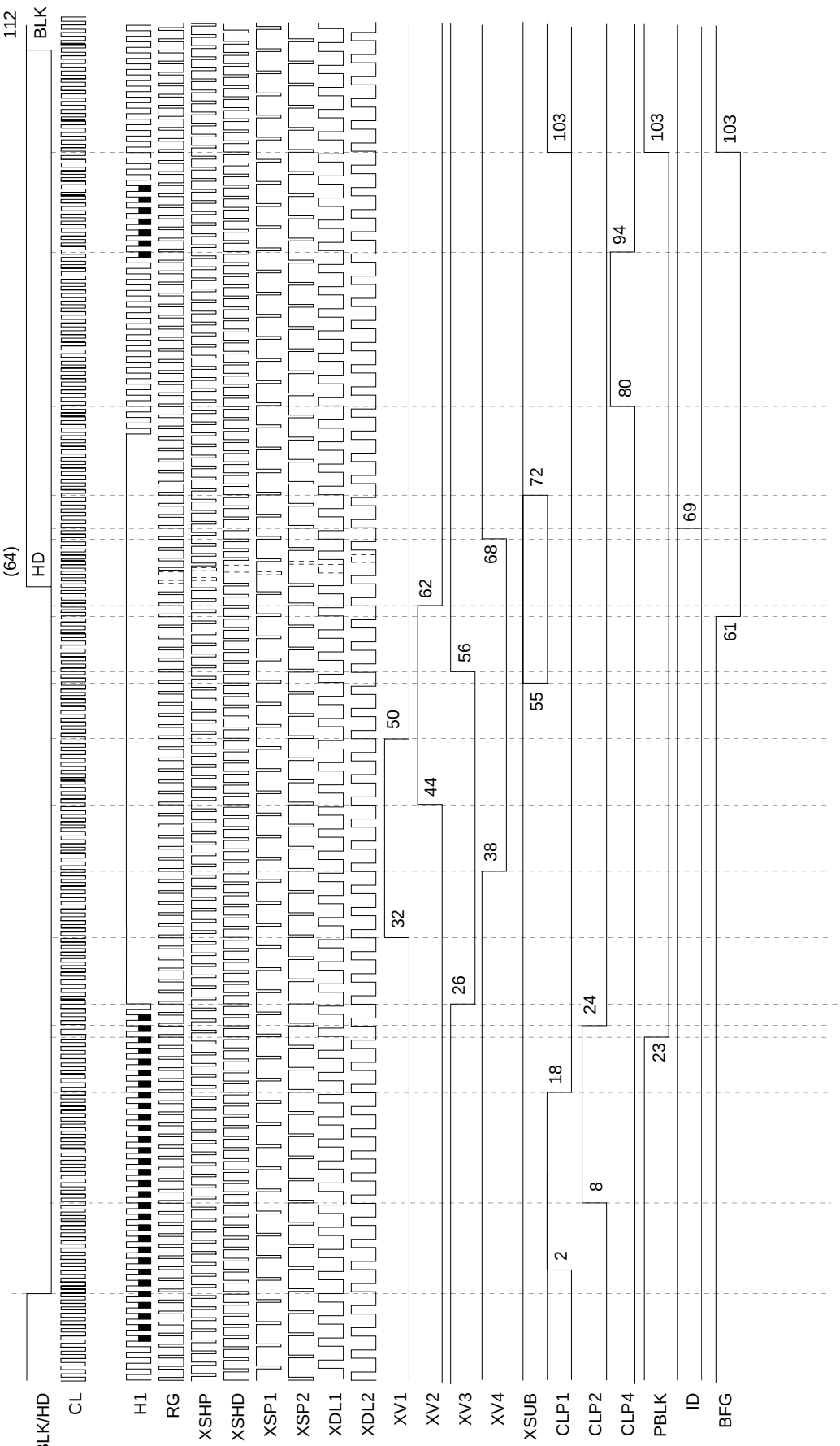
PAL Vertical Direction Timing Chart



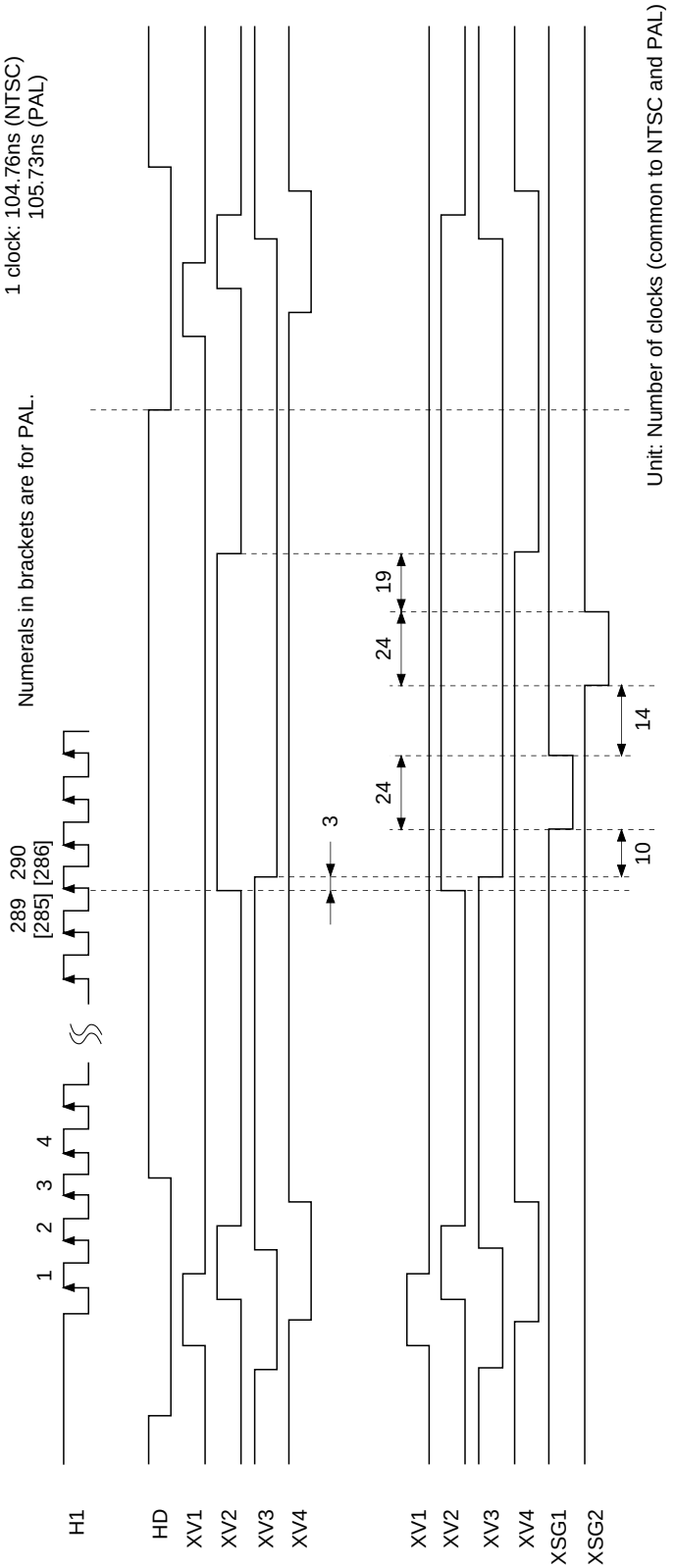
NTSC Horizontal Direction Timing Chart



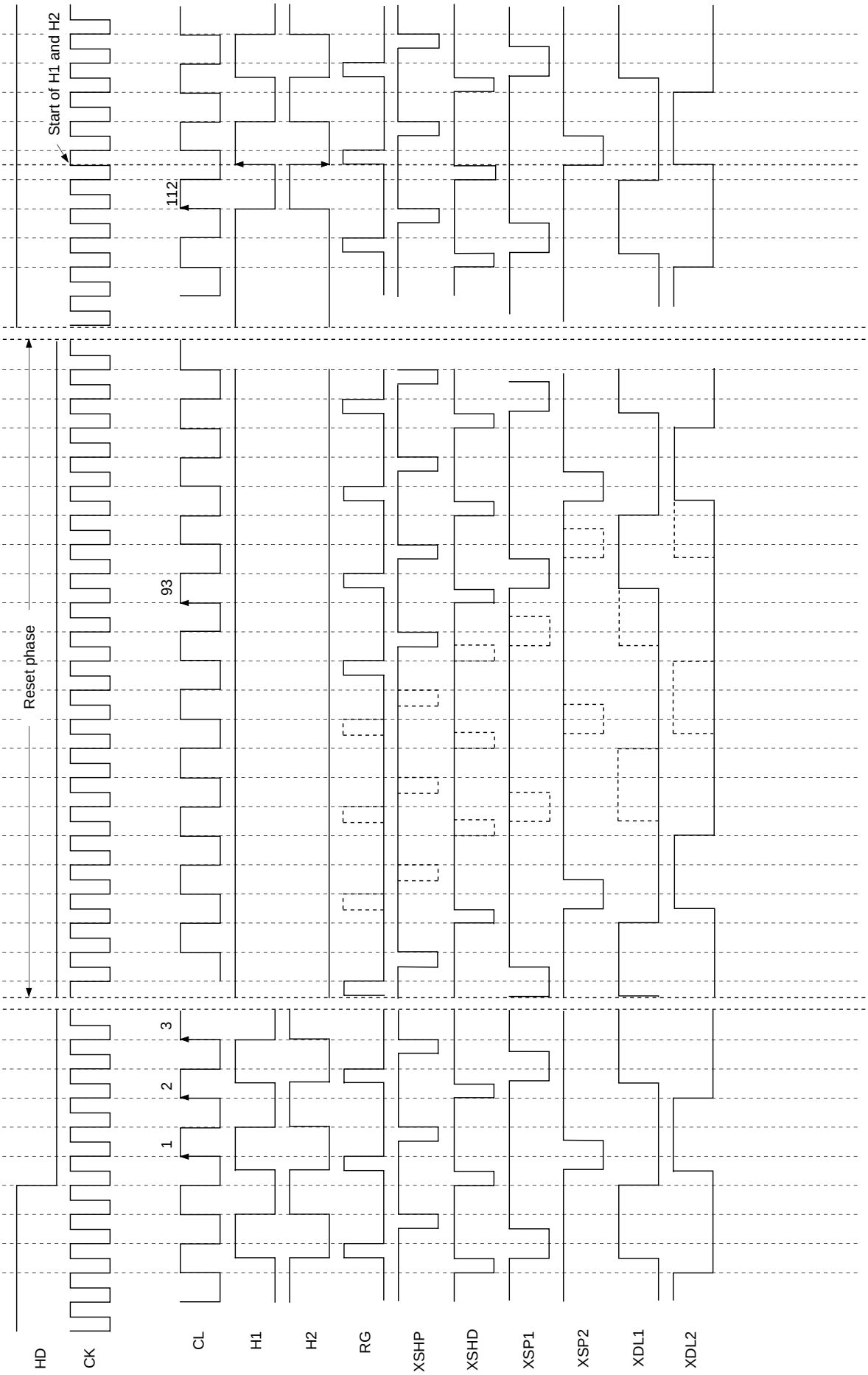
PAL Horizontal Direction Timing Chart



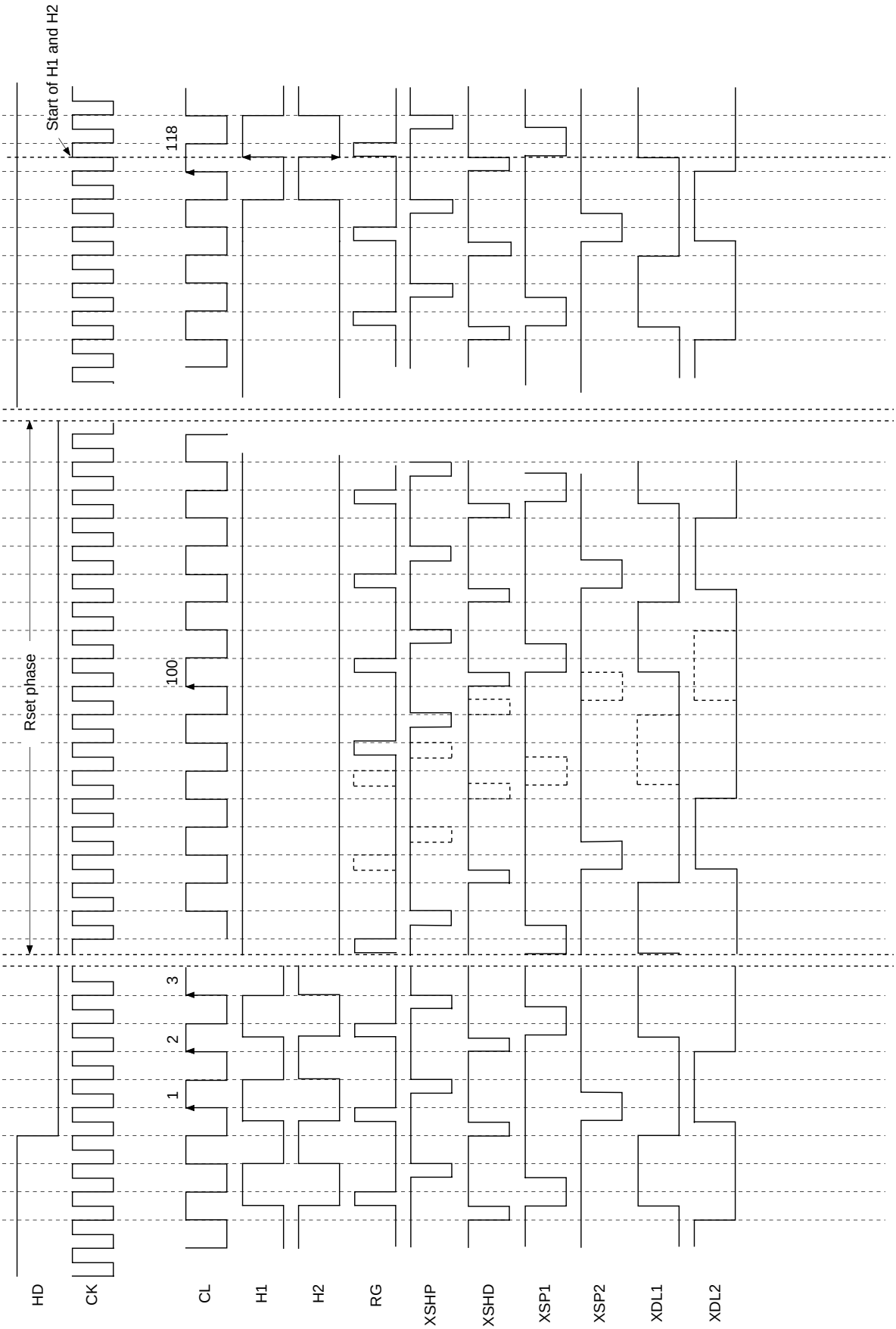
Readout Timing Chart



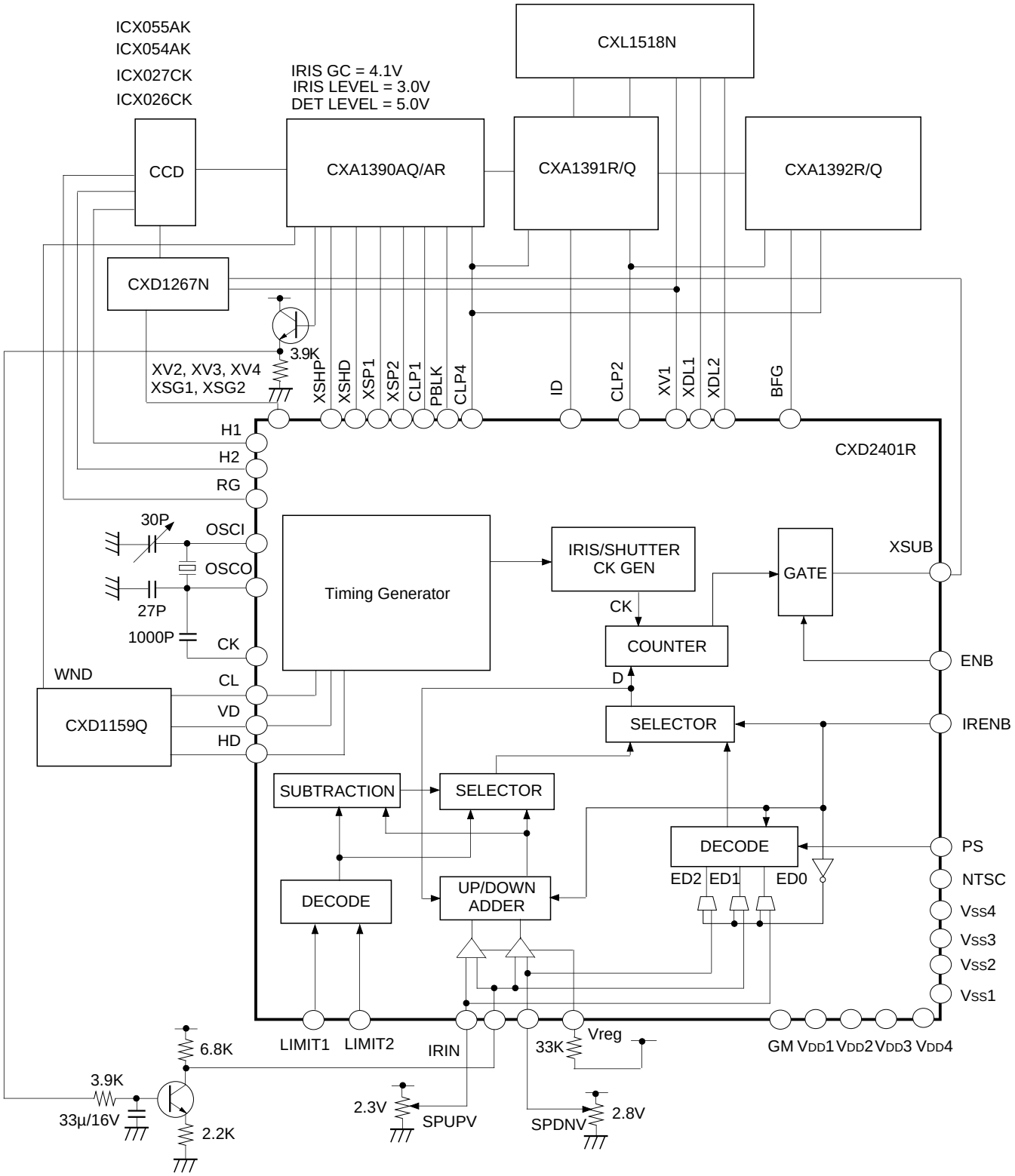
NTSC High-speed Phase Timing Chart



PAL High-speed Phase Timing Chart



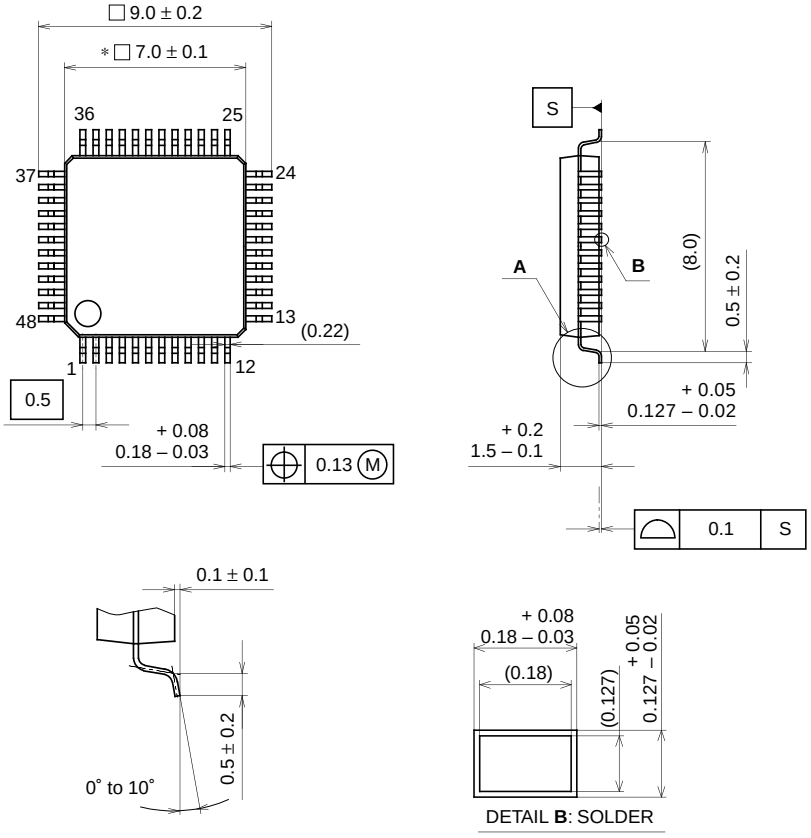
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

48PIN LQFP (PLASTIC)



DETAIL **A**

DETAIL **B**: SOLDER

NOTE: Dimension "∗" does not include mold protrusion.

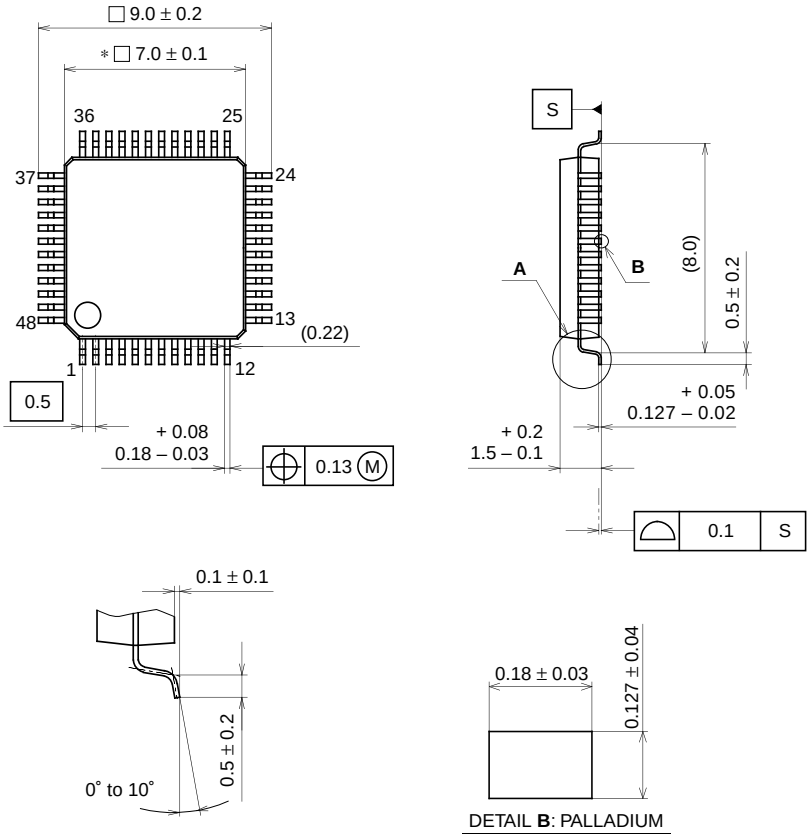
SONY CODE	LQFP-48P-L01
EIAJ CODE	P-LQFP48-7x7-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g

Package Outline Unit: mm

48PIN LQFP (PLASTIC)



DETAIL **A**

DETAIL **B**: PALLADIUM

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	P-LQFP48-7x7-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g