SH3100

Supervisory IC with I²C Interface and PWM

POWER MANAGEMENT

Description

The SH3100 is a size, power, and cost-saving solution for microprocessor support functions. It is intended to replace a number of peripheral devices normally used in conjunction with a microprocessor. Its prime function is to provide an accurate and stable clock source which can be started up and shut down very quickly to enable it to be used in a pulsed fashion for very low power applications.

The SH3100 consumes very little power when in standby, and it provides a stable output clock in less than 2µs. This allows it to outperform ceramic resonators and crystals requiring much longer start-up times.

Features

- Master HFDCO oscillator which can be programmed to between 8MHz and 33.5MHz with 2kHz resolution
- A 32.768kHz crystal oscillator with 5-bit programmable padding capacitance giving a frequency adjustment resolution of 4ppm
- Two clock outputs, each of which can be powered independently from V_{DD} or V_{BAK} and can operate either in-phase or in complementary mode
- An internal oscillator which is fuse-calibrated to provide a 32.768kHz clock source, accuracy is better than ±3% over temperature and supply voltage
- 96-bit electrically programmable non-volatile fuse memory array
- 7-bit programmable threshold reset comparator (VBO) between 1.7V and 4V with 24mV resolution
- Programmable reset duration between 6ms and 5.3 seconds
- Less than 10µA standby current and less than 12mA maximum operating current (excluding LDO load)
- I²C interface with 3-bit fuse-settable address complies with I²C fast mode specification
- General-purpose 8-bit DAC and Comparator
- General-purpose PWM & PDM output
- Programmable watchdog counter with a 7.8ms resolution up to 8 seconds delay
- Periodic interrupt timer (PIT) with a 30µs resolution up to 36 hours
- Real time clock with 1/256 second resolution up to Year 2099
- Spread spectrum option on the output clock
- Battery backup facility, which maintains register contents less than 2µA consumption
- 1.7V to 5.5V operating range on the main V_{DD} supply
- 0.9V to 5.5V operating range on the battery backup supply (V_{BAK})
- Edge-triggered, level-sensitive, and toggling interrupt output (INT)
- General-purpose I/O option on the interrupt pin (INT)
- Low power, low dropout voltage regulator (LDO) output on PWM pin
- Switched mode boost, bootstrap boost, and buck regulation control
- 56 bytes of control registers including a 9-byte scratchpad
- Small 3mm x 3mm 16-lead MLP package

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Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Pin Combination	Min	Max	Units
Supply voltages on VDD or VBAK relative to GND	0.5	5.5	V
Supply voltage on VREG when blowing fuses (1 second maximum)	3.6	3.7	V
Input voltage on CLKIN & INT	-0.5	VDD	V
Input voltage on SDA & SCL	-0.5	5.5	V
Input voltage on SNSE, XIN, XOUT	-0.5	VREG + 0.5	V
Input current on any pin (not VREG)		10	mA
Input current on VREG		150	mA
Ambient operating temperature for full specified performance	-40	85	°C
Ambient operating temperature for chip operation with de-rated performance	-40	125	°C
Storage temperature	-50	160	°C

Notes:
(1) The SH3100 is an ESD-sensitive device.
(2) Package ThetaJA is 100°C/Watt. This should be used to determine core temperature increase based on power dissipation.

Current Consumption

The following table shows the maximum current consumption figures from VDD and VBAK under a number of possible operating conditions.

Battery Backup Modes

State	Condition	MAX VBAK Current
Battery backup 1	Crystal oscillator and RTC running from VBAK; VDD is zero	2µA
Battery backup 2	Internal 32.768kHz oscillator and RTC running from VBAK; VDD is zero	12µA

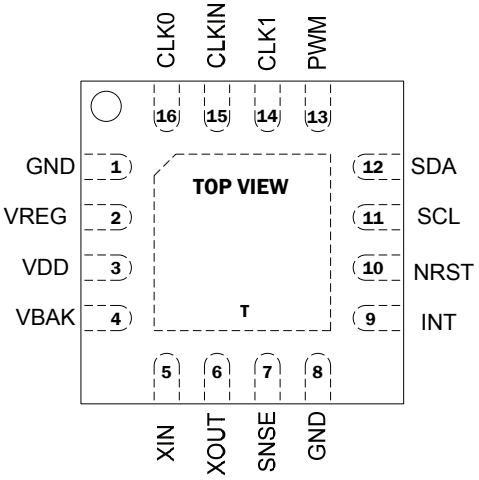
Normal Operating Modes

State	Condition	MAX VDD Current
Standby	32.768kHz system clock, programmable reset, RTC and logic enabled	10µA
Auto-fan mode	Automatic fan mode with 32.768kHz output on CLK0; HFDCO disabled	15µA
Switching regulator standby	Switching regulator maintaining 10µA load with occasional active burst to maintain supply level	20µA
LDO standby	Standby but with LDO running on no load	250µA
Start-up	Current consumed during chip startup	1mA
Active	Up to 33.5MHz output clock enabled on both CLK0 and CLK1; 20pF load on each	12mA
Programming	Simultaneous blowing of up to eight fuses	100mA

Note: At temperatures above 40°C, the above figures start to increase due to leakage. Expect +2µA at 60°C, and +6µA at 80°C.

Note: VBAK current in normal operation mode is dependent on clock feedthrough from CLK0 & CLK1 to VBAK. Under worst-case conditions with CLK output at 33MHz and VDD = 5.5 V, VBAK input current could be up to 2µA. At lower frequencies, VBAK current drops to approximately 50nA. This effect is related to the same phenomenon as described in the VBAK protection section, and the net feedthrough current on to VBAK may be positive or negative, dependent on VDD and VBAK voltage levels.

Pin Configuration



MLPQ16: 3X3 16 LEAD

Ordering Information

Device	Package[2]
SH3100IMTR[1]	16-Pin MLP 3mm x 3mm x 0.9mm
SH3100IMLTRT[2]	

Notes:

1) Available in tape and reel packaging only. A reel contains 3000 devices.

2) Available in lead-free packaging only. This product is fully WEEE, RoHS and J-TD-020B compliant. This component and all homogenous subcomponents are RoHS compliant.

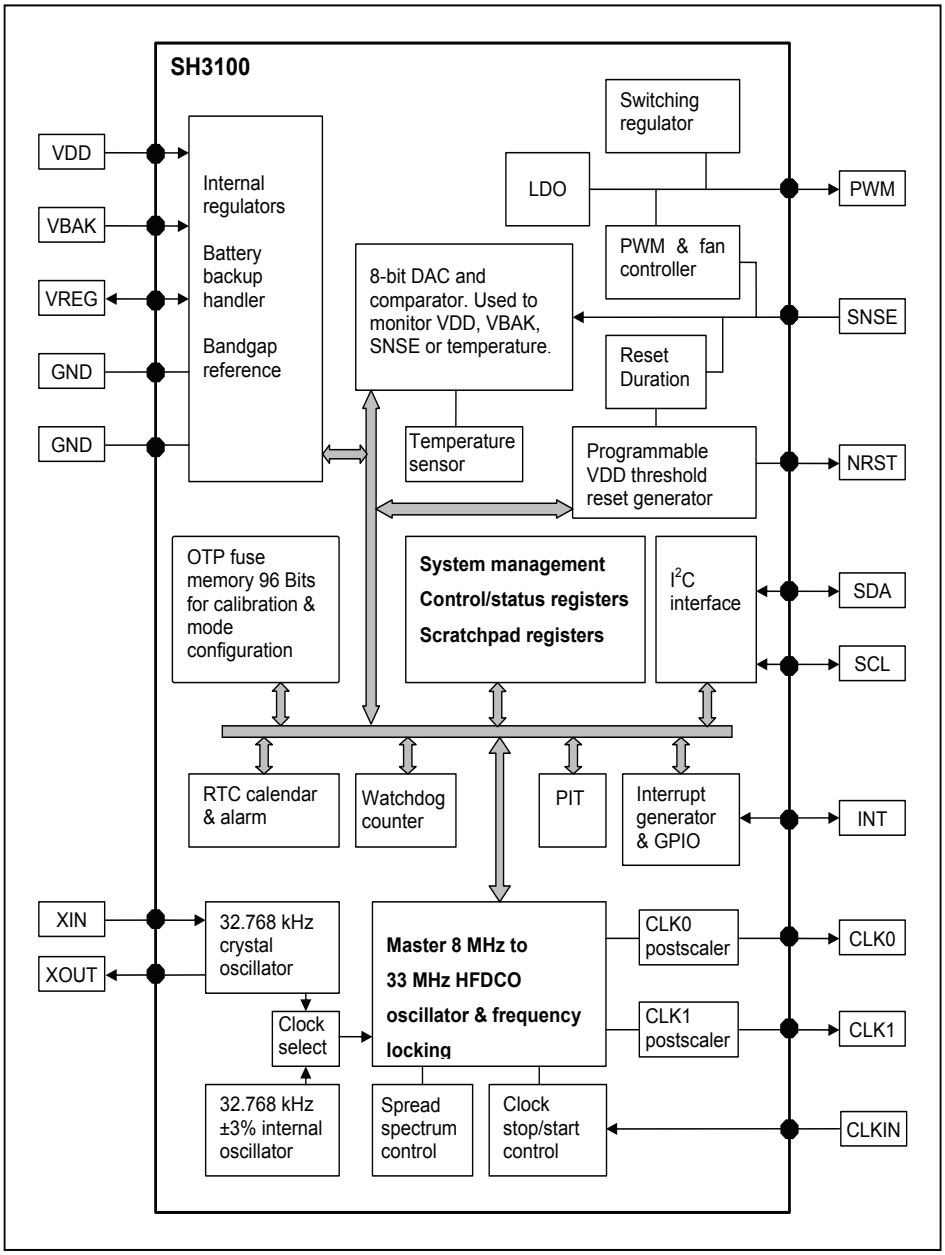
Pin Descriptions

Pin #	Pin Name	Pin Function
1	GND	Ground
2	VREG	1.6V regulated digital supply - generated internally from VDD - collapses to GND during battery backup - may be left unconnected
3	VDD	Main supply (range is 1.7V to 5.5V)
4	VBAK	Backup battery supply to maintain register contents and RTC operation when VDD collapses - can be higher or lower than VDD - range is 0.9V to 5.5V - connect to VDD if not used
5	XIN	32.768kHz crystal oscillator input pin - tie to ground if not used - can be over driven by external clock source up to 250kHz
6	XOUT	32.768kHz crystal oscillator output pin - leave unconnected if not used
7	SNSE	Sense input for fan speed control - spare analog input for switching regulator feedback or ADC conversion - tri state (low, floating, or high) input pin used to select reset duration
8	GND	Ground
9	INT	Level, edge or toggling interrupt output, general-purpose input/output (GPIO)
10	NRST	Active-low system reset output - strong pull-down - weak pull-up - reset state is valid for VDD levels down to 1V - can be externally over driven to trigger programmed duration reset
11	SCL	I²C clock - 400kHz fast mode compliant - operates up to 1MHz
12	SDA	I²C data - 400kHz fast mode compliant - operates up to 1MHz
13	PWM	General-purpose PWM or PDM output - fan control PWM output - LDO output regulated down from VDD - programmable 3V to 4.5V in 18mV steps - 15mA drive capability - switching regulator control output - drives Inductor directly in bootstrap boost mode, or external switching FETs or bipolar transistors - directly drives inductor in bootstrap boost with internal switching

Pin Descriptions (*continued*)

Pin #	Pin Name	Pin Function
14	CLK1	Secondary clock output - can be powered from either V_{DD} or V_{BAK}
15	CLKIN	System clock input - used to detect processor-initiated clock STOP
16	CLK0	Primary clock output - can be powered from either V_{DD} or V_{BAK}
T	PAD	Thermal pad for heatsinking purposes - not connected internally - connect to system ground plane with multiple vias

Block Diagram



Power Supplies & Battery Backup

The main power supply is between VDD and GND and may have any value between 1.7V and 5.5V for normal operation. In order to guarantee start-up, VDD should initially be taken to at least 100mV above the reset threshold (VBO) in order to overcome the reset threshold hysteresis; e.g., for a VBO level of 2.8V, VDD must initially rise to at least 2.9V for the chip to come out of reset.

The battery backup supply is between VBAK and GND. The SH3100 switches to VBAK, if VDD drops below VBO and VBAK is within its valid operating range of 0.9V to 5.5V for battery backup.

While VBAK is within its valid operating range during battery backup, RTC operation is maintained and those register contents not reset by a VBO reset event (Brownout) are maintained. Any functions not required during battery backup are shut down to save power.

Note: If the 32.768kHz system clock output is enabled on CLK1 during battery backup then the maximum VBAK voltage for valid CLK1 output is 4.5V. Battery backup continues for VBAK voltages above 4.5V, but the CLK1 output is no longer guaranteed to function correctly.

When running in battery backup from the 32.768kHz crystal oscillator, full RTC accuracy is maintained down to the minimum VBAK of 0.9V.

When running in battery backup from the internal 32.768kHz oscillator, RTC accuracy is maintained only down to a VBAK level of 1.7V. Below this point, operation continues down to 0.9V, but a flag is set to indicate that the internal oscillator can no longer be guaranteed to be within ±3% of 32.768kHz.

The minimum VBAK level is guaranteed as 0.9V; however, depending on process variations, operation may continue down to 0.7V before battery back up fails.

An unpowered (cold) chip starts up and initializes only when VDD is applied. Applying only VBAK to a cold chip does not cause it to start up.

Battery backup facility is only enabled once the chip has come out of reset after an initial power-up.

VBAK Protection

To avoid degradation of Lithium cells connected to VBAK, charging current over the operating lifetime needs to be limited to less than 3% of the cell capacity. It is therefore necessary to limit any current flowing from VDD to VBAK.

On the SH3100, VDD and VBAK have diode protection structures, so VDD and VBAK can independently have any DC voltage between 0 V and 5.5V, and no DC current flows between VDD and VBAK in either direction.

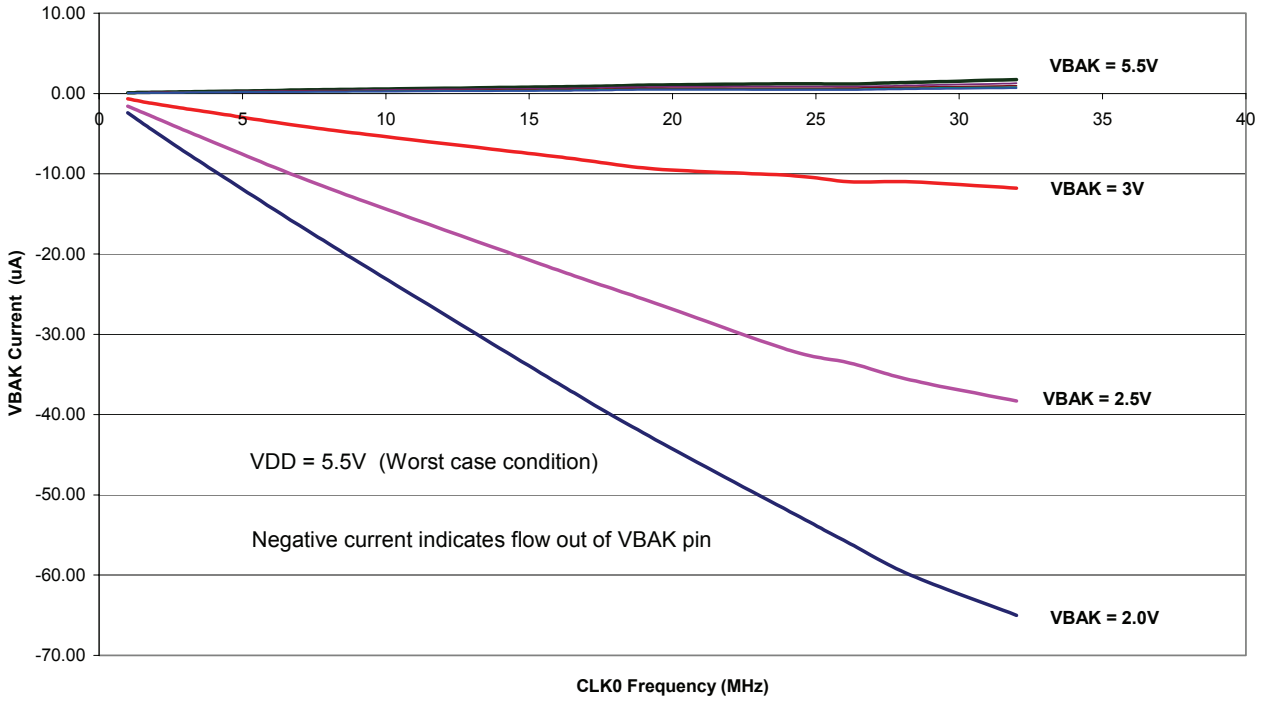
However, since CLK0 and CLK1 may be powered either from VDD or VBAK, there is capacitance between CLK0 or CLK1 and VBAK, so an AC signal on CLK0 or CLK1 powered by VDD would couple some net current through to VBAK. This current coupling is proportional to frequency and to the voltage differential between VDD and VBAK.

The following graph shows the variation in reverse current from VDD to VBAK versus CLK frequency for different settings of VBAK. VDD is fixed at 5.5V, which is the worst-case condition. Note that as VBAK approaches VDD, the net current changes direction so that it flows into VBAK.

Note: If the SH3100 is operated at clock frequencies and supply levels that mean that current flow out of VBAK into the battery would be a problem, then one solution would be to use a series diode between the battery and VBAK to inhibit any reverse current. This lowers the battery voltage by 0.7V on to VBAK; however, since VBAK can go as low as 0.9V, this is unlikely to be a problem for lithium cells.

As additional protection, if the battery is connected in reverse, then a large protection diode between VBAK and GND means that VBAK limits at approximately 0.7V below GND depending on the current flowing through the diode. A safe maximum current through this protection diode is 10mA. The SH3100 continues to function normally (apart from battery backup) while VBAK is negative.

SH3100 R1: VBAK Current versus CLK0 Frequency for different VBAK values



Operating Modes

The SH3100 is fuse programmed to a default power-up operating mode from a number of possible options. Once the device has been initialized, it is possible to use the I²C interface to change between any of the following available modes.

Mode	LDO	Switching Regulator	Fan Control	Reset Duration	Notes
1	NO	NO	NO	YES	Standard operating mode. PWM pin may be used as general-purpose PWM/PDM output. INT defaults to high impedance and may then be programmed by I²C access to define an Interrupt function or GPIO as required. Start-up frequency is determined by configuration fuse setting
2	YES	NO	NO	NO	LDO is enabled on PWM pin with default output voltage between 3V and 4.5V as set by fuses. Setting may then be overridden by I²C access
3	NO	NO	YES	NO	Automatic fan control is enabled with SNSE input used to detect fan rotation and PWM pin used for fan drive
4	NO	YES	NO	NO	Bootstrap boost regulation from an external supply to VDD with internal switching FET and transfer diode on PWM pin. Regulator feedback is determined by the internal VDD divider. The PWM pin is active low during the inductor energize period and floating during the transfer period (to allow current to flow from PWM to VDD through the internal diode). During power up, the PWM pad is clamped to VDD to ensure that the chip can start up with an input battery supply as low as 1.8V. Conversion efficiency is very low due to the relatively high internal switching FET and diode impedances, so this mode is recommended only for powering the SH3100 alone and where energy efficiency is not important
5	NO	YES	NO	NO	Bootstrap boost regulation from an external supply to VDD with external switching FET and transfer diode. Regulator feedback is determined by the internal VDD divider. This is suitable for heavier load requirements and is limited by the capabilities of the external components. The PWM pin drives an external NMOS or NPN switching the inductor to GND, and is High during the inductor energize period and Low during the transfer period (to allow current to flow through the external diode)
6	NO	YES	NO	NO	Normal boost regulation from VDD to a separate supply with external switching FET and transfer diode. Regulator feedback is input on the SNSE pin. The PWM pin drives an external NMOS or NPN switching the inductor to GND, and is High during the inductor energize period and Low during the transfer period

Note: The Reset Duration column refers to the option to select Low, Medium or fuse set reset durations by the tristate input SNSE pin. If this option is not available then the reset duration defaults to the fuse setting.

Operating Modes *(continued)*

Mode	LDO	Switching Regulator	Fan Control	Reset Duration	Notes
7	NO	YES	NO	NO	Normal boost regulation from VDD to VBAK with external switching FET and transfer diode. Operation is as mode six but regulator feedback is determined by the internal VBAK divider
8	NO	YES	NO	NO	Buck regulation from VDD to a separate supply with external switching FET and transfer diode. Regulator feedback is input on the SNSE pin. The PWM pin drives an external PMOS or PNP switching the inductor to VDD and is Low during the inductor energize period and High during the transfer period (to allow current to flow through the external diode)
9	NO	YES	NO	NO	Buck regulation from VDD to VBAK with external switching FET and transfer diode. Operation is as mode 8 but regulator feedback is determined by the internal VBAK divider

Application Diagrams - Modes 1 to 3

Mode 1 – Standard operation

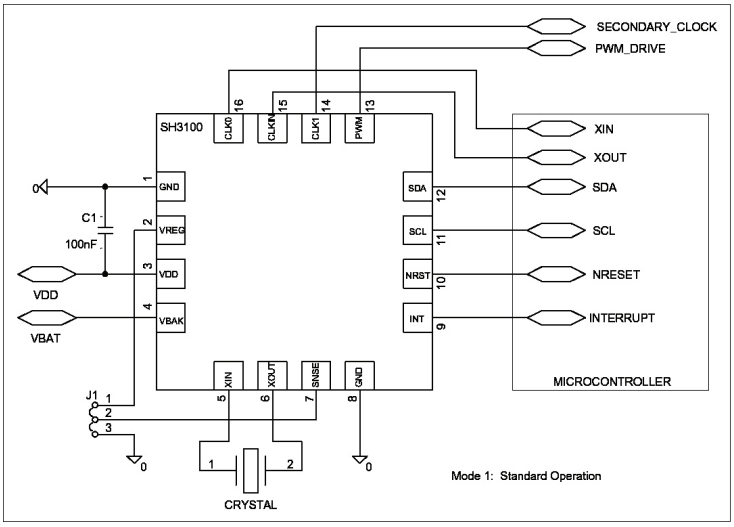
No LDO, fan control or switching regulation.

General purpose PWM/PDM output is available

Use with or without external 32.768 kHz crystal

Register settings

- *DeviceMode* = 000

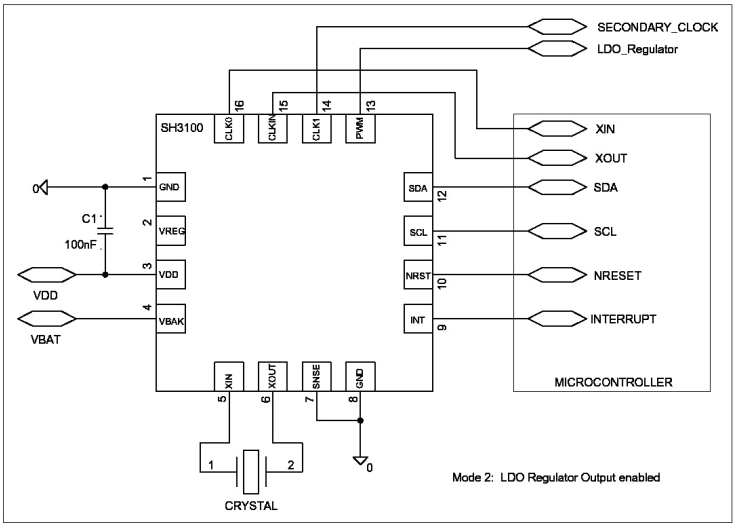


Mode 2 – LDO enabled

As standard operation but with PWM output pin programmed as LDO output. (Linearly regulated down from VDD).

Register settings

- *DeviceMode* = 100
- *ForcedDACValue* = xx (to set LDO voltage)



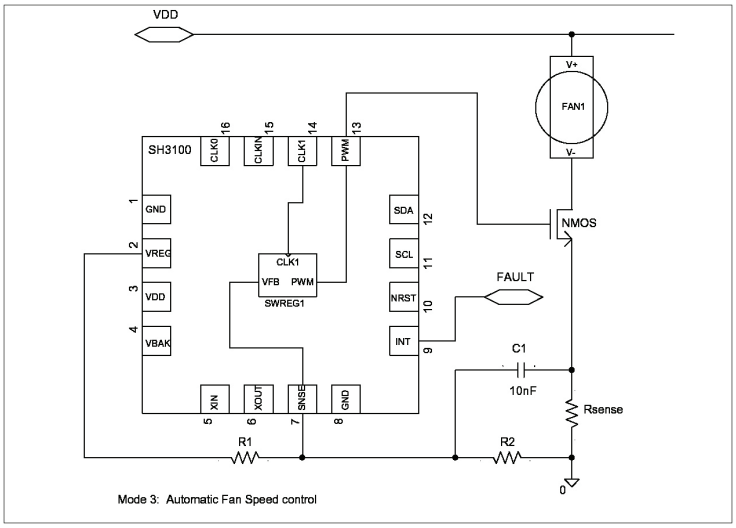
Mode 3 – Auto fan speed control

Fan speed is automatically controlled by measuring temperature at regular intervals and adjusting PWM duty cycle according to configurable control parameters.

SNSE pin is monitored to detect possible fan stall

Register settings

- *DeviceMode* = 101
- *ComparatorSource* = 11 (SNSE)
- CLK1HF/LF = 0
- *ForcedDACValue* = xx (to override 70 mV SNSE threshold if required)



Application Diagrams - Modes 4 to 6

Mode 4 – Bootstrap boost regulation using internal switching FET

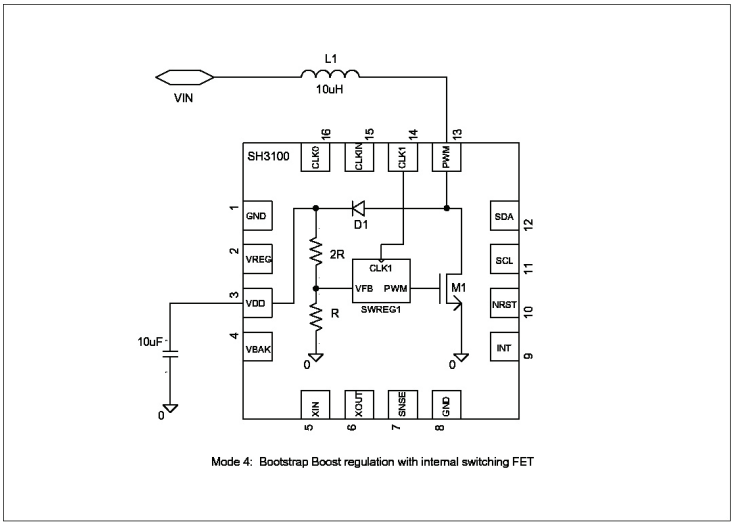
VDD is stepped up from external supply source using internal switching on PWM.

Starts up with external supply as low as 1.8 V and continue to operate as external supply drops as low as 1 V.

Regulation timing for all switching regulator modes is set by internal programmable HFDCO oscillator.

Register settings

- *DeviceMode* = 001
- *ComparatorSource* = 00 (VDD)
- CLK1HF/LF = 1
- *ForcedDACValue* = xx (to set VDD level)
- Set CLK1 frequency as desired



Mode 4: Bootstrap Boost regulation with internal switching FET

Mode 5 – Bootstrap boost regulation using external switching FET.

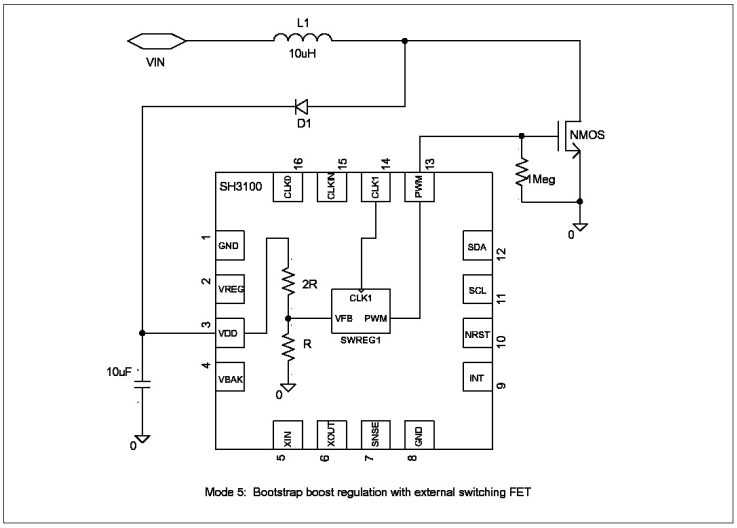
VDD is stepped up from external supply source using external switching FET controlled by PWM. Use for higher load requirements.

Regulated output voltage is set by internal DAC8. Feedback is fixed as VDD/3.

1Mohm pull-down resistor is required to indicate external switching configuration to SH3100.

Register settings

- *DeviceMode* = 001
- *ComparatorSource* = 00 (VDD)
- CLK1HF/LF = 1
- *ForcedDACValue* = xx (to set VDD level)
- Set CLK1 frequency as desired



Mode 5: Bootstrap boost regulation with external switching FET

Mode 6 – Normal boost regulation using external FET & external feedback divider

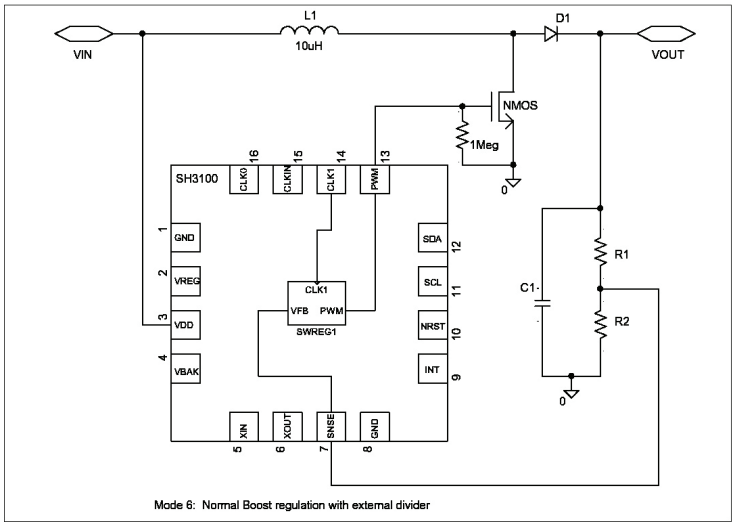
Regulated supply is stepped up from VDD using external switching FET controlled by PWM.

Regulated output voltage is set by internal DAC8 and feedback on SNSE.

1Mohm resistor indicates external switching and also ensures NMOS is turned off during power up

Register settings

- *DeviceMode* = 001
- *ComparatorSource* = 11 (SNSE)
- CLK1HF/LF = 1
- *ForcedDACValue* = xx (to set VDD level)
- Set CLK1 frequency as desired



Mode 6: Normal Boost regulation with external divider

Application Diagrams - Modes 7 to 9

Mode 7 – Normal boost regulation using external FET & internal feedback divider

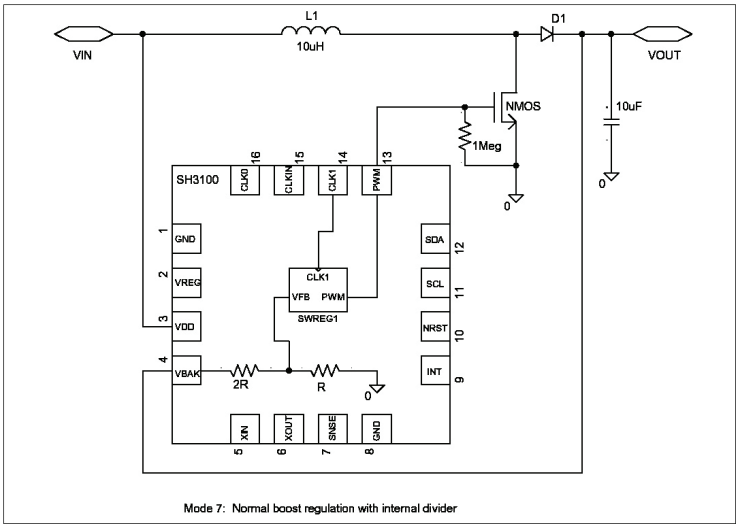
VBAK is stepped up from VDD using external switching FET controlled by PWM.

Regulated output voltage is set by internal DAC8. Feedback is fixed as VBAK/3.

1 MOhm resistor indicates external switching and also ensures NMOS is turned off during power up

Register settings

- *DeviceMode* = 001
- *ComparatorSource* = 01 (VBAK)
- CLK1HF/LF = 1
- *ForcedDACValue* = xx (to set VDD level)
- Set CLK1 frequency as desired



Mode 7: Normal boost regulation with internal divider

Mode 8 – Buck regulation using external FET & external feedback divider

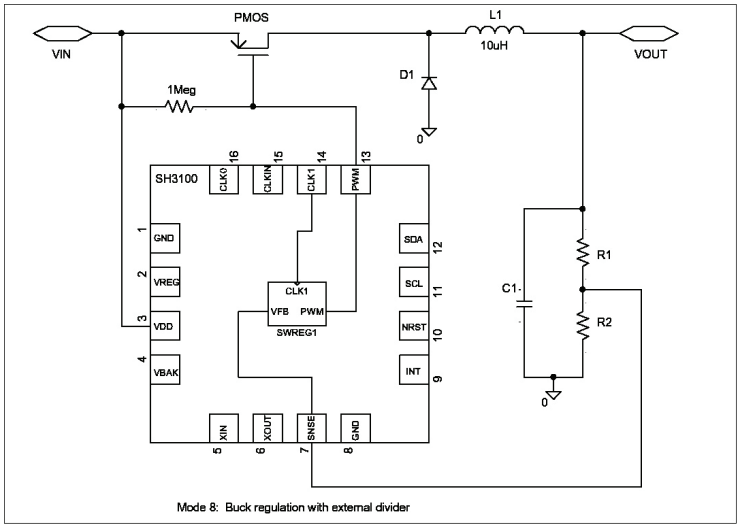
Regulated supply is stepped down from VDD using external switching FET controlled by PWM.

Regulated output voltage is set by internal DAC8 and feedback on SNSE.

1 MOhm resistor indicates external switching and also ensures PMOS is turned off during power up

Register settings

- *DeviceMode* = 011
- *ComparatorSource* = 11 (SNSE)
- CLK1HF/LF = 1
- *ForcedDACValue* = xx (to set VDD level)
- Set CLK1 frequency as desired



Mode 8: Buck regulation with external divider

Mode 9 – Buck regulation using external FET & internal feedback divider

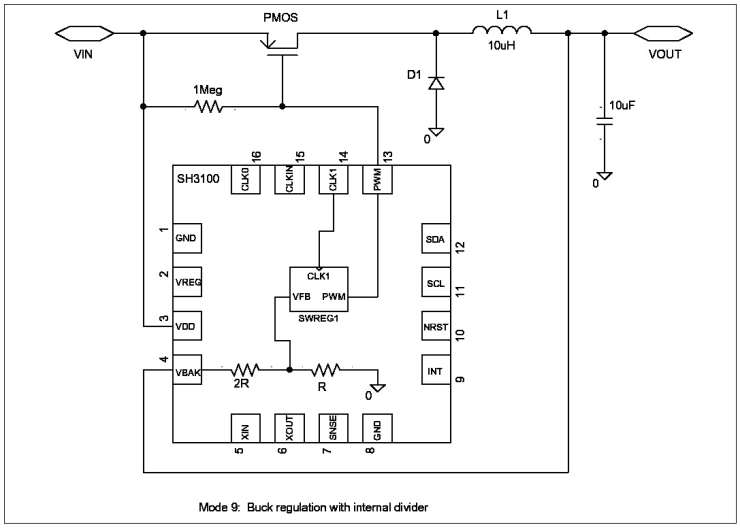
Regulated supply is stepped down from VDD to VBAK using external switching controlled by PWM.

Regulated output voltage is set by internal DAC8. Feedback is fixed as VBAK/3.

1 MOhm resistor indicates external switching and also ensures PMOS is turned off during power up

Register settings

- *DeviceMode* = 011
- *ComparatorSource* = 01 (VBAK)
- CLK1HF/LF = 1
- *ForcedDACValue* = xx (to set VDD level)
- Set CLK1 frequency as desired



Mode 9: Buck regulation with internal divider

Non-Volatile Fuse Memory Registers

The 96-bit non-volatile fuse memory contains the calibration and configuration control registers. The transfer column indicates under which conditions the fuse contents are transferred to the chip control registers. Fuses are blown on test and are extremely robust. There is no mechanism to reset fuses once blown. Calibration fuses are always set to obtain the required parametric specifications. Application fuses are set as required.

P Power on reset. (Power first applied)
B Brownout (VDD drops below VBO threshold)
W Watchdog reset event
R Forced fuse read initiated by I²C access

Fuse Register	Type	Bits	Range of Values	Transfer
Bandgap reference	Calibration	4	Bandgap set to 1.17V ±1%	P, W, R
Internal 32.768kHz ±2% oscillator	Calibration	10	Set to 32.768kHz ±128Hz at 25°C	P, W, B, R
Temperature sensor trim	Calibration	4	Temperature sensor set to ±2°C accuracy	P, W, B, R
VDD reset threshold (VBO)	VBO Reset	7	1.7V to 4	P, W, R
Chip reset duration	Application	5	6ms to 6 seconds	P, W, R
Crystal load capacitance	Application	5	5pF to 22pF	P, R
Master HFDCO clock FLL control Frequency is code x 2.048kHz Accuracy is defined by 32.768kHz source	Application	14	8MHz to 33. MHz	P, W, B, R
Master HFDCO clock start-up frequency Direct HFDCO control if FLL disabled Frequency versus code varies with process	Application	16	Nominally 6MHz to 42MHz	P, W, B, R
CLK0 postscaler	Application	3	1 to 128	P, W, B, R
CLK1 postscaler	Application	4	1 to 32768	P, W, R
Spread-spectrum amplitude	Application	2	32kHz to 128kHz	P, W, B, R
Spread-spectrum enable	Application	1	On or Off	P, W, B, R
CLK1 output enable	Application	1	On or Off	P, W, R
CLK1 switch to VBAK supply	Application	1	On or Off	P, W, R
CLK1 output invert	Application	1	On or Off	P, W, R
CLK1 force to 32.768kHz source	Application	1	On or Off	P, W, R
Chip mode select	Application	3	Normal, boost, buck, LDO, fan control	P, W, R
I²C slave address	Application	3	1 of 8 addresses	P, W, B, R
Regulator start-up voltage	Application	4	1.9V to 4.5V	P, W, R

Non-Volatile Fuse Memory Registers

Fuse Register	Type	Bits	Range of Values	Transfer
Comparator input Mux select	Application	2	VDD, VBAK, temperature, SNSE	P, W, R
Application fuse write-protect	Protection	1	On or Off	P, W, R
VBO threshold write-protect	Protection	1	On or Off	P, W, R
Calibration fuse write-protect	Protection	1	On or Off	P, W, R
Unused	Spare	2	N/A	N/A

SH3100 Default Settings

During production test, the calibration fuses are set as required to trim out process variations. For this device, the start-up configuration fuses are set as follows:

ADDR	Register	Bits	Description	Value	Fuse Setting
0 x 17	DAC Value	[7:0]	Sets default value on the 8-bit DAC if the LDO or switching regulator modes are selected	660mV	01101010
0 x 18	Device mode	[5:3]	Default start-up operating mode	Auto-fan	101
0 x 19	Comparator source	[1:0]	Selects comparator source	SNSE	11
0 x 20	CLK0 postscaler	[2:0]	Set HFDCO to CLK0 divider ratio	8	011
0 x 21	CLK1 supply	[7]	Sets CLK1 supply to VDD or VBAK	VDD	0
	CLK1 HF/LF	[6]	Sets CLK1 to HF or LF	LF	0
	Invert CLK1	[5]	Inverts CLK1 output	Off	0
	CLK1 enable	[4]	CLK1 output enable	Off	0
	CLK1 postscaler	[3:0]	Set HFDCO to CLK1 divider ratio	1	0000
0 x 22	SS enable	[7]	Enable HFDCO spectrum spreading	Off	0
	SS configuration	[6:5]	Spectrum spreading bandwidth	32kHz	00
0 x 23	FLL set frequency (MSB)	[5:0]	MSB of the FLL set frequency. Locked to 32.768kHz crystal	8MHz	001111
0x24	FLL set frequency (LSB)	[7:0]	LSB of the FLL set frequency; locked to 32.768kHz crystal	8MHz	01000001
0x30	Reset threshold	[6:0]	VBO reset threshold	2.93V	0110010
0x31	Reset duration	[4:0]	Reset duration	222ms	01101
0x42	Xtal padding capacitance trim	[4:0]	Crystal load capacitance	11.5pF	00110
0x44	HFDCO start-up frequency	[18:0]	Master HFDCO start-up frequency. Use for direct HFDCO control if FLL disabled. Frequency versus code varies with process	8 MHz	Device Dependent
0x45					
0x46					
0x47	I²C Slave address	[2:0]	LSB of I²C slave address. (MSB fixed at 0100)	000	000
0x49	Application fuse protect	[2]	Application fuse write protect	Off	0
	VBO reset fuse protect	[1]	VBO threshold fuse write protect	Off	0
	Calibration fuse protect	[0]	Calibration fuse write protect	On	1

Register Memory Map

Each register and register group is described in the following register memory map and subsequent register description tables.

Register Organization

The SH3100 uses a total of 53 8-bit registers, identified by a register name and corresponding hexadecimal register address. They are presented here in ascending order by register address. Some registers carry several individual data fields of various sizes; from single-bit values (e.g. flags), upwards. Several data fields are spread across multiple registers, as shown in the register map. Shaded areas in the map are 'don't care' and writing either 0 or 1 does not affect any function of the device. Cross-hatched areas denote registers which are initialized at startup from the on-chip fuse memory.

CAUTION! Do not write to any undefined register addresses, as this may cause the device to operate in a test mode. If an undefined register has been inadvertently addressed, the device should be reset to ensure the undefined registers are at default values.

Register Initialization from Fuses

Some register bits are initialized from the fuse memory on power-up and following selective reset events. All these bits can be overwritten by software once the reset signal NRST has been negated, unless the relevant write-protect fuse has been set. The fuses define only the default, power-on state of the device. The registers which are fuse-initialized are denoted in the register map with cross-hatching.

Multi-Word Registers

The RTC, *PeriodicTimer* (PIT), *WakeupTime* and *DCOCode* are multi-byte registers. The least significant byte (LSB) must be the last of the set to be written, after which their combined value takes effect. Conversely, the LSB must be the first byte of these registers to be read.

Because these registers share common resources within the I^2C interface, it is important that after writing the LSB of one of these registers, neither of the others is accessed for a period to give the internal registers time to update. After writing to the RTC, subsequent writes to the PIT should be delayed by at least 4ms; writes to *DCOCode* by a period equal to CLK0; and writes to *WakeUpTime* by 31µs.

Crystal Trim Write Protect

As an additional measure to protect the crystal loading capacitance from invalid adjustment, each time the value of the *XtalTrim* register is changed, a '0' must first be written to the XtalTrimWP register on the preceding access.

Note: If the *AppSpecificWP* bit is set to '1', then the *XtalTrim* fuses cannot be written, but unlike other registers the *XtalTrim* register CAN still be written - as detailed above.

Register Name RO = Read Only R/W = Read/Write	Address (hex)	Default (hex)	Data Bit							
			7 (MSB)	6	5	4	3	2	1	0 (LSB)
WakeupTime (R/W)	00	00	*WakeupTime*[31:24]							
	01	00	*WakeupTime*[23:16]							
	02	00	*WakeupTime*[15:8]							
	03	00	*WakeupTime*[7:0]							
PeriodicTimer(RO)	06	00	*PeriodicTimer*[31:24]							
	07	00	*PeriodicTimer* [23:16]							
	08	00	*PeriodicTimer* [15:8]							
	09	00	*PeriodicTimer* [7:0]							
RTC. (R/W)	0B	03	Year (upper BCD digit)				Year (lower BCD digit)			
	0C	01				Month (upper BCD digit)	Month (lower BCD digit)			
	0D	01			Day (upper BCD digit)		Day (lower BCD digit)			
	0E	00			Hour (upper BCD digit)		Hour (lower BDC digit)			
	0F	00		Minutes (upper BCD digit)			Minutes (lower BCD digit)			
	10	00		Seconds (upper BCD digit)			Seconds (lower BDC digit)			
	11	00	Subseconds							
InterruptEnable (R/W)	14	00			SNSE Fault	ADC Done		RTC Alarm	Comparator trigger	PIT expired
InterruptStatus (R/W)	15	00			SNSE Fault	ADC Done		RTC Alarm	Comparator trigger	PIT expired
ADCResult (RO)	16	80	ADC Conversion result							
ForcedDACValue (R/W)	17	64	DAC value forced by software							
ADCConfig (R/W)	18	40	Initiate ADC Conversion	Comparator polarity	Device mode			DAC clock post-scaler		DAC enable
Config (R/W)	19	00		Maintain LDO	Comparator interrupt polarity		Force DCO On	Force internal 32.768 kHz on	Comparator source select	
CLK0Config (R/W)	20	30	CLK0 supply	CLK0 HF/LF	CLK1 = CLK0	CLK0 Enable		CLK0 Post-scaler		
CLK1Config (R/W)	21	00	CLK1 supply	CLK1 HF/LF	Invert CLK1	CLK1 Enable	CLK1 Post-scaler			
FLLConfig (R/W)	22	00	SS Enable	SS Config				Fine Lock	Coarse Lock	Enable FLL
FLLDivideRatio (R/W)	23	0F			*FLLDivideRatio*[13:8]					
	24	41	*FLLDivideRatio*[7:0]							
ResetThreshold (R/W)	30	00		*ResetThreshold*						
ResetDuration (R/W)	31	00				*ResetDuration*				
Status (R/W)	32	28	Xtal osc stable	Comparator o/p	RC osc stable	Auto-ClkDetect mode	RTC Invalid		SNSE activity	FLL Locked
CauseOfReset (R/W)	33	09					VBO	WDT Code violation	WDT expired	PORB
WDTCode (R/W)	34	00	Watchdog refresh code							
WDTConfig (R/W)	35	00						AutoWDT-Suspend	WDT prescaler	
WDTPeriod (R/W)	36	00		Watchdog timeout period						
INTConfig (R/W)	37	00		Edge or Level	I²C ShortCode Enable	Value at INT pin	GPIO polariy	GPIO Direction	Enable INT Toggling	Interrupt or GPIO
MinStartTemp (R/W)	38	7B	Minimum start temperature for fan control mode							
DutyCycleStepSize (R/W)	39	11		PDM or PWM		Duty cycle increment per degree in fan control mode				
ManualPWMDutyCycle (R/W)	3A	00							PWM Duty Cycle[9:8]	
	3B	00	PWM duty cycle[7:0]							
Int32kCoarseTrim (R/W)	40	20			Internal 32.768 kHz oscillator trim – CALIBRATION ONLY					
Int32kFineTrim(R/W)	41	00					Internal 32.768 kHz oscillator fine trim – CALIBRATION ONLY			
XtalTrim (R/W)	42	00				Xtal padding capacitor trim				
BGCode (R/W)	43	00					Bandgap trim – CALIBRATION ONLY			
DCOCode (R/W)	44	00			DCO Bank1 startup code					
	45	00			DCO Bank2 startup code					
	46	00		DCO Bank3 startup code[6:3]				DCO Bank3 startup code[2:0]		
I2CSlaveAddr (R/W)	47	00						I²C Slave address [2:0]		
TempTrim (R/W)	48	00					Temperature Sensor Trim – CALIBRATION ONLY			
WriteProtects (R/W)	49	10				Xtal Trim WP		Cal Fuse WP	App-Specific Fuse WP	Reset-Threshold WP
RTCAlarm/Scratchpad (R/W)	80	00	Year (upper BCD digit)/SP[39:36]				Year (lower BCD digit)/SP[35:32]			
	81	00	SP[31:29]			Month (upper BCD digi)/SP[28]	Month (lower BCD digit)/SP[27:24]			
	82	00	SP[23:22]		Day (upper BCD digit)/SP[21:20]		Day (lower BCD digit)/SP[19:16]			
	83	00	SP[15:14]		Hour (upper BCD digit)/SP[13:12]		Hour (lower BDC digit)/SP[11:8]			
	84	00	SP[7]	Minutes (upper BCD digit)/SP[6:4]			Minutes (lower BCD digit)/SP[3:0]			

Address(hex): 00

Register Name *WakeupTime*			**Description** (RW) 8 Most significant bits of the *WakeupTime* .			**Default Value:** 0000 0000 **Reset Event: P**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit No.	**Description**		**Bit Value**	**Value Description**			
[7:0]	*WakeupTime* Most significant byte of the 4-byte *WakeupTime*		00 (hex)	The Periodic Interval Timer (PIT) generates a periodic interrupt, the interval of which is set by the four *WakeupTime* registers. Period = *WakeupTime*/32768. Setting *WakeupTime* to 0 disables the PIT This register only takes effect once the least significant byte (address 03) has been written. All four bytes should be written, even if some have not changed			

Address(hex): 01

Register Name *WakeupTime*			**Description** (RW) Bits [23:16] of the *WakeupTime*.			**Default Value:** 0000 0000 **Reset Event: P**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit No.	**Description**			**Bit Value**	**Value Description**		
[7:0]	*WakeupTime* Bits [23:16] of the 4-byte *WakeupTime*			00 (hex)	See register 00 description		

Address(hex): 02

Register Name *WakeupTime*			**Description** (RW) Bits [15:8] of the *WakeupTime*.			**Default Value:** 0000 0000 **Reset Event: P**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit No.	**Description**			**Bit Value**	**Value Description**		
[7:0]	*WakeupTime* Bits [15:8] of the 4-byte *WakeupTime*			00 (hex)	See register 00 description		

Address(hex): 03

Register Name *WakeupTime*			**Description**	(RW) Least Significant Byte of *WakeupTime*.		**Default Value:** 0000 0000 **Reset Event: P**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit No.	**Description**		**Bit Value**	**Value Description**			
[7:0]	*WakeupTime* Bits [7:0] of the 4-byte *WakeupTime*		00 (hex)	The least significant byte of *WakeupTime*. Writing to this register loads all four bytes of *WakeupTime* into the PIT after up to two periods of the 32.768 kHz clock, i.e. 61 µs later. It is important that no writes or reads to either *WakeupTime*, *RTC*, *PeriodicTimer* nor *DCOCode* occur during this period. The PeriodicTimer is reset whenever this register is written When reading *WakeupTime*, this must be the first of the four bytes to be read			

Address(hex): 06

Register Name *PeriodicTimer*			**Description**	(RO) Most Significant Byte of *PeriodicTimer*.		**Default Value:** 0000 0000 **Reset Event: P, W, B**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit No.	**Description**		**Bit Value**	**Value Description**			
[7:0]	*PeriodicTimer* Bits [31:23] of the 4 byte *PeriodicTimer*		00 (hex)	The most significant byte of *PeriodicTimer*, which repetitively increments from 0 up to *WakeupTime*, clocked by the 32.768 kHz clock (Xtal if stable, internal 32.768 kHz oscillator otherwise). When reading *PeriodicTimer*, the least significant byte should read first The *PeriodicTimer* is disabled if *WakeupTime* is zero			

Address(hex): 07

Register Name *PeriodicTimer*			**Description**	(RO) Bits [23:16] of *PeriodicTimer*.		**Default Value:** 0000 0000 **Reset Event: P, W, B**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit No.	**Description**			**Bit Value**	**Value Description**		
[7:0]	*PeriodicTimer* Bits [23:16] of the 4 byte *PeriodicTimer*			00 (hex)	See register 06 description		

Address(hex): 08

Register Name *PeriodicTimer*			**Description**	(RO) Bits [15:8] of *PeriodicTimer*.		**Default Value:** 0000 0000 **Reset Event: P, W, B**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit No.	**Description**			**Bit Value**	**Value Description**		
[7:0]	*PeriodicTimer* Bits [15:8] of the 4 byte *PeriodicTimer*			00 (hex)	See register 06 description		

Address(hex): 09

Register Name *PeriodicTimer*			**Description** (RO) Bits [7:0] of *PeriodicTimer*.			**Default Value:** 0000 0000 **Reset Event: P, W, B**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit No.	**Description**			**Bit Value**	**Value Description**		
[7:0]	*PeriodicTimer* Bits [7:0] of the 4 byte *PeriodicTimer*			00 (hex)	See register 06 description		

Address(hex): 0B

Register Name *RTC*			**Description** (R/W) Real Time Clock.			**Default Value:** 0000 0011 **Reset Event: P**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Year (MSD)				*Year (LSD)*			
Bit No.	**Description**		**Bit Value**	**Value Description**			
[7:4]	*Year (MSD)*		00 (hex)	Upper digit of the Binary Coded Decimal (BCD) year count			
[3:0]	*Year (LSD)*		03 (hex)	Lower digit of the BCD year count. Years cycle 00 (BCD) to 99 (BCD) RTC runs continuously after startup, even through brownouts and watchdog resets When writing the RTC, all bytes must be written, and LSB (address 11) must be written last When reading the RTC, the LSB must be read first		

Address(hex): 0C

Register Name *RTC*			**Description** (R/W) Real Time Clock.			**Default Value:** 0000 0001 **Reset Event: P**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
			Month (MSD)	***Month (LSD)***			
Bit No.	**Description**		**Bit Value**	**Value Description**			
[4]	*Month (MSD)*		00 (hex)	Upper digit of the Binary Coded Decimal (BCD)month count			
[3:0]	*Month (LSD)*		03 (hex)	Lower digit of the BCD month count. Month counter cycles from 01 (BCD) to 12 (BCD) See also 0B description			

Register Descriptions *(continued)*

Address(hex): 0D

Register Name *RTC*			**Description** (R/W) Real Time Clock.			**Default Value:** 0000 0001 **Reset Event: P**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		Day (MSD)		***Day (LSD)***			

Bit No.	**Description**	**Bit Value**	**Value Description**
[5:4]	*Day (MSD)*	00 (hex)	Upper digit of the Binary Coded Decimal (BCD) day-of-the-month count
[3:0]	*Day (LSD)*	01 (hex)	Lower digit of the BCD day-of-the-month count. Cycles from 01 (BCD) to 28,29,30 or 31 (BCD) according to the month, and tracks leap years correctly up to 2099 See also 0B description

Address(hex): 0E

Register Name *RTC*			**Description** (R/W) Real Time Clock.			**Default Value:** 0000 0000 **Reset Event: P**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		Hour (MSD)		***Hour (LSD)***			

Bit No.	**Description**	**Bit Value**	**Value Description**
[5:4]	*Hour (MSD)*	00 (hex)	Upper digit of the Binary Coded Decimal hour count
[3:0]	*Hour (LSD)*	00 (hex)	Lower digit of the BCD hour count. Cycles from 00 (BCD) to 23 (BCD) See also 0B description

Address(hex): 0F

Register Name *RTC*			**Description** (R/W) Real Time Clock.			**Default Value:** 0000 0000 **Reset Event: P**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	Minutes (MSD)			***Minutes (LSD)***			

Bit No.	**Description**	**Bit Value**	**Value Description**
[6:4]	*Minute (MSD)*	00 (hex)	Upper digit of the Binary Coded Decimal minute count
[3:0]	*Minute (LSD)*	00 (hex)	Lower digit of the BCD minute count. Cycles from 00 (BCD) to 59 (BCD) See also 0B description

Register Descriptions *(continued)*

Address(hex): 10

Register Name *RTC*			**Description** (R/W) Real Time Clock.			**Default Value:** 0000 0000 **Reset Event: P**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	Seconds (MSD)			***Seconds (LSD)***			

Bit No.	**Description**	**Bit Value**	**Value Description**
[6:4]	*Seconds (MSD)*	00 (hex)	Upper digit of the Binary Coded Decimal seconds count
[3:0]	*Seconds (LSD)*	00 (hex)	Lower digit of the BCD seconds count. Cycles from 00 (BCD) to 59 (BCD) See also 0B description

Address(hex): 11

Register Name *RTC*			**Description** (R/W) Real Time Clock.			**Default Value:** 0000 0000 **Reset Event: P**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
SubSeconds							

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:0]	*SubSeconds*	00 (hex)	Least significant byte of the RTC, incrementing at 256 Hz from 00 to FF. Note that this is the only RTC byte which is NOT BCD coded Writing to this register loads all six bytes of *RTC* into the counter after up to two periods of the 256 Hz clock, i.e. 7.8 ms later. It is important that no writes or reads to either *WakeupTime*, *RTC*, *PeriodicTimer* nor *DCOCode* occur during this period When reading the *RTC*, this must be the first byte read

Address(hex): 14

Register Name *InterruptEnable*			**Description** (R/W) Selects which interrupt sources generate interrupts			**Default Value:** 0000 0000 **Reset Event: P, W, B**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		SNSE Fault	*ADC Done*		*RTC Alarm*	*Comparator trigger*	*PIT expired*

Bit No.	**Description**	**Bit Value**	**Value Description**
[5]	*SNSE Fault interrupt enable*	0 1	SNSE fault interrupts disabled SNSE fault interrupts enabled If the *DeviceMode* fuse (address 18, bits [5:3]) are set for fan control mode, this bit is automatically set on startup, but it may be overridden
[4]	*ADC conversion complete indicator interrupt enable*	0 1	ADC complete interrupts disabled ADC complete interrupts enabled
[2]	*RTC alarm interrupt enable*	0 1	RTC alarm interrupt disabled RTC alarm interrupt enabled
[1]	*Comparator trigger interrupt enable*	0 1	Comparator interrupt disabled Comparator interrupt enabled
[0]	*PIT interrupt enable*	0 1	PIT interrupt disabled PIT interrupt enabled

Address(hex): 15

Register Name *InterruptStatus*			**Description**	(R/W) Indicates status of all interrupt sources, and may be used to selectively clear any number of these.		**Default Value:** 0000 0000 **Reset Event: P, W**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		SNSE Fault	*ADC Done*		*RTC Alarm*	*Comparator trigger*	*PIT expired*

Bit No.	**Description**	**Bit Value**	**Value Description**
[5]	*SNSE Fault interrupt*	0 1	No SNSE faults detected In fan control mode, AND the fan is currently active, i.e. the PWM duty cycle is non-zero, this indicates that no SNSE pulse were detected within the last 32768 CLK1 cycles (1 second if CLK1 is set for 32.768 kHz), irrespective of whether CLK1 output is enabled or not In other device modes, this indicates that no activity has been detected on the general-purpose comparator for the last 32768 CLK1 cycles, irrespective whether CLK1 is enabled Write '1' to this bit to clear the *SNSE Fault interrupt*
[4]	*ADC conversion complete indicator interrupt*	0 1	ADC conversion is not complete ADC conversion is complete, and the result may be read in the *ADCResult* register Write '1' to this bit to clear the *ADCDone* interrupt
[2]	*RTC alarm interrupt*	0 1	RTC alarm has not triggered RTC alarm has triggered Write '1' to this bit to clear the *RTC alarm interrupt*
[1]	*Comparator trigger interrupt*	0 1	Comparator interrupt has not triggered If the *CompIntPolarity* bit in the *Config* register is set, then this indicates that the comparator source has risen above the DAC level. If the *CompIntPolarity* bit is clear, then this indicates that the comparator source has fallen below the DAC level Write '1' to this bit to clear the *RTC alarm interrupt*
[0]	*PIT interrupt*	0 1	PIT has not expired PIT has expired Write '1' to this bit to clear the *RTC alarm interrupt*

Address(hex): 16

Register Name *ADCResult*			**Description**	(R) ADC Conversion Result		**Default Value:** 1000 0000 **Reset Event: P, W**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
ADC Conversion Result							

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:0]	*ADC Result*	00 (hex)	Result of 8-bit successive approximation analog to digital conversion

Register Descriptions *(continued)*

Address(hex): 17

Register Name *ForcedDACValue*			**Description** (R/W) Overrides the current DAC setting			**Default Value:** 0000 1011 **Reset Event: P, W**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Forced DAC value							

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:0]	*Forced DAC value* *THIS REGISTER IS FUSE INITIALIZED*	00	This value overrides the existing DAC setting, which may have been initialized by fuse, or as a result of an ADC conversion The fuses can be blown to initialize the DAC to any of the following voltages: 660 mV 690 mV 730 mV 760 mV 800 mV 830 mV 860 mV 890 mV 930 mV 970 mV 1000 mV 1040 mV 1140 mV 1240 mV 1380 mV 1550 mV

Address(hex): 18

Register Name *ADCConfig*			**Description**	(R/W) Configures ADC, DAC and comparator configuration, as well as setting the overall device mode		**Default Value:** 0000 0100 **Reset Event: P, W**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Initiate ADC Conversion	***Comparator polarity***	***Device mode***			***DAC Clock post-scaler***		***DAC Enable***

Bit No.	**Description**	**Bit Value**	**Value Description**
[7]	*Initiate ADC Conversion*	1	Setting this bit initiates an ADC conversion The conversion is completed within 1500 cycles of the internal DAC clock, the rate of which is determined by the *DACClkPostScaler* in this register, and the rate of the HFDCO. ADC conversion completion is signaled by the *ADCDone* flag in the *InterruptStatus* register
[6]	*Comparator Polarity*	0 1	General-purpose comparator output is used directly General-purpose comparator output is inverted
[5:3]	*DeviceMode* *THIS REGISTER IS FUSE INITIALIZED*	000 001 011 100 101	Normal mode – PWM pin can be controlled by setting the *PWMDutyCycle* Switched boost regulator mode – PWM pin controls an external inductor/capacitor network Switched buck regulator mode LDO Mode – PWM pin is driven by internal LDO Fan control mode – PWM pin is controlled as described in the PWM section **Note that this register may not be changed if the *App-specificFuseWP* bit in the *WriteProtects* register is set**
[2:1]	*DACClkPostScaler*	00 01 10 11	*DACClk* is 32.768 kHz (ADC Conversion in 45 ms) *DACClk* is HFDCO/8 (ADC Conversion in 11264 cycles of HFDCO period) *DACClk* is HFDCO/16 (ADC Conversion in 22528 cycles of HFDCO period) *DACClk* is HFDCO/32 (ADC conversion in 45056 cycles of HFDCO period)
[0]	*DAC Enable*	0 1	General-purpose DAC & comparator are powered down General-purpose DAC & comparator are enabled

Address(hex): 19

Register Name	*Config*		**Description**	(R/W) Various general configuration bits		**Default Value:** 0000 0000 **Reset Event: P, W, B**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	Maintain LDO	***Comparator interrupt polarity***		***Force DCO On***	***ForceInt32kHzOscOn***	***Comparator Source Select***	

Bit No.	**Description**	**Bit Value**	**Value Description**
[6]	*Maintain LDO*	0 1	LDO regulates to DAC voltage x 3 when enabled When running in LDO mode (*DeviceMode* bits in the *ADCConfig* register set to 100), this maintains the LDO input voltage **for a short period,** thereby freeing up the DAC and comparator for an ADC conversion. The LDO voltage droops the longer that this bit is set
[5]	*Comparator Interrupt Polarity*	0 1	The general-purpose comparator interrupt is activated when the comparator source is lower than the DAC voltage The general-purpose comparator interrupt is activated when the selected comparator source is higher than the DAC voltage
[3]	*ForceDCOOn*	0 1	High frequency DCO is controlled by the clock generation mechanisms HFDCO is forced on, irrespective of clock generator state. This can be used to enable the FLL coarse locking to occur while CLKO has 32.768 kHz, and thereby protects the microcontroller from undesirable frequency excursions
[2]	*ForceInt32kOn*	0 1	The internal 32.768 kHz oscillator is disabled if and when the external crystal oscillator becomes stable The internal 32.768 kHz oscillator is forced on, and the external crystal oscillator ignored
[1:0]	*ComparatorSourceSelect* *THIS REGISTER IS FUSE INITIALIZED*	00 01 10 11	Comparator input is connected to VDD/3 Comparator input is connected to VBAK/3 Comparator input is connected to the internal temperature sensor Comparator input is connected to the SNSE pin **Note that this register may not be changed if the *App-specificFuseWP* bit in the *WriteProtects* register is set**

Address(hex): 20

Register Name *ClkOConfig*			**Description** (R/W) Sets up CLK0			**Default Value:** 0011 0000 **Reset Event: P, W** (bit 7) **Reset Event: P, W, B** (bits 6:0)	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CLK0Supply	***CLK0 HF/LF***	***CLK1=CLK0***	***CLK0Enable***		***CLK0 post-scaler***		

Bit No.	**Description**	**Bit Value**	**Value Description**
[7]	*CLK0 supply*	0 1	CLK0 pad is supplied by VDD. When VDD drops below VBO, CLK0 ceases CLK0 pad is supplied by VBAK
[6]	*CLK0 HF/LF*	0 1	CLK0 is derived from the post-scaled HFDCO CLK0 is set to 32.768 kHz
[5]	*CLK1 = CLK0*	0 1	CLK1 is treated completely independently from CLK0. Phase relationship can not be guaranteed CLK1 is set to run at the same frequency as CLK0, with or without inversion. CLK1 and CLK0 transition together, and operate as in-phase or complementary clock outputs
[4]	*CLK0Enable*	0 1	If any interrupt is enabled in the *InterruptEnable* register, then setting CLK0 to 0 disables CLK0. The clock resumes whenever any enabled interrupt activates CLK0 is enabled unless in *AutoClkDetect* mode and CLKIN has stopped
[2:0]	*CLK0 PostScaler* *THIS REGISTER IS FUSE INITIALIZED*	000 001 010 011 100 101 110 111	CLK0 frequency = HFDCO frequency CLK0 frequency = HFDCO/2 CLK0 frequency = HFDCO/4 CLK0 frequency = HFDCO/8 CLK0 frequency = HFDCO/16 CLK0 frequency = HFDCO/32 CLK0 frequency = HFDCO/64 CLK0 frequency = HFDCO/128 This register is ignored if the CLK0 HF/LF bit is set **Note that this register may not be changed if the *App-specificFuseWP* bit in the *WriteProtects* register is set**

Address(hex): 21

Register Name *Clk1Config*			**Description** (R/W) Sets up CLK1			**Default Value:** 0000 0000 **Reset Event: P, W**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CLK1Supply	***CLK1 HF/LF***	***Invert CLK1***	***CLK1Enable***	***CLK1 post-scaler***			

Bit No.	**Description**	**Bit Value**	**Value Description**
[7]	*CLK1 supply* *THIS REGISTER IS FUSE INITIALIZED*	0 1	CLK1 pad is supplied by VDD, but automatically switches over to VBAK during VBO CLK1 pad is supplied only by VBAK
[6]	*CLK1 HF/LF* *THIS REGISTER IS FUSE INITIALIZED*	0 1	CLK0 is set to 32.768 kHz CLK0 is derived from the Post-scaled HFDCO
[5]	*InvertCLK1* *THIS REGISTER IS FUSE INITIALIZED*	0 1	CLK1 is in-phase with CLK0 if CLK1=CLK0 bit in the CLK0Config register is set CLK1 is in direct antiphase with CLK0 if CLK1=CLK0 bit is set If the CLK1=CLK0 bit is not set, then this bit has little relevance
[4]	*CLK1Enable* *THIS REGISTER IS FUSE INITIALIZED*	0 1	CLK1 output is disabled CLK1 output is enabled
[3:0]	*CLK1 PostScaler* *THIS REGISTER IS FUSE INITIALIZED*	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	CLK1 frequency = HFDCO frequency CLK1 frequency = HFDCO/2 CLK1 frequency = HFDCO/4 CLK1 frequency = HFDCO/8 CLK1 frequency = HFDCO/16 CLK1 frequency = HFDCO/32 CLK1 frequency = HFDCO/64 CLK1 frequency = HFDCO/128 CLK1 frequency = HFDCO/256 CLK1 frequency = HFDCO/512 CLK1 frequency = HFDCO/1024 CLK1 frequency = HFDCO/2048 CLK1 frequency = HFDCO/4096 CLK1 frequency = HFDCO/8192 CLK1 frequency = HFDCO/16384 CLK1 frequency = HFDCO/32768 This register is ignored if the CLK1 HF/LF bit is clear. This register is fuse-initialized **Note that this register may not be changed if the *App-specificFuseWP* bit in the *WriteProtects* register is set**

Address(hex): 22

Register Name *FLLConfig*			**Description**	(R/W) Sets up the Frequency Locked Loop (FLL)		**Default Value:** 0000 0000 **Reset Event: P, W, B**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
SS Enable	***SS Config***			***Fine Lock***		***Coarse Lock***	***Enable FLL***
Bit No.	**Description**		**Bit Value**	**Value Description**			
[7]	*Spread Spectrum Enable* *THIS REGISTER IS FUSE INITIALIZED*		0 1	Spectrum Spreading is disabled Spectrum Spreading is enabled **Note that this register may not be changed if the *App-specificFuseWP* bit in the *WriteProtects* register is set**			
[6:5]	*Spread Spectrum Configuration*		00 01 10 11	Spreading bandwidth = 16 kHz Spreading bandwidth = 32 kHz Spreading bandwidth = 64 kHz Spreading bandwidth = 128 kHz **Note that this register may not be changed if the *App-specificFuseWP* bit in the *WriteProtects* register is set**			
[2]	*FineLock*		0 1	If the FLL is enabled locked, then it remains locked and tracks the 32.768 kHz clock Least significant bank of the HFDCO is adjusted with a successive approximation algorithm to achieve a fast (4ms) lock with only minor frequency excursions. This is mainly used to return CLK0/1 to optimum accuracy following a long sleep (HFDCO off) during which the temperature may have changed substantially, which would lead to a slight error on the initial startup frequency before the FLL drifted back to lock			
[1]	*CoarseLock*		0 1	If the FLL is enabled locked, then it remains locked and tracks the 32.768 kHz clock The FLL uses a successive approximation algorithm to rapidly (30 ms) adjust the FLL to a new setting in the *FLLDivideRatio* register. There may be substantial frequency excursions on CLK0/CLK1 (if enabled for HF) while locking is taking place. Once locked, the FLL continues to track the 32.768 kHz source			
[0]	*FLLEnable*		0 1	FLL is disabled. HFDCO free-runs with an accuracy of ± 0.5% FLL is enabled – the HFDCO tracks the 32.768 kHz source based on the *FLLDivideRatio* register. *FLLEnable* is by default 0 until the crystal oscillator is stable, and then it is automatically set. If no crystal is connected, the FLL remains disabled. In either case, the *FLLEnable* bit can be overridden by software			

Address(hex): 23

Register Name *FLLDivideRatio*			**Description**	(R/W) Defines the ratio between the HFDCO and 32.768 kHz source when FLL is enabled		**Default Value:** 0000 0000 **Reset Event: P, W, B**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		FLLDivideRatio[13:8]					

Bit No.	**Description**	**Bit Value**	**Value Description**
[5:0]	*FLLDivideRatio[13:8]* *THIS REGISTER IS FUSE INITIALIZED*		The upper 6 bits of the *FLLDivideRatio*. When the FLL is enabled and locked, the HFDCO frequency is 2048*(*FLLDivideRatio*+1) **Note that this register may not be changed if the *App-specificFuseWP* bit in the *WriteProtects* register is set**

Address(hex): 24

Register Name *FLLDivideRatio*			**Description**	(R/W) Defines the ratio between the HFDCO and 32.768 kHz source when FLL is enabled		**Default Value:** 0000 0000 **Reset Event: P, W, B**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
FLLDivideRatio[7:0]							

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:0]	*FLLDivideRatio[7:0]* *THIS REGISTER IS FUSE INITIALIZED*		The least significant byte of the *FLLDivideRatio*. When the FLL is enabled and locked, the HFDCO frequency is 2048*(*FLLDivideRatio*+1) **Note that this register may not be changed if the *App-specificFuseWP* bit in the *WriteProtects* register is set**

Address(hex): 30

Register Name *ResetThreshold*			**Description**	(R/W) Sets the brownout (VBO) level		**Default Value:** 0000 0000 **Reset Event: P, W**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	ResetThreshold						

Bit No.	**Description**	**Bit Value**	**Value Description**
[6:0]	*ResetThreshold* *THIS REGISTER IS FUSE INITIALIZED*		This 7-bit register sets the minimum voltage level (VBO) which would cause a brownout reset and subsequent assertion of the NRST pin. VBO = 1.7 V to 4 V with 24 mV resolution **Note that this register may not be changed if the *ResetThresholdWP* bit in the *WriteProtects* register is set**

Register Descriptions *(continued)*

Address(hex): 31

Register Name *ResetDuration*			**Description** (R/W) Determines the reset duration			**Default Value:** 0000 0000 **Reset Event: P, W**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
			ResetDuration				

Bit No.	**Description**	**Bit Value**	**Value Description**
[4:0]	*ResetDuration* *THIS REGISTER IS FUSE INITIALIZED*		Determines the duration between the deactivation of a reset event (eg. VDD rises above the VBO level, or watchdog expires) and the NRST pin becoming deactivated This register determines the reset duration under the following conditions: If the *DeviceMode* register in *ADCConfig* register is set to 000, i.e. 'Normal' mode, and the SNSE pin is 1 during startup, then this register determines the reset duration. (if SNSE=0 on startup, then reset duration is 6 ms, if SNSE is unconnected, then reset duration is 270 ms) If the *DeviceMode* register is set to any other mode, then this register determines the reset duration irrespective of the SNSE pin. Please note that increasing the value of this register in any mode except normal (*DeviceMode*=000) causes a reset. **Note that this register may not be changed if the *App-specificFuseWP* bit in the *WriteProtects* register is set**

Address(hex): 32

Register Name *Status*		**Description** (R/W) Various device status flags				**Default Value:** 0010 1000 **Reset Event: P, W, B**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Xtal Osc Stable	***Comparator output***	***Internal 32kHz osc stable***	***AutoClkDetect mode***	***RTC invalid***		***SNSE activity***	***FLL locked***
Bit No.	**Description**	**Bit Value**	**Value Description**				
[7]	*Xtal Oscillator Stable*	0 1	Either the crystal oscillator has not yet stabilized or the *ForceInternal32kHzOn* bit in the *Config* register has been set 1024 cycles of the crystal oscillator have been counted, and the crystal is therefore considered stable				
[6]	*Comparator Output*	0 1	The comparator reference input is lower than the DAC voltage The comparator reference input is higher than the DAC voltage This bit can be polled to determine whether SNSE, VBAK, VDD or temperature are above or below a preset threshold, or it can be used with the *ForceDACValue* register to implement alternative ADC algorithms				
[5]	*Internal 32kHz oscillator stable*	0 1	The internal 32.768 kHz oscillator has been stable and accurate since the last write to this bit The supply voltage to the internal 32.768 kHz oscillator has at some point dropped below 1.65 V, resulting in some loss of frequency accuracy. Once the crystal has stabilized, this oscillator is redundant; this oscillator is turned off, and this flag is then set Writing 1 to this bit clears it				
[4]	*AutoClkDetect mode*	0 1	No edges have been observed on the CLKIN pin. CLK0 continues to run until software clears the *CLK0Enable* flag in the *CLK0Config* register Activity has been observed on CLKIN, which is assumed to be connected to the XOUT of the µC. CLK0 stops in the same state as CLKIN, 4 cycles after CLKIN stops, and resumes as soon as CLKIN toggles *AutoClkDetect* mode is one of the prime features of µBuddy, enabling very fast clock startup and shutdown by detecting the microcontroller's own sleep mode				
[3]	*RTCInvalid*	0 1	The RTC clock has been accurate since this flag was last cleared, and the RTC accuracy is therefore assured At some time since this bit was last cleared by software, both VDD and VBAK have been insufficient to sustain an accurate clock to the RTC, and the RTC value therefore can not be trusted Writing 1 to this bit clears it				
[1]	*SNSE activity*	0 1	No activity has been observed on the SNSE pin during the last 32768 periods of CLK1, whether or not CLK1 is enabled Activity has been observed on SNSE during the past 32768 periods of CLK1				
[0]	*FLL Locked*	0 1	The FLL has not stabilized at the desired frequency, and may still be hunting The FLL has locked to frequency and is stable **Note that this bit is invalid once spectrum spreading is enabled**				

Address(hex): 33

Register Name *CauseOfReset*			**Description** (R/W) Shows what caused the last reset			**Default Value:** 0000 1001 **Reset Event:** (see description)	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
				VBO	***WDTCode Violation***	***WDT expired***	***PORB***

Bit No.	**Description**	**Bit Value**	**Value Description**
[3]	*VBO*	0 1	VDD has not dropped below the programmed VBO level since this bit was last cleared VDD dropped below the VBO level at some point since this bit was last cleared. Writing 1 to this bit clears it
[2]	*WDTCode Violation*	0 1	Either the watchdog is disabled, or else only the correct code sequence has been written in good time, to the *WDTCode* register The watchdog was enabled, and an incorrect code was written to the *WDTCode* register Writing 1 to this bit clears it
[1]	*WDTExpired*	0 1	Either the watchdog is disabled, or else *WDTCode* register has been refreshed in a timely fashion The watchdog is enabled, but the *WDTCode* register has not been refreshed in time to prevent the watchdog expiring Writing 1 to this bit clears it
[0]	*PORB*	0 1	VDD has not dropped below 1 V since this bit was last cleared VDD dropped below 1 V at some time since this bit was last cleared Writing 1 to this bit clears it

Address(hex): 34

Register Name *WDTCode*			**Description** (R/W) Watchdog refresh code			**Default Value:** 0000 0000 **Reset Event: P, W, B**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
WDTCode							

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:0]	*WDT refresh code*		Once the watchdog is enabled by writing to the *WDTPeriod* register, alternate writes of 5A and C3 are expected within the time set by *WDTPeriod* and *WDTPrescaler* registers to prevent NRESET activation. Once enabled, the watchdog can not be disabled by software

Address(hex): 35

Register Name *WDTConfig*			**Description** (R/W) Sets up the watchdog			**Default Value:** 0000 0000 **Reset Event: P, W, B**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
					AutoWDT Suspend	***WDTPrescaler***	

Bit No.	**Description**	**Bit Value**	**Value Description**
[2]	*AutoWDTSupend*	0	The watchdog counter, once enabled, is derived from the active 32.768 kHz source (crystal or internal), irrespective of CLK0, and the watchdog period is always consistent and independent of CLK0. The watchdog continues to run even when CLK0 has been disabled
		1	The watchdog counter, once enabled, is derived from CLK0, and therefore suspends counting when CLK0 is disabled. This effectively counts microprocessor cycles (and hence instructions), and is useful to avoid the necessity for very long watchdog periods simply to prevent watchdog activation during long sleeps **Note that once the watchdog period has been written, thereby activating the watchdog timer, this register can no longer be changed**
[1:0]	*WDTPrescaler*	00	If *AutoWDTSuspend* = 0, then Watchdog timeout period = (*WDTPeriod*+1)/128 seconds If *AutoWDTSuspend* = 1, then Watchdog timeout period = *(WDTPeriod+1)**CLK0 period*256
		01	If *AutoWDTSuspend* = 0, then Watchdog timeout period = (*WDTPeriod*+1)/64 seconds If *AutoWDTSuspend* = 1, then Watchdog timeout period = *(WDTPeriod+1)**CLK0 period*512
		10	If *AutoWDTSuspend* = 0, then Watchdog timeout period = (*WDTPeriod*+1)/32 seconds If *AutoWDTSuspend* = 1, then Watchdog timeout period = *(WDTPeriod+1)**CLK0 period*1024
		11	If *AutoWDTSuspend* = 0, then Watchdog timeout period = (*WDTPeriod*+1)/16 seconds If *AutoWDTSuspend* = 1, then Watchdog timeout period = *(WDTPeriod+1)**CLK0 period*2048 **Note that once the watchdog period has been written, thereby activating the watchdog timer, this register can no longer be changed**

Address(hex): 36

Register Name *WDTPeriod*			**Description**	(R/W) Sets up the watchdog period		**Default Value:** 0000 0000 **Reset Event: P, W, B**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	WDTPeriod						
Bit No.	**Description**		**Bit Value**	**Value Description**			
[6:0]	*WDTPeriod*		000000 all others	Watchdog is disabled Watchdog is enabled, and can not be disabled by software. Watchdog timeout period is as defined in register 35, *WDTConfig* Once the watchdog has been activated by writing a non-zero value to this register, then further writes to *WDTPrescaler*, *AutoWDTSuspend* and *WDTPeriod* are disabled			

Address(hex): 37

Register Name *INTConfig*			**Description**	(R/W) Configures the operation of the INT pin		**Default Value:** 0000 0000 **Reset Event: P, W, B**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	Edge or Level	***I²C ShortCode Enable***	***Value at INT pin***	***GPIO polarity***	***GPIO Direction***	***Enable INT Toggling***	***Interrupt or GPIO***
Bit No.	**Description**		**Bit Value**	**Value Description**			
[6]	*Edge or Level*		0 1	When the INT pin is programmed as an interrupt by setting *InterruptOrGPIO* to 1, the INT pin signals each interrupt as a pulse with a duration of 4 CLK0 cycles The INT pin drives to its active level (set by *GPIOPolarity* bit), and remains until the interrupt is cleared by writing the relevant bit in the *InterruptStatus* register. If toggling interrupts are required, then this bit must be set to 1			
[5]	*I2CShortCodeEnable*		0 1	Interrupts can only be cleared with a full-length I²C access. All active interrupts are simultaneously cleared when a short-form version of the I²C access is sent by the microcontroller. This allows for substantially faster interrupt clearing			
[4]	*ValueAtINTPin*		0 1	The INT pin is being driven externally or internally to 0 The INT pin is being driven externally or internally to 1			
[3]	*GPIOPolarity*		0 1	If InterruptOrGPIO = 0 (GPIO), then INT pin is driven to 0. If InterruptOrGPIO = 1 (Interrupt), then INT is hard-driven to 0 when the interrupt is active, but weak-pulled to 1 when inactive If InterruptOrGPIO = 0 (GPIO), then INT pin is driven to 1. If InterruptOrGPIO = 1 (Interrupt), then INT is hard-driven to 1 when the interrupt is active, but weak-pulled to 0 when inactive			
[2]	*GPIODirection*		0 1	When InterruptOrGPIO = 0 (GPIO mode), INT pin is programmed as a general-purpose input port When InterruptOrGPIO = 0 (GPIO mode), INT pin is programmed as a general-purpose output port			
[1]	*EnableINTToggling*		0 1	All Active interrupts are signaled either by a 4 cycle pulse, or by a fixed level, as determined by the *EdgeOrLevel* bit in this register The PIT toggles the INT pin at every activation. This can be used to generate a very slow clock independent of CLK0 and CLK1, with a period between 61 µs and 72 hours In this mode all other interrupts operate normally, but may be masked if the INT pin has been driven to the active state by a PIT timeout			
[0]	*InterruptOrGPIO*		0 1	INT pin is used as GPIO, with direction defined by *GPIODirection* bit, and polarity set by *GPIOPolarity* bit. INT pin is used to signal interrupts, and hard-drives to the active level, weak-pull to the inactive level.			

Register Descriptions *(continued)*

Address(hex): 38

Register Name *MinStartTemp*			**Description**	(R/W) Defines the temperature at which auto-fan mode starts to drive the fan		**Default Value:** 0111 1011 **Reset Event: P, W**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
MinStartTemp							

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:0]	*MinStartTemp*		This is the *ADCCode* corresponding to the lowest temperature at which the automatic fan control mode activates the PWM pin, and switches on the fan Code = 163 minus temperature (°C). In other modes (*DeviceCode* in the *ADCConfig* register not equal to 111), this register has no effect Default start temperature is 40°C, and the default minimum duty cycle is 25%

Address(hex): 39

Register Name *DutyCycleStepSize*			**Description**	(R/W) The PWM duty cycle increment for every degree of rise in the temperature when in auto-fan-control mode		**Default Value:** 0001 0001 **Reset Event: P, W**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DutyCycleStepSize							

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:0]	DutyCycleStepSize		In Auto-fan-control mode (*DeviceMode* bits in the *ADCConfig* register = 111), this is how much the PWM duty cycle increments for every degree of temperature rise. This effectively defines the temperature at which the PWM duty cycle would be 100%, i.e., The fan is on at full speed *DutyCycleStepSize* = 768/(MaxTemp – MinTemp) Default value of 17 gives a maximum temperature of 85°C

Address(hex): 3A

Register Name *ManualPWMDutyCycle*			**Description**	(R/W) Sets the PWM duty cycle when in 'normal' mode.		**Default Value:** 0000 0000 **Reset Event: P, W**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
						PWMDutyCycle[9:8]	

Bit No.	**Description**	**Bit Value**	**Value Description**
[1:0]	*ManualPWMDutyCycle[9:8]*		The most significant 2 bits of the *ManualPWMDutyCycle*. When in normal mode, i.e. *DeviceMode* bits in the *ADCConfig* register set to 000, this defines the duty cycle on the PWM pin. Duty cycle = *ManualPWMDutyCycle*/1024

Address(hex): 3B

Register Name *ManualPWMDutyCycle*			**Description**	(R/W) Sets the PWM duty cycle when in 'normal' mode.		**Default Value:** 0000 0000 **Reset Event: P, W**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
PWMDutyCycle[7:0]							

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:0]	*ManualPWMDutyCycle[7:0]*		The least significant byte of the *ManualPWMDutyCycle*. When in normal mode, i.e. *DeviceMode* bits in the *ADCConfig* register set to 000, this defines the duty cycle on the PWM pin. Duty cycle = *ManualPWMDutyCycle/1024*

Address(hex): 40

Register Name *Int32kCoarseTrim*	**Description**	(R/W) Calibration register.	**Default Value:** 0000 0000 **Reset Event: P, W**
This register is for device calibration only.			

Address(hex): 41

Register Name *Int32kFineTrim*	**Description**	(R/W) Calibration register.	**Default Value:** 0000 0000 **Reset Event: P, W**
This register is for device calibration only.			

Address(hex): 42

Register Name *XtalTrim*			**Description**	(R/W) Sets the padding capacitance on XIN and XOUT		**Default Value:** 0000 0000 **Reset Event: P**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
			XtalTrim				

Bit No.	**Description**	**Bit Value**	**Value Description**
[4:0]	*XtalTrim* *THIS REGISTER IS FUSE INITIALIZED*		Sets the padding capacitance on the XIN/XOUT pins, and can be used to trim the crystal frequency either during system test, or dynamically, based on temperature to greatly improve the intrinsic crystal accuracy in operation. This register is protected against spurious writes by the *XtalTrimWP* bit in the *WriteProtects* register. This flag must be cleared immediately prior to setting this register

Address(hex): 43

Register Name *BGCode*	**Description**	(R/W) Calibration register.	**Default Value:** 0000 0000 **Reset Event: P, W**
This register is for device calibration only.			

Address(hex): 44

Register Name *DCOCode*			**Description**	(R/W) Sets the default HFDCO code for a free-running (non FLL Locked) HFDCO.		**Default Value:** 0000 0000 **Reset Event: P, W, B**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		DCOCode[18:13]					

Bit No.	**Description**	**Bit Value**	**Value Description**
[5:0]	*DCOCode[18:13]* *THIS REGISTER IS FUSE INITIALIZED*		The 19-bit *DCOCode* defines the code and hence frequency at which the High Frequency Digitally Controlled Oscillator (HFDCO) starts, thereby determining its initial frequency prior to the FLL locking it to the 32.768 kHz source. Due to the nature of the HFDCO, the exact frequency for any one device can not be deducted from the *DCOCode*, but can be read back after FLL locking with the *CoarseLock* feature in the *FLLConfig* register, and thereafter programmed into the fuses to ensure that the starting frequency is very close to the target frequency This register is set up so that CLK0 is as close as possible to the target frequency before FLL locking Most customers need not access this register, but it can be used in cases where the standard SH3100 frequency (TBD) is not suitable for the system **Note that this register may not be changed if the *App-specificFuseWP* bit in the *WriteProtects* register is set**

Address(hex): 45

Register Name *DCOCode*			**Description**	(R/W) Sets the default HFDCO code for a free-running (non FLL Locked) HFDCO.		**Default Value:** 0000 0000 **Reset Event: P, W, B**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		DCOCode[12:7]					

Bit No.	**Description**	**Bit Value**	**Value Description**
[5:0]	*DCOCode[12:7]* *THIS REGISTER IS FUSE INITIALIZED*		See description for register 44 **Note that this register may not be changed if the *App-specificFuseWP* bit in the *WriteProtects* register is set**

Address(hex): 46

Register Name *DCOCode*			**Description**	(R/W) Sets the default HFDCO code for a free-running (non-FLL Locked) HFDCO		**Default Value:** 0000 0000 **Reset Event: P, W, B**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	DCOCode[6:0]						

Bit No.	**Description**	**Bit Value**	**Value Description**
[6:0]	*DCOCode[6:0]* *THIS REGISTER IS FUSE INITIALIZED*		See description for register 44 **Note that this register may not be changed if the *App-specificFuseWP* bit in the *WriteProtects* register is set**

Address(hex): 47

Register Name *I2CSlaveAddr*			**Description**	(R/W) Least significant 3 bits of the I²C slave address.		**Default Value:** 0000 0000 **Reset Event: P, W, B**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
					I2CSlaveAddr[2:0]		

Bit No.	**Description**	**Bit Value**	**Value Description**
[2:0]	*I2CSlaveAddr[2:0]* *THIS REGISTER IS FUSE INITIALIZED*		The least significant 3 bits of the I²C slave address. The I²C slave address in its entirety is 0100XYZ where XYZ = *I2CSlaveAddr* Careful selection of these bits allows the SH3100 to share an I²C bus with a number of other devices, including other SH3100s **Note that this register may not be changed if the *App-specificFuseWP* bit in the *WriteProtects* register is set**

Address(hex): 48

Register Name *TempTrim*	**Description**	(R/W) Calibration register.	**Default Value:** 0000 0000 **Reset Event: P, W, B**
This register is for device calibration only.			

Register Descriptions *(continued)*

Address(hex): 49

Register Name *WriteProtects*			**Description** (R/W) Write-protects.			**Default Value:** 0001 0000 **Reset Event: P** (bit 4) **Reset Event: P, W** (bits 2:0)	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
			Xtal Trim WP		***Cal Fuse WP***	***App-specific Fuse WP***	***ResetThresh WP***

Bit No.	**Description**	**Bit Value**	**Value Description**
[4]	*XtalTrimWP*	0 1	The *XtalTrim* register can be written immediately after clearing this bit, whereafter this flag reverts to 1 The *XtalTrim* register can not be written
[2]	*Calibration fuse WP* *THIS REGISTER IS FUSE INITIALIZED*	0 1	The calibration fuses and registers can be changed The calibration fuses and registers can not be changed Calibration registers include: *Int32kCoarseTrim* *Int32kFineTrim* *BGCode* *TempTrim*
[1]	*App-specific fuse WP* *THIS REGISTER IS FUSE INITIALIZED*	0 1	The application-specific fuses and registers can be changed The application-specific fuses and registers can not be changed Application-specific registers include: *CLK0PostScaler* *CLK1PostScaler* *SSEnable* *SSConfig* *FLLDivideRatio* *XtalTrim* *I2CSlaveAddr* *DeviceMode* *ResetDuration* *DACLevel* *DCOCode* *CLK1En* *CLK1Supply* *InvertCLK1* *CLK1 HF/LF*
[0]	*ResetThresholdWP*	0 1	The *ResetThreshold* fuses and register can be changed The *ResetThreshold* fuses and register can not be changed

Address(hex): 80

Register Name *RTCAlarm/Scratchpad*			**Description** (R/W) RTC alarm or scratchpad			**Default Value:** 0000 0000 **Reset Event: P**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Year (MSD)/SP[39:36]				***Year (LSD)/SP[35:32]***			

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:4]	*Year(MSD)/SP[39:36]*		When the RTC alarm interrupt enable is active, this is the upper BCD digit of the year at which the interrupt should be activated. When not used as an RTC alarm, these bits can be used as scratchpad, and remain throughout a brownout condition.
[3:0]	*Year(LSD)/SP[35:32]*		When the RTC alarm interrupt enable is active, this is the lower BCD digit of the year at which the interrupt should be activated. When not used as an RTC alarm, these bits can be used as scratchpad, and remain throughout a brownout condition

Address(hex): 81

Register Name *RTCAlarm/Scratchpad*			**Description** (R/W) RTC alarm or scratchpad			**Default Value:** 0000 0000 **Reset Event: P**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
SP[31:29]			***Month (MSD)/SP[28]***	***Month(LSD)/SP[27:24]***			

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:5]	*SP[31:29]*		Bits [31:29] of the scratchpad memory, irrespective of whether the RTC alarm interrupt is active These bits remain throughout brownout
[4]	*Month(MSD)/SP[28]*		When the RTC alarm interrupt enable is active, this is the upper BCD digit of the calendar month at which the interrupt should be activated When not used as an RTC alarm, these bits can be used as scratchpad, and remain throughout a brownout condition
[3:0]	*Month(LSD)/SP[27:24]*		When the RTC alarm interrupt enable is active, this is the lower BCD digit of the month at which the interrupt should be activated When not used as an RTC alarm, these bits can be used as scratchpad, and remain throughout a brownout condition

Register Descriptions *(continued)*

Address(hex): 82

Register Name *RTCAlarm/Scratchpad*			**Description** (R/W) RTC alarm or scratchpad			**Default Value:** 0000 0000 **Reset Event: P**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
SP[23:22]		***Day (MSD)/SP[21:20]***		***Day(LSD)/SP[19:16]***			

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:6]	*SP[23:22]*		Bits [23:22] of the scratchpad memory, irrespective whether or not the RTC alarm interrupt is active These bits persist throughout brownout
[5:4]	*Day(MSD)/SP[21:20]*		When the RTC alarm interrupt enable is active, this is the upper BCD digit of the day of the month at which the interrupt should be activated When not used as an RTC alarm, these bits can be used as scratchpad, and persist throughout a brownout condition
[3:0]	*Day(LSD)/SP[27:24]*		When the RTC alarm interrupt enable is active, this is the lower BCD digit of the day of the month at which the interrupt should be activated When not used as an RTC alarm, these bits can be used as scratchpad, and remain throughout a brownout condition

Address(hex): 83

Register Name *RTCAlarm/Scratchpad*			**Description** (R/W) RTC alarm or scratchpad			**Default Value:** 0000 0000 **Reset Event: P**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
SP[15:14]		***Hour (MSD)/SP[13:12]***		***Hour(LSD)/SP[11:8]***			

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:6]	*SP[15:14]*		Bits [15:14] of the scratchpad memory, irrespective whether or not the RTC alarm interrupt is active These bits remain throughout brownout
[5:4]	*Day(MSD)/SP[13:12]*		When the RTC alarm interrupt enable is active, this is the upper BCD digit of the hour at which the interrupt should be activated When not used as an RTC alarm, these bits can be used as scratchpad, and remain throughout a brownout condition
[3:0]	*Day(LSD)/SP[11:10]*		When the RTC alarm interrupt enable is active, this is the lower BCD digit of the hour at which the interrupt should be activated When not used as an RTC alarm, these bits can be used as scratchpad, and remain throughout a brownout condition

Register Descriptions *(continued)*

Address(hex): 84

Register Name *RTCAlarm/Scratchpad*			**Description** (R/W) RTC alarm or scratchpad			**Default Value:** 0000 0000 **Reset Event: P**	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
SP[7]	***Minute (MSD)/SP[6:4]***			***Minute(LSD)/SP[3:0]***			

Bit No.	**Description**	**Bit Value**	**Value Description**
[7]	*SP[7]*		Bit [7] of the scratchpad memory, irrespective whether or not the RTC alarm interrupt is active This bit remains throughout brownout
[6:4]	*Minute(MSD)/SP[6:4]*		When the RTC alarm interrupt enable is active, this is the upper BCD digit of the minute at which the interrupt should be activated When not used as an RTC alarm, these bits can be used as scratchpad, and remain throughout a brownout condition
[3:0]	*Minute(LSD)/SP[3:0]*		When the RTC alarm interrupt enable is active, this is the lower BCD digit of the minute at which the interrupt should be activated When not used as an RTC alarm, these bits can be used as scratchpad, and remain throughout a brownout condition

Applications Information

Initial Power-Up

When VDD is first applied to the chip, the following sequence of events occurs:

1. As VDD starts to rise, the internal references, regulators, and oscillator start to power up. Once VDD gets to approximately 0.9V, the internal power-on reset is asserted and the NRST output pin is guaranteed to be asserted Low. If an external 32.768kHz crystal is connected, it also starts to power up. (The internal oscillator is running long before the crystal oscillator.) The VBAK regulator starts up if VBAK is present, however if VBAK is applied before VDD, then it has no effect on chip operation.

2. After a few hundred microseconds, the internal VREG regulator supplying the core logic starts to power up. VREG settles at approximately 1.6V. If VDD is ramping slowly, then VREG tracks with VDD.

3. As VREG increases, the core logic starts to enter a functional state and is held in its power on reset state. Battery backup mode is inhibited to ensure the chip starts up in VDD mode.

4. Once VREG is above 0.9V, internal power-on reset is negated, and the chip waits for VDD to exceed the minimum VBO threshold of 1.7V + Vhys. (Vhys = Rising threshold hysteresis = 25mV to 100mV).

5. Once VDD passes the minimum VBO threshold, the fuses are read, the calibration and configuration settings are applied (including the new VBO threshold), and the SH3100 is placed into the appropriate operating mode. If the mode allows the SNSE pin to determine the reset duration, then the state of the SNSE pin is read and the appropriate duration selected. If not, the reset duration defaults to the fuse setting.

6. Depending on the mode selected, the chip behavior then proceeds as one of the following:

Standard Operation. VDD Settles at Greater than the Programmed VBO

1. The general-purpose DAC/comparator block and PWM outputs are disabled.

2. Since VDD is greater than the VBO threshold, a counter is started which times the following events.

3. Four ms after the new VBO Reset threshold is exceeded; CLK0 starts at the fuse-programmed frequency. CLK1 also starts if fuse enabled.

4. At the end of the VBO Reset duration period (as selected by SNSE), NRST is negated.

5. The micro controller may now communicate with the SH3100.

6. Battery backup facility is enabled.

7. If an external crystal is connected, then the logic monitors the output from the crystal oscillator clock. Once 1024 cycles have been observed to indicate that it is running in stable operation, then the logic switches over to run on the crystal clock and shuts down the internal oscillator to save power. The HFDCO is then switched from free-running mode to FLL locking mode and smoothly pulls into lock. This is done to avoid having to wait for the crystal oscillator to start up before the SH3100 starts to function. If the crystal oscillator does not start within 10 seconds of power-up, then the crystal oscillator circuitry is disabled to save power.

Applications Information *(continued)*

Standard Operation - VDD Settles at less than the Programmed VBO

1. The general-purpose DAC/comparator block and PWM outputs are disabled.

2. Since VDD is less than the new VBO threshold, the chip is held in brownout until VDD exceeds VBO.

3. nRST is held asserted.

4. If an external crystal is connected, the logic monitors the output from the crystal oscillator clock. Once 1024 cycles have been observed to indicate that it is running in stable operation, the logic switches over to run on the crystal clock and shuts down the internal oscillator. When the SH3100 comes out of reset, the HFDCO starts in FLL locked mode and smoothly pulls into lock after starting at the HFDCO programmed frequency. If the crystal oscillator does not start within ten seconds of power-up, the crystal oscillator circuitry is disabled to save power.

5. Battery backup facility is disabled until the chip has come out of reset.

Automatic Fan Speed Control Enabled

1. The general-purpose 8-bit DAC and comparator are enabled. SNSE transition threshold defaults to 70mV. PWM output is enabled. The VBO Reset duration defaults to the fuse register setting.

2. Internal temperature is measured at one second intervals. Fan speed control based on the default automatic settings is enabled. If no pulses are detected on SNSE, then the chip enters fan control fault condition mode.

3. Once VDD passes the VBO threshold, the normal Reset timer sequence is started. If VDD stays below VBO, then automatic fan control continues to run, but the HFDCO remains disabled, resulting in low power consumption (< 10µA).

4. Once VDD exceeds VBO, CLK0 starts at its programmed rate, and the micro controller may communicate with the SH3100. CLK0 and the HFDCO may then be turned off if required to save power.

5. The micro controller may also modify any of the default fan speed control settings if required, or change from automatic mode to manual mode.

6. If VDD then drops below VBO, NRST is asserted but fan control continues to run until VDD collapses below approximately 1V. If a watchdog reset occurs, then fan control continues during the reset condition.

Applications Information *(continued)*

Switching Regulator Modes Enabled

1. The general-purpose 8-bit DAC and comparator and PWM outputs are enabled. The SNSE input is made available for regulator feedback if required. The VBO Reset duration defaults to the fuse register setting.

2. The appropriate selection of internal circuitry is chosen for the desired regulator configuration.

3. Since the switching regulator requires a high frequency clock for operation, the HFDCO is enabled at its programmed rate even if VDD is still below the VBO threshold. CLK0 and CLK1 outputs are not enabled until VDD exceeds VBO.

4. During power up, the PWM pin is set high impedance and its state is monitored during power-on-reset. If it is detected as being pulled High externally and the mode select is bootstrap boost, then this indicates that there is an inductor from PWM to an external supply and that internal FET switching is required. Once this is detected, the PMOS between PWM and VDD is turned on which clamps VDD to the external supply via the inductor so allowing boost regulation to start for external supply inputs of 1.8 V or above. Until the PMOS is turned on, VDD is approximately one diode voltage below the external supply as it is powered through the diode from PWM to VDD. This detection process also allows the control circuitry to know to set PWM active low during the inductor energize period. If PWM is detected as Low during power up, this indicates that an external switching FET is being used and PWM is set High during the inductor energize period.

5. HFDCO is enabled periodically as required by the control logic to maintain regulation.

6. If switching regulator mode is turned off by the micro controller, then VDD drops. If it drops below the VBO, then NRST is asserted, and HFDCO is turned off. If VBAK is high enough, then the chip goes into battery backup mode. If VBAK is not present, then the chip enters power-on-reset when VDD drops to approximately 0.9V, and if VDD rises again, the chip reloads the mode settings from the fuses and tries to repeat the switching regulator startup sequence. If VBAK is present and VBAK drops below 0.9V, the chip switches back on to VDD. If VDD is above 1.8V at this point, the regulator start-up sequence begins again.

7. If the external supply drops so low that VDD can not be maintained above 1.7V, then the HFDCO clock is disabled and regulation stops. VDD may then collapse down to below the power-on-reset level.

Pad Specifications

Digital Input: CLKIN

General-purpose input pad powered from VDD with a Schmitt input stage. Includes diode protection to VDD and GND. Input switching threshold is approximately VDD/2; however, in order to ensure that no power supply current flows during steady state conditions, the input should settle to within 0.4V of either VDD or GND.

Parameter	Symbol	Min	Max	Units
Input Hysteresis	V_{HYS}	100	800	mV
V_{IN} High	V_{IH}	VDD - 0.4		V
V_{IN} Low	V_{IL}		0.4	V
Input Leakage Current	L_{IN}		10	nA
Input Pin Capacitance	C_{IN}		10	pF

Tri-State/Analog Input: SNSE

Dual mode pad set by fuse mode selection. Includes diode protection to VDD and GND. In Mode 1, the pad is used to set the duration of the system reset. It is tri-state so it can detect Low, Floating and High inputs. The state of the pad is sampled during start-up and is then disabled to save power.

In Mode 2, the analog voltage on SNSE is input directly to the general-purpose comparator stage and compared with the output of the 8-bit DAC. Input voltage should be maintained within 0V and 1.6V.

Parameter	Symbol	Min	Typ	Max	Units
Input Voltage Range	V_{IN}	0		V_{REG}	V
Input Current in Mode 1	I_{IN}	-30		+30	µA
Input Current in Mode 2	I_{DD}			10	nA
Mid Level Bias (mode 1)	V_{MID}		0.47 x V_{REG}		V
Logic Low Input (mode 1)	V_{IL}			0.42 x V_{REG}	V
Logic High Input (mode 1)	V_{IH}	0.52 x V_{REG}			V
Input Pin Capacitance	C_{IN}			10	pF

Pad Specifications *(continued)*

Dual Supply Digital Output: CLK0 & CLK1

Digital output pad able to drive clock outputs at up to 33.5MHz powered from either the VDD or VBAK supplies. Includes diode protection to GND.

Parameter	Symbol	Min	Max	Units
V_{OUT} High (Vdd > 3.3V, Ioh = 4mA)	V_{OH1}	Vdd – 0.4	Vdd	V
V_{OUT} Low (Vdd > 3.3V, Iol = 4mA)	V_{OL1}	0	0.4	V
V_{OUT} High (Vdd > 1.7V, Ioh = 1mA)	V_{OH2}	Vdd – 0.25	Vdd	V
V_{OUT} Low (Vdd > 1.7V, Iol = 1mA)	V_{OL2}	0	0.25	V
Pad Rise time (10 pF load, 10 – 90%)	T_r		15	ns
Pad Rall time (10 pF load, 10 – 90%)	T_f		15	ns

Note: VDD may be either VDD or VBAK depending on supply selected. VDD is always VBAK when driving out 32.768 kHz in battery backup mode.

Asymmetric Drive Digital Output: NRST

Asymmetric digital output pad with hard pull-down and weak pull-up. This is used to provide the active low reset output to the microcontroller. The weak pull-up is implemented as a resistance to VDD and allows the NRST pin to be pulled low if required by an external device. Includes diode protection to VDD and GND.

Parameter	Symbol	Min	Typ	Max	Units
Rout High (Weak pull-up to VDD)	R_{OH}	17	20	23	kΩ
Vout Low (VDD > 3.3 V, Iol = 4 mA)	V_{OL1}	0		0.4	V
Vout Low (VDD < 1.7 V, Iol = 1 mA)	V_{OL2}	0		0.2	V
Pad rise time (20 pF load)	T_r		300		ns
Pad fall time (20 pF load)	T_f			15	ns

Pad Specifications *(continued)*

Dual Drive Digital Bidirectional: INT

This is a bi-directional digital pad with optional High or Low output drive strengths. It includes a Schmitt input stage. The pin may be used either as the Interrupt output or as a general-purpose I/O (GPIO).

Low drive strength is implemented as a pull-up or pull-down impedance to allow the pin to be overdriven by an external source if required. Supply is VDD and the pad includes diode protection to VDD and GND.

Parameter		Symbol	Min	Max	Units
High Drive	Vout High (VDD > 3.3 V, Ioh = 4 mA)	V_{OH1}	VDD – 0.4	VDD	V
	Vout Low (VDD > 3.3 V, Iol = 4 mA)	V_{OL1}	0	0.4	V
	Vout High (VDD > 1.7 V, Ioh = 1 mA)	V_{OH2}	VDD – 0.25	VDD	
	Vout Low (VDD > 1.7 V, Iol = 1 mA)	V_{OL2}	0	0.25	
Low Drive	Rout High (Weak pull-up to VDD)	R_{OH}	17	23	kΩ
	Rout Low (Weak pull-down to GND)	R_{OL}	17	23	kΩ
Input mode	Vin High	V_{IH}	VDD - 0.4		V
	Vin Low	V_{IL}		0.4	V
	Input pin capacitance	C_{IN}		20	pF
	Input hysteresis	V_{HY}	50	500	mV
Timing	Pad rise time (10 pF load)	Tr		10	ns
	Pad fall time (10 pF load)	Tf		10	ns

Note: If the INT pin is programmed as a GPIO input (default state), it must be tied high (VDD) or low (GND) to ensure that a floating input does not cause excessive current consumption in the digital input stage.

Pad Specifications *(continued)*

I²C Communication: SCL & SDA

The I²C pads are designed to comply with the 400kHz (Fast) I²C specification. The pads are open drain outputs with diode protection only to GND. This allows VDD to collapse without affecting the common bus. Input stages include input hysteresis and glitch filtering to allow handling of noisy inputs. High levels and rise times are set by external pull-up resistors on SCL and SDA.

Parameter	Symbol	Min	Max	Units
Maximum operating frequency	F_{OP}	1		MHz
Vout Low (Iol = 3 mA, VDD > 2V)	$V_{OL}1$		0.4	V
Vout Low (Iol = 3 mA, VDD < 2V)	$V_{OL}2$		0.2VDD	V
Vin High	V_{IH}	0.7VDD		V
Vin Low	V_{IL}		0.3VDD	V
Input hysteresis (VDD > 2 V)	$V_{HYS}1$	0.05VDD		V
Input hysteresis (VDD < 2 V)	$V_{HYS}2$	0.1VDD		V
Input glitch rejection	T_{SP}	50	100	ns
Input leakage	I_{IN}	-10	10	µA
Input capacitance	C_{IN}		10	pF
Output fall time (Load Cb = 10 pF to 400 pF)	T_F	20 + 0.1Cb	300	ns

Multi-Function Output: PWM

Multi mode pad with function determine by operating mode selection. Includes diode protection to VDD and GND. Mode 1 is a standard digital output powered from VDD. Used for general-purpose PWM drive, fan speed control, or switching regulation using external switching transistors.

Mode 2 is for bootstrap boost regulation with internal switching. PWM is pulled Low to energize the inductor and then set High Impedance to allow energy transfer to VDD through the protection diode. Mode 3 is the power output from the LDO.

Parameter	Min	Typ	Max	Units
Vout High (Mode 1, VDD > 3.3 V, Ioh = 4 mA)	Voh1	VDD – 0.4	VDD	V
Vout Low (Mode 1 or 2, VDD > 3.3 V, Iol = 4 mA)	Vol1	0	0.4	V
Vout High (Mode 1, VDD > 1.7 V, Ioh = 1 mA)	Voh2	VDD – 0.25	VDD	V
Vout Low (Mode 1 or 2, VDD > 1.7 V, Iol = 1 mA)	Vol2	0	0.25	V
Pad rise time (Mode 1, 10 pF load)	Tr		10	ns
Pad fall time (Mode 1 or 2, 10 pF load)	Tf		10	ns
LDO output voltage range (Mode 3)	Vldo	3	4.5	V

32.768 kHz Crystal Oscillator

The crystal oscillator uses a current-starved design to minimize current consumption. It includes a 5-bit adjustable padding capacitance to GND on both XIN and XOUT to allow optimization of the crystal load capacitance under varying conditions.

The 5-bit control selects one of 32 padding capacitances from 10pF to 44pF in a geometric progression. This nonlinear capacitance curve compensates for the non linearity of the crystal and results in a net linear progression of frequency with adjustment code.

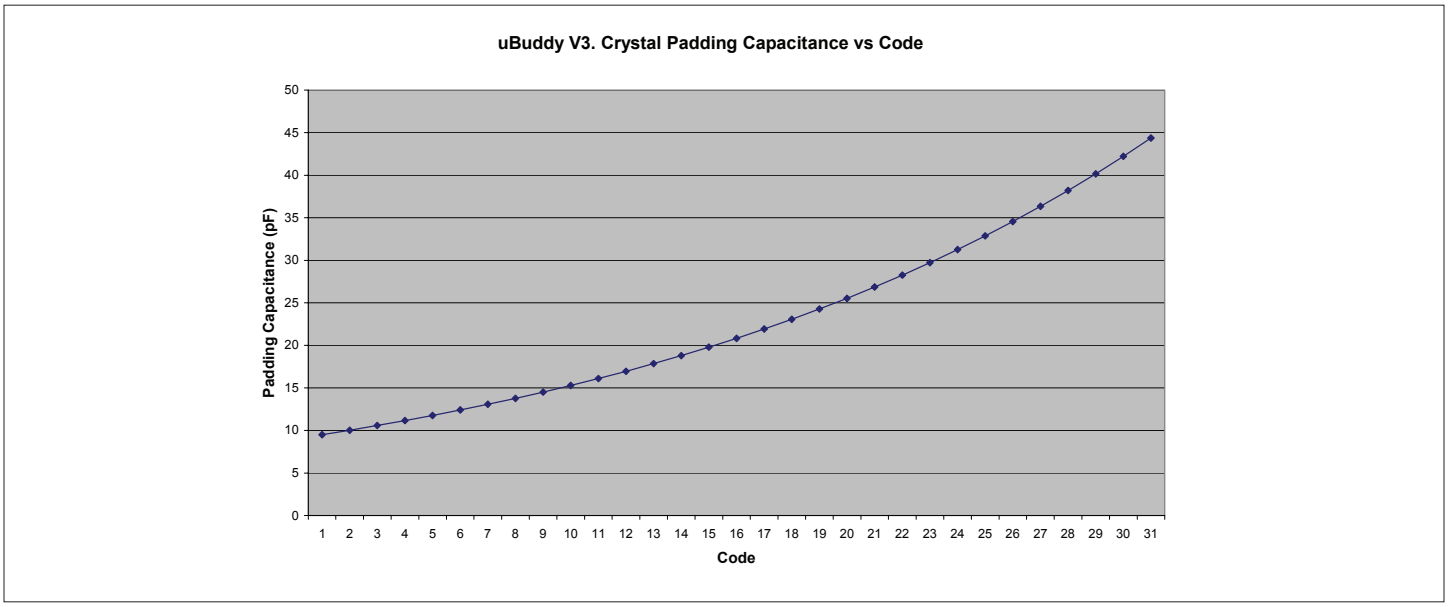
This allows the crystal frequency to be maintained within ±2ppm of 32.768 kHz over temperature, by measuring temperature using the on chip temperature sensor, and then adjusting the padding capacitance accordingly, using a look-up table for that particular device/crystal/PCB combination.

Note: If no crystal is present, XIN should be tied to ground to avoid noise pickup on XIN being misinterpreted as crystal oscillations.

Note: There is no failsafe function on the crystal oscillator, so if the crystal fails during normal operation, the SH3100 hangs up and needs to be power-cycled to allow a fresh start-up. If the crystal does not start up within ten seconds of the next power-up, then it is ignored, and the internal 32kHz oscillator is used as the system clock.

Parameter	Symbol	Min	Typ	Max	Units
Crystal operating frequency	Fx		32.768		kHz
Duty cycle	DC	25	50	75	%
Start-up time	Tst			3	seconds
Min padding capacitance	Cmin	9	10	11	pF
Max padding capacitance	Cmax	32	36	40	pF
ppm adjustment resolution	Rppm		5		ppm
XIN input switching threshold	Vth	0.3	0.5	0.7	V
XOUT pull-up current	Ixout	450		750	nA

Plot of Crystal Padding Capacitance versus Adjustment Code



Note: The MSB of the 5-bit control word is inverted to ensure that mid range capacitance is used as default for an unprogrammed device with all zeros in the control register.

Internal 32.768 kHz Oscillator

The SH3100 is capable of functioning with or without an external 32.768kHz crystal. The chip includes an internal oscillator which is fuse calibrated on test to provide a 32.768 kHz clock source as an integrated alternative to the crystal oscillator. accuracy is better than ±3% over temperature and supply voltage, and initial accuracy at 25°C is better than ±1%. The internal oscillator starts within 100µs of power being supplied to the chip and acts as the low frequency system clock for quick chip initiation.

This means that if a short reset duration has been programmed, the high frequency output clock can be ready very soon after a completely cold start. If a crystal is present, the crystal oscillator starts up within approximately two seconds and then takes over from the internal oscillator as the system clock. The internal oscillator is then shut down to save power. If no crystal is present, then the internal 32.768kHz oscillator continues to run as the system clock, and the crystal oscillator circuitry is shut down to save power, if it has not started up within 10 seconds of power-up. Once in normal operation, it is possible for the microcontroller to override the clock selection by I^2C access, although this would normally only be required for test purposes.

The main reasons for requiring a 32.768kHz crystal are to obtain a very accurate RTC or high frequency clock. If neither of these requirements is critical then it is acceptable to save costs by removing the crystal and just using the internal oscillator.

Note: If no crystal is present, XIN should be tied to ground to avoid noise pickup on XIN being misinterpreted as crystal oscillations.

Functional Descriptions *(continued)*

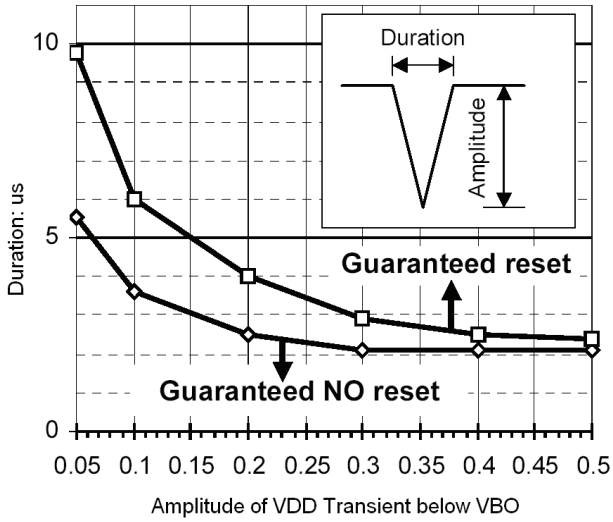
System Reset – Programmable VDD Threshold (VBO)

The SH3100 has two dedicated supervisory functions that manage the reset of the microcontroller, a low VDD monitor (Brownout Detector) with programmable threshold (VBO) and a Watchdog Timer with programmable timeout. Both functions are integrated with the Clock Management System to provide a more complete solution than with standalone components. The SH3100 NRST output pin is active Low with strong drive to the active state and weak drive to the inactive state. This eliminates the need for an external pull-up and allows the NRST pin to be connected in common with other reset sources in a wired-OR configuration.

During power-up, the NRST pin is guaranteed to be correctly asserted by the time VDD reaches 1V. It then stays asserted until VDD exceeds the programmed VDD threshold (VBO) + hysteresis, at which point the SH3100 enters the power up routine with the appropriate sequencing of clock start and NRST negation as determined by the **programmable reset duration** setting. Flags in the register map indicate the cause of reset to the microcontroller. Once powered up, the SH3100 continuously monitors VDD and generates a system reset on the NRST pin if VDD drops below VBO. VBO is set by a 7-bit control code to be between 1.7V and 4V with 24mV resolution. When VDD drops below VBO, this is defined as a brownout event, and if VBAK is present, the chip switches to battery backup mode to maintain register contents and RTC operation at very low current consumption. If VBAK is not present, backup mode operation continues to run from VDD until VDD drops below 1V.

Note: If VDD is likely to collapse very quickly to GND (Less than 100µs) then it is advisable to add an external 100 nF decoupling capacitor on VREG to maintain register contents while the chip changes over to battery backup mode.

The default VBO setting is loaded from nonvolatile memory on power up, but once the chip has come out of reset, it may be changed to any other value using an I^2C access, or it can be permanently protected from any changes by setting the VBO lock flag or the write protect flag. To avoid the system jumping in and out of reset for noisy VDD levels near VBO, there is hysteresis on the reset function. When VDD is falling, NRST asserts at VBO. When VDD is rising, NRST negates at VBO plus the hysteresis (Vhys). There is also internal filtering on the VDD comparator which is set to allow rapid detection of a collapsing VDD while rejecting VDD noise spikes of less than a certain duration and amplitude as shown by the diagram to follow:



Parameter	Symbol	Min	Typ	Max	Units
VBO for Min code (000 0000)	VBOmin	1.65	1.7	1.75	V
VBO for Max code (101 1110)	VBOmax	3.95	4	4.05	V
VDD Hysteresis	Vhys	25		100	mV
VDD falling to NRST asserted delay	Td			5	µs
VBO resolution	Vres	20	24	28	mV
New VBO settling time	Tvbo			4	ms

Programmable Reset Duration

The programmable reset duration is set by a combination ofv a single pin and a 5-bit nonvolatile memory (fuse) register. In normal operating mode the state of the SNSE pin determines the reset duration as follows:

- If SNSE is connected to GND, then the minimum reset duration of 6ms is selected.
- If SNSE is floating, then an intermediate reset duration of 270ms is selected.
- If SNSE is connected to VREG, then the reset duration as set by the register is selected.

If the SH3100 is operating in one of the non standard modes then the reset duration defaults to the register setting.

The reset duration is defined as the time from the end of a reset condition until NRST is negated.

NRST is always asserted immediately at the start of a reset event. Regardless of its programmed frequency, CLK0 continues to run at approximately 700kHz for 2ms after NRST is asserted. This is in case the microcontroller needs a few clock cycles to tidy up internal registers after reset starts. In the case of reset caused by rapidly falling VDD, CLK0 stops if VDD drops below 1.7V during the 2ms of the post-NRST-assert period.

Note 1: CLK0 always starts at the programmed rate 4 ms after the end of a reset condition. This is to ensure that the microcontroller has a clock source running before NRST is negated. Some microcontrollers, which use PLL clock multiplication to generate internal clocks from CLK0, may need a long time to lock onto CLK0, therefore they need a reset duration greater than the lock time of their internal PLL multiplier.

Note 2: When a brownout reset condition occurs, the start-up sequence timer can not start until after a time equal to the programmed reset duration has elapsed. This means that for very short brownout events, the observed reset duration on NRST is double the programmed reset duration.

Note 3: Reset events caused by watchdog timeout or watchdog violation also result in NRST being asserted for double the programmed reset duration.

Note 4**:** On initial power-up, once VDD exceeds VBO, NRST stays asserted for the programmed reset duration.

Note 5: If a new reset duration is loaded which is larger than the current reset duration, this immediately triggers a programmed reset at the new duration. When the reset ends, the new duration is effective for further resets.

Note 6: These reset durations are dependent on the accuracy of the internal 32.268kHz system clock, which may vary by up to ±3% from the stated figures.

The mapping between the register setting and Reset duration is as follows:

Code	Duration	Code	Duration	Code	Duration	Code	Duration
0	6	8	78	16	366	24	1518
1	12	9	102	17	462	25	1902
2	18	10	126	18	558	26	2286
3	24	11	150	19	654	27	2670
4	30	12	174	20	750	28	3054
5	42	13	222	21	942	29	3822
6	54	14	270	22	1134	30	4590
7	66	15	318	23	1326	31	5358

Functional Descriptions *(continued)*

System Reset - Watchdog Timer (WDT)

The watchdog is the other dedicated supervisory function that manages the micro controller reset. Once enabled, it requires the micro controller to alternately write two unique codes (0x5A, 0xC3) to the *WDTCode* register. Failure to write the correct code before the timer expires causes a reset, as does writing an invalid code. This function is disabled on power-up, and is only enabled once it has been initialized.

Note: Once enabled, the WDT cannot be disabled.

By default (non *AutoWDTSuspend* mode), the watchdog runs at a rate determined by the *WDTPrescaler* register, either 128Hz, 64, 32 or 16Hz, and counts up to a maximum of 128 counts, which relates to a maximum timeout period of 1, 2, 4 or 8 seconds respectively.

In order to prevent the WDT from timing out while the processor is legitimately asleep for a long period, the WDT can be optionally set (by setting the *AutoWDTSuspend* bit of the *Config* register) to be divided down from CLK0, instead of from the default selected 32.768kHz source. In this mode the WDT counter counts processor cycles, rather than real time, and can be set for a timeout period of between 256 and 262144 processor cycles determined by *WDTPeriod* and *WDTPreScaler*. This means that the watchdog function sleeps while the HFDCO clock is in standby.

The *AutoWDTSuspend* register bit can only be written to prior to WDT initialization. When the WDT times out, the cause can be identified by reading the *CauseOfReset* register.

System Reset - Manual Override

A system reset can be manually triggered by momentarily pulling down the NRST pin. This is detected by the SH3100, which then holds NRST low for the programmed reset duration. After the reset period ends, NRST is released and pulled high by the internal 20KΩ pullup.

To correctly detect a manual reset, the NRST pin should be pulled low for a period of at least 50ns. This can be achieved by adding a 47pF capacitor to ground on the NRST pin. This gives an effective RC rise time on NRST of 1µs, which is sufficient to ensure that NRST stays low for long enough to be detected, even if initially held low for only 1ns.

Note 1: If manual reset is triggered by a momentary pulldown on NRST, the start-up sequence timer can not start until after a time equal to the programmed reset duration has elapsed. This means that for very short manual reset events, the observed reset duration on NRST appears to be double the programmed reset duration

Note 2: If manual reset is held low for longer than twice the programmed reset duration, then when it is released, NRST rises back to VDD with no further delay.

Note 3: A reset of this type sets the *Brownout Event* status flag.

Real Time Clock (RTC)

The RTC is a 47-bit Binary+BCD counter clocked by a 256 Hz clock derived from the internal 32.768 kHz clock. The RTC is always enabled and continues to run during battery backup and WDT resets. The RTC runs for 99 years before overflowing, and incorporates leap-year adjustment up to the year 2100. For synchronization purposes, the RTC should be read LSB first – this causes all seven bytes to be latched into the serial interface simultaneously in order to avoid problems of byte-overflow between individual byte reads. The RTC should also be written MSB first. Only when the LSB is written are the entire six bytes loaded into the RTC counter. The RTC incorporates an alarm register which causes an interrupt at a specified time with 1 minute resolution. When the alarm is not being used, the register may be used as a scratchpad, as it remains throughout brownout and WDT events.

Note: The RTC read value may not be updated until one 256Hz cycle after an RTC write. Also, the shadow register used to synchronize both reads and writes between the two clock domains is shared with the PIT and the *DCOCode*, so the implication of this is that after writing to any one of these registers, the microcontroller software must wait for a period of the relevant counter before writing any one of the others. (e.g., having written to the RTC, the software can not write to the PIT or *DCO Code* within one 256Hz cycle (4ms).

Note: RTC accuracy is dependent on the accuracy of the crystal oscillator or internal 32.268kHz clock, whichever is being used as the internal system clock.

Register	Format	No. of Bits	Description	Range
RTC0	Binary	8	256ths seconds	0x00 – 0xFF
RTC1	BCD	7	Seconds	0x00 – 0x59
RTC2	BCD	7	Minutes	0x00 – 0x59
RTC3	BCD	6	Hours	0x00 – 0x23
RTC4	BCD	6	Day of the month	0x00 – 0x31
RTC5	BCD	5	Month	0x01 – 0x12
RTC6	BCD	8	Year	0x00-0x99

Functional Descriptions *(continued)*

Periodic Interval Timer (PIT)

The PIT is clocked at 32.768kHz. The interval timer uses the 32-bit *WakeUpTime* register as its ultimate count value. Although the timer continues to run, the interrupt remains active until reset by software. The timer is disabled at power up until the period is initialized.

Period = *WakeUpTime*/32768 to give a range of 30.5µs up to 36.4 hours with 30.5µs resolution, subject to the tolerance of the crystal or internal oscillator.

For synchronization purposes the PIT should be read LSB first – this causes all four bytes to be latched into a shadow register in the *SerialIF* simultaneously in order to avoid problems of byte-overflow between individual byte-reads. The PIT counter can not be written directly, but is reset whenever the LSB of the *WakeUpTime* register is written to start a fresh period. The *WakeupTime* register should be written MSB first, and only when the LSB is written are the entire four bytes loaded into the *WakeupTime* register in the PIT block.

> Note: The *WakeupTime* register remains throughout brown-out and WDT events, and may be used as a general purpose scratchpad, if not used for its primary purpose.

Because the PIT shares a shadow register with the RTC and *DCOCode*, and the same register is used for both reads and writes, it is important that none of these registers are accessed within one period of the last timer written to (therefore 31µs after the wakeup time has been updated, or 4ms after the RTC has been written, or immediately after the HFDCO has been written).

Interrupt Operation

There are five sources of interrupt:

- PIT interrupt – generates an interrupt every time the PIT expires
- RTC alarm interrupt
- General-purpose comparator interrupt
- A/D conversion complete
- Fan speed control fault (absence of pulses on the SNSE pin, or duty cycle is 100%) – this is combined with the general-purpose comparator interrupt

All these interrupts may be individually enabled by seting the relevant field in the *IntEnable* register, and cleared by setting the relevant bit in the *IntStatus* register. The INT pin is highly configurable via the *AlternateINTFunction* register:

- The mode can be specified as level sensitive (the active level remains until the interrupt has been cleared), or edge sensitive (a pulse with period equal to 4 cycles of CLK0, which repeats every time a new interrupt source is activated, thereby removing the need to clear periodic interrupts).
- The polarity can be programmed – the INT pin is pulled (weak) inactive, in order that it may be wire-ORed with any other source, and harddriven to the active state.
- Any individual interrupt can either be cleared by setting the relevant bit(s) in the *IntStatus* register, or with a special short-form version of the I^2C protocol as described in the next section.
- The interrupt can be programmed to toggle (PIT nly), and can be used in this way to generate a very slow square wave output with a period between 61.035µs up to 72.8 hours with 61.035µs resolution. In this mode, the INT output drives hard both states, rather than being pulled to one.
- The INT pin can also be programmed as a general-purpose I/O port.

Additionally, the general-purpose comparator interrupt can be programmed to activate on either the rising or falling edge, so that the interrupt triggers either when the comparator level rises above its DAC-set threshold, or when it drops below it, by programming the relevant bit in the *Config* register.

The INT output is always hard-driven back to its inactive state before returning to weak pullup/down, in order to provide a sharp trailing edge.

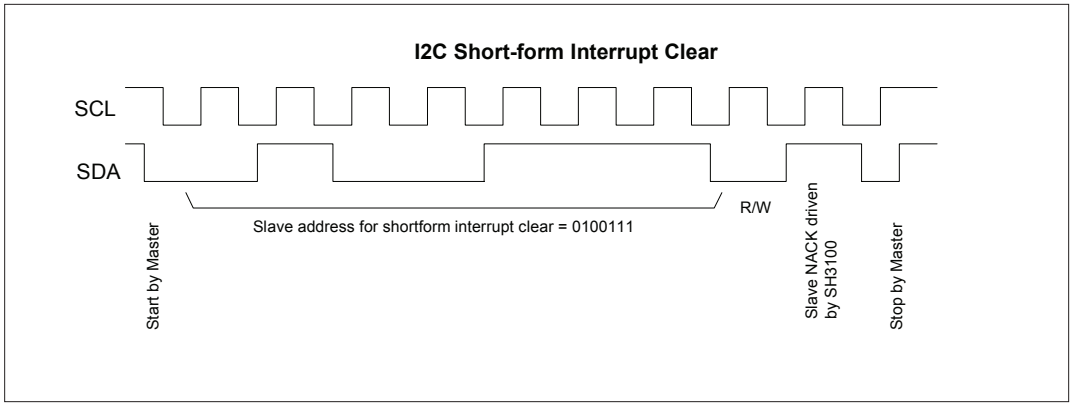
Note: The SNSE interrupt can be used as a periodic interrupt independent from the PIT, because if SNSE is inactive, then an interrupt is generated every 32768 CLK1 cycles. Therefore if CLK1 is set for 32.768kHz output (which can of course be done irrespective of HFDCO setting), then this gives an exact 1Hz interrupt, while still leaving the PIT free.

Functional Descriptions *(continued)*

I²C Short-Form Interrupt Clear

All active interrupts can be simultaneously cleared using a short-form version of the I²C access. This gives much faster interrupt clearing than normal individual I²C access.

An access is started to slave address (0b0100111), but terminated with a STOP instruction immediately after the ACK position (which is not sent by the SH3100 for that address), as shown in the following diagram:



General Purpose 8-Bit DAC & Comparator

The negative input of the comparator is driven by the output of the DAC, and the positive input by one of 4 possible input signals determined by a 4:1 analog multiplexer. Operation is enabled by the *DACEn* bit.

The DAC is an integrating switched capacitor type and is normally clocked at 32.768kHz, so it can run when the HFDCO clock is disabled. The DAC can be set to a higher frequency by setting the 2-bit *DACClkDiv* register.

The 4 inputs are VDD, VBAK, temperature, and SNSE and are selected by the 2-bit *DACSel* register.

SNSE is a general-purpose analog input from the SNSE pin, and can be used only if the SNSE pin is not being used for other purposes. The voltage on SNSE must always be less than VREG.

Temperature has internal calibration correction stored in nonvolatile memory. This compensates for process inaccuracies in the temperature sensor to allow absolute temperature accuracy of ±2°C.

Note 1: To convert the DAC reading into temperature in degrees Celsius, subtract the decimal DAC value from 163.

Note 2: Even though the DAC allows for a theoretical temperature range of -92°C to 163°C, operation should be assumed to be linear only in the -40°C to 85°C range. Temperature resolution is nominally 1 code step per °C.

Note 3: If VBAK is being monitored, then there is additional current drain of a few µA from VBAK due to an internal resistive divider.

The block can operate in one of two modes.

In Mode 1, the DAC is programmed with a fixed value using the *ForceDACValue* register and the appropriate input signal is selected. The comparator output is then monitored and when the signal either rises or falls through the DAC threshold (as set by register bit *Comparator Interrupt Polarity*) an interrupt is generated on the INT pin. This can be useful, for example, as an independent monitor to give a low voltage warning on VDD or VBAK without triggering full sy stem reset or for warning if the ambient temperature rises above or falls below set thresholds. The comparator output state can also be read directly from the status register.

In Mode 2, the DAC and comparator are programmed within a successive approximation ADC controlled by the logic. This allows ADC conversion to be performed on any of the four inputs. The conversion is started by setting the *InitiateA2D* register bit in the *Config* register. Conversion completes in approximately 1000 cycles of the *DACClk* frequency, and is indicated by the *ADCComplete* interrupt and interrupt status. In automatic fan speed control mode (the default mode of the SH3100), the block is automatically set up in ADC mode to measure temperature. The following tables show the four possible input signals and signal values for different DAC codes, plus the functional specifications.

DACSel(1,0)	Input	DAC = 0	DAC = 78	DAC = 138	DAC = 203	DAC =255	Units
00	VDD	0.03	1.47	2.58	3.78	4.74	V
01	VBAK	0.03	1.47	2.58	3.78	4.74	V
10	Temperature	163	85	25	-40	-92	°C
11	SNSE	0.01	0.49	0.86	1.26	1.58	V

Parameter	Symbol	Min	Typ	Max	Units
DAC switching frequency	DACclk	32		2000	kHz
DAC DNL	DNL		± 0.5		LSB
DAC INL.	INL		± 2		LSB
Comparator switching delay	Td			3	µs
DAC settling time	Tst			128	DACclk
Minimum DAC setting			0.01		V
Maximum DAC setting			1.58		V
DAC resolution			6.1		mV

Temperature Measurement

During Mode 3 (Auto Fan Speed control), temperature measurements are made continuously, and it is only necessary to read register 0x16 (*ADCResult*) to make a temperature reading at any time.

In other modes, temperature measurement needs to be manually set up by selecting the temperature input to the ADC and initiating an ADC conversion as described in the previous section.

The contents of the *ADCresult* register are converted to temperature as follows:

- Temperature = (TK - *ADCResult*) + K * (T - 25°C)
- TK = 163 when system clock is running from 32.768kHz crystal oscillator
- TK = 166 when system clock is running from the internal 32.768kHz oscillator (crystal not present)

K is the slope error of the temperature conversion curve and can vary between -0.1 and +0.1. This effectively means that the temperature conversion slope can vary between 0.9°C and 1.1°C per code step. Factory calibration is carried out at 25°C to give a typical error of ± 1°C and a maximum error of ± 2°C at room temperature.

PWM Operation & Fan Speed Control

The PWM function is implemented as a 10-bit PWM counter clocked at the CLK1 rate. Therefore, if CLK1 is set to 32.768 kHz, the PWM repeat rate is 32 Hz.

The PWM duty cycle can either be set directly by writing to the *ForcePWMDutyCycle* register or may be programmed to track the temperature in *AutoPWMMode*.

The PWM function normally operates in standard PWM output format, but it can be programmed to operate in PDM (Pulse Density Modulation) mode, which outputs the same energy density, but distributed more evenly over the PWM cycle. This is useful when the PDM output is going to be filtered to generate a DC level.

Auto-PWM Mode (Fan Control Mode)

This is an application of the PWM function which operates in conjunction with the general purpose 8-bit DAC and comparator to provide automatic fan speed control. It can be enabled by setting the SMPS mode bits in the registers such that operation commences immediately on power-up. The external application circuitry is shown in operating mode 3.

AutoPWMMode has been designed as a flexible fan control engine for brushless DC motors, providing a PWM duty cycle proportional to the temperature. When in *AutoPWMMode*, temperature is measured once per 32 PWM cycles which means once per second at the power-up default rate of 32 Hz.

Fan speed control uses the SNSE input to detect when the fan has stalled. While the fan is running, voltage transients on the SNSE pin crossing the set threshold indicate to the controller that the fan is running correctly. If the SNSE transitions cease for more than 1 second, then this indicates that the fan has stalled, and the PWM duty cycle should be set to 100% to try to restart the fan. Both positive and negative going transitions are detected, so if the SNSE signal stops in any state, then fan stall is detected.

Auto-PWM Engine Features:

- 7-bit minimum temperature setting register, which defines, with 2°C resolution, the temperature at which the PWM comes on. The state machine incorporates 4°C of hysteresis to prevent the fan from continually switching on & off when the temperature is approximately the minimum.
- 10-bit minimum duty cycle register (shared with the *ForcePWMDuty* when not in *AutoPWMMode*), which defines the starting duty cycle.
- 5-bit *DutyCycleStepSize* register, which determines the duty cycle increments per °C. This register along with the *MinTemp* register determines the maximum temperature.
- The PWM starts at 100% duty cycle for between 1 and 2 seconds to kick-start the motor, before settling to MinDutyCycle. Thereafter it tracks with temperature.
- If the SNSE input pulses cease, the PWM generates 100% duty cycle for 1 or 2 seconds, and if there are still no pulses, enters the FAULT state and generates an interrupt.
- If the duty cycle reaches 100% due to the maximum temperature being reached, an interrupt is generated.
- Software can read the *AutoPWMDutyCycle* register to determine the current duty cycle is for diagnostic purposes.
- The PWM counter is clocked from the same source as CLK1. The CLK1 output does not need to be enabled. In theory, this allows the PWM rate to be varied up to a maximum PWM repeat rate of 32.7 kHz (33.5 MHz/1024) , but since the temperature measurement interval scales with PWM rate, the ADC conversion rate or the SNSE pulse repeat rate limits the effective maximum CLK1 frequency.

Functional Descriptions *(continued)*

Auto-PWM Engine Features (Cont.)

- The main control registers are loaded on powerup with values corresponding to a minimum temperature of 40°C, minimum duty cycle of 25%, and a duty cycle step size of 17, which gives a maximum temperature of 85°C. The *ForceDACValue* register is set to 11 to give a comparator reference level of 76mV, which is the switching threshold for the SNSE input. All of these registers can be overridden at any time by I^2C access.

Erratum

The Automatic Fan speed control requires correction as follows:

- *With the power-up default settings, once the temperature rises above 40ºC, the SH3100 kick-starts the fan at 100% for 1 second, and then starts incrementing the PWM duty cycle (at 1.66%/ºC) from its starting position of 25% until it reaches its target duty cycle for that temperature. This is correct.*

- *As the temperature drops, the PWM duty cycle should track down with temperature. What happens, however, is that the duty cycle drops immediately to 25%, and stays at this rate until the temperature rises above the maximum that it reached before it started dropping. The duty cycle then starts to increment the duty cycle as before until it reaches its target duty cycle for the new temperature. This means that automatic temperature regulation controlled by the fan would not function correctly.*

This drastically reduces the utility of the automatic fan control mode. However, since this mode implements automatic temperature measurement and SNSE pin monitoring, it may be useful to enable this mode and then have the microcontroller read the temperature register regularly and manually adjust the starting PWM setting according to the temperature. Setting the increment register to zero means the PWM rate stays set at the value loaded into the starting PWM register. This reduces the time the microcontroller needs for reading temperature and monitoring the SNSE pin in full manual mode.

Manual PWM Control

When the *SMPSMode* bits are set for NORMAL operation (i.e. “00”), the PWM output can be manually set up to give any duty cycle from 0 to 100% in approximately 0.1% steps (1024 steps). The repeat rate is 1024 cycles of the CLK1 frequency. CLK1 output does not need to be enabled. Thus for CLK1 at 32MHz, PWM repeat rate is 32µs, with a minimum pulse width of 31.25ns, and if CLK1 is set to 244Hz, then the PWM repeat rate is over 4 seconds, with a minimum pulse width of approximately 4 ms.

In Manual mode, absence of SNSE pulses can still be detected as interrupts, and SNSE activity can also be detected by setting the general-purpose comparator to SNSE, and enabling the general-purpose comparator interrupt, or by polling the Status register.

In Manual mode, temperature can be measured by initiating an ADC conversion of temperature as normal, although while the conversion is taking place, the SNSE pin can not be monitored.

Note: For correct SNSE pin monitoring, it is necessary to include a simple high pass filter between the sense resistor of the fan drive transistor and the SNSE input on the SH3100. This is required to allow only the high speed commutation pulses to pass through to the SNSE pin. If the filter is not present, the switching pulses caused by the drive transistor could be mistaken for commutation pulses, so the SH3100 would not be able to detect a fan stall condition when the commutation pulses stop. The Mode 3 circuit diagram in the application diagrams section shows this filter. Recommended filter component values assuming the default SNSE threshold of 76mV are:

R1	39 KΩ
R2	15 KΩ
C1 1	0 nF
Rsense	2 to 5Ω

This does bias the SNSE pin at a DC level of 440 mV, and negative transients on the small commutation sense resistor (Rsense) are coupled through the filter and are detected as commutation pulses on the SNSE input when they cross the 76mV threshold.

Functional Descriptions *(continued)*

PDM Mode

An alternative to Pulse Width Modulation (PWM) is Pulse Density Modulation, or PDM. This produces the maximum number of pulses while maintaining the average duty cycle, thereby requiring less smoothing capacitance on the PWM output to yield the same ripple. Both automatic fan control mode and Manual PWM control mode have the option of running PDM instead of PWM by setting the PDM/PWM bit in the *DutyCycleStepSize* register.

Functional Descriptions *(continued)*

Switching Regulator Operation

The general-purpose DAC8 and comparator can be used in conjunction with the PWM output pin as a general-purpose switching regulator control. The various regulation modes are listed in the Operating Modes section and cover a variety of boost and buck configurations. In all cases the switching frequency is set by the CLK1 rate and the regulated voltage by the DAC8 setting.

Note 1: If the HFDCO oscillator has been put into standby by the microcontroller, then it is turned on automatically as required for regulation, and then turned off again until the next inductor energize cycle.

Note 2: Since fan control, LDO, and the switching regulators all use the PWM pin, operation is mutually exclusive. It is not possible to use the other features while one is active.

The regulator feedback may be from VDD, VBAK or the SNSE pin as selected by the value of the 2-bit DACsel register. In the case of VDD and VBAK, they are divided by three before being compared with the DAC level. This means that the regulated level on VDD or VBAK is three times the DAC setting. In the case of SNSE feedback, the regulated level depends on the ratio of the external divider.

In all cases, the inductor energize period is eight cycles of the CLK1 frequency followed by at least one cycle of transfer period. If the output voltage has stabilized, then the energize period only needs to activate occasionally as triggered by the feedback voltage passing through the DAC threshold. This means that for standby level loads, the regulator only needs to activate very infrequently in order to maintain regulation, and since the HFDCO clock is turned off between energize cycles, the average current consumption taken by the SH3100 is very close to the standby current consumption of < 10µA.

The various modes may be set in the register so that they are enabled immediately on power up, or they may be activated later in normal operation. In addition, the start-up regulation level may be stored in the 4-bit DACLevel register to give the following DAC settings on power up. In boost mode, the DAC level starts off at 0.73V and then ramps to the programmed value over a few ms. This is to avoid excessive start-up overshoot in boost mode regulation.

Note 3: The switching regulator function is intended only as a low-cost support function and does not incorporate full synchronous conversion due to lack of pins. Therefore, conversion efficiency is approximately 5% to 10% lower than equivalent synchronous systems.

Note 4: Bootstrap boost using internal switching (Mode 4) has very low efficiency due to the higher relative impedance of the switching FETs, so this mode should be used only if energy efficiency is not important.

DACLevel	DAC8	DAC voltage	VDD/VBAK	DACLevel	DAC8	DAC voltage	VDD/VBAK
0	106	0.66	1.99	8	150	0.93	2.80
1	111	0.69	2.08	9	156	0.97	2.91
2	117	0.73	2.19	10	161	1.00	3.00
3	122	0.76	2.28	11	167	1.04	3.11
4	128	0.80	2.39	12	183	1.14	3.41
5	133	0.83	2.49	13	200	1.24	3.72
6	139	0.86	2.56	14	222	1.38	4.13
7	144	0.89	2.69	15	250	1.55	4.65

DAC Voltage = [1.57 * (DAC8 code / 255) + 0.01] ± 1%

Functional Descriptions *(continued)*

Low Dropout Linear Regulator (LDO)

The LDO function provides low-dropout linear regulation from VDD to the PWM pin. All other PWM pin related functions are disabled in this mode.

The LDO is intended as a low-power support feature for simple low-cost applications. It has good VDD high frequency noise rejection so can be used to clean up a VDD supply.

The output voltage on PWM is determined by the *DACLevel* setting as per the previous table. The voltage on PWM is divided by three and regulated to the same voltage as the DAC8.

Note: Only DAC levels of 1V and above are valid in this mode.

There is also a feature to allow the DAC8 to be used for an ADC conversion while the LDO is active. To do this, the *MaintainRegulatorOp* bit in the *Config* register should be set prior to initiating a conversion. This disconnects the LDO regulator input from the DAC8 and holds the reference level on a capacitor while the DAC8 is used for the conversion. When the conversion is complete, the DAC8 is reset to the correct level and reconnected to the LDO. Due to internal leakage, it is recommended that the maximum disconnect period is kept to 1ms or less.

These LDO specifications assume a 1µF ceramic load capacitor on PWM:

Parameter	Symbol	Min	Max	Units
VDD input voltage	VDD	3.1	5.5	V
PWM output voltage	VLDO	3	4.5	V
No load standby current	Idd		250	µA
Line regulation	REGlin		10	mV/V
Load regulation	REGload		2	mV/mA
VDD noise rejection (100 kHz square wave on VDD, >250 mV headroom)	PSRR	30		dB
Max load current (VLDO = 3 V)	Iload1	10		mA
Max load current (VLDO = 4.5 V)	Iload2	15		mA
Dropout at 10 mA load (50 mV headroom)	Vdo		200	mV
PWM Drift (DAC8 disconnected)	Vdrift		300	mV/ms
10 Hz to 100 kHz RMS output noise	Ntot		100	µV

Functional Descriptions *(continued)*

I²C Interface

The I²C interface conforms to the 400kHz fast-mode of the 2000 Philips I²C specification, acting as a slave only. Both SCL and SDA pins are dedicated. The maximum frequency of the I²C interface is determined by the strength of the external pull-up on SCL and SDA, and there is no minimum frequency.

The seven-bit I²C Slave Address is 0100xxx, and the three LSBs are programmed into the register. Both read and ite protocols can use the I²C combined format, and additionally, the write protocol can support the non-combined ('normal') format.

Combined Write Format

• Start condition (falling edge on SDA while SCL is high) to commence the access to write the register address to the SH3100

- 7-bit slave address on SDA, clocked in by SCL 1-bit read/write indicator, set low because the following 8 bits are the register address, written into the SH3100
- SH3100 generates ACK pulse to acknowledge slave address
- 8-bit register address
- SH3100 generates ACK pulse to confirm register address transfer
- Restart condition to commence the access to write payload data to the register address set up by the last access
- 7-bit slave address
- 1 bit read/write indicator, set low because the following 8 bits are the write data (payload)
- SH3100 generates ACK pulse to acknowledge slave address
- The microcontroller generates 8-bit write data
- SH3100 generates an ACK pulse, and may stretch SCL by holding it low for up to two periods of CLK0, if CLK0 is relatively slow compared to SCL
- Stop condition (rising edge on SDA while SCL is high)

Normal Write Format

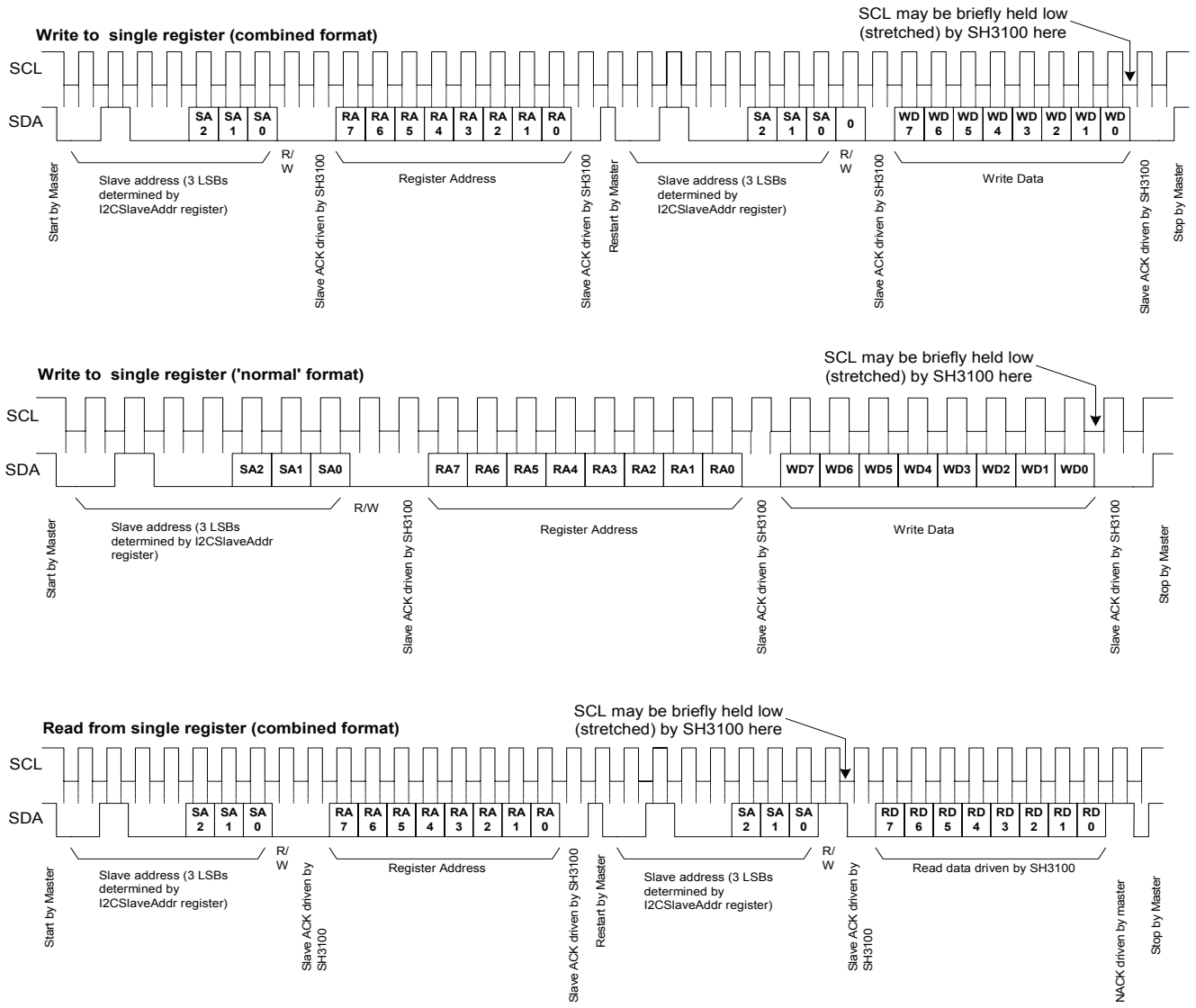
- Start condition (falling edge on SDA while SCL is high) to commence the access to write the register address to the SH3100
- 7-bit slave address on SDA, clocked in by SCL
- 1-bit read/write indicator, set low because the following 8 bits are the register address, written into the SH3100
- SH3100 generates ACK pulse to acknowledge slave address
- 8-bit register address
- SH3100 generates ACK pulse to confirm register address transfer
- The microcontroller generates 8-bit write data
- SH3100 generates an ACK pulse, and may stretch SCL by holding it low for up to two periods of CLK0, if CLK0 is relatively slow compared to SCL
- Stop condition (rising edge on SDA while SCL is high)

Functional Descriptions *(continued)*

Combined Read Format

- Start condition (falling edge on SDA while SCL is high) to commence the access to the register address to the SH3100
- 7-bit slave address on SDA, clocked in by SCL
- 1-bit read/write indicator, set low because the following 8 bits are the register address, written into the SH3100
- SH3100 generates ACK pulse to acknowledge slave address
- 8-bit register address
- SH3100 generates ACK pulse to confirm register address transfer
- Restart condition to commence the access to read from the register address set up by the last access
- 7-bit slave address
- 1-bit read/write indicator, set high because the following 8 bits are the read data (payload)
- SH3100 generates ACK pulse to acknowledge slave address, and may stretch SCL by holding it low for up to 62 µs if reading the LSB of the RTC or PIT registers
- SH3100 generates 8-bit read data
- The microcontroller can generate either an ACK or NACK pulse – this is ignored by SH3100
- Stop condition (rising edge on SDA while SCL is high)

Note: If the I^2C master (microcontroller) does not support SCL stretching, and can not be modified to do so, then the RTC subseconds register (address 0x11) and the PIT LSB (address 0x09) may be read incorrectly. All other reads and writes succeed, provided CLK0 is running reasonably fast compared to SCL, i.e. CLK0 frequency is >= 4xSCL frequency.



SDA and SCL are driven by the Master unless otherwise specified.

SAn = Slave Address (bit n)
RAn = Register Address (bit n)
WDn = Write Data (bit n)
RDn = Read Data (bit n)

I²C Timing Diagrams

Functional Descriptions *(continued)*

High-Frequency Digitally-Controlled Oscillator (HFDCO)

The master HF oscillator is a 19-bit high-frequency digitally-controlled oscillator (HFDCO) which can either free-run or be controlled within a Frequency Locked Loop (FLL) locked to the 32.768kHz crystal clock.

The HFDCO is guaranteed to operate over the range 8MHz to 33.5MHz with approximately 2 kHz resolution.

When free-running, the frequency stays stable to within ±0.5% over 0ºC to 70ºC and within ±1% over -40ºC to +85ºC. When FLL locks to the crystal, the frequency has the same stability as the crystal.

On a programmed device, the start-up code for the HFDCO is programmed into the register at 25°C.

This means that if the chip initially powers up at 25°C, the oscillator frequency is within ±0.1% of the desired frequency. If the temperature is not at 25°C on power up, then the frequency is within ±1% of the desired frequency. Once the FLL starts (assuming the crystal is present) the oscillator is pulled exactly into lock. If the chip is then placed into standby mode at any particular temperature, the oscillator stops, but the control code determined by the FLL is maintained, such that if the oscillator is then started up at the same temperature, the accuracy is within ±0.1% of the desired frequency.

Note 1: If there is no crystal present, the FLL is not automatically enabled, as there is no point in locking to the internal 32.768kHz oscillator, since the HFDCO free-running accuracy is higher than that of the internal oscillator.

Note 2: Due to process variations, there is no fixed correlation between control code and frequency therefore the start-up code is determined on test and uniquely programmed in to the registers for each device.

In order to achieve a frequency resolution of 2kHz over the required range, a linear DCO would require approximately 14 bits of adjustment resolution. To achieve this with a single linear monotonic system is impractical due to component mismatch, therefore an intentionally non-monotonic system is used. This is made up from a number of overlapping frequency banks such that it is guaranteed that every frequency between 8MHz and 33.5MHz can be achieved. This results in a net 19-bit control code, of which the 16 bits stored in the register are sufficient for start-up programming.

There is sufficient bank overlap built into the system to ensure that while the FLL is running, drift in the control code due to temperature variations does not result in the code rolling over a bank boundary and thus requiring a large delay while the FLL loop recovers from the bank rollover. There is also additional protection built in such that if a range rollover point is reached, then the controlling logic detects this and jumps the LSB bank code to the appropriate point to give the theoretically correct frequency for the next bank. In practice, due to component mismatch, the new frequency may not be exactly correct, and the FLL would need a few more cycles to settle to the correct point.

Functional Descriptions *(continued)*

Spectrum Spreading

One other function of the HFDCO is that it has the ability to implement frequency spreading of the HF clock in order to reduce EMI radiation. This is achieved by modulating the LSB bank of the HFDCO using a pseudo random counter clocked at 32.768kHz. Spread spectrum is enabled by setting the *SSEnable* bit and choosing a modulation amplitude of 16kHz, 32kHz , 64kHz, or 128kHz depending on the setting of the 2-bit SS Config register.

Parameter	Min	Typ	Max	Units
Minimum programmable frequency	5		8	MHz
Maximum programmable frequency	33.5		45	MHz
Frequency resolution	1.5	2	2.5	kHz
Free-running accuracy over 0°C to +70°C	-0.5		+0.5	%
Free-running accuracy over -40°C to +85°C	-1		+1	%
Free-running accuracy over VDD	-0.1		+0.1	%
Short term frequency stability (jitter)		0.1	0.2	%
Startup time from standby			2	µs
Settling time to 0.1% after HFDCO code			10	µs
Clock duty cycle	40	50	60	%
Spread spectrum modulation (min. code)	± 12	± 16	± 20	kHz
Spread spectrum modulation (max. code)	± 96	± 128	± 160	kHz

Clock Management & Frequency Locked Loop (FLL)

FLL Operation

The HFDCO is used as the master high frequency clock source on the SH3100. Since this is a free running oscillator with a process dependent correlation between control code and frequency, it is necessary to employ a frequency locked loop (FLL) to generate an output clock which is a set multiple of the crystal reference. In operation, the 32.768kHz crystal clock is divided by 16 to yield an accurate 2048Hz reference. The HFDCO clock cycles are counted over the duration of one reference cycle and compared against the 14-bit FLLDivRatio register to assess whether the HFDCO is running faster or slower than required. The 19-bit HFDCO code is then incremented or decremented accordingly. The exact relationship is:

HFDCO Frequency = 2048Hz x (FLLDivRatio + 1)

The frequency select register (FLLDivRatio) is loaded from its register on power up but can be overwritten by I^2C access.

On power-up, the FLL automatically starts once the crystal oscillator is stable. If no crystal is present, then the FLL does not automatically start, but may be initialized by setting the *FLLEnable* bit of the *FLLConfig* register. In this case, since the crystal is not present, the FLL locks to the internal 32.768kHz oscillator, but since this has an intrinsic free-running accuracy of ±3%, this would result in less accuracy than the intrinsic ±0.5% free-running accuracy of the HFDCO. The only reason for doing this would be to find the approximate HFDCO code for a new frequency in the absence of an accurate crystal reference.

On a programmed device, the HFDCO starts up within ±0.5% of the desired frequency and the FLL then pulls the frequency smoothly into lock.

Fast FLL Lock

On an unprogrammed device, or if a new FLL frequency setting has been programmed into the *FLLDivRatio* register, the FLL can perform a fast locking algorithm using a successive approximation technique. This is initiated by setting the Initiate *FLLCoarseFreqLock* bit of the *FLLConfig* register. Once locked, the HFDCO control code may then be stored for future reference by the system or in the case of an unprogrammed device, it can be stored in the register as the default startup code for the HFDCO.

Note: FLL fast lock causes temporary coarse frequency excursions for approximately 25ms until the frequency is locked. To avoid exposing the microcontroller to these frequency excursions, the locking procedure can be performed while CLKO is programmed for 32.768kHz by setting the ForceDCOOn bit of the Config register.

Fine frequency acquisition can also be initiated with the *InitiateFineFreqLock* bit of the *FLLConfig* register. This performs successive approximation on only the LSB bank of the HFDCO, so it can be used to give a smoother rapid lock for smaller frequency deviations, such as those caused by a large temperature change during a shutdown period when the HFDCO and FLL are disabled.

If the spread spectrum function is enabled, it is temporarily disabled while Coarse or Fine lock are in process, and is re-enabled once FLL lock is achieved.

The HFDCO code is directly accessible for read and write by the I^2C interface. With the FLL disabled, a microcontroller could perform its own locking algorithm if desired.

The state of the FLL can be determined by reading the status register. The *FLLLocked* bit is set when the FLL is locked. This is once the FLL has been stable for three consecutive measurement cycles (i.e., no more than three frequency adjustments in the same direction over three consecutive reference cycles).

Note: The *FLLLocked* indicator is invalid if the spread spectrum function is enabled.

Functional Descriptions *(continued)*

CLK0 & CLK1 Outputs

Once the HFDCO frequency has been set to between 8 MHz and 33.5MHz, it can be driven out on CLK0 and CLK1 via independent postscalers.

The CLK0 postscaler is 3 bits and allows division ratios between 1 and 128 in binary geometric progression. This allows output frequencies between 62.5kHz and 33.5MHz with between 250ppm and 60ppm resolution.

The CLK1 postscaler is 4 bits and allows division ratios between 1 and 32768 in binary geometric progression. This allows output frequencies between 244Hz and 33.5MHz with between 250ppm and 60ppm resolution.

CLK0 is treated as the master clock and would usually be used as the main clock source to the microcontroller. CLK1 is the secondary clock and may be used for any purpose.

Both CLK0 and CLK1 may also be set to use the internal 32.768kHz clock source. This allows a clock output to be maintained while the HFDCO is shutdown or during battery backup.

Both CLK0 and CLK1 output pads may be powered from either VDD or VBAK in normal operation. If CLK1 is set to use the internal 32.768kHz clock source, then the supply automatically switches over to VBAK during battery backup. If it is set to a HFDCO derived frequency, then it stops. CLK0 is always stopped during battery backup.

If spread spectrum is enabled, then the percentage of frequency spreading remains constant, as the native HFDCO frequency is divided down by the postcaler.

HFDCO Clock On/Off Control

The HFDCO automatically starts up at the programmed rate after power-up. It may then be turned off and on by I²C access or by CLKIN control. To use CLKIN for On/Off control, activity needs to be detected on CLKIN after the clock output starts on CLK0. This places the SH3100 into ***AutoClkDetect*** mode which turns off the clock once it detects that four consecutive cycles of CLKIN are missing. In this mode, the clock is restarted within 2µs once a single transition is detected on CLKIN.

The advantage of CLKIN clock control is that it is much faster than I²C access and it fits well with the clock STOP facility of many microcontrollers which use internal gating to disable their own crystal oscillators. In this case CLK0 should be connected to the microcontroller XIN and CLKIN to the XOUT.

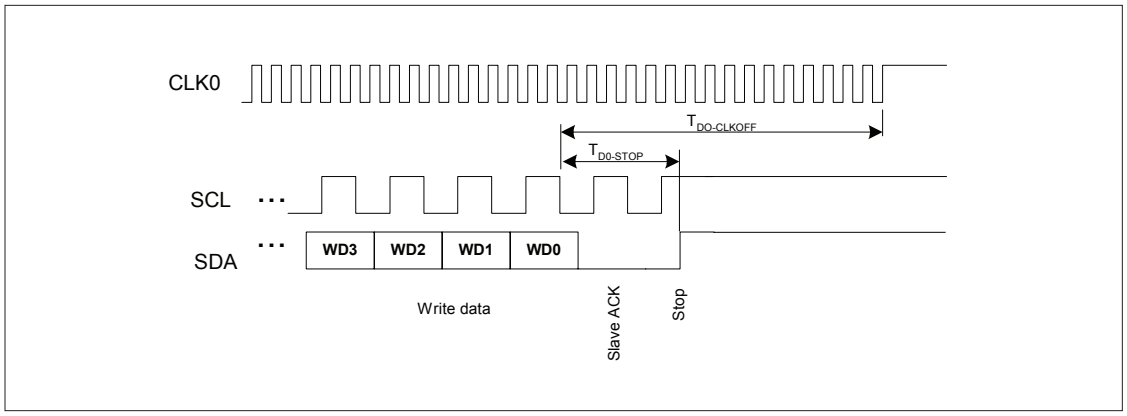
In *AutoClkDetect* mode, CLK0 is stopped at the same polarity as CLKIN. This allows for microcontroller implementations where the microcontroller XOUT is disabled using either a NAND or a NOR gate. To maintain CLK0 active, CLKIN must be synchronous with CLK0, but phase is not important. In non-AutoClkDetect mode, CLK0 is stopped in the High state.

The SH3100 defaults to non-*AutoClkDetect* mode until activity has been sensed on CLKIN. When not in *AutoClkDetect* mode, CLK0 can be disabled by clearing the *ClkEn* bit of the *Config* register, but only once at least one interrupt source has been programmed. This is a protection mechanism to prevent the microcontroller from killing its own clock without setting up the Interrupt with which it can be restarted. CLK0 restarts when the Interrupt event occurs.

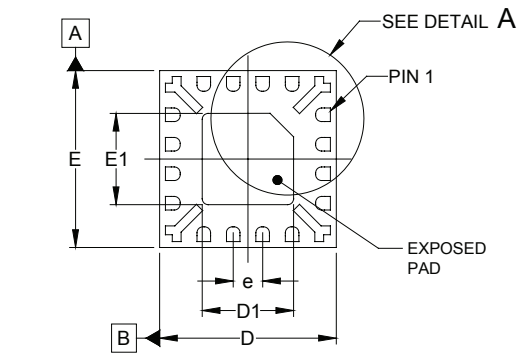
AutoClkDetect mode is disabled on reset, and remains so until activity is first seen on CLKIN. When not in *AutoClkDetect* mode, the write access to the *CLK0Config* register (which disables the clock) must adhere to the following timing constraint:

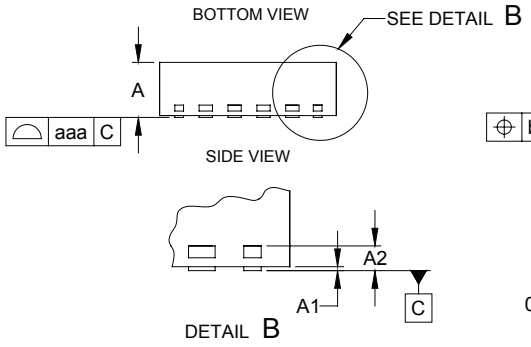
> The time TDO-STOP from the falling edge of SCL clocking in the last data bit D0 to the rising edge of SDA marking the I²C STOP condition must not exceed (1024*CLK0 periods) or (4*SCL periods), whichever is less.

CLK0 is stopped TDO-CLKOFF following the falling edge of SCL clocking in the last data bit D0. This time equates to 4*SCL periods or 1024*CLK0, whichever is less.

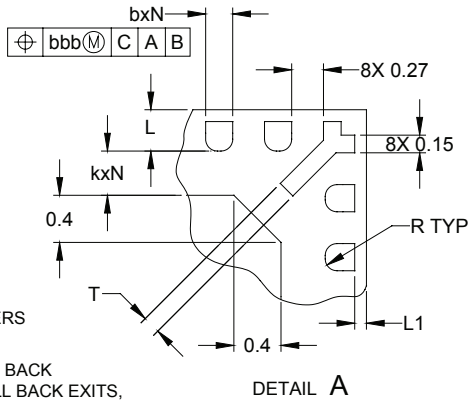


Outline Drawing - MLP 3 x 3 mm 16 pins





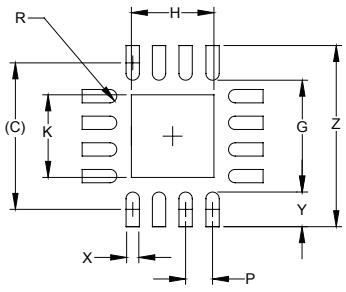
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.040	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
D	.114	.118	.122	2.90	3.00	3.10
D1	.055	.061	.065	1.40	1.55	1.65
E	.114	.118	.122	2.90	3.00	3.10
E1	.055	.061	.065	1.40	1.55	1.65
L	.012	.014	.016	0.30	0.35	0.40
L1	-	-	.004	-	-	0.10
b	.007	.009	.012	0.18	0.23	0.30
N	16			16		
e	.020 BSC			0.50 BSC		
k	.008	-	-	0.20	-	-
R	.004			0.09		
T	-	.006	-	-	0.15	-
aaa	.003			0.08		
bbb	.004			0.10		



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSION "L1" REPRESENTS TERMINAL PULL BACK FROM PACKAGE EDGE. WHERE TERMINAL PULL BACK EXITS, ONLY UPPER HALF OF LEAD IS VISIBLE ON PACKAGE EDGE DUE TO HALF ETCHING OF LEADFRAME.
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern - MLP 3 x 3 mm 16 pins



DIM	INCHES	MILLIMETERS
C	(.108)	(2.75)
G	.083	2.10
H	.065	1.65
K	.065	1.65
R	.005	0.12
P	.020	0.50
X	.010	0.25
Y	.026	0.65
Z	.134	3.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. DO NOT PLACE VIAS BETWEEN THE CORNER LEADS INSIDE THE 3X3MM PACKAGE FOOTPRINT.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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