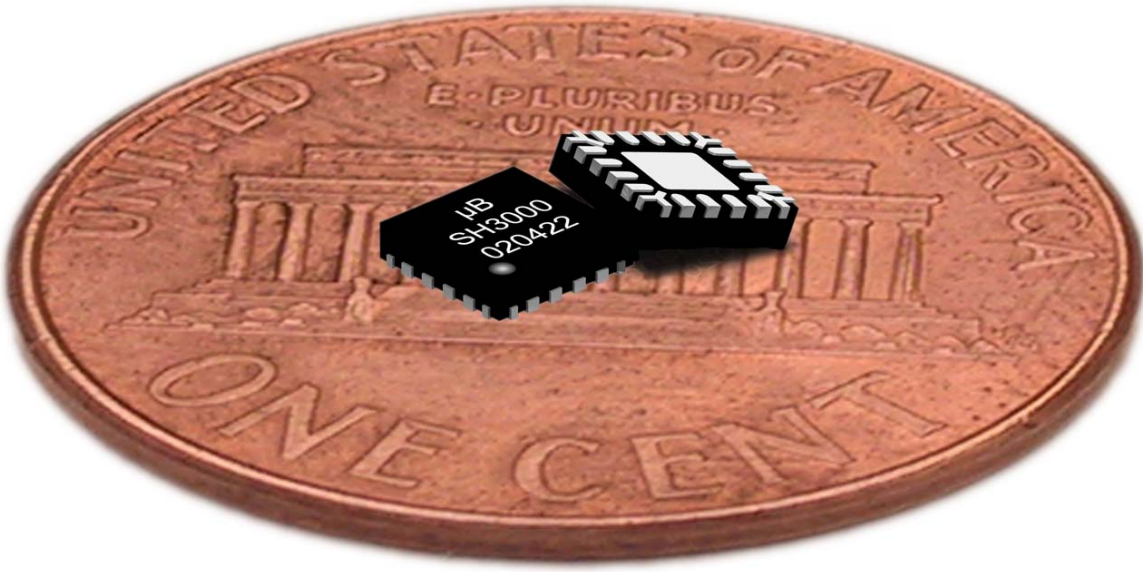
SEMTECH

SH3000 User Manual

Using the SH3000 MicroBuddy™



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Document Revision History

Revision	Date	Reason for Changes
Rev. 0.95	2002-08-09	Preliminary draft

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1. Introduction

The programmable SH3000 MicroBuddy™ (µBuddy™) provides all mandatory microcontroller support functions:

- CPU Supervisor
- Clock Management System
- Real-Time Support
- Auxiliary functions

Three components make a complete system: any microcontroller, the SH3000, and a bypass capacitor. This low-cost system would consume very little power and have clock-frequency accuracy of ±0.5%. A fourth component, a 32.768 kHz watch crystal, raises the clock frequency accuracy to ± 0.0256% (± 256 ppm).

The SH3000 can operate completely stand-alone, or under control of the microcontroller. A single-wire interface handles both bi-directional communications and the interrupt / wake-up signal from the SH3000. The SH3000 stores all configuration, calibration, parameters, and status information in a 36-byte bank of control registers. On reset, most of these are reloaded with defaults from the factory-set One-Time-Programmable (OTP) memory. The microcontroller can change any settings on the fly. If some of the settings must remain fixed, a comprehensive set of write-protect bits is provided for several related groups of registers (with both permanent write-inhibit and lock/unlock capabilities).

A backup power source may also be connected to the SH3000. The IC can directly accommodate 2/3-cell zinc-carbon/alkaline, 2/3-cell mercury, 2/3/4-cell NiCd/NiMH, 1-cell Li/Li+ batteries, or a super cap.

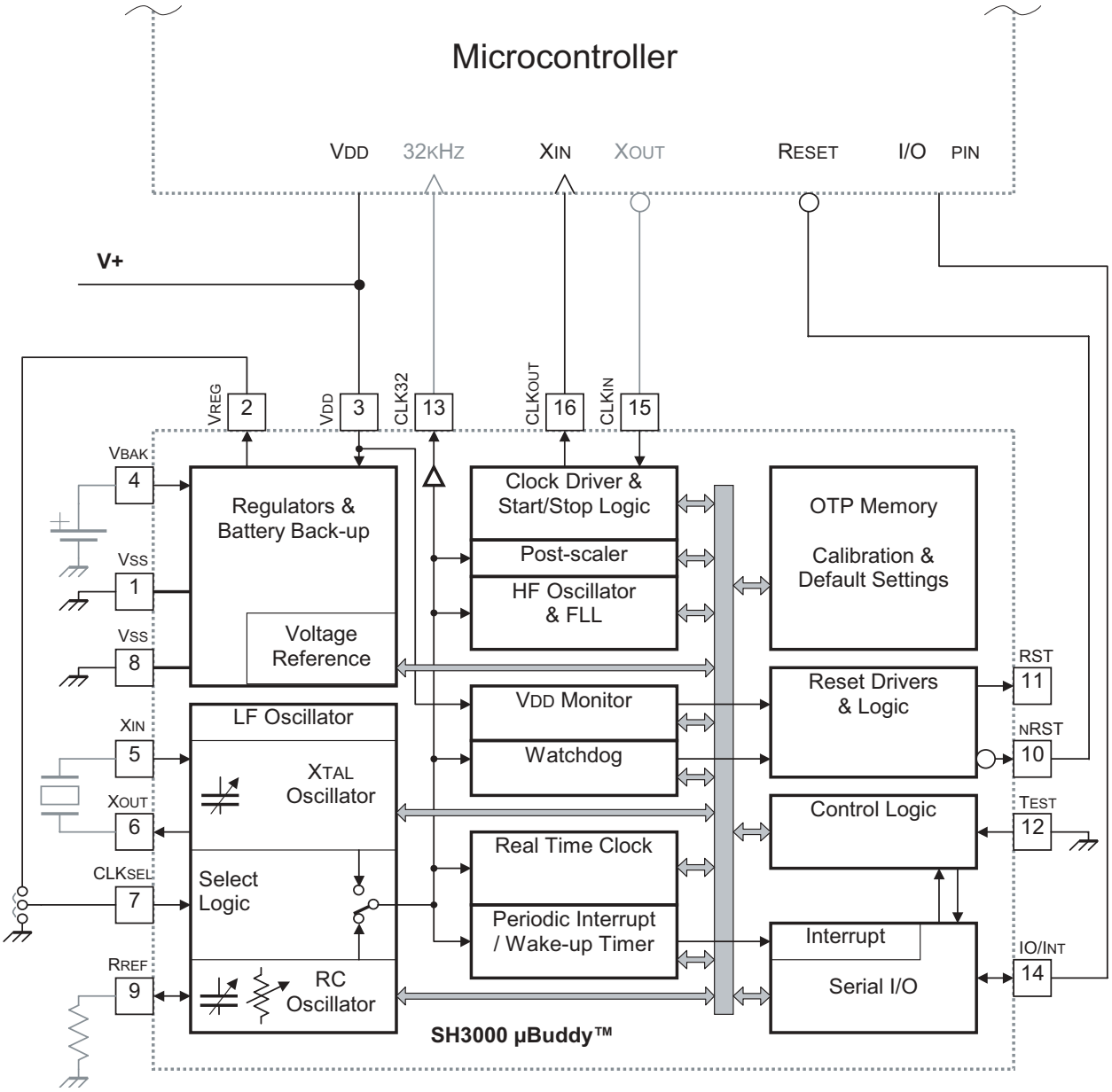

Figure 1: SH3000 MicroBuddy™ Block Diagram

Table 1: SH3000 MicroBuddy™ Pin Descriptions

Pin	Name	Type	Function
1	**VSS**	Power	Ground, 0 V. All **VSS** pins and **TEST (VSS)** pin must be connected together.
2	**VREG**	Power	Output of internal voltage regulator, 2.2 V nominal. This pin can power external loads of <5 mA. If load is "noisy," it requires a bypass capacitor. May be left unconnected or used as a high logic level signal for **CLKSEL** pin (see below).
3	**VDD**	Power	Main power supply, +2.3 to +5.5 V.
4	**VBAK**	Power	Backup power supply for real-time clock, +2.3 to +5.5 V (+1.8 to +5.5 V typical). This voltage can be higher or lower than **VDD**. Connect a backup battery or backup capacitor (with external recharge circuit). Connect to **VDD** if not used.
5	**XIN**	Analog In	Oscillator pins for an optional external low-frequency crystal, typically a 32.768 kHz watch crystal with nominal 12.5 pF load capacitance. Keep open or connect to **VSS** if not used.
6	**XOUT**	Analog Out	
7	**CLKSEL**	Digital In	A logic low level selects the internal 32 kHz RC oscillator (**CLKSEL** tied to **VSS**). A high state on this pin selects the 32 kHz crystal oscillator (**CLKSEL** is connected to **VREG**). The SH3000 always starts up using the internal 32 kHz RC oscillator. If **CLKSEL** is high, the internal 32 kHz clock switches to the crystal oscillator once it has stabilized, and RC oscillator is disabled for power conservation. Do not connect **CLKSEL** to any signals except **VSS** or **VREG**. **CLKSEL** must not be left open.
8	**VSS**	Power	Ground, 0 V. All **VSS** pins and **TEST (VSS)** pin must be connected together.
9	**RREF**	Analog	Optional 1 MOhm external bias resistor for the internal 32 kHz RC oscillator. Can be used to set, trim or modulate the internal RC oscillator. Keep open if not used.
10	**NRST**	Digital Out	Active low system reset output. Asserted with a strong low state when a reset condition occurs. Weakly pulled to **VDD** internally when not active. This signal is valid for **VDD** as low as 1 V. Keep open if not used.
11	**RST**	Digital Out	Active high system reset output. Asserted with a strong high state when a reset condition occurs. Weakly pulled to **VSS** internally when not active. This signal is valid for **VDD** as low as 1 V. Keep open if not used.
12	**TEST (VSS)**	Digital In	Factory test enable. All **VSS** pins and **TEST (VSS)** pin must be connected together.
13	**CLK32**	Digital Out	Buffered internal 32 kHz clock, derived according to the **CLKSEL** pin setting. This pin uses backup power for the buffer when **VDD** is not present. When driving high, this signal is either at **VBAK** or **VDD** (if **VDD** is higher than the reset threshold). When enabled, this signal runs continuously independent of **CLKOUT** activity. Minimize the external load to reduce power consumption during backup operations. When disabled, this pin is driven to **VSS**. Keep open if not used.
14	**IO/INT**	I/O	Serial communications interface and interrupt output pin. This pin is internally weakly pulled to the opposite of the programmed interrupt polarity. For example, if interrupt is programmed to be active low, this pin is weakly pulled to **VDD** when inactive. Keep open if not used.
15	**CLKIN**	Digital In	Clock activity sense input. Used to detect when the target microcontroller enters stop mode (which disables its clock). Connect to the microcontroller's clock output or oscillator output pin. Connect to **VSS** when not used. **CLKIN** must not be left open.
16	**CLKOUT**	Digital Out	Programmable high-frequency clock output. Connect to the target microcontroller's clock input or oscillator input pin. Keep open if not used.

2. CPU Supervisor

The SH3000 has two CPU Supervisor functions that manage the reset of the host microcontroller, a low-**VDD** monitor (brownout detector) and a watchdog timer (see **Figure 2)**.

Both functions are integrated with the Clock Management System to provide a more complete system solution than stand-alone components.

The SH3000 has both active high and active low reset output pins. Both are driven strong in the active state, and weak in the inactive state. This eliminates the need for external pull-ups and allows various reset sources to be connected together in a wire-OR configuration. (this makes it simple to set up a manual rest circuit.)

A set of flags in the **ResetEvent** register (R0x1B) indicates the source of the reset to the system software.

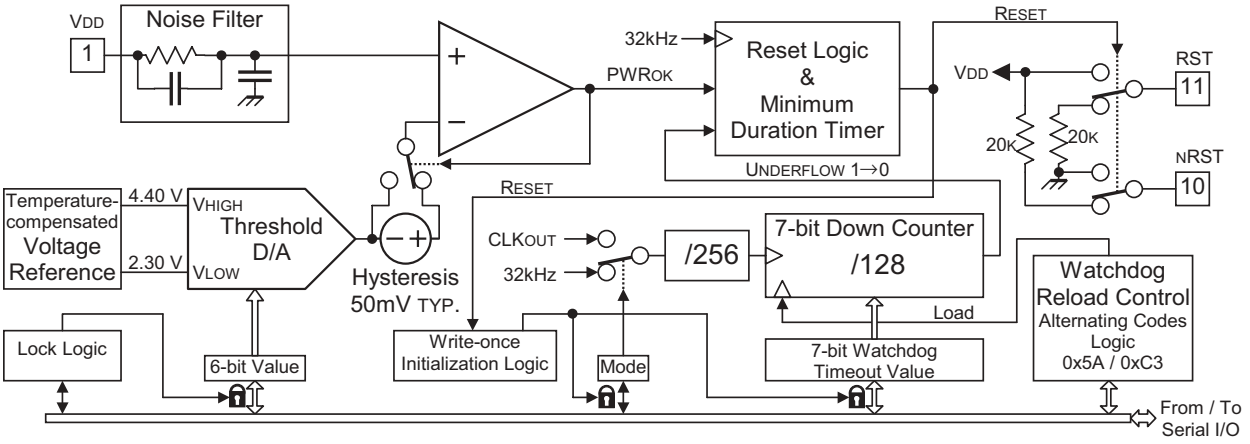

Figure 2: CPU Supervisor

2.1 Low V_{DD} Reset

The SH3000 drives the reset pins active whenever **V_{DD}** is below the value of **V_{BO}**, the brownout reset threshold. **V_{BO}** can be set using bits 0:5 of the **V_{BO}Value** register (R0x10). **V_{BO}** can be set to a value from 2.30 V to 4.40 V in average increments of 33.33 mV–see **Table 2.**

Table 2: Programmable **V_{BO}** Values (Volts)

4.400	4.367	4.333	4.300	4.267	4.233	4.200	4.167
4.133	4.100	4.067	4.033	4.000	3.967	3.933	3.900
3.867	3.833	3.800	3.767	3.733	3.700	3.667	3.633
3.600	3.567	3.533	3.500	3.467	3.433	3.400	3.367
3.333	3.300	3.267	3.233	3.200	3.167	3.133	3.100
3.067	3.033	3.000	2.967	2.933	2.900	2.867	2.833
2.800	2.767	2.733	2.700	2.667	2.633	2.600	2.567
2.533	2.500	2.467	2.433	2.400	2.367	2.333	2.300

The default **V_{BO}** value is loaded on power-up from the factory-programmed OTP nonvolatile memory. It can be re-programmed at any time or it can be permanently protected from any changes by setting the **V_{BO}** lock flag or an OTP write-protect flag.

On power up, both the active high and active low reset pins are driven active. These outputs are typically valid for a **V_{DD}** level of at least 0.5 V, and guaranteed to be valid for a **V_{DD}** level of 1.0 V.

The reset output pins remain active until **V_{DD}** rises and stays above the level of **V_{BO}** + **V_{HYST}**, where **V_{HYST}** is a small fixed amount of hysteresis, nominally 50 mV. This hysteresis is added to prevent false triggering from noise or small power glitches.

At the threshold level (**V_{BO}** + **V_{HYST}**), the power supply is considered valid. On initial power up, the reset lines become inactive 3–5 ms after power is valid. In the case of brownout, the reset is released after a delay of 6 ms, but no less than 12 ms from the moment brownout has been detected.

Such a fast reset is possible because the SH3000 provides a fast-starting clock that is free of crystal start-up time delays. This gives the SH3000 an advantage over other external reset circuits, which must have a long reset pulse duration to accommodate long and unpredictable crystal start-up times.

The SH3000 guarantees that before the reset signals are inactive a valid and stable clock is available for at least 1 ms on power up, or 2 ms after brownout, so that internal synchronous reset and initialization of the host microcontroller can proceed normally.

With the clock becoming active 1-2 ms before the reset lines become inactive, considerable energy is conserved since the clock is not active during the whole reset period.

When a brownout event occurs, the SH3000 continues to provide the clock to the host microcontroller, but at a reduced frequency between 500 kHz and 1.0 MHz. After a delay of 2 ms this clock is stopped, automatically lowering the energy consumption of the whole system; see **Figure 3**.

A noise filter prevents the reset lines from going active due to noise and power glitches on the **VDD** line. **Figure 4** shows typical behavior for the **VDD** level just above **VBO** for negative-going spikes of various duration and amplitude.

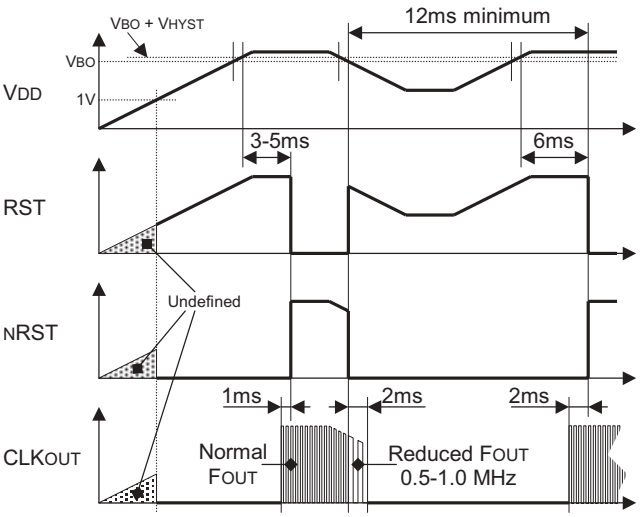

Figure 3: Operation of Low VDD / Brownout Detector

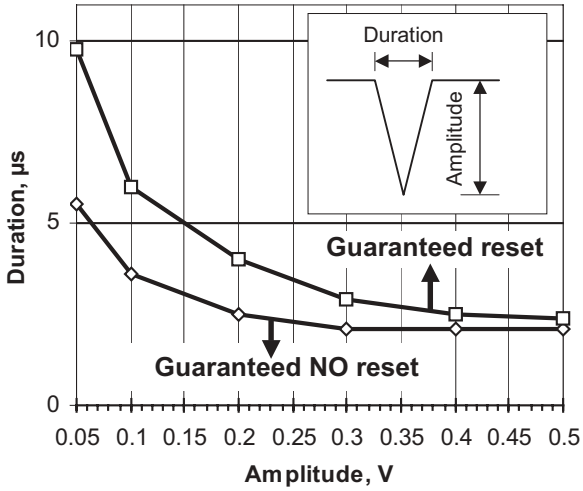

Figure 4: Noise Filtering

When **VDD** power is removed from the chip, the following sequence of events occurs:

1. When **VDD** drops below the programmed reset threshold, **NRST** and **RST** are asserted. Both reset lines are guaranteed to become active within 5 µs after **VDD** has crossed the **VBO** threshold.

2. If **VBATT** is above 1.5 V to 2.2 V, then the chip switches on to **VBATT** operation; **NRST** and **RST** remain asserted

3. **CLKOUT** continues to run at a reduced rate (500 kHz to 1 MHz), provided that **VDD** stays above approximately 2.25 V. If **VDD** falls below this threshold at any time, then **CLKOUT** is stopped immediately. If **CLKOUT** was inactive when the reset condition occurred, it is activated at this time.

4. If enabled, the **CLK32** output continues normal operations when **VDD** is absent and backup power is available.

5. 2 ms after **VDD** drops below the **VBO** threshold, **CLKOUT** switches off.

The four bit flags 0:3 (Power-on reset, watchdog code violation, watchdog timeout, and brownout) in the **ResetEvent** register (R0x1B) reflect reset history. This register is readable, and may be cleared individually by writing a “1” to the relevant bit position; they are not cleared automatically. On a power-on reset (bit 0), the brownout flag (bit 3) is invariably set also.

2.2 Watchdog Timer

The Watchdog Timer is part of the CPU Supervisor function of the SH3000. Whereas the low-**VDD** Brownout Detector monitors supply voltage, the watchdog timer monitors behavior of the host microcontroller. It is based on a programmable timer that must be restarted periodically by the host. If the host does not send a command to restart the timer (which is likely when the host firmware has hung or failed), the watchdog resets the host.

The watchdog is disabled after reset occurs. It stays disabled until initialized by the host microcontroller. The initialization requires the watchdog clock mode to be selected (see **Figure 2**) and the 7-bit time-out value to be set. Once the time-out value is written, the watchdog begins operations and cannot be stopped; the time-out value and clock source can no longer be changed.

The two clock sources available for the watchdog are the internal 32 kHz clock and the **CLKOUT** signal.

The time-out interval can be set with bits 0:6 of the **WdogPeriod** register (R0x1D). When operating from the 32 kHz source, the time-out interval is programmable from 7.8125 ms to 1000 ms with a resolution of 7.8125 ms. Since the internal 32 kHz clock is running all the time, the time-out period is fixed and predictable.

When operating from the **CLKOUT** signal, the time-out period is programmable between 256 and 32768 cycles with a resolution of 256 cycles. The actual time-out duration is variable; it depends both on the frequency of **CLKOUT** and the amount of time the host microcontroller spends in the STOP mode, when the **CLKOUT** signal is also stopped. When the **CLKOUT** signal is stopped, the watchdog is suspended.

These two clock modes, together with the programmable time-out value, allow the SH3000 exceptional flexibility previously unattainable by discrete watchdog solutions.

The watchdog timer is kept from timing out by periodic writing of a code to the **WdogCode** register (R0x1C). As a safety measure, the code values must be alternated between 0x5A and 0xC3. The first code written to the register must be 0x5A; at the next period, the code 0xC3 must be used, and so forth. The timer is reloaded after every write of the correct one of these codes.

If the watchdog code is not written before the time-out period expires, or if the code is incorrect or out of sequence, the SH3000 issues a reset to the microcontroller by asserting both the **RST** (pin 11) and **nRST** (pin 10) lines. The reset state is asserted for 6 ms.

2.3 CPU Supervisor Registers

ADDRESS	NAME	RESET EVENT			RESET VALUE		DESCRIPTION	
		PowerOn	WDog	BrownOut	HEX	BINARY		
0x0E	Config	P			0x88	1	b7	**XTALtune Rewrite-Once Enable** (see notes for use)
		P	W	B		0	b6	Register Page for R0x10 through R0x17. 0 =Page0, 1 =Page1.
		P	W	B		0	b5	ForceDCOon. Forces HF Oscillator to run under all conditions.
		P	W	B		0	b4	CLKOUT source. 1 = 32 kHz, 0 = HFCLK.
		P	W	B		1	b3	CLKOUTEnable. 1 = enable, 0 = disable.
		P	W	B		0	b2	WdogClkSelect. 1 = CLKOUT, 0 = 32 kHz.
		P	W	B		0	b1	Interrupt Flag Clear. 1 = clear, 0 = no effect, always reads 0.
		P	W	B		0	b0	Interrupt Enable. 1 = enable, 0 = disable.

ADDRESS	PAGE	NAME	INIT EVENT			INIT VALUE		WRITE PROTECT				Xtal REWRITE-once	DESCRIPTION	
			PowerOn	WDog	BrownOut	HEX	BINARY	IDCode	Calibration	Application	VBOValue			
0x10	0	VBOValue				0x??	-0-						b7	Reserved, not used
							-0-						b6	Reserved, not used
			P	W			?				V		b5	VBO Threshold Value, 2.3 V to 4.4 V in ~33.33 mV steps.
			P	W			?				V		b4	
			P	W			?				V		b3	
			P	W			?				V		b2	
			P	W			?				V		b1	
			P	W			?				V		b0	
0x17	0	WP_PostScale	P	W		0x??	?						b7	IDCode Write Protect, 1 = no writes.
			P	W			?						b6	Calibration Write Protect, 1 = no writes.
			P	W			?						b5	Application Write Protect, 1 = no writes.
			P	W			?						b4	VBO Value Write Protect, 1 = no writes.
			P	W	B		?			A			b3	CLK32 enable, 1 = enable, 0 = disable.
			P	W	B		?			A			b2	DCO Post-Scaler, 8 (eight) setting: **/1, 2, 4, 8, 16, 32, 64, 128**.
			P	W	B		?			A			b1	
			P	W	B		?			A			b0	

Note: The four bit flags 0:3 (Power-on reset, watchdog code violation, watchdog timeout, and brownout) in the **ResetEvent** register (R0x1B) reflect reset history. This register is readable, and may be cleared individually by writing a "1" to the relevant bit position; they are not cleared automatically. On a power-on reset (bit 0), the brownout flag (bit 3) is invariably set also.

ADDRESS	NAME	RESET EVENT			RESET VALUE			DESCRIPTION
		PowerOn	WDog	BrownOut	HEX	BINARY		
0x1B	**ResetEvent**				0x02 0x04 0x08 or 0x09	-0-	b7	Reserved, not used
						-0-	b6	
						-0-	b5	
						-0-	b4	
		P		**B**		0/1	b3	V_{DD} dropped below V_{BO} threshold (brown-out).
			W			0/1	b2	Watchdog code violation caused the reset.
			W			0/1	b1	Watchdog timeout caused the reset.
		P				0/1	b0	Power-on caused the reset.
0x1C	**WDogCode**	**P**	**W**	**B**	0x00			Alternate writes of code-Bytes 0x5A and 0xC3 are required to prevent timeout. Watchdog is reloaded after every write (only one code has to be written to reload the watchdog, but the value of the code-Byte has to alternate between 0x5A and 0xC3).
0x1D	**WDogPeriod**				0x00	-0-	b7	Reserved, not used
		P	**W**	**B**		0	b6	Watchdog timeout value. Depending on **WdogClkSelect** bit in the **Config** register (R0x0E, b2), the watchdog will be decremented by either a 32 kHz clock or the signal on the **CLKOUT** pin (in which case the watchdog will be suspended when the HFCLK stops). The Watchdog is disabled after the reset and started by writing to **WDogPeriod**. Once started, the clock selection or timeout value cannot be changed.
		P	**W**	**B**		0	b5	
		P	**W**	**B**		0	b4	
		P	**W**	**B**		0	b3	
		P	**W**	**B**		0	b2	
		P	**W**	**B**		0	b1	
		P	**W**	**B**		0	b0	

3. High-Frequency (HF) Oscillator

The frequency synthesizer in the SH3000 is constructed from the 2:1 digitally-tunable 8.0–16.0 MHz High-Frequency (HF) oscillator followed by a programmable binary post-divider; see **Figure 5**.

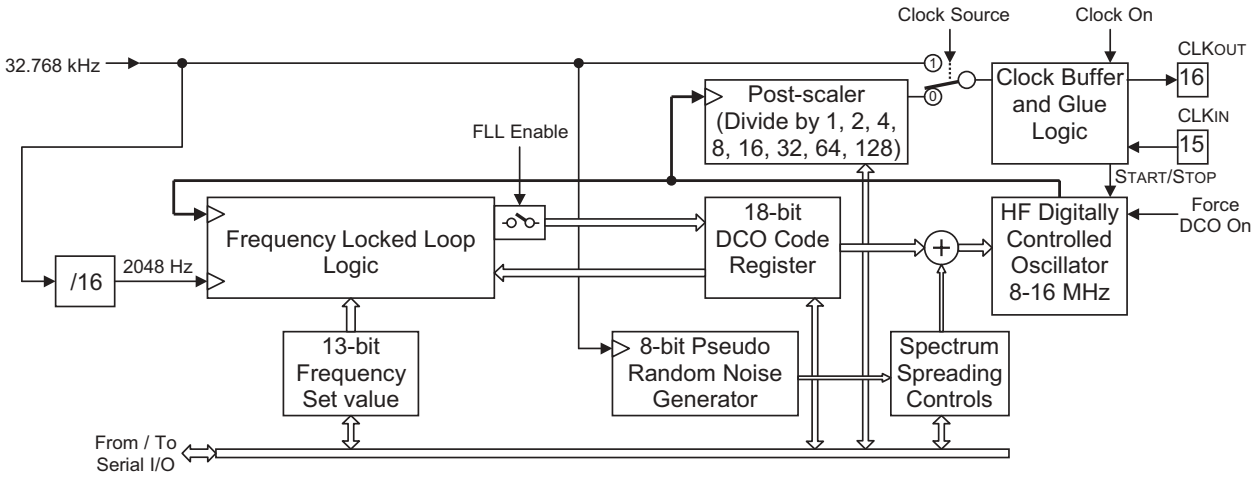

Figure 5: High-Frequency (HF) Oscillator

The **Clock Source** selector and the programmable **Post-scaler** allow instantaneous switching between the 32 kHz internal clock and the divided-down HF oscillator output. There is no settling or instability when the switch occurs.

The SH3000 employs a Frequency Locked Loop (FLL) to synchronize the HF clock to the 32 kHz reference. This architecture has several advantages over the common PLL (Phase Lock Loop) systems, including the ability to stop and re-start without frequency transients and instability, and with instant settling to a correct frequency. The conventional PLL approach invariably includes a low-pass filter that requires a long settling time on restart.

When the HF oscillator is operating without FLL control, it can set the frequency of the clock on the **CLKOUT** pin to ±0.025%, and maintain it to ±0.5% over temperature.

When the HF oscillator is operating under FLL control, the absolute accuracy and stability of the HF clock depends on the quality of the 32.768 kHz internally generated clock. An external 32.768 kHz watch crystal used as a reference provides excellent accuracy and stability for the SH3000.

The primary purpose of the FLL is the maintenance of the correct frequency while the ambient temperature is changing. As the temperature drift of the HF oscillator is quite small, any corrective action from the FLL system is also small and gradual, in proportion with the changes in temperature.

To set a new frequency for the FLL, the host microcontroller writes the 13-bit Frequency Set value to the appropriate bits in registers **SS_FreqSet** (R0x15) and **FreqSetLSB** (R0x16); it may also update the post-scaler setting in the **WP_PostScale** register (R0x17). The resulting output frequency is calculated using simple formulas [1] and [2] (reference frequency is 32.768 kHz):

FOSC = 2048 Hz * (Frequency Set value + 1) [1]

FOUT = FOSC / (Post-divider setting) [2]

For example, a post-divider setting of /8 and the Frequency Set value of 4000 (0x0FA0) produce an output frequency of 1.024 MHz. **Table 3** shows the available frequencies with the corresponding resolution at high and low frequency limits.

Table 3: Operating Parameters for FLL

Post-divider	Frequency Resolution Hz	Frequency Range		
		High (Guaranteed) Hz	Low (Guaranteed) Hz	Low (Typical) Hz
/1	2048	16,777,216	7,999,488	6,144,000
/2	1024	8,388,608	3,999,744	3,072,000
/4	512	4,194,304	1,999,872	1,536,000
/8	256	2,097,152	999,936	768,000
/16	128	1,048,576	499,968	384,000
/32	64	524,288	249,984	192,000
/64	32	262,144	124,992	96,000
/128	16	131,072	62,496	48,000
Frequency Set value	**Dec**	8191	3905	2999
	Hex	0x1FFF	**0x0F41**	**0x0BB7**
Resolution	**%**	0.01221	0.02560	0.03333
	ppm	122	256	333

When the Frequency Set value changes, the FLL synthesizer needs some settling time to lock the new frequency. There are several possible methods for decreasing this time:

1. The host microcontroller may simply wait for the FLL to lock, checking the FLL lock flag (bit 0) in the **Status** register (R0x1A). This approach is the simplest but also the slowest. Depending on the frequency step it may take up to two seconds to obtain the lock. The frequency change from the old to the new value is slow and gradual.

2. The host may issue a Coarse Lock command by setting the coarse lock bit (bit 1) in the **FLLcontrol** register (R0x0F). The SH3000 performs a successive approximation algorithm on the 18-bit DCO (digitally controlled oscillator) code value (contained in registers R0x13, R0x14, and R0x18) and finds a locked setting in approximately 25 ms. The clock may experience frequency fluctuations of up to 2:1.

3. If the frequency step is small (less than 256 kHz at the undivided output of the HF oscillator), the host may issue a fine lock command by setting the fine lock bit (bit 2) in the **FLLcontrol** register. The SH3000 performs a successive approximation algorithm on the 7 least significant bits of the 18-bit DCO code value, and finds a locked setting in approximately 5 ms. The clock may experience the maximum frequency fluctuations of only 3.2%.

4. The host may write the new value into the DCO code registers to directly control the frequency of the HF oscillator. This method is preferable and results in minimum settling time. The 18-bit DCO code value can be obtained from programming the HF oscillator to a correct frequency using method 2 or 3 above (at start-up or at some point in the operation), reading the value from the DCO code registers, and storing the value in the host's memory. This calibration should be performed for each of the frequencies to be employed. This method allows the locking time to be as small as 1 or 2 ms, independent of the frequency step.

5. The host may perform a custom or proprietary algorithm for frequency control; the SH3000 provides all of the information, reference, and timing signals needed.

During each of the settling methods described above, the processor clock can be switched to 32 kHz, and would be completely free of any frequency fluctuations or instabilities. Since the SH3000 automatically shuts down the HF oscillator when 32 kHz is selected as the output frequency, the HF oscillator should be forced to an active state by setting the Force DCO On bit (bit 5) in the **Config** register (R0x0E).

Systems requiring a very stable clock for short periods of time (controlling an integrating D/A converter, for example), may stop the FLL action in the SH3000 by resetting the FLL enable bit (bit 0) in the **FLLcontrol** register (R0x0F).

3.1 Auto Clock Detect Mode

The SH3000 HF oscillator block has two main modes with which to operate.

1. Mode 1 provides a system clock source. In this mode the **CLKOUT** pin supplies a clock at the frequency configured by the register settings. It can be enabled/disabled by setting/resetting the **CLKOUT** pin enable bit (bit 3) of the **Config** register (R0x0E).*

2. Mode 2 provides a CPU oscillator source. In this mode, the **CLKOUT** pin supplies a clock frequency configured by the register settings. It can be enabled/disabled by setting/resetting the **CLKOUT** pin enable bit of the **Config** register.* When the host microcontroller enters stop mode, the SH3000 **CLKIN** pin detects the absence of transitions from the host oscillator output pin, and shuts down the **CLKOUT** pin within four clock cycles to save power. At this time the SH3000 configures the **CLKOUT** pin in such a way that as soon as the host exits stop mode via a reset or interrupt signal, the **CLKIN** pin receives a transition. When this occurs, the SH3000 restarts the clock within 2 μs. This happens much faster than with a standard crystal or a ceramic resonator, faster even than with an LC tank circuit. This is a key feature of low-power operation of the SH3000.

The operating mode is determined by **CLKIN**. If the SH3000 detects at least four transitions on the **CLKIN** pin, it assumes Mode 2 is in effect and configures itself to auto-clock detect. This also sets the corresponding bit (bit 4) in the **Status** register (R0x1A).

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* As programmatically disabling the **CLKOUT** pin causes the clock to be irrecoverable, the periodic timer must be set and enabled before this is done. The SH3000 does not disable the clock unless the periodic timer is enabled.

3.2 Programmable Spread Spectrum

The SH3000 offers a technique for reducing electromagnetic interference (EMI). It can be a part of the initial design strategy, or it can be applied in the prototype stage to fix problems identified during compliance testing. This feature of the SH3000 may greatly reduce the requirements for radio frequency (RF) shielding, and permits the use of simple plastic casings in place of expensive RFI-coated or metal casings.

The SH3000 employs programmable spectrum spreading to reduce RF emissions from the processor's clock. There are five possible settings; see **Table 4** for operating and performance figures in the 8–16 MHz range.

Spectrum spreading is implemented by varying the frequency of the HF oscillator with a pseudo-random sequence (with a zero-average DC component). The Maximum-Length Sequence (MLS) 8-bit random number generator, clocked by 32 kHz, is used. Only 4, 5, 6, or 7 bits of the generated 8-bit random number are used, according to the configuration setting.

Maximum fluctuations of the frequency depend on the selected frequency range and the position within the range. Selecting the HF oscillator frequency near the high end of the range limits the peak variations to ±0.1%, ±0.2%, ±0.4%, or ±0.8%.

The spread spectrum values are set in the **SS_FreqSet** register (R0x15). Bit 5 enables spectrum spreading, and bits 7:6 specify the spreading bandwidth.

Table 4: EMI reduction with Spectrum Spreading

Setting			Spreading Bandwidth **kHz**	Peak EMI Reduction **(guaranteed) db**	Peak EMI Reduction **(measured) db**
En b5	CFG1 b7	CFG0 b6			
0	X	X	Off	0	0
1	0	0	32	-3	-3
1	0	1	64	-6	-7
1	1	0	128	-9	-10
1	1	1	256	-12	-15

3.3 High-Frequency (HF) Oscillator Registers

ADDRESS	NAME	RESET EVENT			RESET VALUE			DESCRIPTION
		PowerOn	WDog	BrownOut	HEX	BINARY		
0x0E	Config	P			0x88	1	b7	**XTALtune Rewrite-Once Enable** (see notes for use)
		P	W	B		0	b6	Register Page for R0x10 through R0x17. 0 =Page0, 1 =Page1.
		P	W	B		0	b5	ForceDCOon. Forces HF Oscillator to run under all conditions.
		P	W	B		0	b4	CLKOUT source. 1 = 32 kHz, 0 = HFCLK.
		P	W	B		1	b3	CLKOUTEnable. 1 = enable, 0 = disable.
		P	W	B		0	b2	WdogClkSelect. 1 = CLKOUT, 0 = 32 kHz.
		P	W	B		0	b1	Interrupt Flag Clear. 1 = clear, 0 = no effect, always reads 0.
		P	W	B		0	b0	Interrupt Enable. 1 = enable, 0 = disable.
0x0F	FLLcontrol				0x00 or 0x01	-0-	b7	Reserved, not used
						-0-	b6	Reserved, not used
						-0-	b5	Reserved, not used
						-0-	b4	Reserved, not used
						-0-	b3	Reserved, not used
		P	W	B		0	b2	Start FLL fine frequency lock (~5 ms to achieve lock).
		P	W	B		0	b1	Start FLL coarse frequency lock (~25 ms to achieve lock).
		P	W	B		0/1	b0	Enable FLL. 1 = enabled, 0 = disabled. On Reset =pin CLKSEL.

ADDRESS	PAGE	NAME	INIT EVENT			INIT VALUE		WRITE PROTECT				Xtal REWRITE-once		DESCRIPTION
			PowerOn	WDog	BrownOut	HEX	BINARY	IDCode	Calibration	Application	VBOValue			
0x13	0	VREF_DCOcode	P	W		0x??	?		C				b7	Adjustment for internal temperature-compensated Voltage Reference, Factory-Only temperature drift trim.
			P	W			?		C				b6	
			P	W			?		C				b5	
			P	W			?		C				b4	
			P	W	B		?			A			b3	Disconnect Internal **RREF**, 0=connected, 1 = disconnected.
			P	W	B		?			A			b2	DCO setting, most-significant bits 15:17.
			P	W	B		?			A			b1	
			P	W	B		?			A			b0	
0x14	0	DCOcode1	P	W	B	0x??				A				Bits 7:14 of DCO setting
0x15	0	SS_FreqSet	P	W	B	0x??	?			A			b7	Amount of HFCLK Spectrum Spreading, 4 (four) settings.
			P	W	B		?			A			b6	
			P	W	B		?			A			b5	EnableSS, enable spectrum spreading.
			P	W	B		?			A			b4	Frequency Set Value for FLL, most-significant bits 8:12
			P	W	B		?			A			b3	
			P	W	B		?			A			b2	
			P	W	B		?			A			b1	
			P	W	B		?			A			b0	
0x16	0	FreqSetLSB	P	W	B	0x??				A				Frequency Set Value for FLL, bits 0:7.
0x17	0	WP_PostScale	P	W		0x??	?	◆					b7	IDCode Write Protect, 1 = no writes.
			P	W			?		◆				b6	Calibration Write Protect, 1 = no writes.
			P	W			?			◆			b5	Application Write Protect, 1 = no writes.
			P	W			?				◆		b4	VBO Value Write Protect, 1 = no writes.
			P	W	B		?			A			b3	CLK32 enable, 1 = enable, 0 = disable.
			P	W	B		?			A			b2	DCO Post-Scaler, 8 (eight) setting: **/1, 2, 4, 8, 16, 32, 64, 128**.
			P	W	B		?			A			b1	
			P	W	B		?			A			b0	

ADDRESS	NAME	RESET EVENT			RESET VALUE			DESCRIPTION
		PowerOn	WDog	BrownOut	HEX	BINARY		
0x18	DCOcodeLSB				0x40	-0-	b7	Reserved, not used
		P	W	B		1	b6	DCO setting, least-significant bits 0:6
		P	W	B		0	b5	
		P	W	B		0	b4	
		P	W	B		0	b3	
		P	W	B		0	b2	
		P	W	B		0	b1	
		P	W	B		0	b0	
0x1A	Status	P	W	B	0x00	0	b7	Xtal oscillator is stable
						-0-	b6	Reserved, not used
						-0-	b5	
		P	W	B		0	b4	Auto CLK shut-down mode (transitions on **CLKIN** detected).
		P	W	B		0	b3	Backup battery low.
		P	W	B		0	b2	Serial I/O parity error.
		P	W	B		0	b1	Interrupt status (1 = pending, 0 = idle).
		P	W	B		0	b0	FLL locked (1 = locked, 0 = unlocked).

4. Low-Frequency (LF) Oscillator

The Low Frequency (LF) Oscillator System provides the 32 kHz clock to all internal circuits and to the dedicated output pin, **CLK32**. The 32 kHz clock can also be output to the **CLKOUT** pin by setting bit 4 in the **Config** register (R0x0E).

If enabled, the **CLK32** output continues normal operations when **VDD** is absent and backup power is available; in this case, the output voltage swings between zero and **VBATT**.

When power is first applied to the SH3000, the RC oscillator takes over. It supplies the 32 kHz clock for start-up and initialization. However, if the **CLKSEL** pin is set high, then the crystal oscillator is enabled. Once the crystal has started and stabilized, the internal 32 kHz clock switches to the very accurate crystal frequency (and the xtal oscillator stable bit, bit 7 in the **Status** register R0x1A, is set). See **Figure 6**.

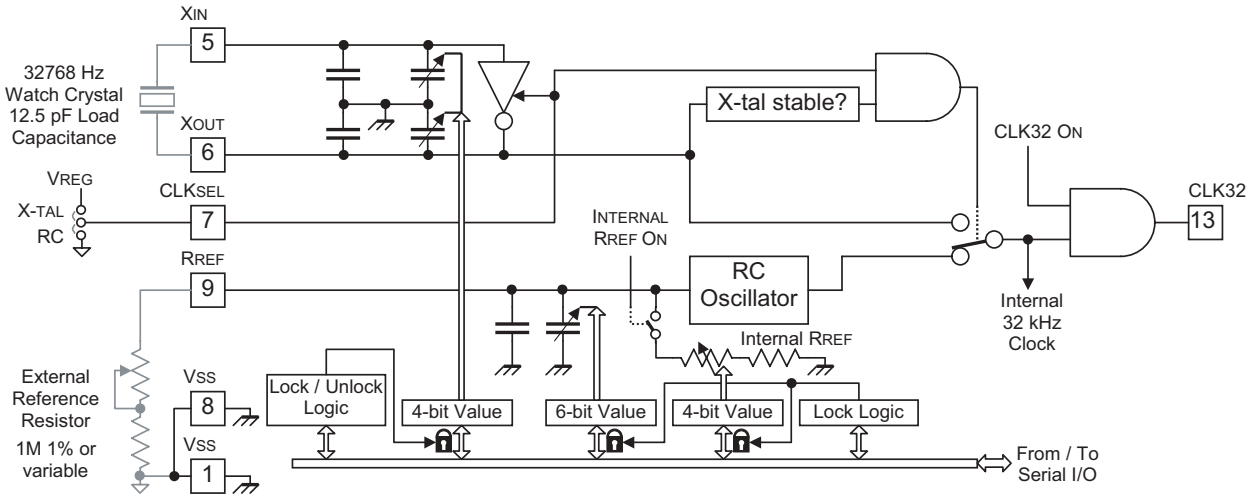


Figure 6: Low-Frequency (LF) Oscillator

The default calibration values for the RC oscillator are loaded on power-up from the factory-programmed OTP non-volatile memory. They can be reprogrammed at any time, or they can be permanently protected from any changes by setting the Lock flag or an OTP write-protect flag. Factory calibration brings the frequency of the RC oscillator within +/- 3 % of the 32768 Hz for the internal reference resistor, and 2% for the external 1M 1 % resistor, over the entire temperature and supply voltage range.

The frequency of the RC oscillator can be tuned or modulated by varying the external reference resistor,which should be located as close as possible to **RREF**, pin 9, to minimize noise pickup.

The crystal oscillator has the unique feature of adjustable load capacitors. It permits tuning of the circuit for initial tolerances of the crystal (often +/- 20 ppm) as well as an adjustment for the required load capacitance (with possible variations from the PCB layout). While the oscillator was designed for a crystal with a nominal load capacitance of 12.5 pF, the circuit accommodates any value from 7–22 pF (depending on parasitics of the layout). All of these corrections can be performed when the part is already installed on the PCB in the actual circuit.

The default value for load capacitance (12.5 pF) loaded on power-up from the factory-programmed OTP non-volatile memory can be re-programmed at any time, or it can be completely protected from any changes by a permanent OTP write-protect flag.

To reprogram the load capacitance, clear the XTALtune Rewrite-Once Enable bit (bit 7) of the **Config** register (R0x0E) and then immediately set bits 7:4 of the register **Xtune_RREFAdj** (R0x12) with the desired value; **Table 5** shows the available values.

Table 5: Load Capacitance Settings

Xtune code	Padding capacitance (pF)	Effective crystal load capacitance (pF)	Effective ppm adjustment
0000	26	13	-4
0001	28	14	-10
0010	30	15	-16
0011	32	16	-21
0100	34	17	-26
0101	36	18	-31
0110	38	19	-35
0111	40	20	-37
1000	10	5	118
1001	12	6	91
1010	14	7	70
1011	16	8	52
1100	18	9	36
1101	20	10	23
1110	22	11	15
1111	24	12	4

The adjustment can set the frequency of the crystal oscillator to within +/- 4 ppm of the ideal value. As a reference, a typical 32.768 kHz crystal changes its frequency 4 ppm for a 10°C change in temperature. Since the temperature characteristics of crystals are well known and stable, the host microcontroller is free to implement an algorithm for temperature compensation of the crystal oscillator using the adjustable load capacitors, with the resulting accuracy of +/- 4 ppm over the entire temperature range.

4.1 Low-Frequency (LF) Oscillator Registers

ADDRESS	NAME	RESET EVENT			RESET VALUE			DESCRIPTION
		PowerOn	WDog	BrownOut	HEX	BINARY		
0x0E	Config	P			0x88	1	b7	**XTALtune Rewrite-Once Enable** (see notes for use)
		P	W	B		0	b6	Register Page for R0x10 through R0x17. 0 =Page0, 1 =Page1.
		P	W	B		0	b5	ForceDCOon. Forces HF Oscillator to run under all conditions.
		P	W	B		0	b4	CLKOUT source. 1 = 32 kHz, 0 = HFCLK.
		P	W	B		1	b3	CLKOUTEnable. 1 = enable, 0 = disable.
		P	W	B		0	b2	WdogClkSelect. 1 = CLKOUT, 0 = 32 kHz.
		P	W	B		0	b1	Interrupt Flag Clear. 1 = clear, 0 = no effect, always reads 0.
		P	W	B		0	b0	Interrupt Enable. 1 = enable, 0 = disable.

ADDRESS	PAGE	NAME	INIT EVENT			INIT VALUE		WRITE PROTECT				Xtal REWRITE-once		DESCRIPTION
			PowerOn	WDog	BrownOut	HEX	BINARY	IDCode	Calibration	Application	VBOValue			
0x11	0	IPol_RCtune				0x??	-0-						b7	Reserved, not used
			P	W	B		?			A			b6	Interrupt Polarity, 1 = High, 0 = Low.
			P	W	B		?		C				b5	32 kHz RC Oscillator Adjustment, nominal ~330 Hz per step.
			P	W	B		?		C				b4	
			P	W	B		?		C				b3	
			P	W	B		?		C				b2	
			P	W	B		?		C				b1	
			P	W	B		?		C				b0	
0x12	0	Xtune_RREFAdj	P			0x??	?					R	b7	32.768 kHz Xtal Oscillator fine tune (see notes for use)
			P				?					R	b6	
			P				?					R	b5	
			P				?					R	b4	
			P	W	B		?		C				b3	Internal **RREF** Adjustment, nominal ~330 Hz per step.
			P	W	B		?		C				b2	
			P	W	B		?		C				b1	
			P	W	B		?		C				b0	
0x13	0	VREF_DCOcode	P	W		0x??	?		C				b7	Adjustment for internal temperature-compensated Voltage Reference, Factory-Only temperature drift trim.
			P	W			?		C				b6	
			P	W			?		C				b5	
			P	W			?		C				b4	
			P	W	B		?			A			b3	Disconnect Internal **RREF**, 0=connected, 1 = disconnected.
			P	W	B		?			A			b2	DCO setting, most-significant bits 15:17.
			P	W	B		?			A			b1	
			P	W	B		?			A			b0	
0x17	0	WP_PostScale	P	W		0x??	?						b7	IDCode Write Protect, 1 = no writes.
			P	W			?						b6	Calibration Write Protect, 1 = no writes.
			P	W			?						b5	Application Write Protect, 1 = no writes.
			P	W			?						b4	VBO Value Write Protect, 1 = no writes.
			P	W	B		?			A			b3	CLK32 enable, 1 = enable, 0 = disable.
			P	W	B		?			A			b2	DCO Post-Scaler, 8 (eight) setting: **/1, 2, 4, 8, 16, 32, 64, 128**.
			P	W	B		?			A			b1	
			P	W	B		?			A			b0	

ADDRESS	NAME	RESET EVENT			RESET VALUE		DESCRIPTION	
		PowerOn	WDog	BrownOut	HEX	BINARY		
0x1A	Status	P	W	B	0x00	0	b7	Xtal oscillator is stable
						-0-	b6	Reserved, not used
						-0-	b5	
		P	W	B		0	b4	Auto CLK shut-down mode (transitions on **CLKIN** detected).
		P	W	B		0	b3	Backup battery low.
		P	W	B		0	b2	Serial I/O parity error.
		P	W	B		0	b1	Interrupt status (1 = pending, 0 = idle).
		P	W	B		0	b0	FLL locked (1 = locked, 0 = unlocked).

5. Real-Time Clock (RTC)

The Real-Time Clock (RTC) feature uses the internal 32 kHz clock from the low-frequency (LF) oscillator. As shown in **Figure 7**, the RTC divides the 32 kHz clock by 128 to produce a 256 Hz clock. The next divider is a modulo-256 counter, which is readable and write-able from the serial interface. The next stage is a divide by 60, which provides seconds in BCD format. Another divide-by-60 counter provides minutes in BCD, followed by a divide-by-24 counter that provides hours in 24-hour mode in BCD format. This in turn clocks a 16-bit binary counter, which can log up to 65535 days (over 179 years).

Using a 4 ppm 32.768 kHz clock from the LF oscillator, the RTC module keeps time with a maximum error as low as 2 minutes per year.

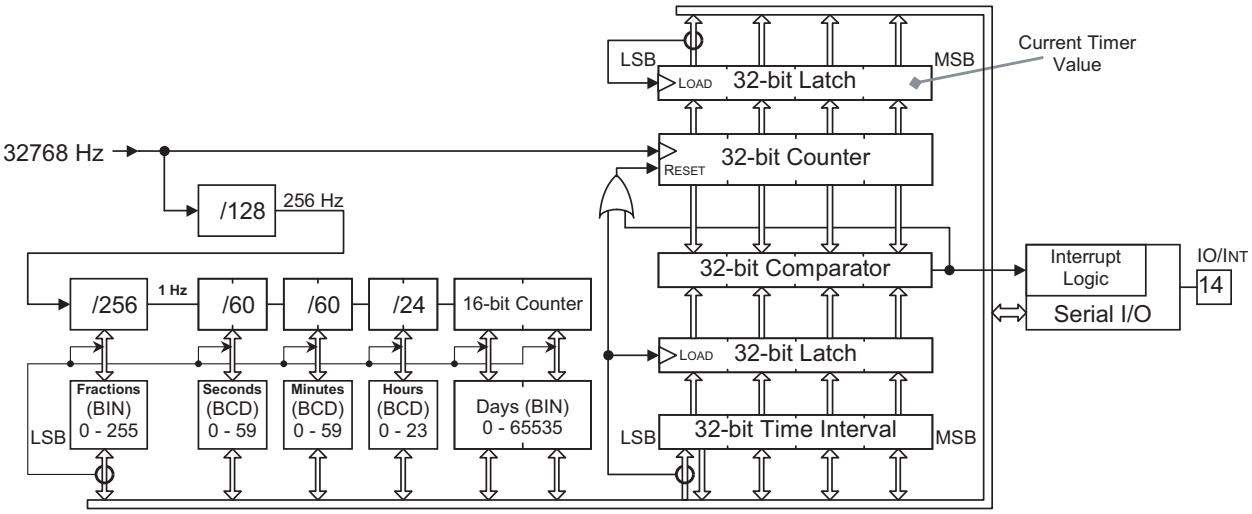


Figure 7: Real-Time Support: Real-Time Clock (RTC), Periodic Interrupt, & Wake-up Timer

The **VBAK** pin can be connected to a backup power supply for the real-time clock, +2.3 to +5.5 V (+1.8 to +5.5 V typical). This voltage can be higher or lower than **VDD**. Connect a backup battery or backup capacitor (with external recharge circuit).

When reading the RTC registers (R0x08–R0x0D), the register **RTCsubseconds** (R0x0D) should be read first. When the register **RTCsubseconds** is read, all six bytes of the RTC counters are latched into the holding registers simultaneously. This avoids problems of counter overflows between individual byte reads.

The RTC registers can be written to in any order. Only when the register **RTCsubseconds** is written are the entire six byte loaded into the RTC counters.

Note: Check the SH3000 Errata document.

5.1 Real-Time Clock (RTC) Registers

ADDRESS	NAME	RESET EVENT			RESET VALUE		DESCRIPTION	
		PowerOn	WDog	BrownOut	HEX	BINARY		
0x08	RTCdaysMSB	P	W		0x00		16-bit binary value, 0x0000 to 0xFFFF (0 to 65535, ~ 179.5 years).	When **RTCsubseconds** is read, all RTC registers are updated. When **RTCsubseconds** is written, the whole RTC counter chain is loaded.
0x09	RTCdaysLSB	P	W		0x00			
0x0A	RTChours	P	W		0x00		BCD value, 0 to 23.	
0x0B	RTCminutes	P	W		0x00		BCD value, 0 to 59.	
0x0C	RTCseconds	P	W		0x00		BCD value, 0 to 59.	
0x0D	RTCsubseconds	P	W		0x00		8-bit binary value, 0 to 0xFF (0 to 255)	

6. Periodic Interrupt/Wake-up Timer

The periodic interrupt / wakeup timer can be used to create very accurate recurring interrupts for use by the host microcontroller. With some minimal software support, it can also be used to create alarms, with practically unlimited duration.

While the timer is running, the host can switch to a low-power mode (halted or stopped). The interrupt wakes up the host, which can perform the requisite task and go back to sleep, until the next periodic interrupt. This mode of operation can achieve extremely low average power consumption.

As shown in **Figure 7**, a 32-bit counter is clocked by 32.768 kHz, producing a minimum interval of 30.5 µs and a maximum interval of 36.4 hours.

After reset, the timer is stopped until the new 32-bit value for the timer interval is written into the four Period registers (R0x00-R0x03). When the least significant byte (the **PeriodLSB** register, R0x03) is written, the whole value is moved to the Timer Interval latch, the counter is reset, and the counter starts to increment with the 32 kHz clock.

When the 32-bit comparator detects a match, an interrupt is generated, and the counter is reset and starts the next timing cycle.

Although the counter cannot be written to, the current value from the counter can be read at any time. The whole 32-bit value is loaded into the 32-bit Timer Interval latch when the least significant byte is read. This prevents errors stemming from the finite time between the readings of individual bytes of the current value.

If there is an interrupt pending from the SH3000, and the host microcontroller does not clear the interrupt pending bit, then the SH3000 issues an interrupt after each subsequent read or write cycle until this bit is cleared (see **Figure 7**).

6.1 Periodic Interrupt/Wake-up Timer Registers

ADDRESS	NAME	RESET EVENT			RESET VALUE		DESCRIPTION
		PowerOn	WDog	BrownOut	HEX	BINARY	
0x00	PeriodMSB	P	W	B	0x00		Periodic Interrupt / Wake-up Timer setting. With 32.768 kHz clock the period = (32-bit value)/32768. When the value = 0, the Timer is disabled. The whole 32-bit value is loaded into timer logic when **PeriodLSB** is written.
0x01	Period2	P	W	B	0x00		
0x02	Period1	P	W	B	0x00		
0x03	PeriodLSB	P	W	B	0x00		
0x04	TimerMSB	P	W	B	0x00		Free-running counter. This counter is reset when the **PeriodLSB** is written (Timer started) or the value of the counter is equal to 32-bit Period value (Interrupt / Wake-up generated). The whole 32-bit Timer value is loaded into Timer registers when **TimerLSB** is read.
0x05	Timer2	P	W	B	0x00		
0x06	Timer1	P	W	B	0x00		
0x07	TimerLSB	P	W	B	0x00		
0x0E	Config	P			0x88	1	b7 **XTALtune Rewrite-Once Enable** (see notes for use)
		P	W	B		0	b6 Register Page for R0x10 through R0x17. 0 =Page0, 1 =Page1.
		P	W	B		0	b5 ForceDCOon. Forces HF Oscillator to run under all conditions.
		P	W	B		0	b4 CLKOUT source. 1 = 32 kHz, 0 = HFCLK.
		P	W	B		1	b3 CLKOUTEnable. 1 = enable, 0 = disable.
		P	W	B		0	b2 WdogClkSelect. 1 = CLKOUT, 0 = 32 kHz.
		P	W	B		0	b1 Interrupt Flag Clear. 1 = clear, 0 = no effect, always reads 0.
		P	W	B		0	b0 Interrupt Enable. 1 = enable, 0 = disable.

ADDRESS	NAME	RESET EVENT			RESET VALUE		DESCRIPTION
		PowerOn	WDog	BrownOut	HEX	BINARY	
0x1A	Status	P	W	B	0x00	0	b7 Xtal oscillator is stable
						-0-	b6 Reserved, not used
						-0-	b5
		P	W	B		0	b4 Auto CLK shut-down mode (transitions on **CLKIN** detected).
		P	W	B		0	b3 Backup battery low.
		P	W	B		0	b2 Serial I/O parity error.
		P	W	B		0	b1 Interrupt status (1 = pending, 0 = idle).
		P	W	B		0	b0 FLL locked (1 = locked, 0 = unlocked).

7. Serial Interface

7.1 Serial Communications Interface

The SH3000 and the host microcontroller communicate using a single wire, bi-directional asynchronous serial interface. The bit rate is automatically determined by the SH3000. The SH3000 contains 36 addressable registers located at 0x00–0x1F; see the Registers chapter of this manual. Some of these registers are accessed through a page operation. Pin 14, **IO/INT**, is the serial communications interface and interrupt output pin. This pin is internally weakly pulled to the opposite of the programmed interrupt polarity. For example, if interrupt is programmed to be active low, this pin is weakly pulled to **VDD** when inactive.

As shown in **Figure 8,** the SH3000 and the host communicate with serial data streams. The host always initiates communication. A data stream consists of the following (in this order):

- 3-bit start field
- 3-bit read/write code
- 5-bit address field
- 1 guard bit
- 8-bit data field
- 2 parity bits

Plus, for write streams only:

- 1 guard bit
- 2 acknowledge (ACK) bits

The 3-bit start field (1,0,1 or 0,1,0, depending on interrupt polarity) uses the middle bit to determine the bit period of the serial data stream.

The 3-bit read/write code consists of 1,1,0 for a read, or 0,1,1 for a write. This protects against early glitches hat might otherwise put the interface into an invalid read or write access mode.

The 5-bit address field contains the address of the register.

A single guard bit gives the interface a safe period in which to change data direction. The value of a guard bit does not matter.

The 8-bit data field is written to (read from) the register.

Two parity bits: The first parity bit is high when there are an odd number of bits in the read/write, address and data fields; the second parity bit is the inverse of the first.

For write streams only, a guard bit is appended to the stream (to allow safe turnaround), and then two acknowledge bits, which are a direct copy of the parity bits, are driven back to the host to indicate a successful write access.

Two guard bits are appended to the end of the access stream (read or write). The host can not start the next access before receiving these bits.

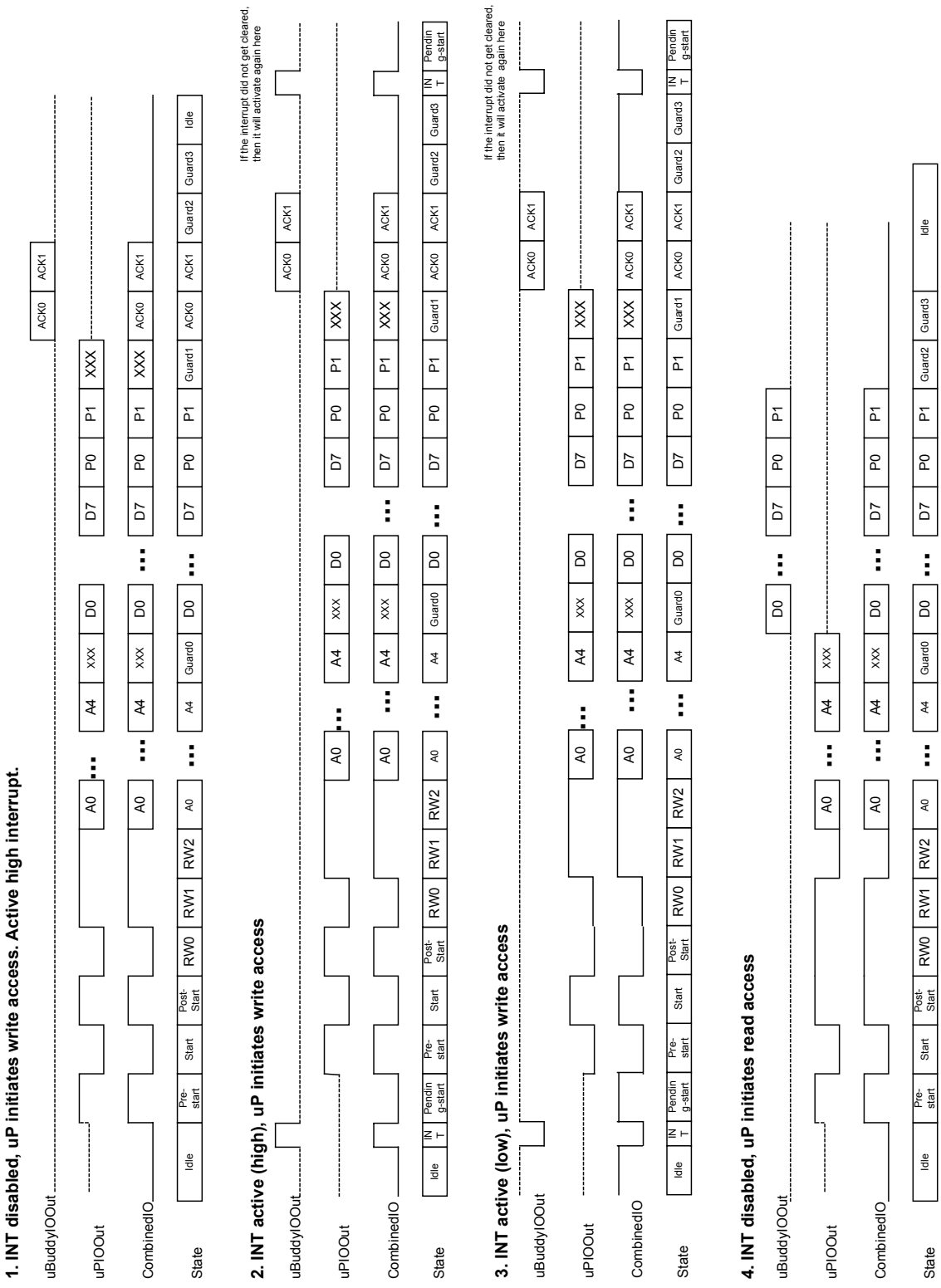
The interface is self-timed based on the duration of the start bit field, and communication can take place whenever **CLKOUT** is active, either at 32 kHz or at a higher frequency. If the host microcontroller is running synchronously to the **CLKOUT** generated by the SH3000 (which should generally be the case), then a minimum of 4 **CLKOUT** cycles per bit are required to maintain communication integrity. If the host's serial interface is asynchronous to **CLKOUT**, then a minimum of 52 cycles per bit are necessary. A maximum of 1024 **CLKOUT** cycles per bit field is supported.

Table 6 displays the minimum and maximum bit periods for the serial communications for **CLKOUT** frequencies of 16 MHz, 8 MHz, and 2 MHz.

Table 6: Minimum/Maximum Serial Bit Timing

CLKOUT Frequency	**Minimum Bit Period (host synchronous to CLKOUT)**	**Minimum Bit Period (host asynchronous to CLKOUT)**	**Maximum Bit Period**
16 MHz	250 ns	1.625 µs	32 µs
8 MHz	500 ns	3.25 µs	63.9 µs
2 MHz	2 µs	13 µs	255 µs

Figure 8: Serial Communication Timing Diagram



7.2 Interrupt Interface

The serial communications line to the SH3000 (Pin 14, **IO/INT**) also serves as the interrupt to the host microcontroller. The polarity of the interrupt is software programmable using the interrupt polarity bit (bit 6) of the **IPol_RCtune** register (R0x11). This pin is asserted for four cycles of **CLKOUT**, and then returns to the inactive state.

The interrupt line is used by the Periodic Interrupt/Wake-up Timer to interrupt the host when it reaches its end of count. See the Periodic Interrupt/Wake-up Timer chapter in this manual.

7.3 Serial Communication/Interrupt Registers

ADDRESS	NAME	RESET EVENT			RESET VALUE		DESCRIPTION	
		PowerOn	WDog	BrownOut	HEX	BINARY		
0x0E	Config	P			0x88	1	b7	**XTALtune Rewrite-Once Enable** (see notes for use)
		P	W	B		0	b6	Register Page for R0x10 through R0x17. 0 =Page0, 1 =Page1.
		P	W	B		0	b5	ForceDCOon. Forces HF Oscillator to run under all conditions.
		P	W	B		0	b4	CLKOUT source. 1 = 32 kHz, 0 = HFCLK.
		P	W	B		1	b3	CLKOUTEnable. 1 = enable, 0 = disable.
		P	W	B		0	b2	WdogClkSelect. 1 = CLKOUT, 0 = 32 kHz.
		P	W	B		0	b1	Interrupt Flag Clear. 1 = clear, 0 = no effect, always reads 0.
		P	W	B		0	b0	Interrupt Enable. 1 = enable, 0 = disable.

ADDRESS	PAGE	NAME	INIT EVENT			INIT VALUE		WRITE PROTECT				Xtal REWRITE-once	DESCRIPTION	
			PowerOn	WDog	BrownOut	HEX	BINARY	IDCode	Calibration	Application	VBOValue			
0x11	0	IPol_RCtune				0x??	-0-						b7	Reserved, not used
			P	W	B		?			A			b6	Interrupt Polarity, 1 = High, 0 = Low.
			P	W	B		?		C				b5	32 kHz RC Oscillator Adjustment, nominal ~330 Hz per step.
			P	W	B		?		C				b4	
			P	W	B		?		C				b3	
			P	W	B		?		C				b2	
			P	W	B		?		C				b1	
			P	W	B		?		C				b0	

ADDRESS	NAME	RESET EVENT			RESET VALUE		DESCRIPTION	
		PowerOn	WDog	BrownOut	HEX	BINARY		
0x1A	Status	P	W	B	0x00	0	b7	Xtal oscillator is stable
						-0-	b6	Reserved, not used
						-0-	b5	
		P	W	B		0	b4	Auto CLK shut-down mode (transitions on **CLKIN** detected).
		P	W	B		0	b3	Backup battery low.
		P	W	B		0	b2	Serial I/O parity error.
		P	W	B		0	b1	Interrupt status (1 = pending, 0 = idle).
		P	W	B		0	b0	FLL locked (1 = locked, 0 = unlocked).

8. Auxiliary Functions

8.1 Scratchpad RAM and ID number

Four bytes of general-purpose RAM reside at addresses R0x00, R0x12, R0x14, and R0x16 on page 1 in the SH3000 register space. Immediately after reset, these four bytes are loaded with the factory-programmed values in the OTP memory. For a standard device, these values are all zeroes. Unique serial numbers or other information could be stored here. Since the RAM/ID registers reside on page 1, a 1 must be written to the page bit (bit 6) of the **Config** register (R0x0E) in order to access the RAM/ID registers.

ADDRESS	NAME	RESET EVENT			RESET VALUE		DESCRIPTION	
		PowerOn	WDog	BrownOut	HEX	BINARY		
0x0E	Config	P			0x88	1	b7	**XTALtune Rewrite-Once Enable** (see notes for use)
		P	W	B		0	b6	Register Page for R0x10 through R0x17. 0 =Page0, 1 =Page1.
		P	W	B		0	b5	ForceDCOon. Forces HF Oscillator to run under all conditions.
		P	W	B		0	b4	CLKOUT source. 1 = 32 kHz, 0 = HFCLK.
		P	W	B		1	b3	CLKOUTEnable. 1 = enable, 0 = disable.
		P	W	B		0	b2	WdogClkSelect. 1 = CLKOUT, 0 = 32 kHz.
		P	W	B		0	b1	Interrupt Flag Clear. 1 = clear, 0 = no effect, always reads 0.
		P	W	B		0	b0	Interrupt Enable. 1 = enable, 0 = disable.

ADDRESS	PAGE	NAME	INIT EVENT			INIT VALUE		WRITE PROTECT				Xtal REWRITE-once	DESCRIPTION
			PowerOn	WDog	BrownOut	HEX	BINARY	IDCode	Calibration	Application	VBOValue		
0x10	1	ID_RAM_MSB	P	W	B	0x??		I					General-purpose RAM, bits 24:31, bits 24:31 of ID code are loaded on initialization.
0x12	1	ID_RAM_2	P	W	B	0x??		I					General-purpose RAM, bits 16:23, bits 16:23 of ID code are loaded on initialization.
0x14	1	ID_RAM_1	P	W	B	0x??		I					General-purpose RAM, bits 8:15, bits 08:15 of ID code are loaded on initialization.
0x16	1	ID_RAM_LSB	P	W	B	0x??		I					General-purpose RAM, bits 0:7, bits 00:07 of ID code are loaded on initialization.

8.2 Write Protect Logic

The SH3000 MicroBuddy™ provides a comprehensive set of write-protect flags to safeguard groups of related bits from inadvertent corruption. Register **WP_PostScale** (R0x17) contains four write-protect flags, each acting on one group of bits.

The individual protected groups are:

1. **VBO** value (controlled by R0x17 bit 4)
2. Application group (controlled by R0x17 bit 5)
3. Calibration group (controlled by R0x17 bit 6)
4. IDCode value (controlled by R0x17 bit 7)

The influence of the individual write-protect bits is shown in the register table on the next page.

If any of these four bits is factory-programmed to “one” in OTP non-volatile memory, then the access to the corresponding group of bits is totally inhibited.

If the write-protect bit is programmed to “zero,” then the access is permitted. The host micro can change the values of any bits within the protected group. When the user desires to enable write-protection, the corresponding write-protect flag should be set. Once any of the write-protect bits is set, it cannot be reset, and write operations on the related group of bits is inhibited.

If the write-protect bit is programmed to “zero,” then the Power-on reset condition or any Watchdog reset condition resets the write-protect flag, and write access is again permitted. The Brownout condition neither resets the write-protect flags nor re-enables the write accesses.

Note: The write-once protection mechanism for the programmable load capacitance of the LF crystal oscillator is independent of these write-protect flags in R0x17. To reprogram the load capacitance, clear the XTALtune Rewrite-Once Enable bit (bit 7) of the **Config** register (R0x0E) and then immediately write bits 4:7 of the register **Xtune_RREFAdj** (R0x12) with the desired value; the write-once enable bit must be cleared just before each and every write access to bits 4:7 of the register **Xtune_RREFAdj** (R0x12). See the LF Oscillator chapter of this manual for the available values.

Write Protect Logic Registers

ADDRESS	NAME	RESET EVENT			RESET VALUE		DESCRIPTION	
		PowerOn	WDog	BrownOut	HEX	BINARY		
0x0E	Config	P			0x88	1	b7	**XTALtune Rewrite-Once Enable** (see notes for use)
		P	W	B		0	b6	Register Page for R0x10 through R0x17. 0 =Page0, 1 =Page1.
		P	W	B		0	b5	ForceDCOon. Forces HF Oscillator to run under all conditions.
		P	W	B		0	b4	CLKOUT source. 1 = 32 kHz, 0 = HFCLK.
		P	W	B		1	b3	CLKOUTEnable. 1 = enable, 0 = disable.
		P	W	B		0	b2	WdogClkSelect. 1 = CLKOUT, 0 = 32 kHz.
		P	W	B		0	b1	Interrupt Flag Clear. 1 = clear, 0 = no effect, always reads 0.
		P	W	B		0	b0	Interrupt Enable. 1 = enable, 0 = disable.

ADDRESS	PAGE	NAME	INIT EVENT			INIT VALUE		WRITE PROTECT				Xtal REWRITE-once	DESCRIPTION	
			PowerOn	WDog	BrownOut	HEX	BINARY	IDCode	Calibration	Application	VBOValue			
0x15	0	SS_FreqSet	P	W	B	0x??	?			A			b7	Amount of HFCLK Spectrum Spreading, 4 (four) settings.
			P	W	B		?			A			b6	
			P	W	B		?			A			b5	EnableSS, enable spectrum spreading.
			P	W	B		?			A			b4	Frequency Set Value for FLL, most-significant bits 8:12
			P	W	B		?			A			b3	
			P	W	B		?			A			b2	
			P	W	B		?			A			b1	
			P	W	B		?			A			b0	
0x16	0	FreqSetLSB	P	W	B	0x??				A				Frequency Set Value for FLL, bits 0:7.
0x17	0	WP_PostScale	P	W		0x??	?	◆					b7	IDCode Write Protect, 1 = no writes.
			P	W			?		◆	↑			b6	Calibration Write Protect, 1 = no writes.
			P	W			?			◆			b5	Application Write Protect, 1 = no writes.
			P	W			?			↓	◆		b4	VBO Value Write Protect, 1 = no writes.
			P	W	B		?			A			b3	CLK32 enable, 1 = enable, 0 = disable.
			P	W	B		?	↓		A			b2	DCO Post-Scaler, 8 (eight) setting: **/1, 2, 4, 8, 16, 32, 64, 128**.
			P	W	B		?			A			b1	
			P	W	B		?			A			b0	

8.3 Voltage Regulator

The **VREG** pin can be used as a nominal 2.20 V reference voltage or a supply source for small loads (< 5 mA). A bypass capacitor may be necessary between this pin and **VSS** if the load generates large current transients or a low ripple reference is required.

Using **VREG** to drive external loads may degrade the performance of the SH3000.

8.4 Backup Power

The **VBAK** pin can be connected to a backup power supply for the real-time clock, +2.3 to +5.5 V (+1.8 to +5.5 V typical). This voltage can be higher or lower than **VDD**. Connect a backup battery or backup capacitor (with external recharge circuit).

9. Registers

Table 7: SH3000 MicroBuddy™ Registers 0x00 to 0x0F

Timer, RTC, Configuration, and Control Registers

ADDRESS	NAME	RESET EVENT			RESET VALUE		DESCRIPTION		
		PowerOn	WDog	BrownOut	HEX	BINARY			
0x00	PeriodMSB	P	W	B	0x00		Periodic Interrupt / Wake-up Timer setting. With 32.768 kHz clock the period = (32-bit value)/32768. When the value = 0, the Timer is disabled. The whole 32-bit value is loaded into timer logic when **PeriodLSB** is written.		
0x01	Period2	P	W	B	0x00				
0x02	Period1	P	W	B	0x00				
0x03	PeriodLSB	P	W	B	0x00				
0x04	TimerMSB	P	W	B	0x00		Free-running counter. This counter is reset when the **PeriodLSB** is written (Timer started) or the value of the counter is equal to 32-bit Period value (Interrupt / Wake-up generated). The whole 32-bit Timer value is loaded into Timer registers when **TimerLSB** is read.		
0x05	Timer2	P	W	B	0x00				
0x06	Timer1	P	W	B	0x00				
0x07	TimerLSB	P	W	B	0x00				
0x08	RTCdaysMSB	P	W		0x00		16-bit binary value, 0x0000 to 0xFFFF (0 to 65535, ~ 179.5 years).	When **RTCsubseconds** is read, all RTC registers are updated. When **RTCsubseconds** is written, the whole RTC counter chain is loaded.	
0x09	RTCdaysLSB	P	W		0x00				
0x0A	RTChours	P	W		0x00		BCD value, 0 to 23.		
0x0B	RTCminutes	P	W		0x00		BCD value, 0 to 59.		
0x0C	RTCseconds	P	W		0x00		BCD value, 0 to 59.		
0x0D	RTCsubseconds	P	W		0x00		8-bit binary value, 0 to 0xFF (0 to 255)		
0x0E	Config	P			0x88	1	b7	**XTALtune Rewrite-Once Enable** (see notes for use)	
		P	W	B		0	b6	Register Page for R0x10 through R0x17. 0 =Page0, 1 =Page1.	
		P	W	B		0	b5	ForceDCOon. Forces HF Oscillator to run under all conditions.	
		P	W	B		0	b4	CLKOUT source. 1 = 32 kHz, 0 = HFCLK.	
		P	W	B		1	b3	CLKOUTEnable. 1 = enable, 0 = disable.	
		P	W	B		0	b2	WdogClkSelect. 1 = CLKOUT, 0 = 32 kHz.	
		P	W	B		0	b1	Interrupt Flag Clear. 1 = clear, 0 = no effect, always reads 0.	
		P	W	B		0	b0	Interrupt Enable. 1 = enable, 0 = disable.	
0x0F	FLLcontrol				0x00 or 0x01	-0-	b7	Reserved, not used	
						-0-	b6	Reserved, not used	
						-0-	b5	Reserved, not used	
						-0-	b4	Reserved, not used	
						-0-	b3	Reserved, not used	
		P	W	B		0	b2	Start FLL fine frequency lock (~5 ms to achieve lock).	
		P	W	B		0	b1	Start FLL coarse frequency lock (~25 ms to achieve lock).	
		P	W	B		0/1	b0	Enable FLL. 1 = enabled, 0 = disabled. On Reset =pin CLKSEL.	

Table 8: SH3000 MicroBuddy™ Registers 0x10 to 0x17

Control, Setting, and Calibration Registers Initialized from OTP Memory

ADDRESS	PAGE	NAME	INIT EVENT			INIT VALUE		WRITE PROTECT				Xtal REWRITE-once		DESCRIPTION
			PowerOn	WDog	BrownOut	HEX	BINARY	IDCode	Calibration	Application	V_{BO}Value			
0x10	0	V_{BO}Value				0x??	-0-						b7	Reserved, not used
							-0-						b6	Reserved, not used
			P	W			?				V		b5	V_{BO} Threshold Value, 2.3 V to 4.4 V in ~33.33 mV steps.
			P	W			?				V		b4	
			P	W			?				V		b3	
			P	W			?				V		b2	
			P	W			?				V		b1	
			P	W			?				V		b0	
0x11	0	IPol_RCtune				0x??	-0-						b7	Reserved, not used
			P	W	B		?			A			b6	Interrupt Polarity, 1 = High, 0 = Low.
			P	W	B		?		C				b5	32 kHz RC Oscillator Adjustment, nominal ~330 Hz per step.
			P	W	B		?		C				b4	
			P	W	B		?		C				b3	
			P	W	B		?		C				b2	
			P	W	B		?		C				b1	
			P	W	B		?		C				b0	
0x12	0	Xtune_R_{REF}Adj	P			0x??	?					R	b7	32.768 kHz Xtal Oscillator fine tune (see notes for use)
			P				?					R	b6	
			P				?					R	b5	
			P				?					R	b4	
			P	W	B		?		C				b3	Internal **R_{REF}** Adjustment, nominal ~330 Hz per step.
			P	W	B		?		C				b2	
			P	W	B		?		C				b1	
			P	W	B		?		C				b0	
0x13	0	V_{REF}_DCOcode	P	W		0x??	?		C				b7	Adjustment for internal temperature-compensated Voltage Reference, Factory-Only temperature drift trim.
			P	W			?		C				b6	
			P	W			?		C				b5	
			P	W			?		C				b4	
			P	W	B		?			A			b3	Disconnect Internal **R_{REF}**, 0=connected, 1 = disconnected.
			P	W	B		?			A			b2	DCO setting, most-significant bits 15:17.
			P	W	B		?			A			b1	
			P	W	B		?			A			b0	
0x14	0	DCOcode1	P	W	B	0x??				A				Bits 7:14 of DCO setting

Control, Setting, and Calibration Registers Initialized from OTP Memory (continued)

ADDRESS	PAGE	NAME	INIT EVENT			INIT VALUE		WRITE PROTECT				Xtal REWRITE-once		DESCRIPTION
			PowerOn	WDog	BrownOut	HEX	BINARY	IDCode	Calibration	Application	VBOValue			
0x15	0	SS_FreqSet	P	W	B	0x??	?			A			b7	Amount of HFCLK Spectrum Spreading, 4 (four) settings.
			P	W	B		?			A			b6	
			P	W	B		?			A			b5	EnableSS, enable spectrum spreading.
			P	W	B		?			A			b4	Frequency Set Value for FLL, most-significant bits 8:12
			P	W	B		?			A			b3	
			P	W	B		?			A			b2	
			P	W	B		?			A			b1	
			P	W	B		?			A			b0	
0x16	0	FreqSetLSB	P	W	B	0x??				A				Frequency Set Value for FLL, bits 0:7.
0x17	0	WP_PostScale	P	W		0x??	?	◆					b7	IDCode Write Protect, 1 = no writes.
			P	W			?		◆				b6	Calibration Write Protect, 1 = no writes.
			P	W			?			◆			b5	Application Write Protect, 1 = no writes.
			P	W			?				◆		b4	VBO Value Write Protect, 1 = no writes.
			P	W	B		?			A			b3	CLK32 enable, 1 = enable, 0 = disable.
			P	W	B		?			A			b2	DCO Post-Scaler, 8 (eight) setting: **/1, 2, 4, 8, 16, 32, 64, 128**.
			P	W	B		?			A			b1	
			P	W	B		?			A			b0	
0x10	1	ID_RAM_MSB	P	W	B	0x??		I						General-purpose RAM, bits 24:31, bits 24:31 of ID code are loaded on initialization.
0x11	1	Reserved												Reserved, not used.
0x12	1	ID_RAM_2	P	W	B	0x??		I						General-purpose RAM, bits 16:23, bits 16:23 of ID code are loaded on initialization.
0x13	1	Reserved												Reserved, not used.
0x14	1	ID_RAM_1	P	W	B	0x??		I						General-purpose RAM, bits 8:15, bits 08:15 of ID code are loaded on initialization.
0x15	1	Reserved												Reserved, not used.
0x16	1	ID_RAM_LSB	P	W	B	0x??		I						General-purpose RAM, bits 0:7, bits 00:07 of ID code are loaded on initialization.
0x17	1	Reserved												Reserved, not used.

Table 9: SH3000 MicroBuddy™ Registers 0x18 to 0x1F

Control and Status Registers

ADDRESS	NAME	RESET EVENT			RESET VALUE			DESCRIPTION
		PowerOn	WDog	BrownOut	HEX	BINARY		
0x18	**DCOcodeLSB**				0x40	-0-	b7	Reserved, not used
		P	W	B		1	b6	DCO setting, least-significant bits 0:6
		P	W	B		0	b5	
		P	W	B		0	b4	
		P	W	B		0	b3	
		P	W	B		0	b2	
		P	W	B		0	b1	
		P	W	B		0	b0	
0x19	Reserved							Reserved, not used
0x1A	**Status**	P	W	B	0x00	0	b7	Xtal oscillator is stable
						-0-	b6	Reserved, not used
						-0-	b5	
		P	W	B		0	b4	Auto CLK shut-down mode (transitions on **CLKIN** detected).
		P	W	B		0	b3	Backup battery low.
		P	W	B		0	b2	Serial I/O parity error.
		P	W	B		0	b1	Interrupt status (1 = pending, 0 = idle).
		P	W	B		0	b0	FLL locked (1 = locked, 0 = unlocked).
0x1B	**ResetEvent**				0x02 0x04 0x08 or 0x09	-0-	b7	Reserved, not used
						-0-	b6	
						-0-	b5	
						-0-	b4	
		P		B		0/1	b3	V_{DD} dropped below V_{BO} threshold (brown-out).
			W			0/1	b2	Watchdog code violation caused the reset.
			W			0/1	b1	Watchdog timeout caused the reset.
		P				0/1	b0	Power-on caused the reset.
0x1C	**WDogCode**	P	W	B	0x00			Alternate writes of code-Bytes 0x5A and 0xC3 are required to prevent timeout. Watchdog is reloaded after every write (only one code has to be written to reload the watchdog, but the value of the code-Byte has to alternate between 0x5A and 0xC3).
0x1D	**WDogPeriod**				0x00	-0-	b7	Reserved, not used
		P	W	B		0	b6	Watchdog timeout value. Depending on **WdogClkSelect** bit in the **Config** register (R0x0E, b2), the watchdog will be decremented by either a 32 kHz clock or the signal on the **CLKOUT** pin (in which case the watchdog will be suspended when the HFCLK stops). The Watchdog is disabled after the reset and started by writing to **WDogPeriod**. Once started, the clock selection or timeout value cannot be changed.
		P	W	B		0	b5	
		P	W	B		0	b4	
		P	W	B		0	b3	
		P	W	B		0	b2	
		P	W	B		0	b1	
		P	W	B		0	b0	
0x1E	Reserved							Reserved, not used
0x1F	Factory Test							Reserved, do not write to this register.

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