S3C2443X

USER'S MANUAL

Revision 1.2

REVISION HISTORY

Revision	Date	Description
1.0	February 7, 2007	First release
1.1	March 6, 2007	IIC Bus Interface update
1.2	March 22, 2007	Overview, Electrical Data update (Operating voltage of VDD_SDRAM: 1.8V => 1.8V/2.5V/3.3V)

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32-BIT RISC MICROCONTROLLERS USER MANUAL

Revision 1.2

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Samsung Electronics Co., Ltd.
San #24 Nongseo-Dong, Giheung- gu
Yongin-City, Gyeonggi-Do, Korea
C.P.O. Box #37, Suwon 449-900

TEL: (82)-(031)-209-1928
FAX: (82)-(031)-209-1909

Home Page: http://www.samsungsemi.com
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NOTES

1 PRODUCT OVERVIEW

INTRODUCTION

This user's manual describes SAMSUNG's S3C2443X 16/32-bit RISC microprocessor. SAMSUNG's S3C2443X is designed to provide hand-held devices and general applications with low-power, and high-performance micro-controller solution in small die size. To reduce total system cost, the S3C2443X includes the following components.

The S3C2443X is developed with ARM920T core, 0.13um CMOS standard cells and a memory complier. Its low-power, simple, elegant and fully static design is particularly suitable for cost- and power-sensitive applications. It adopts a new bus architecture known as Advanced Micro controller Bus Architecture (AMBA).

The S3C2443X offers outstanding features with its CPU core, a 16/32-bit ARM920T RISC processor designed by Advanced RISC Machines, Ltd. The ARM920T implements MMU, AMBA BUS, and Harvard cache architecture with separate 16KB instruction and 16KB data caches, each with an 8-word line length.

By providing a complete set of common system peripherals, the S3C2443X minimizes overall system costs and eliminates the need to configure additional components. The integrated on-chip functions that are described in this document include:

- Around 400MHz @ 1.3V, 533MHz @ 1.375V Core, 1.8V/2.5V/3.3V ROM/SRAM, 1.8V/2.5V/3.3V SDRAM, 3.3V external I/O microprocessor with 16KB I-Cache/16KB D-Cache/MMU
- External memory controller (SDRAM Control and Chip Select logic) and CF/ATA I/F controller
- LCD controller (up to 4K color STN and 256K color TFT) with LCD-dedicated DMA
- 6-ch DMA controllers with external request pins
- 4-ch UARTs (IrDA1.0, 64-Byte Tx FIFO, and 64-Byte Rx FIFO)
- 2-ch SPIs (1-ch High Speed SPI)
- IIC bus interface (multi-master support)
- IIS Audio CODEC interface & AC97 CODEC Interface
- SD Host interface version 1.0 & MMC Protocol version 2.11 compatible
- High-Speed MMC Protocol version 4.0 compatible
- 2-ch USB Host controller (ver 1.1 Complaint)/1-ch USB Device controller (ver 2.0 Complaint)
- 4-ch PWM timers / 1-ch Internal timer / Watch Dog Timer
- 10-ch 10-bit ADC and Touch screen interface
- RTC with calendar function
- Camera interface (Max. 8M pixels input support. 2M pixel input support for scaling)
- 147 General Purpose I/O ports / 24-ch external interrupt source
- Power control: Normal, Idle, Stop and Sleep mode
- On-chip clock generator with PLL

FEATURES

Architecture

- Integrated system for hand-held devices and general embedded applications.
- 16/32-Bit RISC architecture and powerful instruction set with ARM920T CPU core.
- Enhanced ARM architecture MMU to support WinCE, EPOC 32 and Linux.
- Instruction cache, data cache, write buffer and Physical address TAG RAM to reduce the effect of main memory bandwidth and latency on performance.
- ARM920T CPU core supports the ARM debug architecture.
- Internal Advanced Microcontroller Bus Architecture (AMBA) (AMBA2.0, AHB/APB).

System Manager

- Little/Big Endian support.
- Two independent memory bus - one for the ROM/SRAM bus (ROM Bank0~Bank5) and one for the DRAM bus (SDRAM Bank0~Bank1)
- Address space: 64M bytes for Rom bank0 ~ bank5, 128M bytes for SDRAM bank0 ~ bank1.
- Supports programmable 8/16-bit data bus width for ROM/SRAM bank and programmable 16/32-bit data bus width for DRAM bank
- Fixed bank start address from Rom bank 0 to bank 5 and SDRAM bank 0 to bank1.
- Eight memory banks:
  - Six memory banks for ROM, SRAM, and others (NAND/CF etc.).
  - Two memory banks for Synchronous DRAM.
- Complete Programmable access cycles for all memory banks.
- Supports external wait signals to expand the bus cycle.
- Supports self-refresh mode in SDRAM for power-down.
- Supports various types of ROM for booting (NOR/NAND Flash, EEPROM, OneNAND and others).

NAND Flash Boot Loader

- Supports booting from NAND flash memory. (Only 8bit boot support)
- 4KB internal buffer for booting.
- Supports storage memory for NAND flash memory after booting.
- Supports Advanced NAND flash

Cache Memory

- 64-way set-associative cache with I-Cache (16KB) and D-Cache (16KB).
- 8words length per line with one valid bit and two dirty bits per line.
- Pseudo random or round robin replacement algorithm.
- Write-through or write-back cache operation to update the main memory.
- The write buffer can hold 16 words of data and four addresses.

Clock & Power Manager

- On-chip MPLL and EPLL:
  EPLL generates the clock to operate USB Host, IIS, UART, etc.
  MPLL generates the clock to operate MCU at maximum 533Mhz @ 1.375V.
- Clock can be fed selectively to each function block by software.
- Power mode: Normal, Idle, STOP and Sleep mode
  Normal mode: Normal operating mode
  Idle mode: The clock for only CPU is stopped.
  STOP mode: All clocks are stopped.
  Sleep mode: The Core power including all peripherals is shut down.
- Woken up by EINT[15:0] or RTC alarm & tick interrupt from Sleep mode and STOP mode.

FEATURES (Continued)

Interrupt Controller

- 69 Interrupt sources
  (One Watch dog timer, 5 timers, 12 UARTs, 24 external interrupts, 6 DMA, 2 RTC, 2 ADC, 1 IIC, 2 SPI, 2 SDI, 2 USB, 4 LCD, 1 Battery Fault, 1 NAND, 1 CF, 1 AC97 and 2 CAM I/F)
- Level/Edge mode on external interrupt source
- Programmable polarity of edge and level
- Supports Fast Interrupt request (FIQ) for very urgent interrupt request

Timer with Pulse Width Modulation (PWM)

- 4-ch 16-bit Timer with PWM / 1-ch 16-bit internal timer with DMA-based or interrupt-based operation
- Programmable duty cycle, frequency, and polarity
- Dead-zone generation
- Supports external clock sources

RTC (Real Time Clock)

- Full clock feature: msec, second, minute, hour, date, day, month, and year
- 32.768 KHz operation
- Alarm interrupt
- Time tick interrupt

General Purpose Input/Output Ports

- 24 external interrupt ports
- 147 Multiplexed input/output ports

DMA Controller

- 6-ch DMA controller
- Supports memory to memory, IO to memory, memory to IO, and IO to IO transfers
- Burst transfer mode to enhance the transfer rate

LCD Controller STN LCD Displays Feature

- Supports 3 types of STN LCD panels: 4-bit dual scan, 4-bit single scan, 8-bit single scan display type
- Supports monochrome mode, 4 gray levels, 16 gray levels, 256 colors and 4096 colors for STN LCD
- Supports multiple screen size
  – Typical actual screen size: 640x480, 320x240,
  160x160, and others.
  – Maximum frame buffer size is 4 Mbytes.
  – Maximum virtual screen size in 256 color mode: 4096x1024, 2048x2048, 1024x4096 and others

TFT(Thin Film Transistor) Color Displays Feature

- Supports 1, 2, 4 or 8 bpp (bit-per-pixel) palette color displays for color TFT
- Supports 16, 24 bpp non-palette true-color displays for color TFT
- Supports maximum 16M color TFT at 24 bpp mode
- Supports multiple screen size
  – Typical actual screen size: 640x480, 320x240, 160x160, and others.
  – Maximum frame buffer size is 4Mbytes.
  – Maximum virtual screen size in 64K color mode: 2048x2048, and others
- Support 2 overlay windows for TFT

UART

- 4-channel UART with DMA-based or interrupt-based operation
- Supports 5-bit, 6-bit, 7-bit, or 8-bit serial data transmit/receive (Tx/Rx)
- Supports external clocks for the UART operation (UEXTCLK)
- Programmable baud rate
- Supports IrDA 1.0
- Loopback mode for testing
- Each channel has internal 64-byte Tx FIFO and 64-byte Rx FIFO.

FEATURES (Continued)

A/D Converter & Touch Screen Interface

- 10-ch multiplexed ADC
- Max. 500KSPS and 10-bit Resolution
- Internal FET for direct Touch screen interface

Watchdog Timer

- 16-bit Watchdog Timer
- Interrupt request or system reset at time-out

IIC-Bus Interface

- 1-ch Multi-Master IIC-Bus
- Serial, 8-bit oriented and bi-directional data transfers can be made at up to 100 Kbit/s in Standard mode or up to 400 Kbit/s in Fast mode.

IIS-Bus Interface

- 1-ch IIS-bus for audio interface with DMA-based operation
- Serial, 8-/16-bit per channel data transfers
- 128 Bytes (64-Byte + 64-Byte) FIFO for Tx/Rx
- Supports IIS format and MSB-justified data format

AC97 Audio Interface

- 1-ch AC97 for audio interface with DMA-based operation
- 16-bit Stereo Audio

USB Host

- 2-port USB Host
- Complies with OHCI Rev. 1.0
- Compatible with USB Specification version 1.1

USB Device

- 1-port USB Device
- 9 Endpoints for USB Device
- Compatible with USB Specification version 2.0

SD/MMC Host Interface

- Normal, Interrupt and DMA data transfer mode (byte, halfword, word transfer)
- DMA burst4 access support (only word transfer)
- Compatible with SD Memory Card Protocol version 1.0
- Compatible with SDIO Card Protocol version 1.0
- 64 Bytes FIFO for Tx/Rx
- One Compatible with Multimedia Card Protocol version 2.11, the other with version 4.0 (HS-MMC)

SPI Interface

- Compatible with 2-ch Serial Peripheral Interface Protocol version 2.11 (1ch. High speed SPI interface)
- 2x8 bits Shift register for Tx/Rx
- DMA-based or interrupt-based operation

Camera Interface

- ITU-R BT 601/656 8-bit mode support
- DZI (Digital Zoom In) capability
- Programmable polarity of video sync signals
- Max. 16M pixels input support (8M pixel input support for scaling)
- Image mirror and rotation (X-axis mirror, Y-axis mirror, and 180° rotation)
- Camera output format (RGB 16/24-bit and YCbCr 4:2:0/4:2:2 format)

Operating Voltage Range

- Core: 1.3 V for 400MHz
  1.375 V for 533MHz
  ROM/SRAM: 1.8V/ 2.5V/3.0V/3.3V
  SDRAM: 1.8V/ 2.5V/ 3.3V
- I/O: 1.8V/2.5V/3.3V(refer to electrical data)

Operating Frequency

- Fclk Up to 533MHz
- Hclk Up to 133MHz
- Pclk Up to 67MHz

Package

- 400 FBGA 13x13

BLOCK DIAGRAM

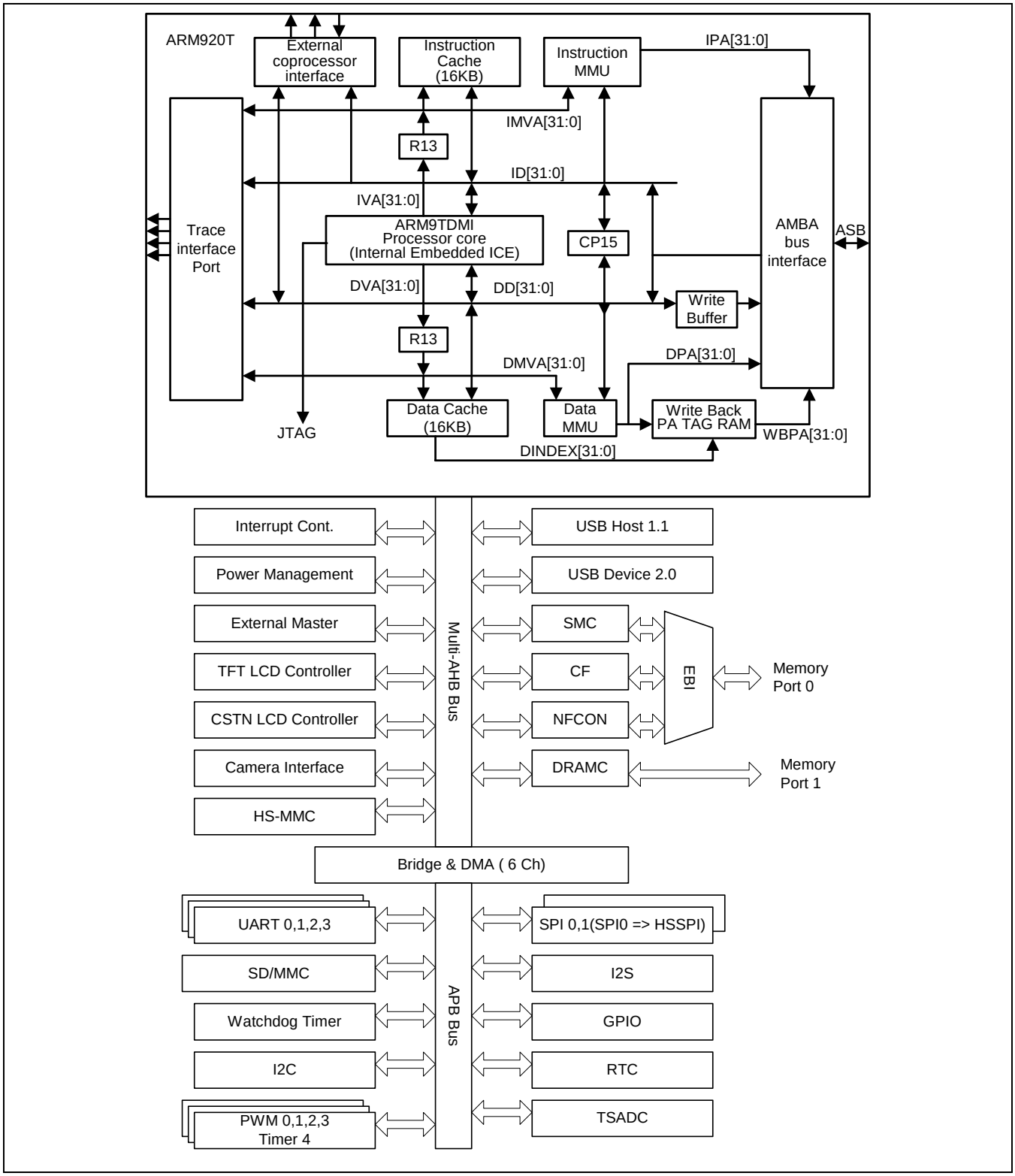


Figure 1-1. S3C2443X Block Diagram

PIN ASSIGNMENTS

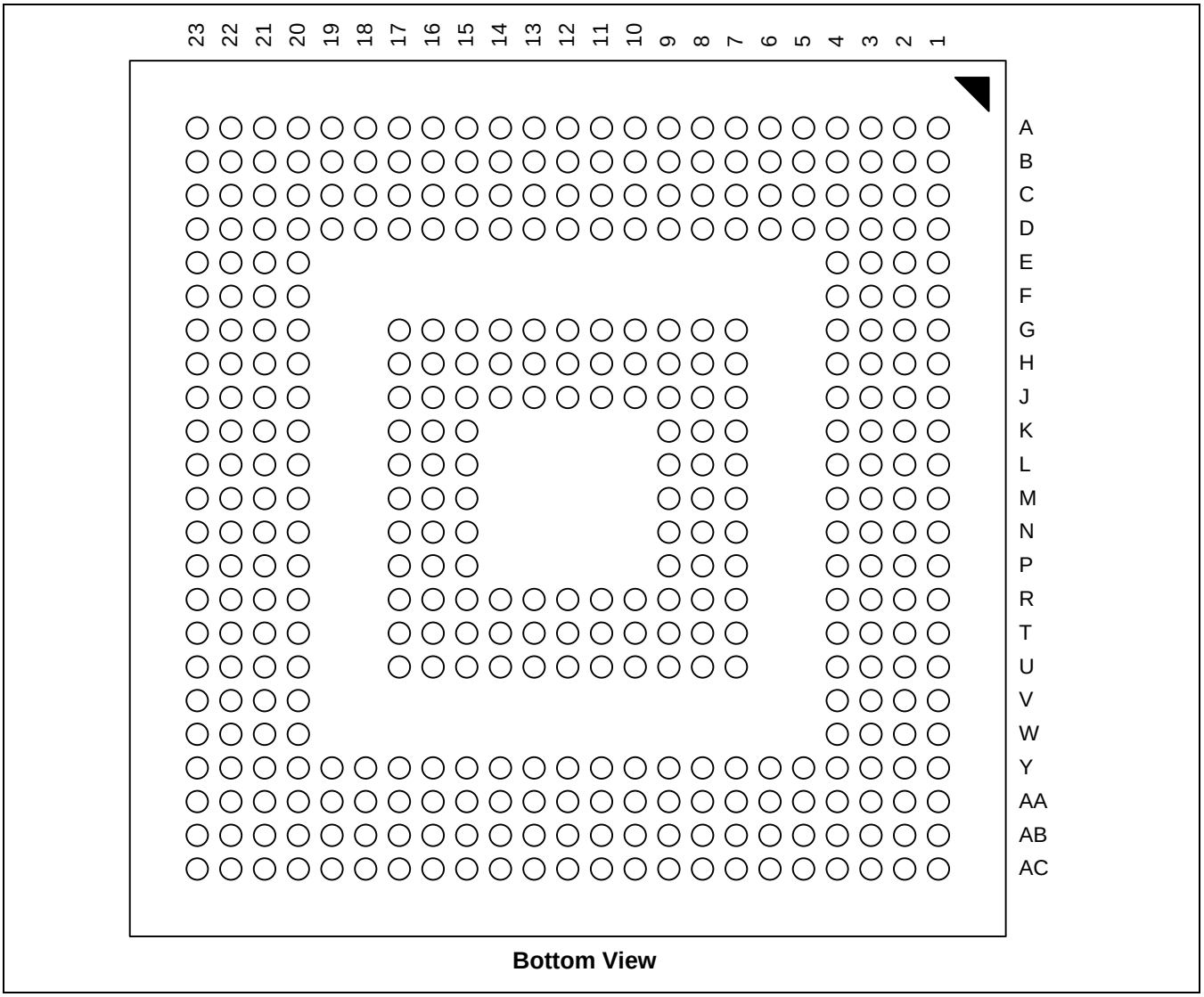


Figure 1-2. S3C2443X Pin Assignments (400-FBGA) Top view

Table 1-1. 400-Pin FBGA Pin Assignments – Pin Number Order (1/4)

Pin	Pin Name	Ball	Pin	Pin Name	Ball	Pin	Pin Name	Ball
1	VDD_SRAM	C3	35	RDATA2	K3	69	VSSiarm	R1
2	RSMCLK/GPA13	B2	36	RDATA1	K8	70	VD1/GPC9	P7
3	VSS_SRAM	D4	37	RDATA0	J1	71	VSS_LCD	R2
4	RSMVAD/GPA14	C2	38	CAMVSYNC/GPJ9	K7	72	VDD_LCD	P8
5	RSMBWAIT/GPM0	B1	39	CAMHREF/GPJ10	K2	73	VD2/GPC10	T1
6	nRCS3	C1	40	VSSi	L4	74	VD3/GPC11	P9
7	nRCS4	C4	41	VDDi	L3	75	VD4/GPC12	R3
8	nRCS5/GPA12	E4	42	CAMPCLK/GPJ8	K9	76	VD5/GPC13	T2
9	nWAIT	D2	43	CAMDATA0/GPJ0	K1	77	VD6/GPC14	T3
10	FCLE	F3	44	CAMDATA1/GPJ1	L8	78	VD7/GPC15	R7
11	FALE	D3	45	CAMDATA2/GPJ2	L2	79	VD8/GPD0	U1
12	VDDi	D1	46	CAMDATA3/GPJ3	L7	80	VD9/GPD1	R8
13	VSSi	E2	47	VDD_CAM	M4	81	VDDiarm	U4
14	nFWE	G4	48	VSS_CAM	L1	82	VSSiarm	U2
15	nFRE	E1	49	CAMDATA4/GPJ4	M2	83	VD10/GPD2	V1
16	nFCE	F4	50	CAMDATA5/GPJ5	L9	84	VD11/GPD3	T7
17	FRnB/GPM1	F2	51	CAMDATA6/GPJ6	M3	85	VD12/GPD4	U3
18	VDD_SRAM	F1	52	CAMDATA7/GPJ7	M8	86	VD13/GPD5	T8
19	VSS_SRAM	E3	53	VDDiarm	M1	87	VD14/GPD6	V2
20	RDATA15	H4	54	VSSiarm	N4	88	VD15/GPD7	V3
21	RDATA14	G2	55	CAMPCLKOUT/GPJ11	N3	89	VD16/GPD8	W1
22	RDATA13	G3	56	CAMRESET/GPJ12	M7	90	VD17/GPD9	W3
23	RDATA12	G1	57	LEND/GPC0	N1	91	VD18/GPD10	W2
24	RDATA11	H7	58	VDDiarm	P4	92	VDDiarm	V4
25	RDATA10	H2	59	VSSiarm	N2	93	VDDiarm	Y1
26	RDATA9	J8	60	VCLK/GPC1	M9	94	VSSiarm	Y2
27	RDATA8	H3	61	VLINE/GPC2	R4	95	VDD_LCD	W4
28	RDATA7	J4	62	VM/GPC4	N7	96	VSS_LCD	AA1
29	RDATA6	J3	63	VFRAME/GPC3	P3	97	VD19/GPD11	Y3
30	RDATA5	H1	64	LCDVF0/GPC5	N8	98	VD20/GPD12	Y4
31	VDD_SRAM	J2	65	LCDVF1/GPC6	P1	99	VD21/GPD13	AB1
32	VSS_SRAM	J9	66	LCDVF2/GPC7	N9	100	VD22/GPD14	AB2
33	RDATA4	K4	67	VD0/GPC8	P2	101	VD23/GPD15	AA2
34	RDATA3	J7	68	VDDiarm	T4	102	TOUT0/GPB0	AC1

Table 1-1. 400-Pin FBGA Pin Assignments – Pin Number Order (2/4)

Pin	Pin Name	Ball	Pin	Pin Name	Ball	Pin	Pin Name	Ball
103	TOUT1/GPB1	AC2	137	VSS_OP2	Y9	171	VSSi	Y15
104	TOUT2/GPB2	AB3	138	EINT20/GPG12/ nINPACK	R10	172	VDDi	T15
105	TOUT3/GPB3	AA3	139	EINT21/GPG13/ nREG_CF	AC10	173	SD0_CMD/GPL8	AB15
106	VDDiarm	AC3	140	EINT22/GPG14/ RESET_CF	T11	174	SD0_DAT[0]/GPL0	AC16
107	VSSiarm	AB4	141	EINT23/GPG15/ CF_PWREN	AA10	175	SD0_DAT[1]/GPL1	AA15
108	TCLK/GPB4	AA4	142	VDDiarm	AB11	176	SD0_DAT[2]/GPL2	U15
109	nXBACK/GPB5	AC4	143	VSSiarm	Y10	177	SD0_DAT[3]/GPL3	AA16
110	nXBREQ/GPB6	Y5	144	IICSCL/GPE14	U11	178	SD0_DAT[4]/GPL4	R15
111	VDD_OP2	AB5	145	IICSDA/GPE15	AC11	179	SD0_DAT[5]/GPL5	AB16
112	VSS_OP2	U7	146	I2SLRCK/GPE0/ AC_nRESET	AA11	180	SD0_DAT[6]/GPL6	U16
113	nXDACK1/GPB7	AC5	147	I2SSCLK/GPE1/ AC_SYNC	Y11	181	SD0_DAT[7]/GPL7	AC17
114	nXDREQ1/GPB8	AA5	148	I2SCDCLK/GPE2/ AC_BIT_CLK	R11	182	VDD_SD	AA17
115	nXDACK0/GPB9	AB6	149	I2SSDI/GPE3/ AC_SDI	AA12	183	VSS_SD	AB17
116	nXDREQ0/GPB10	U8	150	I2SSDO/GPE4/ AC_SDO	T12	184	SD1_CLK/GPE5/ AC_BIT_CLK	Y16
117	VDDiarm	Y6	151	SPIMISO0/GPE11	AC12	185	SD1_CMD/GPE6/ AC_SDI	AC18
118	VSSiarm	Y7	152	SPIMOSI0/GPE12	U12	186	SD1_DAT[0]/GPE7 /AC_SDO	Y17
119	EXTUARTCLK/ GPH12	AC6	153	SPICLK0/GPE13	AB12	187	SD1_DAT[1]/GPE8 /AC_SYNC	AB18
120	nCTS0/GPH8	AB7	154	VDDi	Y12	188	SD1_DAT[2]/GPE9 /AC_nRESET	AA18
121	nRTS0/GPH9	AA6	155	VSSi	Y13	189	SD1_DAT[3]/ GPE10	AC19
122	TXD0/GPH0	AC7	156	VSS_SD	R12	190	VSSA_MPLL	AB19
123	RXD0/GPH1	AA7	157	VDD_SD	AC13	191	MPLLCAP	Y18
124	nCTS1/GPH10	T9	158	TXD2/GPH4	T13	192	VDDA_MPLL	AC20
125	nRTS1/GPH11	AB8	159	RXD2/GPH5	AB13	193	VSSA_EPLL	AC21
126	TXD1/GPH2	U9	160	TXD3/GPH6/nRTS2	U13	194	EPLLCAP	AC22
127	RXD1/GPH3	AA8	161	RXD3/GPH7/nCTS2	AA13	195	VDDA_EPLL	AA19
128	EINT16/GPG8	R9	162	SS[1]/GPL14	R13	196	VSSA_ADC	AB20
129	EINT17/GPG9	AB9	163	SS[0]/GPL13	AC14	197	AIN9	AA20
130	VDDiarm	AC8	164	SPIMISO1/GPL12	Y14	198	AIN8	Y19
131	VSSiarm	Y8	165	SPIMOSI1/GPL11	AB14	199	AIN7	AC23
132	EINT18/GPG10	T10	166	SPICLK1/GPL10	T14	200	AIN6	AB21
133	EINT19/GPG11/ nIREQ_CF	AA9	167	SD0_nWP/GPJ15	AC15	201	AIN5	AB22
134	VDD_OP2	U10	168	SD0_nCD/GPJ14	U14	202	AIN4	AA22
135	CLKOUT0/GPH13	AC9	169	SD0_LED/GPJ13	AA14	203	AIN3	AB23
136	CLKOUT1/GPH14	AB10	170	SD0_CLK/GPL9	R14	204	AIN2	AA21

Table 1-1. 400-Pin FBGA Pin Assignments – Pin Number Order (3/4)

Pin	Pin Name	Ball	Pin	Pin Name	Ball	Pin	Pin Name	Ball
205	AIN1	AA23	239	TDI	P17	273	SDATA30	K15
206	AIN0	Y22	240	TCK	P20	274	SDATA29	H23
207	Vref	W20	241	nTRST	N15	275	SDATA28	J17
208	VDDA_ADC	Y21	242	EINT8/GPG0	N22	276	VDD_SDRAM	H20
209	VDD_RTC	Y23	243	EINT9/GPG1	N16	277	VSS_SDRAM	J16
210	Xtortc	V20	244	EINT10/GPG2	N23	278	SDATA27	H22
211	Xtirtc	W22	245	EINT11/GPG3	P21	279	SDATA26	H21
212	OM[4]	Y20	246	EINT12/GPG4/ LCD_PWREN	N20	280	VDDi	G23
213	OM[3]	U17	247	EINT13/GPG5	N17	281	VSSi	H17
214	OM[2]	W23	248	EINT14/GPG6	N21	282	SDATA25	G21
215	OM[1]	V23	249	EINT15/GPG7	M15	283	SDATA24	F21
216	OM[0]	V22	250	VDD_OP1	M20	284	SDATA23	G22
217	VDDi	T16	251	DP	M23	285	SDATA22	F23
218	VSSi	W21	252	DN	L23	286	SDATA21	E23
219	VSS_OP1	T17	253	VSS_OP1	M21	287	VDD_SDRAM	E20
220	EXTCLK	V21	254	nRSTOUT	M16	288	VSS_SDRAM	F22
221	VDD_OP1	U22	255	VDDalive	M22	289	SDATA20	F20
222	VDDalive	U20	256	VSSalive	M17	290	SDATA19	E21
223	XTIpll	R16	257	VDDalive	L20	291	SDATA18	G20
224	XTOpll	U23	258	XI_UDEV	L21	292	SDATA17	D23
225	VSSalive	U21	259	XO_UDEV	L15	293	SDATA16	E22
226	EINT0/GPF0	T22	260	VSSA33C	L22	294	SDATA15	D21
227	EINT1/GPF1	T20	261	VDDA33C	L16	295	SDATA14	C23
228	EINT2/GPF2	R17	262	REXT	K23	296	VDD_SDRAM	C22
229	EINT3/GPF3	T23	263	VDDA33T1	K20	297	VSS_SDRAM	D22
230	EINT4/GPF4	P15	264	VSSA33T2	K22	298	SDATA13	B23
231	EINT5/GPF5	R22	265	DM_UDEV	L17	299	SDATA12	A23
232	EINT6/GPF6	P16	266	VSSA33T2	K21	300	SDATA11	C21
233	EINT7/GPF7	T21	267	DP_UDEV	K17	301	SDATA10	B22
234	PWR_EN	R23	268	VSSA33T2	J20	302	SDATA9	B21
235	BATT_FLT	R20	269	VDDA33T1	K16	303	SDATA8	B20
236	NRESET	P22	270	VDDI_UDEV	J23	304	SDATA7	A22
237	TDO	P23	271	VSSI_UDEV	J21	305	SDATA6	A21
238	TMS	R21	272	SDATA31	J22	306	SDATA5	D20

Table 1-1. 400-Pin FBGA Pin Assignments – Pin Number Order (4/4)

Pin	Pin Name	Ball	Pin	Pin Name	Ball	Pin	Pin Name	Ball
307	VDD_SDRAM	C20	341	SADDR3	D15	375	RADDR14	B9
308	VSS_SDRAM	D19	342	SADDR4	B13	376	RADDR13	D8
309	SDATA4	A20	343	VDD_SDRAM	C13	377	RADDR12	A8
310	SDATA3	B19	344	VSS_SDRAM	J13	378	RADDR11	C8
311	VSSi	C19	345	SADDR5	A13	379	RADDR10	B8
312	VDDi	A19	346	SADDR6	H13	380	VDDi	H8
313	SDATA2	B18	347	SADDR7	D14	381	VSSi	D7
314	SDATA1	D18	348	SADDR8	G12	382	RADDR9	A7
315	SDATA0	C18	349	SADDR9	B12	383	RADDR8	C7
316	VDD_SDRAM	G17	350	SADDR10	C12	384	RADDR7	B7
317	VSS_SDRAM	A18	351	SADDR11	A12	385	RADDR6	A6
318	DQS1	B17	352	SADDR12	H12	386	RADDR5	G8
319	DQS0	C17	353	VDD_SDRAM	D13	387	VDD_SRAM	C6
320	DQM3	G16	354	VSS_SDRAM	J12	388	VSS_SRAM	G7
321	DQM2	C16	355	SADDR13	D12	389	RADDR4	B6
322	DQM1	H16	356	SADDR14	G11	390	RADDR3	A5
323	DQM0	A17	357	SADDR15	D11	391	RADDR2	B5
324	nSCS[0]	H15	358	VDDi	C11	392	RADDR1	D6
325	nSCS[1]	D17	359	VSSi	A11	393	RADDR0/GPA0	C5
326	nSWE	B16	360	nWE_CF/GPA15	B11	394	nRBE1	D5
327	VDD_SDRAM	C15	361	nOE_CF/GPA11	H11	395	nRBE0	A4
328	VSS_SDRAM	G15	362	RADDR25/RDATA_OEN	D10	396	nROE	B4
329	SCLK	A16	363	RADDR24/GPA9	C10	397	nRWE	A3
330	VDD_SDRAM	J15	364	RADDR23/GPA8	J11	398	nRCS0	A2
331	nSCLK	B15	365	RADDR22/GPA7	A10	399	nRCS1	A1
332	VSS_SDRAM	J14	366	RADDR21/GPA6	G10	400	nRCS2	B3
333	SCKE	A15	367	RADDR20/GPA5	B10			
334	VSSi	D16	368	VDD_SRAM	H10			
335	VDDi	B14	369	VSS_SRAM	D9			
336	nSRAS	G14	370	RADDR19/GPA4	J10			
337	nSCAS	C14	371	RADDR18/GPA3	C9			
338	SADDR0	H14	372	RADDR17/GPA2	G9			
339	SADDR1	A14	373	RADDR16/GPA1	A9			
340	SADDR2	G13	374	RADDR15	H9			

Table 1-2. S3C2443X 400-Pin FBGA Pin Assignments (Sheet 1 of 12,TBD)

Pin Number	Pin Name	Default Function	I/O State @Sleep	I/O State @nRESET	I/O Type
1	VDD_SRAM	VDD_SRAM	-	P	vdd33oph_hvt
2	RSMCLK/GPA13	RSMCLK	-/-	O(L)	pvbsdct16cdrt_hvt
3	VSS_SRAM	VSS_SRAM	-	P	vssoh_hvt
4	RSMVAD/GPA14	RSMVAD	-/-	O(H)	pvot16cdrt_hvt
5	RSMBWAIT/GPM0	RSMBWAIT	-/-	I	pvisudcrt_hvt
6	nRCS3	nRCS3	-	O(H)	pvot16cdrt_hvt
7	nRCS4	nRCS4	-	O(H)	pvot16cdrt_hvt
8	nRCS5/GPA12	nRCS5	-/-	O(H)	pvot16cdrt_hvt
9	nWAIT	nWAIT	-	I	pvisudcrt_hvt
10	FCLE	FCLE	-	O(L)	pvot16cdrt_hvt
11	FALE	FALE	-	O(L)	pvot16cdrt_hvt
12	VDDi	VDDi	-	P	vdd12ih_hvt
13	VSSi	VSSi	-	P	vssiph_hvt
14	nFWE	nFWE	-	O(H)	pvot16cdrt_hvt
15	nFRE	nFRE	-	O(H)	pvot16cdrt_hvt
16	nFCE	nFCE	-	O(H)	pvot16cdrt_hvt
17	FRnB/GPM1	FRnB	-	I	pvisudcrt_hvt
18	VDD_SRAM	VDD_SRAM	-	P	vdd33oph_hvt
19	VSS_SRAM	VSS_SRAM	-	P	vssoh_hvt
20	RDATA15	RDATA15	-	Hi-z	pvbsdct16cdrt_hvt
21	RDATA14	RDATA14	-	Hi-z	pvbsdct16cdrt_hvt
22	RDATA13	RDATA13	-	Hi-z	pvbsdct16cdrt_hvt
23	RDATA12	RDATA12	-	Hi-z	pvbsdct16cdrt_hvt
24	RDATA11	RDATA11	-	Hi-z	pvbsdct16cdrt_hvt
25	RDATA10	RDATA10	-	Hi-z	pvbsdct16cdrt_hvt
26	RDATA9	RDATA9	-	Hi-z	pvbsdct16cdrt_hvt
27	RDATA8	RDATA8	-	Hi-z	pvbsdct16cdrt_hvt
28	RDATA7	RDATA7	-	Hi-z	pvbsdct16cdrt_hvt
29	RDATA6	RDATA6	-	Hi-z	pvbsdct16cdrt_hvt
30	RDATA5	RDATA5	-	Hi-z	pvbsdct16cdrt_hvt
31	VDD_SRAM	VDD_SRAM	-	P	vdd33oph_hvt
32	VSS_SRAM	VSS_SRAM	-	P	vssoh_hvt
33	RDATA4	RDATA4	-	Hi-z	pvbsdct16cdrt_hvt
34	RDATA3	RDATA3	-	Hi-z	pvbsdct16cdrt_hvt

Table 1-2. S3C2443X 400-Pin FBGA Pin Assignments (Sheet 2 of 12) (Continued)

Pin Number	Pin Name	Default Function	I/O State @Sleep	I/O State @nRESET	I/O Type
35	RDATA2	RDATA2	-	Hi-z	pvbsdct16cdrt_hvt
36	RDATA1	RDATA1	-	Hi-z	pvbsdct16cdrt_hvt
37	RDATA0	RDATA0	-	Hi-z	pvbsdct16cdrt_hvt
38	CAMVSYNC/GPJ9	GPJ9	-/-	I	pvbsudct8smrt_hvt
39	CAMHREF/GPJ10	GPJ10	-/-	I	pvbsudct8smrt_hvt
40	VSSi	VSSi	-	P	vssiph_hvt
41	VDDi	VDDi	-	P	vdd12ih_hvt
42	CAMPCLK/GPJ8	GPJ8	-/-	I	pvbsudct8smrt_hvt
43	CAMDATA0/GPJ0	GPJ0	-/-	I	pvbsudct8smrt_hvt
44	CAMDATA1/GPJ1	GPJ1	-/-	I	pvbsudct8smrt_hvt
45	CAMDATA2/GPJ2	GPJ2	-/-	I	pvbsudct8smrt_hvt
46	CAMDATA3/GPJ3	GPJ3	-/-	I	pvbsudct8smrt_hvt
47	VDD_CAM	VDD_CAM	-	P	vdd33oph_hvt
48	VSS_CAM	VSS_CAM	-	P	vssoh_hvt
49	CAMDATA4/GPJ4	GPJ4	-/-	I	pvbsudct8smrt_hvt
50	CAMDATA5/GPJ5	GPJ5	-/-	I	pvbsudct8smrt_hvt
51	CAMDATA6/GPJ6	GPJ6	-/-	I	pvbsudct8smrt_hvt
52	CAMDATA7/GPJ7	GPJ7	-/-	I	pvbsudct8smrt_hvt
53	VDDiarm	VDDiarm	-	P	vdd12ih_core_hvt
54	VSSiarm	VSSiarm	-	P	vssiph_hvt
55	CAMPCLKOUT/GPJ11	GPJ11	-/-	I	pvbsudct8smrt_hvt
56	CAMRESET/GPJ12	GPJ12	-/-	I	pvbsudct8smrt_hvt
57	LEND/GPC0	GPC0	-/-	I	pvbsudct8smrt_hvt
58	VDDiarm	VDDiarm	-	P	vdd12ih_core_hvt
59	VSSiarm	VSSiarm	-	P	vssiph_hvt
60	VCLK/GPC1	GPC1	-/-	I	pvbsudct8smrt_hvt
61	VLINE/GPC2	GPC2	-/-	I	pvbsudct8smrt_hvt
62	VM/GPC4	GPC4	-/-	I	pvbsudct8smrt_hvt
63	VFRAME/GPC3	GPC3	-/-	I	pvbsudct8smrt_hvt
64	LCDVF0/GPC5	GPC5	-/-	I	pvbsudct8smrt_hvt
65	LCDVF1/GPC6	GPC6	-/-	I	pvbsudct8smrt_hvt
66	LCDVF2/GPC7	GPC7	-/-	I	pvbsudct8smrt_hvt
67	VD0/GPC8	GPC8	-/-	I	pvbsudct8smrt_hvt
68	VDDiarm	VDDiarm	-	P	vdd12ih_core_hvt

Table 1-2. S3C2443X 400-Pin FBGA Pin Assignments (Sheet 3 of 12) (Continued)

Pin Number	Pin Name	Default Function	I/O State @Sleep	I/O State @nRESET	I/O Type
69	VSSiarm	VSSiarm	-	P	vssiph_hvt
70	VD1/GPC9	GPC9	-/-	I	pvbsudct8smrt_hvt
71	VSS_LCD	VSS_LCD	-	P	vssoh_hvt
72	VDD_LCD	VDD_LCD	-	P	vdd33oph_hvt
73	VD2/GPC10	GPC10	-/-	I	pvbsudct8smrt_hvt
74	VD3/GPC11	GPC11	-/-	I	pvbsudct8smrt_hvt
75	VD4/GPC12	GPC12	-/-	I	pvbsudct8smrt_hvt
76	VD5/GPC13	GPC13	-/-	I	pvbsudct8smrt_hvt
77	VD6/GPC14	GPC14	-/-	I	pvbsudct8smrt_hvt
78	VD7/GPC15	GPC15	-/-	I	pvbsudct8smrt_hvt
79	VD8/GPD0	GPD0	-/-	I	pvbsudct8smrt_hvt
80	VD9/GPD1	GPD1	-/-	I	pvbsudct8smrt_hvt
81	VDDiarm	VDDiarm	-	P	vdd12ih_core_hvt
82	VSSiarm	VSSiarm	-	P	vssiph_hvt
83	VD10/GPD2	GPD2	-/-	I	pvbsudct8smrt_hvt
84	VD11/GPD3	GPD3	-/-	I	pvbsudct8smrt_hvt
85	VD12/GPD4	GPD4	-/-	I	pvbsudct8smrt_hvt
86	VD13/GPD5	GPD5	-/-	I	pvbsudct8smrt_hvt
87	VD14/GPD6	GPD6	-/-	I	pvbsudct8smrt_hvt
88	VD15/GPD7	GPD7	-/-	I	pvbsudct8smrt_hvt
89	VD16/GPD8	GPD8	-/-	I	pvbsudct8smrt_hvt
90	VD17/GPD9	GPD9	-/-	I	pvbsudct8smrt_hvt
91	VD18/GPD10	GPD10	-/-	I	pvbsudct8smrt_hvt
92	VDDiarm	VDDiarm	-	P	vdd12ih_core_hvt
93	VDDiarm	VDDiarm	-	P	vdd12ih_core_hvt
94	VSSiarm	VSSiarm	-	P	vssiph_hvt
95	VDD_LCD	VDD_LCD	-	P	vdd33oph_hvt
96	VSS_LCD	VSS_LCD	-	P	vssoh_hvt
97	VD19/GPD11	GPD11	-/-	I	pvbsudct8smrt_hvt
98	VD20/GPD12	GPD12	-/-	I	pvbsudct8smrt_hvt
99	VD21/GPD13	GPD13	-/-	I	pvbsudct8smrt_hvt
100	VD22/GPD14	GPD14	-/-	I	pvbsudct8smrt_hvt
101	VD23/GPD15	GPD15	-/-	I	pvbsudct8smrt_hvt
102	TOUT0/GPB0	GPB0	-/-	I	pvbsudct8smrt_hvt

Table 1-2. S3C2443X 400-Pin FBGA Pin Assignments (Sheet 4 of 12) (Continued)

Pin Number	Pin Name	Default Function	I/O State @Sleep	I/O State @nRESET	I/O Type
103	TOUT1/GPB1	GPB1	-/-	I	pvbsudct8smrt_hvt
104	TOUT2/GPB2	GPB2	-/-	I	pvbsudct8smrt_hvt
105	TOUT3/GPB3	GPB3	-/-	I	pvbsudct8smrt_hvt
106	VDDiarm	VDDiarm	-	P	vdd12ih_core_hvt
107	VSSiarm	VSSiarm	-	P	vssiph_hvt
108	TCLK/GPB4	GPB4	-/-	I	pvbsudct8smrt_hvt
109	nXBACK/GPB5	GPB5	-/-	I	pvbsudct8smrt_hvt
110	nXBREQ/BPG6	BPG6	-/-	I	pvbsudct8smrt_hvt
111	VDD_OP2	VDD_OP2	-	P	vdd33oph_hvt
112	VSS_OP2	VSS_OP2	-	P	vssoh_hvt
113	nXDACK1/GPB7	GPB7	-/-	I	pvbsudct8smrt_hvt
114	nXDREQ1/GPB8	GPB8	-/-	I	pvbsudct8smrt_hvt
115	nXDACK0/GPB9	GPB9	-/-	I	pvbsudct8smrt_hvt
116	nXDREQ0/GPB10	GPB10	-/-	I	pvbsudct8smrt_hvt
117	VDDiarm	VDDiarm	-	P	vdd12ih_core_hvt
118	VSSiarm	VSSiarm	-	P	vssiph_hvt
119	EXTUARTCLK/GPH12	GPH12	-/-	I	pvbsudct8smrt_hvt
120	nCTS0/GPH8	GPH8	-/-	I	pvbsudct8smrt_hvt
121	nRTS0/GPH9	GPH9	-/-	I	pvbsudct8smrt_hvt
122	TXD0/GPH0	GPH0	-/-	I	pvbsudct8smrt_hvt
123	RXD0/GPH1	GPH1	-/-	I	pvbsudct8smrt_hvt
124	nCTS1/GPH10	GPH10	-/-	I	pvbsudct8smrt_hvt
125	nRTS1/GPH11	GPH11	-/-	I	pvbsudct8smrt_hvt
126	TXD1/GPH2	GPH2	-/-	I	pvbsudct8smrt_hvt
127	RXD1/GPH3	GPH3	-/-	I	pvbsudct8smrt_hvt
128	EINT16/GPG8	GPG8	-/-	I	pvbsudct8smrt_hvt
129	EINT17/GPG9	GPG9	-/-	I	pvbsudct8smrt_hvt
130	VDDiarm	VDDiarm	-	P	vdd12ih_core_hvt
131	VSSiarm	VSSiarm	-	P	vssiph_hvt
132	EINT18/GPG10	GPG10	-/-	I	pvbsudct8smrt_hvt
133	EINT19/nIREQ_CF/GPG11	GPG11	-/-/-	I	pvbsudct8smrt_hvt
134	VDD_OP2	VDD_OP2	-	P	vdd33oph_hvt
135	CLKOUT0/GPH13	GPH13	-/-	I	pvbsudct8smrt_hvt
136	CLKOUT1/GPH14	GPH14	-/-	I	pvbsudct8smrt_hvt

Table 1-2. S3C2443X 400-Pin FBGA Pin Assignments (Sheet 5 of 12) (Continued)

Pin Number	Pin Name	Default Function	I/O State @Sleep	I/O State @nRESET	I/O Type
137	VSS_OP2	VSS_OP2	-	P	vssoh_hvt
138	EINT20/nINPACK/GPG12	GPG12	-/-/-	I	pvbsudct8smrt_hvt
139	EINT21/nREG_CF/GPG13	GPG13	-/-/-	I	pvbsudct8smrt_hvt
140	EINT22/RESET_CF/GPG14	GPG14	-/-/-	I	pvbsudct8smrt_hvt
141	EINT23/CF_PWREN/GPG15	GPG15	-/-/-	I	pvbsudct8smrt_hvt
142	VDDiarm	VDDiarm	-	P	vdd12ih_core_hvt
143	VSSiarm	VSSiarm	-	P	vssiph_hvt
144	IICSCL/GPE14	GPE14	-/-	I	pvbsudct8smrt_hvt
145	IICSDA/GPE15	GPE15	-/-	I	pvbsudct8smrt_hvt
146	I2SLRCK/GPE0/ AC_nRESET	GPE0	-/-/-	I	pvbsudct8smrt_hvt
147	I2SSCLK/GPE1/AC_SYNC	GPE1	-/-/-	I	pvbsudct8smrt_hvt
148	I2SCDCLK/GPE2/ AC_BIT_CLK0	GPE2	-/-/-	I	pvbsudct8smrt_hvt
149	I2SSDI/GPE3/AC_SDI0	GPE3	-/-/-	I	pvbsudct8smrt_hvt
150	I2SSDO/GPE4/AC_SDO0	GPE4	-/-/-	I	pvbsudct8smrt_hvt
151	SPIMISO0/GPE11	GPE11	-/-	I	pvbsudct8smrt_hvt
152	SPIMOSI0/GPE12	GPE12	-/-	I	pvbsudct8smrt_hvt
153	SPICLK0/GPE13	GPE13	-/-	I	pvbsudct8smrt_hvt
154	VDDi	VDDi	-	P	vdd12ih_hvt
155	VSSi	VSSi	-	P	vssiph_hvt
156	VSS_SD	VSS_SD	-	P	vssoh_hvt
157	VDD_SD	VDD_SD	-	P	vdd33oph_hvt
158	TXD2/GPH4	GPH4	-/-	I	pvbsudct8smrt_hvt
159	RXD2/GPH5	GPH5	-/-	I	pvbsudct8smrt_hvt
160	TXD3/GPH6/nRTS2	GPH6	-/-/-	I	pvbsudct8smrt_hvt
161	RXD3/GPH7/nCTS2	GPH7	-/-/-	I	pvbsudct8smrt_hvt
162	SS[1]/GPL14	GPL14	-/-	I	pvbsudct8smrt_hvt
163	SS[0]/GPL13	GPL13	-/-	I	pvbsudct8smrt_hvt
164	SPIMISO1/GPL12	GPL12	-/-	I	pvbsudct8smrt_hvt
165	SPIMOSI1/GPL11	GPL11	-/-	I	pvbsudct8smrt_hvt
166	SPICLK1/GPL10	GPL10	-/-	I	pvbsudct8smrt_hvt
167	SD0_nWP/GPJ15	GPJ15	-/-	I	pvbsudct8smrt_hvt
168	SD0_nCD/GPJ14	GPJ14	-/-	I	pvbsudct8smrt_hvt
169	SD0_LED/GPJ13	GPJ13	-/-	I	pvbsudct8smrt_hvt
170	SD0_CLK/GPL9	GPL9	-/-	I	pvbsudct8smrt_hvt

Table 1-2. S3C2443X 400-Pin FBGA Pin Assignments (Sheet 6 of 12) (Continued)

Pin Number	Pin Name	Default Function	I/O State @Sleep	I/O State @nRESET	I/O Type
171	VSSi	VSSi	-	P	vssiph_hvt
172	VDDi	VDDi	-	P	vdd12ih_hvt
173	SD0_CMD/GPL8	GPL8	-/-	I	pvbsudct8smrt_hvt
174	SD0_DAT[0]/GPL0	GPL0	-/-	I	pvbsudct8smrt_hvt
175	SD0_DAT[1]/GPL1	GPL1	-/-	I	pvbsudct8smrt_hvt
176	SD0_DAT[2]/GPL2	GPL2	-/-	I	pvbsudct8smrt_hvt
177	SD0_DAT[3]/GPL3	GPL3	-/-	I	pvbsudct8smrt_hvt
178	SD0_DAT[4]/GPL4	GPL4	-/-	I	pvbsudct8smrt_hvt
179	SD0_DAT[5]/GPL5	GPL5	-/-	I	pvbsudct8smrt_hvt
180	SD0_DAT[6]/GPL6	GPL6	-/-	I	pvbsudct8smrt_hvt
181	SD0_DAT[7]/GPL7	GPL7	-/-	I	pvbsudct8smrt_hvt
182	VDD_SD	VDD_SD	-	P	vdd33oph_hvt
183	VSS_SD	VSS_SD	-	P	vssoh_hvt
184	SD1_CLK/GPE5/AC_BIT_CLK	GPE5	-/-/-	I	pvbsudct8smrt_hvt
185	SD1_CMD/GPE6/AC_SDI	GPE6	-/-/-	I	pvbsudct8smrt_hvt
186	SD1_DAT[0]/GPE7/AC_SDO	GPE7	-/-/-	I	pvbsudct8smrt_hvt
187	SD1_DAT[1]/GPE8/ AC_SYNC	GPE8	-/-/-	I	pvbsudct8smrt_hvt
188	SD1_DAT[2]/GPE9/ AC_RESET	GPE9	-/-/-	I	pvbsudct8smrt_hvt
189	SD1_DAT[3]/GPE10	GPE10	-/-	I	pvbsudct8smrt_hvt
190	VSSA_MPLL	VSSA_MPLL	-	P	vssbb_abb
191	MPLLCAP	MPLLCAP	-	AI	poar50_pll_abb
192	VDDA_MPLL	VDDA_MPLL	-	P	vdd12t_abb
193	VSSA_EPLL	VSSA_EPLL	-	P	vssbb_abb
194	UPLLCAP	UPLLCAP	-	AI	poar50_pll_abb
195	VDDA_EPLL	VDDA_EPLL	-	P	vdd12t_abb
196	VSSA_ADC	VSSA_ADC	-	P	vssbbh_abb
197	AIN9(XP)	AIN9		AI	phiar10_abb
198	AIN8(XM)	AIN8	-	AI	phiar10_abb
199	AIN7(YP)	AIN7	-	AI	phiar10_abb
200	AIN6(YM)	AIN6	-	AI	phiar10_abb
201	AIN5	AIN5	-	AI	phiar10_abb
202	AIN4	AIN4	-	AI	phiar10_abb
203	AIN3	AIN3	-	AI	phiar10_abb
204	AIN2	AIN2	-	AI	phiar10_abb

Table 1-2. S3C2443X 400-Pin FBGA Pin Assignments (Sheet 7 of 12) (Continued)

Pin Number	Pin Name	Default Function	I/O State @Sleep	I/O State @nRESET	I/O Type
205	AIN1	AIN1	-	AI	phiar10_abb
206	AIN0	AIN0	-	AI	phiar10_abb
207	Vref	Vref	-	AI	phia_abb
208	VDDA_ADC	VDDA_ADC	-	P	vdd33th_abb
209	VDD_RTC	VDD_RTC	-	P	vdd30th_rtc
210	Xtortc	Xtortc	-	AO	rtc_osc
211	Xtirtc	Xtirtc	-	AI	rtc_osc
212	OM[4]	OM[4]	-	I	pvis_hvt
213	OM[3]	OM[3]	-	I	pvis_hvt
214	OM[2]	OM[2]	-	I	pvis_hvt
215	OM[1]	OM[1]	-	I	pvis_hvt
216	OM[0]	OM[0]	-	I	pvis_hvt
217	VDDi	VDDi	-	P	vdd12ih_hvt
218	VSSi	VSSi	-	P	vssiph_hvt
219	VSS_OP1	VSS_OP1	-	P	vssoh_hvt
220	EXTCLK	EXTCLK	-	I	pvis_hvt
221	VDD_OP1	VDD_OP1	-	P	vdd33oph_hvt
222	VDDalive	VDDalive	-	P	vdd12ih_hvt
223	XTIpll	XTIpll	-	AI	pvsoscm26_hvt
224	XTOpll	XTOpll	-	AO	pvsoscm26_hvt
225	VSSalive	VSSalive	-	P	vssiph_hvt
226	EINT0/GPF0	GPF0	-/-	I	pvbsudct8sm_hvt
227	EINT1/GPF1	GPF1	-/-	I	pvbsudct8sm_hvt
228	EINT2/GPF2	GPF2	-/-	I	pvbsudct8sm_hvt
229	EINT3/GPF3	GPF3	-/-	I	pvbsudct8sm_hvt
230	EINT4/GPF4	GPF4	-/-	I	pvbsudct8sm_hvt
231	EINT5/GPF5	GPF5	-/-	I	pvbsudct8sm_hvt
232	EINT6/GPF6	GPF6	-/-	I	pvbsudct8sm_hvt
233	EINT7/GPF7	GPF7	-/-	I	pvbsudct8sm_hvt
234	PWR_EN	PWR_EN	O(L)	O(H)	pvob8sm_hvt
235	BATT_FLT	BATT_FLT	-	I	pvis_hvt
236	nRESET	nRESET	-	I	pvis_hvt
237	TDO	TDO	-	O	pvot8sm_hvt
238	TMS	TMS	-	I	pvisu_hvt

Table 1-2. S3C2443X 400-Pin FBGA Pin Assignments (Sheet 8 of 12) (Continued)

Pin Number	Pin Name	Default Function	I/O State @Sleep	I/O State @nRESET	I/O Type
239	TDI	TDI	-	I	pvisu_hvt
240	TCK	TCK	-	I	pvisu_hvt
241	nTRST	nTRST	-	I	pvis_hvt
242	EINT8/GPG0	GPG0	-/-	I	pvbsudct8sm_hvt
243	EINT9/GPG1	GPG1	-/-	I	pvbsudct8sm_hvt
244	EINT10/GPG2	GPG2	-/-	I	pvbsudct8sm_hvt
245	EINT11/GPG3	GPG3	-/-	I	pvbsudct8sm_hvt
246	EINT12/GPG4/ LCD_PWREN	GPG4	-/-/-	I	pvbsudct8sm_hvt
247	EINT13/GPG5	GPG5	-/-	I	pvbsudct8sm_hvt
248	EINT14/GPG6	GPG6	-/-	I	pvbsudct8sm_hvt
249	EINT15/GPG7	GPG7	-/-	I	pvbsudct8sm_hvt
250	VDD_OP1	VDD_OP1	-	P	vdd33oph_hvt
251	DP	DP	-	AI	pbusb1
252	DN	DN	-	AI	pbusb1
253	VSS_OP1	VSS_OP1	-	P	vssoh_hvt
254	nRSTOUT	nRSTOUT	O(H)	O(L)	pvob8sm_hvt
255	VDDalive	VDDalive	-	P	vdd12ih_hvt
256	VSSalive	VSSalive	-	P	vssiph_hvt
257	VDDalive	VDDalive	-	P	vdd12ih_core_hvt
258	XI_UDEV	XI_UDEV	-	I	phia_abb
259	XO_UDEV	XO_UDEV	-	I	phia_abb
260	VSSA33C	VSSA33C	-	P	vssbbh_abb
261	VDDA33C	VDDA33C	-	P	vdd33th_abb
262	REXT	REXT	-		phoarext_abb
263	VDDA33T1	VDDA33T1	-	P	vdd33th_abb
264	VSSA33T2	VSSA33T2	-	P	vssbbh_abb
265	DM_UDEV	DM_UDEV		Hi-z	phtoa_abb
266	VSSA33T2	VSSA33T2	-	P	vssbbh_abb
267	DP_UDEV	DP_UDEV	-	Hi-z	phtoa_abb
268	VSSA33T2	VSSA33T2	-	P	vssbbh_abb
269	VDDA33T1	VDDA33T1	-	P	vdd33th_abb
270	VDDI_UDEV	VDDI_UDEV	-	P	vdd12ih_core_hvt
271	VSSI_UDEV	VSSIP_UDEV	-	P	vssiph_hvt
272	SDATA31	SDATA31	-	Hi-z	phnbsud100ct12cd_ddrret

Table 1-2. S3C2443X 400-Pin FBGA Pin Assignments (Sheet 9 of 12) (Continued)

Pin Number	Pin Name	Default Function	I/O State @Sleep	I/O State @nRESET	I/O Type
273	SDATA30	SDATA30	-	Hi-z	phnbsud100ct12cd_ddrret
274	SDATA29	SDATA29	-	Hi-z	phnbsud100ct12cd_ddrret
275	SDATA28	SDATA28	-	Hi-z	phnbsud100ct12cd_ddrret
276	VDD_SDRAM	VDD_SDRAM	-	P	vdd18op_ddr
277	VSS_SDRAM	VSS_SDRAM	-	P	vsso_ddr
278	SDATA27	SDATA27	-	Hi-z	phnbsud100ct12cd_ddrret
279	SDATA26	SDATA26	-	Hi-z	phnbsud100ct12cd_ddrret
280	VDDi	VDDi	-	P	vdd12i_ddr
281	VSSi	VSSi	-	P	vssip_ddr
282	SDATA25	SDATA25	-	Hi-z	phnbsud100ct12cd_ddrret
283	SDATA24	SDATA24	-	Hi-z	phnbsud100ct12cd_ddrret
284	SDATA23	SDATA23	-	Hi-z	phnbsud100ct12cd_ddrret
285	SDATA22	SDATA22	-	Hi-z	phnbsud100ct12cd_ddrret
286	SDATA21	SDATA21	-	Hi-z	phnbsud100ct12cd_ddrret
287	VDD_SDRAM	VDD_SDRAM	-	P	vdd18op_ddr
288	VSS_SDRAM	VSS_SDRAM	-	P	vsso_ddr
289	SDATA20	SDATA20	-	Hi-z	phnbsud100ct12cd_ddrret
290	SDATA19	SDATA19	-	Hi-z	phnbsud100ct12cd_ddrret
291	SDATA18	SDATA18	-	Hi-z	phnbsud100ct12cd_ddrret
292	SDATA17	SDATA17	-	Hi-z	phnbsud100ct12cd_ddrret
293	SDATA16	SDATA16	-	Hi-z	phnbsud100ct12cd_ddrret
294	SDATA15	SDATA15	-	Hi-z	phnbsud100ct12cd_ddrret
295	SDATA14	SDATA14	-	Hi-z	phnbsud100ct12cd_ddrret
296	VDD_SDRAM	VDD_SDRAM	-	Hi-z	vdd18op_ddr
297	VSS_SDRAM	VSS_SDRAM	-	Hi-z	vsso_ddr
298	SDATA13	SDATA13	-	Hi-z	phnbsud100ct12cd_ddrret
299	SDATA12	SDATA12	-	Hi-z	phnbsud100ct12cd_ddrret
300	SDATA11	SDATA11	-	Hi-z	phnbsud100ct12cd_ddrret
301	SDATA10	SDATA10	-	Hi-z	phnbsud100ct12cd_ddrret
302	SDATA9	SDATA9	-	Hi-z	phnbsud100ct12cd_ddrret
303	SDATA8	SDATA8	-	Hi-z	phnbsud100ct12cd_ddrret
304	SDATA7	SDATA7	-	Hi-z	phnbsud100ct12cd_ddrret
305	SDATA6	SDATA6	-	Hi-z	phnbsud100ct12cd_ddrret
306	SDATA5	SDATA5	-	Hi-z	phnbsud100ct12cd_ddrret

Table 1-2. S3C2443X 400-Pin FBGA Pin Assignments (Sheet 10 of 12) (Continued)

Pin Number	Pin Name	Default Function	I/O State @Sleep	I/O State @nRESET	I/O Type
307	VDD_SDRAM	VDD_SDRAM	-	P	vdd18op_ddr
308	VSS_SDRAM	VSS_SDRAM	-	P	vsso_ddr
309	SDATA4	SDATA4	-	Hi-z	phnbsud100ct12cd_ddrret
310	SDATA3	SDATA3	-	Hi-z	phnbsud100ct12cd_ddrret
311	VSSi	VSSi	-	P	vssip_ddr
312	VDDi	VDDi	-	P	vdd12i_ddr
313	SDATA2	SDATA2	-	Hi-z	phnbsud100ct12cd_ddrret
314	SDATA1	SDATA1	-	Hi-z	phnbsud100ct12cd_ddrret
315	SDATA0	SDATA0	-	Hi-z	phnbsud100ct12cd_ddrret
316	VDD_SDRAM	VDD_SDRAM	-	P	vdd18op_ddr
317	VSS_SDRAM	VSS_SDRAM	-	P	vsso_ddr
318	DQS1	DQS1	O(L)	Hi-z	phnbsud100ct12cd_ddrret
319	DQS0	DQS0	O(L)	Hi-z	phnbsud100ct12cd_ddrret
320	DQM3	DQM3	O(H)-	O(L)	phnot12cd_ddrret
321	DQM2	DQM2	O(H)	O(L)	phnot12cd_ddrret
322	DQM1	DQM1	O(H)	O(L)	phnot12cd_ddrret
323	DQM0	DQM0	O(H)	O(L)	phnot12cd_ddrret
324	nSCS[0]	nSCS[0]	O(H)	O(H)	phnot12cd_ddrret
325	nSCS[1]	nSCS[1]	O(H)	O(H)	phnot12cd_ddrret
326	nSWE	nSWE	O(H)	O(H)	phnot12cd_ddrret
327	VDD_SDRAM	VDD_SDRAM	-	P	vdd18op_ddr
328	VSS_SDRAM	VSS_SDRAM	-	P	vsso_ddr
329	SCLK	SCLK	O(L)	O(SCLK)	phnbsud100ct12cd_ddrret
330	VDD_SDRAM	VDD_SDRAM	-	P	vdd18op_ddr
331	nSCLK	nSCLK	O(H)	O(nSCLK)	phnot12cd_ddrret
332	VSS_SDRAM	VSS_SDRAM		P	vsso_ddr
333	SCKE	SCKE	O(L)	O(L)	phnoud100ct12cd_ddrret
334	VSSi	VSSi	-	P	vssip_ddr
335	VDDi	VDDi	-	P	vdd12i_ddr
336	nSRAS	nSRAS	O(H)	O(H)	phnot12cd_ddrret
337	nSCAS	nSCAS	O(H)	O(H)	phnot12cd_ddrret
338	SADDR0	SADDR0	-	O(L)	phnot12cd_ddrret
339	SADDR1	SADDR1	-	O(L)	phnot12cd_ddrret
340	SADDR2	SADDR2	-	O(L)	phnot12cd_ddrret

Table 1-2. S3C2443X 400-Pin FBGA Pin Assignments (Sheet 11 of 12) (Continued)

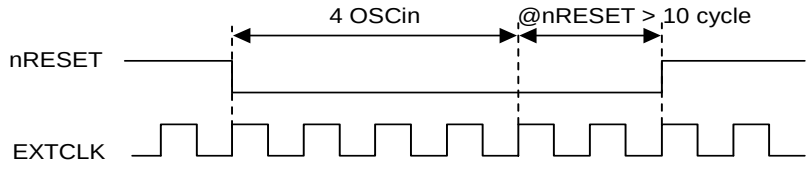
Pin Number	Pin Name	Default Function	I/O State @Sleep	I/O State @nRESET	I/O Type
341	SADDR3	SADDR3	-	O(L)	phnot12cd_ddrret
342	SADDR4	SADDR4	-	O(L)	phnot12cd_ddrret
343	VDD_SDRAM	VDD_SDRAM	-	P	vdd18op_ddr
344	VSS_SDRAM	VSS_SDRAM	-	P	vsso_ddr
345	SADDR5	SADDR5	-	O(L)	phnot12cd_ddrret
346	SADDR6	SADDR6	-	O(L)	phnot12cd_ddrret
347	SADDR7	SADDR7	-	O(L)	phnot12cd_ddrret
348	SADDR8	SADDR8	-	O(L)	phnot12cd_ddrret
349	SADDR9	SADDR9	-	O(L)	phnot12cd_ddrret
350	SADDR10	SADDR10	-	O(L)	phnot12cd_ddrret
351	SADDR11	SADDR11	-	O(L)	phnot12cd_ddrret
352	SADDR12	SADDR12	-	O(L)	phnot12cd_ddrret
353	VDD_SDRAM	VDD_SDRAM	-	P	vdd18op_ddr
354	VSS_SDRAM	VSS_SDRAM	-	P	vsso_ddr
355	SADDR13	SADDR13	-	O(L)	phnot12cd_ddrret
356	SADDR14	SADDR14	-	O(L)	phnot12cd_ddrret
357	SADDR15	SADDR15	-	O(L)	phnot12cd_ddrret
358	VDDi	VDDi	-	P	vdd12i_ddr
359	VSSi	VSSi	-	P	vssip_ddr
360	nWE_CF/GPA15	nWE_CF	-/-	O(H)	pvot16cdrt_hvt
361	nOE_CF/GPA11	nOE_CF	-/-	O(H)	pvot16cdrt_hvt
362	RADDR25/RDATA_OEN	RADDR25	-/-	O(L)	pvot16cdrt_hvt
363	RADDR24/GPA9	RADDR24	-/-	O(L)	pvot16cdrt_hvt
364	RADDR23/GPA8	RADDR23	-/-	O(L)	pvot16cdrt_hvt
365	RADDR22/GPA7	RADDR22	-/-	O(L)	pvot16cdrt_hvt
366	RADDR21/GPA6	RADDR21	-/-	O(L)	pvot16cdrt_hvt
367	RADDR20/GPA5	RADDR20	-/-	O(L)	pvot16cdrt_hvt
368	VDD_SRAM	VDD_SRAM	-	P	vdd33oph_hvt
369	VSS_SRAM	VSS_SRAM	-	P	vssoh_hvt
370	RADDR19/GPA4	RADDR19	-/-	O(L)	pvot16cdrt_hvt
371	RADDR18/GPA3	RADDR18	-/-	O(L)	pvot16cdrt_hvt
372	RADDR17/GPA2	RADDR17	-/-	O(L)	pvot16cdrt_hvt
373	RADDR16/GPA1	RADDR16	-/-	O(L)	pvot16cdrt_hvt
374	RADDR15	RADDR15	-/-	O(L)	pvot16cdrt_hvt

Table 1-2. S3C2443X 400-Pin FBGA Pin Assignments (Sheet 12 of 12) (Continued)

Pin Number	Pin Name	Default Function	I/O State @Sleep	I/O State @nRESET	I/O Type
375	RADDR14	RADDR14	-	O(L)	pvot16cdrt_hvt
376	RADDR13	RADDR13	-	O(L)	pvot16cdrt_hvt
377	RADDR12	RADDR12	-	O(L)	pvot16cdrt_hvt
378	RADDR11	RADDR11	-	O(L)	pvot16cdrt_hvt
379	RADDR10	RADDR10	-	O(L)	pvot16cdrt_hvt
380	VDDi	VDDi	-	P	vdd12ih_hvt
381	VSSi	VSSi	-	P	vssiph_hvt
382	RADDR9	RADDR9	-	O(L)	pvot16cdrt_hvt
383	RADDR8	RADDR8	-	O(L)	pvot16cdrt_hvt
384	RADDR7	RADDR7	-	O(L)	pvot16cdrt_hvt
385	RADDR6	RADDR6	-	O(L)	pvot16cdrt_hvt
386	RADDR5	RADDR5	-	O(L)	pvot16cdrt_hvt
387	VDD_SRAM	VDD_SRAM	-	P	vdd33oph_hvt
388	VSS_SRAM	VSS_SRAM	-	P	vssoh_hvt
389	RADDR4	RADDR4	-	O(L)	pvot16cdrt_vt
390	RADDR3	RADDR3	-	O(L)	pvot16cdrt_hvt
391	RADDR2	RADDR2	-	O(L)	pvot16cdrt_hvt
392	RADDR1	RADDR1	-	O(L)	pvot16cdrt_hvt
393	RADDR0/GPA0	RADDR0	-/-	O(L)	pvot16cdrt_hvt
394	nRBE1	nRBE1	-	O(H)	pvot16cdrt_hvt
395	nRBE0	nRBE0	-	O(H)	pvot16cdrt_hvt
396	nROE	nROE	-	O(H)	pvot16cdrt_hvt
397	nRWE	nRWE	-	O(H)	pvot16cdrt_hvt
398	nRCS0	nRCS0	-	O(H)	pvot16cdrt_hvt
399	nRCS1	nRCS1	-	O(H)	pvot16cdrt_hvt
400	nRCS2	nRCS2	-	O(H)	pvot16cdrt_hvt

NOTES:

1. The @BUS REQ. shows the pin state at the external bus, which is used by the other bus master.
2. ' – ' mark indicates the unchanged pin state at Bus Request mode.
3. Hi-z or Pre means Hi-z or early state and it is determined by the setting of MISCCR register.
4. AI/AO means analog input/analog output.
5. P, I, and O mean power, input and output respectively.
6. The I/O state @nRESET shows the pin status in the @nRESET duration below.



THE TABLE BELOW SHOWS I/O TYPES AND DESCRIPTIONS

IO Type	Description
vdd33oph_hvt	Power for IO(1.8V/2.5V/3.3V)
pvbsdct16cdrt_hvt	1.8V/2.5V/3.3V interface, bi-directional, schmitt triggered, pull-down controllerable, tri-state, retention(4/8/12/16m driver controllable)
vssoh_hvt	Ground for IO
pvot16cdrt_hvt	1.8V/2.5V/3.3V interface, output, tri-state, retention(4/8/12/16m driver controllable)
pvisudcrt_hvt	1.8V/2.5V/3.3V interface, input, schmitt triggered, pull-up/pull-down controllable, retention
vdd12ih_hvt	Power for internal logic(1.2V)
vssiph_hvt	Ground for internal logic
pvbsudct8smrt_hvt	1.8V/2.5V/3.3V interface, bi-directional, schmitt triggered, pull-up/pull-down controllable, tri-state, retention(8m driver)
vdd12ih_core_hvt	Power for internal logic(1.2V)
vssbb_abb	Ground for analog circuit
poar50_pll_abb	1.2V interface, output, analog for PMPLLCAP/PEPLLCAP
vdd12t_abb	Power for analog circuit(1.2V)
vssbbh_abb	Ground for analog circuit
phiar10_abb	3.3V interface, input, analog for AIN[9:0]
phia_abb	3.3V interface, input, analog for Vref
vdd33th_abb	Power for analog circuit(3.3V)
vdd30th_rtc	Power for rtc circuit(3.0V)
rtc_osc	3.0V interface, Oscillator for RTC
pvis_hvt	2.5V/3.3V interface, input, Schmitt triggered
pvsoscm26_hvt	2.5V/3.3V interface, oscillator, Schmitt triggered,
pvbsudct8sm_hvt	1.8V/2.5V/3.3V interface, bi-directional, schmitt triggered, pull-up/pull-down controllable, tri-state(8m driver)
pvob8sm_hvt	2.5V/3.3V interface, output, normal buffer
pvot8sm_hvt	2.5V/3.3V interface, output, tri-state buffer
pvisu_hvt	2.5V/3.3V interface, input, Schmitt triggered, pull-up
pbusb1	USB host Pad (DP/DN)
phoa_abb	3.3V interface, output, analog for
phoarext_abb	3.3V interface, output, analog for REXT

phtoa_abb	USB 3.3V interface, bi-directional, alalog for DP_UDEV, DM_UDEV
phnbsud100ct12cd_ddrret	1.8V/2.5V/3.3V interface, bi-directional, Schmitt triggered, tri-state, retention(6/8/10/12m driver controllable)
vdd18op_ddr	1.8V/2.5V/3.3V IO Power for DRAM Interface
vsso_ddr	IO Ground for DRAM Interface
vdd12i_ddr	1.2V Power for internal logic
vssip_ddr	Ground for Internal logic
phnot12cd_ddrret	1.8V/2.5V/3.3V interface, output, tri-state, retention(6/8/10/12m driver controllable)

SIGNAL DESCRIPTIONS

Table 1-3. S3C2443X Signal Descriptions

Signal	In/Out	Description
Reset, Clock & Power		
XTIpll	AI	Crystal input signals for internal osc circuit. When OM[0] = 0, XTIpll is used for MPLL CLK source and EPLL CLK source. If it isn't used, it has to be Low (0V)
XTOpll	AO	Crystal output signals for internal osc circuit. When OM[0] = 0, XTIpll is used for MPLL CLK source and EPLL CLK source. If it isn't used, it has to be float
MPLLCAP	AI	Loop filter capacitor for Main PLL.
EPLLCAP	AI	Loop filter capacitor for Extra PLL
XTIrtc	AI	32.768 kHz crystal input for RTC. If it isn't used, it has to be High (VDD_RTC=3.3V).
XTOrtc	AO	32.768 kHz crystal output for RTC. If it isn't used, it has to be float.
CLKOUT[1:0]	O	Clock output signal. The CLKSEL of MISCCR(GPIO register) register configures the clock output mode among the MPLL_CLK, EPLL CLK, ARMCLK, HCLK, PCLK.
nRESET	ST	nRESET suspends any operation in progress and places S3C2443X into a known reset state. For a reset, nRESET must be held to L level for at least 4 OSCin after the processor power has been stabilized.
nRSTOUT	O	For external device reset control (nRSTOUT = nRESET & nWDTRST & SW_RESET) *SW_RESET = nRSTCON of GPIO MISCCR
PWREN	O	core power on-off control signal
nBATT_FLT	I	Probe for battery state (Does not wake up at Sleep mode in case of low battery state). If it isn't used, it has to be High (3.3V).
OM[4:0]	I	OM[4:0] set operating modes of S3C2443X Refer to "**S3C2443 OPERATION MODE DESCRIPTION TABLE**"
EXTCLK	I	External clock source. When OM[0] = 1, EXTCLK is used for MPLL and EPLL CLK source. If it isn't used, it has to be Low (0V).
Memory Interface (ROM/SRAM/NAND/CF)		
RADDR[25:0]	O	RADDR[25:0] (Address Bus) outputs the memory address of the corresponding bank .
RDATA[15:0]	IO	RDATA[15:0] (Data Bus) inputs data during memory read and outputs data during memory write. The bus width is programmable among 8/16-bit.
nRCS[5:0]	O	nRCS[5:0] (Chip Select) are activated when the address of a memory is within the address region of each bank. The number of access cycles and the bank size can be programmed.
nRWE	O	nRWE (Write Enable) indicates that the current bus cycle is a write cycle.
nROE	O	nOE (Output Enable) indicates that the current bus cycle is a read cycle.
nRBE[1:0]	O	Upper byte/lower byte enable (In case of 16-bit SRAM)
nWAIT	I	nWAIT requests to prolong a current bus cycle. As long as nWAIT is L, the current bus cycle cannot be completed. If nWAIT signal isn't used in your system, nWAIT signal must be tied on pull-up resistor.

Signal	In/Out	Description
SDRAM I/F		
SADDR[15:0]	O	SDRAM/DDR Address bus
SDATA[31:0]	IO	SDRAM/DDR Data Bus
nSRAS	O	SDRAM/DDR row address strobe
nSCAS	O	SDRAM/DDRcolumn address strobe
nSCS[1:0]	O	SDRAM/DDR chip select
DQM[3:0]	O	SDRAM/DDR data mask
DQS[1:0]	O	DDR Data Strobe
SCLK	O	SDRAM/DDR clock
nSCLK	O	DDR Conversion clock
SCKE	O	SDRAM/DDR clock enable
NAND Flash		
FCLE	O	Command latch enable
FALE	O	Address latch enable
nFCE	O	Nand flash chip enable
nFRE	O	Nand flash read enable
nFWE	O	Nand flash write enable
FRnB	I	Nand flash ready/busy
SMC/OneNAND		
RSMCLK	I/O	SMC Clock
RSMVAD	O	SMC Address Valid
RSMBWAIT	O	SMC Burst Wait
CF I/F		
nOE_CF	O	CF Output Enable Strobe
nWE_CF	O	CF Write Enable Strobe
nIREQ_CF	I	Interrupt request from CF card
nINPACK_CF	I	Input acknowledge in I/O mode
CardPWR_CF	O	Card Power Enable
nREG_CF	O	Register in CF card strobe
RESET_CF	O	CF card reset

Signal	In/Out	Description
LCD Control Unit		
VD[23:0]	O	**STN/TFT/SEC TFT:** LCD data bus
LCD_PWREN	O	**STN/TFT/SEC TFT:** LCD panel power enable control signal
VCLK	O	**STN/TFT:** LCD clock signal
VFRAME	O	**STN:** VFRAM signal **TFT:** VSYNC signal
VLINE	O	**STN:** VLINE signal **TFT:** HSYNC signal
VM	O	**STN:** VM alternates the polarity of the row and column voltage **TFT:** VDEN enable data signals
LEND	O	**TFT:** Line end signal
LCDVF[2:0]	O	**SEC TFT:** Timing control signal for specific TFT LCD(OE/REV/REVB)
CAMERA Interface		
CAMRESET	O	Camera interface reset
CAMCLKOUT	O	Camera interface master clock
CAMPCLK	I	Camera interface pixel clock
CAMHREF	I	Camera interface horizontal sync
CAMVSYNC	I	Camera interface horizontal sync
CAMDATA[7:0]	I	Camera interface data
Interrupt Control Unit		
EINT[23:0]	I	External interrupt request
External I/F		
nXDREQ[1:0]	I	External DMA request
nXDACK[1:0]	O	External DMA acknowledge
nXBREQ	I	nXBREQ (Bus Hold Request) allows another bus master to request control of the local bus. nXBACK active indicates that bus control has been granted.
nXBACK	O	nXBACK (Bus Hold Acknowledge) indicates that the S3C2443X has surrendered control of the local bus to another bus master.
UART		
RXD[3:0]	I	UART receives data input (ch. 0/1/2)
TXD[3:0]	O	UART transmits data output (ch. 0/1/2)
nCTS[2:0]	I	UART clear to send input signal (ch. 0/1)
nRTS[2:0]	O	UART request to send output signal (ch. 0/1)
EXTUARTCLK	I	External clock input for UART

Signal	In/Out	Description
TSADC		
AIN[9:0]	AI	ADC input[9:0]. If it isn't used pin, it has to be low (ground). When touch screen device is used, A[6], A[7] , A[8] and A[9] are used as YM, YP, XM and XP, respectively.
Vref	AI	ADC Vref
IIC-Bus		
IICSDA	IO	IIC-bus data
IICSCL	IO	IIC-bus clock
IIS-Bus		
I2SLRCK	IO	IIS-bus channel select clock
I2SSCLK	IO	IIS-bus serial clock
I2SCDCLK	O	CODEC system clock
I2SSDI	I	IIS-bus serial data input
I2SSDO	O	IIS-bus serial data output
AC'97		
AC_nRESET	IO	AC'97 Master H/W Reset
AC_SYNC	IO	12.288MHz serial data clock
AC_BIT_CLK0	O	48kHz fixed rate sample sync
AC_SDI0	I	Serial, time division multiplexed, AC'97 input stream
AC_SDO0	O	Serial, time division multiplexed, AC'97 output stream
USB Host		
DN	IO	DATA(–) from USB host. (Need to 15kΩ pull-down)
DP	IO	DATA(+) from USB host. (Need to 15kΩ pull-down)
USB Device		
DM_UDEV	IO	DATA(–) for USB peripheral.
DP_UDEV	IO	DATA(+) for USB peripheral.
REXT	O	External Resist (3.4Kohm +/- 1%)
XO_UDEV	OSC	Crystal output
XI_UDEV	OSC	Crystal input

Signal	In/Out	Description
SPI		
SPIMISO[1:0]	IO	SPIMISO is the master data input line, when SPI is configured as a master. When SPI is configured as a slave, these pins reverse its role. * SPIMISO[0] is for the High Speed SPI Interface.
SPIMOSI[1:0]	IO	SPIMOSI is the master data output line, when SPI is configured as a master. When SPI is configured as a slave, these pins reverse its role. * SPIMOSI[0] is for the High Speed SPI Interface.
SPICLK[1:0]	IO	SPI clock * SPICLK[0] is for the High Speed SPI Interface.
nSS[1:0]	I	SPI chip select (only for slave mode) *nSS[0] is for the High Speed SPI Interface.
SDMMC Interface		
SD0_DAT[7:0]	IO	SD0 receive/transmit data
SD0_CMD	IO	SD0 receive response/ transmit command
SD0_CLK	O	SD0 clock
SD0_nWP	O	SD0 Write Protect
SD0_nCD	O	SD0 Card Detect
SD0_nLED	O	SD0 LED
SD1_DAT[3:0]	IO	SD1 receive/transmit data
SD1_CMD	IO	SD1 receive response/ transmit command
SD1_CLK	O	SD1 clock
General Port		
GPn[147:0]	IO	General input/output ports, which are multiplexed with other function pins (some ports are output only).
TIMMER/PWM		
TOUT[3:0]	O	Timer output[3:0]
TCLK	I	External timer clock input
JTAG TEST LOGIC		
nTRST	I	nTRST (TAP Controller Reset) resets the TAP controller at start. If debugger is used, A 10K pull-up resistor has to be connected. If debugger (black ICE) is not used, nTRST pin must be issued by a low active pulse (Typically connected to nRESET).
TMS	I	TMS (TAP Controller Mode Select) controls the sequence of the TAP controller's states.
TCK	I	TCK (TAP Controller Clock) provides the clock input for the JTAG logic.
TDI	I	TDI (TAP Controller Data Input) is the serial input for test instructions and data.
TDO	O	TDO (TAP Controller Data Output) is the serial output for test instructions and data.

Signal	In/Out	Description
Power		
VDDalive	P	S3C2443X reset block and port status register VDD. It should be always supplied whether in normal mode or in Sleep mode.
VDDiarm	P	S3C2443X core logic VDD for ARM core.
VDDi	P	S3C2443X core logic VDD for Internal block.
VSSi/VSSiarm	P	S3C2443X core logic VSS
VDDA_MPLL	P	S3C2443X MPLL analog and digital VDD.
VSSA_MPLL	P	S3C2443X MPLL analog and digital VSS.
VDD_RTC	P	RTC VDD (3.0V, Input range: 2.5 ~ 3.6V) This pin must be connected to power properly if RTC isn't used.
VDDA_EPLL	P	S3C2443X EPLL analog and digital VDD
VSSA_EPLL	G	S3C2443X EPLL analog and digital VSS
VDD_OP1	P	S3C2443X System I/O Power (2.5 ~ 3.3V)
VDD_OP2	P	S3C2443X System I/O Power 2 (1.8 ~ 3.3V)
VDD_CAM	P	S3C2443X Camera I/O Power (1.8 ~ 3.3V)
VDD_LCD	P	S3C2443X LCD I/O Power (2.5 ~ 3.3V)
VDD_SD	P	S3C2443X SD/MMC I/O Power (1.8 ~ 3.3V)
VDD_SDRAM	P	S3C2443X SDRAM/DDR I/O Power (1.8V/ 2.5V/ 3.3V)
VDD_SRAM	P	S3C2443X ROM/SRAM I/O Power
VSS_OP1	G	S3C2443X System I/O Ground
VSS_OP2	G	S3C2443X System I/O Ground
VSS_CAM	G	S3C2443X Camera I/O Ground
VSS_LCD	G	S3C2443X LCD I/O Ground
VSS_SD	G	S3C2443X SD/MMC I/O Ground
VSS_SDRAM	G	S3C2443X SDRAM/DDR I/O Ground
VSS_SRAM	G	S3C2443X ROM/SRAM I/O Ground
VDDA_ADC	P	S3C2443X ADC VDD(3.3V)
VSSA_ADC	P	S3C2443X ADC VSS
VDDI_UDEV	P	USB 2.0 Phy Power (1.2V)
VSSI_UDEV	G	USB 2.0 Phy Ground
VDDA33C/VDDA33T1	P	USB 2.0 Phy Power (3.3V)
VSSA33C/VSSA33T2	G	USB 2.0 Phy Ground

NOTES:

1. I/O means Input/Output.
2. AI/AO means analog input/analog output.
3. ST means schmitt-trigger.
4. P means power.

S3C2443X OPERATION MODE DESCRIPTION

Table 1-4. S3C2443X Operation Mode Description

OM[4]	OM[3]	OM[2]	OM[1]	OM[0]	OM[4]	OM[3]	OM[2]	OM[1]	OM[0]	Operation Mode
0	0	0	0	0	NAND	Advanced	-	addr(4)	OSC	NAND
				1					EXT	
			1	0				addr(5)	OSC	
				1					EXT	
		1	0	0			page(2K)	addr(4)	OSC	
				1					EXT	
			1	0				addr(5)	OSC	
				1					EXT	
	1	0	0	0		Normal	-	addr(3)	OSC	
				1					EXT	
			1	0				addr(4)	OSC	
				1					EXT	
		1	0	0			page(512)	addr(3)	OSC	
				1					EXT	
			1	0				addr(4)	OSC	
				1					EXT	
1	0	0	0	0	OneNAND/ ROM		One NAND	16-bit	OSC	OneNAND (Muxed)
				1					EXT	
			1	0					OSC	
				1					EXT	
		1	0	0			ROM	8-bit	OSC	ROM/ OneNAND (Demuxed)
				1					EXT	
			1	0				16-bit	OSC	
				1					EXT	

* OM[0] selects the clock source of MPLL/EPLL
(You can select different EPLL clock source with that of MPLL by software setting – refer to SYSCON)
* addr(x) means the number of address cycle during NAND Flash operation.

S3C2443X MEMORY MAP AND BASE ADDRESS OF SPECIAL REGISTERS

Memory Map

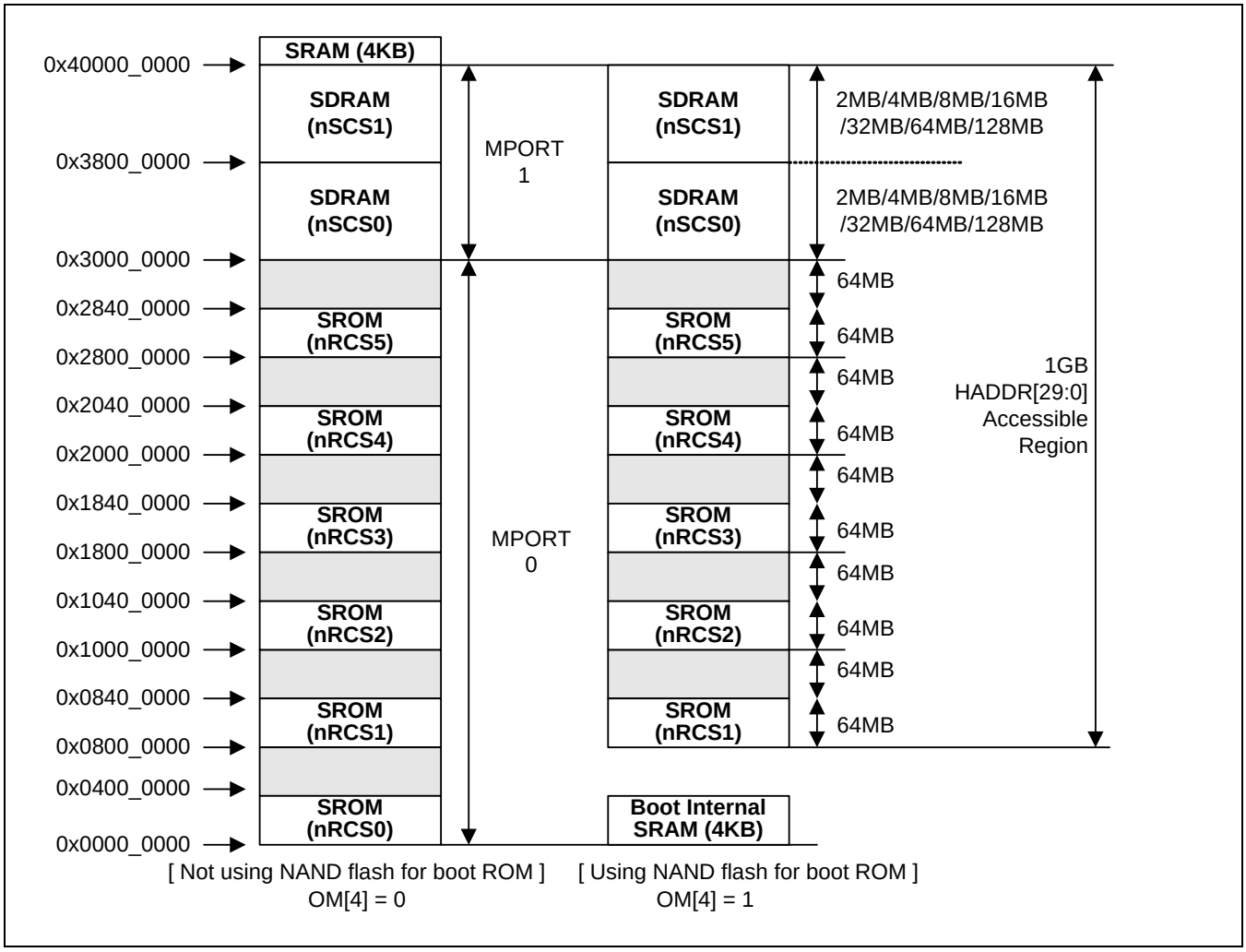


Figure 1-3. Memory Map

Base Address of Special Registers

Address	Module	Address	Module
0x5100_0000	PWM	0x5B00_0000	AC97
0x5000_0000	UART	0x5A00_0000	SDI
0x4F80_0000	TIC	0x5900_0000	SPI
0x4F00_0000	SSMC		
0x4E80_0000	MATRIX	0x5800_0000	TSADC
0x4E00_0000	NFCON		
0x4D80_0000	CAM I/F	0x5700_0000	RTC
0x4D00_0000	STN-LCD		
0x4C80_0000	TFT-LCD	0x5600_0000	IO Port
0x4C00_0000	SYSCON		
0x4B80_0000	CF Card	0x5500_0000	IIS
0x4B00_0000	DMA		
0x4A80_0000	HS-MMC	0x5400_0000	IIC
0x4A00_0000	INTC		
0x4980_0000	USB Device	0x5300_0000	WDT
0x4900_0000	USB HOST		
0x4880_0000	EBI	0x5200_0000	HS-SPI
0x4800_0000	SDRAM		

Table 1-5. S3C2443X Special Registers

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
DRAM Controller					
BANKCFG	0x48000000	←	W	R/W	Mobile DRAM configuration register
BANKCON1	0x48000004				Mobile DRAM control register
BANKCON2	0x48000008				Mobile DRAM timing control register
BANKCON3	0x4800000C				Mobile DRAM (E)MRS Register
REFRESH	0x48000010				Mobile DRAM refresh control register
TIMEOUT	0x48000014				Write Buffer Time out control register
MATRIX & EBI					
BPRIORITY0	0X4E800000			R/W	Matrix Core 0 priority control register
BPRIORITY1	0X4E800004			R/W	Matrix Core 1 priority control register
EBICON	0X4E800008			R/W	EBI control register
Memory Controllers (SSMC)					
SMBIDCYR0	0x4F000000		W	R/W	Bank0 idle cycle control register
SMBIDCYR1	0x4F000020			R/W	Bank1 idle cycle control register
SMBIDCYR2	0x4F000040			R/W	Bank2 idle cycle control register
SMBIDCYR3	0x4F000060			R/W	Bank3 idle cycle control register
SMBIDCYR4	0x4F000080			R/W	Bank4 idle cycle control register
SMBIDCYR5	0x4F0000A0			R/W	Bank5 idle cycle control register
SMBWSTRDR0	0x4F000004			R/W	Bank0 read wait state control register
SMBWSTRDR1	0x4F000024			R/W	Bank1 read wait state control register
SMBWSTRDR2	0x4F000044			R/W	Bank2 read wait state control register
SMBWSTRDR3	0x4F000064			R/W	Bank3 read wait state control register
SMBWSTRDR4	0x4F000084			R/W	Bank4 read wait state control register
SMBWSTRDR5	0x4F0000A4			R/W	Bank5 read wait state control register
SMBWSTWRR0	0x4F000008			R/W	Bank0 write wait state control register
SMBWSTWRR1	0x4F000028			R/W	Bank1 write wait state control register
SMBWSTWRR2	0x4F000048			R/W	Bank2 write wait state control register
SMBWSTWRR3	0x4F000068			R/W	Bank3 write wait state control register
SMBWSTWRR4	0x4F000088			R/W	Bank4 write wait state control register
SMBWSTWRR5	0x4F0000A8			R/W	Bank5 write wait state control register
SMBWSTOENR0	0x4F00000C			R/W	Bank0 output enable assertion delay control register
SMBWSTOENR1	0x4F00002C			R/W	Bank1 output enable assertion delay control register

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
SMBWSTOENR2	0x4F00004C			R/W	Bank2 output enable assertion delay control register
SMBWSTOENR3	0x4F00006C			R/W	Bank3 output enable assertion delay control register
SMBWSTOENR4	0x4F00008C			R/W	Bank4 output enable assertion delay control register
SMBWSTOENR5	0x4F0000AC			R/W	Bank5 output enable assertion delay control register
SMBWSTWENR0	0x4F000010			R/W	Bank0 write enable assertion delay control register
SMBWSTWENR1	0x4F000030			R/W	Bank1 write enable assertion delay control register
SMBWSTWENR2	0x4F000050			R/W	Bank2 write enable assertion delay control register
SMBWSTWENR3	0x4F000070			R/W	Bank3 write enable assertion delay control register
SMBWSTWENR4	0x4F000090			R/W	Bank4 write enable assertion delay control register
SMBWSTWENR5	0x4F0000B0			R/W	Bank5 write enable assertion delay control register
SMBCR0	0x4F000014			R/W	Bank0 control register
SMBCR1	0x4F000034			R/W	Bank1 control register
SMBCR2	0x4F000054			R/W	Bank2 control register
SMBCR3	0x4F000074			R/W	Bank3 control register
SMBCR4	0x4F000094			R/W	Bank4 control register
SMBCR5	0x4F0000B4			R/W	Bank5 control register
SMBSR0	0x4F000018			R/W	Bank0 status register
SMBSR1	0x4F000038			R/W	Bank1 status register
SMBSR2	0x4F000058			R/W	Bank2 status register
SMBSR3	0x4F000078			R/W	Bank3 status register
SMBSR4	0x4F000098			R/W	Bank4 status register
SMBSR5	0x4F0000B8			R/W	Bank5 status register
SMBWSTBRDR0	0x4F00001C			R/W	Bank0 burst read wait delay control register
SMBWSTBRDR1	0x4F00003C			R/W	Bank1 burst read wait delay control register

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
SMBWSTBRDR2	0x4F00005C			R/W	Bank2 burst read wait delay control register
SMBWSTBRDR3	0x4F00007C			R/W	Bank3 burst read wait delay control register
SMBWSTBRDR4	0x4F00009C			R/W	Bank4 burst read wait delay control register
SMBWSTBRDR5	0x4F0000BC			R/W	Bank5 burst read wait delay control register
SMBONETYPER	0x4F000100			R/W	SMC Bank OneNAND TYPE SELECTION REGISTER
SMCSR	0x4F000200			R/W	SMC status register
SMCCR	0x4F000204			R/W	SMC Control register

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
CF Controller					
MUX_REG	0x4B801800			R/W	Top level control & configuration register
PCCARD_ CNFG&STATUS	0x4B801820				PC card configuration & status register
PCCARD_ INTMSK&SRC	0x4B801824				PC card interrupt mask & source regiseter
PCCARD_ATTR	0x4B801828				PC card attribute memory area operation timing config regiseter
PCCARD_I/O	0x4B80182C				PC card I/O area operation timing config regiseter
PCCARD_COMM	0x4B801830				PC card common memory area operation timing config regiseter
ATA_CONTROL	0x4B801900				ATA enable and clock down status
ATA_STATUS	0x4B801904				ATA status
ATA_COMMAND	0x4B801908				ATA command
ATA_SWRST	0x4B80190C				ATA software reset
ATA_IRQ	0x4B801910				ATA interrupt sources
ATA_IRQ_MASK	0x4B801914				ATA interrut mask
ATA_CFG	0x4B801918				ATA configuration for ATA interface
ATA_PIO_TIME	0x4B80192C				ATA PIO timing
ATA_UDMA_TIME	0x4B801930				ATA UDMA timing
ATA_XFR_NUM	0x4B801934				ATA transfer number
ATA_XFR_CNT	0x4B801938				ATA current transfer count
ATA_TBUF_START	0x4B80193C				ATA start address of track buffer
ATA_TBUF_SIZE	0x4B801940				ATA size of track buffer
ATA_SBUF_ START	0x4B801944				ATA start address of source buffer
ATA_SBUF_SIZE	0x4B801948				ATA size of source buffer
ATA_SBUF_ START	0x4B801944				ATA start address of source buffer
ATA_SBUF_SIZE	0x4B801948				ATA size of source buffer
ATA_CADR_TBUF	0x4B80194C				ATA current write address of track buffer
ATA_CADR_SBUF	0x4B801950				ATA current read address of source buffer
ATA_PIO_DTR	0x4B801954				ATA PIO device data register

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
ATA_PIO_FED	0x4B801958				ATA PIO device Feature/Error register
ATA_PIO_SCR	0x4B80195C				ATA PIO sector count register
ATA_PIO_LLR	0x4B801960				ATA PIO device LBA low register
ATA_PIO_LMR	0x4B801964				ATA PIO device LBA middle register
ATA_PIO_LHR	0x4B801968				ATA PIO device LBA high register
ATA_PIO_DVR	0x4B80196C				ATA PIO device register
ATA_PIO_CSD	0x4B801970				ATA PIO device command/status register
ATA_PIO_DAD ATA_PIO_READY	0x4B801974 0x4B801978				ATA PIO device control/alternate status register
ATA_PIO_RDATA	0x4B80197C				ATA PIO read data from device data register
BUS_FIFO_ STATUS	0x4B801990				ATA internal AHB FIFO status
ATA_FIFO_ STATUS	0x4B801994				ATA internal ATA FIFO status

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
USB Host Controller					
HcRevision	0x49000000	←	W	R/W	Control and status group
HcControl	0x49000004			R/W	
HcCommonStatus	0x49000008			R/W	
HcInterruptStatus	0x4900000C			R/W	
HcInterruptEnable	0x49000010			R/W	
HcInterruptDisable	0x49000014			R/W	
HcHCCA	0x49000018			R/W	Memory pointer group
HcPeriodCuttentED	0x4900001C			R/W	
HcControlHeadED	0x49000020			R/W	
HcControlCurrent ED	0x49000024			R/W	
HcBulkHeadED	0x49000028			R/W	
HcBulkCurrentED	0x4900002C			R/W	
HcDoneHead	0x49000030			R/W	Frame counter group
HcRmInterval	0x49000034			R/W	
HcFmRemaining	0x49000038			R/W	
HcFmNumber	0x4900003C			R/W	
HcPeriodicStart	0x49000040			R/W	
HcLSThreshold	0x49000044			R/W	
HcRhDescriptorA	0x49000048			R/W	Root hub group
HcRhDescriptorB	0x4900004C			R/W	
HcRhStatus	0x49000050			R/W	
HcRhPortStatus1	0x49000054			R/W	
HcRhPortStatus2	0x49000058			R/W	
Interrupt Controller					
SRCPND	0X4A000000	←	W	R/W	Interrupt request status
INTMOD	0X4A000004			R/W	Interrupt mode control
INTMSK	0X4A000008			R/W	Interrupt mask control
PRIORITY	0X4A00000C			R/W	IRQ priority control
INTPND	0X4A000010			R/W	Interrupt request status
INTOFFSET	0X4A000014			R	Interrupt request source offset
SUBSRCPND	0X4A000018			R/W	Sub source pending
INTSUBMSK	0X4A00001C			R/W	Interrupt sub mask

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
DMA					
DISRC0	0x4B000000	←	W	R/W	DMA 0 initial source
DISRCC0	0x4B000004			R/W	DMA 0 initial source control
DIDST0	0x4B000008			R/W	DMA 0 initial destination
DIDSTC0	0x4B00000C			R/W	DMA 0 initial destination control
DCON0	0x4B000010			R/W	DMA 0 control
DSTAT0	0x4B000014			R	DMA 0 count
DCSRC0	0x4B000018			R	DMA 0 current source
DCDST0	0x4B00001C			R	DMA 0 current destination
DMASKTRIG0	0x4B000020			R/W	DMA 0 mask trigger
DMAREQSEL0	0x4B000024			R/W	DMA0 Request Selection Register
DISRC1	0x4B000100	←	W	R/W	DMA 1 initial source
DISRCC1	0x4B000104			R/W	DMA 1 initial source control
DIDST1	0x4B000108			R/W	DMA 1 initial destination
DIDSTC1	0x4B00010C			R/W	DMA 1 initial destination control
DCON1	0x4B000110			R/W	DMA 1 control
DSTAT1	0x4B000114			R	DMA 1 count
DCSRC1	0x4B000118			R	DMA 1 current source
DCDST1	0x4B00011C			R	DMA 1 current destination
DMASKTRIG1	0x4B000120			R/W	DMA 1 mask trigger
DMAREQSEL1	0x4B000124			R/W	DMA1 Request Selection Register
DISRC2	0x4B000200	←	W	R/W	DMA 2 initial source
DISRCC2	0x4B000204			R/W	DMA 2 initial source control
DIDST2	0x4B000208			R/W	DMA 2 initial destination
DIDSTC2	0x4B00020C			R/W	DMA 2 initial destination control
DCON2	0x4B000210			R/W	DMA 2 control
DSTAT2	0x4B000214			R	DMA 2 count
DCSRC2	0x4B000218			R	DMA 2 current source
DCDST2	0x4B00021C			R	DMA 2 current destination
DMASKTRIG2	0x4B000220			R/W	DMA 2 mask trigger
DMAREQSEL2	0x4B000224			R/W	DMA2 Request Selection Register

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
DISRC3	0x4B000300	←	W	R/W	DMA 3 initial source
DISRCC3	0x4B000304			R/W	DMA 3 initial source control
DIDST3	0x4B000308			R/W	DMA 3 initial destination
DIDSTC3	0x4B00030C			R/W	DMA 3 initial destination control
DCON3	0x4B000310			R/W	DMA 3 control
DSTAT3	0x4B000314			R	DMA 3 count
DCSRC3	0x4B000318			R	DMA 3 current source
DCDST3	0x4B00031C			R	DMA 3 current destination
DMASKTRIG3	0x4B000320			R/W	DMA 3 mask trigger
DMAREQSEL3	0x4B000324			R/W	DMA3 Request Selection Register
DISRC4	0x4B000400	←	W	R/W	DMA 4 initial source
DISRCC4	0x4B000404			R/W	DMA 4 initial source control
DIDST4	0x4B000408			R/W	DMA 4 initial destination
DIDSTC4	0x4B00040C			R/W	DMA 4 initial destination control
DCON4	0x4B000410			R/W	DMA 4 control
DSTAT4	0x4B000414			R	DMA 4 count
DCSRC4	0x4B000418			R	DMA 4 current source
DCDST4	0x4B00041C			R	DMA 4 current destination
DMASKTRIG4	0x4B000420			R/W	DMA 4 mask trigger
DMAREQSEL4	0x4B000424			R/W	DMA4 Request Selection Register
DISRC5	0x4B000500	←	W	R/W	DMA 5 initial source
DISRCC5	0x4B000504			R/W	DMA 5 initial source control
DIDST5	0x4B000508			R/W	DMA 5 initial destination
DIDSTC5	0x4B00050C			R/W	DMA 5 initial destination control
DCON5	0x4B000510			R/W	DMA 5 control
DSTAT5	0x4B000514			R	DMA 5 count
DCSRC5	0x4B000518			R	DMA 5 current source
DCDST5	0x4B00051C			R	DMA 5 current destination
DMASKTRIG5	0x4B000520			R/W	DMA 5 mask trigger
DMAREQSEL5	0x4B000524			R/W	DMA5 Request Selection Register

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
Syscon					
LOCKCON0	0x4C00_0000	←	W	R/W	MPLL lock time count register
LOCKCON1	0x4C00_0004				EPLL lock time count register
OSCSET	0x4C00_0008				Oscillator stabilization control register
Reserved	0x4C00_000C				Reserved
MPLLCON	0x4C00_0010				MPLL configuration register
RESERVED	0x4C00_0014				RESERVED
EPLLCON	0x4C00_0018				EPLL configuration register
CLKSRC	0x4C00_0020				Clock source control register
CLKDIV0	0x4C00_0024				Clock divider ratio control register0
CLKDIV1	0x4C00_0028				Clock divider ratio control register1
HCLKCON	0x4C00_0030				HCLK enable register
PCLKCON	0x4C00_0034				PCLK enable register
SCLKCON	0x4C00_0038				Special clock enable register
RESERVED	0x4C00_003C				Reserved
PWRMODE	0x4C00_0040				Power mode control register
SWRST	0x4C00_0044				Software reset control register
BUSPRI0	0x4C00_0050				Bus priority control register 0
SYSID	0x4C00_005C			R	System ID register
PWRCFG	0x4C00_0060			R/W	Power management configuration register
RSTCON	0x4C00_0064				Reset control register
RSTSTAT	0x4C00_0068			R	Reset status register
WKUPSTAT	0x4C00_006C			R/W	Wake-up status register
INFORM0	0x4C00_0070				SLEEP mode information register 0
INFORM1	0x4C00_0074				SLEEP mode information register 1
INFORM2	0x4C00_0078				SLEEP mode information register 2
INFORM3	0x4C00_007C				SLEEP mode information register 3
PHYCTRL	0x4C00_0080				usb phy control register
PHYPWR	0x4C00_0084				usb phy power control register
URSTCON	0x4C00_0088				usb phy reset control register
UCLKCON	0x4C00_008C				usb phy clock control register

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
TFT LCD Controller					
VIDCON0	0x4C80_0000			R/W	Video control 0 register
VIDCON1	0x4C80_0004				Video control 1 register
VIDTCON0	0x4C80_0008				Video time control 0 register
VIDTCON1	0x4C80_000C				Video time control 1 register
VIDTCON2	0x4C80_0010				Video time control 2 register
WINCON0	0x4C80_0014				Window control 0 register
WINCON1	0x4C80_0018				Window control 1 register
VIDOSD0A	0x4C80_0028				Video Window 0's position control register
VIDOSD0B	0x4C80_002C				Video Window 0's position control register
VIDOSD0C	0x4C80_0030				Video Window 0's position control register
VIDOSD1A	0x4C80_0034				Video Window 1's position control register
VIDOSD1B	0x4C80_0038				Video Window 1's position control register
VIDOSD1C	0x4C80_003C				Video Window 1's position control register
VIDW00ADD0B0	0x4C80_0064				Window 0's buffer start address register, buffer 0
VIDW00ADD0B1	0x4C80_0068				Window 0's buffer start address register, buffer 1
VIDW01ADD0	0x4C80_006C				Window 1's buffer start address register
VIDW00ADD1B0	0x4C80_007C				Window 0's buffer end address register, buffer 0
VIDW00ADD1B1	0x4C80_0080				Window 0's buffer end address register, buffer 1
VIDW01ADD1	0x4C80_0084				Window 1's buffer end address register
VIDW00ADD2B0	0x4C80_0094				Window 0's buffer size register, buffer 0
VIDW00ADD2B1	0x4C80_0098				Window 0's buffer size register, buffer 1
VIDW01ADD2	0x4C80_009C				Window 1's buffer size register

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
VIDINTCON	0x4C80_00AC				Indicate the Video interrupt control register
W1KEYCON0	0x4C80_00B0				Color key control register
W1KEYCON1	0x4C80_00B4				Color key value (transparent value) register
W2KEYCON0	0x4C80_00B8				Color key control register
W2KEYCON1	0x4C80_00BC				Color key value (transparent value) register
W3KEYCON0	0x4C80_00C0				Color key control register
W3KEYCON1	0x4C80_00C4				Color key value (transparent value) register
W4KEYCON0	0x4C80_00C8				Color key control register
W4KEYCON1	0x4C80_00CC				Color key value (transparent value) register
WIN0MAP	0x4C80_00D0				Window color control
WIN1MAP	0x4C80_00D4				Window color control
WPALCON	0x4C80_00E4				Window Palette control register
SYSIFCON0	0x4C80_0130				System Interface control for Main LDI
SYSIFCON1	0x4C80_0134				System Interface control for Sub LDI
DITHMODE1	0x4C80_0138				Dithering mode register.
rSIFCCON0	0x4C80_013C				System interface command control
rSIFCCON1	0x4C80_0140				SYS IF command data write control
rSIFCCON2	0x4C80_0144				SYS IF command data read control
rCPUTRIGCON1	0x4C80_015C				CPU trigger source mask
rCPUTRIGCON2	0x4C80_0160				Software based trigger control
rVIDW00ADD0B1	0x4C80_0068				Window 0’s buffer start ADDR
rVIDW01ADD0	0x4C80_006C				Window 1’s buffer start ADDR

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
CSTN LCD Controller					
LCDCON1	0X4D000000	←	W	R/W	LCD control 1 register
LCDCON2	0X4D000004			R/W	LCD control 2 register
LCDCON3	0X4D000008			R/W	LCD control 3 register
LCDCON4	0X4D00000C			R/W	LCD control 4 register
LCDCON5	0X4D000010			R/W	LCD control 5 register
LCDSADDR1	0X4D000014	←	W	R/W	**STN/TFT**: Frame buffer start address 1 register
LCDSADDR2	0X4D000018			R/W	**STN/TFT**: Frame buffer start address 2 register
LCDSADDR3	0X4D00001C			R/W	**STN/TFT**: Virtual screen address set
REDLUT	0X4D000020			R/W	**STN**: Red lookup table register
GREENLUT	0X4D000024			R/W	**STN**: Green lookup table register
BLUELUT	0X4D000028			R/W	**STN**: Blue lookup table register
DITHMODE	0X4D00004C			R/W	Dithering Mode Register
LCDINTPND	0X4D000054				Indicate the LCD interrupt pending register
LCDSRCPND	0X4D000058				Indicate the LCD interrupt source pending register
LCDINTMSK	0X4D00005C				Determine which interrupt source is masked. The masked interrupt source will not be serviced.

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
NAND Flash					
NFCONF	0x4E000000	←	W	R/W	Configuration register
NFCONT	0x4E000004				Control register
NFCMMD	0x4E000008				Command register
NFADDR	0x4E00000C				Address register
NFDATA	0x4E000010				Data register
NFMECCD0	0x4E000014				1st and 2nd main ECC data register
NFMECCD1	0x4E000018				3rd and 4th main ECC data register
NFSECCD	0x4E00001C				Spare ECC read register
NFSBLK	0x4E000020				Programmable start block address register
NFEBLK	0x4E000024				Programmable end block address register
NFSTAT	0x4E000028			R	NAND status registet
NFECCERR0	0x4E00002C			R	ECC error status0 register
NFECCERR1	0x4E000030			R	ECC error status1 register
NFMECC0	0x4E000034			R	Generated ECC status0 register
NFMECC1	0x4E000038			R	Generated ECC status1 register
NFSECC	0x4E00003C			R	Generated Spare area ECC status register
NFMLCBITPT	0x4E000040			R	4-bit ECC error bit pattern register

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
Camera Interface					
CISRCFMT	0x4D80_0000	←	W	RW	Input source format
CIWDOFST	0x4D80_0004				Window offset register
CIGCTRL	0x4D80_0008				Global control register
CIDOWSFT2	0x4D80_0014				Window option register 2
CICOYSA1	0x4D80_0018				Y 1st frame start address for codec DMA
CICOYSA2	0x4D80_001C				Y 2nd frame start address for codec DMA
CICOYSA3	0x4D80_0020				Y 3rd frame start address for codec DMA
CICOYSA4	0x4D80_0024				Y 4th frame start address for codec DMA
CICOCBSA1	0x4D80_0028				Cb 1st frame start address for codec DMA
CICOCBSA2	0x4D80_002C				Cb 2nd frame start address for codec DMA
CICOCBSA3	0x4D80_0030				Cb 3rd frame start address for codec DMA
CICOCBSA4	0x4D80_0034				Cb 4th frame start address for codec DMA
CICOCRSA1	0x4D80_0038				Cr 1st frame start address for codec DMA
CICOCRSA2	0x4D80_003C				Cr 2nd frame start address for codec DMA
CICOCRSA3	0x4D80_0040				Cr 3rd frame start address for codec DMA
CICOCRSA4	0x4D80_0044				Cr 4th frame start address for codec DMA
CICOTRGFMT	0x4D80_0048				Target image format of codec DMA
CICOCTRL	0x4D80_004C				Codec DMA control related
CICOSC PRERATIO	0x4D80_0050				Codec pre-scaler ratio control
CICOSCPREDST	0x4D80_0054				Codec pre-scaler destination format
CICOSCCTRL	0x4D80_0058				Codec main-scaler control
CICOTAREA	0x4D80_005C				Codec scaler target area
CICOSTATUS	0x4D80_0064				Codec path status

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L.Endian)	Acc. Unit	Read/ Write	Function
CIPRCLRSA1	0x4D80_006C				RGB 1st frame start address for preview DMA
CIPRCLRSA2	0x4D80_0070				RGB 2nd frame start address for preview DMA
CIPRCLRSA3	0x4D80_0074				RGB 3rd frame start address for preview DMA
CIPRCLRSA4	0x4D80_0078				RGB 4th frame start address for preview DMA
CIPRTRGFMT	0x4D80_007C				Target image format of preview DMA
CIPRCTRL	0x4D80_0080				Preview DMA control related
CIPRSCPRERATIO	0x4D80_0084				Preview pre-scaler ratio control
CIPRSCPREDST	0x4D80_0088				Preview pre-scaler destination format
CIPRSCCTRL	0x4D80_008C				Preview main-scaler control
CIPRTAREA	0x4D80_0090				Preview scaler target area
CIPRSTATUS	0x4D80_0098				Preview path status
CIIMGCPT	0x4D80_00A0				Image capture enable command
CICOCPTSEQ	0x4D80_00A4				Codec dma capture sequence related
CICOSCOS	0x4D80_00A8				Codec scan line offset related
CIIMGEFF	0x4D80_00B0				Image Effects related
CIMSYSA	0x4D80_00B4				MSDMA Y start address related
CIMSCBSA	0x4D80_00B8				MSDMA Cb start address related
CIMSCRSA	0x4D80_00BC				MSDMA Cr start address related
CIMSYEND	0x4D80_00C0				MSDMA Y end address related
CIMSCBEND	0x4D80_00C4				MSDMA Cb end address related
CIMSCREND	0x4D80_00C8				MSDMA Cr end address related
CIMSYOFF	0x4D80_00CC				MSDMA Y offset related
CIMSCBOFF	0x4D80_00D0				MSDMA Cb offset related
CIMSCROFF	0x4D80_00D4				MSDMA Cr offset related
CIMSWIDTH	0x4D80_00D8				MSDMA source image width related
CIMSCTRL	0x4D80_00DC				MSDMA control register

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
UART					
ULCON0	0x50000000	←	W	R/W	UART 0 line control
UCON0	0x50000004				UART 0 control
UFCON0	0x50000008				UART 0 FIFO control
UMCON0	0x5000000C				UART 0 modem control
UTRSTAT0	0x50000010			R	UART 0 Tx/Rx status
UERSTAT0	0x50000014				UART 0 Rx error status
UFSTAT0	0x50000018				UART 0 FIFO status
UMSTAT0	0x5000001C				UART 0 modem status
UTXH0	0x50000023	0x50000020	B	W	UART 0 transmission hold
URXH0	0x50000027	0x50000024		R	UART 0 receive buffer
UBRDIV0	0x50000028	←	W	R/W	UART 0 baud rate divisor
UDIVSLOT0	0x5000002C				Baud rate divisior(decimal place) register 0
ULCON1	0x50004000				UART 1 line control
UCON1	0x50004004				UART 1 control
UFCON1	0x50004008				UART 1 FIFO control
UMCON1	0x5000400C				UART 1 modem control
UTRSTAT1	0x50004010			R	UART 1 Tx/Rx status
UERSTAT1	0x50004014				UART 1 Rx error status
UFSTAT1	0x50004018				UART 1 FIFO status
UMSTAT1	0x5000401C				UART 1 modem status
UTXH1	0x50004023	0x50004020	B	W	UART 1 transmission hold
URXH1	0x50004027	0x50004024		R	UART 1 receive buffer
UBRDIV1	0x50004028	←	W	R/W	UART 1 baud rate divisor
UDIVSLOT1	0x500402C				Baud rate divisior(decimal place) register 1
ULCON2	0x50008000				UART 2 line control
UCON2	0x50008004				UART 2 control
UFCON2	0x50008008				UART 2 FIFO control
UTRSTAT2	0x50008010			R	UART 2 Tx/Rx status
UERSTAT2	0x50008014				UART 2 Rx error status
UFSTAT2	0x50008018				UART 2 FIFO status
UTXH2	0x50008023	0x50008020	B	W	UART 2 transmission hold
URXH2	0x50008027	0x50008024		R	UART 2 receive buffer

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
UBRDIV2	0x50008028	←	W	R/W	UART 2 baud rate divisor
UDIVSLOT2	0x500802C				Baud rate divisior(decimal place) register 2
ULCON3	0x5000C000				UART 3 line control
UCON3	0x5000C004				UART 3 control
UFCON3	0x5000C008				UART 3 FIFO control
UTRSTAT3	0x5000C010			R	UART 3 Tx/Rx status
UERSTAT3	0x5000C014				UART 3 Rx error status
UFSTAT3	0x5000C018				UART 3 FIFO status
UTXH3	0x5000C023	0x5000C020	B	W	UART 3 transmission hold
URXH3	0x5000C027	0x5000C024		R	UART 3 receive buffer
UBRDIV3	0x5000C028	←	W	R/W	UART 3 baud rate divisor
UDIVSLOT3	0x500C02C				Baud rate divisior(decimal place) register 3
PWM Timer					
TCFG0	0x51000000	←	W	R/W	Timer configuration
TCFG1	0x51000004				Timer configuration
TCON	0x51000008				Timer control
TCNTB0	0x5100000C				Timer count buffer 0
TCMPB0	0x51000010				Timer compare buffer 0
TCNTO0	0x51000014			R	Timer count observation 0
TCNTB1	0x51000018			R/W	Timer count buffer 1
TCMPB1	0x5100001C				Timer compare buffer 1
TCNTO1	0x51000020			R	Timer count observation 1
TCNTB2	0x51000024			R/W	Timer count buffer 2
TCMPB2	0x51000028				Timer compare buffer 2
TCNTO2	0x5100002C			R	Timer count observation 2
TCNTB3	0x51000030			R/W	Timer count buffer 3
TCMPB3	0x51000034				Timer compare buffer 3
TCNTO3	0x51000038			R	Timer count observation 3
TCNTB4	0x5100003C			R/W	Timer count buffer 4
TCNTO4	0x51000040			R	Timer count observation 4

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
USB Device					
IR	0x4980_0000			R/W	Index Register
EIR	0x4980_0004			R/W	Endpoint Interrupt Register
EIER	0x4980_0008			R/W	Endpoint Interrupt Enable Register
FAR	0x4980_000C			R	Function Address Register
FNR	0x4980_0010			R	Frame Number Register
EDR	0x4980_0014			R/W	Endpoint Direction Register
TR	0x4980_0018			R/W	Test Register
SSR	0x4980_001C			R/W	System Status Register
SCR	0x4980_0020			R/W	System Control Register
EP0SR	0x4980_0024			R/W	EP0 Status Register
EP0CR	0x4980_0028			R/W	EP0 Control Register
EP0BR	0x4980_0060			R/W	EP0 Buffer Register
EP1BR	0x4980_0064			R/W	EP1 Buffer Register
EP2BR	0x4980_0068			R/W	EP2 Buffer Register
EP3BR	0x4980_006C			R/W	EP3 Buffer Register
EP4BR	0x4980_0070			R/W	EP4 Buffer Register
EP5BR	0x4980_0074			R/W	EP5 Buffer Register
EP6BR	0x4980_0078			R/W	EP6 Buffer Register
EP7BR	0x4980_007C			R/W	EP7 Buffer Register
EP8BR	0x4980_0080			R/W	EP8 Buffer Register
FCON	0x4980_0100			R/W	Burst FIFO-DMA Control
FSTAT	0x4980_0104			R	Burst FIFO status
ESR	0x4980_002C			R/W	Endpoints Status Register
ECR	0x4980_0030			R/W	Endpoints Control Register
BRCR	0x4980_0034			R	Byte Read Count Register
BWCR	0x4980_0038			R/W	Byte Write Count Register
MPR	0x4980_003C			R/W	Max Packet Register
DCR	0x4980_0040			R/W	DMA Control Register
DTCR	0x4980_0044			R/W	DMA Transfer Counter Register
DFCR	0x4980_0048			R/W	DMA FIFO Counter Register
DTTCR1	0x4980_004C			R/W	DMA Total Transfer Counter1 Register
DTTCR2	0x4980_0050			R/W	DMA Total Transfer Counter2 Register
MICR	0x4980_0084			R/W	Master Interface Control Register
MBAR	0x4980_0088			R/W	Memory Base Address Register
MCAR	0x4980_008C			R	Memory Current Address Register

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
Watchdog Timer					
WTCON	0x53000000	←	W	R/W	Watchdog timer mode
WTDAT	0x53000004				Watchdog timer data
WTCNT	0x53000008				Watchdog timer count
IIC					
IICCON	0x54000000	←	W	R/W	IIC control
IICSTAT	0x54000004				IIC status
IICADD	0x54000008				IIC address
IICDS	0x5400000C				IIC data shift
IICLC	0x54000010				IIC multi-master line control
IIS					
IISCON	0x55000000		W	R/W	IIS control
IISMOD	0x55000004				IIS mode
I2SFIC	0x55000008				I2S interface FIFO control register
I2SPSR	0x5500000C				I2S interface clock divider control register
I2STXD	0x55000010			W	I2S interface transmit data register
I2SRXD	0x55000014			R	I2S interface receive data register

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
I/O port					
GPACDL	0x56000000	←	W	R/W	Port A control & Data
GPACDH	0x56000004				Port A control & Data
GPBCON	0x56000010				Port B control
GPBDAT	0x56000014				Port B data
GPBUDP	0x56000018				Pull-up/down control B
GPCCON	0x56000020				Port C control
GPCDAT	0x56000024				Port C data
GPCUDP	0x56000028				Pull-up/down control C
GPDCON	0x56000030				Port D control
GPDDAT	0x56000034				Port D data
GPDUDP	0x56000038				Pull-up/down control D
GPECON	0x56000040				Port E control
GPEDAT	0x56000044				Port E data
GPEUDP	0x56000048				Pull-up/down control E
GPFCON	0x56000050				Port F control
GPFDAT	0x56000054				Port F data
GPGCON	0x56000060				Port G control
GPGDAT	0x56000064				Port G data
GPGUDP	0x56000068				Pull-up/down control G
GPHCON	0x56000070				Port H control
GPHDAT	0x56000074				Port H data
GPHUDP	0x56000078				Pull-up/down control H
GPJCON	0x560000D0				Port J control
GPJDAT	0x560000D4				Port J data
GPJUDP	0x560000D8				Pull-up/down control J
-	0x560000E0	-	-	-	-
-	0x560000E4	-	-	-	-
DATAPDEN	0x560000E8				Pull-up/down control SDATA/RDATA
GPLCON	0x560000F0				Port L control
GPLDAT	0x560000F4				Port L data
GPLUDP	0x560000F8				Pull-up/down control L
GPMCON	0x56000100				Port M control
GPMDAT	0x56000104				Port M data

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
GPMUDP	0x56000108				Pull-up/down control M
MISCCR	0x56000080				Miscellaneous control
DCLKCON	0x56000084				DCLK0/1 control
EXTINT0	0x56000088				External interrupt control register 0
EXTINT1	0x5600008C				External interrupt control register 1
EXTINT2	0x56000090				External interrupt control register 2
EINTFLT2	0x5600009c				External interrupt control register 2
EINTFLT3	0x4c6000a0				External interrupt control register 3
EINTMASK	0x4c6000a4				External interrupt mask register
EINTPEND	0x560000a8				External interrupt pending register
GSTATUS0	0x560000ac				External pin status
GSTATUS1	0x560000b0				Chip ID
DSC0	0x560000c0				Strength control register 0
DSC1	0x560000c4				Strength control register 1
DSC2	0x560000c8				Strength control register 2
MSLCON	0x560000cc				Memory I/F HiZ control register
DATAPEN	0x560000e8				Pull down control for S/RDATA
RTC					
RTCCON	0x57000043	0x57000040	B	R/W	RTC control
TICNT0	0x57000047	0x57000044			Tick time count register 0
TICNT1	0x5700004F	0x5700004C			Tick time count register 1
RTCALM	0x57000053	0x57000050			RTC alarm control
ALMSEC	0x57000057	0x57000054			Alarm second
ALMMIN	0x5700005B	0x57000058			Alarm minute
ALMHOUR	0x5700005F	0x5700005C			Alarm hour
ALMDATE	0x57000063	0x57000060			Alarm day
ALMMON	0x57000067	0x57000064			Alarm month
ALMYEAR	0x5700006B	0x57000068			Alarm year
BCDSEC	0x57000073	0x57000070			BCD second
BCDMIN	0x57000077	0x57000074			BCD minute
BCDHOUR	0x5700007B	0x57000078			BCD hour
BCDDATE	0x5700007F	0x5700007C			BCD day
BCDDAY	0x57000083	0x57000080			BCD date
BCDMON	0x57000087	0x57000084			BCD month
BCDYEAR	0x5700008B	0x57000088			BCD year
TICKCNT		0x57000090	W	R	Internal tick time counter
RTCLBAT	0x57000097	0x57000094	B	R/W	RTC LOW battery check

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
A/D Converter					
ADCCON	0x58000000	←	W	R/W	ADC control
ADCTSC	0x58000004				ADC touch screen control
ADCDLY	0x58000008				ADC start or interval delay
ADCDAT0	0x5800000C			R	ADC conversion data
ADCDAT1	0x58000010				ADC conversion data
ADCUPDN	0x58000014			R/W	Stylus up or down interrupt status
ADCMUX	0x58000018			R/W	Analog input channel select
SPI(SPI Channel 1)					
SPCON1	0x59000000	←	W	R/W	SPI Channel 1 control
SPSTA1	0x59000004			R	SPI Channel 1 status
SPPIN1	0x59000008			R/W	SPI Channel 1 pin control
SPPRE1	0x5900000C				SPI Channel 1 baud rate prescaler
SPTDAT1	0x59000010				SPI Channel 1 Tx data
SPRDAT1	0x59000014			R	SPI Channel 1 Rx data
SPTXFIFO1	0x59000018			W	SPI Channel 1 Tx FIFO Register
SPRXFIFO1	0x5900001C			R	SPI Channel 1 Rx FIFO Register
SPRDATB1	0x59000020			R	SPI Channel 1 Rx Data Register
SPFIC1	0x59000024			R/W	SPI Channel 1 FIFO Interrupt and DMA control Register
SPTOV1	0x59000028			R/W	SPI Channel 1 Rx FIFO Timeout Value Register
SD/MMC Interface (SD/MMC Channel 1)					
SDICON	0x5A000000	←	W	R/W	SDI control
SDIPRE	0x5A000004				SDI baud rate prescaler
SDICARG	0x5A000008				SDI command argument
SDICCON	0x5A00000C				SDI command control
SDICSTA	0x5A000010			R/(C)	SDI command status
SDIRSP0	0x5A000014			R	SDI response
SDIRSP1	0x5A000018				SDI response
SDIRSP2	0x5A00001C				SDI response
SDIRSP3	0x5A000020				SDI response
SDIDTIMER	0x5A000024			R/W	SDI data / busy timer
SDIBSIZE	0x5A000028				SDI block size
SDIDCON	0x5A00002C				SDI data control
SDIDCNT	0x5A000030			R	SDI data remain counter
SDIDSTA	0x5A000034			R/(C)	SDI data status
SDIFSTA	0x5A000038			R	SDI FIFO status
SDIIMSK	0x5A00003C	←	W		SDI interrupt mask
SDIDAT	0x5A000043	0x5A000040	B	R/W	SDI data

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
HSSPI(SPI Channel 0)					
CH_CFG	0x52000000			R/W	SPI configuration register
Clk_CFG	0x52000004				Clock configuration register
MODE_CFG	0x52000008				SPI FIFO control register
Slave_slection_reg	0x5200000C				Slave selection signal
SPI_INT_EN	0x52000010				SPI Interrupt Enable register
SPI_STATUS	0x52000014				SPI status register
SPI_TX_DATA	0x52000018				SPI TX DATA register
SPI_RX_DATA	0x5200001C				SPI RX DATA register
Packet_Count_reg	0x52000020				Count how many data master gets
Pending_clr_reg	0x52000024				Pending clear register
HSMMC(SD/MMC Channel 0)					
SYSAD	0x4A800000	←		R/W	SDI control register
BLKSIZE	0x4A800004				Host DMA Buffer Boundary and Transfer Block Size Register
BLKCNT	0x4A800006				Blocks Count For Current Transfer
ARGUMENT	0x4A800008				Command Argument Register
TRNMOD	0x4A80000C				Transfer Mode Setting Register
CMDREG	0x4A80000E				Command Register
RSPREG0	0x4A800010				Response Register 0
RSPREG1	0x4A800014				Response Register 1
RSPREG2	0x4A800018				Response Register 2
RSPREG3	0x4A80001C				Response Register 3
BDATA	0x4A800020				Buffer Data Register
PRNSTS	0x4A800024				Present State Register
HOSTCTL	0x4A800028				Present State Register
PWRCON	0x4A800029				Present State Register
BLKGAP	0x4A80002A				Block Gap Control Register
WAKCON	0x4A80002B				Wakeup Control Register
CLKCON	0x4A80002C				Command Register
TIMEOUTCON	0x4A80002E				Timeout Control Register
SWRST	0x4A80002F				Software Reset Register
NORINTSTS	0x4A800030				Normal Interrupt Status Register
ERRINTSTS	0x4A800032				Error Interrupt Status Register

Table 1-5. S3C2443X Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
NORINTSTSEN	0x4A800034				Normal Interrupt Status Enable Register
ERRINTSTSEN	0x4A800036				Error Interrupt Status Enable Register
NORINTSIGEN	0x4A800038				Normal Interrupt Signal Enable Register
ERRINTSIGEN	0x4A80003A				Error Interrupt Signal Enable Register
ACMD12ERRSTS	0x4A80003C				Auto CMD12 Error Status Register
CAPAREG	0x4A800040				Capabilities Register
MAXCURR	0x4A800048				Maximum Current Capabilities Register
CONTROL2	0x4A800080				Control register 2
CONTROL3	0x4A800084				FIFO Interrupt Control (Control Register 3)
HCVER	0x4A8000FE				Host Controller Version Register
AC97 Audio-CODEC Interface					
AC_GLBCTRL	0x5B000000	←	W	R/W	AC97 global control register
AC_GLBSTAT	0x5B000004			R	AC97 global status register
AC_CODEC_CMD	0x5B000008			R/W	AC97 codec command register
AC_CODEC_STAT	0x5B00000C			R	AC97 codec status register
AC_PCMADDR	0x5B000010				AC97 PCM out/in channel FIFO address register
AC_MICADDR	0x5B000014				AC97 mic in channel FIFO address register
AC_PCMDATA	0x5B000018			R/W	AC97 PCM out/in channel FIFO data register
AC_MICDATA	0x5B00001C				AC97 MIC in channel FIFO data register

Cautions on S3C2443X Special Registers

1. In the little endian mode ‘L’, endian address must be used. In the big endian mode ‘B’ endian address must be used.
2. The special registers have to be accessed for each recommended access unit.
3. All registers except ADC registers, RTC registers and UART registers must be read/write in word unit (32-bit) in little/big endian.
4. Make sure that the ADC registers, RTC registers and UART registers be read/write by the specified access unit and the specified address. Moreover, one must carefully consider which endian mode is used.
5. W : 32-bit register, which must be accessed by LDR/STR or int type pointer (int *).
   HW : 16-bit register, which must be accessed by LDRH/STRH or short int type pointer (short int *).
   B : 8-bit register, which must be accessed by LDRB/STRB or char type pointer (char int *).

2 SYSTEM CONTROLLER

OVERVIEW

The system controller consists of three parts; reset control, system clock control, and system power-management control. The system clock control logic in S3C2443X can generate the required system clock signals which are the inputs of ARM920T, several AHB blocks, and APB blocks. There are two PLLs in S3C2443X to generate internal clocks. One is for general functional blocks, which include ARM, AHB, and APB. The other is for the special functional clocks which are the USB, I2S and camera interface clock. Software program control the operating frequency of the PLLs, internal clock sources and enabled or disabled the clocks to reduce the power consumption.

S3C2443X has various power-down modes to keep optimal power consumption for a given task. The power-down modes consists of four modes; NORMAL mode, IDLE mode, STOP mode, and SLEEP mode. In NORMAL mode, the input clock of each block is enabled or disabled according to the software to eliminate the power consumption of unused blocks for a certain application. For example, if an UART is not needed, the software can disable the input clock independently. The major power dissipation of S3C2443X is due to ARM core, since the operating speed is relative higher than that of the other blocks. Typically, the operating frequency of the ARM core is 533MHz, while the AHB blocks and the APB blocks operate on 133MHz and 66MHz, respectively. Thus, the power control of the ARM core is major issue to reduce the overall power dissipation in S3C2443X, and IDLE mode is supported for this purpose. In IDLE mode, the ARM core is not operated until the external interrupts or internal interrupts. The STOP mode freezes all clocks to all peripherals as well as the ARM core by disabling PLLs. The power consumption is only due to the leakage current and the minimized alive block in S3C2443X. SLEEP mode is intended to disconnect the internal power. So, the power consumption due to the ARM core and the internal logic except the wake-up logic will be nearly zero in the SLEEP mode. In order to use the SLEEP mode two indenpendent power sources are required. One of the two power soruces supplies the power for the wake-up logic. The other one supplies the normal functional blocks including the ARM core. It should be controlled in order to turn ON/OFF with a special pin in S3C2443X. The detailed description of the power-saving modes such as the entering sequence to the specific power-down mode or the wake-up sequence from a power-down mode is given in the following Power Management section.

FEATURE

- Include two on-chip PLLs called main PLL(MPLL), extra PLL(EPLL)
- MPLL generates the system reference clock
- EPLL generates the clocks for the special functional blocks
- Independent clock ON/OFF control to reduce power consumption
- Support three power-down modes, IDLE, STOP, and SLEEP, to optimize the power dissipation
- Wake-up by one of external Interrupt, RTC alarm, Tick interrupt and BATT_FLT.(Stop and Sleep mode)
- Control internal bus arbitration priority

BLOCK DIAGRAM

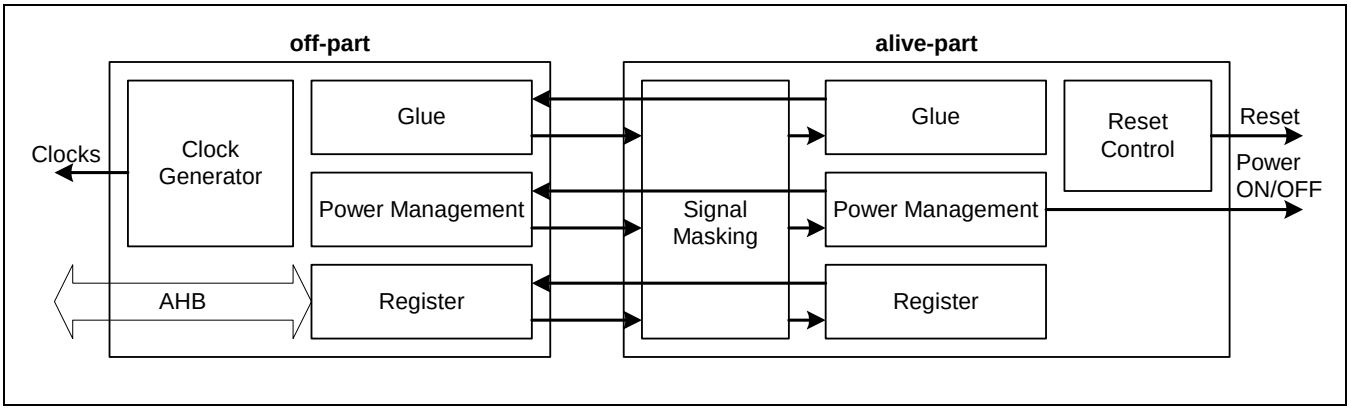


Figure 2-1. System controller block diagram

Figure 2-1 shows the system controller block diagram. The system controller is divided into two blocks, which are the OFF block and the ON block. Since the system controller must be alive when the external power supply is disabled. The ALIVE-part is supplied by an auxiliary power source and waits until external/internal interrupts. However, the OFF-part is disabled when the power-down mode is SLEEP. The clock generator makes all internal clocks, which include ARMCLK for the ARM core, HCLK for the AHB blocks, PCLK for the APB block, and other special clocks. The special functional registers (SFR) are located at the register blocks, and their values are configured through AHB interface. If a software want to change into a power-down mode, then the power management blocks detect the values within the SFR and change the mode. In addition, they assert the external power ON/OFF signal if required. All reset signals are generated at the reset control block.

The detailed explanations for each block will be described in the following sections.

FUNCTIONAL DESCRIPTIONS

The system controller for S3C2443X has three functions, which include the reset management, the clock generation, and the power management. In this section, the behavior will be described.

Reset Management

When S3C2443X is power-on, the external device must assert reset to initialize internal states.

Reset Types

S3C2443X has four types of resets and reset controller in system controller can place the system into the predefined states with one of the following four resets.

- Hardware Reset – It is generated when nRESET pin is asserted. It is an uncompromised, unmaskable, and complete reset, which is used when you need no information in system any more.
- Watchdog Reset – The watchdog timer monitors the device state and generates the watchdog reset when the state is abnormal.
- Software Reset – Software can initialize the internal state by writing the special control register (SWRST).
- Wakeup Reset – When the system wakes up from SLEEP mode, it generates reset signals.

Hardware Reset

Hardware reset is invoked when the nRESET pin is asserted and all units in the system (except RTC) are initialized to known states. During the hardware reset, the following actions will occur:

- All internal registers and ARM920T core goes into their pre-defined initial state.
- All pins get their reset state, and BATT_FLT pin is ignored.
- The nRSTOUT pin is asserted while the reset is progressed.

When the unmaskable nRESET pin is asserted as low, the internal hardware reset signal is generated. Upon assertion of nRESET, S3C2443X enters into reset state regardless of the previous state. To enter hardware reset state, nRESET must be held long enough to allow internal stabilization and propagation of the reset state.

Caution: An external power source, regulator, for S3C2443X must be stable prior to the deassertion of nRESET. Otherwise, it damages to S3C2443X and its operation will not be guaranteed.

Figure 2-2 shows the clock behavior during the power-on reset sequence. The crystal oscillator begins oscillation within several milliseconds after the power source supplies enough power-level to S3C2443X. Initially, two internal PLLs (MPLL and EPLL) stop. The nRESET pin should be released after the fully settle-down of the power supply-level. S3C2443X requires a hazard-free system clock (SYSCLK, ARMCLK, HCLK, and PCLK) to operate properly when the system reset is released. Since the PLL does not work initially, the PLL input clock (F_{IN}) is directly fed to SYSCLK instead of the PLL output clock (F_{OUT}). Software must configure MPLLCON and EPLLCON register to use each PLL. The PLL begins the lockup sequence toward the new frequency only after the S/W configures the PLL with a new frequency-value. The PLL output is immediately fed to SYSCLK after lock time.

You should be aware that the crystal oscillator settle-down time is not explicitly added by the hardware during the power-up sequence and the crystal oscillation must be settle-down during this period. However, S3C2443X will explicitly add the crystal oscillator settle-down time (XTALWAIT) when it wakes up from the STOP mode.

The EPLL output clock is directly fed to some special clocks for TFT Controller, I2S, HS-MMC, USB host and UART. Since the EPLL input clock is initially fed to the input clocks for them, software must configure EPLLCON register to use the EPLL.

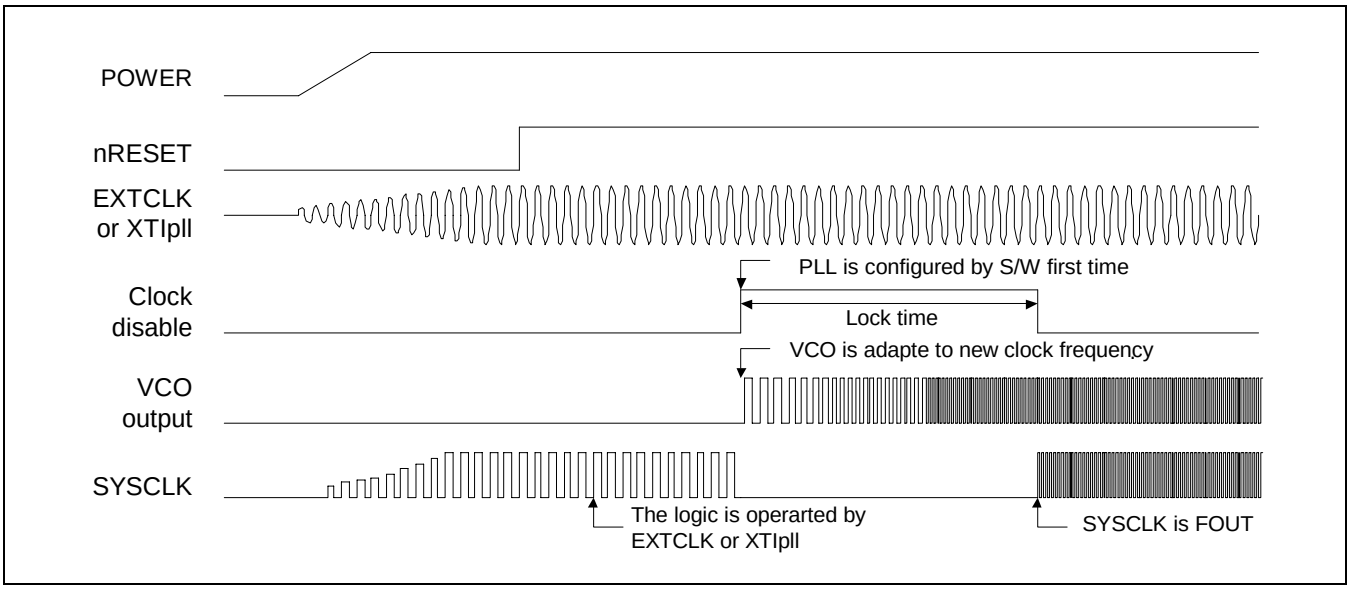


Figure 2-2. Power-on reset sequence

WATCHDOG RESET

Watchdog reset is invoked when software fails to prevent the watchdog timer from timing out.

During the watchdog reset, the following actions occur :

- All units(except some blocks listed in table 2-1) go into their pre-defined reset state.
- All pins get their reset state, and BATT_FLT pin is ignored.
- The nRSTOUT pin is asserted during watchdog reset.

Watchdog reset can be activated in normal and idle mode because watchdog timer can expire with clock.

Watchdog reset is invoked when watchdog timer and reset are enabled (WTCON[5] = 1, WTCON[0]=1) and watchdog timer is expired. Watchdog reset is invoked then, the following sequence occurs. :

1. Watchdog reset source asserts.
2. Internal reset signals and nRSTOUT are asserted and reset counter is activated.
3. Reset counter is expired then, internal reset signals and nRSTOUT are deasserted.

SOFTWARE RESET

Software can initialize the device state itself when it writes “0x533C_2443” to SWRST register.

During the software reset, the following actions occur :

- All units(except some blocks listed in table 2-1) go into their pre-defined reset state.
- All pins get their reset state, and BATT_FLT pin is ignored.
- The nRSTOUT pin is asserted during software reset.

Software reset is invoked then, the following sequence occurs. :

1. User write “0x533C_2443” to SWRST register.
2. System controller request bus controller to finish current transactions.
3. Bus controller send acknowledge to system controller after completed bus transactions.
4. System controller request memory controller to enter into self refresh mode.
5. System controller wait for self refresh acknowledge from memory controller.
6. Internal reset signals and nRSTOUT are asserted and reset counter is activated.
7. Reset counter is expired then, internal reset signals and nRSTOUT are deasserted.

WAKEUP RESET

When S3C2443X is woken up from SLEEP mode by wakeup event, the wakeup reset is invoked. The detail description will be explained in the power management mode section.

Table 2-1 lists alive registers which are not influenced various reset sources except nRESET. With the exception of below registers(in table 2-1), All S3C2443X’s internal registers are reset by above-mentioned reset sources.

Table 2-1. Registers & GPIO status in RESET (R: reset, S: sustain previous value)

Region	Registers	Software	Wakeup	Watchdog	nRESET
SYSCON	OSCSET , PWRCFG, RSTCON, RSTSTAT, WKUPSTAT, INFORM0, INFORM1, INFORM2, INFORM3	S	S	S	R
GPIO	GPFCON, GPFUDP, GPFDAT, GPGCON[7:0], GPGUDP, GPGDAT[7:0], EXTINT0 ~ EXTINT15	R	S	R	R

CLOCK MANAGEMENT

CLOCK GENERATION OVERVIEW

Figure 2-3 shows the block diagram of the clock generation module. The main clock source comes from an external crystal (XTI) or external clock (EXTCLK). The clock generator consists of two PLLs (Phase-Locked-Loop) which generate the high-frequency clock signals required in S3C2443X.

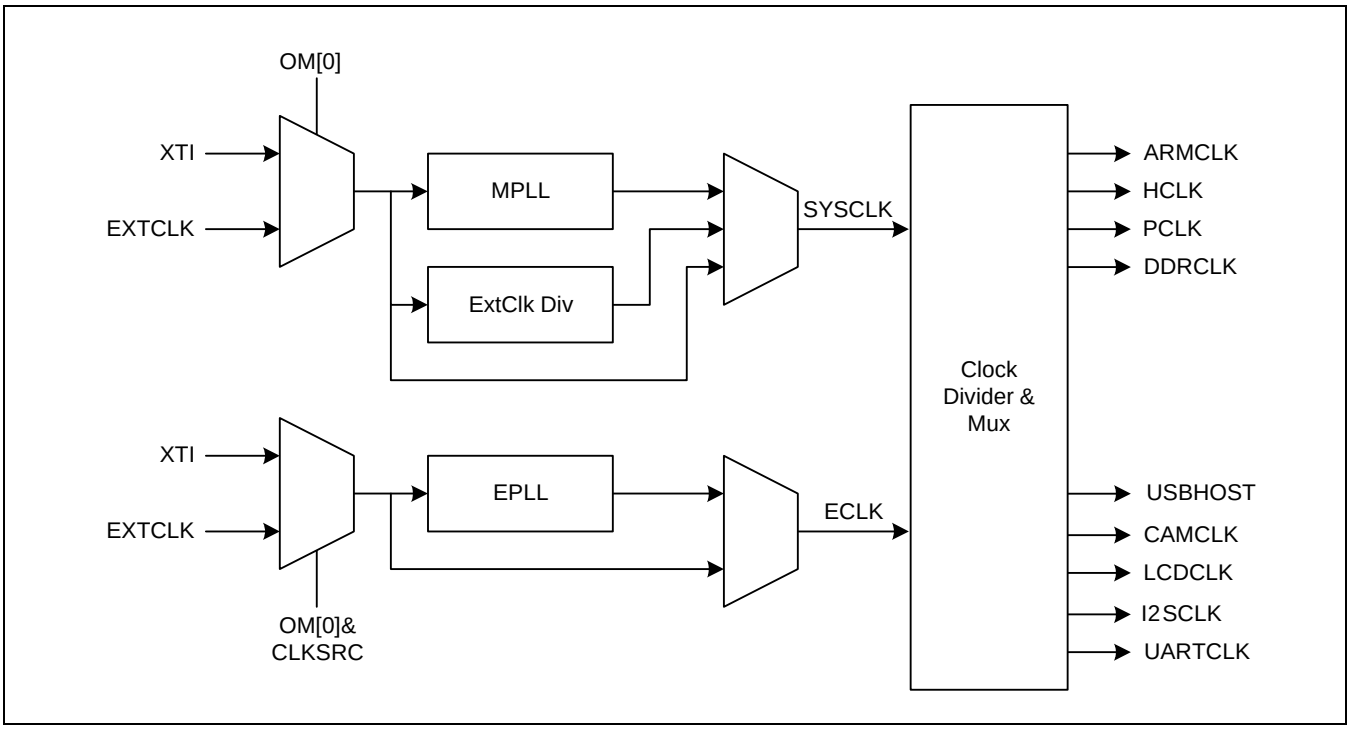


Figure 2-3. Clock generator block diagram

CLOCK SOURCE SELECTION

Table 2-2 and 2-3 show the relationship between the combination of mode control pins OM[0] and the selection of source clock for S3C2443X.

Table 2-2. Clock source selection for the main PLL and clock generation logic[note1]

OM[0]	MPLL Reference Clock (Main clock source)
0	XTI
1	EXTCLK

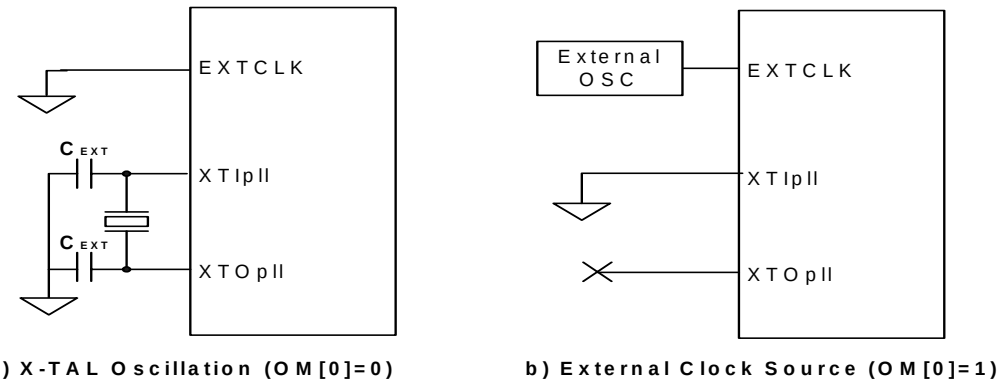
Table 2-3. Clock source selection for the EPLL

CLKSRC[8] (register)	CLKSRC[7] (register)	OM[0]	EPLL Reference Clock
0	X	0	XTI
0	X	1	EXTCLK
1	0	X	XTI
1	1	X	EXTCLK

PLL & Clock Generator generally uses the following conditions.

Loop filter capacitance	C_{LF}	MPLLCAP :Typ. :150pF(142 ~ 175pF)
		EPLLCAP :Typ: 700pF(630 ~ 770pF)
Fin	-	MPLL: 10 – 30 MHz EPLL: 10 – 40 MHz
Fout		MPLL: 300 – 1100 MHz EPLL: 20 – 100 MHz
External capacitance used for X-tal	C_{EXT}	15 – 22 pF

Main Oscillator circuit examples



a) X-TAL Oscillation (OM[0]=0) b) External Clock Source (OM[0]=1)

PLL (PHASE-LOCKED-LOOP)

The PLL (Phase-Locked Loop) frequency synthesizer is constructed in CMOS on single monolithic structure. The PLL provides frequency multiplication capabilities.

MPLL generates the clock sources for ARMCLK, HCLK, PCLK, DDRCLK and SSMCCLK and EPLL generates clock sources for USBHOSTCLK, CAMCLK and so forth.

The following sections describe the operation of the PLL, that includes the phase difference detector, charge pump, VCO (Voltage controlled oscillator), and loop filter.

Refer to MPLLCON and EPLLCON registers to change PLL output frequency.

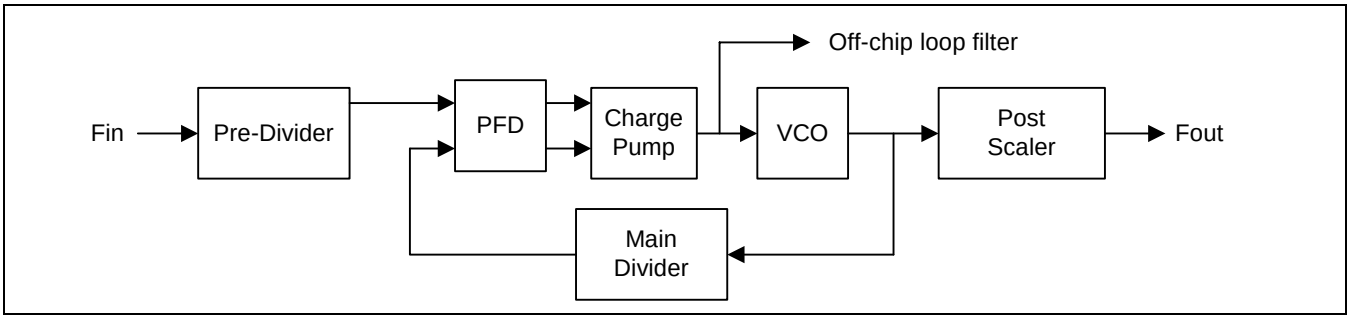


Figure 2-4. PLL(Phase-Locked Loop) Block Diagram

CHANGE PLL SETTINGS IN NORMAL OPERATION

During the operation of S3C2443X in NORMAL mode, if the user wants to change the frequency by writing the PMS value, the PLL lock time is automatically inserted. During the lock time, the clock is not supplied to the internal blocks in S3C2443X. The timing diagram is as follow.

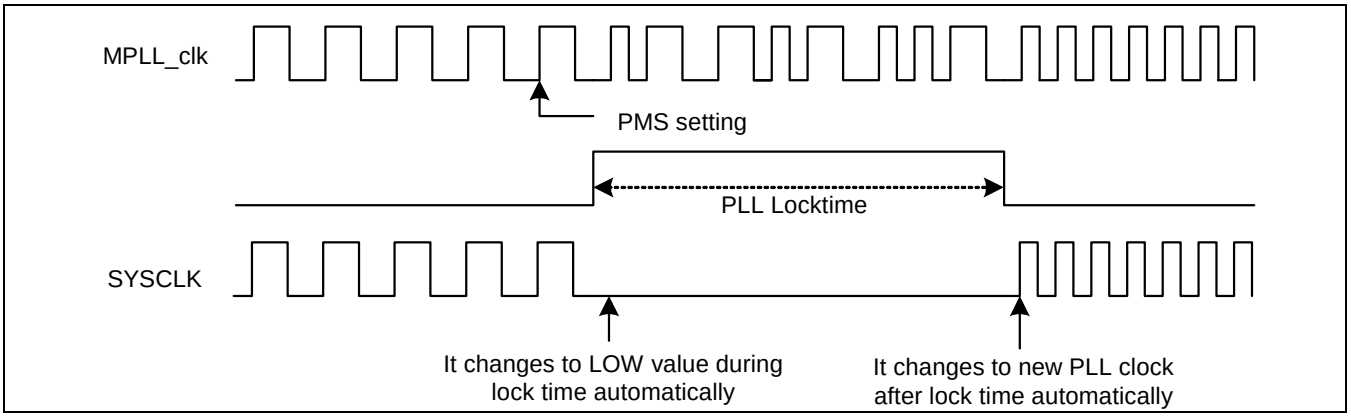


Figure 2-5. The case that changes slow clock by setting PMS value

SYSTEM CLOCK CONTROL

The ARMCLK is used for ARM920T core, the main CPU of S3C2443X. The HCLK is the reference clock for internal AHB bus and peripherals such as the memory controller, the interrupt controller, LCD controller, the DMA, USB host block, System Controller, Power down controller and etc. The PCLK is used for internal APB bus and peripherals such as WDT, IIS, I2C, PWM timer, ADC, UART, GPIO, RTC and SPI etc. DDRCLK is the data strobe clock for DDR memories. CAMclk is used for camera interface block.

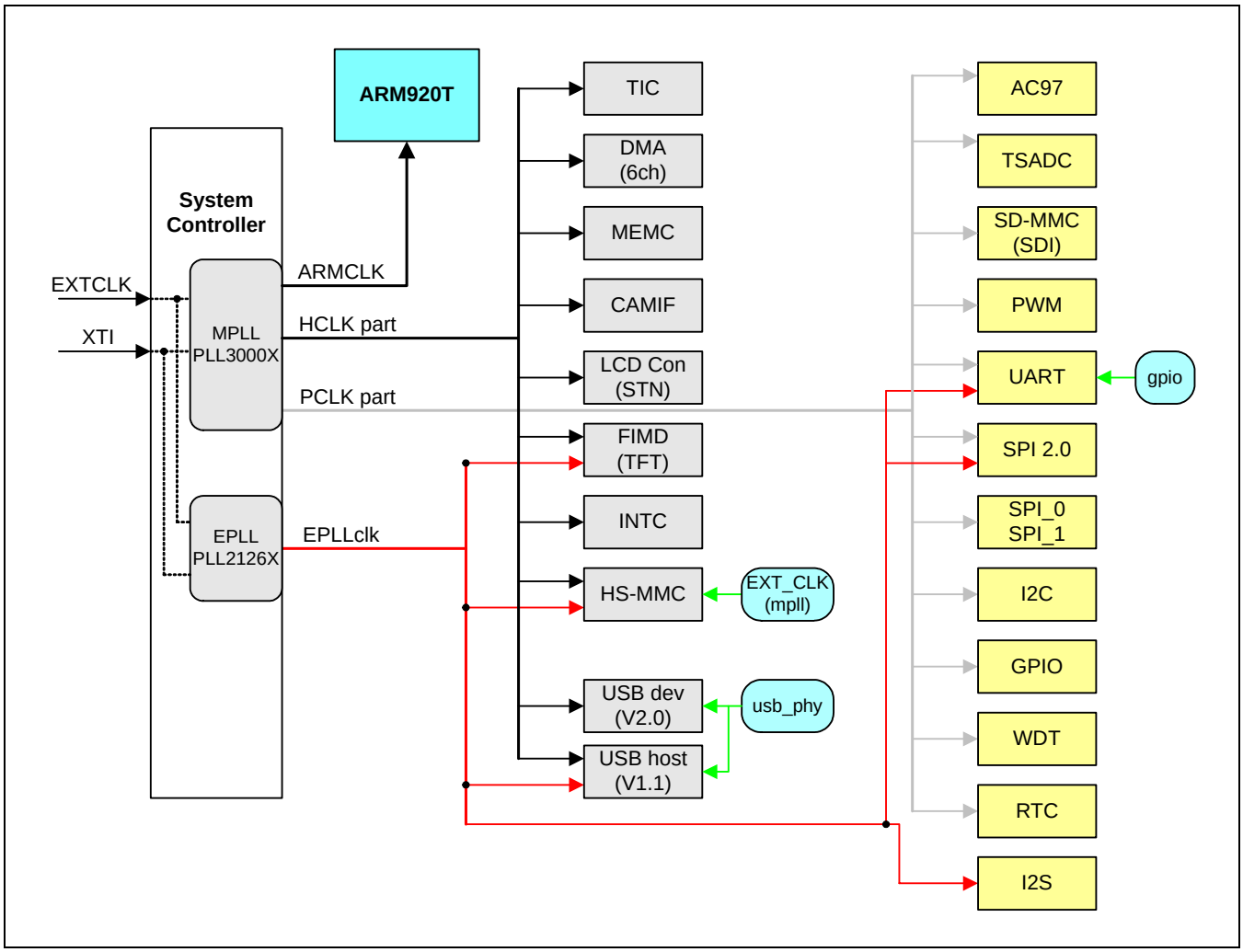


Figure 2-6. The clock distribution block diagram

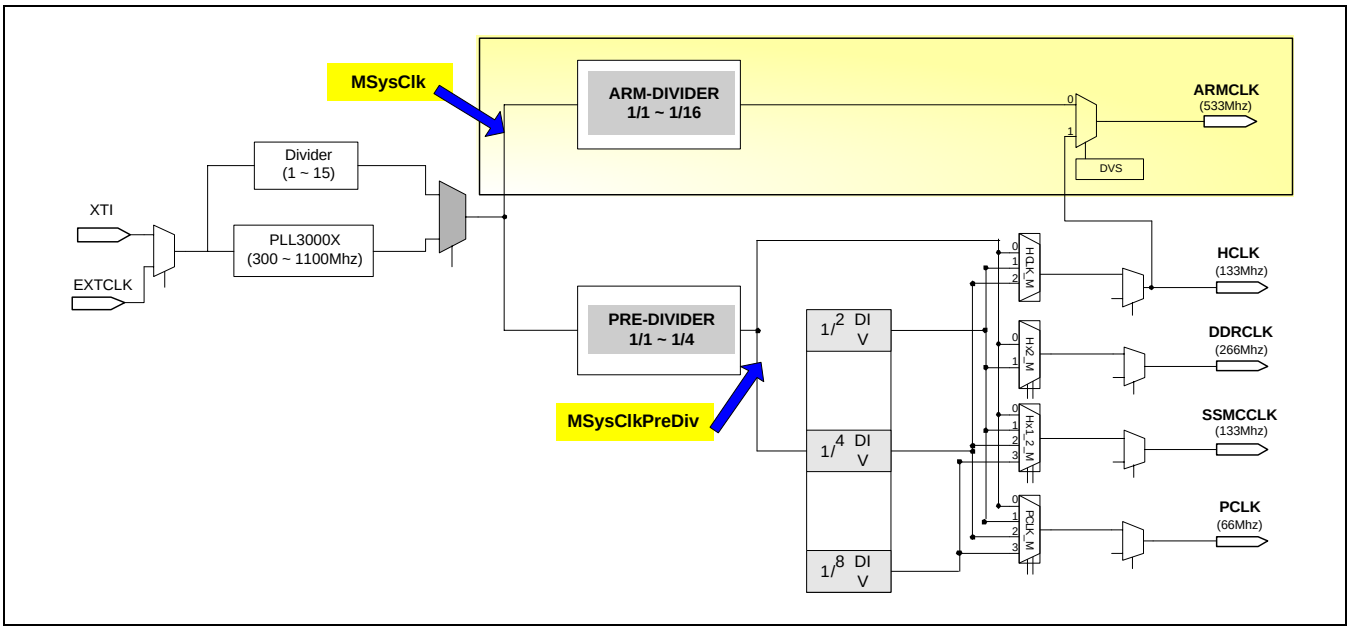


Figure 2-7. MPLL Based clock domain

The MSysClk is the base clock for S3C2443 system clock, such as ARMCLK, HCLK, PCLK, DDRCLK, etc.

The following table shows the clock division ratios between ARMCLK, HLCK and PCLK. This ratio is determined by PREDIV, HCLKDIV and PCLKDIV bits of CLKDIV0 control register.

Table 2-4. Clock division ratio of MPLL region

MPLL Clock Domain						
HCLKDIV	PCLKDIV	Division Ratio (to MSysClk) [HCLK:DDRCLK:PCLK]				ARMCLK(async)
		PREDIV (2'b00)	PREDIV (2'b01)	PREDIV (2'b10)	PREDIV (2'b11)	
2'b00	1'b0	1:1:1	2:2:2	3:3:3	4:4:4	MSysClk
2'b00	1'b1	1:1:2	2:2:4	3:3:6	4:4:8	MSysClk / 2
2'b01	1'b0	2:1:2	4:2:4	6:3:6	8:4:8	MSysClk / 3
2'b01	1'b1	2:1:4	4:2:8	6:3:12	8:4:16	MSysClk / 4
2'b11	1'b0	4:2:4	8:4:8	12:6:12	16:8:16	MSysClk / 6
2'b11	1'b1	4:2:8	8:4:16	12:6:24	16:8:32	MSysClk / 8
						MSysClk / 12
						MSysClk / 16

EXAMPLE FOR CONFIGURING CLOCK REGITER TO PRODUCE SPECIFIC FREQUENCY OF AMBA CLOCKS.

PLL output frequency = 1066Mhz

Target frqeuency

ARMCLK = 533Mhz

HCLK = 133Mhz

PCLK = 66Mhz

DDRCLK = 266Mhz

SSMCCLK = 66Mhz

Register value

ARMDIV = 4'b1000

PREDIV = 2'b01

HCLKDIV = 2'b01

PCLKDIV = 1'b1

HALKHCLK = 1'b1

Figure 2-8 shows EPLL and special clocks for various peripherals

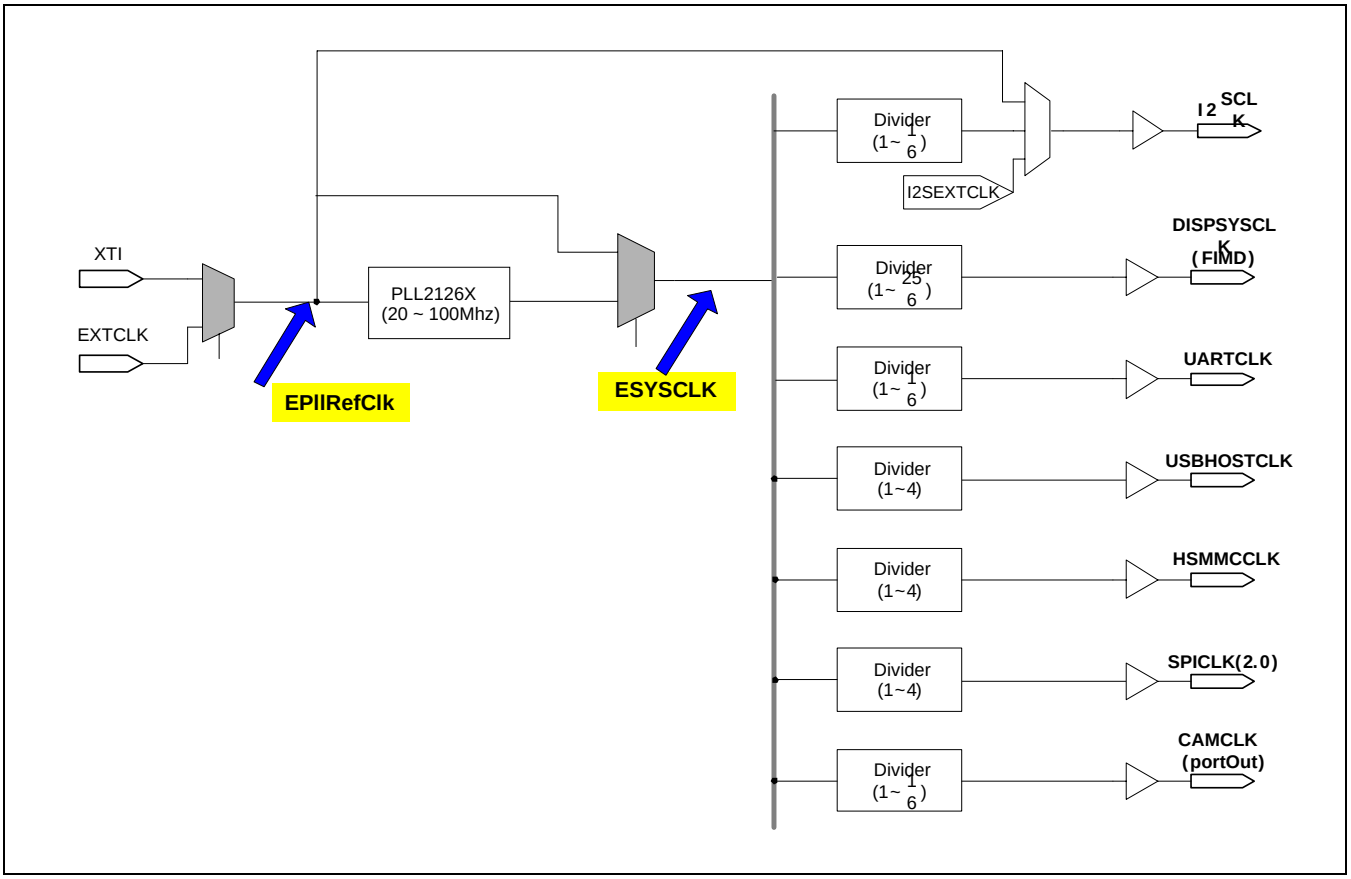


Figure 2-8. EPLL Based clock domain

ESYSCLK CONTROL

Clocks of the EPLL can be used for various peripherals. Each divider value is configured in CLKDIV1 register and all clocks are enabled or disabled by accessing SCLKCON register. According to USB host interface, If you want to get the clock with exact 50% duty cycle, then make EPLL generate 96MHz and divide the clock.

EPLL will be turned off during STOP and SLEEP mode automatically. Also, EPLL will be generated clock to ESYSCLK, after exiting STOP and SLEEP mode if corresponding bits are enabled in SCLKCON register.

Table 2-5. ESYSCLK Control

Condition	ESYSCLK state	EPLL state
After reset	EPLL reference clock	off
After configuring EPLL	During PLL lock time: LOW After PLL lock time: EPLL output	on

POWER MANAGEMENT

The power management block controls the system clocks by software for the reduction of power consumption in S3C2443X. These schemes are related to PLL, clock control logic(ARMCLK, HCLK, PCLK) and wake-up signal. S3C2443X has four power-down modes. The following section describes each power management mode.

Related registers are PWRMODE, PWRCFG and WKUPSTAT.

POWER MODE STATE DIAGRAM

Figure 2-9 shows that Power Saving mode state and Entering or Exiting condition. In general, the entering conditions are set by the main CPU.

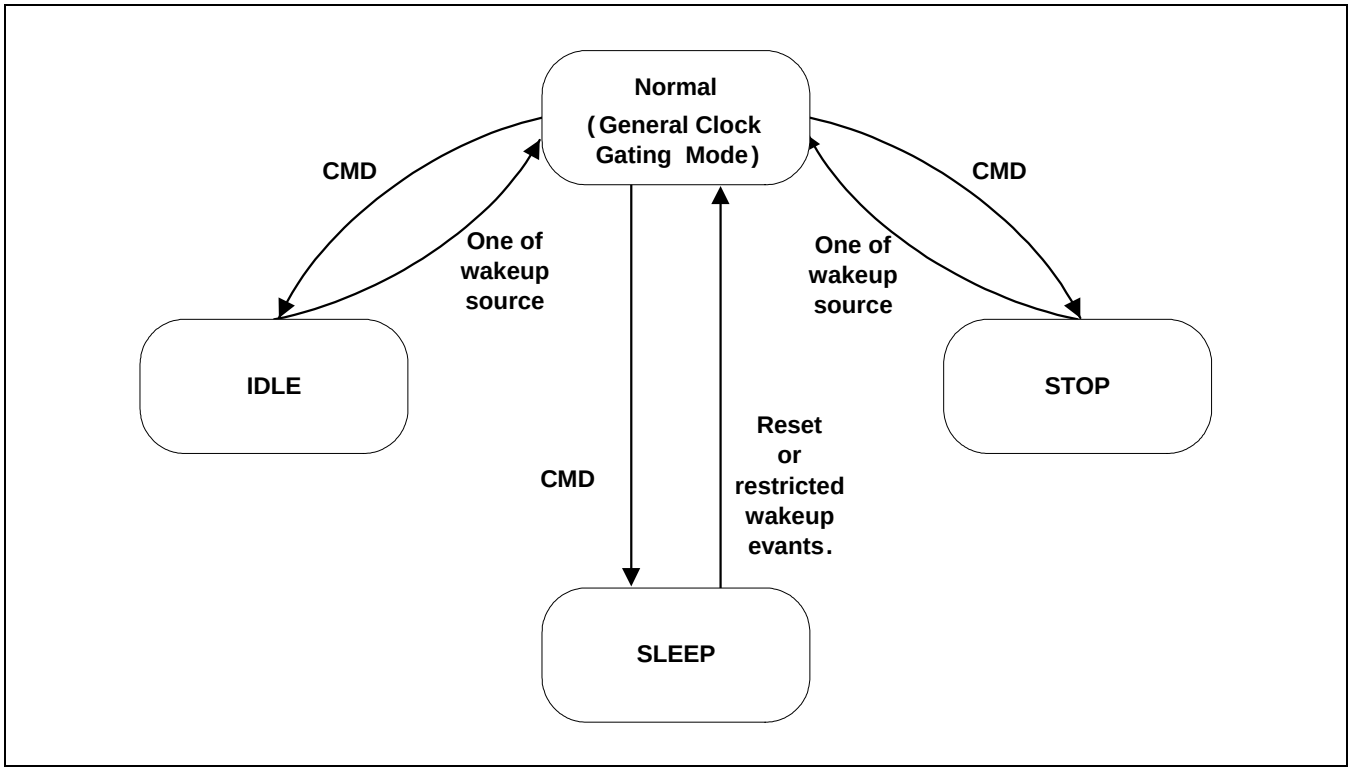


Figure 2-9. Power mode state diagram

POWER SAVING MODES

Normal Mode (General Clock Gating Mode)

In General Clock Gating mode, the On/Off clock gating of the individual clock source of each IP block is performed by controlling of each corresponding clock source enable bit. The Clock Gating is applied instantly whenever the corresponding bit (or bits) is changed. (these bits are set or cleared by the main CPU.)

IDLE Mode

In IDLE mode, the clock to CPU core is stopped. The IDLE mode is activated just after the execution of the STORE instruction that enables the IDLE Mode bit. The IDLE Mode bit should be cleared after the wake-up from the IDLE state for the entering of next IDLE Mode. The H/W logic only detects the low-to-high triggering of the IDLE Mode bit.

STOP Mode

In STOP mode, all clocks are stopped for minimum power consumption. Therefore, the PLL and oscillator circuit are also stopped(oscillator circuit is stopped optionally, see PWRCFG register). The STOP Mode is activated after the execution of the STORE instruction that enables the STOP mode bit. The STOP Mode bit should be cleared after the wake-up from the STOP state for the entering of next STOP mode. The H/W logic only detects the low-to-high triggering of the STOP Mode bit.

To exit from STOP mode, External interrupt, RTC alarm, RTC Tick, or BATT_FLT has to be activated. During the wake-up sequences, the crystal oscillator and PLL may begin to operate. The crystal-oscillator settle-down-time and the PLL locking-time is required to provide stabilized ARMCLK. Those time-waits are automatically inserted by the hardware of S3C2443X. During these time-waits, the clock is not supplied to the internal logic circuitry.

STOP mode Entering sequence[note3] is as follows

1. Set the STOP Mode bit (by the main CPU)
2. System controller requests bus controller to finish current transactions.
3. Bus controller send acknowledge to system controller after completed bus transactions.
4. System controller request memory controller to enter into self refresh mode. It is for preserving contents in SDRAM.
5. System controller wait for self refresh acknowledge from memory controller.
6. After receiving the self-refresh acknowledge, system controller disables system clocks, and switches SYSCLK's source to MPLL reference clock.
7. Disables PLLs and Crystal(XTI) oscillation. If OSC_EN_STOP bit in PWRCFG register is 'high' then system controller doesn't disable crystal oscillation.

note3. DRAM has to be in self-refresh mode during STOP and SLEEP mode to retain valid memory data. LCD must be stopped before STOP and SLEEP mode, because DRAM can't be accessed when it is in self-refresh mode.

STOP mode Exiting sequence is as follows

1. Enable X-tal Oscillator if it is used, and wait the OSC settle down (around 1ms).
2. After the Oscillator settle-down, the System Clock is fed using the PLL input clock and also enable the PLLs and waits the PLL locking time
3. Switching the clock source, now the PLL is the clock source.

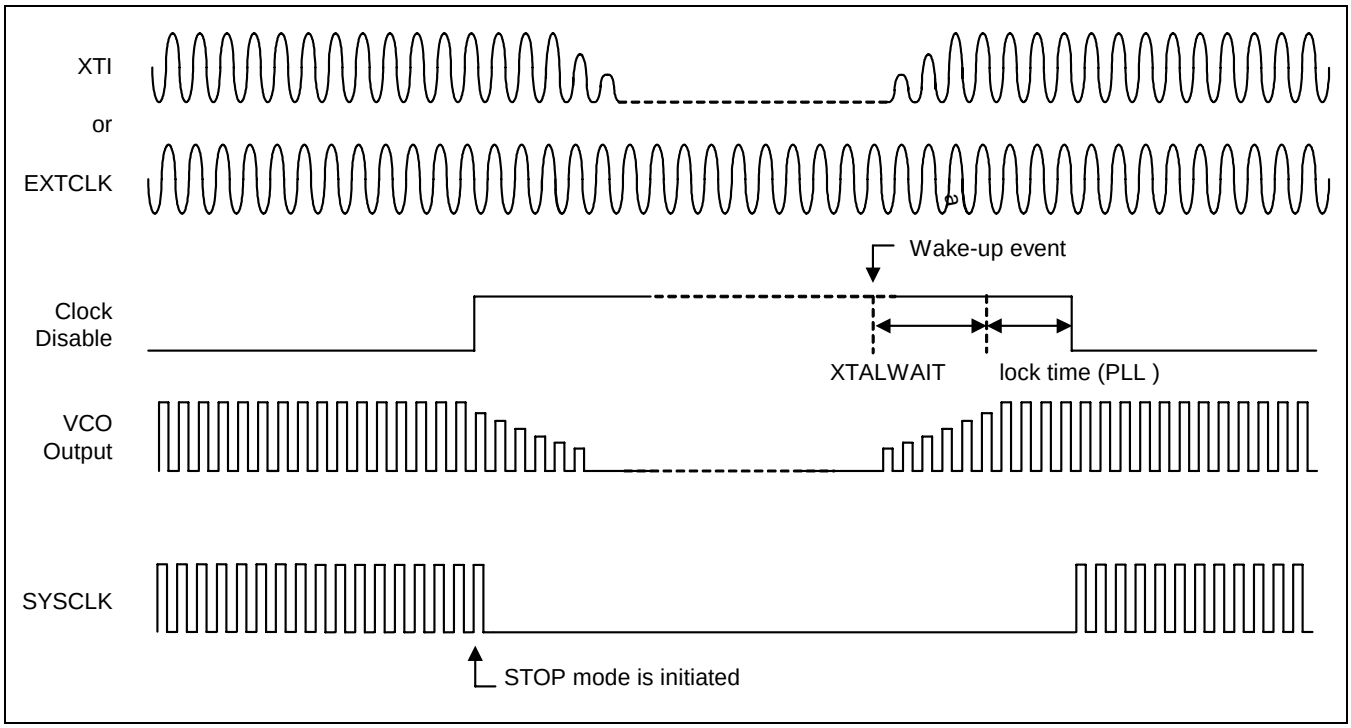


Figure 2-10. Entering STOP mode and exiting STOP mode (wake-up)

SLEEP MODE

In the SLEEP Mode, all the clock sources are off and also the internal logic-power is not supplied except for the wake-up logic circuitry. In this mode, the static power-dissipation of internal logic can be minimized.

SLEEP Mode Entering sequence is as follows.

1. One of the SLEEP Mode entering events is triggered by the system software or by the hardware.
2. System controller requests bus controller to finish current transactions.
3. Bus controller send acknowledge to system controller after completed bus transactions.
4. System controller request memory controller to enter into self refresh mode. It is for preserving contents in SDRAM.
5. System controller wait for self refresh acknowledge from memory controller.
6. After receiving the self-refresh acknowledge, disables the X-tal and PLL oscillation and also disables the external power source for the internal logic by asserting PWR_EN pin to low-state. PWR_EN pin is the regulator-disable control signal for the internal-logic power-source.

SLEEP Mode Exiting sequence is as follows.

1. SYSCON enable external power source by deactivation of the PWR_EN pin and wait power settle down time (it is programmable by a register in the PWRSETCNT field of RSTCON register).
2. SYSCON release the System Reset (synchronously, relatively to the system clock) after the power supply is stabilized.

WAKE-UP EVENT

When S3C2443X wakes up from the STOP Mode by an External Interrupt, a RTC alarm interrupt and other interrupts, the PLL is turned on automatically. The initial-state of S3C2443X after wake-up from the SLEEP Mode is almost the same as the Power-On-Reset state except for the contents of the external DRAM is preserved. In contrast, S3C2443X automatically recovers the previous working state after wake-up from the STOP Mode. The following table shows the states of PLLs and internal clocks after wake-ups from the power-saving modes.

Table 2-6. The status of PLL and ARMCLK after wake-up

Mode before wake-up	PLL on/off after wake-up	SYSCLK after wake-up and before the lock time	SYSCLK after the lock time by internal logic
IDLE	Unchanged	PLL output	PLL output
STOP	PLL state ahead of entering STOP mode (PLL ON or not)	PLL reference clock	SYSCLK ahead of entering STOP mode (PLL output or not)
SLEEP	Off	PLL reference clock	PLL reference(input) clock

OUTPUT PORT STATE AND STOP AND SLEEP MODE

Refer to GPIO chapter.

POWER SAVING MODE ENTERING/EXITING CONDITION

Table 2-7 shows that Power Saving mode state and Entering or Exiting condition. In general, the entering conditions are set by the main CPU.

Pleas refer to power-related registers(PWRMODE, PWRCFG and WKUPSTAT) before apopting power saving scheme on your system.

In dealing with sleep mode, It is good for you to know following two restrictions. To enter sleep mode by BATT_FLT, you have to configure BATF_CFG bits of PWRCFG register. Not to exit from sleep mode when BATT_FLT is LOW, you have to configure SLEEP_CFG bit of PWRCFG register.

Table 2-7. Power saving mode entering/exiting condition

Power down mode	Enter	Exit
Clock Gating at NORMAL	Clear a respective clock on/off bit for each IP to save power.	Set a respective clock on/off bit for each IP to operate normally
IDLE	CMD	1. All interrupt sources 2. RTC alarm 3. RTC Tick 4. BATT_FLT
STOP	CMD	1. EINT[15:0] (External Interrup) 2. RTC alarm 3. RTC Tick 4. BATT_FLT
SLEEP	CMD	1. EINT[15:0] (External Interrupt) 2. RTC alarm 3. RTC Tick 4. BATT_FLT

REGISTER DESCRIPTIONS

The system controller registers are divided into seven categories; clock source control, clock control, power management, reset control, system controller status, bus configuration, and misc. The following section will describe the behavior of the system controller.

ADDRESS MAP

Table summarizes the address map of the system controller.

Table 2-8. System Controller Address Map

Register	Address	R/W	Description	Alive	Reset Value
LOCKCON0	0x4C00_0000	R/W	MPLL lock time count register	X	0x0000_FFFF
LOCKCON1	0x4C00_0004	R/W	EPLL lock time count register	X	0x0000_FFFF
OSCSET	0x4C00_0008	R/W	Oscillator stabilization control register	O	0x0000_8000
reserved	0x4C00_000C	-	reserved		-
MPLLCON	0x4C00_0010	R/W	MPLL configuration register	X	0x0198_0301
RESERVED	0x4C00_0014	-	RESERVED		-
EPLLCON	0x4C00_0018	R/W	EPLL configuration register	X	0x015C_0801
reserved	0x4C00_001C	-	reserved		-
CLKSRC	0x4C00_0020	R/W	Clock source control register	X	0x0000_0000
CLKDIV0	0x4C00_0024	R/W	Clock divider ratio control register0	X	0x0000_000C
CLKDIV1	0x4C00_0028	R/W	Clock divider ratio control register1	X	0x0000_0000
reserved	0x4C00_002C	-	reserved		-
HCLKCON	0x4C00_0030	R/W	HCLK enable register	X	0xFFFF_FFFF
PCLKCON	0x4C00_0034	R/W	PCLK enable register	X	0xFFFF_FFBF
SCLKCON	0x4C00_0038	R/W	Special clock enable register	X	0xFFFF_9FFF
RESERVED	0x4C00_003C	-	reserved		-
PWRMODE	0x4C00_0040	R/W	Power mode control register	X	0x0000_0000
SWRST	0x4C00_0044	R/W	Software reset control register	X	0x0000_0000
reserved	0x4C00_0048	-	reserved		-
reserved	0x4C00_004C	-	reserved		-
BUSPRI0	0x4C00_0050	R/W	Bus priority control register 0	X	0x0000_0000
reserved	0x4C00_0054	-	reserved		-
reserved	0x4C00_0058	-	reserved		-
reserved	0x4C00_005C	-	reserved		-

Table 2-8. System Controller Address Map (Continued)

Register	Address	R/W	Description	Alive	Reset Value
PWRCFG	0x4C00_0060	R/W	Power management configuration register	O	0x0000_0000
RSTCON	0x4C00_0064	R/W	Reset control register	O	0x0000_0101
RSTSTAT	0x4C00_0068	R	Reset status register	O	0x0000_0001
WKUPSTAT	0x4C00_006C	R/W	Wake-up status register	O	0x0000_0000
INFORM0	0x4C00_0070	R/W	SLEEP mode information register 0	O	0x0000_0000
INFORM1	0x4C00_0074	R/W	SLEEP mode information register 1	O	0x0000_0000
INFORM2	0x4C00_0078	R/W	SLEEP mode information register 2	O	0x0000_0000
INFORM3	0x4C00_007C	R/W	SLEEP mode information register 3	O	0x0000_0000
PHYCTRL	0x4C00_0080	R/W	usb phy control register	X	0x0000_0000
PHYPWR	0x4C00_0084	R/W	usb phy power control register	X	0x0000_0000
URSTCON	0x4C00_0088	R/W	usb phy reset control register	X	0x0000_0000
UCLKCON	0x4C00_008C	R/W	usb phy clock control register	X	0x0000_0000

INDIVIDUAL REGISTER DESCRIPTIONS

CLOCK SOURCE CONTROL REGISTERS (LOCKCON0, LOCKCON1, OSCSET, MPLLCON, AND EPLLCON)

The five registers control two internal PLLs and an external oscillator. The output frequency of the PLL is determined by the divider values of MPLLCON and EPLLCON. The stabilization time for PLLs and the oscillator is controlled by LOCKCON0/1 and OSCSET, respectively.

Register	Address	R/W	Description	Reset Value
LOCKCON0	0x4C00_0000	R/W	MPLL lock time count register	0x0000_FFFF
LOCKCON1	0x4C00_0004	R/W	EPLL lock time count register	0x0000_FFFF
OSCSET	0x4C00_0008	R/W	Oscillator stabilization control register	0x0000_8000
MPLLCON	0x4C00_0010	R/W	MPLL configuration register	0x0198_0301
EPLLCON	0x4C00_0018	R/W	EPLL configuration register	0x015C_0801

Conventional PLL requires stabilization duration after the PLL is ON. The duration can be varied according to the device variation. Thus, software must adjust these fields with appropriate values in the LOCKTIME0/1 register whose values mean the number of the external reference clock.

LOCKCON0	Bit	Description	Initial Value
RESERVED	[31:16]	RESERVED	0x0000
M_LTIME	[15:0]	MPLL lock time count value for ARMCLK, HCLK, and PCLK Typically, M_LTIME must be longer than 300 usec.	0xFFFF

LOCKCON1	Bit	Description	Initial Value
RESERVED	[31:16]	RESERVED	0x0000
E_LTIME	[15:0]	EPLL lock time count value for UARTCLK, SPICLK and etc. Typically, E_LTIME must be longer than 150 usec.	0xFFFF

In general, an oscillator requires stabilization time. This register specifies the duration based on the reference clock.

OSCSET	Bit	Description	Initial Value
RESERVED	[31:0]	RESERVED	0x0000
XTALWAIT	[15:0]	Crystal oscillator settle-down wait time, this value is valid when s3c2443 is wakeup by stop mode	0x8000

MPLLCON	Bit	Description	Initial Value
RESERVED	[31]	RESERVED	0
RESERVED	[30:26]	RESERVED	0x00
MPLLEN_STOP	[25]	MPLL ON/OFF in STOP mode. 0:OFF, 1:ON	0
ONOFF	[24]	MPLL ON/OFF. 0:ON, 1:OFF	1
MDIV	[23:16]	MPLL main divider value	0x98
RESERVED	[15:10]	RESERVED	0x0
PDIV	[9:8]	MPLL pre-divider value	0x3
RESERVED	[7:2]	RESERVED	0x00
SDIV	[1:0]	PLL post-divider value	0x1

The output frequencies of **MPLL** can be calculated using the following equations:

$F_{OUT} = (2m \times F_{IN}) / (p \times 2^{S})$ (should be 300~1100Mhz)

$Fvco = (2m \times F_{IN}) / p$ (should be 600~1100Mhz)

where, m = (MDIV + 8), p = PIDV, s = SDIV, Fin = 10~30Mhz

NOTE:

Although there is the equation for choosing PLL value, we strongly recommend only the values in the PLL value recommendation table. If you have to use other values, please contact us.

FIN (MHz)	Target FOUT (MHz)	P (decimal)	M (decimal)	S (decimal)	Duty
12	300	1	17	1	45~55%
12	348	1	21	1	45~55%
12	400	3	92	1	45~55%
12	450	2	67	1	45~55%
12	498	2	75	1	45~55%
12	534	2	81	1	45~55%
12	800	3	92	0	40~60%
12	1068	2	81	0	40~60%

EPLLCON	Bit	Description	Initial Value
RESERVED	[31]	RESERVED	0
RESERVED	[30:26]	RESERVED	0x00
EPLLEN_STOP	[25]	EPLL ON/OFF in STOP mode. 0:OFF, 1:ON	0
ONOFF	[24]	EPLL ON/OFF. 0:ON, 1:OFF	1
MDIV	[23:16]	EPLL main divider value	0x5C
RESERVED	[15:14]	RESERVED	0x0
PDIV	[13:8]	EPLL pre-divider value	0x8
RESERVED	[7:2]	RESERVED	0x00
SDIV	[1:0]	EPLL post-divider value	0x1

The output frequencies of **EPLL** can be calculated using the following equations:

$F_{OUT} = (m \times F_{IN}) / (p \times 2^S)$ (should be 20~100Mhz)

$Fvco = (m \times F_{IN}) / p$ (should be 100~200Mhz)

where, m = (MDIV + 8), p = PIDV+2, s =SDIV, Fin = 10~40Mhz

NOTE:

Although there is the equation for choosing PLL value, we strongly recommend only the values in the PLL value recommendation table. If you have to use other values, please contact us.

FIN (MHz)	FOUT (MHz)	P(decimal)	M(decimal)	S(decimal)	Error [Mhz]
12	36	1	28	2	0
12	48	1	40	2	0
12	60	1	22	1	0
12	72	1	28	1	0
12	84	1	34	1	0
12	96	1	40	1	0

CLOCK CONTROL REGISTER (CLKSRC, CLKDIV, HCLKCON, PCLKCON, AND SCLKCON)

The clock generator within the system controller has many dividers and MUXs to generate appropriate clocks. These clocks are controlled by the clock control registers as described in here.

Register	Address	R/W	Description	Reset Value
CLKSRC	0x4C00_0020	R/W	Clock source control register	0x0000_0000
CLKDIV0	0x4C00_0024	R/W	Clock divider ratio control register0	0x0000_000C
CLKDIV1	0x4C00_0028	R/W	Clock divider ratio control register1	0x0000_0000
HCLKCON	0x4C00_0030	R/W	HCLK enable register	0xFFFF_FFFF
PCLKCON	0x4C00_0034	R/W	PCLK enable register	0xFFFF_FFBF
SCLKCON	0x4C00_0038	R/W	Special clock enable register	0xFFFF_FFFF

The CLKSRC selects the source input of the clocks.

CLKSRC	Bit	Description	Initial Value
RESERVED	[31:16]	RESERVED	0x0_0000
SELI2S	[15:14]	I2S clock source selection 00 = divided clock of EPLL, 01 = external I2S clock 1X = EpllRefClk	0x0
RESERVED	[13:9]	RESERVED	0
SELESRC	[8:7]	Selection EPLL reference clock 10 = XTI, 11 = EXTCLK 0x = identical to that of MPLL reference clock	00
SELEPLL	[6]	ESYSCLK selection (refer to figure 2-8) 0 = EPLL reference clock, 1 = EPLL output	0
RESERVED	[5]	RESERVED	0
SELMPLL	[4]	MSYSCLK selection 0 = MPLL reference clock (produced through clock divider) 1 = MPLL output	0
SELEXTCLK	[3]	Configure MPLL reference clock divider 0 = don't use MPLL reference clock divider (means 1/1 divide ratio) 1 = use MPLL reference clock divider (See EXTDIV field of CLKDIV)	0
RESERVED	[2:0]	RESERVED	0x0

The CLKDIV0 configures the division ratio of each clock generator. The operating speed of ARM can be slow to reduce the overall power dissipation, if software doest not require full operating performance. In this case, the power dissipation due to the ARM core can be reduced if the DVS field is ON. The set of DVS field makes that the operating frequency of ARM is the same as system operating clock (HCLK).

CLKDIV0	Bit	Description	Initial Value
RESERVED	[31:14]	RESERVED	0x0
DVS	[13]	Enable/disable DVS (Dynamic Voltage Scaling) feature 0 = disable 1 = enable (The frequency of ARMCLK is the same frequency of HCLK regardless of ARMDIV field.)	0
ARMDIV	[12:9]	ARM clock divider ratio Be careful that ARMCLK should be equal or faster than HCLK. Supported ratios are follows 1/1 = 4'b0000 have to be configured 1/2 = 4'b1000 have to be configured 1/3 = 4'b0010 have to be configured 1/4 = 4'b1001 have to be configured 1/6 = 4'b1010 have to be configured 1/8 = 4'b1011 have to be configured 1/12 = 4'b1101 have to be configured 1/16 = 4'b1111 have to be configured	0x0
EXTDIV	[8:6]	External clock divider ratio ratio = (MPLL reference clock) / (EXTDIV*2 + 1)	0
PREDIV	[5:4]	Pre Divider for HCLK PREDIV value should be one of 0,1,2,3 Output frequency of PREDIVIDER should be less than 266Mhz	0
HALFHCLK	[3]	HCLKx1_2(SSMC) clock divider ratio, 0 = HCLK, 1 = HCLK/2 User also have to configure SSMC's special register which related with half clock. This value must be same with SMCCR[2:1] (page 5-20)	1
PCLKDIV	[2]	PCLK clock divider ratio, 0 = HCLK, 1 = HCLK / 2 if HCLKDIV=2'b11 or 10, PCLK should be same with HCLK	1
HCLKDIV	[1:0]	HCLK clock divider ratio HCLKDIV value should be one of 0,1,3. (2'b10 is invalid) ratio = (PREDIV+1) * (HCLKDIV + 1)	0x0

CLKDIV1 configures the clock ratio related on EPLL.

CLKDIV1	Bit	Description	Initial Value
RESERVED	[31:30]	RESERVED	0
CAMDIV	[29:26]	CAM clock divider ratio. ratio = CAMDIV + 1	0x0
HSSPIDIV	[25:24]	HS_Spi clock divider ratio, ratio = (HSSPIDIV +1)	0x0
DISPDIV	[23:16]	Display controller clock divider ratio, ratio = (DISPDIV + 1)	0x0
I2SDIV	[15:12]	I2S clock divider ratio, ratio = (I2SDIV + 1)	0x0
UARTDIV	[11:8]	UART clock divider ratio, ratio = (UARTDIV + 1)	0x0
HSMMCDIV	[7:6]	HSMMC clock divider ratio, ratio = (HSMMCDIV + 1)	0x0
USBHOSTDIV	[5:4]	Usb Host clock divider ratio, ratio = (USBHOSTDIV + 1)	0x0
RESERVED	[3:0]	RESERVED	0

The AHB clocks are enabled and disabled by HCLKCON register.

HCLKCON	Bit	Description	Initial Value
RESERVED	[31:20]	RESERVED	1
DRAMC	[19]	Enable HCLK into DRAM controller	1
SSMC	[18]	Enable HCLK into the SSMC block	1
CFC	[17]	Enable HCLK into the CF	1
HSMMC	[16]	Enable HCLK into the HSMMC	1
RESERVED	[15:13]	RESERVED	1
USBDEV	[12]	Enable HCLK into the USB device	1
USBHOST	[11]	Enable HCLK into the USB HOST	1
LCDCON	[10]	Enable HCLK into LCD controller (STN)	1
DISPCON	[9]	Enable HCLK into the display controller	1
CAMIF	[8]	Enable HCLK into the camera interface	1
RESERVED	[7:6]	RESERVED	1
DMA0~5	[5:0]	Enable HCLK into DMA channel 0~5	0x3F

The APB clocks are controlled by PCLKCON register.

PCLKCON	Bit	Description	Initial Value
RESERVED	[31:16]	RESERVED	0x7FF
SPI_1	[15]	Enable PCLK into the SPI_1	1
SPI_0	[14]	Enable PCLK into the SPI_0	1
GPIO	[13]	Enable PCLK into the GPIO	1
RTC	[12]	Enable PCLK into the RTC	1
WDT	[11]	Enable PCLK into the watch dog timer	1
PWM	[10]	Enable PCLK into the PWM	1
I2S	[9]	Enable PCLK into the I2S	1
AC97	[8]	Enable PCLK into the AC97	1
TSADC	[7]	Enable PCLK into the TSADC	1
SPI_HS	[6]	Enable PCLK into the SPI_HS	0
SDI	[5]	Enable PCLK into the SDI (SDMMC)	1
I2C	[4]	Enable PCLK into the I2C	1
UART0~3	[3:0]	Enable PCLK into the UART0~3	0xF

The special clocks are controlled by SCLKCON register. Some blocks in the device require several operating frequencies, i.e., 48 MHz and 24 MHz for USB interface block. Thus, these output frequencies can be controlled by the CLKDIV values.

SCLKCON	Bit	Description	Initial Value
RESERVED	[31:17]	RESERVED	0x7FF
DDRCLK(Hx2CLK)	[16]	Enable DDRCLK (see figure 2-7)	1
SSMCCLK (HX1_2CLK)	[15]	Enable SSMCCLK (see figure 2-7)	1
HSSPICLK	[14]	Enable HS-SPI clock (see figure 2-8)	0
HSMMCCLK_EXT	[13]	Enable HSMMC_EXT clock (EXTCLK)	0
HSMMCCLK	[12]	Enable HSMMC clock (from EPLL output)	1
CAMCLK	[11]	Enable CAM clock (see figure 2-8)	1
DISPCLK	[10]	Enable display controller clock (see figure 2-8)	1
I2SCLK	[9]	Enable I2S clock (see figure 2-8)	1
UARTCLK	[8]	Enable UART clock (see figure 2-8)	1
RESERVED	[7:2]	RESERVED	0x3F
USB HOST	[1]	Enable USB HOST clock (see figure 2-8)	1
RESERVED	[0]	RESERVED	1

POWER MANAGEMENT REGISTERS (PWRMODE AND PWRCFG)

If you want to change the power management mode, you just write a bit(s) into PWRMODE register. Before writing, you must configure condition to wake-up from the power down mode.

Register	Address	R/W	Description	Reset Value
PWRMODE	0x4C00_0040	R/W	Power mode control register	0x0000_0000
PWRCFG	0x4C00_0060	R/W	Power management configuration register	0x0000_0000

S3C2443X consists of three power-down modes, which are IDLE, STOP, and SLEEP. The mode transition from the NORMAL mode occurs when the appropriate value is written into PWRMODE register. If software tries to write illegal value, i.e., tries to set multiple power modes concurrently, then the write operation will be ignored.

PWRMODE	Bit	Description	Initial Value
RESERVED	[31:18]	RESERVED	0x0_0000
IDLE	[17]	The system enters into IDLE mode when this field is set to ‘1’.	0
STOP	[16]	The system enters into STOP mode when this field is set to ‘1’.	0
SLEEP	[15:0]	The system enters into SLEEP mode when this field is set to ‘0x2BED’. The bit pattern, ‘0x2BED’, represents “Go To BED”.	0

PWRCFG register control the configuration of power mode transition.

PWRCFG	Bit	Description	Initial Value
RESERVED	[31:16]	RESERVED	0x0000
SLEEP_CFG	[15]	Enable wakeup source 0 = wakeup sources are enabled depending on BATT_FLT in sleep mode. If BATT_FLT pin is asserted logic '1' system can be exit from sleep mode by appropriate wakeup sources. If not, system continuously remain it's sleep state. 1 = enable wakeup sources regardless of BATT_FLT in sleep mode.	0
RESERVED	[14:10]	RESERVED	0x00
NFRESET_CFG	[9]	Reset configuration when internal resets is generated (this bit is valid in software reset & watchdog reset) 0 = reset NAND flash controller. 1 = do not reset NAND flash controller.	0
RTC_CFG	[8]	Configure RTC alarm interrupt wakeup mask 0 = wake-up signal event is generated when RTC alarm ccurs. 1 = mask RTC alarm interrupt	0
RTCTICK_CFG	[7]	Configure RTC Tick interrupt wakeup mask 0 = wake-up signal event is generated when RTC Tick occurs. 1 = mask RTC alarm interrupt	0
RESERVED	[6:5]	RESERVED	0
nSW_PHY_ OFF_USB	[4]	Power on/off of usb phy. (see USB manual to get more details.) 0: OFF 1: ON	0
OSC_EN_SLP	[3]	Crystal oscillator enable bit in SLEEP mode 0 = disable in SLEEP mode, 1 = enable in SLEEP mode	0
OSC_EN_STOP	[2]	Crystal oscillator enable bit in STOP mode 0 = disable in STOP mode, 1 = enable in STOP mode	0
BATF_CFG	[1:0]	Configure BATT_FLT operation 00, 10 = ignore, 01 = generate interrupt in idle mode and can be used as a wakeup source in stop and sleep mode when BATT_FLT is asserted (active LOW) 11 = reserved (Please don't use)	0x0

RESET CONTROL REGISTERS (SWRST AND RSTCON)

Software can reset S3C2443X using SWRST register. The waveform of the reset signals are determined by RSTCON register.

Register	Address	R/W	Description	Reset Value
SWRST	0x4C00_0044	R/W	Software reset control register	0x0000_0000
RSTCON	0x4C00_0064	R/W	Reset control register	0x0000_0101

When software write the predefined value, 0x533C2443, into SWRST register, then the system controller asserts internal reset signal and initializes internal state. The 0x533C2443 means the device code name, S3C2443, since 'S' character has 0x53 in ASCII.

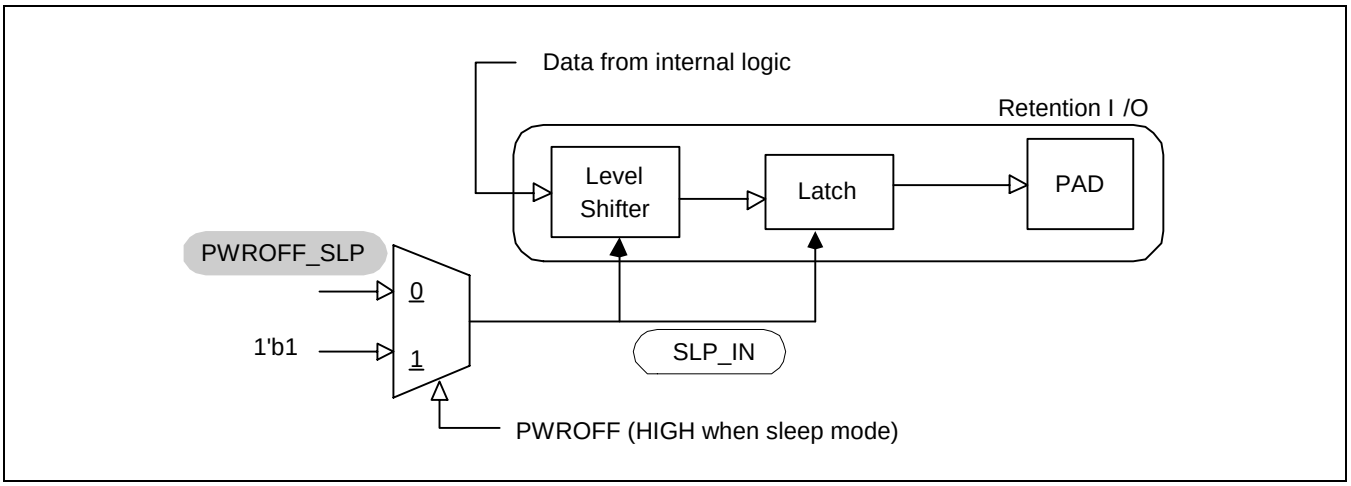
SWRST	Bit	Description	Initial Value
SWRST	[31:0]	If this field has 0x533C2443, then the system will restart.	0x0000_0000

RSTCON register controls the duration of the system reset signal.

RSTCON	Bit	Description	Initial Value
RESERVED	[31:17]	RESERVED	0x0000
PWROFF_SLP	[16]	Power Control on pad retention cell I/O. Retention cell I/O's power will be off when sleep mode, but when wakeup process starts, User should write '1' to produce power on retention I/O (see below detailed description) 1 : set automatically when sleep mode. 0 : cleared by user writing '1'	0
RSTCNT	[15:8]	Only watch dog and software reset can start couter which is counted from RSTCNT value. This RSTCNT value effects delay of releasing reset. After this counter expired, internal reset (like HRESETn) sould be HIGH state.	0x01
PWRSETCNT	[7:0]	This field configures value of Power Settle Down Counter. Only When waking up from sleep mode, Power Settle Down Counter starts counting to wait for stability of external voltage source. As soon as counter reachs PWRSETCNT value, the system escape from sleep mode. Range which user can configure is from 0x01 to 0xFE. (Don't write 0xFF to this field) Real count number = (PWRSETCNT[7:0] + 1) * 2048	0x01

USAGE OF PWROFF_SLP

Control of retention PAD(I/O) when normal mode and wake-up from sleep mode.



S3C2443X has a lot of retention PADs. Retention pad's ability is remaining data when internal logic power is off. In normal mode, PWROFF_SLP signal which from RSTCON register can cotrol about PAD output. If SLP_IN signal has LOW value, data assigned to specific PAD go out through level shifter and latch. Otherwise If SLP_IN signal has HIGH value, output of level shifter cannot pass therefore retention PAD produces latched data only.

When the system enters into a sleep mode, SLP_IN value has HIGH value as a result of PWROFF's HIGH state. Futhermore, PWROFF_SLP register bit is automatically set to 1'b1.

When the system wakeup from sleep mode, SLP_IN still remains HIGH state until user configure PWROFF_SLP bit as 1'b0. Therfore, user has to configure PWROFF_SLP bit to prodce internal logic data through PAD after waking up from sleep mode.

Pin lists that are not affected by PWROFF_SLP

OM[4:0], EINT[15:0], AIN[9:0],

Vref, DM_UDEV, DP_UDEV, REXT, X0_UDEV, X1_UDEV,

ANALOG_TEST, nTRST, TMS, TCK, TDI, TDO,

XTOpll, XTIpll, MPLLCAP, EPLLCAP,

XTIrtc, XTOrtc, nRESET, nRSTOUT, PWREN, BATT_FLT, EXTCLK,

GPF, GPG[7:0]

SYSTEM CONTROLLER STATUS REGISTERS (WKUPSTAT AND RSTSTAT)

Software must know the status of the system controller after wakeup or reset. WKUPSTAT and RSTSTAT registers store the information.

Register	Address	R/W	Description	Reset Value
RSTSTAT	0x4C00_0068	R	Reset status register	0x0000_0001
WKUPSTAT	0x4C00_006C	R/W	Wake-up status register	0x0000_0000

After S3C2443X is resetted or woken-up, the following two registers store the source of the activation. The value of RSTSTAT register is cleared by the other reset. If each bit has '1' value, resets or wakeup events are occurred.

RSTSTAT	Bit	Description	Initial Value
RESERVED	[31:6]	RESERVED	0x0000_000
SWRST	[5]	Reset by software (see SWRST register)	0
RESERVED	[4]	-	0
SLEEP	[3]	Wakeup by RTC_TICK, RTC_ALARM and EINT from power-down mode. *(Reset by waking-up from SLEEP mode)*	0
WDTRST	[2]	Reset by Watch-dog reset	0
RESERVED	[1]	Reserved	0
EXTRST	[0]	External reset by nRESET pin	1

The reset priority is as follows: nRESET > WDTRST > SLEEP > E-SLEEP > SW Reset

WKUPSTAT register indicates that which source was used for changing system state into normal mode from idle, stop and sleep mode. The value of WKUPSTAT register can be cleared by writing '1'.

WKUPSTAT	Bit	Description	Initial Value
RESERVED	[31:6]	RESERVED	0x0000_000
BATF	[5]	Waked-up by BATT_FLT assertion. This field is valid when PWRCFG[1:0] = 2'b01	0
RTC_TICK	[4]	Waked-up by RTC tick	0
RESERVED	[3:2]	RESERVED	0x0000_000
RTC	[1]	Waked-up by RTC alarm	0
RESERVED	[0]	RESERVED	0

BUS CONFIGURATION REGISTER (BUSPRI0, BUSPRI1, AND BUSMISC)

To improve AHB bus performance, software must control the arbitration scheme and type.

Register	Address	R/W	Description	Reset Value
BUSPRI0	0x4C00_0050	R/W	Bus priority control register 0	0x0000_0000
	0x4C00_0054	-	RESERVED	

S3C2443X consists of eight hierarchical AHB buses. The arbitration priority and order can be configured with BUSPRI0. You can see specific priority number that assigned to each AMBA master in User's Manual section '04-BUS PRIORITIES'.

Each TYPE field of BUSPRI0 register has three possible choices as follows:

1. 2'b00: the fixed type
2. 2'b01: the last granted maser has the lowest priority
3. 2'b10: the rotated type
4. 2'b11: undefined

<table>
<tr><th>BUSPRI0</th><th>Bit</th><th>Description</th><th>Initial Value</th></tr>
<tr><td>RESERVED</td><td>[31:16]</td><td>RESERVED</td><td>0x0000</td></tr>
<tr><td>TYPE_S</td><td>[15:14]</td><td>Priority type for AHB-System bus</td><td>0x0</td></tr>
<tr><td>RESERVED</td><td>[13:12]</td><td>RESERVED</td><td>0x0</td></tr>
<tr><td>ORDER_S</td><td>[11:8]</td><td>Fixed priority order for AHB-S bus
<table>
<tr><th>Value</th><th>Priority</th><th>Value</th><th>Priority</th></tr>
<tr><td>4’h0</td><td>0-1-2-3-4-5-6-7-8-9-10-11-12</td><td>4’h8</td><td>8-9-10-11-12-0-1-2-3-4-5-6-7</td></tr>
<tr><td>4’h1</td><td>1-2-3-4-5-6-7-8-9-10-11-12-0</td><td>4’h9</td><td>9-10-11-12-0-1-2-3-4-5-6-7-8</td></tr>
<tr><td>4’h2</td><td>2-3-4-5-6-7-8-9-10-11-12-0-1</td><td>4’ha</td><td>10-11-12-0-1-2-3-4-5-6-7-8-9</td></tr>
<tr><td>4’h3</td><td>3-4-5-6-7-8-9-10-11-12-0-1-2</td><td>4’hb</td><td>11-12-0-1-2-3-4-5-6-7-8-9-10</td></tr>
<tr><td>4’h4</td><td>4-5-6-7-8-9-10-11-12-0-1-2-3</td><td>4’hc</td><td>12-0-1-2-3-4-5-6-7-8-9-10-11</td></tr>
<tr><td>4’h5</td><td>5-6-7-8-9-10-11-12-0-1-2-3-4</td><td>4’hd</td><td>undefined</td></tr>
<tr><td>4’h6</td><td>6-7-8-9-10-11-12-0-1-2-3-4-5</td><td>4’he</td><td>undefined</td></tr>
<tr><td>4’h7</td><td>7-8-9-10-11-12-0-1-2-3-4-5-6</td><td>4’hf</td><td>undefined</td></tr>
</table></td><td>0x0</td></tr>
<tr><td>TYPE_I</td><td>[7:6]</td><td>Priority type for AHB-Image bus</td><td>0x0</td></tr>
<tr><td>RESERVED</td><td>[5:3]</td><td>RESERVED</td><td>0x0</td></tr>
<tr><td>ORDER_I</td><td>[2:0]</td><td>Fixed priority order for AHB-I bus
<table>
<tr><th>Value</th><th>Priority</th><th>Value</th><th>Priority</th></tr>
<tr><td>3’b000</td><td>0-1-2-3-4-5-6</td><td>3’b100</td><td>4-5-6-0-1-2-3</td></tr>
<tr><td>3’b001</td><td>1-2-3-4-5-6-0</td><td>3’b101</td><td>5-6-0-1-2-3-4</td></tr>
<tr><td>3’b010</td><td>2-3-4-5-6-0-1</td><td>3’b110</td><td>6-0-1-2-3-4-5</td></tr>
<tr><td>3’b011</td><td>3-4-5-6-0-1-2</td><td>3’b111</td><td>undefined</td></tr>
</table></td><td>0x0</td></tr>
</table>

MISC. (INFORM0~3)

Register	Address	R/W	Description	Reset Value
INFORM0	0x4C00_0070	R/W	SLEEP mode information register 0	0x0000_0000
INFORM1	0x4C00_0074	R/W	SLEEP mode information register 1	0x0000_0000
INFORM2	0x4C00_0078	R/W	SLEEP mode information register 2	0x0000_0000
INFORM3	0x4C00_007C	R/W	SLEEP mode information register 3	0x0000_0000

INFORM0~3 registers retain their contents during SLEEP mode. Thus, if you want to reserve some important data during SLEEP mode, you can use these registers.

INFORM0~3	Bit	Description	Initial Value
DATA	[31:0]	User specific information	0x0000_0000

USB PHY CONTROL REGISTER (PHYCTRL)

Register	Address	R/W	Description	Reset Value
PHYCTRL	0x4C00_0080	R/W	USB2.0 PHY Control Register	0x0000_0000

PHYCTRL	Bit	Description	Initial State
		RESERVED	0
CLK_SEL	[4:3]	Reference Clock Frequency Select 00 = 48MHz 01 = Reserved 10 = 12MHz 11 = 24MHz	2’b00
EXT_CLK	[2]	Clock Select for XO Block 0 = Crystal 1 = Oscillator	0
INT_PLL_SEL	[1]	Host 1.1 uses Internal PLL Clock (48Mhz) 0 = System PLL Clock (USBHOSTCLK in Figure 2-8 should be 48Mhz and The clk_sel[1:0] bus must be set to 2’b00) 1 = USB Internal PLL Clock	0
DOWNSTREAM_ PORT	[0]	Downstream Port Select 0 = Device (Function) Mode 1 = Host Mode	0

USB PHY POWER CONTROL REGISTER (PHYPWR)

Register	Address	R/W	Description	Reset Value
PHYPWR	0x4C00_0084	R/W	USB2.0 PHY Power Control Register	0x0000_0000

PHYCTRL	Bit	Description	Initial State
COMMON_ON_N	[31]	Force XO(Crystal Oscillator), Bias, Bandgap, and PLL to Remain Powered During a Suspend This signal controls the power-down signals of sub-blocks in the Common block when the USB 2.0 PHY is suspended. • 0: The 48 MHz clock on clk48m_ohci is available at all times, except in Suspend mode. • 1: The 48 MHz clock on clk48m_ohci is available at all times, even in Suspend mode. This signal is a strapping option that must be tied to a valid, static value at all times. Because the signal is a strapping option, this pin is non-critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables. **NOTE:** If common_on_n is set low, clk_ref_ohci and clk12m_ohci are also available, even in Suspend mode. The common_on_n signal overrides xo_on_n.	
		Reserved	
ANALOG_ POWERDOWN	[5:4]	Analog block power down in PHY2.0 01 = Analog block power down others = Analog block power up(Normal Operation)	2'b00
PLL_REF_CLK	[3]	Switch reference clock used in Internal PLL of USB block 0 = External X-tal clock source 1 = Internal System PLL clock source (USBHOSTCLK in Figure 2-8 should be 48Mhz and The clk_sel[1:0] bus must be set to 2'b00)	0
XO_ON	[2]	Force XO Block on During Suspend 1 = XO block is powered up 0 = XO block is powered down when all ports are suspended	0
PLL_ POWERDOWN	[1]	PLL power down in PHY2.0 0 = PLL power up 1 = PLL power down	0
FORCE_ SUSPEND	[0]	Apply Suspend signal for power save 0 = disable (Normal Operation) 1 = enable	0

USB RESET CONTROL REGISTER (URSTCON)

Register	Address	R/W	Description	Reset Value
URSTCON	0x4C00_0088	R/W	USB Reset Control Register	0x0000_0000

ADCPARA	Bit	Description	Initial State
FUNC_RESET	[2]	Function 2.0 S/W Reset 1: reset	0
HOST_RESET	[1]	Host 1.1 S/W Reset 1: reset	0
PHY_RESET	[0]	PHY 2.0 S/W Reset The phy_reset signal must be asserted for at least 10us 1: reset	0

USB CLOCK CONTROL REGISTER (UCLKCON)

Register	Address	R/W	Description	Reset Value
UCLKCON	0x4C00_008C	R/W	USB Clock Control Register	0x0000_0000

MSINTEN	Bit	Description	Initial State
DETECT_VBUS	[31]	Vbus Detect This Vbus indicator signal indicates that the Vbus signal on the USB cable is active. For the serial interface, this signal controls the pull-up resistance on the D+ line in Device mode only. 1: Pull-up resistance on the D+ line is enabled based on the speed of operation. 0: Pull-up resistance on the D+ line is disabled.	0
	[30:5]	Reserved	0
HOST_CLK_TEST	[4]	Host CLK Test mode Enable To ensure correct operations, this field should be set to 1’b1. 0 = Enable 1 = Disable	0
	[3]	Reserved	0
FUNC_CLK_EN	[2]	USB 2.0 Function Clock Enable 0 = disable 1 = enable	0
HOST_CLK_EN	[1]	USB 1.1 Host Clock Enable 0 = disable 1 = enable	0
TCLK_EN	[0]	USB 2.0 PHY Test Clock Enable 0 = disable 1 = enable	0h

3 BUS MATRIX & EBI

OVERVIEW

S3C2443 MATRIX provides the interface between dual AHB bus and Memory sub-system. It is used for achieving high system performance by accessing various kinds of memory (SDRAM, SRAM, Flash Memory, ROM etc) from different AHB bus (one is for system and the other is for image) at the same time. S3C2443 have two MATRIX cores because it has two memory ports, and each MATRIX can select the priority between rotation type and fixed type. User can select which one is excellent for improving system performance.

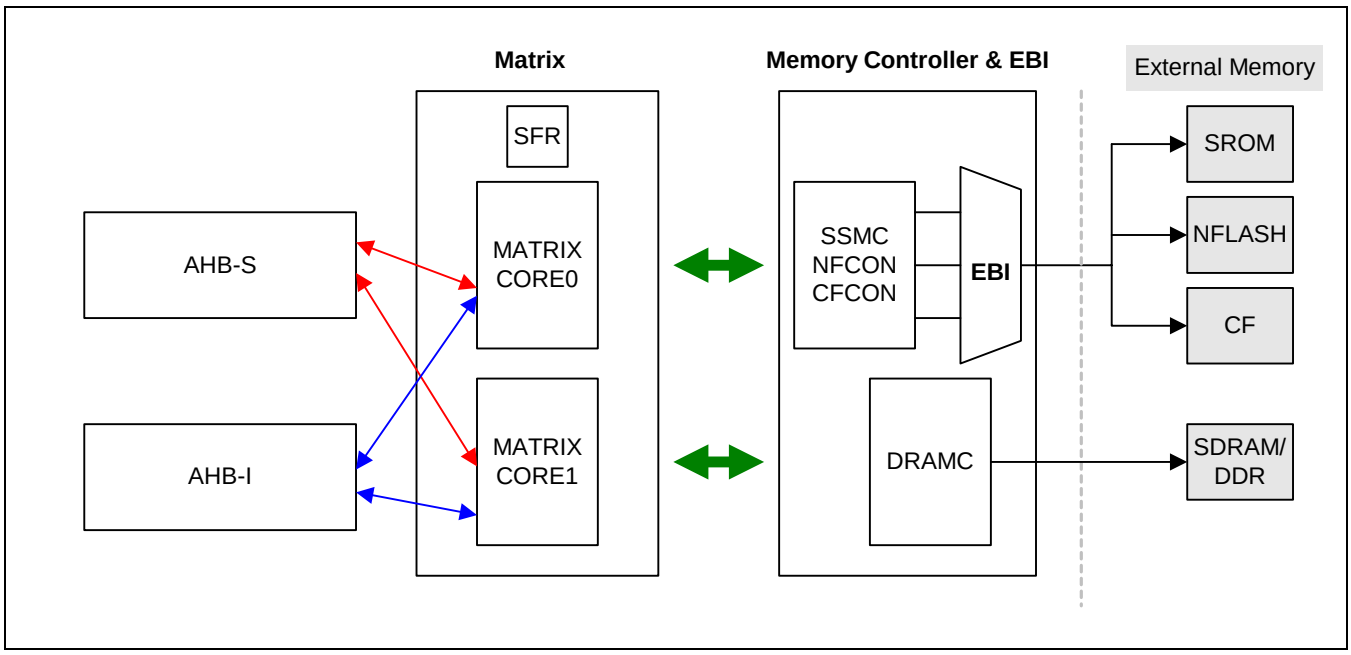


Figure 3-1. The configuration of MATRIX and Memory sub-system of S3C2443

SPECIAL FUNCTION REGISTERS

MATRIX CORE 0 PRIORITY REGISTER (BPRIORITY0)

Register	Address	R/W	Description	Reset Value
BPRIORITY0	0X4E800000	R/W	Matrix Core 0 priority control register	0x0000_0004

BPRIORITY0	Bit	Description	Initial State
PRI_TYP	[2]	Priority type 0: Fixed Type 1: Rotation Type	1
FIX_PRI_TYP	[0]	Priority for the fixed priority type 0: AHB_S > AHB_I 1: AHB_I > AHB_S	0

MATRIX CORE 1 PRIORITY REGISTER (BPRIORITY1)

Register	Address	R/W	Description	Reset Value
BPRIORITY1	0X4E800004	R/W	Matrix Core 1 priority control register	0x0000_0004

BPRIORITY1	Bit	Description	Initial State
PRI_TYP	[2]	Priority type 0: Fixed Type 1: Rotation Type	1
FIX_PRI_TYP	[0]	Priority for the fixed priority type 0: AHB_S > AHB_I 1: AHB_I > AHB_S	0

EBI CONTROL REGISTER (EBICON)

Register	Address	R/W	Description	Reset Value
EBICON	0X4E800008	R/W	EBI control register	0x0000_0004

EBICON	Bit	Description	Initial State
BANK3_CFG	[10]	Bank3 Configuration 0: SROM 1:CF	0
BANK2_CFG	[9]	Bank2 Configuration 0: SROM 1:CF	0
BANK1_CFG	[8]	Bank1 Configuration 0: SROM 1:NAND	0
PRI_TYP	[2]	Priority type 0: Fixed Type 1: Rotation Type	1
FIX_PRI_TYP	[1:0]	Priority for the fixed priority type 0: SSMC > NFCON > CFCON > ExtBusMaster 1: SSMC > CFCON > NFCON > ExtBusMaster 2: SSMC > ExtBusMaster > NFCON > CFCON 3: ExtBusMaster > SSMC > NFCON > CFCON	00

NOTES

4 BUS PRIORITIES

OVERVIEW

The bus arbitration logic determines the priorities of bus masters. It supports a combination of rotation priority mode and fixed priority mode.

BUS PRIORITY MAP

The S3C2443 holds 13 masters on the AHB_S(System Bus), 8 masters on the AHB_I(Image Bus) and 7masters on the APB Bus. The following list shows the priorities among these bus masters after a reset.

Priority	AHB_S BUS MASTERS	Comment
0	CF	1. Fix Type: all priority can be changed according to register value stored in The System Controller. 2 Rotation Type: all masters' priority can be rotatable according to register value stored in The System Controller. (Except for TIC/ARM920T/Default Masters)
1	HS-MMC	
2	DMA0	
3	DMA1	
4	DMA2	
5	DMA3	
6	DMA4	
7	DMA5	
8	UHOST	
9	UDEVICE20	
10	TIC	
11	ARM920T	
12	Default	

Priority	AHB_I BUS MASTERS	Comment
0	CSTN_LCD	1. Fix Type: all priority can be changed according to register value stored in The System Controller. 2 Rotation Type : all masters' priority can be rotatable according to register value stored in The System Controller. (except for Default Master)
1	TFTW1-LCD	
2	TFTW2-LCD	
3	CAMIF_PREVIEW	
4	CAMIF_CODEC	
5	CAMIF_PIP	
6	AHB2AHB	
7	Default	

Priority	APB BUS MASTERS	Comment
0	AHB2APB	AHB2APB Bridge Master obtains always highest priority and the priority of six DMA channels rotate internally.
1	DMA0	
2	DMA1	
3	DMA2	
4	DMA3	
5	DMA4	
6	DMA5	

5 STATIC MEMORY CONTROLLER (SMC)

OVERVIEW

The SMC provides simultaneous support for up to six memory banks (bank0 to bank5) that you can configure independently. Each memory bank supports:

- SRAM
- ROM
- Flash EPROM
- Burst SRAM, ROM, and flash
- OneNAND

You can configure each memory bank to use 8 or 16-bit external memory data paths. You can configure the SMC to support either little-endian or big-endian operation. For example, each memory bank can be configured to support:

- nonburst read and write accesses to high-speed CMOS asynchronous static RAM
- nonburst write accesses, nonburst read accesses, and asynchronous page mode read accesses to fast-boot block flash memory
- synchronous single and burst read and write accesses to synchronous static RAM.

FEATURE

- Supports asynchronous static memory-mapped devices including RAM, ROM, OneNAND and flash
- Supports synchronous static memory-mapped devices including synchronous burst flash
- Supports asynchronous page mode read operation in non-clocked memory subsystems
- Supports asynchronous burst mode read access to burst mode ROM and flash devices
- Supports synchronous burst mode read, write access to burst mode ROM and flash devices
- Supports 8 and 16-bit data bus
- Address space : Up to 64MB per Bank
- Fixed memory bank start address
- External wait to extend the bus cycle
- Support byte, half-word and word access for external memory
- Programmable wait states, up to 31
- Programmable bus turnaround cycles, up to 15
- Programmable output enable and write enable delays, up to 15
- Configurable size at reset for boot memory bank using external control pins
- Support for interfacing to another memory controller using an External Bus Interface (EBI)
- Multiple memory clock frequencies available, HCLK and HCLK/2
- Eight word, 32-bit, wrapping reads from 16-bit memory
- SMBSTWAIT is synchronous burst wait input that the external device uses to delay a synchronous burst transfer for bank 0. When this signal is not used, it shall be driven to high.
- nWAIT is wait mode input from external memory controller. Active HIGH or active LOW, as programmed in the SMC Control Registers for each bank.

BLOCK DIAGRAM

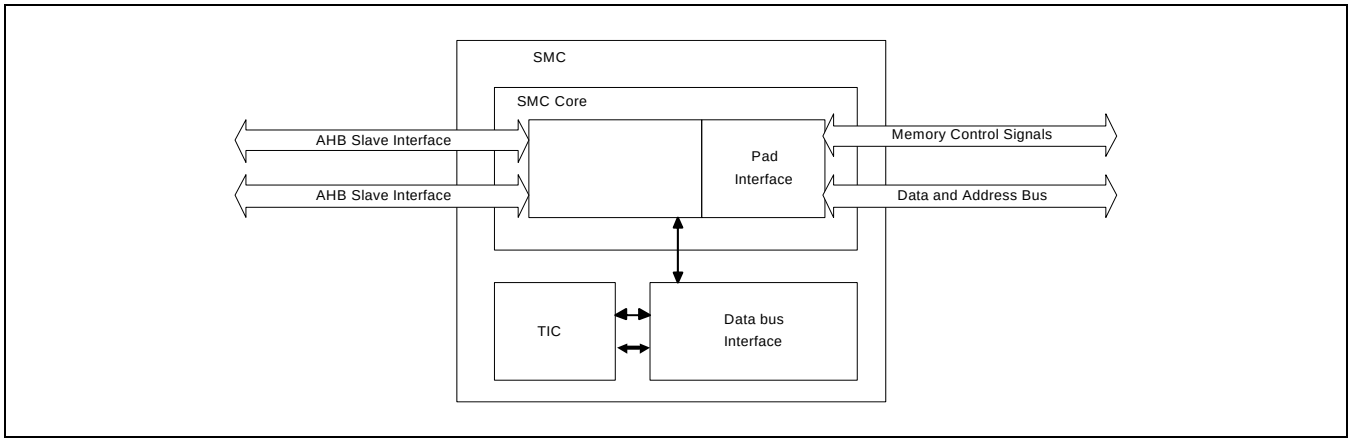


Figure 5-1. SMC Block Diagram

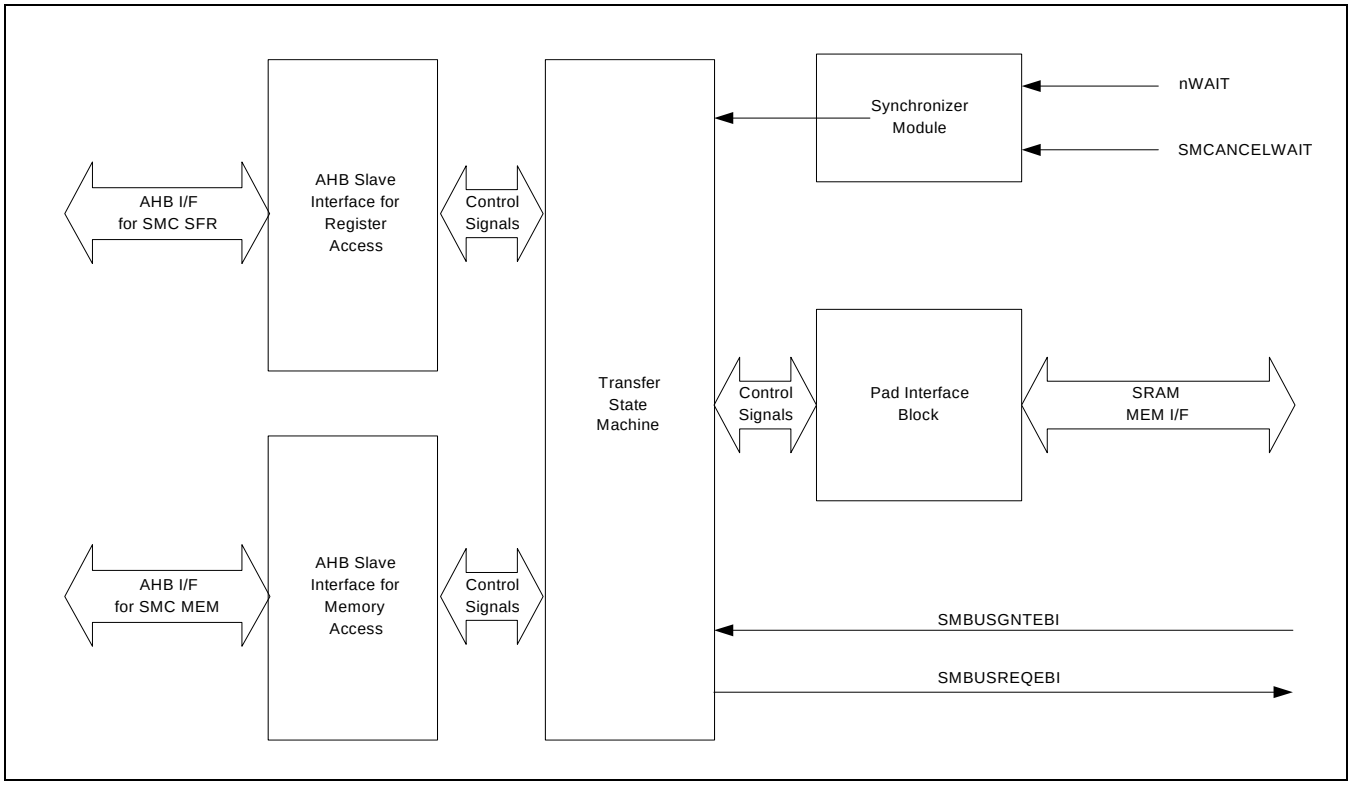


Figure 5-2. SMC Core Block Diagram

ASYNCHRONOUS READ

Figure 5-3 shows an external memory read transfer with two output enable delay states, WSTOEN = 2, and two wait states, WSTRD = 2. Four AHB wait states are inserted during the transfer, two for the standard read, and additional two because of the programmed wait states added.

The PSMAVD signal might be required for synchronous static memory devieces when you use it in asynchronous mode. You can disable this using the AddrValidReadEn bit in the SMBCRx register. This bit defaults to being set (enable) to enable a system to boot from synchronous memory. You can then clear it if you do not require it. When disabled, the signal is driven HIGH continuously.

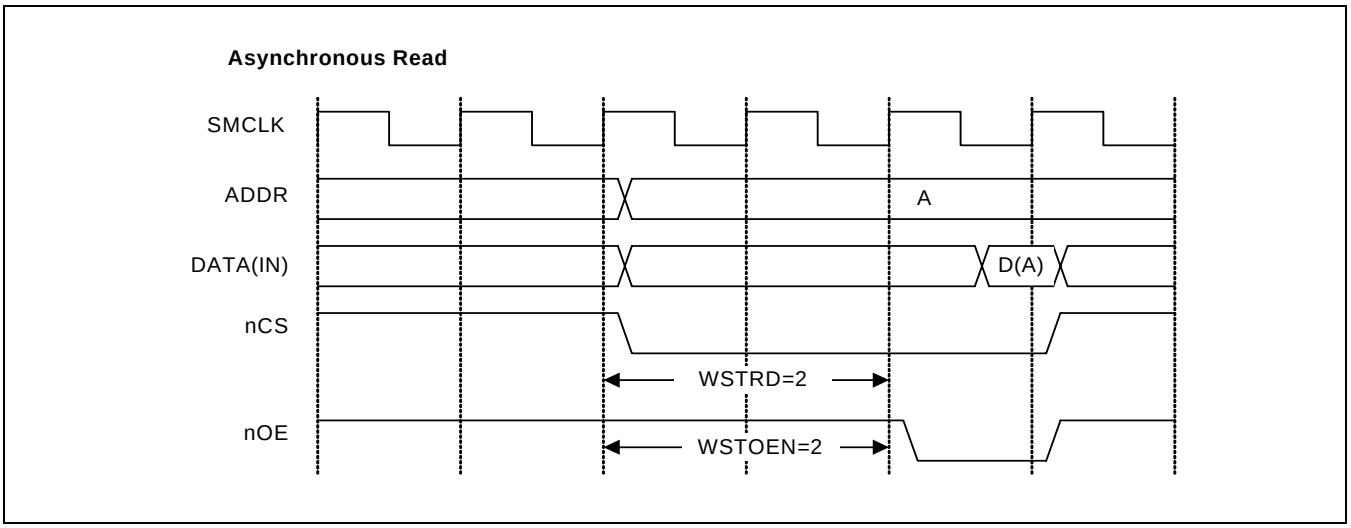


Figure 5-3. External Memory Two Output Enable Delay State Read

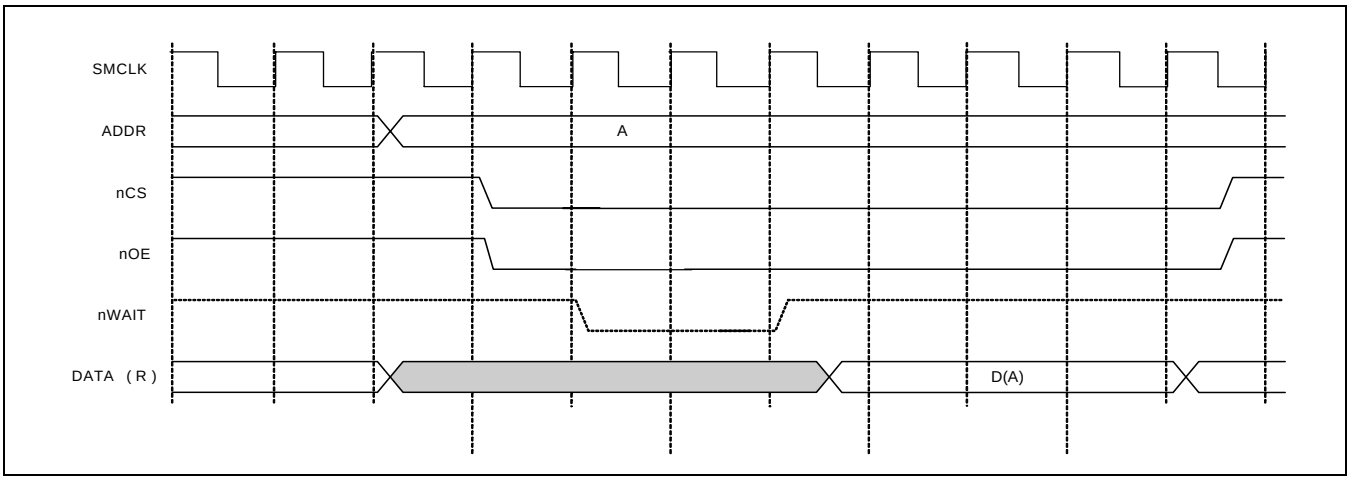


Figure 5-4. Read Timing diagram (DRnCS = 1, DRnOWE = 0)

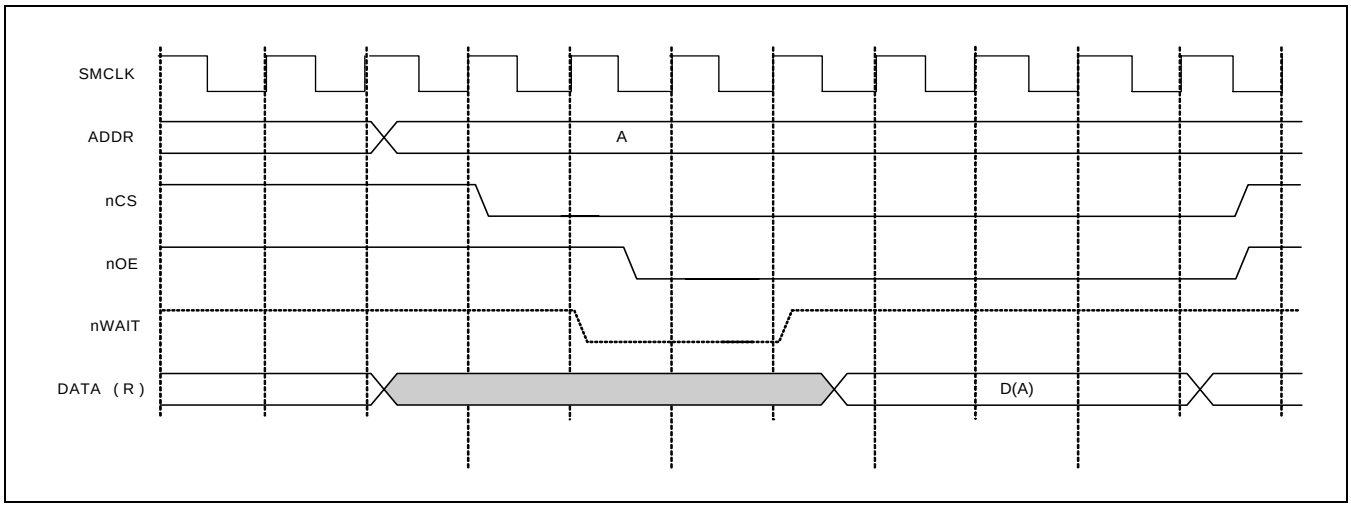


Figure 5-5. Read Timing Diagram (DRnCS = 1, DRnOWE = 1)

ASYNCHRONOUS BURST READ

The SMC supports sequential access asynchronous burst reads to four or eight consecutive locations in 8 or 16-bit memories, as set using the BurstLenRead bits of the Control Register SMBCRx. Burst mode is enabled by setting the Burst Mode bits, BMRead or BMWrite, in the Control register. This feature supports burst mode devices and increases the bandwidth by using a reduced access time (that you can configure) for the sequential reads, WSTBRD, following the first read, WSTRD. The chip select and output enable lines are held during the burst, and only the address changes between subsequent accesses. At the end of the burst the chip select and output enable lines are deasserted together.

Asynchronous page mode read operation is supported. This is enabled by setting the BMRead bit and by setting the burst length using BurstLenRead in the SMBCRx register. Sequential bursts of up to four or eight beats are the only type of access supported for page mode operation.

Figure 5-6 shows an external memory burst read transfer with two initial wait states, and one sequential wait state. The first read has four AHB wait states inserted, and all additional sequential transfers have only one AHB wait state.

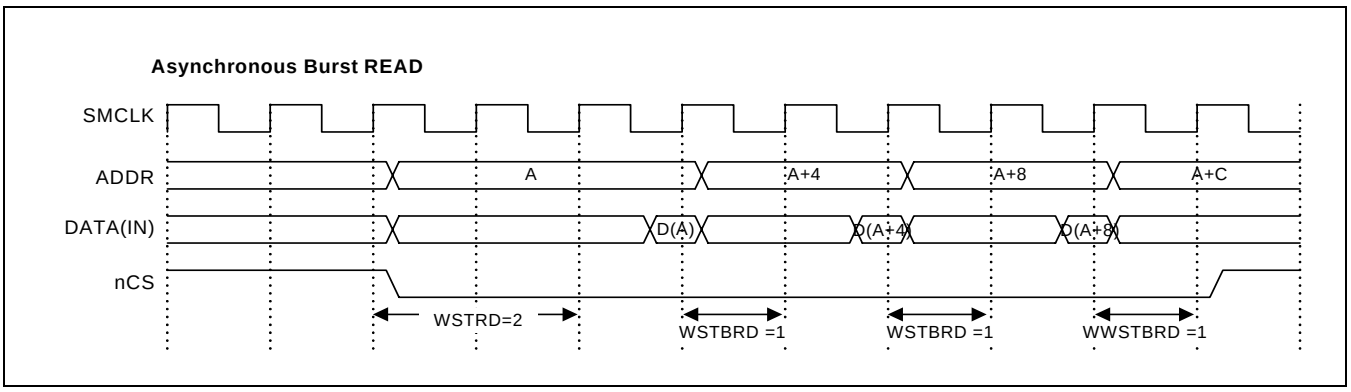


Figure 5-6. External burst ROM with WSTRD=2 and WSTBRD=1 Fixed Length Burst Read

SYNCHRONOUS READ/SYNCHRONOUS BURST READ

Single synchronous read operations have the same control signal timing as an asynchronous read operation, but with different timing requirements for setup and hold relative to the clock. Because the output signals of the SMC are generated internally from clocked logic, the timing for single synchronous reads is the same as for asynchronous reads.

Synchronous burst read transfers are performed differently to asynchronous burst reads, because of the internal address incrementing performed by synchronous burst devices. The PADDR outputs are held with the initial address value, and the PSMAVD output is asserted during the transfer to indicate that the address is valid.

Four, eight, or continuous synchronous burst lengths are supported, and are controlled by the BurstLenRead bits in the Bank Control Register SMBCRx when the SyncEnRead and BMRead bits indicate that the device supports synchronous bursts.

Figure 5-7 shows continuous burst read transfers, where WSTRD = 3 and WSTBRD = 0.

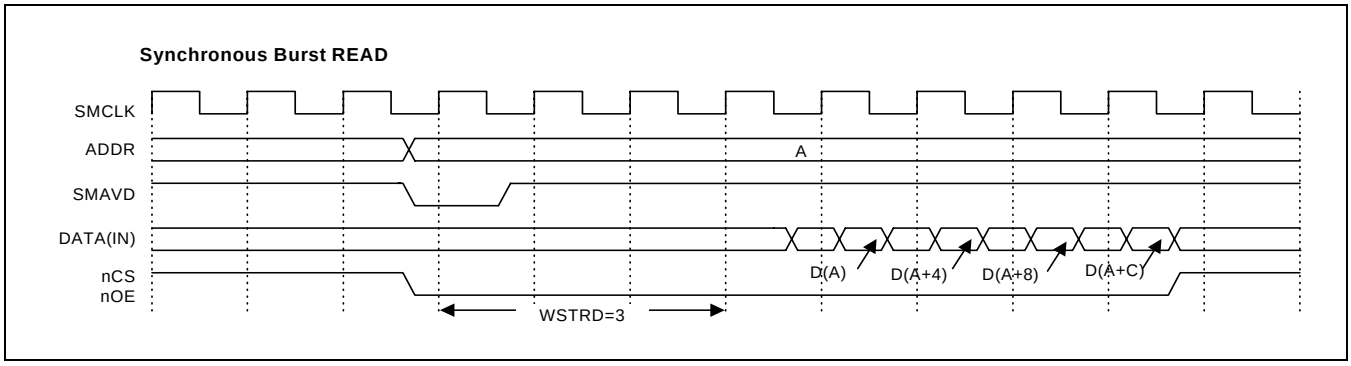


Figure 5-7. External Synchronous Fixed Length Four Transfer Burst Read

ASYNCHRONOUS WRITE

You can program the delay between the assertion of the chip select and the write enable from 0-15 cycles using the WSTWEN bits of the Bank Write Enable Assertion Delay Control Register, SMBWSTWENRx. This reduces the power consumption for memories. The write enable is asserted on the rising edge of nSMMEMCLK, half a clock after the assertion of chip select.

For most asynchronous memory devices an SMMEMCLK cycle is required before the assertion of nWE otherwise there is the hazard that nCS changes after nWE. You can add extra cycles before nWE is asserted using the WSTWEN bits in the Bank Write Enable Assertion Delay Control Registers. For example, setting WSTWR=WSTWEN=1 extends the transfer by one cycle and delays the assertion of nWE by one cycle.

The Write enable is always deasserted half a cycle before the chip select, at the end of the transfer. nSMBLS has the same timing as nSMWEN for writes to 8-bit devices that use the byte lane selects instead of the write enables.

The WSTWEN programmed value must be equal to, or less than the WSTWR programmed value otherwise an invalid access sequence is generated. The access is timed by the WSTWR value and not by the WSTWEN value.

In the External Wait enabled mode, the timing of the transfer (controlled by SMWAIT) is not known. WSTWEN still delays the assertion of nSMWEN. nSMWEN is delayed more by the external wait signal if it has not been asserted when SMWAIT is asserted.

You might require the SMADDRVALID signal for synchronous static memory devices when you use it in asynchronous mode. You can disable it using the AddrValidWriteEn bit in the SMBCRx Register. This bit defaults to being set(enable). You can then clear it if you do not require it. When you disable it, the signal is driven HIGH continuously.

Figure 5-8 shows a single external memory write transfer with two write enable delay states, WSTEN=2, and two wait states, WSTWR=2. A single AHB wait state is inserted.

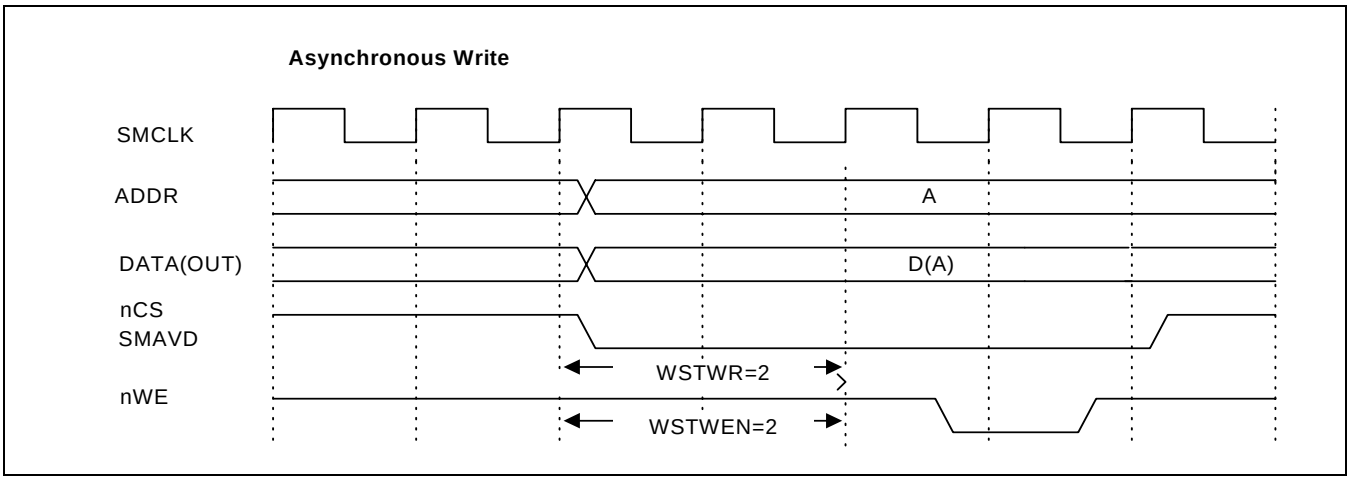


Figure 5-8. External Memory Two Write Enable Delay State Write

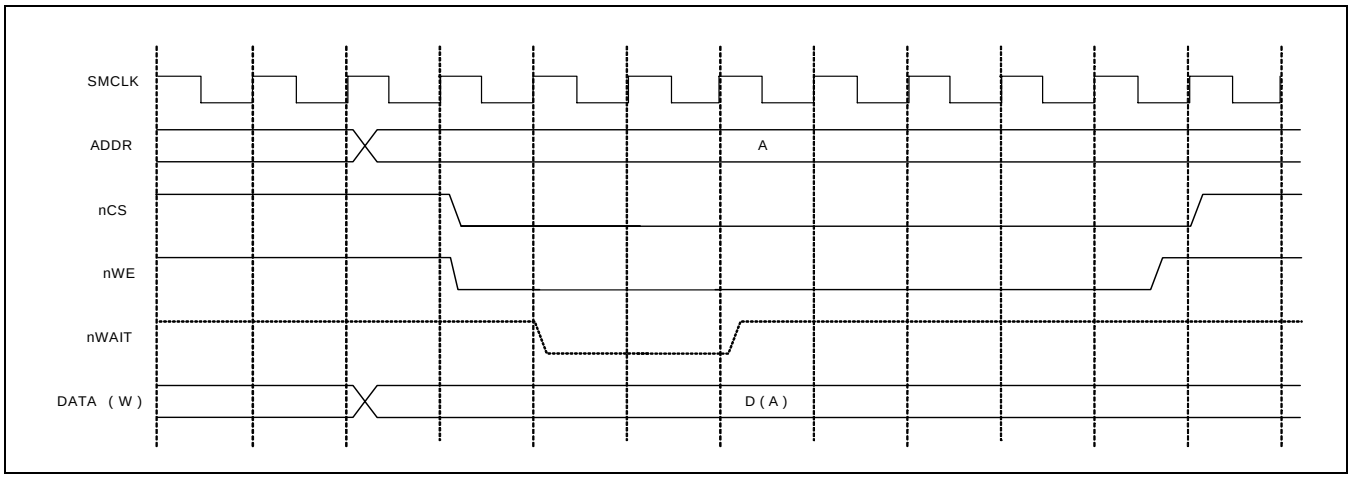


Figure 5-9. Write Timing Diagram (DRnCS = 1, DRnOWE = 0)

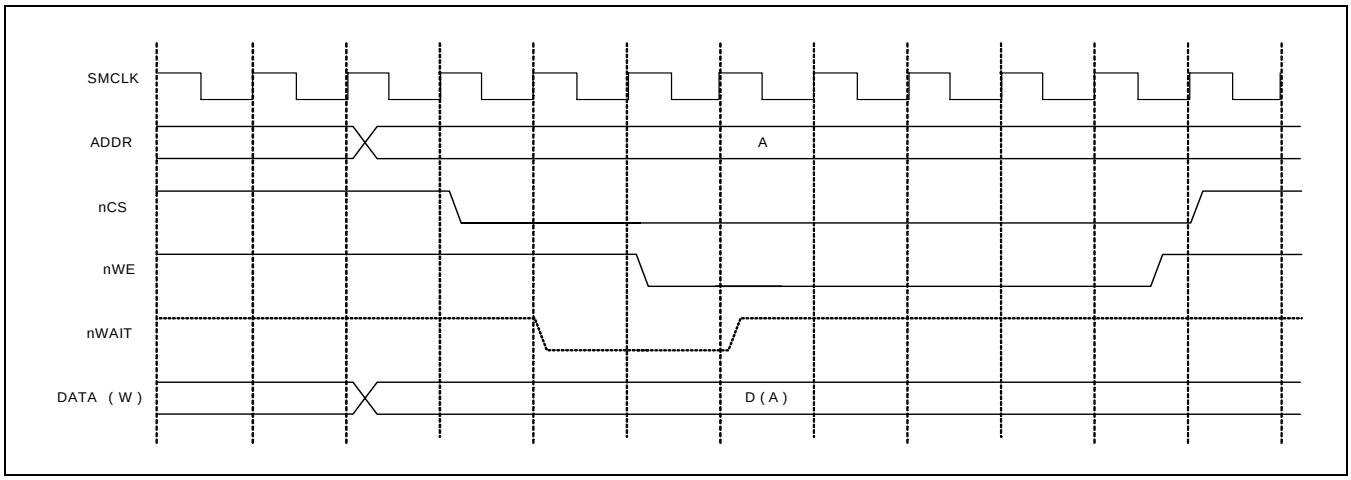


Figure 5-10. Write Timing Diagram (DRnCS = 1, DRnOWE = 1)

SYNCHRONOUS WRITE/ SYNCHRONOUS BURST WRITE

Figure 5-11 shows an example synchronous write operation. In this example the signal SMADDRVALID provides a one-cycle pulse. This behavior is enabled by setting the SyncWriteDev bit in the SMBCRx register. You must also set the AddrValidWriteEn bit for synchronous write.

The signal PnWE is only active for one cycle. This is active at the start of the transfer unless it is delayed using the control bits WSTWEN to delay it.

Synchronous burst writes are supported by the SMC. There is no write buffer so you must delay the AHB transfer to enable the data to be output onto the SMDATA bus. You can control the write in the same way as reads using the bits AddrValidWriteEn, BurstLenWrite, SyncEnWrite, and BMWrite contained in the Bank Control Register, SMCRx.

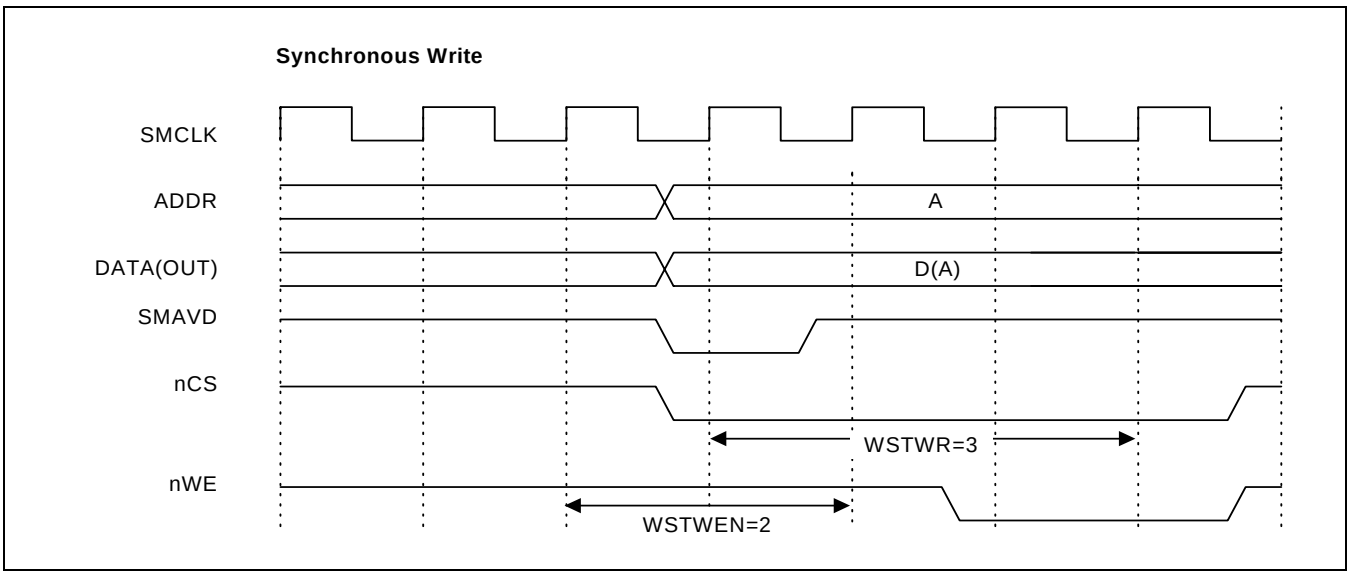


Figure 5-11. Synchronous Two Wait State Write

BUS TURNAROUND

You can configure the SMC for each memory bank to use external bus turnaround cycles between read and write memory accesses. You can program the IDCY field for up to 15 bus turnaround wait states. This avoids bus contention on the external memory data bus. Bus turnaround cycles are generated between external bus transfers as follows:

read-to-read, to different memory banks

read-to-write to the same memory banks

read-to-write to different memory banks

Figure 5-12 shows a zero wait asynchronous read followed by two zero wait asynchronous writes with two turnaround cycles added. The standard minimum of two AHB wait states are added to the read transfer, one is added to the first write, as for any read-write transfer sequence, and three are added to the second write because of insertion of the two turnaround cycles that are only generated after the first write transfer has been detected, and the standard one wait state added when a write transfer is buffered.

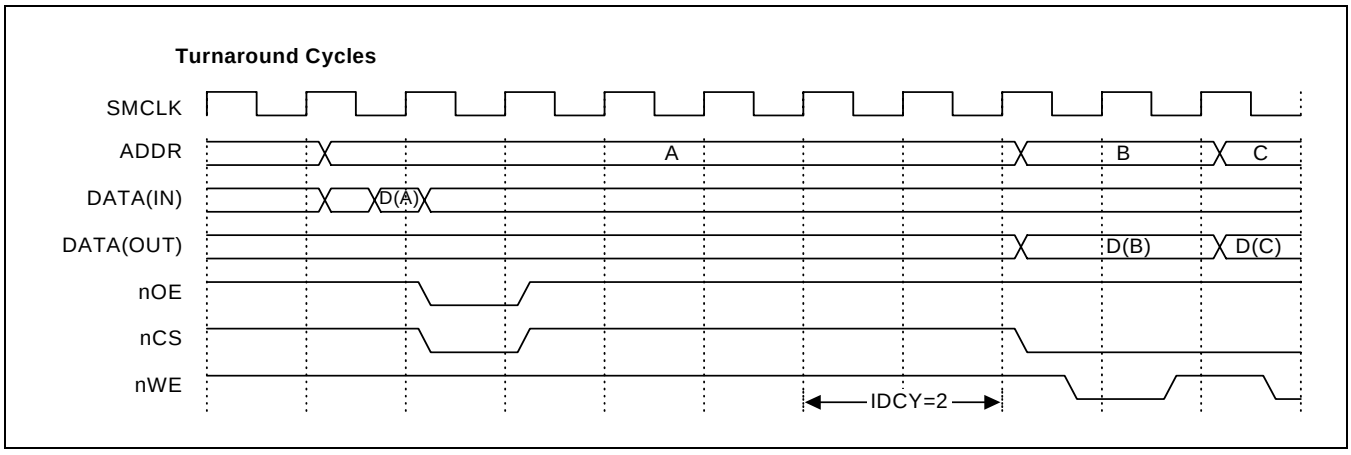


Figure 5-12. Read, then wo Writes (WSTRD=WSTWR=0), Two Turnaround Cycles (IDCY=2)

SRAM Memory Interface Examples

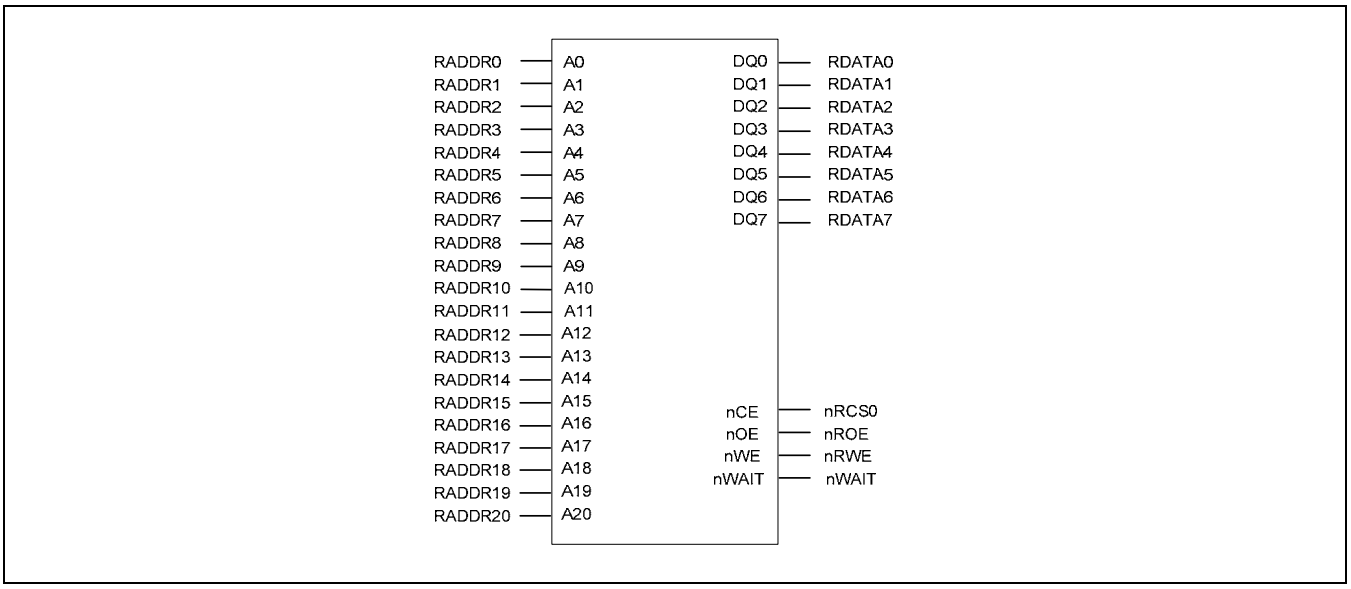


Figure 5-13. Memory Interface with 8-bit SRAM (512KB)

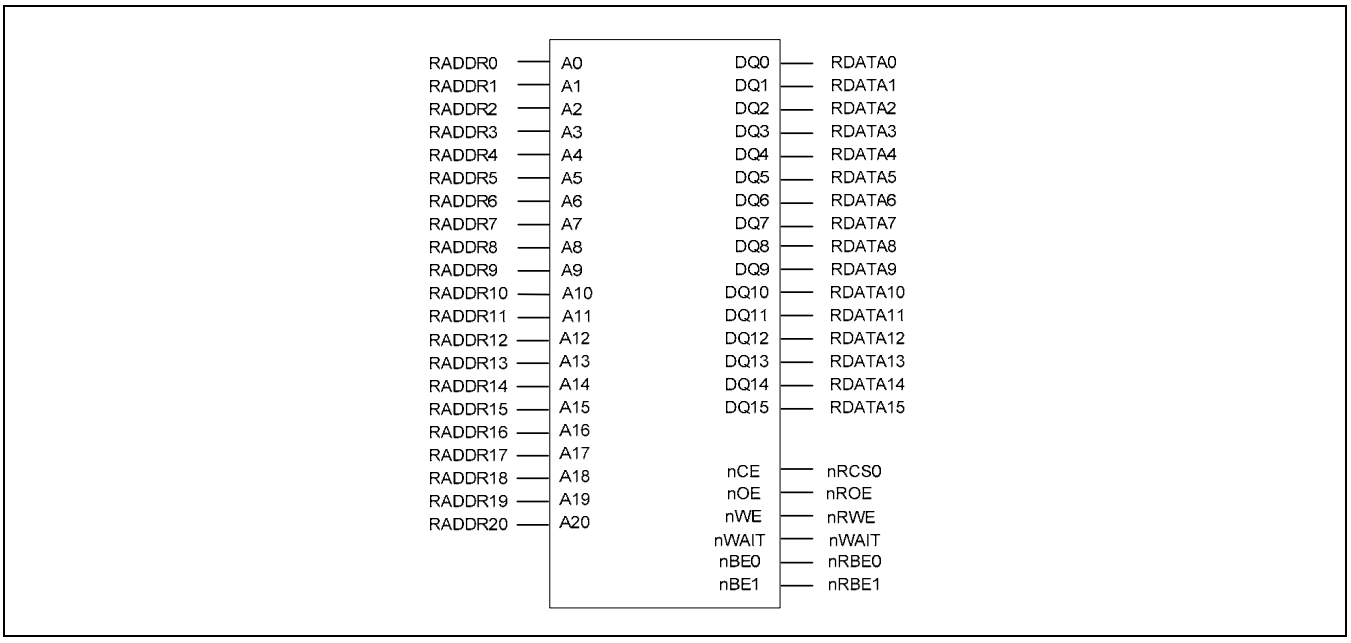


Figure 5-14. Memory Interface with 16-bit SRAM (1MB)

		SRAM/ROM	S3C2443
Addr. connection	8bit data bus	A0	RADDR0
	16bit data bus	A0	RADDR0

SPECIAL REGISTERS

BANK IDLE CYCLE CONTROL REGISTERS 0-5

Register	Address	R/W	Description	Reset Value
SMBIDCYR0	0x4F000000	R/W	Bank0 idle cycle control register	0xF
SMBIDCYR1	0x4F000020	R/W	Bank1 idle cycle control register	0xF
SMBIDCYR2	0x4F000040	R/W	Bank2 idle cycle control register	0xF
SMBIDCYR3	0x4F000060	R/W	Bank3 idle cycle control register	0xF
SMBIDCYR4	0x4F000080	R/W	Bank4 idle cycle control register	0xF
SMBIDCYR5	0x4F0000A0	R/W	Bank5 idle cycle control register	0xF

	Bit	Description	Initial State
	[31:4]	Read undefined. Write as zero.	0x0
IDCY	[3:0]	Idle or turnaround cycles. Default to 1111 at reset. This field controls the number of bus turnaround cycles added between read and write accesses to prevent bus contention on the external memory data bus. Turnaround time = IDCY x SMCLK period	0xF

BANK READ WAIT STATE CONTROL REGISTERS 0-5

Register	Address	R/W	Description	Reset Value
SMBWSTRDR0	0x4F000004	R/W	Bank0 read wait state control register	0x1F
SMBWSTRDR1	0x4F000024	R/W	Bank1 read wait state control register	0x1F
SMBWSTRDR2	0x4F000044	R/W	Bank2 read wait state control register	0x1F
SMBWSTRDR3	0x4F000064	R/W	Bank3 read wait state control register	0x1F
SMBWSTRDR4	0x4F000084	R/W	Bank4 read wait state control register	0x1F
SMBWSTRDR5	0x4F0000A4	R/W	Bank5 read wait state control register	0x1F

	Bit	Description	Initial State
	[31:5]	Read undefined. Write as zero.	0x0
WSTRD	[4:0]	Read wait state. Defaults to 11111 at reset. For SRAM and ROM, the wSTRD field controls the number of wait states for read accesses, and the external wait assertion timing for reads. For burst ROM, the WSTRD field controls the number of wait states for the first read access only. Wait state time = WSTRD x SMCLK period	0x1F

BANK WRITE WAIT STATE CONTROL REGISTERS 0-5

Register	Address	R/W	Description	Reset Value
SMBWSTWRR0	0x4F000008	R/W	Bank0 write wait state control register	0x1F
SMBWSTWRR1	0x4F000028	R/W	Bank1 write wait state control register	0x1F
SMBWSTWRR2	0x4F000048	R/W	Bank2 write wait state control register	0x1F
SMBWSTWRR3	0x4F000068	R/W	Bank3 write wait state control register	0x1F
SMBWSTWRR4	0x4F000088	R/W	Bank4 write wait state control register	0x1F
SMBWSTWRR5	0x4F0000A8	R/W	Bank5 write wait state control register	0x1F

	Bit	Description	Initial State
	[31:5]	Read undefined. Write as zero.	0x0
WSTWR	[4:0]	Write wait state. Defaults to 11111 at reset. For SRAM , the WSTWR field controls the number of wait states for read accesses, and the external wait assertion timing for writes. Wait state time = WSTWR x SMCLK period WSTWR does not apply to read-only devices such as ROM.	0x1F

BANK OUTPUT ENABLE ASSERTION DELAY CONTROL REGISTERS 0-5

Register	Address	R/W	Description	Reset Value
SMBWSTOENR0	0x4F00000C	R/W	Bank0 output enable assertion delay control register	0x2
SMBWSTOENR1	0x4F00002C	R/W	Bank1 output enable assertion delay control register	0x2
SMBWSTOENR2	0x4F00004C	R/W	Bank2 output enable assertion delay control register	0x2
SMBWSTOENR3	0x4F00006C	R/W	Bank3 output enable assertion delay control register	0x2
SMBWSTOENR4	0x4F00008C	R/W	Bank4 output enable assertion delay control register	0x2
SMBWSTOENR5	0x4F0000AC	R/W	Bank5 output enable assertion delay control register	0x2

	Bit	Description	Initial State
	[31:4]	Read undefined. Write as zero.	0x0
WSTOEN	[3:0]	Output enable assertion delay from chip select assertion. Default to 0x2 at reset	0x2

NOTE: If you would use a muxed OneNAND, the regiseter value of WSTOEN should be larger than 2.

BANK WRITE ENABLE ASSERTION DELAY CONTROL REGISTERS 0-5

Register	Address	R/W	Description	Reset Value
SMBWSTWENR 0	0x4F000010	R/W	Bank0 write enable assertion delay control register	0x2
SMBWSTWENR 1	0x4F000030	R/W	Bank1 write enable assertion delay control register	0x2
SMBWSTWENR 2	0x4F000050	R/W	Bank2 write enable assertion delay control register	0x2
SMBWSTWENR 3	0x4F000070	R/W	Bank3 write enable assertion delay control register	0x2
SMBWSTWENR 4	0x4F000090	R/W	Bank4 write enable assertion delay control register	0x2
SMBWSTWENR 5	0x4F0000B0	R/W	Bank5 write enable assertion delay control register	0x2

	Bit	Description	Initial State
	[31:4]	Read undefined. Write as zero.	0x0
WSTWEN	[3:0]	Write enable assertion delay from chip select assertion. Default to 0x2 at reset	0x2

BANK CONTROL REGISTERS 0-5

Register	Address	R/W	Description	Reset Value
SMBCR0	0x4F000014	R/W	Bank0 control register	0x3030x0
SMBCR1	0x4F000034	R/W	Bank1 control register	0x303000
SMBCR2	0x4F000054	R/W	Bank2 control register	0x303010
SMBCR3	0x4F000074	R/W	Bank3 control register	0x303000
SMBCR4	0x4F000094	R/W	Bank4 control register	0x303020
SMBCR5	0x4F0000B4	R/W	Bank5 control register	0x303020

	Bit	Description	Initial State
	[31:22]	Read undefined. Write as zero.	0x0
	[21]	not available(should be high)	0x1
AddrValid WriteEn	[20]	Controls the behavior of the signal RSMAVD during write operations: 0: Signal always HIGH 1: Signal active for asynchronous and synchronous write accesses (default).	0x1
BurstLenWrite	[19:28]	Burst transfer length. Sets the number of sequential transfers that the burst device supports for a write: 00: 4-transfer burst (default) 01: 8-transfer burst 10: Reserved 11: Continuous burst (synchronous only).	0x0
Reserved	[17]	Should be ‘ 0 ’	0x0
BMWrite	[16]	Burst mode write: 0: Nonburst writes to memory devices (default at reset) 1: Burst mode writes to memory devices.	0x0
DRnOWE	[15]	0: No delay (default) 1: Get the delay between nCS signal and nOE/nWE signal. nOE : 2 cycle, nWE : 2 cycle of SMCLK. Note: The only use for Bank1, Bank4, and if DRnCS is set “0”. It must be set “0”.	0x0
WrapRead	[14]	Enables the wrapping burst feature from external memory. This is to support eight word wrapping bursts only. Only valid for burst 16 from 16-bit external memory 0: Disabled (default). 1: Enabled. Note: The SMC supports wrapping reads, but does not support wrapping writes.	0x0
	[13]	not available(should be high)	0x1
AddrValid ReadEn	[12]	Controls the behavior of the signal RSMAVD during read operations: 0: Signal always HIGH. 1: Signal active for asynchronous and synchronous read accesses (default).	0x1
BurstLen Read	[11:10]	Burst transfer length. Sets the number of sequential transfers that the burst device supports for a read: 00: 4-transfer burst. 01: 8-transfer burst. 10: 16-transfer burst. 11: Continuous burst (synchronous only).	0x0

	Bit	Description	Initial State
SyncReadDev	[9]	Synchronous access capable device connected. Access the device using synchronous accesses for reads: 0: Asynchronous device (default). 1: Synchronous device.	0x0
BMRead	[8]	Burst mode read and asynchronous page mode: 0: Nonburst reads from memory devices (default at reset). 1 Burst mode reads from memory devices.	0x0
DRnCS	[7]	0: No delay (defualt) 1: Get the 1 SMCLK cycle delay between ADDR signal and nCS signal. Note: The only use for Bank1, Bank4.	0x0
SMBLSPOL	[6]	Polarity of signal nBE: 0: Signal is active LOW (default). 1: Signal is active HIGH.	0x0
MW	[5:4]	Memory width: 00: 8-bit. 01: 16-bit. 10: Reserved. 11: Reserved. Defaults to different values at reset for each bank.	-
WP	[3]	Write protect: 0: No write protection, for example, SRAM or write enabled Flash (default at reset). 1: Device is write protected, for example, ROM, burst ROM, read-only Flash, or SRAM.	0x0
WaitEn	[2]	External memory controller wait signal enable: 0: The SMC is not controlled by the external wait signal (default at reset). 1: The SMC looks for the external wait input signal, nWAIT.	0x0
WaitPol	[1]	Polarity of the external wait input for activation: 0: The nWAIT signal is active LOW (default at reset). 1: The nWAIT signal is active HIGH.	0x0
RBLE	[0]	Read byte lane enable: 0: nBE[1:0] all deasserted HIGH during system reads from external memory. This is for 8-bit devices where the byte lane enable is connected to the write enable pin so you must deassert it during a read (default at reset). The nBE signals act as write enables in this configuration. 1: nBE[1:0] all asserted LOW during system reads from external memory. This is for 16 or 32-bit devices where you use the separate write enable signal, and you must hold the byte lane selects asserted during a read. The nBE signal acts as the write enable in this configuration.	0x0

BANK STATUS REGISTERS 0-5

Register	Address	R/W	Description	Reset Value
SMBSR0	0x4F000018	R/W	Bank0 status register	0x0
SMBSR1	0x4F000038	R/W	Bank1 status register	0x0
SMBSR2	0x4F000058	R/W	Bank2 status register	0x0
SMBSR3	0x4F000078	R/W	Bank3 status register	0x0
SMBSR4	0x4F000098	R/W	Bank4 status register	0x0
SMBSR5	0x4F0000B8	R/W	Bank5 status register	0x0

	Bit	Description	Initial State
	[31:1]	Read undefined. Write as zero.	0x0
WaitToutErr	[0]	External wait timeout error flag. Reading this bit: 0: No Error (default at reset). 1: External wait timeout error. Writing this bit: 0: Has no effect. 1: Clears the write protect error status flag.	0x0

BANK BURST READ WAIT DELAY CONTROL REGISTERS 0-5

Register	Address	R/W	Description	Reset Value
SMBWSTBRDR0	0x4F00001C	R/W	Bank0 burst read wait delay control register	0x1F
SMBWSTBRDR1	0x4F00003C	R/W	Bank1 burst read wait delay control register	0x1F
SMBWSTBRDR2	0x4F00005C	R/W	Bank2 burst read wait delay control register	0x1F
SMBWSTBRDR3	0x4F00007C	R/W	Bank3 burst read wait delay control register	0x1F
SMBWSTBRDR4	0x4F00009C	R/W	Bank4 burst read wait delay control register	0x1F
SMBWSTBRDR5	0x4F0000BC	R/W	Bank5 burst read wait delay control register	0x1F

	Bit	Description	Initial State
	[31:5]	Read undefined. Write as zero.	0x0
WSTBRD	[4:0]	Burst read wait state. For burst devices, the WSTBRD field controls the number of wait states for the burst read accesses after the first read. Wait state time = WSTBRD x SMCLK period WSTBRD does not apply to nonburst devices.	0x1F

BANK ONENAND TYPE SELECTION REGISTER

Register	Address	R/W	Description	Reset Value
SMBONETYPER	0x4F000100	R/W	SMC Bank OneNAND TYPE SELECTION REGISTER	-

	Bit	Description	Initial State
	[31:6]	Read undefined.	0x0
BANK5TYPE	[5]	0: DEMUXED OneNAND 1: MUXED OneNAND	0x0
BANK4TYPE	[4]	0: DEMUXED OneNAND 1: MUXED OneNAND	0x0
BANK3TYPE	[3]	0: DEMUXED OneNAND 1: MUXED OneNAND	0x0
BANK2TYPE	[2]	0: DEMUXED OneNAND 1: MUXED OneNAND	0x0
BANK1TYPE	[1]	0: DEMUXED OneNAND 1: MUXED OneNAND	0x0
BANK0TYPE	[0]	It's determined by OM[4:2] signals.	-

SMC STATUS REGISTER

Register	Address	R/W	Description	Reset Value
SMCSR	0x4F000200	R	SMC status register	0x0

	Bit	Description	Initial State
	[31:1]	Read undefined.	0x0
WaitStatus	[0]	External wait status, read: 0: nWAIT deasserted. 1: nWAIT asserted. After an externally waited transfer that was terminated early, this bit value can detect when nWAIT is deasserted. At all other times, this bit reads zero.	0x0

SMC CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
SMCCR	0x4F000204	R/W	SMC control register	0x3

	Bit	Description	Initial State
	[31:2]	Read undefined. Write as zero.	0x0
MemClkRatio	[1]	Defines the ratio of SMCLK to HCLK: 0: SMCLK = HCLK. 1: SMCLK = HCLK/2.	0x1
SMClockEn	[0]	SMCLK enable: 0: Clock only active during memory accesses. 1: Clock always running. Clock stopping saves power by stopping SMCLK when it is not required. If clock stopping is enabled before the memory access, the SMC stops SMCLK on the following conditions: • asynchronous read access to asynchronous memory • asynchronous write access to asynchronous memory • asynchronous read access to synchronous memory • asynchronous write access to synchronous memory.	0x1

6 MOBILE DRAM CONTROLLER

OVERVIEW

The S3C2443 Mobile DRAM Controller supports two kinds of memory interface. One is for (Mobile) SDRAM and the other is for mobile DDR memory interface. Mobile DRAM controller provides 2 chip select signals (2 memory banks), these are used for up to 2 (mobile) SDRAM banks or 2 mobile DDR banks. Mobile DRAM controller can't support 2 kinds of memory interface simultaneous, for example one bank for (mobile) SDRAM and one bank for mobile DDR.

Mobile DRAM controller has the following features:

- Mobile DDR SDRAM and (Mobile) SDRAM
  - Supports 16/32-bit data bus interface for (mobile) SDRAM
  - Supports 16-bit data bus interface for mobile DDR
  - Supports up to 1Gbit memory per bank
  - Supports 2 banks: 2-nCS (chip selection)
  - 16-bit Refresh Timer
  - Self Refresh Mode support (controlled by power management)
  - Programmable CAS Latency
  - Provide Write buffer: 8-word size
  - Provide pre-charge and active power down mode
  - Provide power save mode
  - Support EMRS (Extended MRS) for mobile DRAM
    - ♦ DS, TSCR, PASR

BLOCK DIAGRAM

Follow figure 6-1 shows the block diagram of Mobile DRAM Controller

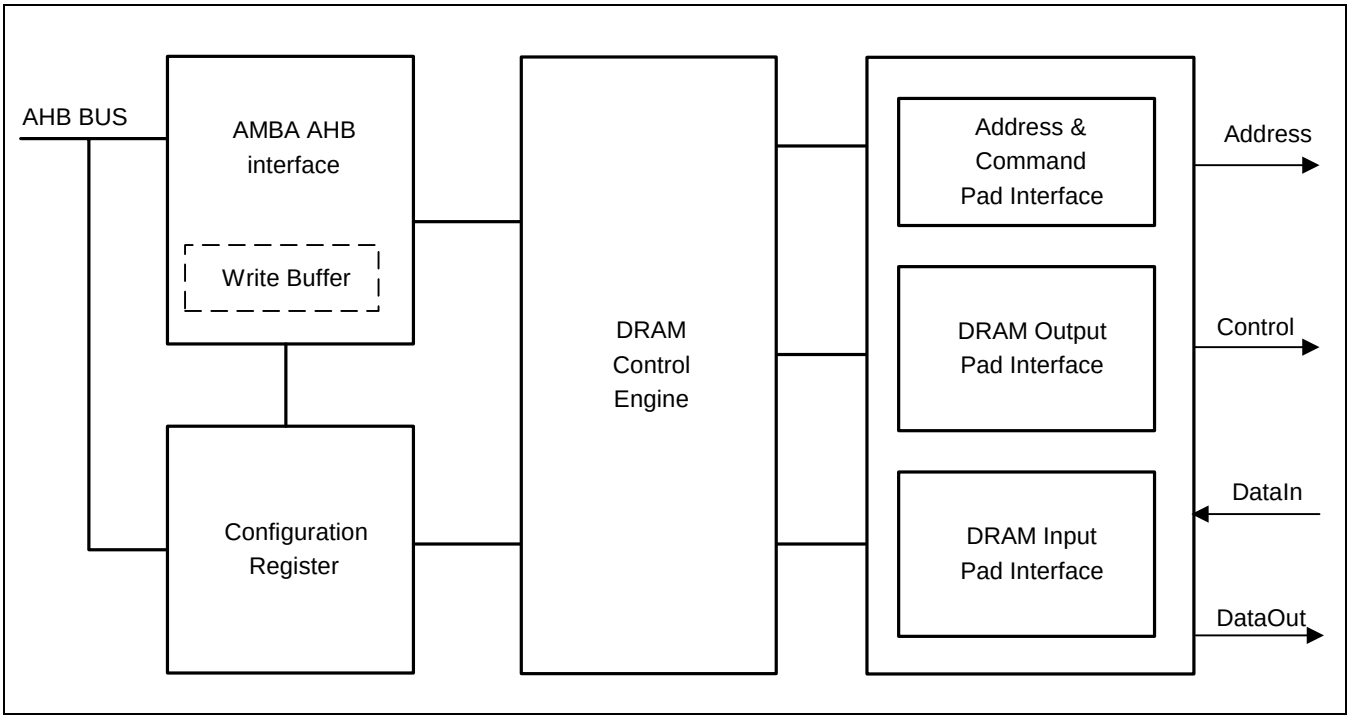


Figure 6-1. Mobile DRAM Controller Block Diagram

MOBILE DRAM INITIALIZATION SEQUENCE

On power-on reset, software must initialize the memory controller and the mobile DRAM connected to the controller. Refer to the mobile DRAM(SDRAM or DDR) data sheet for the start up procedure, and example sequences are given below:

MOBILE DRAM (SDRAM OR DDR) INITIALIZATION SEQUENCE

1. Wait 200us to allow DRAM power and clock stabilize.
2. Setting the Configuration Register0. This is for MRS and EMRS command to DRAM.
3. Program the Control Register1, and 3 to their normal operation values
4. Program the INIT[1:0] to '01b'. This automatically issues a PALL(pre-charge all) cammand to the DRAM.
5. Write '0xff' into the refresh timer register. This provides a refresh cycle every 255-clock cycles.
6. Wait minimum 2 auto-refresh cycle; DRAM requires minimun 2 auto-refresh cycle.
7. Program the INIT[1:0] of Control Register1 to '10b'. This automatically issues a MRS command to the DRAM
8. Program the normal operational value(auto-refresh ducy cycle) into the refresh timer.
9. Program the INIT[1:0] of Control Register1 to '11b'. This automatically issues a EMRS command to the Mobile DRAM, It's only needed for Mobile DRAM.
10. Program the INIT[1:0] to '00b'. The controller enters the normal mode.
11. The external DRAM is now ready for normal operation.

(Mobile) SDRAM Memory Interface Examples

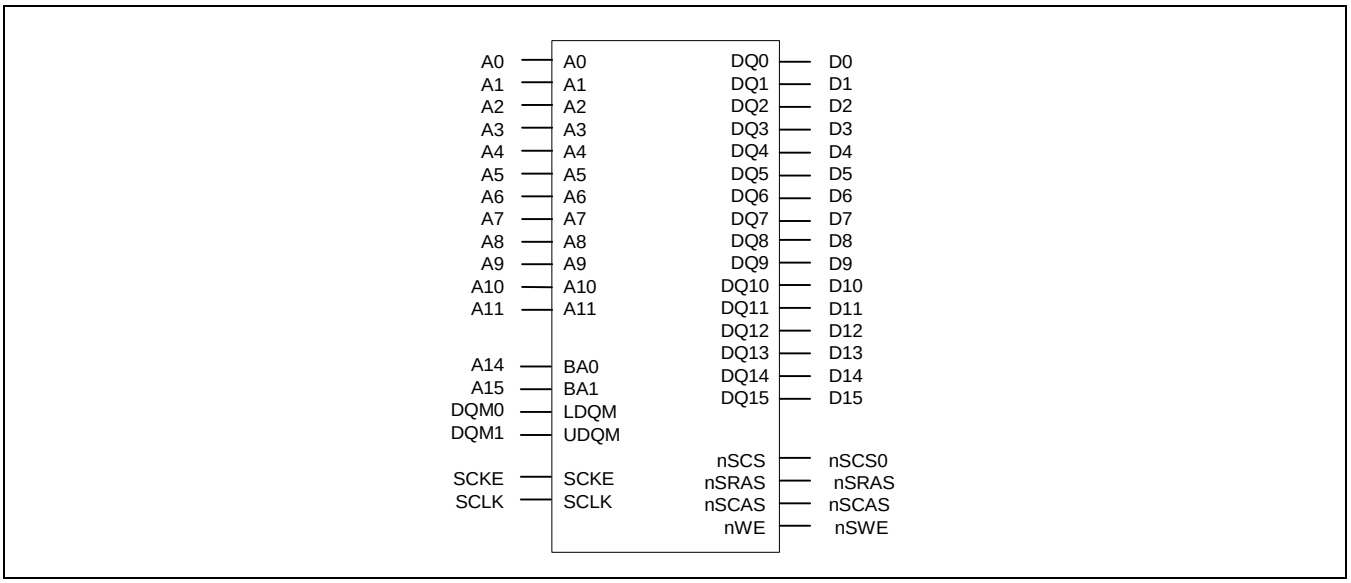


Figure 6-2. Memory Interface with 16-bit SDRAM (4Mx16, 4banks)

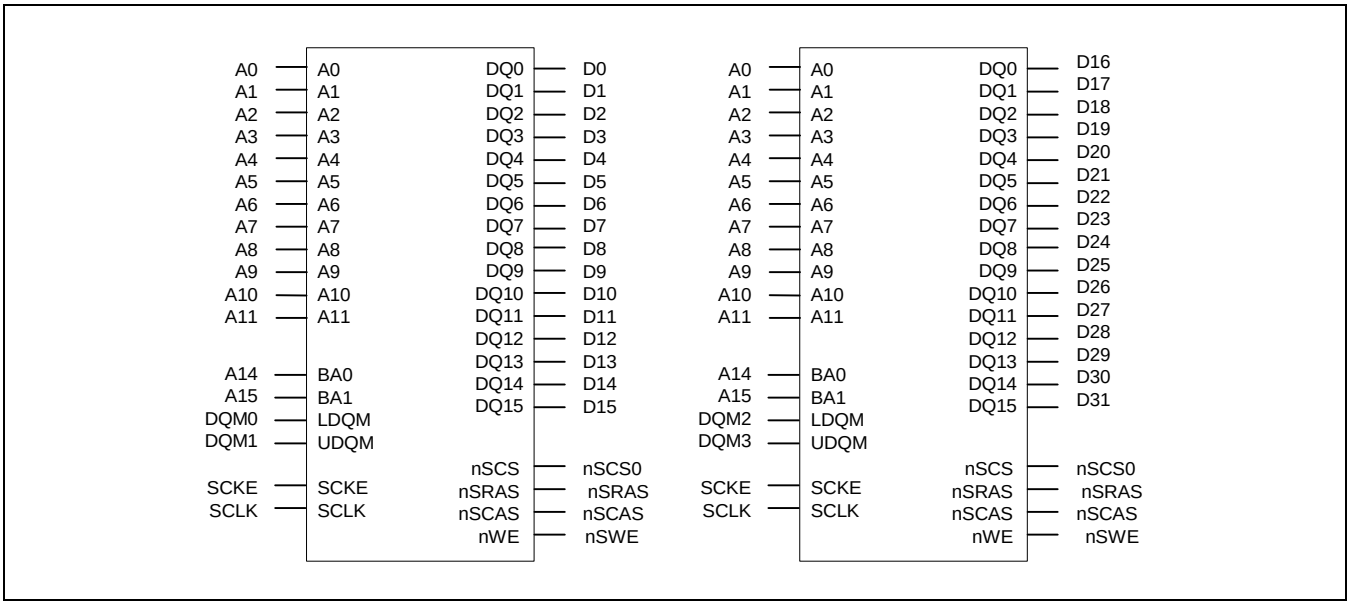


Figure 6-3. Memory Interface with 32-bit SDRAM (4Mx16 * 2ea, 4banks)

Mobile DDR Memory Interface Examples

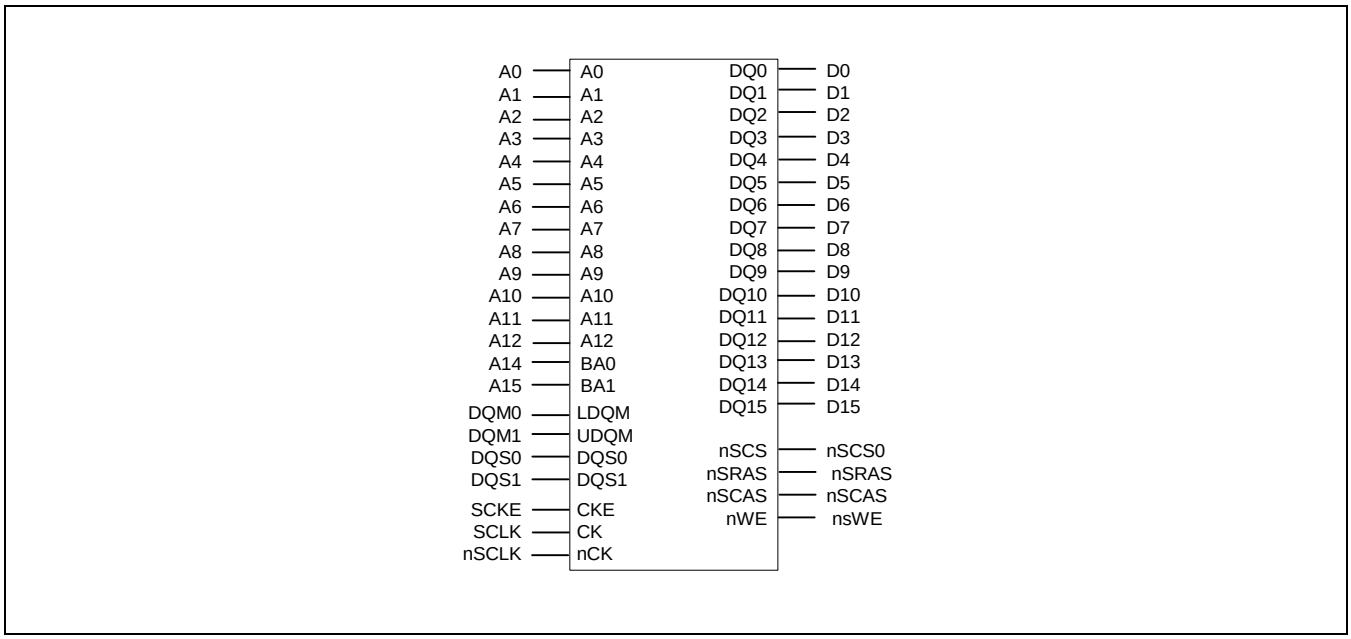


Figure 6-4. Memory Interface with 16-bit Mobile DDR

MOBLE DRAM CONFIGURATION REGISTER

Register	Address	R/W	Description	Reset Value
BANKCFG	0x48000000	R/W	Mobile DRAM configuration register	0x0000_000C

BANKCFG	Bit	Description	Initial State
Reserved	[31:19]	Should be '0'	0x0000
RASBW0	[18:17]	The bit width of RAS (row) address of bank 0 00 = 11-bit 01 = 12-bit 10 = 13-bit 11 = 14-bit	00b
Reserved	[16]	Should be '0'	0b
RASBW1	[15:14]	The bit width of RAS (row) address of bank 1 00 = 11-bit 01 = 12-bit 10 = 13-bit 11 = 14-bit	00b
Reserved	[13]	Should be '0'	0b
CASBW0	[12:11]	The bit width of CAS (column) address of bank 0 00 = 8-bit 01 = 9-bit 10 = 10-bit 11 = 11-bit	00b
Reserved	[10]	Should be '0'	0b
CASBW1	[9:8]	The bit width of CAS (column) address of bank 1 00 = 8-bit 01 = 9-bit 10 = 10-bit 11 = 11-bit	00b
ADDRCFG0	[7:6]	Memory address configuration of 00 = {BA, RAS, CAS} 01 = {RAS, BA, CAS}	0b
ADDRCFG1	[5:4]	Memory address configuration 00 = {BA, RAS, CAS} 01 = {RAS, BA, CAS}	0b
MEMCFG	[3:2]	External memory configuration 00 = SDR 01 = MSDR 1x = DDR	11b
Reserved	[1]	Should be '0'	0b
BW	[0]	Determine external memory data bus width 0 = 32-bit 1 = 16-bit Note : DDR/Mobile DDR interface is supported 16-bit only	0b

NOTE: BANKCFG register should not be written when the DRAM controller is busy. The controller status bit, BUSY in BANKCON register, can be used to check if the controller is idle.

MOBILE DRAM CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
BANKCON1	0x48000004	R/W	Mobile DRAM control register	0x4400_0040

BANKCON	Bit	Description	Initial State
BUSY	[31]	DRAM controller status bit (read only) 0 = IDLE 1 = BUSY	0b
DQSInDLL*	[30:28]	DQSIn Delay selection Should be set “100b”	100b
Reserved	[27:26]	Should be ‘1’	01b
Reserved	[25:8]	Should be ‘0’	0
BurstStop	[7]	Burst stop control (Only used in DDR interface) 0 = Disable 1 = Enable	0
WBUF	[6]	Write buffer control 0 = Disable 1 = Enable Note: Disabling the write buffer will flush any stored values to the external DRAM memory. Recommend value is ‘1’	1
AP	[5]	Auto pre-charge control 0 = Enable auto pre-charge 1 = Disable auto pre-charge Note: If PWRDN is enabled, then AP=0 provides active power down and AP=1 provides pre-charge power down.	0b
PWRDN	[4]	0 : not support sdram power down control 1 : support sdram power down control	0b
Reserved	[3:2]	Should be ‘0’	00b
INIT	[1:0]	DRAM initialization control 00 = Normal operation 01 = Issue PALL command 10 = Issue MRS command 11 = Issue EMRS command	00b

Note: There are difference between the reset value and the recommended value. Please keep in mind to adopt the recommended value for this field.

MOBILE DRAM TIMMING CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
BANKCON2	0x48000008	R/W	Mobile DRAM timing control register	0x0099_003F

BANKCON	Bit	Description	Initial State
Reserved	[31:24]	Should be '0'	0x00
tRAS	[23:20]	Row active time 0000 = 1-clock 0001 = 2-clock 0010 = 3-clock 0011 = 4-clock 0100 = 5-clock 0101 = 6-clock 0110 = 7-clock 0111 = 8-clock 1000 = 9-clock 1001 = 10-clock 1010 = 11-clock 1011 = 12-clock 1100 = 13-clock 1101 = 14-clock 1110 = 15-clock 1111 = 16-clock	1001b
tRC	[19:16]	Row cycle time 0000 = 1-clock 0001 = 2-clock 0010 = 3-clock 0011 = 4-clock 0100 = 5-clock 0101 = 6-clock 0110 = 7-clock 0111 = 8-clock 1000 = 9-clock 1001 = 10-clock 1010 = 11-clock 1011 = 12-clock 1100 = 13-clock 1101 = 14-clock 1110 = 15-clock 1111 = 16-clock	1001b
Reserved	[15:4]	Should be '0'	0x000
CAS Latency	[5:4]	CAS Latency Control 00 = Reserved 01 = 1-clock 10 = 2-clock 11 = 3-clock	011b
tRCD	[3:2]	RAS to CAS delay 00 = 1-clock 01 = 2-clock 10 = 3-clock 11 = 4-clock	11b
tRP	[1:0]	Row pre-charge time 00 = 1-clock 01 = 2-clock 10 = 3-clock 11 = 4-clock	11b

MOBILE DRAM (EXTENDED) MODE REGITER SET REGISTER

Register	Address	R/W	Description	Reset Value
BANKCON3	0x4800000C	R/W	Mobile DRAM (E)MRS Register	0x8000_0033

PnBANKCON	Bit	Description	Initial State
BA	[31:30]	Bank address for EMRS	10b
Reserved	[29:23]	Should be '0'	0x0000
DS	[22:21]	DS(Driver Strength) for EMRS	00b
Reserved	[20:19]	Should be '0'	00b
PASR	[18:16]	PASR(Partial Array Self Refresh) for EMRS	00b
BA	[15:14]	Bank address for MRS	
Reserved	[15:7]	Should be '0'	000000000b
CAS Latency	[6:4]	CAS Latency for MRS 00 = Reserved 01 = 1-clock 10 = 2-clock 11 = 3-clock	011b
Burst Type	[3]	DRAM Burst Type (Read Only) Only support sequential burst type.	0b
Burst Length	[2:0]	DRAM Burst Length (Read Only) This value is determined internally.	011b

NOTE: Bit[15:0] is used for MRS command cycle, and Bit[31:16] is for EMRS command cycle. You can program this register as memory type you are using. Each 16-bit exactly map the (E)MRS register bit location. Refer to memory data sheet.

MOBILE DRAM REFRESH CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
REFRESH	0x48000010	R/W	Mobile DRAM refresh control register	0x0000_0020

REFRESH	Bit	Description	Initial State
Reserved	[31:16]	Should be '0'	0x0000
REFCYC	[15:0]	DRAM refresh cycle. **Example:** Refresh period is 15.6us, and HCLK is 66MHz. The value of REFCYC is as follows: $REFCYC = 15.6 \times 10^{-6} \times 66 \times 10^{6} = 1029$	0x0020

MOBILE DRAM WRITE BUFFER TIME OUT REGISTER

A write to a enabling write buffer loads the value in the timeout register into timeout down counter of the buffer. When the timeout counter reached 0 the contents of write buffer is flushed to the external DRAM. The down counter is clocked HCLK. Writing a value of 0 in the TIMEOUT register disables the write buffer timeout function.

Register	Address	R/W	Description	Reset Value
TIMEOUT	0x480000014	R/W	Write Buffer Time out control register	0x0000_0000

TIMEOUT	Bit	Description	Initial State
Reserved	[31:16]	Should be '0'	0x0000
TIMEOUT	[15:0]	Write buffer time-out delay time	0x0000

7 NAND FLASH CONTROLLER

OVERVIEW

In recent times, NOR flash memory gets high in price while an SDRAM and a NAND flash memory get moderate, motivating some users to execute the boot code on a NAND flash and execute the main code on an SDRAM.

S3C2443X boot code can be executed on an external NAND flash memory. In order to support NAND flash boot loader, the S3C2443X is equipped with an internal SRAM buffer called 'Steppingstone'. When booting, the first 4 KBytes of the NAND flash memory will be loaded into Steppingstone and the boot code loaded into Steppingstone will be executed.

Generally, the boot code will copy NAND flash content to SDRAM. Using hardware ECC, the NAND flash data validity will be checked. Upon the completion of the copy, the main program will be executed on the SDRAM.

FEATURES

1. Auto boot: The boot code is transferred into 4-kbytes Steppingstone during reset. After the transfer, the boot code will be executed on the Steppingstone.
2. NAND Flash memory I/F: Support 256Words, 512Bytes, 1KWords and 2KBytes Page.
3. Software mode: User can directly access NAND flash memory, *for example this feature can be used in read/erase/program NAND flash memory*.
4. Interface: 8 / 16-bit NAND flash memory interface bus.(Only 8-bit nand booting)
5. Hardware ECC generation, detection and indication (Software correction).
6. Support both SLC and MLC NAND flash memory : 1-bit ECC for SLC and 4-bit ECC for MLC NAND flash.
7. SFR I/F: Support Little Endian Mode, Byte/half word/word access to Data and ECC Data register, and Word access to other registers
8. SteppingStone I/F: Support Little/Big Endian, Byte/half word/word access.
9. The Steppingstone 4-KB internal SRAM buffer can be used for another purpose after NAND flash booting.

BLOCK DIAGRAM

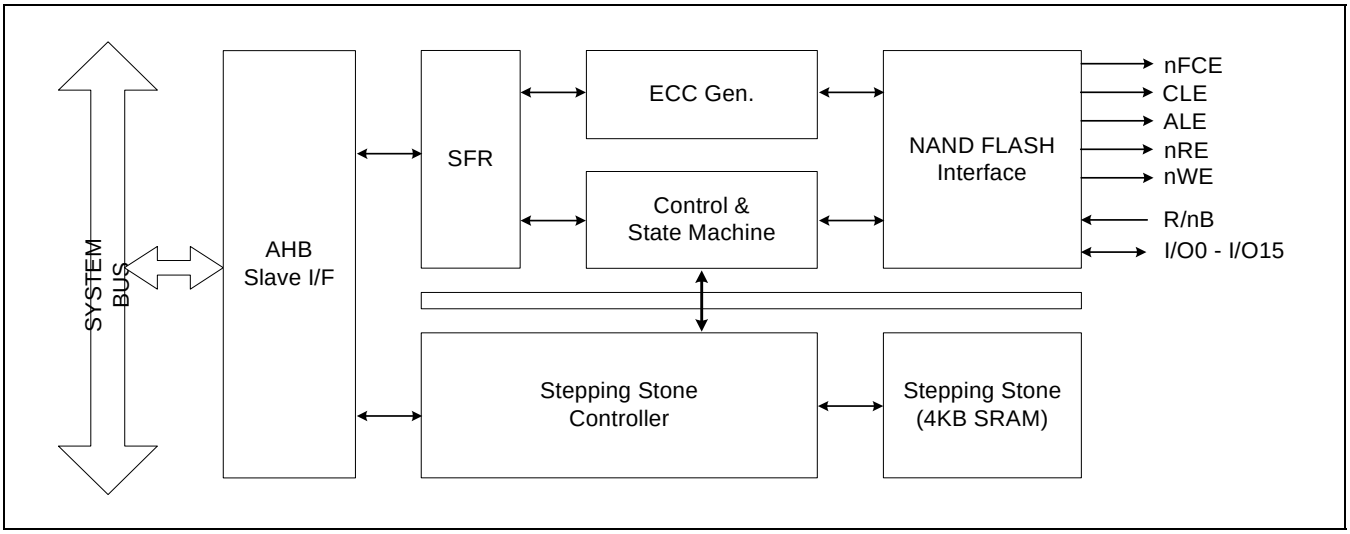


Figure 7-1. NAND Flash Controller Block Diagram

BOOT LOADER FUNCTION

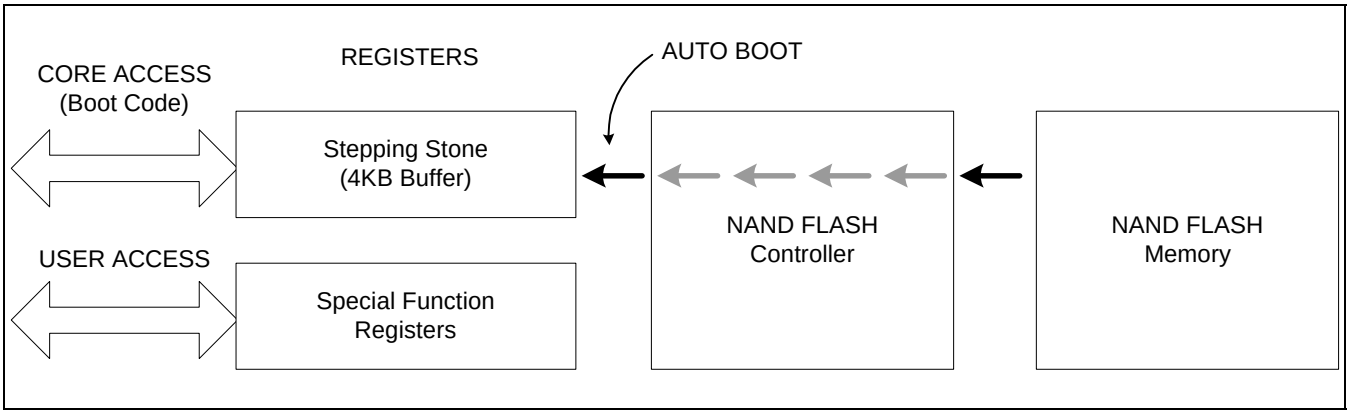


Figure 7-2. NAND Flash Controller Boot Loader Block Diagram

During reset, Nand flash controller will get information about connected NAND flash through Pin status of POM – refer to **PIN CONFIGURATION**), After power-on or system reset is occurred, the NAND Flash controller load automatically the 4-KBytes boot loader codes. After loading the boot loader codes, the boot loader code in steppingstone is executed.

NOTE:

During the auto boot, the ECC is not checked. So, the first 4-KB of NAND flash should have no bit error.

PIN CONFIGURATION TABLE

OM[4]	OM[3]	OM[2]	OM[1]	OM[0]	OM[4]	OM[3]	OM[2]	OM[1]	OM[0]	Operation Mode
0	0	0	0	0	NAND	Advanced	-	addr(4)	OSC	NAND
				1					EXT	
			1	0				addr(5)	OSC	
				1					EXT	
		1	0	0			page(2K)	addr(4)	OSC	
				1					EXT	
			1	0				addr(5)	OSC	
				1					EXT	
	1	0	0	0		Normal	-	addr(3)	OSC	
				1					EXT	
			1	0				addr(4)	OSC	
				1					EXT	
		1	0	0			page(512)	addr(3)	OSC	
				1					EXT	
			1	0				addr(4)	OSC	
				1					EXT	

NAND FLASH MEMORY TIMING

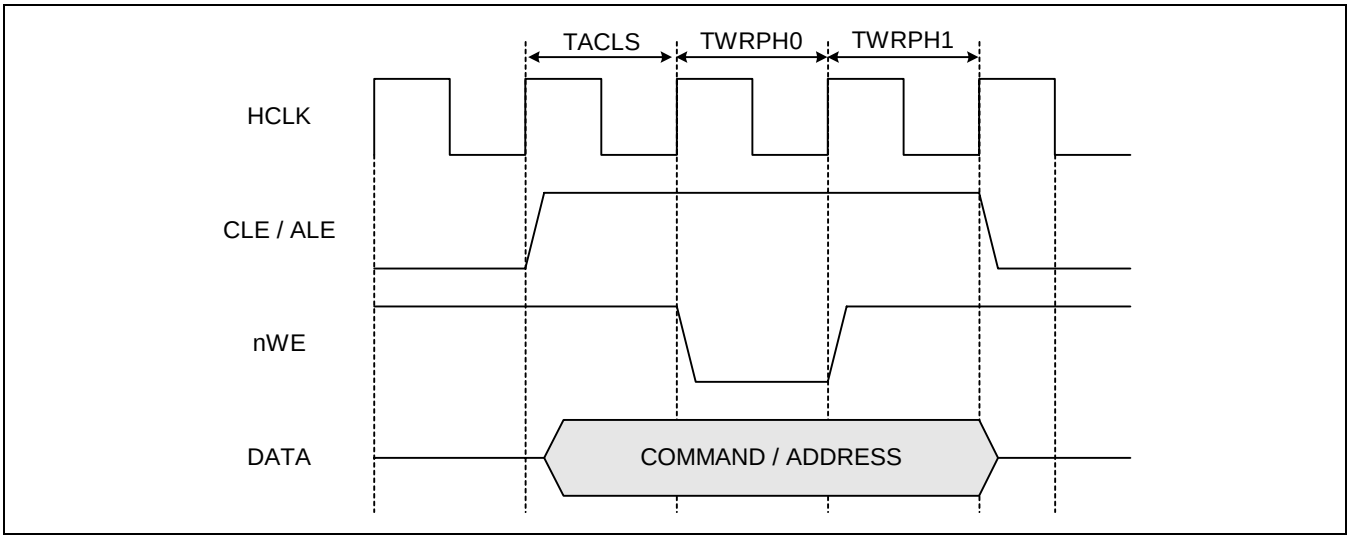


Figure 7-3. CLE & ALE Timing (TACLS=1, TWRPH0=0, TWRPH1=0)

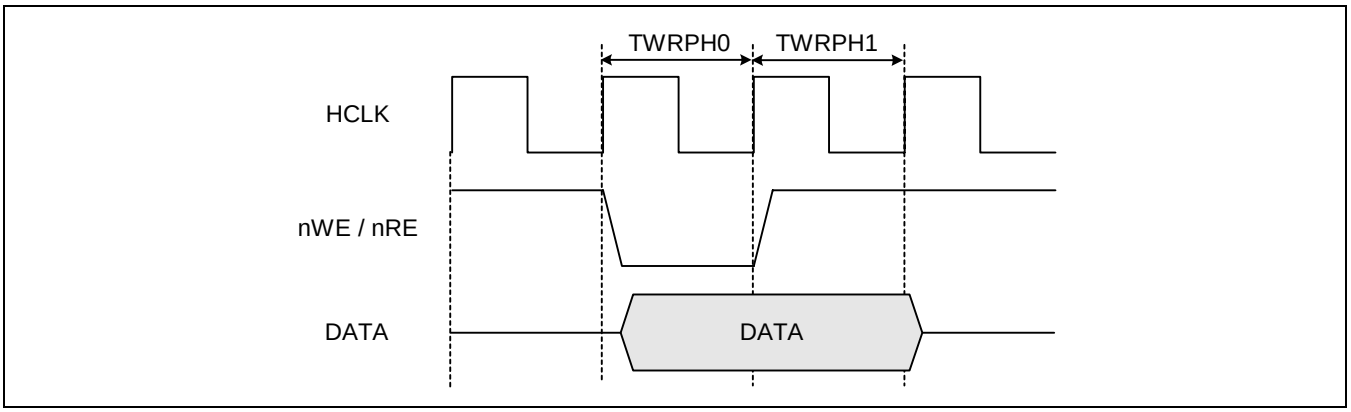


Figure 7-4. nWE & nRE Timing (TWRPH0=0, TWRPH1=0)

SOFTWARE MODE

S3C2443X only supports software mode access. Using this mode, you can completely access the NAND flash memory. The NAND Flash Controller supports direct access interface with the NAND flash memory.

1. Writing to the command register = the NAND Flash Memory command cycle
2. Writing to the address register = the NAND Flash Memory address cycle
3. Writing to the data register = write data to the NAND Flash Memory (write cycle)
4. Reading from the data register = read data from the NAND Flash Memory (read cycle)
5. Reading main ECC registers and Spare ECC registers = read data from the NAND Flash Memory

NOTE:

In the software mode, you have to check the RnB status input pin by using polling or interrupt.

Data Register Configuration

1) 16-bit NAND Flash Memory Interface

A. Word Access

Register	Endian	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFDATA	Little	2nd I/O[15:8]	2nd I/O[7:0]	1st I/O[15:8]	1st I/O[7:0]
NFDATA	Big	1st I/O[15:8]	1st I/O[7:0]	2nd I/O[15:8]	2nd I/O[7:0]

B. Half-word Access

Register	Endian	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFDATA	Little/Big	Invalid value	Invalid value	1st I/O[15:8]	1st I/O[7:0]

2) 8-bit NAND Flash Memory Interface

A. Word Access

Register	Endian	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFDATA	Little	4th I/O[7:0]	3rd I/O[7:0]	2nd I/O[7:0]	1st I/O[7:0]
NFDATA	Big	1st I/O[7:0]	2nd I/O[7:0]	3rd I/O[7:0]	4th I/O[7:0]

B. Half-word Access

Register	Endian	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFDATA	Little	Invalid value	Invalid value	2nd I/O[7:0]	1st I/O[7:0]
NFDATA	Big	Invalid value	Invalid value	1st I/O[7:0]	2nd I/O[7:0]

C. Byte Access

Register	Endian	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFDATA	Little/Big	Invalid value	Invalid value	Invalid value	1st I/O[7:0]

STEPPINGSTONE (4K-Byte SRAM)

The NAND Flash controller uses Steppingstone as the buffer on booting and also you can use this area for another purpose.

SLC / MLC ECC (Error Correction Code)

NAND flash controller has four ECC (Error Correction Code) modules for SLC NAND flash memory. And has one ECC module for MLC NAND flash memory.

For SLC NAND flash memory interface, NAND flash controller has 4 ECC modules. The two SLC ECC modules (one for data [7:0] and the other for data [15:8]) can be used for (up to) 2048 bytes ECC parity code generation, and the others (one for data[7:0] and the other for data[15:8]) can be used for (up to) 3 bytes ECC Parity code generation.

For MLC NAND flash memory interface, NAND flash controller has one ECC module. This can be used only 512 bytes ECC parity code generation. For 8-bit memory interface, MLC ECC module generate parity code for each 512 byte. And for 16-bit memory interface, MLC ECC module generate parity code for each 256 words(512 bytes). But SLC ECC modules generate parity code per byte lane separately.

Following ECC parity code and two tables are SLC ECC.

28-bit ECC Parity Code = 22-bit Line parity + 6-bit Column Parity

14-bit ECC Parity Code = 2 -bit Line parity + 6-bit Column Parity

2048 BYTE SLC ECC PARITY CODE ASSIGNMENT TABLE

	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
MECCn_0	~P64	~P64’	~P32	~P32’	~P16	~P16’	~P8	~P8’
MECCn_1	~P1024	~P1024’	~P512	~P512’	~P256	~P256’	~P128	~P128’
MECCn_2	~P4	~P4’	~P2	~P2’	~P1	~P1’	~P2048	~P2048’
MECCn_3	1	1	1	1	~P8192	~P8192’	~P4096	~P4096’

16 BYTE ECC SLC PARITY CODE ASSIGNMENT TABLE

	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
SECCn_0	~P2	~P2’	~P1	~P1’	~P16	~P16’	~P8	~P8’
SECCn_1	1	1	1	1	1	1	~P4	~P4’

ECC MODULE FEATURES

ECC generation is controlled by the ECC Lock (MainECCLock, SpareECCLock) bit of the Control register. When ECCLock is Low, ECC codes are generated by the H/W ECC modules.

SLC ECC Register Configuration (Little / Big Endian)

Following tables shows the configuration of SLC ECC value read from spare area of external NAND flash memory. For comparing to ECC parity code generated by the H/W modules, the format of ECC read from memory is important.

Note: MLC ECC decoding scheme is different to SLC ECC.

1) 16-bit NAND Flash Memory Interface

Register	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFMECCD0	2nd ECC for I/O[15:8]	2nd ECC for I/O[7:0]	1st ECC for I/O[15:8]	1st ECC for I/O[7:0]
NFMECCD1	4th ECC for I/O[15:8]	4th ECC for I/O[7:0]	3rd ECC for I/O[15:8]	3rd ECC for I/O[7:0]

Register	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFSECCD	2nd ECC for I/O[15:8]	2nd ECC for I/O[7:0]	1st ECC for I/O[15:8]	1st ECC for I/O[7:0]

2) 8-bit NAND Flash Memory Interface

Register	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFMECCD0	4th ECC for I/O[7:0]	3rd ECC for I/O[7:0]	2nd ECC for I/O[7:0]	1st ECC for I/O[7:0]
NFMECCD1	Not used			

Register	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFSECCD	Not used		2nd ECC for I/O[7:0]	1st ECC for I/O[7:0]

SLC ECC PROGRAMMING GUIDE

1. To use SLC ECC in software mode, reset the ECCType to '0'(enable SLC ECC)'. ECC module generates ECC parity code for all read / write data when MainECCLock (NFCON[7]) and SpareECCLock (NFCON[6]) are unlocked('0'). So you have to reset ECC value by writing the InitMECC (NFCONT[5]) and InitSECC (NFCON[4]) bit as '1' and have to clear the MainECCLock (NFCONT[7]) bit to '0'(Unlock) before read or write data.
   MainECCLock (NFCONT[7]) and SpareECCLock(NFCONT[6]) bit controls whether ECC Parity code is generated or not.
2. Whenever data is read or written, the ECC module generates ECC parity code on register NFMECC0/1.
3. After you complete read or write one page (not include spare area data), Set the MainECCLock bit to '1'(Lock). ECC Parity code is locked and the value of the ECC status register will not be changed.
4. To generate spare area ECC parity code, Clear as '0'(Unlock) SpareECCLock(NFCONT[6]) bit.
5. Whenever data is read or written, the spare area ECC module generates ECC parity code on register NFSECC.
6. After you complete read or write spare area, set the SpareECCLock bit to '1'(Lock). ECC Parity code is locked and the value of the ECC status register will not be changed.
7. From now, you can use these values to record to the spare area or check the bit error.
8. For example, to check the bit error of main data area on page read operation, after generating of ECC codes for main data area, you have to move the ECC parity codes (is stored to spare area) to NFMECCD0 and NFMECCD1. From this time, the NFECCERR0 and NFECCERR1 have the valid error status values.

NOTE:

NFSECCD is for ECC in the spare area (Usually, the user will write the ECC value generated from main data area to Spare area, which value will be the same as NFMECC0/1) and which is generated from the main data area.

MLC ECC PROGRAMMING GUIDE (ENCODING)

1. To use MLC ECC in software mode, set the ECCType to '1'(enable MLC ECC). ECC module generates ECC parity code for all write data. So you have to reset ECC value by writing the InitMECC (NFCONT[5]) and InitSECC (NFCON[4]) bit as '1' and have to clear the MainECCLock (NFCONT[7]) bit to '0'(Unlock) before write data.
   MainECCLock (NFCONT[7]) and SpareECCLock(NFCONT[6]) bit controls whether ECC Parity code is generated or not.
2. Whenever data is written, the MLC ECC module generates ECC parity code internally.
3. After you complete write 512-byte or 256-words (16-bit I/O) (not include spare area data), Set the MainECCLock bit to '1'(Lock). ECC Parity code generation is locked and the values are updated to NFMECC0, NFMECC1 register when NFSTAT[7] (ECCEncDone) is set('1'). If you use 512-byte or 256-word (16-bit I/O) NAND flash memory, you can program these values to spare area. But if you use NAND flash memory more than 512-byte or 256-word (16-bit I/O) page, you can't program right now. In this case, you have to copy these parity codes to other memory like DRAM. After writing all main data, you can write the copied ECC values to spare area.
4. To generate spare area ECC parity code, Clear as '0'(Unlock) SpareECCLock(NFCONT[6]) bit.
5. Whenever data is written, the spare area ECC module generates ECC parity code on register NFSECC.
6. After you complete write spare area, set the SpareECCLock bit to '1'(Lock). ECC Parity code is locked and the value of the ECC status register will not be changed.
7. From now, you can use these values to record to the spare area.

MLC ECC PROGRAMMING GUIDE (DECODING)

1. To use MLC ECC in software mode, set the ECCType to '1'(enable MLC ECC). ECC module generates ECC parity code for all read data. So you have to reset ECC value by writing the InitMECC (NFCONT[5]) and InitSECC (NFCON[4]) bit as '1' and have to clear the MainECCLock (NFCONT[7]) bit to '0'(Unlock) before read data.
   MainECCLock (NFCONT[7]) and SpareECCLock(NFCONT[6]) bit controls whether ECC Parity code is generated or not.
2. Whenever data is read, the MLC ECC module generates ECC parity code internally.
3. After you complete read 512-byte or 256-words (16-bit I/O) (not include spare area data), Set the MainECCLock bit to '1'(Lock). ECC Parity code generation is locked. MLC ECC module needs parity codes to detect whether error bits are or not. So you have to read ECC parity code right after read 512-byte or 256-word (in 16-bit I/O). Once ECC parity code is read, MLC ECC engine start to search any error internally. MLC ECC error searching engine need minimum 155 cycles to find any error. During this time, you can continue read main data from external NAND flash memory. NFSTAT[6] can be used to check whether ECC decoding is completed or not.
4. When ECCDecDone (NFSTAT[7]) is set ('1'), NFESTAT0 indicates whether error bit exist or not. If any error exist, you can fix it by referencing NFSTAT0/1 and NFMLCBITPT register.
5. If you have more main data to read, continue to step 10).
6. MLC ECC parity code scheme is used only for main data area to find up to 4-bit error.
7. Whenever data is read, the spare area ECC module generates ECC parity code on register NFSECC.
8. After you complete read spare area, set the SpareECCLock bit to '1'(Lock). ECC Parity code is locked and the value of the ECC status register will not be changed.
9. From now, you can use these values to check the bit error.

NAND FLASH MEMORY MAPPING

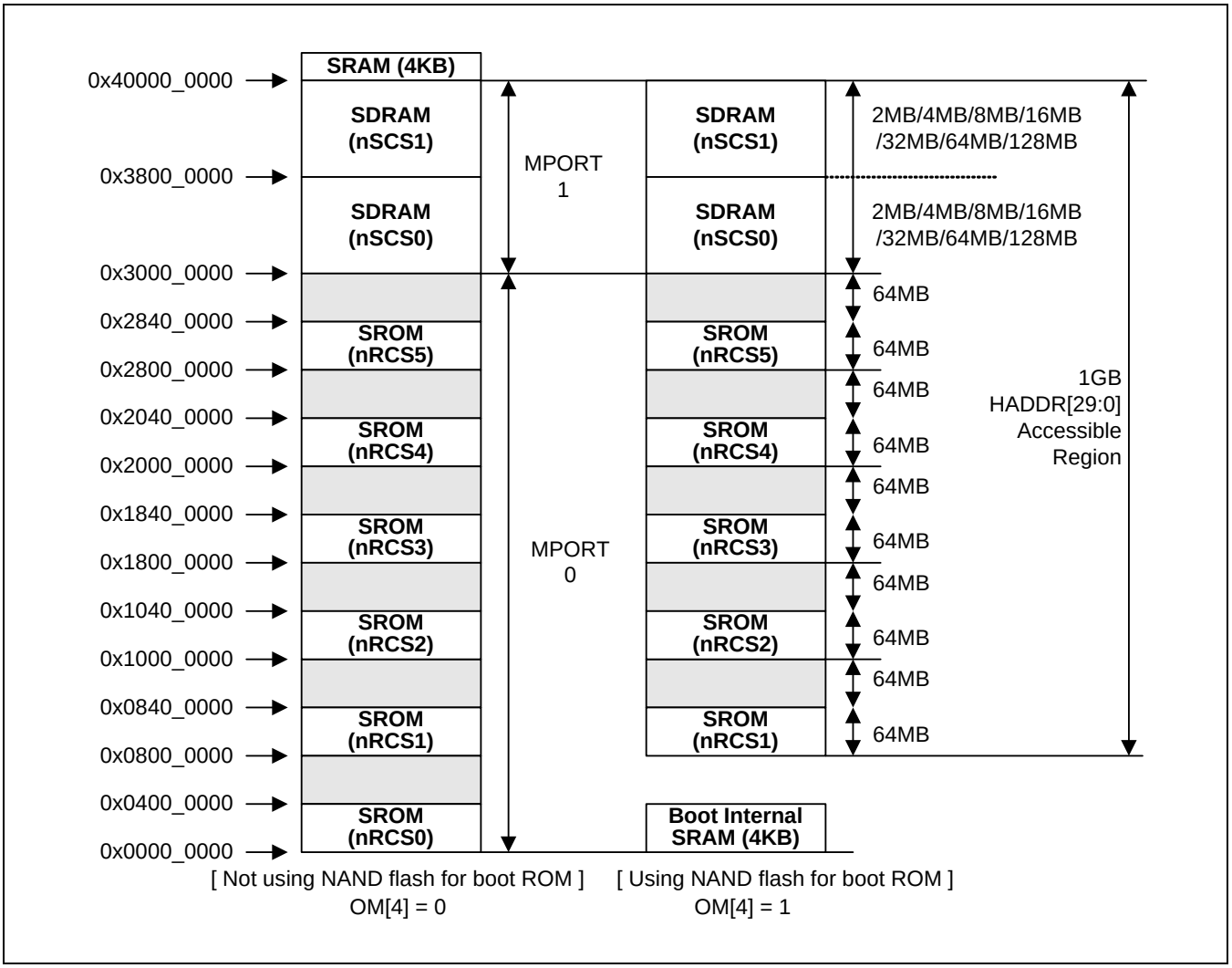


Figure 7-5. NAND Flash Memory Mapping

NOTE:

SROM means ROM or SRAM type memory

NAND FLASH MEMORY CONFIGURATION

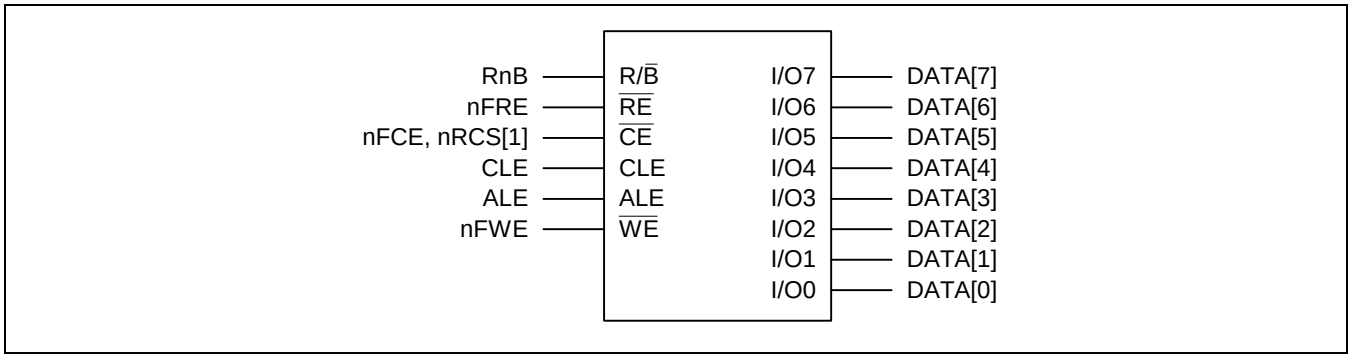


Figure 7-6. A 8-bit NAND Flash Memory Interface

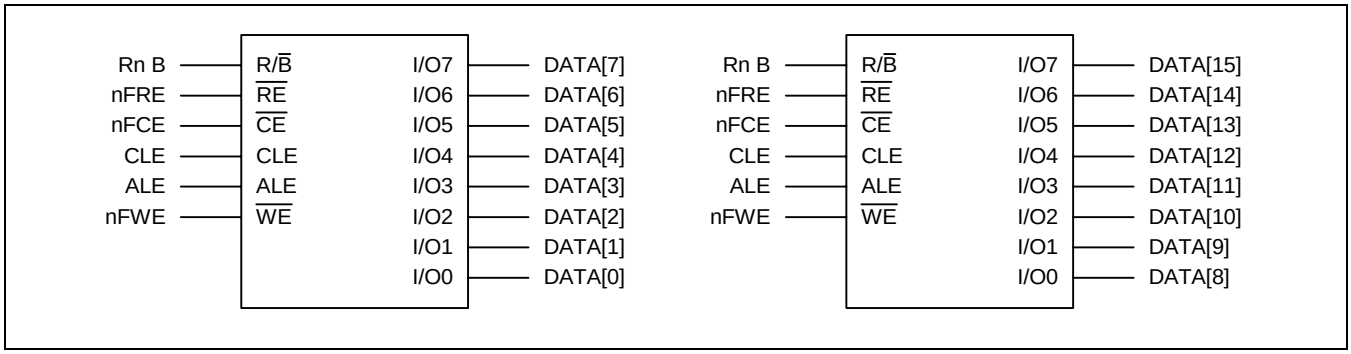


Figure 7-7. Two 8-bit NAND Flash Memory Interface

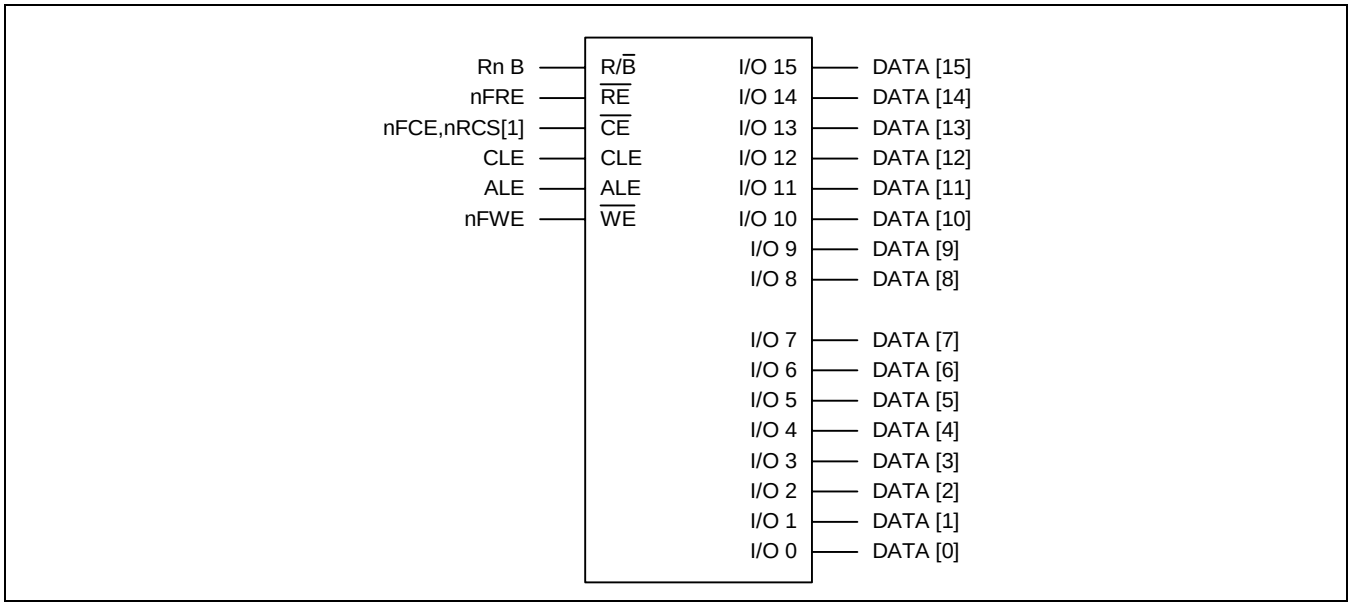


Figure 7-8. A 16-bit NAND Flash Memory Interface

NOTE:

NAND CONTROLLER can support to control two nand flash memories.

	NAND BOOT	ROM BOOT
Reg_nCE0	nFCE	nFCE
Reg_nCE1	nRCS[1]	nRCS[1]

If you want NAND BOOT, nFCE should be used for boot. Optionally you can use nRCS[1] for storage.

Or if you want ROM BOOT, Both nFCE and nRCS[1] can be used for storage optionally.

NAND FLASH CONTROLLER SPECIAL REGISTERS

NAND FLASH CONTROLLER REGISTER MAP

Address	R/W	Reset value	Name	Description
Base + 0x00	R/W		NFCONF	Configuration register
Base + 0x04	R/W		NFCONT	Control register
Base + 0x08	R/W		NFCMMD	Command register
Base + 0x0c	R/W		NFADDR	Address register
Base + 0x10	R/W		NFDATA	Data register
Base + 0x14	R/W		NFMECCD0	1st and 2nd main ECC data register
Base + 0x18	R/W		NFMECCD1	3rd and 4th main ECC data register
Base + 0x1c	R/W		NFSECCD	Spare ECC read register
Base + 0x20	R/W		NFSBLK	Programmable start block address register
Base + 0x24	R/W		NFEBLK	Programmable end block address register
Base + 0x28	R/W		NFSTAT	NAND status registet
Base + 0x2C	R		NFECCERR0	ECC error status0 register
Base + 0x30	R		NFECCERR1	ECC error status1 register
Base + 0x34	R		NFMECC0	Generated ECC status0 register
Base + 0x38	R		NFMECC1	Generated ECC status1 register
Base + 0x3C	R		NFSECC	Generated Spare area ECC status register
Base + 0x40	R		NFMLCBITPT	4-bit ECC error bit pattern register
* Base = 0x4E00_0000				

NAND FLASH CONFIGURATION REGISTER

Register	Address	R/W	Description	Reset Value
NFCONF	0x4E000000	R/W	NAND Flash Configuration register	0x0000100X

NFCONF	Bit	Description	Initial State
NANDBoot	[31]	Shows whether NAND boot or not 1=NAND Flash memory boot	000000
Reserved	[30:25]	Reserved	0000000
ECCType	[24]	ECC type selection 0: SLC (1-bit correction) ECC 1:MLC (4-bit correction) ECC	0
Reserved	[15]	Reserved	0
TACLS	[14:12]	CLE & ALE duration setting value (0~7) Duration = HCLK x TACLS	001
Reserved	[11]	Reserved	0
TWRPH0	[10:8]	TWRPH0 duration setting value (0~7) Duration = HCLK x (TWRPH0 + 1)	000
Reserved	[7]	Reserved	0
TWRPH1	[6:4]	TWRPH1 duration setting value (0~7) Duration = HCLK x (TWRPH1 + 1)	000
AdvFlash (Read only)	[3]	Advance NAND flash memory for auto-booting 0: Support 256 or 512 byte/page NAND flash memory 1: Support 1024 or 2048 byte/page NAND flash memory This bit is determined by NCON0 pin status during reset and wake-up from sleep mode.	H/W Set
PageSize (R/W)	[2]	NAND flash memory page size for auto-booting AdvFlash PageSize When AdvFlash is 0, 0: 256 Bytes/page, 1: 512 Bytes/page When AdvFlash is 1, 0: 1024 Bytes/page, 1: 2048 Bytes/page This bit is determined by OM[3:0] pin status during reset and wake-up from sleep mode.	H/W Set
AddrCycle (Read only)	[1]	NAND flash memory Address cycle for auto-booting AdvFlash AddrCycle When AdvFlash is 0, 0: 3 address cycle 1: 4 address cycle When AdvFlash is 1, 0: 4 address cycle 1: 5 address cycle This bit is determined by OM[3:0] pin status during reset and wake-up from sleep mode.	H/W Set
BusWidth (R/W)	[0]	NAND Flash Memory I/O bus width for auto-booting and general access. 0: 8-bit bus 1: 16-bit bus S3C2443X support only 8-bit nand booting (Not support 16-bit) This bit can be changed by software.	H/W Set [0]

CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
NFCONT	0x4E000004	R/W	NAND Flash control register	0x0384

NFCONT	Bit	Description	Initial State
Reserved	[31:19]	Reserved	0
ECC Direction	[18]	4-bit ECC encoding / decoding control 0: Decoding 4-bit ECC, It is used for page read 1: Encoding 4-bit ECC, It is be used for page program	0
Lock-tight	[17]	Lock-tight configuration 0: Disable lock-tight 1: Enable lock-tight, Once this bit is set to 1, you cannot clear. Only reset or wake up from sleep mode can make this bit disable (can not cleared by software). When it is set to 1, the area setting in NFSBLK (0x4E000038) to NFEBLK (0x4E00003C)-1 is unlocked, and except this area, write or erase command will be invalid and only read command is valid. When you try to write or erase locked area, the illegal access will be occur (NFSTAT [3] bit will be set). If the NFSBLK and NFEBLK are same, entire area will be locked.	0
Soft Lock	[16]	Soft Lock configuration 0: Disable lock 1: Enable lock Soft lock area can be modified at any time by software. When it is set to 1, the area setting in NFSBLK (0x4E000038) to NFEBLK (0x4E00003C)-1 is unlocked, and except this area, write or erase command will be invalid and only read command is valid. When you try to write or erase locked area, the illegal access will be occur (NFSTAT [3] bit will be set). If the NFSBLK and NFEBLK are same, entire area will be locked.	1
EnbECC EncINT	[13]	4-bit ECC encoding completion interrupt control 0: Disable interrupt 1: Enable interrupt	0
EnbECC DecINT	[12]	4-bit ECC decoding completion interrupt control 0: Disable interrupt 1: Enable interrupt	0
Reserved	[11]	Reserved	0
EnbIllegal AccINT	[10]	Illegal access interrupt control 0: Disable interrupt 1: Enable interrupt Illegal access interrupt is occurs when CPU tries to program or erase locking area (the area setting in NFSBLK (0x4E000038) to NFEBLK (0x4E00003C)-1).	0

NFCONT	Bit	Description	Initial State
EnbRnBINT	[9]	RnB status input signal transition interrupt control 0: Disable RnB interrupt 1: Enable RnB interrupt	0
RnB_ TransMode	[8]	RnB transition detection configuration 0: Detect rising edge 1: Detect falling edge	0
MainECC Lock	[7]	Lock Main area ECC generation 0: Unlock Main area ECC 1: Lock Main area ECC Main area ECC status register is NFMECC0/1(0x4E00002C/30),	1
SpareECC Lock	[6]	Lock Spare area ECC generation. 0: Unlock Spare ECC 1: Lock Spare ECC Spare area ECC status register is NFSECC(0x4E000034),	1
InitMECC	[5]	1: Initialize main area ECC decoder/encoder (write-only)	
InitSECC	[4]	1: Initialize spare area ECC decoder/encoder (write-only)	0
Reserved	[3]	Reserved (HW_nCE)	0
Reg_nCE1	[2]	NAND Flash Memory nRCS[1] signal control	1
Reg_nCE0	[1]	NAND Flash Memory nFCE signal control 0: Force nFCE to low(Enable chip select) 1: Force nFCEto High(Disable chip select) Note: During boot time, it is controlled automatically. This value is only valid while MODE bit is 1	1
MODE	[0]	NAND Flash controller operating mode 0: NAND Flash Controller Disable (Don't work) 1: NAND Flash Controller Enable	0

COMMAND REGISTER

Register	Address	R/W	Description	Reset Value
NFCMMD	0x4E000008	R/W	NAND Flash command set register	0x00

NFCMMD	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0x00
NFCMMD	[7:0]	NAND Flash memory command value	0x00

ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
NFADDR	0x4E00000C	R/W	NAND Flash address set register	0x0000XX00

REG_ADDR	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0x00
NFADDR	[7:0]	NAND Flash memory address value	0x00

DATA REGISTER

Register	Address	R/W	Description	Reset Value
NFDATA	0x4E000010	R/W	NAND Flash data register	0xXXXX

NFDATA	Bit	Description	Initial State
NFDATA	[31:0]	NAND Flash read/program data value for I/O (Note) Refer to **DATA REGISTER CONFIGURATION** in p6-5.	0xXXXX

MAIN DATA AREA ECC REGISTER

Register	Address	R/W	Description	Reset Value
NFMECCD0	0x4E000014	R/W	NAND Flash ECC 1st and 2nd register for main data read (Note) Refer to **ECC MODULE FEATURES** in p7-8.	0x00000000
NFMECCD1	0x4E000018	R/W	NAND Flash ECC 3rd 4th register for main data read (Note) Refer to **ECC MODULE FEATURES** in p7-8.	0x00000000

When 16-bit NAND flash is used.

NFMECCD0	Bit	Description	Initial State
ECCData1_1	[31:24]	2nd ECC for I/O[15:8]	0x00
ECCData1_0	[23:16]	2nd ECC for I/O[7:0] Note : In Software mode, Read this register when you need to read 2nd ECC value from NAND flash memory	0x00
ECCData0_1	[15:8]	1st ECC for I/O[15:8]	0x00
ECCData0_0	[7:0]	1st ECC for I/O[7:0] Note : In Software mode, Read this register when you need to read 1st ECC value from NAND flash memory. This register has same read function of NFDATA.	0x00

NOTE: Only word access is valid.

NFMECCD1	Bit	Description	Initial State
ECCData3_1	[31:24]	4th ECC for I/O[15:8]	0x00
ECCData3_0	[23:16]	4th ECC for I/O[7:0] Note : In Software mode, Read this register when you need to read 4th ECC value from NAND flash memory	0x00
ECCData2_1	[15:8]	3rd ECC for I/O[15:8]	0x00
ECCData2_0	[7:0]	3rd ECC for I/O[7:0] Note: In Software mode, Read this register when you need to read 3rd ECC value from NAND flash memory. This register has same read function of NFDATA.	0x00

NOTE: Only word access is valid.

When 8-bit interface NAND flash is used.

NFMECCD0	Bit	Description	Initial State
Reserved	[31:24]	Not used	0x00
ECCData1	[23:16]	ECC1 for I/O[7:0]	0x00
Reserved	[15:8]	Not used	0x00
ECCData0	[7:0]	ECC0 for I/O[7:0]	0x00

NOTE: Only word access is valid.

NFMECCD1	Bit	Description	Initial State
Reserved	[31:0]	Not used	0x00
ECCData3	[23:16]	ECC3 for I/O[7:0]	0x00
Reserved	[31:0]	Not used	0x00
ECCData2	[7:0]	ECC2 for I/O[7:0]	0x00

NOTE: Only word access is valid.

SPARE AREA ECC REGISTER

Register	Address	R/W	Description	Reset Value
NFSECCD	0x4E00001C	R/W	NAND Flash ECC(Error Correction Code) register for spare area data read	0x00000000

When 16-bit NAND flash is used.

NFSECCD	Bit	Description	Initial State
ECCData1_1	[31:24]	2nd ECC for I/O[15:8]	0x00
ECCData1_0	[23:16]	2nd ECC for I/O[7:0] Note: In Software mode, Read this register when you need to read 2nd ECC value from NAND flash memory	0x00
ECCData0_1	[15:8]	1st ECC for I/O[15:8]	0x00
ECCData0_0	[7:0]	1st ECC for I/O[7:0] Note: In Software mode, Read this register when you need to read 1st ECC value from NAND flash memory. This register has same read function of NFDATA.	0x00

NOTE: Only word access is valid.

When 8-bit NAND flash is used.

NFSECCD	Bit	Description	Initial State
Reserved	[31:16]	Not used	0x00
SECCData1	[23:16]	2nd Spare area ECC for I/O[7:0]	0x00
Reserved	[15:8]	Not used	0x00
SECCData0	[7:0]	1st Spare area ECC for I/O[7:0]	0x00

NOTE: Only word or half word access is valid.

PROGRMMABLE BLOCK ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
NFSBLK	0x4E000020	R/W	NAND Flash programmable start block address	0x000000
NFEBLK	0x4E000024	R/W	NAND Flash programmable end block address Nand Flash can be programmed between start and end address. When the Soft lock or Lock-tight is enabled and the Start and End address has same value, Entire area of NAND flash will be locked.	0x000000

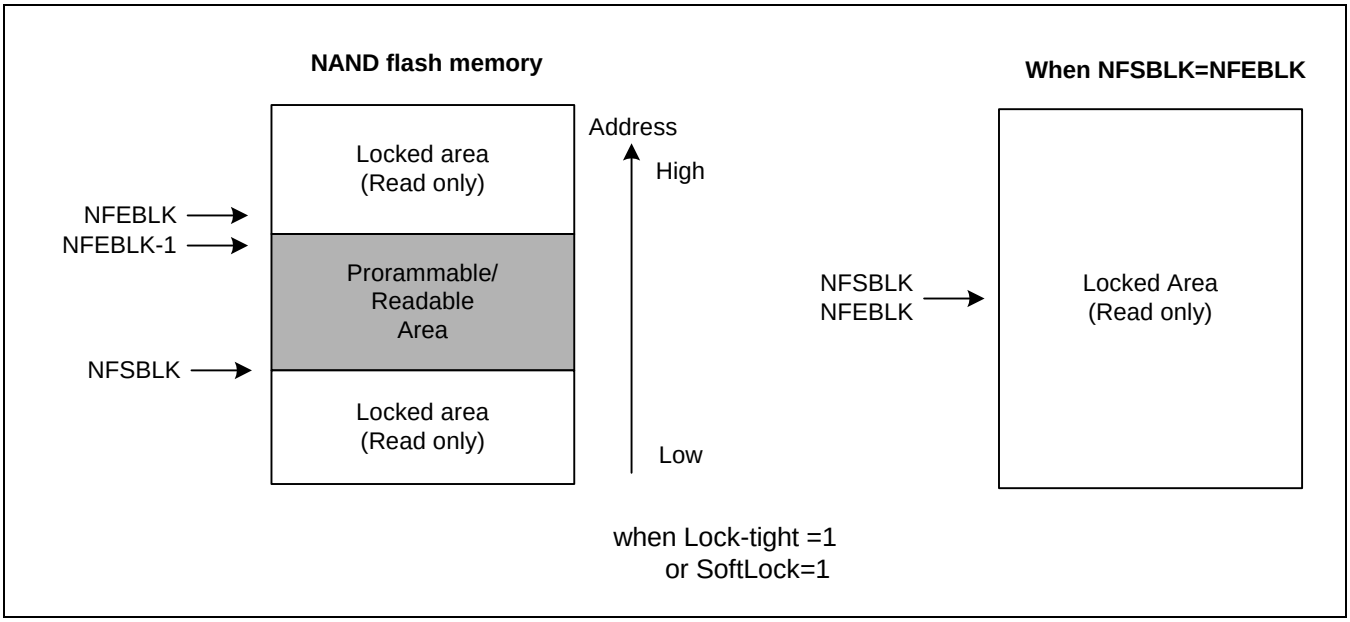
NFSBLK	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
SBLK_ADDR2	[23:16]	The 3rd block address of the block erase operation	0x00
SBLK_ADDR1	[15:8]	The 2nd block address of the block erase operation	0x00
SBLK_ADDR0	[7:0]	The 1st block address of the block erase operation (Only bit [7:5] are valid)	0x00

NOTE: Advance Flash's block Address start from 3-address cycle. So block address register only needs 3-bytes.

NFEBLK	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
EBLK_ADDR 2	[23:16]	The 3rd block address of the block erase operation	0x00
EBLK_ADDR 1	[15:8]	The 2nd block address of the block erase operation	0x00
EBLK_ADDR 0	[7:0]	The 1st block address of the block erase operation (Only bit [7:5] are valid)	0x00

NOTE: Advance Flash's block Address start from 3-address cycle. So block address register only needs 3-bytes.

The NFSLK and NFEBLK can be changed while Soft lock bit(NFCONT[12]) is enabled. But cannot be changed when Lock-tight bit(NFCONT[13]) is set.



NFCON STATUS REGISTER

Register	Address	R/W	Description	Reset Value
NFSTAT	0x4E000028	R/W	NAND Flash operation status register	0xXX00

NFSTAT	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0x00
ECCEncDone	[7]	When 4-bit ECC encodng is finished, this value set and issue interrupt if enabled. The NFMLCECC0 and NFMLCECC1 have valid values. To clear this write to '1' 1: 4-bit ECC encoding is completed	0
ECCDecDone	[6]	When 4-bit ECC decoding is finished, this value set and issue interrupt if enabled. The NFMLCBITPT, NFMLCL0 and NFMLCEL1 have valid values., .To clear this write to '1' 1: 4-bit ECC decoding is completed	0
IllegalAccess	[5]	Once Soft Lock or Lock-tight is enabled, The illegal access (program, erase) to the memory makes this bit set. 0: illegal access is not detected 1: illegal access is detected	0
RnB_ TransDetect	[4]	When RnB low to high transition is occurred, this value set and issue interrupt if enabled. To clear this write '1'. 0: RnB transition is not detected 1: RnB transition is detected Transition configuration is set in RnB_TransMode(NFCONT[8]).	0
NCE[1] (Read-only)	[3]	The status of nCE[1] output pin	1
nFCE (Read-only)	[2]	The status of nFCE output pin	1
Reserved	[1]	Reserved	0
RnB (Read-only)	[0]	The status of RnB input pin. 0: NAND Flash memory busy 1: NAND Flash memory ready to operate	1

ECC0/1 STATUS REGISTER

Register	Address	R/W	Description	Reset Value
NFECCERR0	0x4E00002C	R	NAND Flash ECC Error Status register for I/O [7:0]	0x00000000
NFECCERR1	0x4E000030	R	NAND Flash ECC Error Status register for I/O [15:8]	0x00000000

When ECCType is SLC.

NFESTAT0	Bit	Description	Initial State
Reserved	[31:25]	Reserved	
Serror DataNo	[24:21]	In spare area, Indicates which number data is error	00
Serror BitNo	[20:18]	In spare area, Indicates which bit is error	000
MErrorDataNo	[17:7]	In main data area, Indicates which number data is error	0x00
MErrorBitNo	[6:4]	In main data area, Indicates which bit is error	000
SpareError	[3:2]	Indicates whether spare area bit fail error occurred 00: No Error 01: 1-bit error(correctable) 10: Multiple error 11: ECC area error	00
MainError	[1:0]	Indicates whether main data area bit fail error occurred 00: No Error 01: 1-bit error(correctable) 10: Multiple error 11: ECC area error	00

NOTE: The above values are only valid when both ECC register and ECC status register have valid value.

NFESTAT1	Bit	Description	Initial State
Reserved	[31:25]	Reserved	
SErrorDataNo	[24:21]	In spare area, Indicates which number data is error	00
SErrorBitNo	[20:18]	In spare area, Indicates which bit is error	000
MErrorDataNo	[17:7]	In main data area, Indicates which number data is error	0x00
MErrorBitNo	[6:4]	In main data area, Indicates which bit is error	000
SpareError	[3:2]	Indicates whether spare area bit fail error occurred 00: No Error 01: 1-bit error(correctable) 10: Multiple error 11: ECC area error	00
MainError	[1:0]	Indicates whether main data area bit fail error occurred 00: No Error 01: 1-bit error(correctable) 10: Multiple error 11: ECC area error	00

NOTE: The above values are only valid when both ECC register and ECC status register have valid value.

When ECCType is MLC.

NFESTAT0	Bit	Description	Initial State
ECC Busy	[31]	Indicates the 4-bit ECC decoding engine is searching whether a error exists or not 0: Idle 1: Busy	0
ECC Ready	[30]	ECC Ready bit	1
Free Page	[29]	Inidicates the page data red from NAND flash has all 'FF' value.	0
MLC MECC Error	[28:26]	4-bit ECC decoding result 000: No error 001: 1-bit error 010: 2-bit error 011: 3-bit error 100: 4-bit error 101: Uncorrectable 11x: reserved	000
2nd Bit Error Location	[25:16]	Error byte location of 2nd bit error	0x00
Reserved	[15:10]	Reserved	
1st Bit Error Location	[9:0]	Error byte location of 1st bit error	0x00

NOTE: These values are updated when ECCDecDone (NFSTAT[6]) is set ('1').

NFESTAT1	Bit	Description	Initial State
Reserved	[31:26]	Reserved	0x00
4th Bit Error Location	[25:16]	Error byte location of 4th bit error	0x00
Reserved	[15:10]	Reserved	
3rd Bit Error Location	[9:0]	Error byte location of 3rd bit error	0x00

NOTE: These values are updated when ECCDecDone (NFSTAT[6]) is set ('1').

MAIN DATA AREA ECC0 STATUS REGISTER

Register	Address	R/W	Description	Reset Value
NFMECC0	0x4E000034	R	SLC or MLC NAND Flash ECC status register	0xXXXXXX
NFMECC1	0x4E000038	R	SLC or MLC NAND Flash ECC status register	0xXXXXXX

When ECCType is SLC

NFMECC0	Bit	Description	Initial State
MECC0_3	[31:24]	ECC3 for data[7:0]	0xXX
MECC0_2	[23:16]	ECC2 for data[7:0]	0xXX
MECC0_1	[15:8]	ECC1 for data[7:0]	0xXX
MECC0_0	[7:0]	ECC0 for data[7:0]	0xXX
MECC0_3	[31:24]	ECC3 for data[7:0]	0xXX

NFMECC1	Bit	Description	Initial State
MECC1_3	[31:24]	ECC3 data[15:8]	0xXX
MECC1_2	[23:16]	ECC2 data[15:8]	0xXX
MECC1_1	[15:8]	ECC1 data[15:8]	0xXX
MECC1_0	[7:0]	ECC0 data[15:8]	0xXX

NOTE: The NAND flash controller generate NFMECC0/1 when read or write main area data while the MainECCLock(NFCONT[7]) bit is '0'(Unlock).

When ECCType is MLC.

NFMECC0	Bit	Description	Initial State
4^{th} Parity	[31:24]	4^{th} Check Parity generated from main area (512-byte)	0x00
3^{rd} Parity	[23:16]	3^{rd} Check Parity generated from main area (512-byte)	0x00
2^{nd} Parity	[15:8]	2^{nd} Check Parity generated from main area (512-byte)	0x00
1^{st} Parity	[7:0]	1^{st} Check Parity generated from main area (512-byte)	0x00

NFMECC1	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
7^{th} Parity	[23:16]	7^{th} Check Parity generated from main area (512-byte)	0x00
6^{th} Parity	[15:8]	6^{th} Check Parity generated from main area (512-byte)	0x00
5^{th} Parity	[7:0]	5^{th} Check Parity generated from main area (512-byte)	0x00

NOTE: The NAND flash controller generate these ECC parity codes when write main area data while the MainECCLock (NFCON[7]) bit is '0'(unlock).

SPARE AREA ECC STATUS REGISTER

Register	Address	R/W	Description	Reset Value
NFSECC	0x4E00003C	R	NAND Flash ECC register for I/O [15:0]	0xXXXXXX

NFSECC	Bit	Description	Initial State
SECC1_1	[31:24]	Spare area ECC1 Status for I/O[15:8]	0xXX
SECC1_0	[23:16]	Spare area ECC0 Status for I/O[15:8]	0xXX
SECC0_1	[15:8]	Spare area ECC1 Status for I/O[7:0]	0xXX
SECC0_0	[7:0]	Spare area ECC0 Status for I/O[7:0]	0xXX

NOTE: The NAND flash controller generate NFSECC when read or write spare area data while the SpareECCLock(NFCONT[6]) bit is '0'(Unlock).

MLC 4-BIT ECC ERROR PATTEN REGISTER

Register	Address	R/W	Description	Reset Value
NFMLCBITPT	0x4E000040	R	NAND Flash 4-bit ECC Error Pattern register for data[7:0]	0x00000000

NFMLCBITPT	Bit	Description	Initial State
4th Error bit pattern	[31:24]	4th Error bit pattern	0x00
3rd Error bit pattern	[23:16]	3rd Error bit pattern	0x00
2nd Error bit pattern	[15:8]	2nd Error bit pattern	0x00
1st Error bit pattern	[7:0]	1st Error bit pattern	0x00

NOTES

8 CF CONTROLLER

OVERVIEW

CF controller supports PC card memory/IO mode & True-IDE mode.
CF controller is compatible with CF standard spec. R3.0.

FEATURES

The CF controller features:

The CF controller supports only 1 slot.

The CF controller consists of 2 parts – PC card controller & ATA controller. They are multiplexing from or to PAD signals. Users have to use the only 1 mode, PC card or True-IDE mode. Default mode is PC card mode. The CF controller has a top level SFR that has card power enable bit, output port enable bit & mode select (True-IDE or PC card) bit.

The PC card controller features:

The PC card controller has 2 half-word (16bits) write buffers & 4 half-word (16bits) read buffers.

The PC card controller has 5 word-sized (32bits) Special Function Registers.

- 3 timing configuration registers. (Attribute memory, Common memory, I/O interface)
- 1 status & control configuration register
- 1 interrupt source & mask register

Timing configuration register consists of 3 parts – Setup, Command & Hold.

- PC card interface has 4 state (IDLE, SETUP, COMMAND & HOLD)
- Each part of register indicates the operation timing of each state.

The ATA controller features:

The ATA controller is compatible with the ATA/ATAPI-6 standard.

The ATA controller has 30 word-sized (32bits) Special Function Registers.

The ATA controller has 1 FIFO that is 16 x 32bit.

The ATA controller has internal DMA controller (from ATA device to memory or from memory to ATA device).

AHB master (DMA controller) support 8 burst & word size transfer.

SIGNAL DESCRIPTION

CF interface Signals	Pins	I/O	Description
nCD_CF	1	I	Card detect signals (software control by GPIO MISCCR[30])
nIREQ_CF(EINT[19])	1	I	Interrupt request from CF card. PC card mode: active low (memory mode: level triggering, I/O mode: edge triggering). True-IDE mode: active high
nWAIT_CF(nWAIT)	1	I	Wait signal from CF card
nINPACK(EINT[20])	1	I	Input acknowledge in I/O mode PC card mode: not used True-IDE mode: DMA request
nCE1_CF(nRCS[2])	1	O	Card enable strobe PC card mode : lower byte enable strobe True-IDE mode : chip selection (nCS0)
nCE2_CF(nRCS[3])	1	O	Card enable strobe PC card mode: higher byte enable strobe True-IDE mode: chip selection (nCS1)
nREG_CF(EINT[21])	1	O	Register in CF card strobe PC card mode: It is used for accessing register in CF card True-IDE mode: DMA Acknowledge
nOE_CF(nOE_CF)	1	O	Output enable strobe PC card mode: output enable strobe for memory True-IDE mode: GND.
nWE_CF(nWE_CF)	1	O	Write enable strobe PC card mode: output enable strobe for memory True-IDE mode: VCC.
nIORD_CF(nROE)	1	O	Read strobe for I/O mode
nIOWR_CF(nRWE)	1	O	Write strobe for I/O mode
RESET_CF(EINT[22])	1	O	CF card reset PC card mode: active high True-IDE mode: active low
ADDR_CF(RADDR[10:0])	11	O	CF card address PC card mode: full address use True-IDE mode: only ADDR[2:0] use, The other address line is connected to GND.
DATA_CF(RDATA[15:0])	16	I/O	CF data bus
CARD_PWREN(EINT[23])	1	O	Card power enable strobe (active low)

BLOCK DIAGRAM

Top-Level Block Diagram

A top-level block diagram of the overall CF controller is shown below in Figure 8-1.

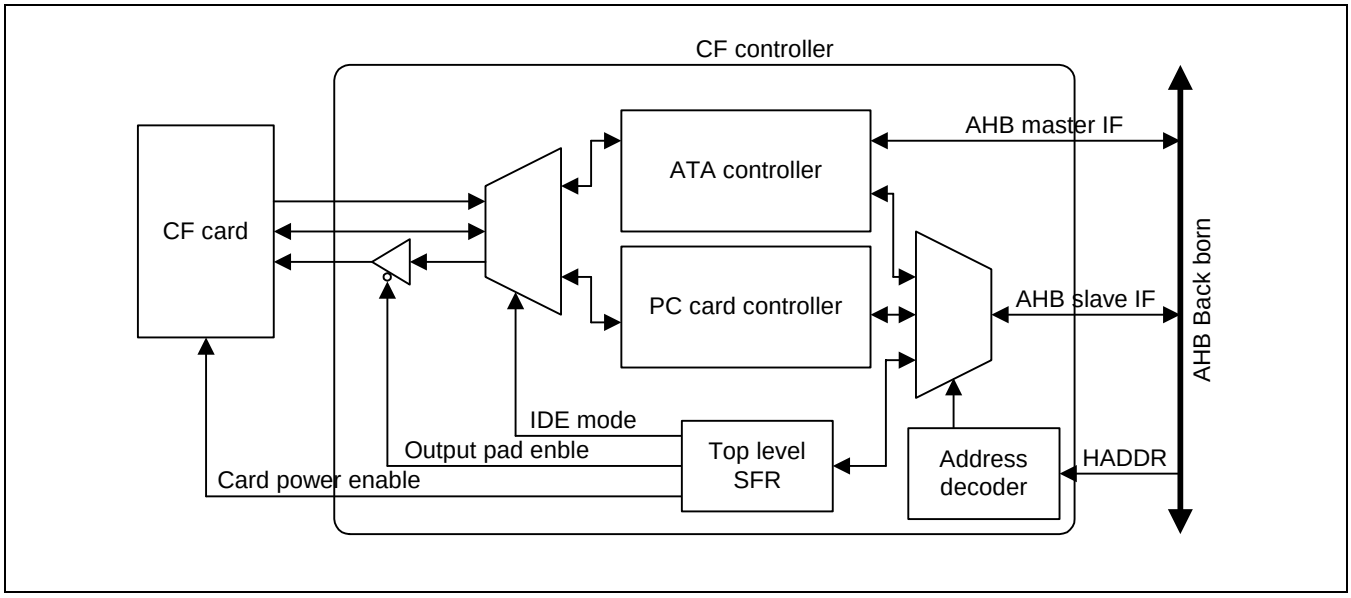


Figure 8-1. CF Controller Top Block Diagram

PC Card Controller Block Diagram

A top-level block diagram of the PC card controller is shown below in Figure 8-2.

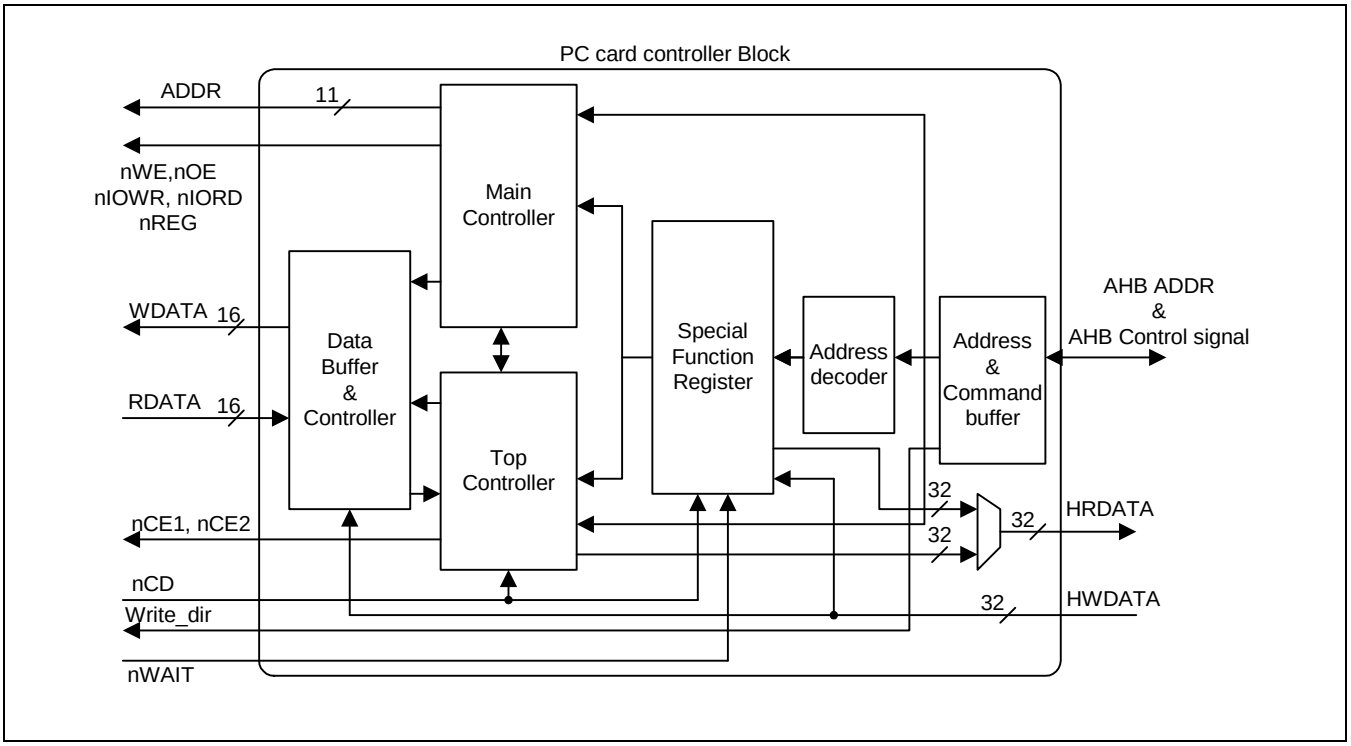


Figure 8-2. PC Card Controller Top Block Diagram

ATA Controller Block Diagram

A top-level block diagram of the ATA controller is shown below in Figure 8-3.

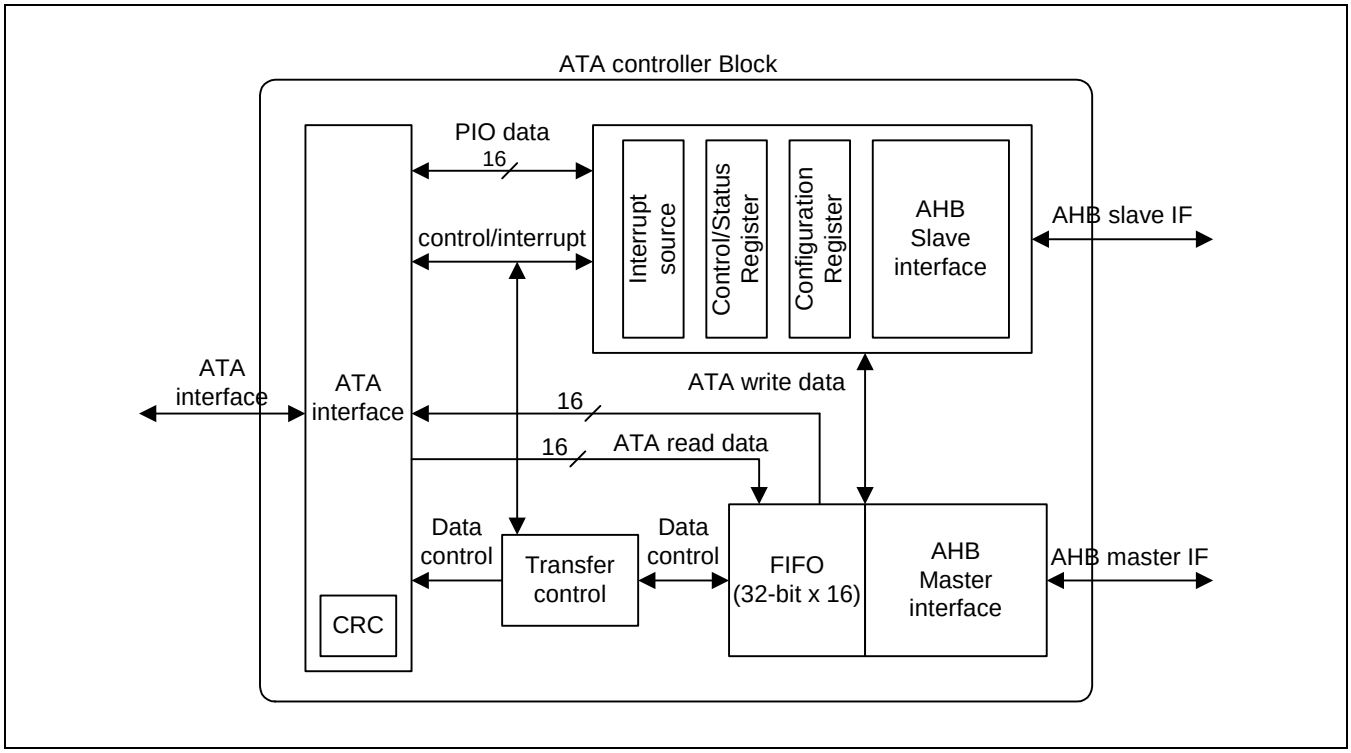


Figure 8-3. ATA Controller Top Block Diagram

TIMING DIAGRAM

PC Card Mode

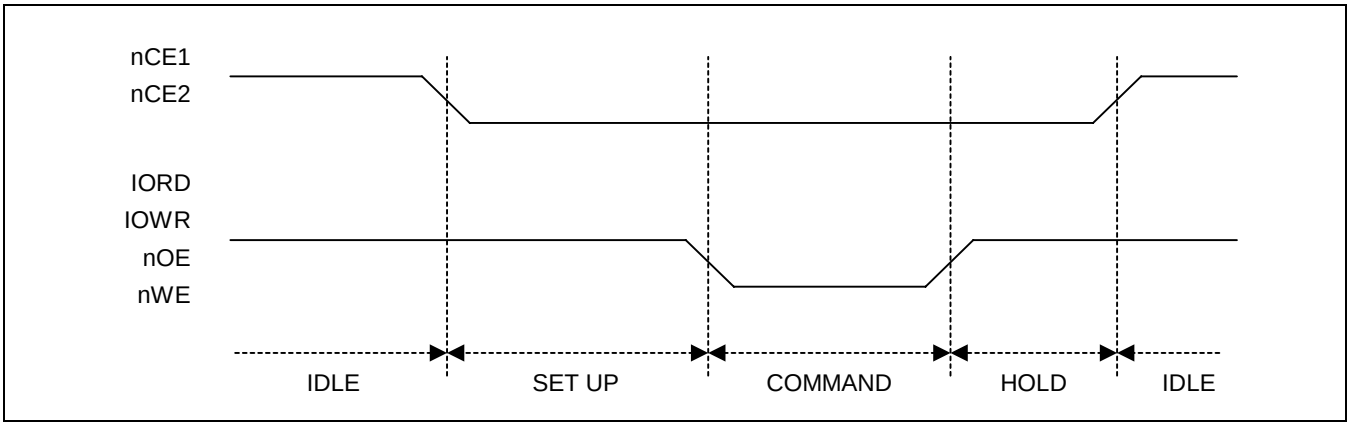


Figure 8-4. PC Card State Definition

Area	Attribute memory	I/O interface	Common memory
	(min, Max) nS		
Set up	(30, --)	(70, --)	(30, --)
Command	(150, --)	(165, --)	(150, --)
Hold	(30, --)	(20, --)	(20, --)
S + C + H	(300, --)	(290, --)	(--, --)

True-IDE Mode

PIO Mode

PIO Mode Waveform

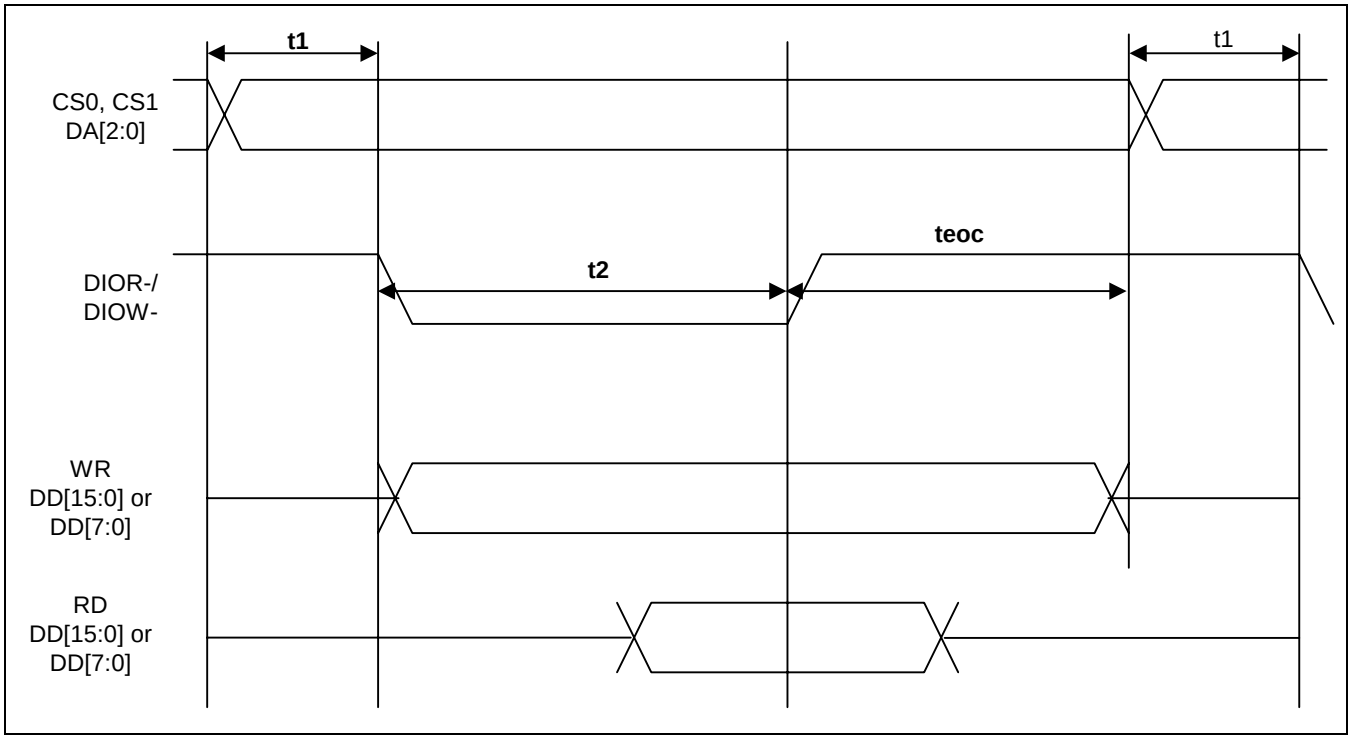


Figure 8-5. PIO Mode Waveform

Timing Parameter In PIO Mode

Table 8-1. Timing Parameter Each PIO Mode

PIO mode	PIO 0	PIO 1	PIO 2	PIO 3	PIO 4
T1	(70, --)	(50, --)	(30, --)	(30, --)	(25, --)
T2 (16bit)	(165, --)	(125, --)	(100, --)	(80, --)	(70, --)
T2 Register (8-bit)	(290, --)	(290, --)	(290, --)	(80, --)	(70, --)
TEOC	(20, --)	(15, --)	(10, --)	(10, --)	(10, --)
T1 + T2 + TEOC	(600, --)	(383, --)	(240, --)	(180, --)	(120, --)

ATA_PIO_TIME (Tpara) = PIO mode (min, max) / system clock – 1

UDMA Mode

UDMA-In Transfer (termination by device)

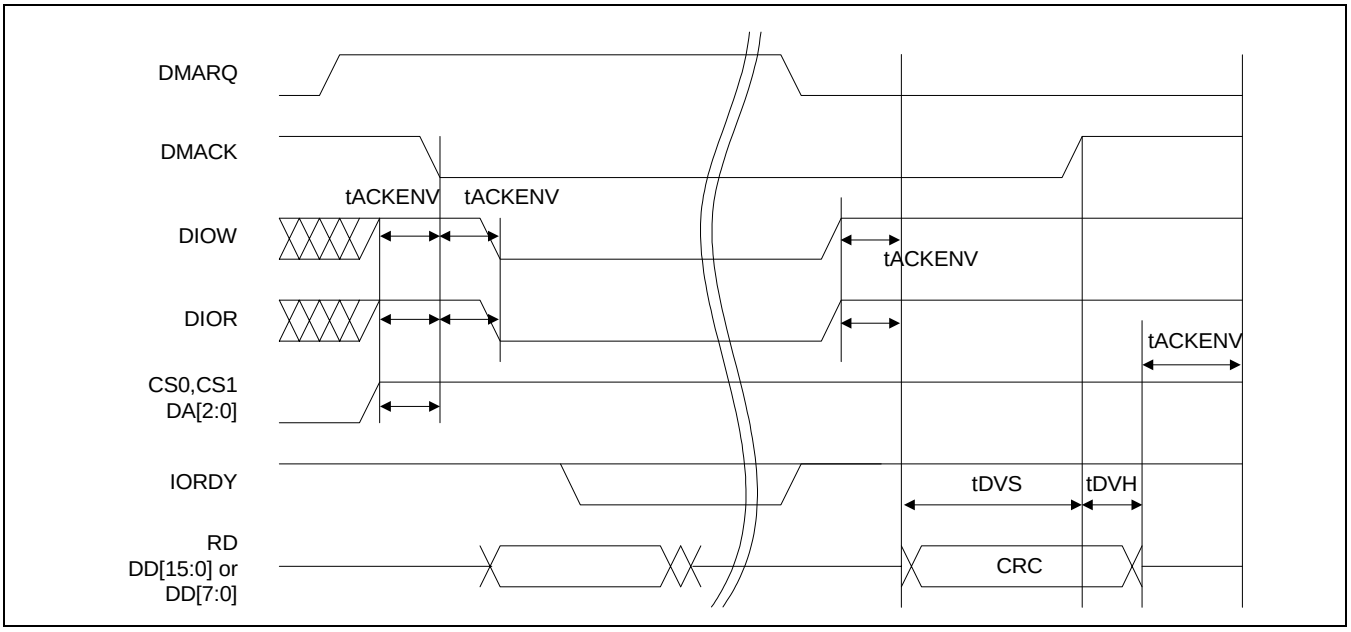


Figure 8-6. UDMA - In operation (terminated by device)

UDMA-In Transfer (termination by host)

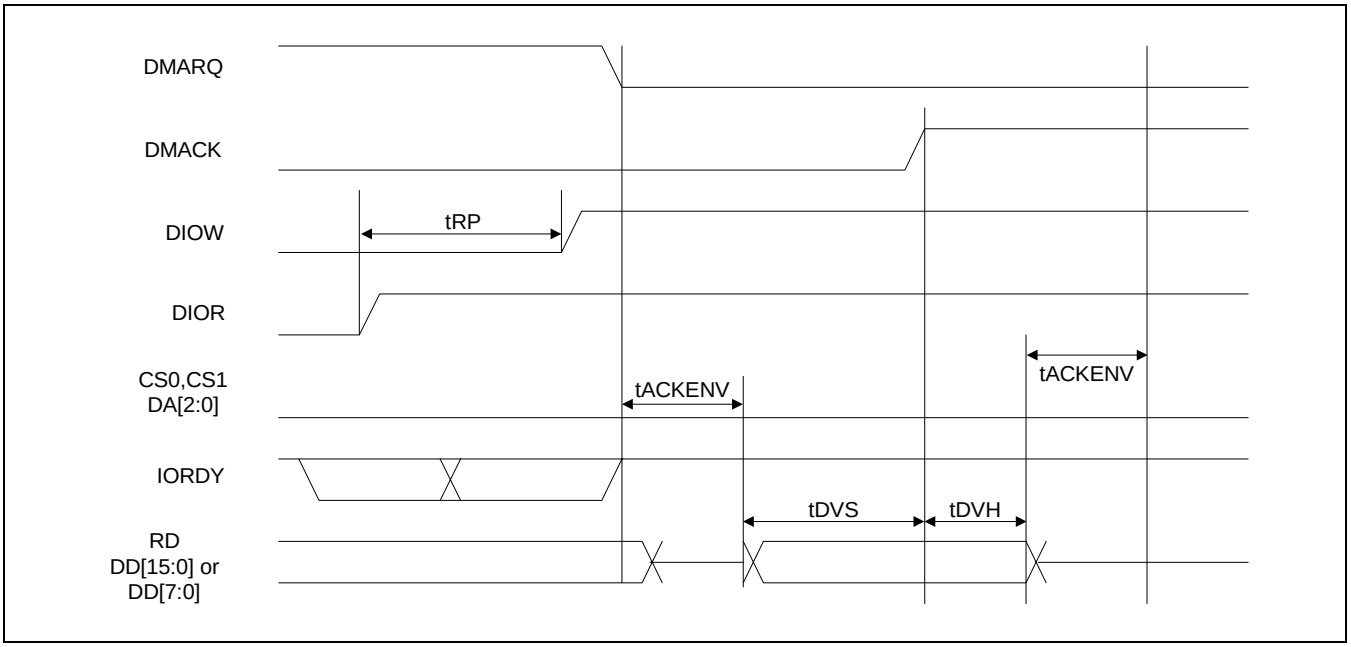


Figure 8-7. UDMA - In Operation (terminated by host)

UDMA-Out Transfer (termination by device)

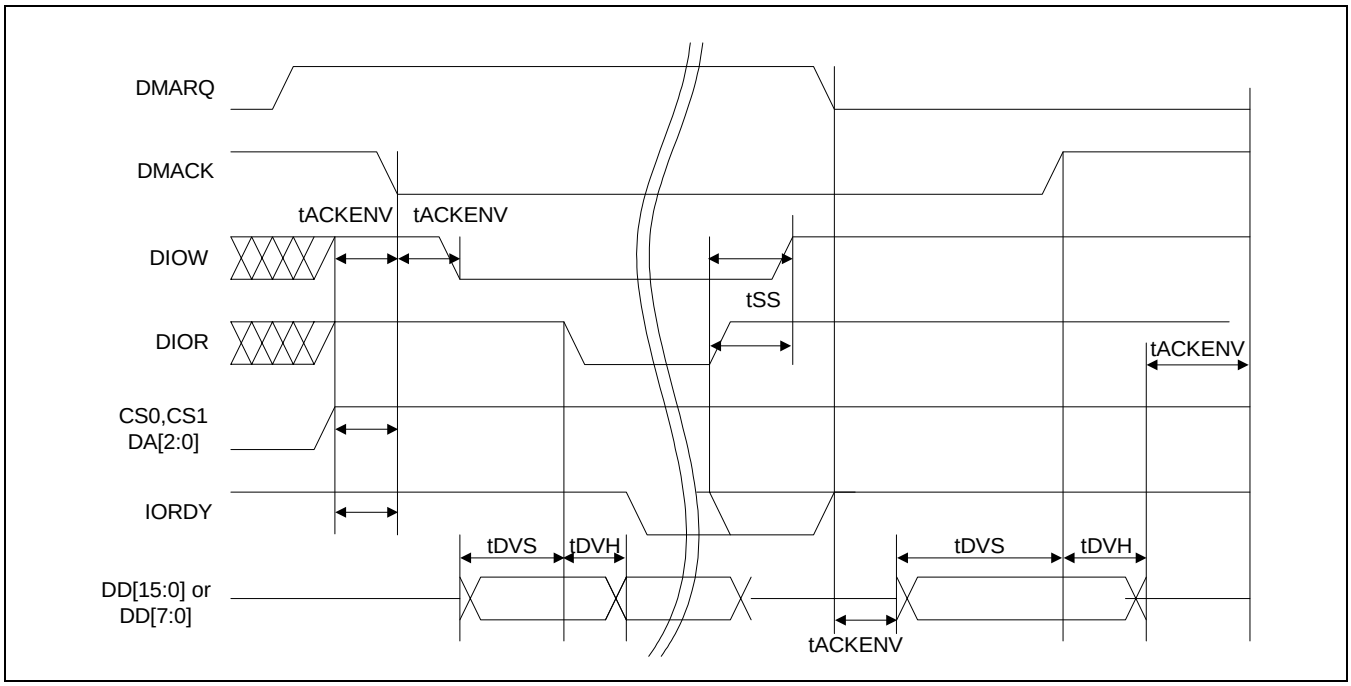


Figure 8-8. UDMA - Out Operation (terminated by device)

UDMA-Out Transfer (termination by host)

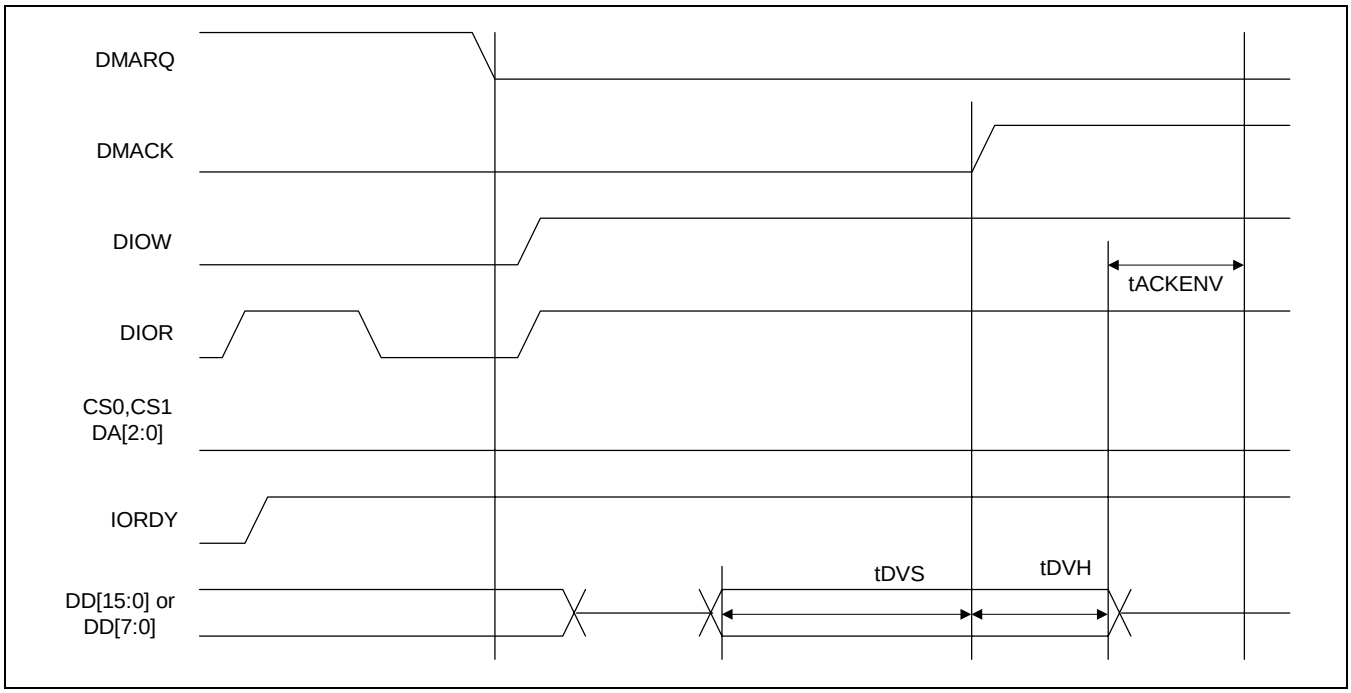


Figure 8-9. UDMA - Out Operation (terminated by host)

Timing Parameter In UDMA Mode

Table 8-2. Timing Parameter Each UDMA Mode

UDMA mode	UDMA 0	UDMA 1	UDMA 2	UDMA 3	UDMA 4
tACKENV	(20, 70)	(20, 70)	(20, 70)	(20, 55)	(20, 55)
tRP	(160, --)	(125, --)	(100, --)	(100, --)	(100, --)
tSS	(50, --)	(50, --)	(50, --)	(50, --)	(50, --)
tDVS	(70, --)	(48, --)	(31, --)	(20, --)	(6.7, --)
tDVH	(6.2, --)	(6.2, --)	(6.2, --)	(6.2, --)	(6.2, --)
tDVS+tDVH	(120, --)	(80, --)	(60, --)	(45, --)	(30, --)

ATA_UDMA_TIME (Tpara) = UDMA mode (min, max) / system clock – 1

SPECIAL FUNCTION REGISTERS

Memory Map

Memory Map Diagram (HSEL_SLV_Base = 0x4B80_0000)

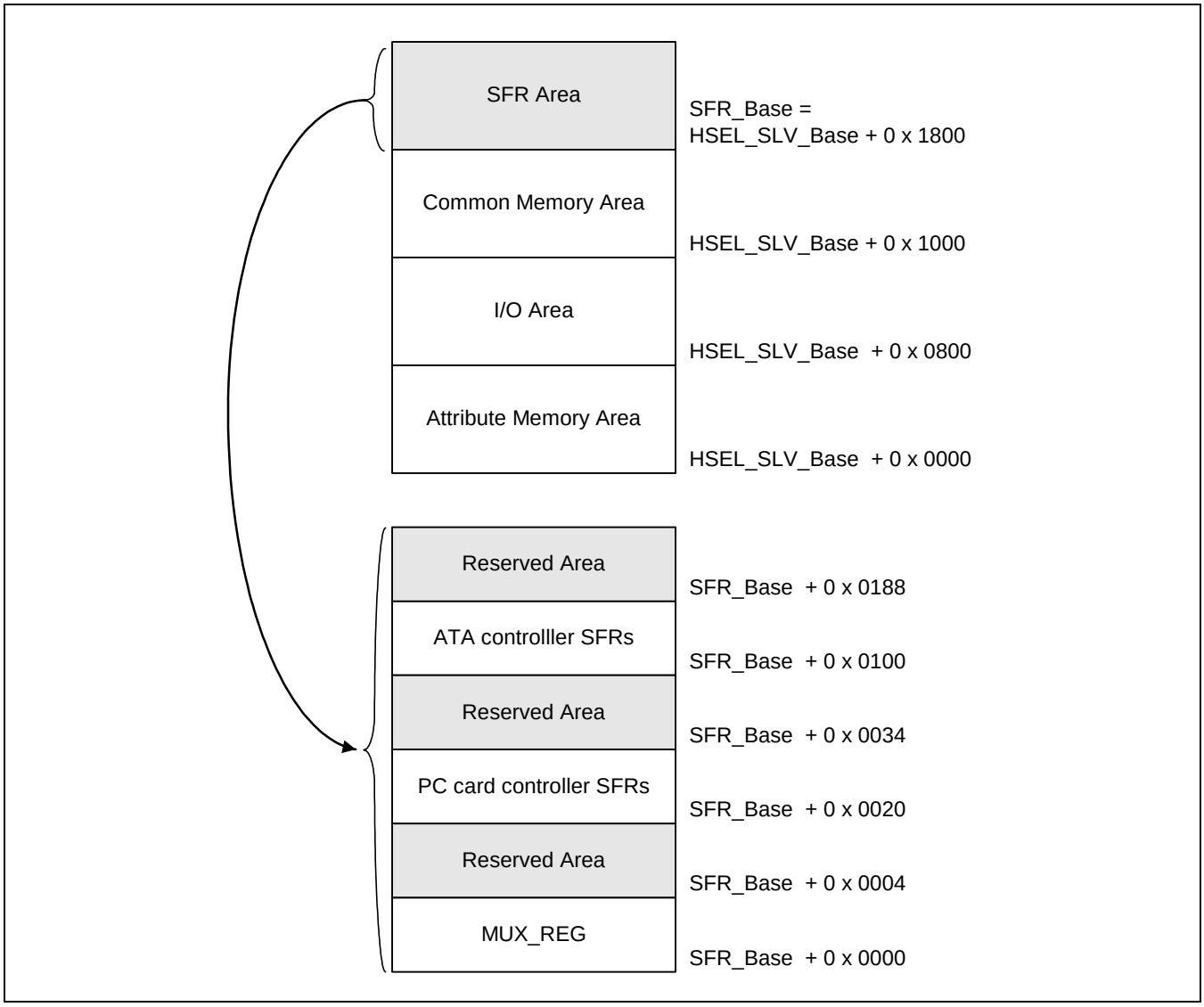


Figure 8-10. Memory Map Diagram

Memory Map Table

Table 8-3. Memory Map Table

Register	Address	Description	Reset Value
SFR_BASE	0x4B801800	CF card host controller base address	
MUX_REG	0x4B801800	Top level control & configuration register	0x00000006
Reserved	~ 0x001C	Reserved area	
PCCARD_BASE	0x4B801820	PC card controller base address	
PCCARD_CFG	0x4B801820	PC card configuration & status register	0x00000F07
PCCARD_INT	0x4B801824	PC card interrupt mask & source regiseter	0x00000700
PCCARD_ATTR	0x4B801828	PC card attribute memory area operation timing config regiseter	0x00031909
PCCARD_I/O	0x4B80182C	PC card I/O area operation timing config regiseter	0x00031909
PCCARD_COMM	0x4B801830	PC card common memory area operation timing config regiseter	0x00031909
Reserved	~ 0x00FC	Reserved area	
ATA_BASE	0x4B801900	ATA controller base address	
ATA_CONTROL	0x4B801900	ATA enable and clock down status	0x00000002
ATA_STATUS	0x4B801904	ATA status	0x00000000
ATA_COMMAND	0x4B801908	ATA command	0x00000000
ATA_SWRST	0x4B80190C	ATA software reset	0x00000000
ATA_IRQ	0x4B801910	ATA interrupt sources	0x00000000
ATA_IRQ_MASK	0x4B801914	ATA interrut mask	0x0000001F
ATA_CFG	0x4B801918	ATA configuration for ATA interface	0x00000000
Reserved	0x4B80191C ~ 0x4B801928	Reserved	
ATA_PIO_TIME	0x4B80192C	ATA PIO timing	0x0001C238
ATA_UDMA_TIME	0x4B801930	ATA UDMA timing	0x020b1362
ATA_XFR_NUM	0x4B801934	ATA transfer number	0x00000000
ATA_XFR_CNT	0x4B801938	ATA current transfer count	0x00000000
ATA_TBUF_START	0x4B80193C	ATA start address of track buffer	0x00000000
ATA_TBUF_SIZE	0x4B801940	ATA size of track buffer	0x00000000
ATA_SBUF_START	0x4B801944	ATA start address of source buffer	0x00000000
ATA_SBUF_SIZE	0x4B801948	ATA size of source buffer	0x00000000
ATA_CADR_TBUF	0x4B80194C	ATA current write address of track buffer	0x00000000

Table 8-3. Memory Map Table (Continued)

Register	Address	Description	Reset Value
ATA_CADR_SBUF	0x4B801950	ATA current read address of source buffer	0x00000000
ATA_PIO_DTR	0x4B801954	ATA PIO device data register	0x00000000
ATA_PIO_FED	0x4B801958	ATA PIO device Feature/Error register	0x00000000
ATA_PIO_SCR	0x4B80195C	ATA PIO sector count register	0x00000000
ATA_PIO_LLR	0x4B801960	ATA PIO device LBA low register	0x00000000
ATA_PIO_LMR	0x4B801964	ATA PIO device LBA middle register	0x00000000
ATA_PIO_LHR	0x4B801968	ATA PIO device LBA high register	0x00000000
ATA_PIO_DVR	0x4B80196C	ATA PIO device register	0x00000000
ATA_PIO_CSD	0x4B801970	ATA PIO device command/status register	0x00000000
ATA_PIO_DAD	0x4B801974	ATA PIO device control/alternate status register	0x00000000
ATA_PIO_RDATA	0x4B80197C	ATA PIO read data from device data register	0x00000000
BUS_FIFO_STATUS	0x4B801990	ATA internal AHB FIFO status	0x00000000
ATA_FIFO_STATUS	0x4B801994	ATA internal ATA FIFO status	0x00000000

INDIVIDUAL REGISTER DESCRIPTIONS

MUX_REG REGISTER

Register	Address	R/W	Description	Reset Value
MUX_REG	0x4B801800	R/W	MUX_REG is used to set the internal mode, output port enable & card power enable.	0x0000_0006

MUX_REG	Bit	Description	R/W	Reset Value
Reserved	[31:3]	Reserved bits	R	0x0
OUTPUT_EN	[2]	Output port enable 0 : output port enable 1 : output port disable	R/W	0x1
CARDPWR_EN	[1]	Card power supply enable 0 : card power on 1 : card power off	R/W	0x1
IDE_MODE	[0]	Internal operation mode select 0 : PC card mode 1 : True-IDE mode	R/W	0x0

PCCARD CONFIGURATION & STATUS REGISTER

Register	Address	R/W	Description	Reset Value
PCCARD_CFG	0x4B801820	R/W	PCCARD_CFG is used to set the configuration & read the status of card.	0x0000_0F07

PCCARD_CFG	Bits	Description	R/W	Reset Value
Reserved	[31:14]	Reserved bits	R	0x0
CARD_ RESET	[13]	CF card reset in PC card mode 0 : no reset 1 : reset	R/W	0x0
INT_SEL	[12]	Card interrupt request type select 0 : edge triggering 1 : level triggering	R/W	0x0
nWAIT_EN	[11]	nWAIT(from CF card) enable 0 : disable(always ready) 1 : enable	R/W	0x1
DEVICE_ATT	[10]	Device type is 16bits or 8bits (Attribute memory area) 0 : 8-bit device 1 : 16-bit device	R/W	0x1
DEVICE_ COMM	[9]	Device type is 16bits or 8bits (Common memory area) 0 : 8-bit device 1 : 16-bit device	R/W	0x1
DEVICE_IO	[8]	Device type is 16bits or 8bits (I/O area) 0 : 8-bit device 1 : 16-bit device	R/W	0x1
Reserved	[7:4]	Reserved bits	R	0x0
NOCARD_ERR	[3]	No card operation 0 : no error 1 : error	R	0x0
nWAIT	[2]	nWAIT from CF card 0 : wait 1 : ready	R	0x1
nIREQ	[1]	Interrupt request from CF card 0 : interrupt request 1 : no interrupt request	R	0x1
nCD	[0]	Card detect 0 : card detect 1 : card not detect	R	0x1

PCCARD INTERRUPT MASK & SOURCE REGISTER

Register	Address	R/W	Description	Reset Value
PCCARD_INT	0x4B801824	R/W	PCCARD_INT is interrupt source & interrupt mask register.	0x0000_0600

PCCARD_INT	Bits	Description	R/W	Reset Value
Reserved	[31:11]	Reserved bits	R	0x0
INTMSK_ ERR_N	[10]	Interrupt mask bit of no card error 0 : unmask 1 : mask	R/W	0x1
INTMSK_IREQ	[9]	Interrupt mask bit of CF card interrupt request 0 : unmask 1 : mask	R/W	0x1
INTMSK_CD	[8]	Interrupt mask bit of CF card detect 0 : unmask 1 : mask	R/W	0x0
Reserved	[7:3]	Reserved bits	R	0x0
INTSRC_ ERR_N	[2]	When host access no card in slot. CPU can clear this interrupt by writing “1”.	R/W	0x0
INTSRC_IREQ	[1]	When CF card interrupt request CPU can clear this interrupt by writing “1”.	R/W	0x0
INTSRC_CD	[0]	When CF card is detected in slot CPU can clear this interrupt by writing “1”.	R/W	0x0

PCCARD_ATTR REGISTER

Register	Address	R/W	Description	Reset Value
PCCARD_ ATTR	0x4B801828	R/W	PCCARD_ATTR is used to set the card access timing.	0x0003_1909

PCCARD_ATTR	Bits	Description	R/W	Reset Value
Reserved	[31:23]	Reserved bits	R	0x0
HOLD_ATTR	[22:16]	Hold state timing of attribute memory area Hold time = HCLK time * (HOLD_ATTR + 1)	R/W	0x03
Reserved	[15]	Reserved bits	R	0x0
CMND_ATTR	[14:8]	Command state timing of attribute memory area Command time = HCLK time * (CMND_ATTR + 1)	R/W	0x19
Reserved	[7]	Reserved bits	R	0x0
SETUP_ATTR	[6:0]	Setup state timing of attribute memory area Setup time = HCLK time * (SETUP_ATTR + 1)	R/W	0x09

PCCARD_I/O REGISTER

Register	Address	R/W	Description	Reset Value
PCCARD_I/O	0x4B80182C	R/W	PCCARD_I/O is used to set the card access timing.	0x0003_1909

PCCARD_I/O	Bits	Description	R/W	Reset Value
Reserved	[31:23]	Reserved bits	R	0x0
HOLD_IO	[22:16]	Hold state timing of I/O area Hold time = HCLK time * (HOLD_IO + 1)	R/W	0x03
Reserved	[15]	Reserved bits	R	0x0
CMND_IO	[14:8]	Command state timing of I/O area Command time = HCLK time * (CMND_IO + 1)	R/W	0x19
Reserved	[7]	Reserved bits	R	0x0
SETUP_IO	[6:0]	Setup state timing of I/O area Setup time = HCLK time * (SETUP_IO + 1)	R/W	0x09

PCCARD_COMM REGISTER

Register	Address	R/W	Description	Reset Value
PCCARD_ COMM	0x4B801830	R/W	PCCARD_COMM is used to set the card access timing.	0x0003_1909

PCCARD_COMM	Bits	Description	R/W	Reset Value
Reserved	[31:23]	Reserved bits	R	0x0
HOLD_COMM	[22:16]	Hold state timing of common memory area Hold time = HCLK time * (HOLD_COMM + 1)	R/W	0x03
Reserved	[15]	Reserved bits	R	0x0
CMND_COMM	[14:8]	Command state timing of common memory area Command time = HCLK time * (CMND_COMM + 1)	R/W	0x19
Reserved	[7]	Reserved bits	R	0x0
SETUP_COMM	[6:0]	Setup state timing of common memory area Setup time = HCLK time * (SETUP_COMM + 1)	R/W	0x09

ATA_CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
ATA_CONTROL	0x4B801900	R/W	ATA Control register	0x0000_0002

ATA_CONTROL	Bits	Description	R/W	Reset Value
Reserved	[31:2]	Reserved bits	R	0x0
clk_down_ready	[1]	Status for clock down This bit is asserted in idle state when ATA_CONTROL bit [0] is zero. 0 : not ready for clock down 1 : ready for clock down	R	0x1
ata_enable	[0]	ATA enable 0 : ATA is disabled and preparation for clock down maybe in progress 1 : ATA is enabled.	R/W	0x0

ATA_STATUS REGISTER

Register	Address	R/W	Description	Reset Value
ATA_STATUS	0x4B801904	R	ATA Status register	0x0000_0000

ATA_STATUS	Bits	Description	R/W	Reset Value
Reserved	[31:6]	Reserved bits	R	0x0
atadev_cblid	[5]	ATA cable identification	R	0x0
atadev_irq	[4]	ATA interrupt signal line	R	0x0
atadev_iordy	[3]	ATA iordy signal line	R	0x0
atadev_dmareq	[2]	ATA dmareq signal line	R	0x0
xfr_state	[1:0]	Transfer state 2'b00 : idle state 2'b01 : transfer state 2'b11 : wait for completion state	R	0x0

ATA_COMMAND REGISTER

Register	Address	R/W	Description	Reset Value
ATA_COMMAND	0x4B801908	R/W	ATA Command register	0x0000_0000

ATA_COMMAND	Bits	Description	R/W	Reset Value
Reserved	[31:2]	Reserved bits	R	0x0
xfr_command	[1:0]	ATA transfer command Four command types (START, STOP, ABORT and CONTINUE) are supported for data transfer control. The “START” command is used to start data transfer. The “STOP” command can pause transfer temporarily. The “CONTINUE” command shall be used after “STOP” command or internal state of “pause” when track buffer is full or UDMA hold state. The “ABORT” command terminated current data transfer sequences and make ATA host controller move to idle state. 00 : command stop 01 : command start (Only available in idle state) 10 : command abort 11 : command continue (Only available in transfer pause) ** After CPU commands ABORT, make a software reset by ATA_SWRST to clear the leftover values of internal registers.	R/W	0x0

The STOP command is a thing, which use when CPU wants to pause upon data transfer. When the CPU wants to judge the transmission data is valid or not while transfer transmits, for a moment.

To send data continually, give a CONTINUE command to do data transmission continuously.

The STOP command does control ATA Device side signal but does not control DMA side. Namely, if the FIFO has data after STOP command, DMA operation progresses until the FIFO has empty at read operation. In case of write operation, the DMA acts the same way until the FIFO has full.

The ABORT command uses when the transmitting data has proved useless data or discontinues absurd state by error interrupt from device.

At that time, all data in ATA Host controller (register, FIFO) cleared and the transmission state machine goes to IDLE.

The Software Reset's meaning become clear all registers even though the ABORT command had been executed before do configuration register set for next transmission. But it is not mandatory.

ATA_SWRST REGISTER

Register	Address	R/W	Description	Reset Value
ATA_SWRST	0x4B80190C	R/W	ATA S/W RESET register	0x0000_0000

ATA_SWRST	Bits	Description	R/W	Reset Value
Reserved	[31:1]	Reserved bits	R	0x0
ata_swrstn	[0]	Software reset for the ATA host 0: No reset 1: Software reset for all ATA host module. After software reset, to continue transfer, user must configure all registers of host controller and device registers.	R/W	0x0

ATA_IRQ REGISTER

Register	Address	R/W	Description	Reset Value
ATA_IRQ	0x4B801910	R/W	ATA IRQ register	0x0000_0000

ATA_IRQ	Bits	Description	R/W	Reset Value
Reserved	[31:5]	Reserved bits	R	0x0
sbuf_empty_int	[4]	When source buffer is empty. CPU can clear this interrupt by writing “1”.	R/W	0x0
tbuf_full_int	[3]	When track buffer is half full. CPU can clear this interrupt by writing “1”.	R/W	0x0
atadev_irq_int	[2]	When ATA device generates interrupt. CPU can clear this interrupt by writing “1”.	R/W	0x0
udma_hold_int	[1]	When ATA device makes early termination in UDMA class. CPU can clear this interrupt by writing “1”.	R/W	0x0
xfr_done_int	[0]	When all data transfers are finished. CPU can clear this interrupt by writing “1”.	R/W	0x0

ATA_IRQ_MASK REGISTER

Register	Address	R/W	Description	Reset Value
ATA_IRQ_MASK	0x4B801914	R/W	ATA IRQ MASK register	0x0000_001F

ATA_IRQ_MASK	Bits	Description	R/W	Reset Value
Reserved	[31:5]	Reserved bits	R	0x0
mask_sbut_ empty_int	[4]	Interrupt mask bit of source buffer empty 0 : unmask 1 : mask	R/W	0x1
mask_tbuf_ full_int	[3]	Interrupt mask bit of target buffer full 0 : unmask 1 : mask	R/W	0x1
mask_atadev_ irq_int	[2]	Interrupt mask bit of ATA device interrupt request 0 : unmask 1 : mask	R/W	0x1
mask_udma_ hold_int	[1]	Interrupt mask bit of UDMA hold 0 : unmask 1 : mask	R/W	0x1
mask_xfr_ done_int	[0]	Interrupt mask bit of xfr done 0 : unmask 1 : mask	R/W	0x1

ATA_CFG REGISTER

Register	Address	R/W	Description	Reset Value
ATA_CFG	0x4B801918	R/W	ATA Configuration register	0x0000_0000

ATA_CFG	Bits	Description	R/W	Reset Value
Reserved	[31:10]	Reserved bits	R	0x0
udma_auto_ mode	[9]	Determines whether to continue automatically in case of early termination in UDMA mode by Device. This bit should not be changed during runtime operation. 0: stay in pause state and wait for CPU's action. 1: continue automatically	R/W	0x0
sbuf_empty_ mode	[8]	Determines whether to continue automatically when source buffer is empty. This bit should not be changed during runtime operation. 0: continue automatically with new source buffer address. 1: stay in pause state and wait for CPU's action. ** With the sbuf_empty mode is "0" and the transmission data size is bigger than the source buffer size, the source buffer empty interrupt(sbuf_empty_int) happens before setting of the second source buffer base address and size. Then ATA host controller brings data from the first source buffer repeatedly. To avoid this, after 1st source buffer is empty, the "sbuf_empty_mode" bit automatically goes to HIGH even though the default is "0". So user must make a command "CONTINUE". And then user don't want that the CPU dose not interfere the change of the next source buffer address, set "0" at the bit 8 before/after the next base address and size.	R/W	0x0
tbuf_full_mode	[7]	Determines whether to continue automatically when track buffer is full. This bit should not be changed during runtime operation. 0: continue automatically with new track buffer address. 1: stay in pause state and wait for CPU's action. ** With the tbuf_full mode is "0" and the transmission data size is bigger than the target buffer size, the target buffer full interrupt(tbuf_full_int) happens before setting of the second target buffer base address and size. Then ATA host controller sends data to the first target buffer repeatedly. To avoid this, after 1st target buffer is full, the "tbuf_buf_mode" bit automatically goes to HIGH even though the default is "0". So user must make a command "CONTINUE". And then user don't want that the CPU dose not interfere the change of the next target buffer address, set "0" at the bit 8 before/after the next base address and size.	R/W	0x0

ATA_CFG	Bits	Description	R/W	Reset Value
byte_swap	[6]	Determines whether data endian is little or big in 16bit data. 0 : little endian (data[15:8], data[7:0]) 1 : big endian (data[7:0], data[15:8])	R/W	0x0
atadev_irq_al	[5]	Device interrupt signal level 0: active high 1: active low	R/W	0x0
dma_dir	[4]	DMA transfer direction 0 : Host read data from device 1 : Host write data to device	R/W	0x0
ata_class	[3:2]	ATA transfer class select 0 : transfer class is PIO 1 : transfer class is PIO DMA 2,3 : transfer class is UDMA	R/W	0x0
ata_iordy_en	[1]	Determines whether IORDY input can extend data transfer. 0 : IORDY disable(ignored) 1 : IORDY enable (can extend)	R/W	0x0
ata_rst	[0]	ATA device reset by this host. 0 : no reset 1 : reset	R/W	0x0

ATA_PIO_TIME REGISTER

Register	Address	R/W	Description	Reset Value
ATA_PIO_TIME	0x4B80192C	R/W	ATA PIO Timing Control register	0x0001_C238

ATA_PIO_TIME	Bits	Description	R/W	Reset Value
Reserved	[31:20]	Reserved bits	R	0x0
pio_teoc	[19:12]	PIO timing parameter, teoc, end of cycle time It shall not have zero value. teoc = HCLK time * (pio_teoc + 1)	R/W	0x1C
pio_t2	[11:4]	PIO timing parameter, t2, DIOR/Wn pulse width It shall not have zero value. t2 = HCLK time * (pio_t2 + 1)	R/W	0x23
pio_t1	[3:0]	PIO timing parameter, t1, address valid to DIOR/Wn t1 = HCLK time * (pio_t1 + 1)	R/W	0x8

ATA_UDMA_TIME REGISTER

Register	Address	R/W	Description	Reset Value
ATA_UDMA_TIME	0x4B801930	R/W	ATA UDMA Timing Control register	0x020B_1362

ATA_UDMA_TIME	Bits	Description	R/W	Reset Value
Reserved	[31:28]	Reserved bits	R	0x0
udma_tdvh	[27:24]	UDMA timing parameter tDVH tDVH = HCLK time * (udma_tdvh + 1)	R/W	0x2
udma_tdvs	[23:16]	UDMA timing parameter tDVS It shall not have zero value. tDVS = HCLK time * (udma_tdvs + 1)	R/W	0x0B
udma_trp	[15:8]	UDMA timing parameter tRP tRP = HCLK time * (udma_trp + 1)	R/W	0x13
udma_tss	[7:4]	UDMA timing parameter, tSS tSS = HCLK time * (udma_tss + 1)	R/W	0x6
udma_tackenv	[3:0]	UDMA timing parameter tENV(envelope time(from DMACKn to STOP and HDMARDYn), tACK(setup and hold time for DMACKn) tENV = HCLK time * (udma_tackenv + 1)	R/W	0x2

ATA_XFR_NUM REGISTER

Register	Address	R/W	Description	Reset Value
ATA_XFR_NUM	0x4B801934	R/W	ATA Data Transfer Number register	0x0000_0000

ATA_XFR_NUM	Bits	Description	R/W	Reset Value
xfr_num	[31:1]	Data transfer number.	R/W	0x00000000
Reserved	[0]	Reserved bits	R	0x0

ATA_XFR_CNT REGISTER

Register	Address	R/W	Description	Reset Value
ATA_XFR_CNT	0x4B801938	R/W	ATA Data Transfer Counter register	0x0000_0000

ATA_XFR_CNT	Bits	Description	R/W	Reset Value
xfr_cnt	[31:1]	Current remaining transfer counter. This value counts down from ATA_XFR_NUM. It goes to zero when pre-defined all data has been transferred.	R/W	0x00000000
Reserved	[0]	Reserved bits	R	0x0

ATA_TBUF_START REGISTER

Register	Address	R/W	Description	Reset Value
ATA_TBUF_ START	0x4B80193C	R/W	Start address of track buffer	0x0000_0000

ATA_TBUF_ START	Bits	Description	R/W	Reset Value
track_buffer_ start	[31:2]	Start address of track buffer (4byte unit)	R/W	0x00000000
Reserved	[1:0]	Reserved bits	R	0x0

ATA_TBUF_SIZE REGISTER

Register	Address	R/W	Description	Reset Value
ATA_TBUF_ SIZE	0x4B801940	R/W	Size of track buffer	0x0000_0000

ATA_TBUF_ SIZE	Bits	Description	R/W	Reset Value
track_buffer_ size	[31:5]	Size of track buffer (32byte unit) This should be set to “size_of_data_in_bytes – 1”. For example, to transfer 1-sector (512-byte, 32’h200), user should set 32’h1FF (= 32’h200 – 1).	R/W	0x0000000
Reserved	[4:0]	Reserved bits	R	0x00

ATA_SBUF_START REGISTER

Register	Address	R/W	Description	Reset Value
ATA_SBUF_ START	0x4B801944	R/W	Start address of source buffer	0x0000_0000

ATA_SBUF_ START	Bits	Description	R/W	Reset Value
src_buffer_start	[31:2]	Start address of source buffer (4byte unit)	R/W	0x00000000
Reserved	[1:0]	Reserved bits	R	0x0

ATA_SBUF_SIZE REGISTER

Register	Address	R/W	Description	Reset Value
ATA_SBUF_ SIZE	0x4B801948	R/W	Size of source buffer	0x0000_0000

ATA_SBUF_ SIZE	Bits	Description	R/W	Reset Value
src_buffer_ size	[31:5]	Size of source buffer (32byte unit) This should be set to “size_of_data_in_bytes – 1”. For example, to transfer 1-sector (512-byte, 32’h200), user should set 32’h1FF (= 32’h200 – 1).	R/W	0x0000000
Reserved	[4:0]	Reserved bits	R	0x00

ATA_CADDR_TBUF REGISTER

Register	Address	R/W	Description	Reset Value
ATA_CADDR_TBUF	0x4B80194C	R/W	Current address of track buffer	0x0000_0000

ATA_CADDR_TBUF	Bits	Description	R/W	Reset Value
track_buf_cur_adr	[31:2]	Current address of track buffer	R/W	0x00000000
Reserved	[1:0]	Reserved bits	R	0x0

ATA_CADDR_SBUF REGISTER

Register	Address	R/W	Description	Reset Value
ATA_CADDR_SBUF	0x4B801950	R/W	Current address of source buffer	0x0000_0000

ATA_CADDR_SBUF	Bits	Description	R/W	Reset Value
src_buf_cur_adr	[31:2]	Current address of source buffer	R/W	0x00000000
Reserved	[1:0]	Reserved bits	R	0x0

ATA_PIO_DTR REGISTER

Register	Address	R/W	Description	Reset Value
ATA_PIO_DTR	0x4B801954	W	16bit PIO data register	0x0000_0000

ATA_PIO_DTR	Bits	Description	R/W	Reset Value
Reserved	[31:16]	Reserved bits	R	0x0
pio_dev_dtr*	[15:0]	16-bit PIO data register	W	0x0000

NOTE: pio_dev_dtr can be read by accessing register ATA_PIO_RDATA

ATA_PIO_FED REGISTER

Register	Address	R/W	Description	Reset Value
ATA_PIO_FED	0x4B801958	W	8bit PIO device feature/error register	0x0000_0000

ATA_PIO_FED	Bits	Description	R/W	Reset Value
Reserved	[31:8]	Reserved bits	R	0x0
pio_dev_fed	[7:0]	8-bit PIO device feature/error (command block) register	W	0x00

NOTE: pio_dev_fed can be read by accessing register ATA_PIO_RDATA

ATA_PIO_SCR REGISTER

Register	Address	R/W	Description	Reset Value
ATA_PIO_SCR	0x4B80195C	W	8-bit PIO device sector count register	0x0000_0000

ATA_PIO_SCR	Bits	Description	R/W	Reset Value
Reserved	[31:8]	Reserved bits	R	0x0
pio_dev_scr	[7:0]	8-bit PIO device sector count (command block) register	W	0x00

NOTE: pio_dev_scr can be read by accessing register ATA_PIO_RDATA

ATA_PIO_LLR REGISTER

Register	Address	R/W	Description	Reset Value
ATA_PIO_LLR	0x4B801960	W	8-bit PIO device LBA low register	0x0000_0000

ATA_PIO_LLR	Bits	Description	R/W	Reset Value
Reserved	[31:8]	Reserved bits	R	0x0
pio_dev_llr	[7:0]	8-bit PIO device LBA low (command block) register	W	0x00

NOTE: pio_dev_llr can be read by accessing register ATA_PIO_RDATA

ATA_PIO_LMR REGISTER

Register	Address	R/W	Description	Reset Value
ATA_PIO_LMR	0x4B801964	W	8-bit PIO device LBA middle register	0x0000_0000

ATA_PIO_LMR	Bits	Description	R/W	Reset Value
Reserved	[31:8]	Reserved bits	R	0x0
pio_dev_lmr	[7:0]	8-bit PIO device LBA middle (command block) register	W	0x00

NOTE: pio_dev_lmr can be read by accessing register ATA_PIO_RDATA

ATA_PIO_LMR REGISTER

Register	Address	R/W	Description	Reset Value
ATA_PIO_LHR	0x4B801968	W	8-bit PIO device LBA high register	0x0000_0000

ATA_PIO_LHR	Bits	Description	R/W	Reset Value
Reserved	[31:8]	Reserved bits	R	0x0
pio_dev_lhr	[7:0]	8-bit PIO LBA high (command block) register	W	0x00

NOTE: pio_dev_lhr can be read by accessing register ATA_PIO_RDATA

ATA_PIO_DVR REGISTER

Register	Address	R/W	Description	Reset Value
ATA_PIO_DVR	0x4B80196C	W	8-bit PIO device register	0x0000_0000

ATA_PIO_DVR	Bits	Description	R/W	Reset Value
Reserved	[31:8]	Reserved bits	R	0x0
pio_dev_dvr	[7:0]	8-bit PIO device (command block) register	W	0x00

NOTE: pio_dev_dvr can be read by accessing register ATA_PIO_RDATA

ATA_PIO_CSD REGISTER

Register	Address	R/W	Description	Reset Value
ATA_PIO_CSD	0x4B801970	W	8-bit PIO device command/status register	0x0000_0000

ATA_PIO_CSD	Bits	Description	R/W	Reset Value
Reserved	[31:8]	Reserved bits	R	0x0
pio_dev_csd	[7:0]	8-bit PIO device command/status (command block) register	W	0x00

NOTE: pio_dev_csd can be read by accessing register ATA_PIO_RDATA

ATA_PIO_DAD REGISTER

Register	Address	R/W	Description	Reset Value
ATA_PIO_DAD	0x4B801974	W	8-bit PIO device control/alternate status register	0x0000_0000

ATA_PIO_DAD	Bits	Description	R/W	Reset Value
Reserved	[31:8]	Reserved bits	R	0x0
pio_dev_dad	[7:0]	8-bit PIO device control/alternate status (control block) register	W	0x00

NOTE: pio_dev_dad can be read by accessing register ATA_PIO_RDATA

ATA_PIO_RDATA REGISTER

Register	Address	R/W	Description	Reset Value
ATA_PIO_ RDATA	0x4B80197C	R	PIO read data register	0x0000_0000

ATA_PIO_ RDATA	Bits	Description	R/W	Reset Value
Reserved	[31:16]	Reserved bits	R	0x0
pio_rdata	[15:0]	PIO read data register while HOST read from ATA device register	R	0x0000

BUS_FIFO_STATUS REGISTER

Register	Address	R/W	Description	Reset Value
BUS_FIFO_ STATUS	0x4B801990	R	BUS FIFO status register	0x0000_0000

BUS_FIFO_ STATUS	Bits	Description	R/W	Reset Value
Reserved	[31:19]	Reserved bits	R	0x0
bus_state[2:0]	[18:16]	3'b000 : IDLE Another value is in operation.	R	0x00
Reserved	[15:14]	Reserved bits	R	0x0
bus_fifo_rdpnt	[13:8]	bus fifo read pointer	R	0x00
Reserved	[7:6]	Reserved bits	R	0x0
bus_fifo_wrpnt	[5:0]	bus fifo write pointer	R	0x00

ATA_FIFO_STATUS REGISTER

Register	Address	R/W	Description	Reset Value
ATA_FIFO_ STATUS	0x4B801994	R	ATA FIFO status register	0x0000_0000

ATA_FIFO_ STATUS	Bits	Description	R/W	Reset Value
Reserved	[31]	Reserved bit	R	0x0
ata_state	[30:28]	PIO read data register while HOST read from ATA device register	R	0x0000
pio_state	[27:26]	2'b00 : IDLE 2''b01 : T1 2'b10 : T2 2'b11 : TEOC	R	0x0
pdma_state	[25:24]	2'b00 : IDLE 2'b01 : T1 2'b10 : T2 2'b11 : TEOC	R	0x0
Reserved	[23:21]	Reserved bits	R	0x0
udma_state	[20:16]	5'b00000 : IDLE 5'b00100 : END Another value is in UDMA operation.	R	0x00
Reserved	[15:0]	Reserved bits	R	0x0

9 DMA CONTROLLER

OVERVIEW

S3C2443X supports six-channel DMA (Bridge DMA or peripheral DMA) controller that is located between the system bus and the peripheral bus. Each channel of DMA controller can perform data movements between devices in the system bus and/or peripheral bus with no restrictions. In other words, each channel can handle the following four cases: 1) both source and destination are in the system bus, 2) source is in the system bus while destination is in the peripheral bus, 3) source is in the peripheral bus while destination is in the system bus, 4) both source and destination are in the peripheral bus.

The main advantage of DMA is that it can transfer the data without CPU intervention. The operation of DMA can be initiated by S/W, or the request from internal peripherals, or the external request pins.

DMA REQUEST SOURCES

Each channel of DMA controller can select one source among 21 DMA sources if H/W DMA request mode is selected by REQSEL register. (Note that if S/W request mode is selected, this DMA request sources have no meaning at all.) The 21 DMA sources for each channel are as follows.

Table 9-1. DMA request sources for each channel

Bit	Source	Bit	Source	Bit	Source	Bit	Source
0	SPI_0_TX	8	Reserved	16	Reserved	24	UART_2[1]
1	SPI_0_RX	9	PWM Timer	17	nXDREQ0	25	UART_3[0]
2	SPI_1_TX	10	SDMMC	18	nXDREQ1	26	UART_3[1]
3	SPI_1_RX	11	Reserved	19	UART_0[0]	27	PCMOUT
4	I2S TX	12	Reserved	20	UART_0[1]	28	PCMIN
5	I2S RX	13	Reserved	21	UART_1[0]	29	MICIN
6	Reserved	14	Reserved	22	UART_1[1]	30	Reserved
7	Reserved	15	Reserved	23	UART_2[0]	31	Reserved

Here, nXDREQ0 and nXDREQ1 represent two external sources (External Devices).

DMA OPERATION

The details of DMA operation can be explained using three-state FSM (finite state machine) as follows:

State-1. As an initial state, it waits for the DMA request. If it comes, go to state-2. At this state, DMA ACK and INT REQ are 0.

State-2. In this state, DMA ACK becomes 1 and the counter (CURR_TC) is loaded from DCON[19:0] register. Note that DMA ACK becomes 1 and remains 1 until it is cleared later.

State-3. In this state, sub-FSM handling the atomic operation of DMA is initiated. The sub-FSM reads the data from the source address and then writes it to destination address. In this operation, data size and transfer size (single or burst) are considered. This operation is repeated until the counter (CURR_TC) becomes 0 in the whole service mode, while performed only once in a single service mode. The main FSM (this FSM) counts down the CURR_TC when the sub-FSM finishes each of atomic operation. In addition, this main FSM asserts the INT REQ signal when CURR_TC becomes 0 and the interrupt setting of DCON [29] register is set to 1. In addition, it clears DMA ACK if one of the following conditions is met.

1) CURR_TC becomes 0 in the whole service mode
2) atomic operation finishes in the single service mode.

Note that in the single service mode, these three states of main FSM are performed and then stops, and wait for another DMA REQ. And if DMA REQ comes in all three states are repeated. Therefore, DMA ACK is asserted and then de-asserted for each atomic transfer. In contrast, in the whole service mode, main FSM waits at state-3 until CURR_TC becomes 0. Therefore, DMA ACK is asserted during all the transfers and then de-asserted when TC reaches 0.

However, INT REQ is asserted only if CURR_TC becomes 0 regardless of the service mode (single service mode or whole service mode).

EXTERNAL DMA DREQ/DACK PROTOCOL

There are four types of external DMA request/acknowledge protocols. Each type defines how the signals like DMA request and acknowledge are related to these protocols.

Basic DMA Timing

The DMA service means paired Reads and Writes cycles during DMA operation, which is one DMA operation. The Figure. 9-1 shows the basic Timing in the DMA operation of the S3C2443X.

- The setup time and the delay time of XnXDREQ and XnXDACK are same in all the modes.
- If the completion of XnXDREQ meets its setup time, it is synchronized twice and then XnXDACK is asserted.
- After assertion of XnXDACK, DMA requests the bus and if it gets the bus it performs its operations. XnXDACK is deasserted when DMA operation finishes.

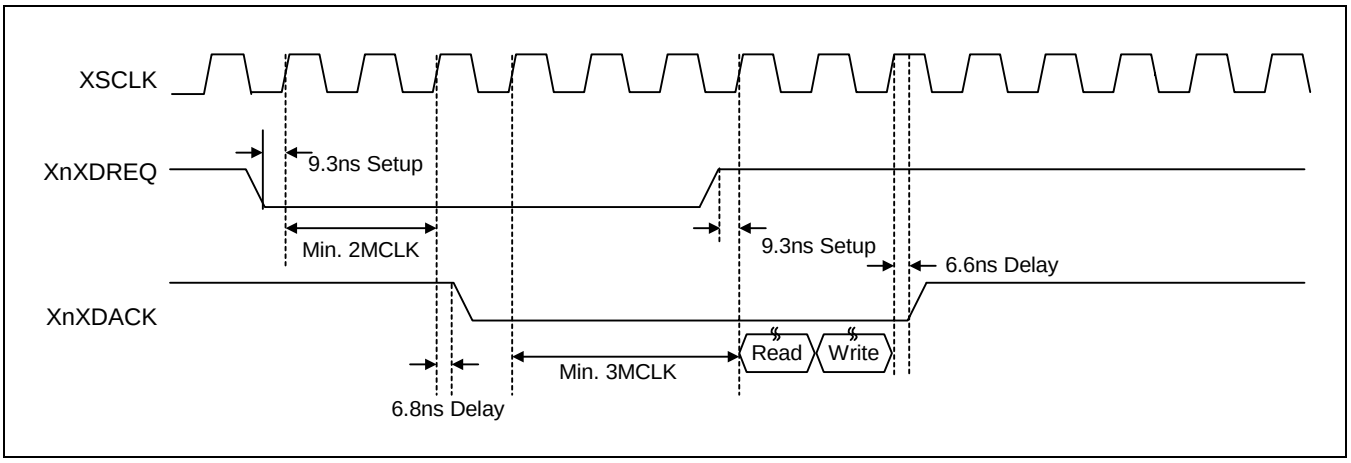


Figure 9-1. Basic DMA Timing Diagram

Demand/Handshake Mode Comparison – Related to the Protocol between XnXDREQ and XnXDACK

These are two different modes related to the protocol between XnXDREQ and XnXDACK. Figure. 9-2 shows the differences between these two modes i.e., Demand and Handshake modes.

At the end of one transfer (Single/Burst transfer), DMA checks the state of double-synched XnXDREQ.

Demand mode

- If XnXDREQ remains asserted, the next transfer starts immediately. Otherwise it waits for XnXDREQ to be asserted.

Handshake mode

- If XnXDREQ is deasserted, DMA deasserts XnXDACK in 2cycles. Otherwise it waits until XnXDREQ is deasserted.

  Caution: XnXDREQ has to be asserted (low) only after the deassertion (high) of XnXDACK.

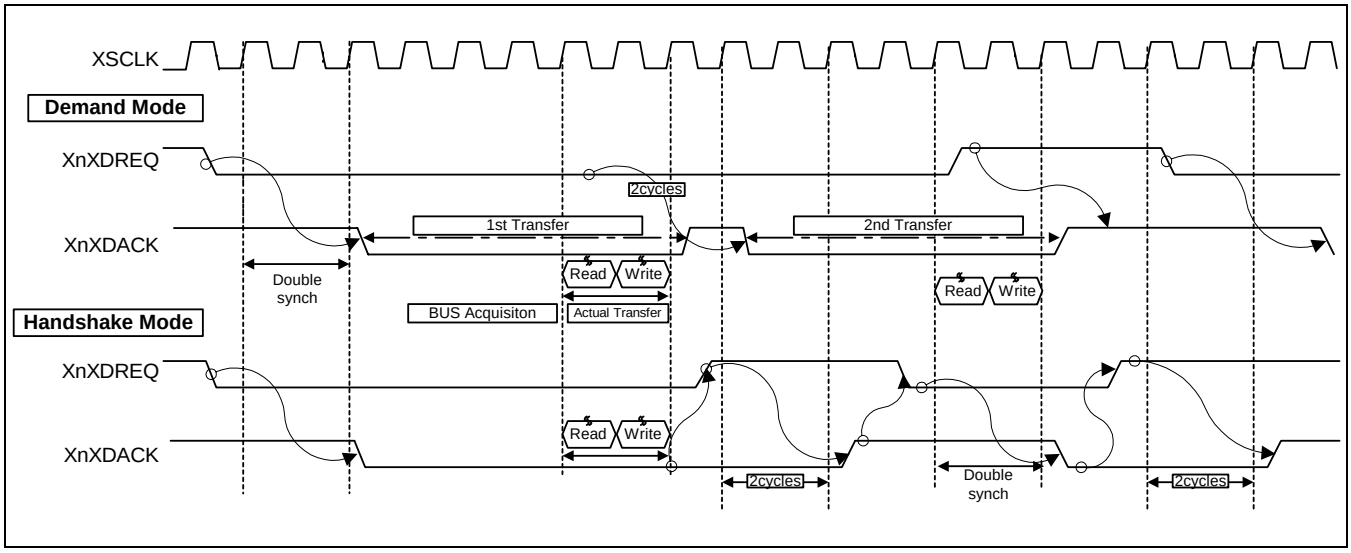


Figure 9-2. Demand/Handshake Mode Comparison

Transfer Size

- There are two different transfer sizes; single and Burst 4.
- DMA holds the bus firmly during the transfer of these chunk of data, thus other bus masters can not get the bus.

Burst 4 Transfer Size

4 sequential Reads and 4 sequential Writes are performed in the Burst 4 Transfer.

NOTE:

Single Transfer size: One read and one write are performed.

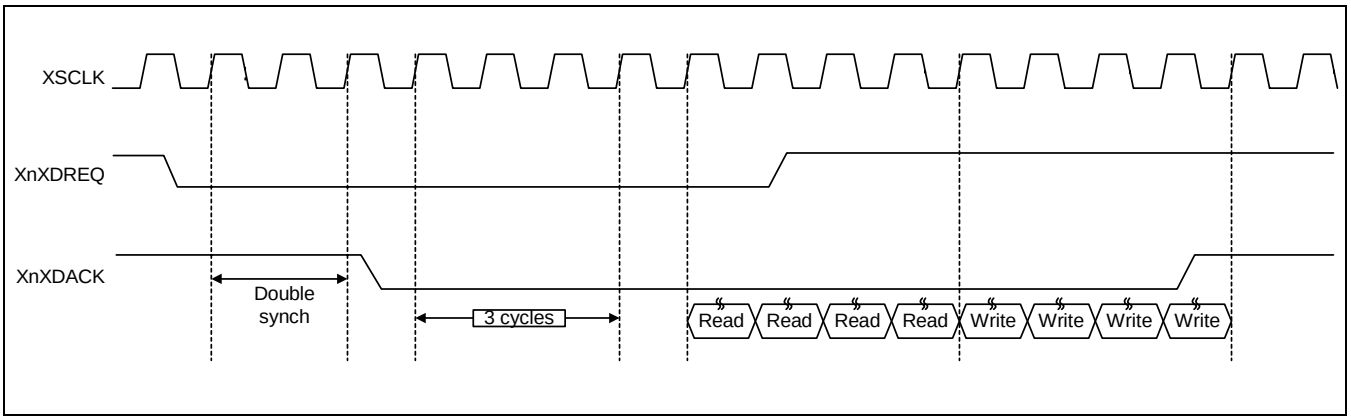


Figure 9-3. Burst 4 Transfer size

EXAMPLES OF POSSIBLE CASES

Single service, Demand Mode, Single Transfer Size

The assertion of XnXDREQ is need for every unit transfer (Single service mode), the operation continues while the XnXDREQ is asserted(Demand mode), and one pair of Read and Write(Single transfer size) is performed.

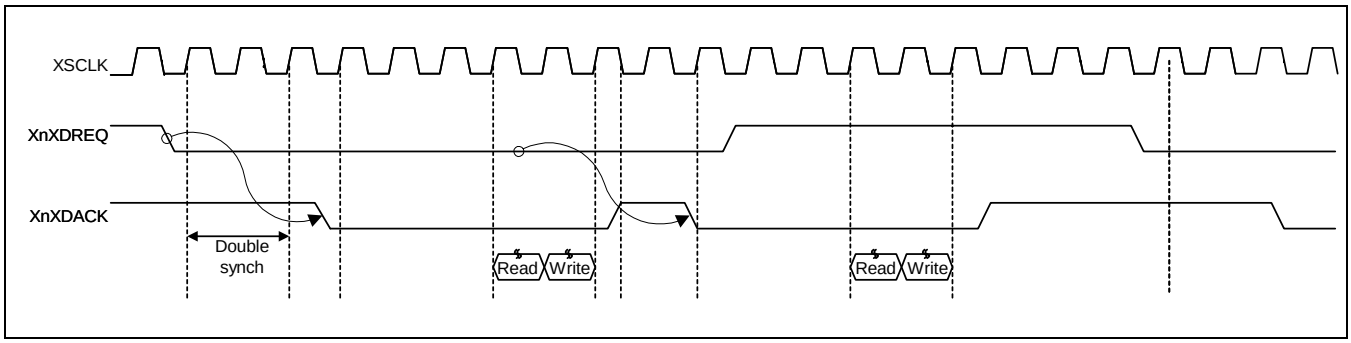


Figure 9-4. Single service, Demand Mode, Single Transfer Size

Single service/Handshake Mode, Single Transfer Size

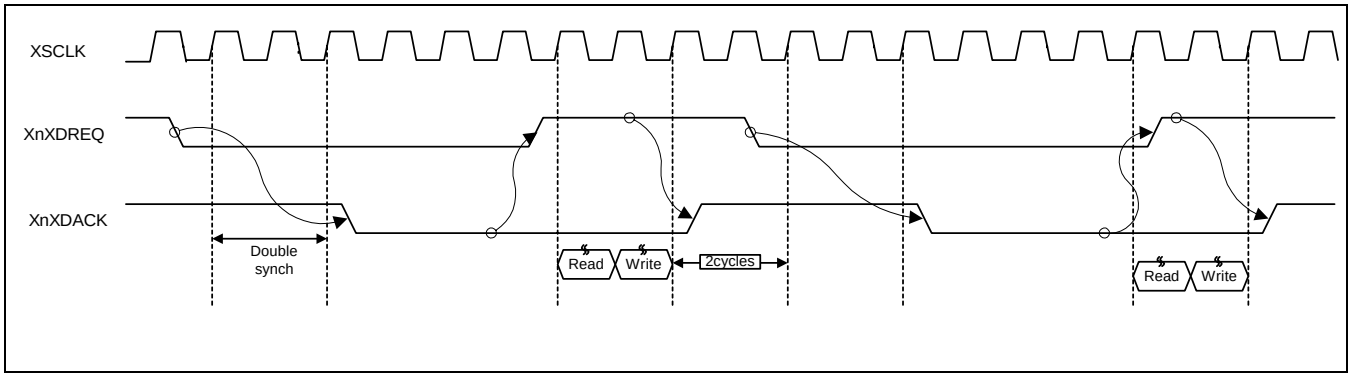


Figure 9-5. Single service, Handshake Mode, Single Transfer Size

Whole service/Handshake Mode, Single Transfer Size

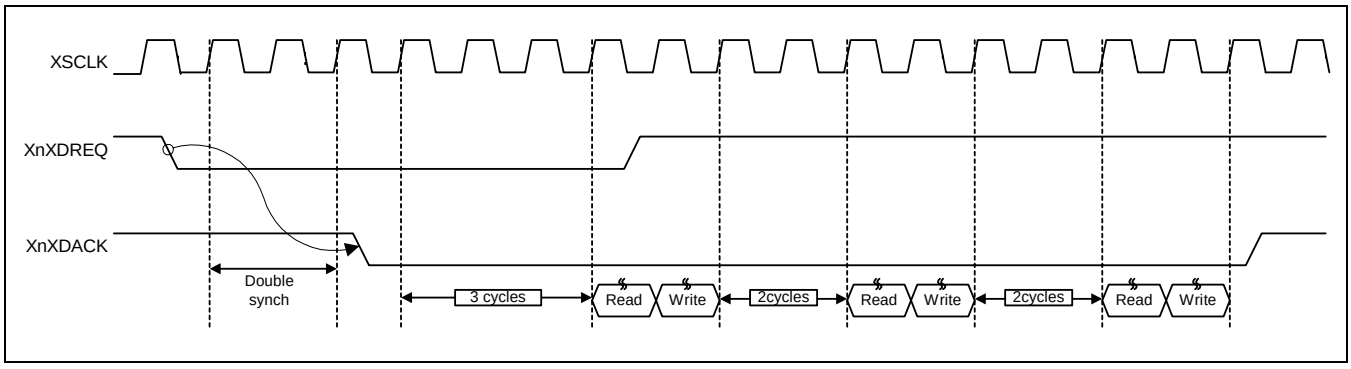


Figure 9-6. Whole service, Handshake Mode, Single Transfer Size

DMA SPECIAL REGISTERS

There are 10 control registers for each DMA channel. (Since there are six channels, the total number of control registers is 60.) Seven of them are to control the DMA transfer, and other three are to see the status of DMA controller. The details of those registers are as follows.

DMA INITIAL SOURCE REGISTER (DISRC)

Register	Address	R/W	Description	Reset Value
DISRC0	0x4B000000	R/W	DMA0 Initial Source Register	0x00000000
DISRC1	0x4B000100	R/W	DMA1 Initial Source Register	0x00000000
DISRC2	0x4B000200	R/W	DMA2 Initial Source Register	0x00000000
DISRC3	0x4B000300	R/W	DMA3 Initial Source Register	0x00000000
DISRC4	0x4B000400	R/W	DMA4 Initial Source Register	0x00000000
DISRC5	0x4B000500	R/W	DMA5 Initial Source Register	0x00000000

DISRCn	Bit	Description	Initial State
S_ADDR	[30:0]	These bits are the base address (start address) of source data to transfer. This value will be loaded into CURR_SRC only if the CURR_SRC is 0 and the DMA ACK is 1.	0x00000000

DMA INITIAL SOURCE CONTROL REGISTER (DISRCC)

Register	Address	R/W	Description	Reset Value
DISRCC0	0x4B000004	R/W	DMA0 Initial Source Control Register	0x00000000
DISRCC1	0x4B000104	R/W	DMA1 Initial Source Control Register	0x00000000
DISRCC2	0x4B000204	R/W	DMA2 Initial Source Control Register	0x00000000
DISRCC3	0x4B000304	R/W	DMA3 Initial Source Control Register	0x00000000
DISRCC4	0x4B000404	R/W	DMA4 Initial Source Control Register	0x00000000
DISRCC5	0x4B000504	R/W	DMA5 Initial Source Control Register	0x00000000

DISRCn	Bit	Description	Initial State
LOC	[1]	Bit 1 is used to select the location of source. 0: the source is in the system bus (AHB), 1: the source is in the peripheral bus (APB)	0
INC	[0]	Bit 0 is used to select the address increment. 0 = Increment 1= Fixed If it is 0, the address is increased by its data size after each transfer in burst and single transfer mode. If it is 1, the address is not changed after the transfer (In the burst mode, address is increased during the burst transfer, but the address is recovered to its first value after the transfer).	0

DMA INITIAL DESTINATION REGISTER (DIDST)

Register	Address	R/W	Description	Reset Value
DIDST0	0x4B000008	R/W	DMA0 Initial Destination Register	0x00000000
DIDST1	0x4B000108	R/W	DMA1 Initial Destination Register	0x00000000
DIDST2	0x4B000208	R/W	DMA2 Initial Destination Register	0x00000000
DIDST3	0x4B000308	R/W	DMA3 Initial Destination Register	0x00000000
DIDST4	0x4B000408	R/W	DMA4 Initial Destination Register	0x00000000
DIDST5	0x4B000508	R/W	DMA5 Initial Destination Register	0x00000000

DIDSTn	Bit	Description	Initial State
D_ADDR	[30:0]	These bits are the base address (start address) of destination for the transfer. This value will be loaded into CURR_SRC only if the CURR_SRC is 0 and the DMA ACK is 1.	0x00000000

DMA INITIAL DESTINATION CONTROL REGISTER (DIDSTC)

Register	Address	R/W	Description	Reset Value
DIDSTC0	0x4B00000C	R/W	DMA0 Initial Destination Control Register	0x00000000
DIDSTC1	0x4B00010C	R/W	DMA1 Initial Destination Control Register	0x00000000
DIDSTC2	0x4B00020C	R/W	DMA2 Initial Destination Control Register	0x00000000
DIDSTC3	0x4B00030C	R/W	DMA3 Initial Destination Control Register	0x00000000
DIDSTC4	0x4B00040C	R/W	DMA4 Initial Destination Control Register	0x00000000
DIDSTC5	0x4B00050C	R/W	DMA5 Initial Destination Control Register	0x00000000

DIDSTn	Bit	Description	Initial State
CHK_INT	[2]	Select interrupt occurrence time when auto reload is setting 0: interrupt will occur when TC reaches 0. 1: interrupt will occur after auto-reload is performed	0
LOC	[1]	Bit 1 is used to select the location of destination. 0: the destination is in the system bus (AHB). 1: the destination is in the peripheral bus (APB).	0
INC	[0]	Bit 0 is used to select the address increment. 0 = Increment 1= Fixed If it is 0, the address is increased by its data size after each transfer in burst and single transfer mode. If it is 1, the address is not changed after the transfer (In the burst mode, address is increased during the burst transfer, but the address is recovered to its first value after the transfer).	0

DMA CONTROL REGISTER (DCON)

Register	Address	R/W	Description	Reset Value
DCON0	0x4B000010	R/W	DMA0 Control Register	0x00000000
DCON1	0x4B000110	R/W	DMA1 Control Register	0x00000000
DCON2	0x4B000210	R/W	DMA2 Control Register	0x00000000
DCON3	0x4B000310	R/W	DMA3 Control Register	0x00000000
DCON4	0x4B000410	R/W	DMA4 Control Register	0x00000000
DCON5	0x4B000510	R/W	DMA5 Control Register	0x00000000

DCONn	Bit	Description	Initial State
DMD_HS	[31]	Select one between demand mode and handshake mode. 0 : demand mode is selected 1 : handshake mode is selected. In both modes, DMA controller starts its transfer and asserts DACK for a given asserted DREQ. The difference between two modes is whether it waits for the de-asserted DACK or not. In handshake mode, DMA controller waits for the de-asserted DREQ before starting a new transfer. If it sees the de-asserted DREQ, it de-asserts DACK and waits for another asserted DREQ. In contrast, in the demand mode, DMA controller does not wait until the DREQ is de-asserted. It just de-asserts DACK and then starts another transfer if DREQ is asserted. We recommend using handshake mode for external DMA request sources to prevent unintended starts of new transfers.	0
SYNC	[30]	Select DREQ/DACK synchronization. 0: DREQ and DACK are synchronized to PCLK (APB clock). 1: DREQ and DACK are synchronized to HCLK (AHB clock). Therefore, devices attached to AHB system bus, this bit has to be set to 1, while those attached to APB system, it should be set to 0. For the devices attached to external system, user should select this bit depending on whether the external system is synchronized with AHB system or APB system.	0
INT	[29]	Enable/Disable the interrupt setting for CURR_TC(terminal count) 0: CURR_TC interrupt is disabled. User has to look the transfer count in the status register. (i.e., polling) 1: interrupt request is generated when all the transfer is done (i.e., CURR_TC becomes 0).	0
TSZ	[28]	Select the transfer size of an atomic transfer (i.e., transfer performed at each time DMA owns the bus before releasing the bus). 0: a unit transfer is performed. 1: a burst transfer of length four is performed.	0

DCONn	Bit	Description	Initial State
SERVMODE	[27]	Select the service mode between single service mode and whole service mode. 0: single service mode is selected in which after each atomic transfer (single or burst of length four) DMA stops and waits for another DMA request. 1: whole service mode is selected in which one request gets atomic transfers to be repeated until the transfer count reaches to 0. In this mode, additional request is not required. Here, note that even in the whole service mode, DMA releases the bus after each atomic transfer and then tries to re-get the bus to prevent starving of other bus masters.	0
Reserved	[26:25]	Reserved for future use	00
PADDRFIX	[24]	APB Address fix control 0: increment, 1: fix If you want to fix the APB address during burst operation, set this bit to 1.	0
Reserved	[23]	Reserved for future use	0
RELOAD	[22]	Set the reload on/off option. 0: auto reload is performed when a current value of transfer count becomes 0 (i.e., all the required transfers are performed). 1: DMA channel (DMA REQ) is turned off when a current value of transfer count becomes 0. The channel on/off bit(DMASKTRIGn[1]) is set to 0(DREQ off) to prevent unintended further start of new DMA operation	0
DSZ	[21:20]	Data size to be transferred. 00 = Byte 01 = Half word 10 = Word 11 = reserved	00
TC	[19:0]	Initial transfer count (or transfer beat). Note that the actual number of bytes that are transferred is computed by the following equation: DSZ x TSZ x TC, where DSZ, TSZ, and TC represent data size (DCONn[21:20]), transfer size (DCONn[28]), and initial transfer count, respectively. This value will be loaded into CURR_TC only if the CURR_TC is 0 and the DMA ACK is 1.	00000

DMA STATUS REGISTER (DSTAT)

Register	Address	R/W	Description	Reset Value
DSTAT0	0x4B000014	R	DMA0 Count Register	000000h
DSTAT1	0x4B000114	R	DMA1 Count Register	000000h
DSTAT2	0x4B000214	R	DMA2 Count Register	000000h
DSTAT3	0x4B000314	R	DMA3 Count Register	000000h
DSTAT4	0x4B000414	R	DMA4 Count Register	000000h
DSTAT5	0x4B000514	R	DMA5 Count Register	000000h

DSTATn	Bit	Description	Initial State
STAT	[21:20]	Status of this DMA controller. 00: It indicates that DMA controller is ready for another DMA request. 01: It indicates that DMA controller is busy for transfers.	00b
CURR_TC	[19:0]	Current value of transfer count. Note that transfer count is initially set to the value of DCONn[19:0] register and decreased by one at the end of every atomic transfer.	00000h

DMA CURRENT SOURCE REGISTER (DCSRC)

Register	Address	R/W	Description	Reset Value
DCSRC0	0x4B000018	R	DMA0 Current Source Register	0x00000000
DCSRC1	0x4B000118	R	DMA1 Current Source Register	0x00000000
DCSRC2	0x4B000218	R	DMA2 Current Source Register	0x00000000
DCSRC3	0x4B000318	R	DMA3 Current Source Register	0x00000000
DCSRC4	0x4B000418	R	DMA4 Current Source Register	0x00000000
DCSRC5	0x4B000518	R	DMA5 Current Source Register	0x00000000

DCSRCn	Bit	Description	Initial State
CURR_SRC	[30:0]	Current source address for DMAn.	0x00000000

CURRENT DESTINATION REGISTER (DCDST)

Register	Address	R/W	Description	Reset Value
DCDST0	0x4B00001C	R	DMA0 Current Destination Register	0x00000000
DCDST1	0x4B00011C	R	DMA1 Current Destination Register	0x00000000
DCDST2	0x4B00021C	R	DMA2 Current Destination Register	0x00000000
DCDST3	0x4B00031C	R	DMA3 Current Destination Register	0x00000000
DCDST4	0x4B00041C	R	DMA4 Current Destination Register	0x00000000
DCDST5	0x4B00051C	R	DMA5 Current Destination Register	0x00000000

DCDSTn	Bit	Description	Initial State
CURR_DST	[30:0]	Current destination address for DMAn.	0x00000000

DMA MASK TRIGGER REGISTER (DMASKTRIG)

Register	Address	R/W	Description	Reset Value
DMASKTRIG0	0x4B000020	R/W	DMA0 Mask Trigger Register	000
DMASKTRIG1	0x4B000120	R/W	DMA1 Mask Trigger Register	000
DMASKTRIG2	0x4B000220	R/W	DMA2 Mask Trigger Register	000
DMASKTRIG3	0x4B000320	R/W	DMA3 Mask Trigger Register	000
DMASKTRIG4	0x4B000420	R/W	DMA4 Mask Trigger Register	000
DMASKTRIG5	0x4B000520	R/W	DMA5 Mask Trigger Register	000

DMASKTRIGn	Bit	Description	Initial State
STOP	[2]	Stop the DMA operation. 1: DMA stops as soon as the current atomic transfer ends. If there is no current running atomic transfer, DMA stops immediately. The CURR_TC, CURR_SRC, CURR_DST will be 0. NOTE: Due to possible current atomic transfer, “stop” may take several cycles. The finish of “stopping” operation (i.e., actual stop time) can be detected by waiting until the channel on/off bit (DMASKTRIGn[1]) is set to off. This stop is “actual stop”.	0
ON_OFF	[1]	DMA channel on/off bit. 0: DMA channel is turned off. (DMA request to this channel is ignored.) 1: DMA channel is turned on and the DMA request is handled. This bit is automatically set to off if we set the DCONn[22] bit to “no auto reload” and/or STOP bit of DMASKTRIGn to “stop”. Note that when DCON [22] bit is "no auto reload", this bit becomes 0 when CURR_TC reaches 0. If the STOP bit is 1, this bit becomes 0 as soon as the current atomic transfer finishes. NOTE. This bit should not be changed manually during DMA operations (i.e., this has to be changed only by using DCON [22] or STOP bit.)	0
SW_TRIG	[0]	Trigger the DMA channel in S/W request mode. 1: it requests a DMA operation to this controller. However, note that for this trigger to have effects S/W request mode has to be selected (DCONn[23]) and channel ON_OFF bit has to be set to 1 (channel on). When DMA operation starts, this bit is cleared automatically.	0

NOTE: You can freely change the values of DISRC register, DIDST registers, and TC field of DCON register. Those changes take effect only after the finish of current transfer (i.e., when CURR_TC becomes 0). On the other hand, any change made to other registers and/or fields takes immediate effect. Therefore, be careful in changing those registers and fields.

DMA REQUESET SELECTION REGISTER (DMAREQSEL)

Register	Address	R/W	Description	Reset Value
DMAREQSEL0	0x4B000024	R/W	DMA0 Request Selection Register	000
DMAREQSEL1	0x4B000124	R/W	DMA1 Request Selection Register	000
DMAREQSEL2	0x4B000224	R/W	DMA2 Request Selection Register	000
DMAREQSEL3	0x4B000324	R/W	DMA3 Request Selection Register	000
DMAREQSEL4	0x4B000424	R/W	DMA4 Request Selection Register	000
DMAREQSEL5	0x4B000524	R/W	DMA5 Request Selection Register	000

DMAREQSELn	Bit	Description	Initial State
HWSRCSEL	[5:1]	Select DMA request source for each DMA. → Refer to the Table 11-1 on page 11-2. This bits control the 8-1 MUX to select the DMA request source of each DMA. These bits have meanings if and only if H/W request mode is selected by DMAREQSELn[0].	00000
SWHW_SEL	[0]	Select the DMA source between software (S/W request mode) and hardware (H/W request mode). 0: S/W request mode is selected and DMA is triggered by setting SW_TRIG bit of DMASKTRIG control register. 1: DMA source selected by bit [5:1] is used to trigger the DMA operation.	0

NOTES

10 INTERRUPT CONTROLLER

OVERVIEW

The interrupt controller in the S3C2443X receives the request from 51 interrupt sources. These interrupt sources are provided by internal peripherals such as the DMA controller, the UART, IIC, and others. In these interrupt sources, the UARTn and EINTn interrupts are 'OR'ed to the interrupt controller.

When receiving multiple interrupt requests from internal peripherals and external interrupt request pins, the interrupt controller requests FIQ or IRQ interrupt of the ARM920T core after the arbitration procedure.

The arbitration procedure depends on the hardware priority logic and the result is written to the interrupt pending register, which helps users notify which interrupt is generated out of various interrupt sources.

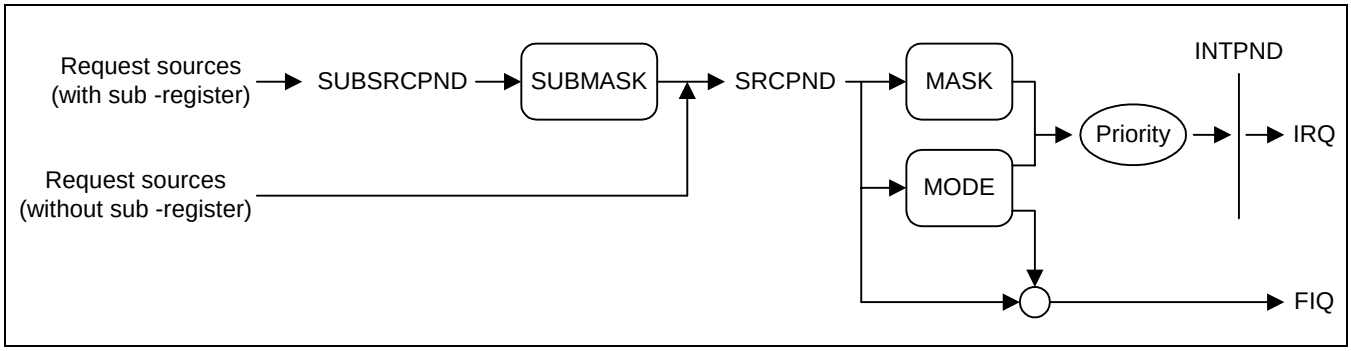


Figure 10-1. Interrupt Process Diagram

INTERRUPT CONTROLLER OPERATION

F-bit and I-bit of Program Status Register (PSR)

If the F-bit of PSR in ARM920T CPU is set to 1, the CPU does not accept the Fast Interrupt Request (FIQ) from the interrupt controller. Likewise, If I-bit of the PSR is set to 1, the CPU does not accept the Interrupt Request (IRQ) from the interrupt controller. So, the interrupt controller can receive interrupts by clearing F-bit or I-bit of the PSR to 0 and setting the corresponding bit of INTMSK to 0.

Interrupt Mode

The ARM920T has two types of Interrupt mode: FIQ or IRQ. All the interrupt sources determine which mode is used at interrupt request.

Interrupt Pending Register

The S3C2443X has two interrupt pending resisters: source pending register (SRCPND) and interrupt pending register (INTPND). These pending registers indicate whether or not an interrupt request is pending. When the interrupt sources request interrupt service, the corresponding bits of SRCPND register are set to 1, and at the same time, only one bit of the INTPND register is set to 1 automatically after arbitration procedure. If interrupts are masked, the corresponding bits of the SRCPND register are set to 1. This does not cause the bit of INTPND register changed. When a pending bit of the INTPND register is set, the interrupt service routine starts whenever the I-flag or F-flag is cleared to 0. The SRCPND and INTPND registers can be read and written, so the service routine must clear the pending condition by writing a 1 to the corresponding bit in the SRCPND register first and then clear the pending condition in the INTPND registers by using the same method.

Interrupt Mask Register

This register indicates that an interrupt has been disabled if the corresponding mask bit is set to 1. If an interrupt mask bit of INTMSK is 0, the interrupt will be serviced normally. If the corresponding mask bit is 1 and the interrupt is generated, the source pending bit will be set.

INTERRUPT SOURCES

The interrupt controller supports 51 interrupt sources as shown in the table below.

Sources	Descriptions	Arbiter Group
INT_ADC	ADC EOC and Touch interrupt (INT_ADC/INT_TC)	ARB5
INT_RTC	RTC alarm interrupt	ARB5
INT_SPI1	Low speed SPI interrupt	ARB5
INT_UART0	UART0 Interrupt (ERR, RXD, and TXD)	ARB5
INT_IIC	IIC interrupt	ARB4
INT_USBH	USB Host interrupt	ARB4
INT_USBD	USB Device interrupt	ARB4
INT_NAND	NAND Flash Controller interrupt	ARB4
INT_UART1	UART1 Interrupt (ERR, RXD, and TXD)	ARB4
INT_SPI0	High speed SPI interrupt	ARB4
INT_SDI_0	SDMMC interrupt	ARB 3
INT_SDI_1	High Speed SDMMC interrupt	ARB3
INT_CFCON	CFCON interrupt	ARB3
INT_UART3	UART3 Interrupt (ERR, RXD, and TXD)	ARB3
INT_DMA	DMA channel 6 interrupt(DMA0 ~ DMA5)	ARB3
INT_LCD	LCD interrupt(STN interrupt 1 + TFT interrupt 3)	ARB3
INT_UART2	UART2 Interrupt (ERR, RXD, and TXD)	ARB2
INT_TIMER4	Timer4 interrupt	ARB2
INT_TIMER3	Timer3 interrupt	ARB2
INT_TIMER2	Timer2 interrupt	ARB2
INT_TIMER1	Timer1 interrupt	ARB 2
INT_TIMER0	Timer0 interrupt	ARB2
INT_WDT_AC97	Watch-Dog / AC97 interrupt	ARB1
INT_TICK	RTC Time tick interrupt	ARB1
nBATT_FLT	Battery Fault interrupt	ARB1
INT_CAM	Camera Interface(INT_CAM_C, INT_CAM_P)	ARB1
EINT8_23	External interrupt 8 – 23	ARB1
EINT4_7	External interrupt 4 – 7	ARB1
EINT3	External interrupt 3	ARB0
EINT2	External interrupt 2	ARB0
EINT1	External interrupt 1	ARB0
EINT0	External interrupt 0	ARB0

INTERRUPT PRIORITY GENERATING BLOCK

The priority logic for 32 interrupt requests is composed of seven rotation based arbiters: six first-level arbiters and one second-level arbiter as shown in Figure 10-2 below.

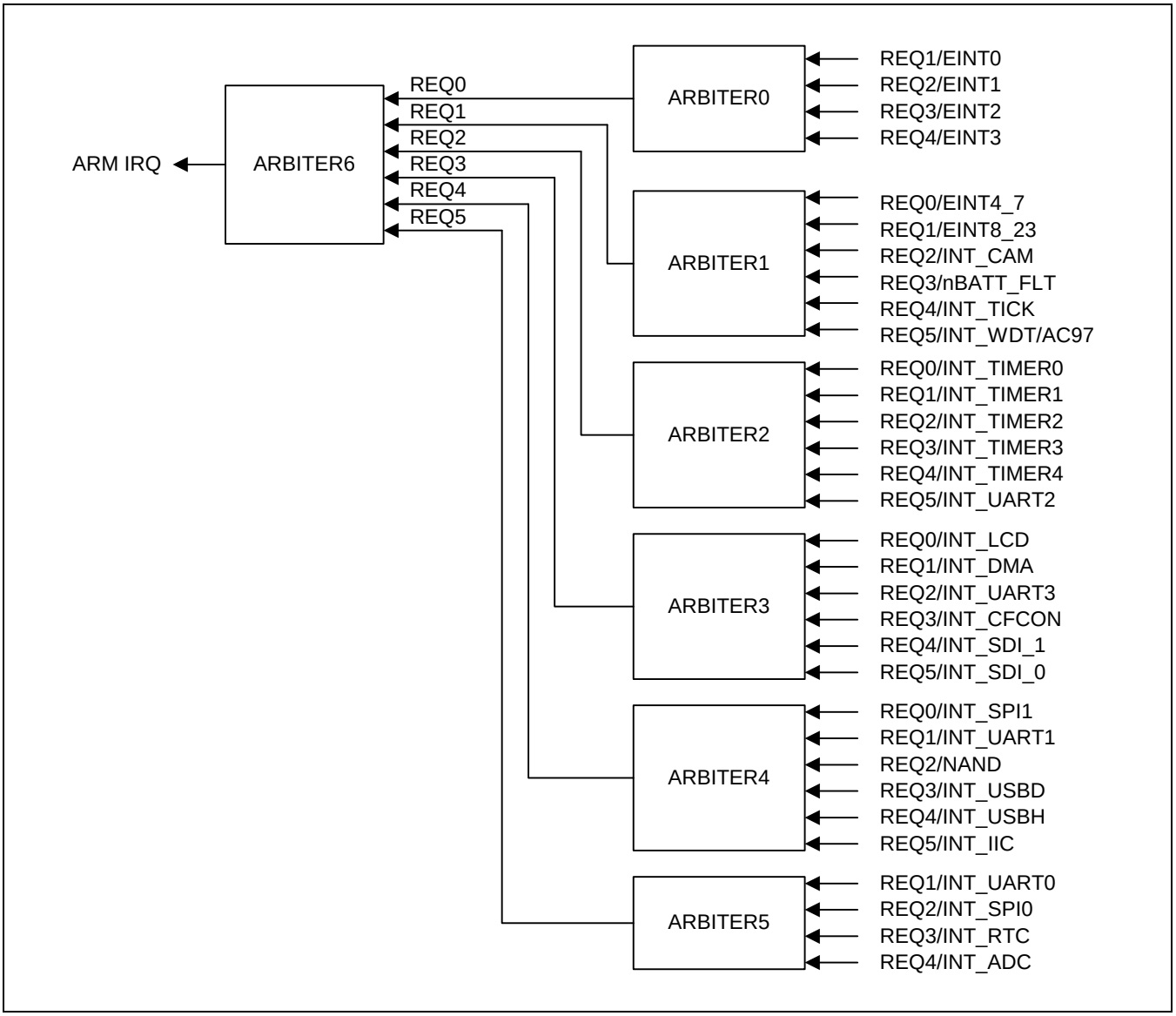


Figure 10-2. Priority Generating Block

INTERRUPT PRIORITY

Each arbiter can handle six interrupt requests based on the one bit arbiter mode control (ARB_MODE) and two bits of selection control signals (ARB_SEL) as follows:

— If ARB_SEL bits are 00b, the priority order is REQ0, REQ1, REQ2, REQ3, REQ4, and REQ5.

— If ARB_SEL bits are 01b, the priority order is REQ0, REQ2, REQ3, REQ4, REQ1, and REQ5.

— If ARB_SEL bits are 10b, the priority order is REQ0, REQ3, REQ4, REQ1, REQ2, and REQ5.

— If ARB_SEL bits are 11b, the priority order is REQ0, REQ4, REQ1, REQ2, REQ3, and REQ5.

Note that REQ0 of an arbiter always has the highest priority, and REQ5 has the lowest one. In addition, by changing the ARB_SEL bits, we can rotate the priority of REQ1 to REQ4.

Here, if ARB_MODE bit is set to 0, ARB_SEL bits are not automatically changed, making the arbiter to operate in the fixed priority mode (note that even in this mode, we can reconfigure the priority by manually changing the ARB_SEL bits). On the other hand, if ARB_MODE bit is 1, ARB_SEL bits are changed in rotation fashion, e.g., if REQ1 is serviced, ARB_SEL bits are changed to 01b automatically so as to put REQ1 into the lowest priority. The detailed rules of ARB_SEL change are as follows:

— If REQ0 or REQ5 is serviced, ARB_SEL bits are not changed at all.

— If REQ1 is serviced, ARB_SEL bits are changed to 01b.

— If REQ2 is serviced, ARB_SEL bits are changed to 10b.

— If REQ3 is serviced, ARB_SEL bits are changed to 11b.

— If REQ4 is serviced, ARB_SEL bits are changed to 00b.

INTERRUPT CONTROLLER SPECIAL REGISTERS

There are following control registers in the interrupt controller: source pending register, interrupt mode register, mask register, priority register, interrupt pending register, interrupt offset register, sub-source pending register and sub-mask register.

All the interrupt requests from the interrupt sources are first registered in the source pending register. They are divided into two groups including Fast Interrupt Request (FIQ) and Interrupt Request (IRQ), based on the interrupt mode register. The arbitration procedure for multiple IRQs is based on the priority register.

SOURCE PENDING (SRCPND) REGISTER

The SRCPND register is composed of 32 bits each of which is related to an interrupt source. Each bit is set to 1 if the corresponding interrupt source generates the interrupt request and waits for the interrupt to be serviced. Accordingly, this register indicates which interrupt source is waiting for the request to be serviced. Note that each bit of the SRCPND register is automatically set by the interrupt sources regardless of the masking bits in the INTMASK register. In addition, the SRCPND register is not affected by the priority logic of interrupt controller.

In the interrupt service routine for a specific interrupt source, the corresponding bit of the SRCPND register has to be cleared to get the interrupt request from the same source correctly. If you return from the ISR without clearing the bit, the interrupt controller operates as if another interrupt request came in from the same source. In other words, if a specific bit of the SRCPND register is set to 1, it is always considered as a valid interrupt request waiting to be serviced.

The time to clear the corresponding bit depends on the user's requirement. If you want to receive another valid request from the same source, you should clear the corresponding bit first, and then enable the interrupt.

You can clear a specific bit of the SRCPND register by writing a data to this register. It clears only the bit positions of the SRCPND corresponding to those set to one in the data. The bit positions corresponding to those that are set to 0 in the data remains as they are.

Register	Address	R/W	Description	Reset Value
SRCPND	0X4A000000	R/W	Indicate the interrupt request status. 0 = The interrupt has not been requested. 1 = The interrupt source has asserted the interrupt request.	0x00000000

SOURCE PENDING (SRCPND) REGISTER (Continued)

SRCPND	Bit	Description	Initial State
INT_ADC	[31]	0 = Not requested, 1 = Requested	0
INT_RTC	[30]	0 = Not requested, 1 = Requested	0
INT_SPI1	[29]	0 = Not requested, 1 = Requested	0
INT_UART0	[28]	0 = Not requested, 1 = Requested	0
INT_IIC	[27]	0 = Not requested, 1 = Requested	0
INT_USBH	[26]	0 = Not requested, 1 = Requested	0
INT_USBD	[25]	0 = Not requested, 1 = Requested	0
INT_NAND	[24]	0 = Not requested, 1 = Requested	0
INT_UART1	[23]	0 = Not requested, 1 = Requested	0
INT_SPI0	[22]	0 = Not requested, 1 = Requested	0
INT_SDI_0	[21]	0 = Not requested, 1 = Requested	0
INT_SDI_1	[20]	0 = Not requested, 1 = Requested	0
INT_CFCON	[19]	0 = Not requested, 1 = Requested	0
INT_UART3	[18]	0 = Not requested, 1 = Requested	0
INT_DMA	[17]	0 = Not requested, 1 = Requested	0
INT_LCD	[16]	0 = Not requested, 1 = Requested	0
INT_UART2	[15]	0 = Not requested, 1 = Requested	0
INT_TIMER4	[14]	0 = Not requested, 1 = Requested	0
INT_TIMER3	[13]	0 = Not requested, 1 = Requested	0
INT_TIMER2	[12]	0 = Not requested, 1 = Requested	0
INT_TIMER1	[11]	0 = Not requested, 1 = Requested	0
INT_TIMER0	[10]	0 = Not requested, 1 = Requested	0
INT_WDT/AC97	[9]	0 = Not requested, 1 = Requested	0
INT_TICK	[8]	0 = Not requested, 1 = Requested	0
nBATT_FLT	[7]	0 = Not requested, 1 = Requested	0
INT_CAM	[6]	0 = Not requested, 1 = Requested	0
EINT8_23	[5]	0 = Not requested, 1 = Requested	0
EINT4_7	[4]	0 = Not requested, 1 = Requested	0
EINT3	[3]	0 = Not requested, 1 = Requested	0
EINT2	[2]	0 = Not requested, 1 = Requested	0
EINT1	[1]	0 = Not requested, 1 = Requested	0
EINT0	[0]	0 = Not requested, 1 = Requested	0

INTERRUPT MODE (INTMOD) REGISTER

This register is composed of 32 bits each of which is related to an interrupt source. If a specific bit is set to 1, the corresponding interrupt is processed in the FIQ (fast interrupt) mode. Otherwise, it is processed in the IRQ mode (normal interrupt).

Note that only one interrupt source can be serviced in the FIQ mode in the interrupt controller (you should use the FIQ mode only for the urgent interrupt). Thus, only one bit of INTMOD can be set to 1.

Register	Address	R/W	Description	Reset Value
INTMOD	0X4A000004	R/W	Interrupt mode regiseter. 0 = IRQ mode 1 = FIQ mode	0x00000000

NOTE: If an interrupt mode is set to FIQ mode in the INTMOD register, FIQ interrupt will not affect both INTPND and INTOFFSET registers. In this case, the two registers are valid only for IRQ mode interrupt source.

INTMOD	Bit	Description	Initial State
INT_ADC	[31]	0 = IRQ, 1 = FIQ	0
INT_RTC	[30]	0 = IRQ, 1 = FIQ	0
INT_SPI1	[29]	0 = IRQ, 1 = FIQ	0
INT_UART0	[28]	0 = IRQ, 1 = FIQ	0
INT_IIC	[27]	0 = IRQ, 1 = FIQ	0
INT_USBH	[26]	0 = IRQ, 1 = FIQ	0
INT_USBD	[25]	0 = IRQ, 1 = FIQ	0
INT_NAND	[24]	0 = IRQ, 1 = FIQ	0
INT_UART1	[23]	0 = IRQ, 1 = FIQ	0
INT_SPI0	[22]	0 = IRQ, 1 = FIQ	0
INT_SDI_0	[21]	0 = IRQ, 1 = FIQ	0
INT_SDI_1	[20]	0 = IRQ, 1 = FIQ	0
INT_CFCON	[19]	0 = IRQ, 1 = FIQ	0
INT_UART3	[18]	0 = IRQ, 1 = FIQ	0
INT_DMA	[17]	0 = IRQ, 1 = FIQ	0
INT_LCD	[16]	0 = IRQ, 1 = FIQ	0
INT_UART2	[15]	0 = IRQ, 1 = FIQ	0
INT_TIMER4	[14]	0 = IRQ, 1 = FIQ	0
INT_TIMER3	[13]	0 = IRQ, 1 = FIQ	0
INT_TIMER2	[12]	0 = IRQ, 1 = FIQ	0
INT_TIMER1	[11]	0 = IRQ, 1 = FIQ	0
INT_TIMER0	[10]	0 = IRQ, 1 = FIQ	0
INT_WDT/AC97	[9]	0 = IRQ, 1 = FIQ	0
INT_TICK	[8]	0 = IRQ, 1 = FIQ	0
nBATT_FLT	[7]	0 = IRQ, 1 = FIQ	0
INT_CAM	[6]	0 = IRQ, 1 = FIQ	0
EINT8_23	[5]	0 = IRQ, 1 = FIQ	0
EINT4_7	[4]	0 = IRQ, 1 = FIQ	0
EINT3	[3]	0 = IRQ, 1 = FIQ	0
EINT2	[2]	0 = IRQ, 1 = FIQ	0
EINT1	[1]	0 = IRQ, 1 = FIQ	0
EINT0	[0]	0 = IRQ, 1 = FIQ	0

INTERRUPT MASK (INTMSK) REGISTER

This register also has 32 bits each of which is related to an interrupt source. If a specific bit is set to 1, the CPU does not service the interrupt request from the corresponding interrupt source (note that even in such a case, the corresponding bit of SRCPND register is set to 1). If the mask bit is 0, the interrupt request can be serviced.

Register	Address	R/W	Description	Reset Value
INTMSK	0X4A000008	R/W	Determine which interrupt source is masked. The masked interrupt source will not be serviced. 0 = Interrupt service is available. 1 = Interrupt service is masked.	0xFFFFFFFF

INTMSK	Bit	Description	Initial State
INT_ADC	[31]	0 = Service available, 1 = Masked	1
INT_RTC	[30]	0 = Service available, 1 = Masked	1
INT_SPI1	[29]	0 = Service available, 1 = Masked	1
INT_UART0	[28]	0 = Service available, 1 = Masked	1
INT_IIC	[27]	0 = Service available, 1 = Masked	1
INT_USBH	[26]	0 = Service available, 1 = Masked	1
INT_USBD	[25]	0 = Service available, 1 = Masked	1
INT_NAND	[24]	0 = Service available, 1 = Masked	1
INT_UART1	[23]	0 = Service available, 1 = Masked	1
INT_SPI0	[22]	0 = Service available, 1 = Masked	1
INT_SDI_0	[21]	0 = Service available, 1 = Masked	1
INT_SDI_1	[20]	0 = Service available, 1 = Masked	1
INT_CFCON	[19]	0 = Service available, 1 = Masked	1
INT_UART3	[18]	0 = Service available, 1 = Masked	1
INT_DMA	[17]	0 = Service available, 1 = Masked	1
INT_LCD	[16]	0 = Service available, 1 = Masked	1
INT_UART2	[15]	0 = Service available, 1 = Masked	1
INT_TIMER4	[14]	0 = Service available, 1 = Masked	1
INT_TIMER3	[13]	0 = Service available, 1 = Masked	1
INT_TIMER2	[12]	0 = Service available, 1 = Masked	1
INT_TIMER1	[11]	0 = Service available, 1 = Masked	1
INT_TIMER0	[10]	0 = Service available, 1 = Masked	1
INT_WDT/AC97	[9]	0 = Service available, 1 = Masked	1
INT_TICK	[8]	0 = Service available, 1 = Masked	1
nBATT_FLT	[7]	0 = Service available, 1 = Masked	1
INT_CAM	[6]	0 = Service available, 1 = Masked	1
EINT8_23	[5]	0 = Service available, 1 = Masked	1
EINT4_7	[4]	0 = Service available, 1 = Masked	1
EINT3	[3]	0 = Service available, 1 = Masked	1
EINT2	[2]	0 = Service available, 1 = Masked	1
EINT1	[1]	0 = Service available, 1 = Masked	1
EINT0	[0]	0 = Service available, 1 = Masked	1

PRIORITY REGISTER (PRIORITY)

Register	Address	R/W	Description	Reset Value
PRIORITY	0x4A00000C	R/W	IRQ priority control register	0x7F

PRIORITY	Bit	Description	Initial State
ARB_SEL6	[20:19]	Arbiter 6 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
ARB_SEL5	[18:17]	Arbiter 5 group priority order set 00 = REQ 1-2-3-4 01 = REQ 2-3-4-1 10 = REQ 3-4-1-2 11 = REQ 4-1-2-3	0
ARB_SEL4	[16:15]	Arbiter 4 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
ARB_SEL3	[14:13]	Arbiter 3 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
ARB_SEL2	[12:11]	Arbiter 2 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
ARB_SEL1	[10:9]	Arbiter 1 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
ARB_SEL0	[8:7]	Arbiter 0 group priority order set 00 = REQ 1-2-3-4 01 = REQ 2-3-4-1 10 = REQ 3-4-1-2 11 = REQ 4-1-2-3	0
ARB_MODE6	[6]	Arbiter 6 group priority rotate enable 0 = Priority does not rotate 1 = Priority rotate enable	1
ARB_MODE5	[5]	Arbiter 5 group priority rotate enable 0 = Priority does not rotate 1 = Priority rotate enable	1
ARB_MODE4	[4]	Arbiter 4 group priority rotate enable 0 = Priority does not rotate 1 = Priority rotate enable	1
ARB_MODE3	[3]	Arbiter 3 group priority rotate enable 0 = Priority does not rotate 1 = Priority rotate enable	1
ARB_MODE2	[2]	Arbiter 2 group priority rotate enable 0 = Priority does not rotate 1 = Priority rotate enable	1

PRIORITY REGISTER (PRIORITY) (Continued)

PRIORITY	Bit	Description	Initial State
ARB_MODE1	[1]	Arbiter 1 group priority rotate enable 0 = Priority does not rotate 1 = Priority rotate enable	1
ARB_MODE0	[0]	Arbiter 0 group priority rotate enable 0 = Priority does not rotate 1 = Priority rotate enable	1

INTERRUPT PENDING (INTPND) REGISTER

Each of the 32 bits in the interrupt pending register shows whether the corresponding interrupt request, which is unmasked and waits for the interrupt to be serviced, has the highest priority. Since the INTPND register is located after the priority logic, only one bit can be set to 1, and that interrupt request generates IRQ to CPU. In interrupt service routine for IRQ, you can read this register to determine which interrupt source is serviced among the 32 sources.

Like the SRCPND register, this register has to be cleared in the interrupt service routine after clearing the SRCPND register. We can clear a specific bit of the INTPND register by writing a data to this register. It clears only the bit positions of the INTPND register corresponding to those set to one in the data. The bit positions corresponding to those that are set to 0 in the data remains as they are.

Register	Address	R/W	Description	Reset Value
INTPND	0X4A000010	R/W	Indicate the interrupt request status. 0 = The interrupt has not been requested. 1 = The interrupt source has asserted the interrupt request.	0x00000000

NOTES:

1. If the FIQ mode interrupt occurs, the corresponding bit of INTPND will not be turned on as the INTPND register is available only for IRQ mode interrupt.
2. Cautions in clearing the INTPND register. The INTPND register is cleared to "0" by writing "1". If the INTPND bit, which has "1", is cleared by "0", the INTPND register & INTOFFSET register may have unexpected value in some case. So, you never write "0" on the INTPND bit having "1". The convenient method to clear the INTPND register is writing the INTPND register value on the INTPND register. (In even our example code, this guide hasn't been applied yet.)

INTPND	Bit	Description	Initial State
INT_ADC	[31]	0 = Not requested, 1 = Requested	0
INT_RTC	[30]	0 = Not requested, 1 = Requested	0
INT_SPI1	[29]	0 = Not requested, 1 = Requested	0
INT_UART0	[28]	0 = Not requested, 1 = Requested	0
INT_IIC	[27]	0 = Not requested, 1 = Requested	0
INT_USBH	[26]	0 = Not requested, 1 = Requested	0
INT_USBD	[25]	0 = Not requested, 1 = Requested	0
INT_NAND	[24]	0 = Not requested, 1 = Requested	0
INT_UART1	[23]	0 = Not requested, 1 = Requested	0
INT_SPI0	[22]	0 = Not requested, 1 = Requested	0
INT_SDI_0	[21]	0 = Not requested, 1 = Requested	0
INT_SDI_1	[20]	0 = Not requested, 1 = Requested	0
INT_CFCON	[19]	0 = Not requested, 1 = Requested	0
INT_UART3	[18]	0 = Not requested, 1 = Requested	0
INT_DMA	[17]	0 = Not requested, 1 = Requested	0
INT_LCD	[16]	0 = Not requested, 1 = Requested	0
INT_UART2	[15]	0 = Not requested, 1 = Requested	0
INT_TIMER4	[14]	0 = Not requested, 1 = Requested	0
INT_TIMER3	[13]	0 = Not requested, 1 = Requested	0
INT_TIMER2	[12]	0 = Not requested, 1 = Requested	0
INT_TIMER1	[11]	0 = Not requested, 1 = Requested	0
INT_TIMER0	[10]	0 = Not requested, 1 = Requested	0
INT_WDT/AC97	[9]	0 = Not requested, 1 = Requested	0
INT_TICK	[8]	0 = Not requested, 1 = Requested	0
nBATT_FLT	[7]	0 = Not requested, 1 = Requested	0
INT_CAM	[6]	0 = Not requested, 1 = Requested	0
EINT8_23	[5]	0 = Not requested, 1 = Requested	0
EINT4_7	[4]	0 = Not requested, 1 = Requested	0
EINT3	[3]	0 = Not requested, 1 = Requested	0
EINT2	[2]	0 = Not requested, 1 = Requested	0
EINT1	[1]	0 = Not requested, 1 = Requested	0
EINT0	[0]	0 = Not requested, 1 = Requested	0

INTERRUPT OFFSET (INTOFFSET) REGISTER

The value in the interrupt offset register shows, which interrupt request of IRQ mode is in the INTPND register. This bit can be cleared automatically by clearing SRCPND and INTPND.

Register	Address	R/W	Description	Reset Value
INTOFFSET	0X4A000014	R	Indicate the IRQ interrupt request source	0x00000000

INT Source	The OFFSET Value	INT Source	The OFFSET Value
INT_ADC	31	INT_UART2	15
INT_RTC	30	INT_TIMER4	14
INT_SPI1	29	INT_TIMER3	13
INT_UART0	28	INT_TIMER2	12
INT_IIC	27	INT_TIMER1	11
INT_USBH	26	INT_TIMER0	10
INT_USBD	25	INT_WDT/AC97	9
INT_NAND	24	INT_TICK	8
INT_UART1	23	nBATT_FLT	7
INT_SPI0	22	INT_CAM	6
INT_SDI_0	21	EINT8_23	5
INT_SDI_1	20	EINT4_7	4
INT_CFCON	19	EINT3	3
INT_UART3	18	EINT2	2
INT_DMA	17	EINT1	1
INT_LCD	16	EINT0	0

NOTE: FIQ mode interrupt does not affect the INTOFFSET register as the register is available only for IRQ mode interrupt.

SUB SOURCE PENDING (SUBSRCPND) REGISTER

You can clear a specific bit of the SUBSRCPND register by writing a data to this register. It clears only the bit positions of the SUBSRCPND register corresponding to those set to one in the data. The bit positions corresponding to those that are set to 0 in the data remains as they are.

Register	Address	R/W	Description	Reset Value
SUBSRCPND	0X4A000018	R/W	Indicate the interrupt request status. 0 = The interrupt has not been requested. 1 = The interrupt source has asserted the interrupt request.	0x00000000

SUBSRCPND	Bit	Description	SRCPND	Initial State
Reserved	[31:29]	Not used		0
SUBINT_AC97	[28]	0 = Not requested, 1 = Requested	INT_WDT_AC97	0
SUBINT_WDT	[27]	0 = Not requested, 1 = Requested		0
SUBINT_ERR3	[26]	0 = Not requested, 1 = Requested	INT_UART3	0
SUBINT_TXD3	[25]	0 = Not requested, 1 = Requested		0
SUBINT_RXD3	[24]	0 = Not requested, 1 = Requested		0
SUBINT_DMA5	[23]	0 = Not requested, 1 = Requested	INT_DMA	0
SUBINT_DMA4	[22]	0 = Not requested, 1 = Requested		0
SUBINT_DMA3	[21]	0 = Not requested, 1 = Requested		0
SUBINT_DMA2	[20]	0 = Not requested, 1 = Requested		0
SUBINT_DMA1	[19]	0 = Not requested, 1 = Requested		0
SUBINT_DMA0	[18]	0 = Not requested, 1 = Requested		0
SUBINT_LCD4 (TFT CPU I/F)	[17]	0 = Not requested, 1 = Requested	INT_LCD	0
SUBINT_LCD3 (TFT Frame)	[16]	0 = Not requested, 1 = Requested		0
SUBINT_LCD2 (TFT FIFO)	[15]	0 = Not requested, 1 = Requested		0
SUBINT_LCD1 (STN)	[14]	0 = Not requested, 1 = Requested		0
Reserved	[13]	Reserved for future usage	Reserved	0
SUBINT_CAM_P	[12]	0 = Not requested, 1 = Requested	INT_CAM	0
SUBINT_CAM_C	[11]	0 = Not requested, 1 = Requested		0
SUBINT_ADC	[10]	0 = Not requested, 1 = Requested	INT_ADC	0
SUBINT_TC	[9]	0 = Not requested, 1 = Requested		0
SUBINT_ERR2	[8]	0 = Not requested, 1 = Requested	INT_UART2	0
SUBINT_TXD2	[7]	0 = Not requested, 1 = Requested		0
SUBINT_RXD2	[6]	0 = Not requested, 1 = Requested		0
SUBINT_ERR1	[5]	0 = Not requested, 1 = Requested	INT_UART1	0
SUBINT_TXD1	[4]	0 = Not requested, 1 = Requested		0
SUBINT_RXD1	[3]	0 = Not requested, 1 = Requested		0
SUBINT_ERR0	[2]	0 = Not requested, 1 = Requested	INT_UART0	0
SUBINT_TXD0	[1]	0 = Not requested, 1 = Requested		0
SUBINT_RXD0	[0]	0 = Not requested, 1 = Requested		0

INTERRUPT SUB MASK (INTSUBMSK) REGISTER

This register has 27 bits each of which is related to an interrupt source. If a specific bit is set to 1, the interrupt request from the corresponding interrupt source is not serviced by the CPU (note that even in such a case, the corresponding bit of the SUBSRCPND register is set to 1). If the mask bit is 0, the interrupt request can be serviced.

Register	Address	R/W	Description	Reset Value
INTSUBMSK	0X4A00001C	R/W	Determine which interrupt source is masked. The masked interrupt source will not be serviced. 0 = Interrupt service is available. 1 = Interrupt service is masked.	0xFFFFFFFF

INTSUBMASK	Bit	Description	INTMASK	Initial State
Reserved	[31:29]	Not used		0
SUBINT_AC97	[28]	0 = Service available, 1 = Masked	INT_WDT_AC97	
SUBINT_WDT	[27]	0 = Service available, 1 = Masked		
SUBINT_ERR3	[26]	0 = Service available, 1 = Masked	INT_UART3	0
SUBINT_TXD3	[25]	0 = Service available, 1 = Masked		0
SUBINT_RXD3	[24]	0 = Service available, 1 = Masked		0
SUBINT_DMA5	[23]	0 = Service available, 1 = Masked	INT_DMA	0
SUBINT_DMA4	[22]	0 = Service available, 1 = Masked		0
SUBINT_DMA3	[21]	0 = Service available, 1 = Masked		0
SUBINT_DMA2	[20]	0 = Service available, 1 = Masked		0
SUBINT_DMA1	[19]	0 = Service available, 1 = Masked		0
SUBINT_DMA0	[18]	0 = Service available, 1 = Masked		0
SUBINT_LCD4 (TFT CPU I/F)	[17]	0 = Service available, 1 = Masked	INT_LCD	0
SUBINT_LCD3 (TFT Frame)	[16]	0 = Service available, 1 = Masked		0
SUBINT_LCD2 (TFT FIFO)	[15]	0 = Service available, 1 = Masked		0
SUBINT_LCD1 (STN)	[14]	0 = Service available, 1 = Masked		0
Reserved	[13]	Reserved for future usage	Reserved	0
SUBINT_CAM_P	[12]	0 = Service available, 1 = Masked	INT_CAM	0
SUBINT_CAM_C	[11]	0 = Service available, 1 = Masked		0
SUBINT_ADC	[10]	0 = Service available, 1 = Masked	INT_ADC	0
SUBINT_TC	[9]	0 = Service available, 1 = Masked		0
SUBINT_ERR2	[8]	0 = Service available, 1 = Masked	INT_UART2	0
SUBINT_TXD2	[7]	0 = Service available, 1 = Masked		0
SUBINT_RXD2	[6]	0 = Service available, 1 = Masked		0
SUBINT_ERR1	[5]	0 = Service available, 1 = Masked	INT_UART1	0
SUBINT_TXD1	[4]	0 = Service available, 1 = Masked		0
SUBINT_RXD1	[3]	0 = Service available, 1 = Masked		0
SUBINT_ERR0	[2]	0 = Service available, 1 = Masked	INT_UART0	0
SUBINT_TXD0	[1]	0 = Service available, 1 = Masked		0
SUBINT_RXD0	[0]	0 = Service available, 1 = Masked		0

11 I/O PORTS

OVERVIEW

S3C2443X has 147 multi-functional input/output port pins and there are 11 ports as shown below:

— Port A(GPA): 16-output port
— Port B(GPB): 11-input/output port
— Port C(GPC): 16-input/output port
— Port D(GPD): 16-input/output port
— Port E(GPE): 16-input/output port
— Port F(GPF): 8-input/output port
— Port G(GPG): 16-input/output port
— Port H(GPH): 15-input/output port
— Port J(GPJ): 16-input/output port
— Port L(GPL): 15-input/output port
— Port M(GPM): 2-input port

Each port can be easily configured by software to meet various system configurations and design requirements. You have to define which function of each pin is used before starting the main program. If a pin is not used for multiplexed functions, the pin can be configured as I/O ports.

Initial pin states are configured seamlessly to avoid problems.

S3C2443X PORT CONFIGURATION

Table 11-1. S3C2443X Port Configuration (Sheet 1 of 6)

Port A	Selectable Pin Functions			
GPA15	Output only	nWE_CF	–	–
GPA14	Output only	RSMAVD	–	–
GPA13	Output only	RSMCLK	–	–
GPA12	Output only	nRCS5	–	–
GPA11	Output only	nOE_CF	–	–
GPA10	RDATA_OEN	RADDR25	–	–
GPA9	Output only	RADDR24	–	–
GPA8	Output only	RADDR23	–	–
GPA7	Output only	RADDR22	–	–
GPA6	Output only	RADDR21	–	–
GPA5	Output only	RADDR20	–	–
GPA4	Output only	RADDR19	–	–
GPA3	Output only	RADDR18	–	–
GPA2	Output only	RADDR17	–	–
GPA1	Output only	RADDR16	–	–
GPA0	Output only	RADDR0	–	–

Table 11-1. S3C2443X Port Configuration (Sheet 2 of 6) (Continued)

Port B	Selectable Pin Functions			
GPB10	Input/output	nXDREQ0	XDREQ0	–
GPB9	Input/output	nXDACK0	XDACK0	–
GPB8	Input/output	nXDREQ1	XDREQ1	–
GPB7	Input/output	nXDACK1	XDACK1	–
GPB6	Input/output	nXBREQ	XBREQ	–
GPB5	Input/output	nXBACK	XBACK	–
GPB4	Input/output	TCLK	–	–
GPB3	Input/output	TOUT3	–	–
GPB2	Input/output	TOUT2	–	–
GPB1	Input/output	TOUT1	–	–
GPB0	Input/output	TOUT0	–	–

Port C	Selectable Pin Functions			
GPC15	Input/output	VD7	–	–
GPC14	Input/output	VD6	–	–
GPC13	Input/output	VD5	–	–
GPC12	Input/output	VD4	–	–
GPC11	Input/output	VD3	–	–
GPC10	Input/output	VD2	–	–
GPC9	Input/output	VD1	–	–
GPC8	Input/output	VD0	–	–
GPC7	Input/output	LCD_VF[2]	–	–
GPC6	Input/output	LCD_VF[1]	–	–
GPC5	Input/output	LCD_VF[0]	–	–
GPC4	Input/output	VM	–	–
GPC3	Input/output	VFRAME	–	–
GPC2	Input/output	VLINE	–	–
GPC1	Input/output	VCLK	–	–
GPC0	Input/output	LEND	–	–

Table 11-1. S3C2443X Port Configuration (Sheet 3 of 6) (Continued)

Port D	Selectable Pin Functions			
GPD15	Input/output	VD23	–	–
GPD14	Input/output	VD22	–	–
GPD13	Input/output	VD21	–	–
GPD12	Input/output	VD20	–	–
GPD11	Input/output	VD19	–	–
GPD10	Input/output	VD18	–	–
GPD9	Input/output	VD17	–	–
GPD8	Input/output	VD16		–
GPD7	Input/output	VD15	–	–
GPD6	Input/output	VD14	–	–
GPD5	Input/output	VD13	–	–
GPD4	Input/output	VD12	–	–
GPD3	Input/output	VD11	–	–
GPD2	Input/output	VD10	–	–
GPD1	Input/output	VD9	–	–
GPD0	Input/output	VD8	–	–

Port E	Selectable Pin Functions			
GPE15	Input/output	IICSDA	–	–
GPE14	Input/output	IICSCL	–	–
GPE13	Input/output	SPICLK0	–	–
GPE12	Input/output	SPIMOSI0	–	–
GPE11	Input/output	SPIMISO0	–	–
GPE10	Input/output	SD1_DAT3	–	–
GPE9	Input/output	SD1_DAT2	AC_nRESET	–
GPE8	Input/output	SD1_DAT1	AC_SYNC	–
GPE7	Input/output	SD1_DAT0	AC_SDO	–
GPE6	Input/output	SD1_CMD	AC_SDI	–
GPE5	Input/output	SD1_CLK	AC_BIT_CLK	–
GPE4	Input/output	I2SSDO	AC_SDO	–
GPE3	Input/output	I2SSDI	AC_SDI	–
GPE2	Input/output	CDCLK	AC_BIT_CLK	–
GPE1	Input/output	I2SSCLK	AC_SYNC	–
GPE0	Input/output	I2SLRCK	AC_nRESET	–

Table 11-1. S3C2443X Port Configuration (Sheet 4 of 6) (Continued)

Port F	Selectable Pin Functions			
GPF7	Input/output	EINT7	–	–
GPF6	Input/output	EINT6	–	–
GPF5	Input/output	EINT5	–	–
GPF4	Input/output	EINT4	–	–
GPF3	Input/output	EINT3	–	–
GPF2	Input/output	EINT2	–	–
GPF1	Input/output	EINT1	–	–
GPF0	Input/output	EINT0	–	–

Port G	Selectable Pin Functions			
GPG15	Input/output	EINT23	CARD_PWREN	–
GPG14	Input/output	EINT22	RESET_CF	–
GPG13	Input/output	EINT21	nREG_CF	–
GPG12	Input/output	EINT20	nINPACK	–
GPG11	Input/output	EINT19	nIREQ_CF	–
GPG10	Input/output	EINT18	–	–
GPG9	Input/output	EINT17	–	–
GPG8	Input/output	EINT16	–	–
GPG7	Input/output	EINT15	–	–
GPG6	Input/output	EINT14	–	–
GPG5	Input/output	EINT13	–	–
GPG4	Input/output	EINT12	LCD_PWREN	–
GPG3	Input/output	EINT11	–	–
GPG2	Input/output	EINT10	–	–
GPG1	Input/output	EINT9	–	–
GPG0	Input/output	EINT8	–	–

Table 11-1. S3C2443X Port Configuration (Sheet 5 of 6) (Continued)

Port H	Selectable Pin Functions			
GPH14	Input/output	CLKOUT1	–	–
GPH13	Input/output	CLKOUT0	–	–
GPH12	Input/output	EXTUARTCLK	–	–
GPH11	Input/output	nRTS1	–	–
GPH10	Input/output	nCTS1	–	–
GPH9	Input/output	nRTS0	–	–
GPH8	Input/output	nCTS0	–	–
GPH7	Input/output	RXD3	nCTS2	–
GPH6	Input/output	TXD3	nRTS2	–
GPH5	Input/output	RXD2	–	–
GPH4	Input/output	TXD2	–	–
GPH3	Input/output	RXD1	–	–
GPH2	Input/output	TXD1	–	–
GPH1	Input/output	RXD0	–	–
GPH0	Input/output	TXD0	–	–

Port J	Selectable Pin Functions			
GPJ15	Input/output	nSD0_WP	–	–
GPJ14	Input/output	nSD0_CD		
GPJ13	Input/output	SD0_LED		
GPJ12	Input/output	CAMRESET		
GPJ11	Input/output	CAMCLKOUT	–	–
GPJ10	Input/output	CAMHREF	–	–
GPJ9	Input/output	CAMVSYNC	–	–
GPJ8	Input/output	CAMPCLK	–	–
GPJ7	Input/output	CAMDATA7	–	–
GPJ6	Input/output	CAMDATA6	–	–
GPJ5	Input/output	CAMDATA5	–	–
GPJ4	Input/output	CAMDATA4	–	–
GPJ3	Input/output	CAMDATA3	–	–
GPJ2	Input/output	CAMDATA2	–	–
GPJ1	Input/output	CAMDATA1	–	–
GPJ0	Input/output	CAMDATA0	–	–

Table 11-1. S3C2443X Port Configuration (Sheet 6 of 6) (Continued)

Port L	Selectable Pin Functions			
GPL14	Input/output	SS1	–	–
GPL13	Input/output	SS0	–	–
GPL12	Input/output	SPIMISO1	–	–
GPL11	Input/output	SPIMOSI1	–	–
GPL10	Input/output	SPICLK1	–	–
GPL9	Input/output	SD0_CLK	–	–
GPL8	Input/output	SD0_CMD	–	–
GPL7	Input/output	SD0_DAT7	–	–
GPL6	Input/output	SD0_DAT6	–	–
GPL5	Input/output	SD0_DAT5	–	–
GPL4	Input/output	SD0_DAT4	–	–
GPL3	Input/output	SD0_DAT3	–	–
GPL2	Input/output	SD0_DAT2	–	–
GPL1	Input/output	SD0_DAT1	–	–
GPL0	Input/output	SD0_DAT0	–	–

Port M	Selectable Pin Functions			
GPM1	Input	FRnB	–	–
GPM0	Input	RSMBWAIT	–	–

PORT CONTROL DESCRIPTIONS

PORT CONFIGURATION REGISTER (GPACON-GPMCON)

In S3C2443X, most of the pins are multiplexed pins. So, It is determined which function is selected for each pins. The PnCON(port control register) determines which function is used for each pin.

If GPF0 – GPF7, GPG0 – GPG7 is used for the wakeup signal in power down mode, these ports must be configured in interrupt mode.

PORT DATA REGISTER (GPADAT-GPMDAT)

If ports are configured as output ports, data can be written to the corresponding bit of PnDAT. If Ports are configured as input ports, the data can be read from the corresponding bit of PnDAT.

PORT PULL-UP/DOWN REGISTER (GPBUDP-GPEUDP,GPGUDPH,GPHUDP,GPJUDP,GPLUDP,GPMUDP)

The port pull-up/down register controls the pull-up/down resister enable/disable of each port group. When the corresponding bit is 0, the pull-down resister of the pin is enabled. When 1, the pull-down resister is disabled.

If the port pull-down register is enabled then the pull-down resisters work without pin's functional setting(input, output, DATAn, EINTn and etc)

MISCELLANEOUS CONTROL REGISTER

This register controls mode selection, and CLKOUT selection.

EXTERNAL INTERRUPT CONTROL REGISTER

The 24 external interrupts are requested by various signaling methods. The EXTINT register configures the signaling method among the low level trigger, high level trigger, falling edge trigger, rising edge trigger, and both edge trigger for the external interrupt request Because each external interrupt pin has a digital filter, the interrupt controller can recognize the request signal that is longer than 3 clocks.

EINT[15:0] are used for wakeup sources.

I/O PORT CONTROL REGISTER

PORT A CONTROL REGISTERS (GPACDL, GPACDH)

Register*	Address	R/W	Description	Reset Value
GPACDL	0x56000000	R*/W	Configuration and data register for port A low	0xAAAA
GPACDH	0x56000004	R*/W	Configuration and data register for port A high	0x1AAAA
Reserved	0x56000008	–	Reserved	Undef
Reserved	0x5600000c	–	Reserved	Undef

GPACDL	Bit	Description	
GPA7	GPACDL[15]	0 = Output	1 = RADDR22
GPA7	GPACDL[14]	Data	
GPA6	GPACDL[13]	0 = Output	1 = RADDR21
GPA6	GPACDL[12]	Data	
GPA5	GPACDL[11]	0 = Output	1 = RADDR20
GPA5	GPACDL[10]	Data	
GPA4	GPACDL[9]	0 = Output	1 = RADDR19
GPA4	GPACDL[8]	Data	
GPA3	GPACDL[7]	0 = Output	1 = RADDR18
GPA3	GPACDL[6]	Data	
GPA2	GPACDL[5]	0 = Output	1 = RADDR17
GPA2	GPACDL[4]	Data	
GPA1	GPACDL[3]	0 = Output	1 = RADDR16
GPA1	GPACDL[2]	Data	
GPA0	GPACDL[1]	0 = Output	1 = RADDR0
GPA0	GPACDL[0]	Data	

NOTES:

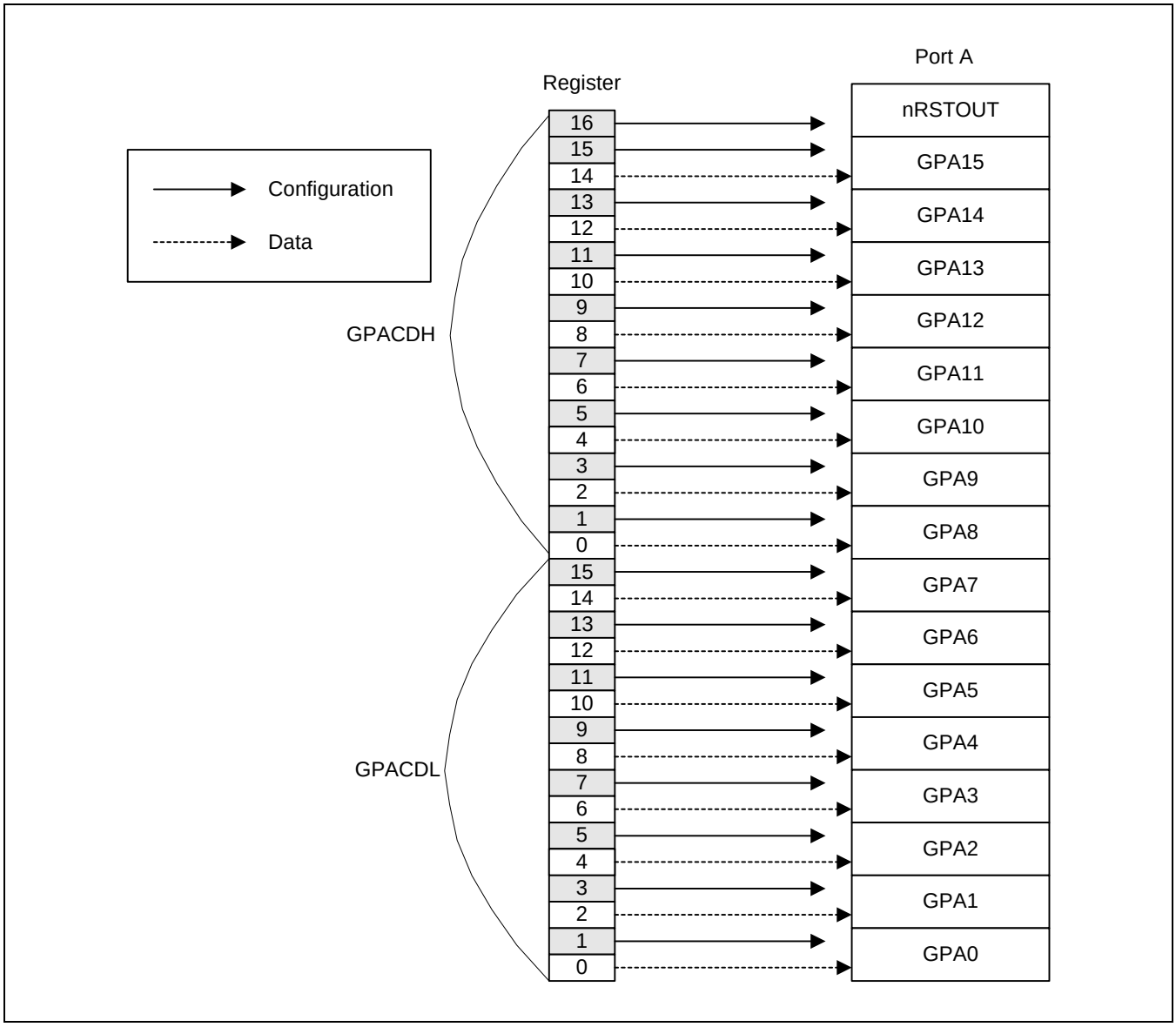
1. When the port is configured as output port, the pin state is the same as the corresponding bit.
   When the port is configured as functional pin, the undefined value will be read.
2. To read GPACDL, GPACDH extra function is necessary, Refer to ‘S3C2443 GUIDE TO EXTRA GPIO’

PORT A CONTROL/DATA REGISTERS (GPACDH)(Continued)

GPACDH	Bit	Description
nRSTOUT[note1]	GPACDH[16]	nRSTOUT Pin signal manual control, 0: nRSTOUT signal level will be low (‘0’). 1: nRSTOUT signal level will be the PRESET.
GPA15	GPACDH[15]	0 = Output 1 = nWE_CF
GPA15	GPACDH[14]	Data
GPA14	GPACDH[13]	0 = Output 1 = RSMAVD
GPA14	GPACDH[12]	Data
GPA13	GPACDH[11]	0 = Output 1 = RSMCLK
GPA13	GPACDH[10]	Data
GPA12	GPACDH[9]	0 = Output 1 = nRCS[5]
GPA12	GPACDH[8]	Data
GPA11	GPACDH[7]	0 = Output 1 = nOE_CF
GPA11	GPACDH[6]	Data
GPA10	GPACDH[5]	0 = RDATA_OEN 1 = RADDR25
GPA10	GPACDH[4]	Data
GPA9	GPACDH[3]	0 = Output 1 = RADDR24
GPA9	GPACDH[2]	Data
GPA8	GPACDH[1]	0 = Output 1 = RADDR23
GPA8	GPACDH[0]	Data

NOTE1: nRSTOUT = nRESET & S/W Reset & Watch dog Reset

GPACDL/GPACDH SETUP



PORT B CONTROL REGISTERS (GPBCON, GPBDAT, GPBUDP)

Register	Address	R/W	Description	Reset Value
GPBCON	0x56000010	R/W	Configures the pins of port B	0x0
GPBDAT	0x56000014	R/W	The data register for port B	Undef.
GPBUDP	0x56000018	R/W	Pull-up/down control register for port B	0x2AAAAA
Reserved	0x5600001c			

PBCON	Bit	Description
GPB10	[21:20]	00 = Input 01 = Output 10 = nXDREQ[0] 11 = XDREQ[0]
GPB9	[19:18]	00 = Input 01 = Output 10 = nXDACK[0] 11 = XDACK[0]
GPB8	[17:16]	00 = Input 01 = Output 10 = nXDREQ[1] 11 = XDREQ[1]
GPB7	[15:14]	00 = Input 01 = Output 10 = nXDACK[1] 11 = XDACK[1]
GPB6	[13:12]	00 = Input 01 = Output 10 = nXBREQ 11 = XBREQ
GPB5	[11:10]	00 = Input 01 = Output 10 = nXBACK 11 = XBACK
GPB4	[9:8]	00 = Input 01 = Output 10 = TCLK 11 = reserved
GPB3	[7:6]	00 = Input 01 = Output 10 = TOUT3 11 = reserved
GPB2	[5:4]	00 = Input 01 = Output 10 = TOUT2 11 = reserved]
GPB1	[3:2]	00 = Input 01 = Output 10 = TOUT1 11 = reserved
GPB0	[1:0]	00 = Input 01 = Output 10 = TOUT0 11 = reserved

PORT B CONTROL REGISTERS (GPBCON, GPBDAT, GPBUDP)(CONTINUED)

GPBDAT	Bit	Description
GPBDAT[10:0]	[10:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

GPBUDP	Bit	Description
GPB10	[21:20]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPB9	[19:18]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPB8	[17:16]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPB7	[15:14]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPB6	[13:12]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPB5	[11:10]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPB4	[9:8]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPB3	[7:6]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPB2	[5:4]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPB1	[3:2]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPB0	[1:0]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable

PORT C CONTROL REGISTERS (GPCCON, GPCDAT, GPCUDP)

Register	Address	R/W	Description	Reset Value
GPCCON	0x56000020	R/W	Configures the pins of port C	0x0
GPCDAT	0x56000024	R/W	The data register for port C	Undef.
GPCUDP	0x56000028	R/W	Pull-up/down control for port C	0xAAAAAAAA
Reserved	0x5600002c	–	–	–

GPCCON	Bit	Description
GPC15	[31:30]	00 = Input 01 = Output 10 = VD[7] 11 = Reserved
GPC14	[29:28]	00 = Input 01 = Output 10 = VD[6] 11 = Reserved
GPC13	[27:26]	00 = Input 01 = Output 10 = VD[5] 11 = Reserved
GPC12	[25:24]	00 = Input 01 = Output 10 = VD[4] 11 = Reserved
GPC11	[23:22]	00 = Input 01 = Output 10 = VD[3] 11 = Reserved
GPC10	[21:20]	00 = Input 01 = Output 10 = VD[2] 11 = Reserved
GPC9	[19:18]	00 = Input 01 = Output 10 = VD[1] 11 = Reserved
GPC8	[17:16]	00 = Input 01 = Output 10 = VD[0] 11 = Reserved
GPC7	[15:14]	00 = Input 01 = Output 10 = LCD_VF[2] 11 = Reserved
GPC6	[13:12]	00 = Input 01 = Output 10 = LCD_VF[1] 11 = Reserved
GPC5	[11:10]	00 = Input 01 = Output 10 = LCD_VF[0] 11 = Reserved
GPC4	[9:8]	00 = Input 01 = Output 10 = VM 11 = Reserved
GPC3	[7:6]	00 = Input 01 = Output 10 = VFRAME 11 = Reserved
GPC2	[5:4]	00 = Input 01 = Output 10 = VLINE 11 = Reserved
GPC1	[3:2]	00 = Input 01 = Output 10 = VCLK 11 = Reserved
GPC0	[1:0]	00 = Input 01 = Output 10 = LEND 11 = Reserved

PORT C CONTROL REGISTERS (GPCCON, GPCDAT, GPCUDP) (Continued)

GPCDAT	Bit	Description
GPC[15:0]	[15:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

GPCUDP	Bit	Description
GPC15	[31:30]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPC14	[29:28]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPC13	[27:26]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPC12	[25:24]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPC11	[23:22]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPC10	[21:20]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPC9	[19:18]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPC8	[17:16]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPC7	[15:14]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPC6	[13:12]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPC5	[11:10]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPC4	[9:8]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPC3	[7:6]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPC2	[5:4]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPC1	[3:2]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPC0	[1:0]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable

PORT D CONTROL REGISTERS (GPDCON, GPDDAT, GPDUDP)

Register	Address	R/W	Description	Reset Value
GPDCON	0x56000030	R/W	Configures the pins of port D	0x0
GPDDAT	0x56000034	R/W	The data register for port D	Undef.
GPDUDP	0x56000038	R/W	Pull-up/down control register for port D	0xA
Reserved	0x5600003c	–	–	–

GPDCON	Bit	Description
GPD15	[31:30]	00 = Input 01 = Output 10 = VD[23] 11 = Reserved
GPD14	[29:28]	00 = Input 01 = Output 10 = VD[22] 11 = Reserved
GPD13	[27:26]	00 = Input 01 = Output 10 = VD[21] 11 = Reserved
GPD12	[25:24]	00 = Input 01 = Output 10 = VD[20] 11 = Reserved
GPD11	[23:22]	00 = Input 01 = Output 10 = VD[19] 11 = Reserved
GPD10	[21:20]	00 = Input 01 = Output 10 = VD[18] 11 = Reserved
GPD9	[19:18]	00 = Input 01 = Output 10 = VD[17] 11 = Reserved
GPD8	[17:16]	00 = Input 01 = Output 10 = VD[16] 11 = Reserved
GPD7	[15:14]	00 = Input 01 = Output 10 = VD[15] 11 = Reserved
GPD6	[13:12]	00 = Input 01 = Output 10 = VD[14] 11 = Reserved
GPD5	[11:10]	00 = Input 01 = Output 10 = VD[13] 11 = Reserved
GPD4	[9:8]	00 = Input 01 = Output 10 = VD[12] 11 = Reserved
GPD3	[7:6]	00 = Input 01 = Output 10 = VD[11] 11 = Reserved
GPD2	[5:4]	00 = Input 01 = Output 10 = VD[10] 11 = Reserved
GPD1	[3:2]	00 = Input 01 = Output 10 = VD[9] 11 = Reserved
GPD0	[1:0]	00 = Input 01 = Output 10 = VD[8] 11 = Reserved

PORT D CONTROL REGISTERS (GPDCON, GPDDAT, GPDUDP) (Continued)

GPDDAT	Bit	Description
GPD[15:0]	[15:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

GPDUDP	Bit	Description
GPD15	[31:30]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPD14	[29:28]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPD13	[27:26]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPD12	[25:24]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPD11	[23:22]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPD10	[21:20]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPD9	[19:18]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPD8	[17:16]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPD7	[15:14]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPD6	[13:12]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPD5	[11:10]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPD4	[9:8]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPD3	[7:6]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPD2	[5:4]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPD1	[3:2]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPD0	[1:0]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable

PORT E CONTROL REGISTERS (GPECON, GPEDAT, GPEUDP)

Register	Address	R/W	Description	Reset Value
GPECON	0x56000040	R/W	Configures the pins of port E	0x0
GPEDAT	0x56000044	R/W	The data register for port E	Undef.
GPEUDP	0x56000048	R/W	Pull-up/down control register for port E	0xAAAAAAAA
Reserved	0x5600004c	–	–	–

GPECON	Bit	Description
GPE15	[31:30]	00 = Input 01 = Output 10 = IICSDA 11 = Reserved
GPE14	[29:28]	00 = Input 01 = Output 10 = IICSCL 11 = Reserved
GPE13	[27:26]	00 = Input 01 = Output 10 = SPICLK0 11 = Reserved
GPE12	[25:24]	00 = Input 01 = Output 10 = SPIMOSI0 11 = Reserved
GPE11	[23:22]	00 = Input 01 = Output 10 = SPIMISO0 11 = Reserved
GPE10	[21:20]	00 = Input 01 = Output 10 = SD1_DAT3 11 = Reserved
GPE9	[19:18]	00 = Input 01 = Output 10 = SD1_DAT2 11 = AC_nRESET
GPE8	[17:16]	00 = Input 01 = Output 10 = SD1_DAT1 11 = AC_SYNC
GPE7	[15:14]	00 = Input 01 = Output 10 = SD1_DAT0 11 = AC_SDO
GPE6	[13:12]	00 = Input 01 = Output 10 = SD1_CMD 11 = AC_SDI
GPE5	[11:10]	00 = Input 01 = Output 10 = SD1_CLK 11 = AC_BIT_CLK
GPE4	[9:8]	00 = Input 01 = Output 10 = I2SDO 11 = AC_SDO
GPE3	[7:6]	00 = Input 01 = Output 10 = I2SDI 11 = AC_SDI
GPE2	[5:4]	00 = Input 01 = Output 10 = CDCLK 11 = AC_BIT_CLK
GPE1	[3:2]	00 = Input 01 = Output 10 = I2SSCLK 11 = AC_SYNC
GPE0	[1:0]	00 = Input 01 = Output 10 = I2SLRCK 11 = AC_nRESET

PORT E CONTROL REGISTERS (GPECON, GPEDAT, GPEUDP) (Continued)

GPEDAT	Bit	Description
GPE[15:0]	[15:0]	When the port is configured as an input port, the corresponding bit is the pin state. When the port is configured as an output port, the pin state is the same as the corresponding bit. When the port is configured as a functional pin, the undefined value will be read.

GPEUDP	Bit	Description
GPE15	[31:30]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPE14	[29:28]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPE13	[27:26]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPE12	[25:24]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPE11	[23:22]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPE10	[21:20]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPE9	[19:18]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPE8	[17:16]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPE7	[15:14]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPE6	[13:12]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPE5	[11:10]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPE4	[9:8]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPE3	[7:6]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPE2	[5:4]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPE1	[3:2]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPE0	[1:0]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable

PORT F CONTROL REGISTERS (GPFCON, GPFDAT, GPFUDP)

If GPF0–GPF7 will be used for wake-up signals at power down mode, the ports will be set in interrupt mode.

Register	Address	R/W	Description	Reset Value
GPFCON	0x56000050	R/W	Configures the pins of port F	0x0
GPFDAT	0x56000054	R/W	The data register for port F	Undef.
Reserved	0x56000058	–	–	–
Reserved	0x5600005c	–	–	–

GPFCON	Bit	Description
GPF7	[15:14]	00 = Input 01 = Output 10 = EINT[7] 11 = Reserved
GPF6	[13:12]	00 = Input 01 = Output 10 = EINT[6] 11 = Reserved
GPF5	[11:10]	00 = Input 01 = Output 10 = EINT[5] 11 = Reserved
GPF4	[9:8]	00 = Input 01 = Output 10 = EINT[4] 11 = Reserved
GPF3	[7:6]	00 = Input 01 = Output 10 = EINT[3] 11 = Reserved
GPF2	[5:4]	00 = Input 01 = Output 10 = EINT2] 11 = Reserved
GPF1	[3:2]	00 = Input 01 = Output 10 = EINT[1] 11 = Reserved
GPF0	[1:0]	00 = Input 01 = Output 10 = EINT[0] 11 = Reserved

GPFDAT	Bit	Description
GPF[7:0]	[7:0]	When the port is configured as an input port, the corresponding bit is the pin state. When the port is configured as an output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

NOTE: For GPF[7:0] Pull-down enable control, refer to the register EXTINT0(0x56000088)

PORT G CONTROL REGISTERS (GPGCON, GPGDAT, GPGUDP)

If GPG0–GPG7 will be used for wake-up signals at Sleep mode, the ports will be set in interrupt mode.

Register	Address	R/W	Description	Reset Value
GPGCON	0x56000060	R/W	Configures the pins of port G	0x0
GPGDAT	0x56000064	R/W	The data register for port G	Undef.
GPGUDP	0x56000068	R/W	Pull-up/down control register for sub port G	0xAAAA****

GPGCON	Bit	Description
GPG15	[31:30]	00 = Input 01 = Output 10 = EINT[23] 11 = CARD_PWREN
GPG14	[29:28]	00 = Input 01 = Output 10 = EINT[22] 11 = RESET_CF
GPG13*	[27:26]	00 = Input 01 = Output 10 = EINT[21] 11 = nREG_CF
GPG12	[25:24]	00 = Input 01 = Output 10 = EINT[20] 11 = nINPACK
GPG11	[23:22]	00 = Input 01 = Output 10 = EINT[19] 11 = nIREQ_CF
GPG10	[21:20]	00 = Input 01 = Output 10 = EINT[18] 11 = Reserved
GPG9	[19:18]	00 = Input 01 = Output 10 = EINT[17] 11 = Reserved
GPG8	[17:16]	00 = Input 01 = Output 10 = EINT[16] 11 = Reserved
GPG7	[15:14]	00 = Input 01 = Output 10 = EINT[15] 11 = Reserved
GPG6	[13:12]	00 = Input 01 = Output 10 = EINT[14] 11 = Reserved
GPG5	[11:10]	00 = Input 01 = Output 10 = EINT[13] 11 = Reserved
GPG4	[9:8]	00 = Input 01 = Output 10 = EINT[12] 11 = LCD_PWRDN
GPG3	[7:6]	00 = Input 01 = Output 10 = EINT[11] 11 = Reserved
GPG2	[5:4]	00 = Input 01 = Output 10 = EINT[10] 11 = Reserved
GPG1	[3:2]	00 = Input 01 = Output 10 = EINT[9] 11 = Reserved
GPG0	[1:0]	00 = Input 01 = Output 10 = EINT[8] 11 = Reserved

PORT G CONTROL REGISTERS (GPGCON, GPGDAT, GPFUDP) (CONTINUED)

GPGDAT	Bit	Description
GPG[15:0]	[15:0]	When the port is configured as an input port, the corresponding bit is the pin state. When the port is configured as an output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

GPGUDP	Bit	Description
GPG15	[31:30]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPG14	[29:28]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPG13*	[27:26]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPG12	[25:24]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPG11	[23:22]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPG10	[21:20]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPG9	[19:18]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPG8	[17:16]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable

NOTE: For GPG[7:0] Pull-down enable control, refer to the register EXTINT1(0x5600008C)

PORT H CONTROL REGISTERS (GPHCON, GPHDAT, GPHUDP)

Register	Address	R/W	Description	Reset Value
GPHCON	0x56000070	R/W	Configures the pins of port H	0x0
GPHDAT	0x56000074	R/W	The data register for port H	Undef.
GPHUDP	0x56000078	R/W	pull-up/down control register for port H	0x2AAAAAAA
Reserved	0x5600007c	–	–	–

GPHCON	Bit	Description
GPH14	[29:28]	00 = Input 01 = Output 10 = CLKOUT1 11 = Reserved
GPH13	[27:26]	00 = Input 01 = Output 10 = CLKOUT0 11 = Reserved
GPH12	[25:24]	00 = Input 01 = Output 10 = EXTUARTCLK 11 = Reserved
GPH11	[23:22]	00 = Input 01 = Output 10 = nRTS1 11 = Reserved
GPH10	[21:20]	00 = Input 01 = Output 10 = nCTS1 11 = Reserved
GPH9	[19:18]	00 = Input 01 = Output 10 = nRTS0 11 = Reserved
GPH8	[17:16]	00 = Input 01 = Output 10 = nCTS0 11 = Reserved
GPH7	[15:14]	00 = Input 01 = Output 10 = RXD[3] 11 = nCTS2
GPH6	[13:12]	00 = Input 01 = Output 10 = TXD[3] 11 = nRTS2
GPH5	[11:10]	00 = Input 01 = Output 10 = RXD[2] 11 = Reserved
GPH4	[9:8]	00 = Input 01 = Output 10 = TXD[2] 11 = Reserved
GPH3	[7:6]	00 = Input 01 = Output 10 = RXD[1] 11 = reserved
GPH2	[5:4]	00 = Input 01 = Output 10 = TXD[1] 11 = Reserved
GPH1	[3:2]	00 = Input 01 = Output 10 = RXD[0] 11 = Reserved
GPH0	[1:0]	00 = Input 01 = Output 10 = TXD[0] 11 = Reserved

PORT H CONTROL REGISTERS (GPHCON, GPHDAT, GPHUDP)(Continued)

GPHDAT	Bit	Description
GPH[14:0]	[14:0]	When the port is configured as an input port, the corresponding bit is the pin state. When the port is configured as an output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

GPHUDP	Bit	Description
GPH14	[29:28]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPH13	[27:26]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPH12	[25:24]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPH11	[23:22]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPH10	[21:20]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPH9	[19:18]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPH8	[17:16]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPH7	[15:14]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPH6	[13:12]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPH5	[11:10]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPH4	[9:8]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPH3	[7:6]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPH2	[5:4]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPH1	[3:2]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPH0	[1:0]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable

PORT J CONTROL REGISTERS (GPJCON, GPJDAT, GPJUDP)

Register	Address	R/W	Description	Reset Value
GPJCON	0x560000d0	R/W	Configures the pins of port J	0x0
GPJDAT	0x560000d4	R/W	The data register for port J	Undef.
GPJUDP	0x560000d8	R/W	pull-up/down control register for port J	0xAAAAAAAA
Reserved	0x560000dc	–	–	–

GPJCON	Bit	Description
GPJ15	[31:30]	00 = Input 10 = nSD0_WP 01 = Output 11 = Reserved
GPJ14	[29:28]	00 = Input 10 = nSD0_CD 01 = Output 11 = Reserved
GPJ13	[27:26]	00 = Input 10 = SD0_LED 01 = Output 11 = Reserved
GPJ12	[25:24]	00 = Input 10 = CAMRESET 01 = Output 11 = Reserved
GPJ11	[23:22]	00 = Input 10 = CAMCLKOUT 01 = Output 11 = Reserved
GPJ10	[21:20]	00 = Input 10 = CAMHREF 01 = Output 11 = Reserved
GPJ9	[19:18]	00 = Input 10 = CAMVSYNC 01 = Output 11 = Reserved
GPJ8	[17:16]	00 = Input 10 = CAMPCLK 01 = Output 11 = Reserved
GPJ7	[15:14]	00 = Input 10 = CAMDATA[7] 01 = Output 11 = Reserved
GPJ6	[13:12]	00 = Input 10 = CAMDATA[6] 01 = Output 11 = Reserved
GPJ5	[11:10]	00 = Input 10 = CAMDATA[5] 01 = Output 11 = Reserved
GPJ4	[9:8]	00 = Input 10 = CAMDATA[4] 01 = Output 11 = Reserved
GPJ3	[7:6]	00 = Input 10 = CAMDATA[3] 01 = Output 11 = Reserved
GPJ2	[5:4]	00 = Input 10 = CAMDATA[2] 01 = Output 11 = Reserved
GPJ1	[3:2]	00 = Input 10 = CAMDATA[1] 01 = Output 11 = Reserved
GPJ0	[1:0]	00 = Input 10 = CAMDATA[0] 01 = Output 11 = Reserved

PORT J CONTROL REGISTERS (GPJCON, GPJDAT, GPJUDP) (Continued)

GPJDAT	Bit	Description
GPJ[15:0]	[15:0]	When the port is configured as an input port, the corresponding bit is the pin state. When the port is configured as an output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

GPJUDP	Bit	Description
GPJ15	[31:30]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPJ14	[29:28]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPJ13	[27:26]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPJ12	[25:24]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPJ11	[23:22]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPJ10	[21:20]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPJ9	[19:18]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPJ8	[17:16]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPJ7	[15:14]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPJ6	[13:12]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPJ5	[11:10]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPJ4	[9:8]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPJ3	[7:6]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPJ2	[5:4]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPJ1	[3:2]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPJ0	[1:0]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable

PORT L CONTROL REGISTERS (GPLCON, GPLDAT, GPLUDP)

Register	Address	R/W	Description	Reset Value
GPLCON	0x560000f0	R/W	Configures the pins of port L	0x0
GPLDAT	0x560000f4	R/W	The data register for port L	Undef.
GPLUDP	0x560000f8	R/W	pull-up/down control register for port L	0x2AAAAAAA
Reserved	0x560000fc	–	–	–

GPLCON	Bit	Description
GPL14	[29:28]	00 = Input 01 = Output 10 = SS1 11 = Reserved
GPL13	[27:26]	00 = Input 01 = Output 10 = SS0 11 = Reserved
GPL12	[25:24]	00 = Input 01 = Output 10 = SPIMISO1 11 = Reserved
GPL11	[23:22]	00 = Input 01 = Output 10 = SPIMOSI1 11 = Reserved
GPL10	[21:20]	00 = Input 01 = Output 10 = SPICLK1 11 = Reserved
GPL9	[19:18]	00 = Input 01 = Output 10 = SD0_CLK 11 = Reserved
GPL8	[17:16]	00 = Input 01 = Output 10 = SD0_CMD 11 = Reserved
GPL7	[15:14]	00 = Input 01 = Output 10 = SD0_DAT7 11 = Reserved
GPL6	[13:12]	00 = Input 01 = Output 10 = SD0_DAT6 11 = Reserved
GPL5	[11:10]	00 = Input 01 = Output 10 = SD0_DAT5 11 = Reserved
GPL4	[9:8]	00 = Input 01 = Output 10 = SD0_DAT4 11 = Reserved
GPL3	[7:6]	00 = Input 01 = Output 10 = SD0_DAT3 11 = Reserved
GPL2	[5:4]	00 = Input 01 = Output 10 = SD0_DAT2 11 = Reserved
GPL1	[3:2]	00 = Input 01 = Output 10 = SD0_DAT1 11 = Reserved
GPL0	[1:0]	00 = Input 01 = Output 10 = SD0_DAT0 11 = Reserved

PORT L CONTROL REGISTERS (GPLCON, GPLDAT, GPLPUD) (Continued)

GPLDAT	Bit	Description
GPL[14:0]	[14:0]	When the port is configured as an input port, the corresponding bit is the pin state. When the port is configured as an output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

GPLUDP	Bit	Description
GPL14	[29:28]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPL13	[27:26]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPL12	[25:24]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPL11	[23:22]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPL10	[21:20]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPL9	[19:18]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPL8	[17:16]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPL7	[15:14]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPL6	[13:12]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPL5	[11:10]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPL4	[9:8]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPL3	[7:6]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPL2	[5:4]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPL1	[3:2]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPL0	[1:0]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable

PORT M CONTROL REGISTERS (GPMCON, GPMDAT, GPMUDP)

Register	Address	R/W	Description	Reset Value
GPMCON	0x56000100	R/W	Configures the pins of port M	0xA
GPMDAT	0x56000104	R	The data register for port M	Undef.
GPMUDP	0x560000108	R/W	pull-up/down control register for port M	0x15
Reserved	0x56000010c	–	–	–

GPMCON	Bit	Description
GPM1	[3:2]	Others = GPM Input 10 = FRnB
GPM0	[1:0]	Others = GPM Input 10 = RSMBWAIT

GPMDAT	Bit	Description
GPM[1:0]	[1:0]	When the port is configured as an input port, the corresponding bit is the pin state When the port is configured as functional pin, the undefined value will be read.

GPMUDP	Bit	Description
nWAIT	[5:4]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPM1	[3:2]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable
GPM0	[1:0]	00 : pull-up function, 10 : pull-down function , 01,11 : pull-up/down disable

NOTE: GPMUDP is in Sleep Area. At Sleep Wake Up, GPMUDP is reset.

MISCELLANEOUS CONTROL REGISTER (MISCCR)

In Sleep mode, the data bus(SD[15:0] or RD[15:0] can be set as Hi-Z and Output '0' state. But, because of the characteristics of IO pad, the data bus pull-up/down resisters have to be turned on or off to reduce the power consumption. SD[15:0] or RD[15:0] pin pull-up/down resisters can be controlled by MISCCR register.

Pads related USB are controlled by this register for USB host, or for USB device.

Register	Address	R/W	Description	Reset Value
MISCCR	0x56000080	R/W	Miscellaneous control register	0x40010020

MISCCR	Bit	Description	Reset Value
HSSPI_EN2	[31]	Must be set '1'	0
nCD_CF	[30]	nCD_CF Signal Register 0 : card detected 1 : card not detected	1
LCD_SEL	[28]	Display Type Select (0:LCD / 1:FIMD)	0
Reserved	[27:25]	Reserved	0
FLT_I2C	[24]	Clocked Noise Filter Enable for IIC	0
Reserved	[23][18:16][13]	Reserved	0
SEL_SUSPND	[12]	USB Port Suspend mode 0 = Normal mode 1 = Suspend mode	0
CLKSEL1 *	[10:8]	Select source clock with CLKOUT1 pad 000 = RESERVED 001 = Gated EPLL output 010 = RTC clock output 011 = HCLK 100 = PCLK 101 = DCLK1(Divided PCLK) 11x = reserved	000
CLKSEL0 *	[6:4]	Select source clock with CLKOUT0 pad 000 = MPLL INPUT Clock(XTAL) 001 = EPLL output 010 = FCLK(ARMCLK) 011 = HCLK 100 = PCLK 101 = DCLK0 (Divided PCLK) 110 = OSC To PLL INPUT Clock 111 = reserved	010
Reserved	[3:0]	Reserved	0

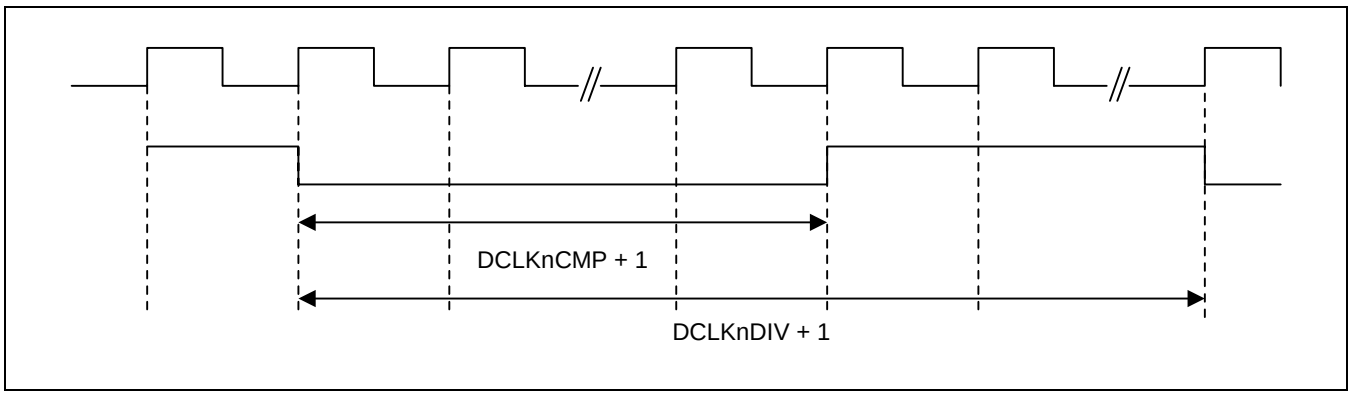
NOTE1: User must set first rMISCCR[31] = 1b1 when use the high speed SPI.

NOTE: We recommend not using this output pad to other device's pll clock source.

DCLK CONTROL REGISTERS (DCLKCON)

Register	Address	R/W	Description	Reset Value
DCLKCON	0x56000084	R/W	DCLK0/1 control register	0x0

DCLKCON	Bit	Description
DCLK1CMP	[27:24]	DCLK1 compare value clock toggle value. (< DCLK1DIV) If the DCLK1CMP is n, Low level duration is(n + 1), High level duration is((DCLK1DIV + 1) –(n +1))
DCLK1DIV	[23:20]	DCLK1 divide value DCLK1 frequency = source clock /(DCLK1DIV + 1)
DCLK1SelCK	[17]	Select DCLK1 source clock 0 = PCLK 1 = EPLL
DCLK1EN	[16]	DCLK1 enable 0 = DCLK1 disable 1 = DCLK1 enable
DCLK0CMP	[11:8]	DCLK0 compare value clock toggle value.(< DCLK0DIV) If the DCLK0CMP is n, Low level duration is(n + 1), High level duration is((DCLK0DIV + 1) –(n +1))
DCLK0DIV	[7:4]	DCLK0 divide value. DCLK0 frequency = source clock /(DCLK0DIV + 1)
DCLK0SelCK	[1]	Select DCLK0 source clock 0 = PCLK 1 = EPLL
DCLK0EN	[0]	DCLK0 enable 0 = DCLK0 disable 1 = DCLK0 enable



EXTINTN (EXTERNAL INTERRUPT CONTROL REGISTER N)

The 8 external interrupts can be requested by various signaling methods. The EXTINT register configures the signaling method between the level trigger and edge trigger for the external interrupt request, and also configures the signal polarity.

To recognize the level interrupt, the valid logic level on EXTINTn pin must be retained for 40ns at least because of the noise filter.

Register	Address	R/W	Description	Reset Value
EXTINT0	0x56000088	R*/W	External interrupt control register 0	0x000000
EXTINT1	0x5600008c	R*/W	External interrupt control register 1	0x000000
EXTINT2	0x56000090	R*/W	External interrupt control register 2	0x000000

EXTINT0	Bit	Description
EINT7/GPF[7]	[31]	Pull-Down Enable Control, 0=Enable, 1=Disable
EINT7	[30:28]	Setting the signaling method of the EINT7. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT6/GPF[6]	[27]	Pull-Down Enable Control, 0=Enable, 1=Disable
EINT6	[26:24]	Setting the signaling method of the EINT6. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT5/GPF[5]	[23]	Pull-Down Enable Control, 0=Enable, 1=Disable
EINT5	[22:20]	Setting the signaling method of the EINT5. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT4/GPF[4]	[19]	Pull-Down Enable Control, 0=Enable, 1=Disable
EINT4	[18:16]	Setting the signaling method of the EINT4. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT3/GPF[3]	[15]	Pull-Down Enable Control, 0=Enable, 1=Disable
EINT3	[14:12]	Setting the signaling method of the EINT3. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT2/GPF[2]	[11]	Pull-Down Enable Control, 0=Enable, 1=Disable
EINT2	[10:8]	Setting the signaling method of the EINT2. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT1/GPF[1]	[7]	Pull-Down Enable Control, 0=Enable, 1=Disable
EINT1	[6:4]	Setting the signaling method of the EINT1. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT0/GPF[0]	[3]	Pull-Down Enable Control, 0=Enable, 1=Disable
EINT0	[2:0]	Setting the signaling method of the EINT0. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered

EXTINTN (EXTERNAL INTERRUPT CONTROL REGISTER N) (CONTINUED)

EXTINT1	Bit	Description
EINT15/GPG[7]	[31]	Pull-Down Enable Control, 0 = Enable 1 = Disable
EINT15	[30:28]	Setting the signaling method of the EINT15. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT14/GPG[6]	[27]	Pull-Down Enable Control, 0 = Enable 1 = Disable
EINT14	[26:24]	Setting the signaling method of the EINT14. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT13/GPG[5]	[23]	Pull-Down Enable Control, 0 = Enable 1 = Disable
EINT13	[22:20]	Setting the signaling method of the EINT13. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT12/GPG[4]	[19]	Pull-Down Enable Control, 0 = Enable 1 = Disable
EINT12	[18:16]	Setting the signaling method of the EINT12. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT11/GPG[3]	[15]	Pull-Down Enable Control, 0 = Enable 1 = Disable
EINT11	[14:12]	Setting the signaling method of the EINT11. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT10/GPG[2]	[11]	Pull-Down Enable Control, 0 = Enable 1 = Disable
EINT10	[10:8]	Setting the signaling method of the EINT10. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT9/GPG[1]	[7]	Pull-Down Enable Control, 0 = Enable 1 = Disable
EINT9	[6:4]	Setting the signaling method of the EINT9. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT8/GPG[0]	[3]	Pull-Down Enable Control, 0 = Enable 1 = Disable
EINT8	[2:0]	Setting the signaling method of the EINT8. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered

EXTINTN (EXTERNAL INTERRUPT CONTROL REGISTER N) (Continued)

EXTINT2	Bit	Description	Reset Value
FLTEN23	[31]	Filter enable for EINT23 0 = Filter Disable 1= Filter Enable	0
EINT23	[30:28]	Setting the signaling method of the EINT23. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered	000
FLTEN22	[27]	Filter Enable for EINT22 0 = Filter Disable 1= Filter Enable	0
EINT22	[26:24]	Setting the signaling method of the EINT22. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered	000
FLTEN21	[23]	Filter Enable for EINT21 0 = Filter Disable 1= Filter Enable	0
EINT21	[22:20]	Setting the signaling method of the EINT21. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered	000
FLTEN20	[19]	Filter Enable for EINT20 0 = Filter Disable 1= Filter Enable	0
EINT20	[18:16]	Setting the signaling method of the EINT20. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered	000
FLTEN19	[15]	Filter enable for EINT19 0 = Filter Disable 1= Filter Enable	0
EINT19	[14:12]	Setting the signaling method of the EINT19. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered	000
FLTEN18	[11]	Filter enable for EINT18 0 = Filter Disable 1= Filter Enable	0
EINT18	[10:8]	Setting the signaling method of the EINT18. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered	000

EXTINTN (EXTERNAL INTERRUPT CONTROL REGISTER N) (Continued)

EXTINT2	Bit	Description	Reset Value
FLTEN17	[7]	Filter enable for EINT17 0 = Filter Disable 1= Filter Enable	0
EINT17	[6:4]	Setting the signaling method of the EINT17. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered	000
FLTEN16	[3]	Filter enable for EINT16 0 = Filter Disable 1= Filter Enable	0
EINT16	[2:0]	Setting the signaling method of the EINT16. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered	000

NOTE: To read EXTINT0, EXTINT1, EXTINT2 extra function is necessary, Refer to ‘S3C2443 GUIDE TO EXTRA GPIO’

EINTFLTN (EXTERNAL INTERRUPT FILTER REGISTER N)

To recognize the level interrupt, the valid logic level on EXTINTn pin must be retained for 40ns at least because of the noise filter.

Register	Address	R/W	Description	Reset Value
EINTFLT0	0x56000094	R/W	Reserved	0x000000
EINTFLT1	0x56000098	R/W	Reserved	0x000000
EINTFLT2	0x5600009c	R*/W	External interrupt control register 2	0x000000
EINTFLT3	0x560000a0	R*/W	External interrupt control register 3	0x000000

EINTFLT2	Bit	Description
FLTCLK19	[31]	Filter clock of EINT19 (configured by OM) 0 = PCLK 1= EXTCLK/OSC_CLK
EINTFLT19	[30:24]	Filtering width of EINT19
FLTCLK18	[23]	Filter clock of EINT18 (configured by OM) 0 = PCLK 1= EXTCLK/OSC_CLK
EINTFLT18	[22:16]	Filtering width of EINT18
FLTCLK17	[15]	Filter clock of EINT17 (configured by OM) 0 = PCLK 1= EXTCLK/OSC_CLK
EINTFLT17	[14:8]	Filtering width of EINT17
FLTCLK16	[7]	Filter clock of EINT16 (configured by OM) 0 = PCLK 1= EXTCLK/OSC_CLK
EINTFLT16	[6:0]	Filtering width of EINT16

EINTFLT3	Bit	Description
FLTCLK23	[31]	Filter clock of EINT23 (configured by OM) 0 = PCLK 1= EXTCLK/OSC_CLK
EINTFLT23	[30:24]	Filtering width of EINT23
FLTCLK22	[23]	Filter clock of EINT22 (configured by OM) 0 = PCLK 1= EXTCLK/OSC_CLK
EINTFLT22	[22:16]	Filtering width of EINT22
FLTCLK21	[15]	Filter clock of EINT21(configured by OM) 0 = PCLK 1= EXTCLK/OSC_CLK
EINTFLT21	[14:8]	Filtering width of EINT21
FLTCLK20	[7]	Filter clock of EINT20 (configured by OM) 0 = PCLK 1= EXTCLK/OSC_CLK
EINTFLT20	[6:0]	Filtering width of EINT20

NOTE: To read EINTFLT2, EINTFLT3 extra function is necessary, Refer to ‘S3C2443 GUIDE TO EXTRA GPIO’

EINTMASK (EXTERNAL INTERRUPT MASK REGISTER)

Register	Address	R/W	Description	Reset Value
EINTMASK	0x560000a4	R/W	External interrupt mask register	0x000fffff

EINTMASK	Bit	Description
EINT23	[23]	0 = enable interrupt 1= masked
EINT22	[22]	0 = enable interrupt 1= masked
EINT21	[21]	0 = enable interrupt 1= masked
EINT20	[20]	0 = enable interrupt 1= masked
EINT19	[19]	0 = enable interrupt 1= masked
EINT18	[18]	0 = enable interrupt 1= masked
EINT17	[17]	0 = enable interrupt 1= masked
EINT16	[16]	0 = enable interrupt 1= masked
EINT15	[15]	0 = enable interrupt 1= masked
EINT14	[14]	0 = enable interrupt 1= masked
EINT13	[13]	0 = enable interrupt 1= masked
EINT12	[12]	0 = enable interrupt 1= masked
EINT11	[11]	0 = enable interrupt 1= masked
EINT10	[10]	0 = enable interrupt 1= masked
EINT9	[9]	0 = enable interrupt 1= masked
EINT8	[8]	0 = enable interrupt 1= masked
EINT7	[7]	0 = enable interrupt 1= masked
EINT6	[6]	0 = enable interrupt 1= masked
EINT5	[5]	0 = enable interrupt 1= masked
EINT4	[4]	0 = enable interrupt 1= masked
Reserved	[3:0]	Reserved

EINTPEND (EXTERNAL INTERRUPT PENDING REGISTER)

Register	Address	R/W	Description	Reset Value
EINTPEND	0x560000a8	R/W	External interrupt pending register	0x00

EINTPEND	Bit	Description	Reset Value
EINT23	[23]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT22	[22]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT21	[21]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT20	[20]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT19	[19]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT18	[18]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT17	[17]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT16	[16]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT15	[15]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT14	[14]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT13	[13]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT12	[12]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT11	[11]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT10	[10]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT9	[9]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT8	[8]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT7	[7]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT6	[6]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT5	[5]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
EINT4	[4]	It is cleared by writing '1' 0 = Not occur 1 = Occur interrupt	0
Reserved	[3:0]	Reserved	0000

GSTATUSN (GENERAL STATUS REGISTERS)

Register	Address	R/W	Description	Reset Value
GSTATUS0	0x560000ac	R	External pin status	Not define
GSTATUS1	0x560000b0	R	Chip ID	0x32443001

GSTATUS0	Bit	Description
nWAIT	[3]	Status of nWAIT pin
NCON	[2]	Status of NCON pin
RnB	[1]	Status of RnB pin
BATT_FLT	[0]	Status of BATT_FLT pin

GSTATUS1	Bit	Description
CHIP ID	[0]	ID register = 0x32443001

DSCN (DRIVER STRENGTH CONTROL)

Control the Memory I/O Driver strength

Register	Address	R/W	Description	Reset Value
DSC0	0x560000c0	R/W	Strength control register 0	0x0
DSC1	0x560000c4	R/W	Strength control register 1	0x0
DSC2	0x560000c8	R/W	Strength control register 2	0x0

DSC0	Bit	Description	Reset Value
nEN_DSC	[31]	Enable Driver Strength Control 0: enable 1: Disable	0
Reserved	[30]	–	0
PUD_CF	[29:28]	nWE_CF, nOE_CF Driver strength 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_nRBE	[27:26]	nRBE, nROE, nRWE Driver strength 00: 12mA 10: 10mA 01: 8mA 11: 6mA	
DSC_nROE	[25:24]		
DSC_nRWE	[23:22]		
DSC_nRCS5	[21:20]	nRCS5 ~ nRCS0 Address Bus Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	
DSC_nRCS4	[19:18]		
DSC_nRCS3	[17:16]		
DSC_nRCS2	[15:14]		
DSC_nRCS1	[13:12]		
DSC_nRCS0	[11:10]		00
DSC_RADDRH	[9:8]	ROM Address Bus[25:16] Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_RADDRL	[7:6]	ROM Address Bus[15:1] Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_RADDR0	[5:4]	ROM Address Bus[0] Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_RDATA1	[3:2]	ROM DATA[15:8] I/O Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_RDATA0	[1:0]	ROM DATA[7:0] I/O Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00

DSCN (DRIVER STRENGTH CONTROL)

DSC1	Bit	Description	Reset Value
DSC_nSCLK	[27:26]	nSCLK Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_SCLK	[25:24]	SCLK Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_SCKE	[23:22]	SCKE Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_nSOE	[21:20]	nSOE Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_nSWE	[19:18]	nSWE Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_nSCAS	[17:16]	nSCAS Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_nSRAS	[15:14]	nSRAS Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_nSCS1	[13:12]	nSCS1 Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_nSCS0	[11:10]	nSCS0 Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_SADDR	[9:8]	SADDR Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_SDATA3	[7:6]	SDATA[31:24] Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_SDATA2	[5:4]	SDATA[23:16] Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_SDATA1	[3:2]	SDATA[15:8] Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_SDATA0	[1:0]	SDATA[7:0] Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00

DSCN (DRIVER STRENGTH CONTROL)

DSC2	Bit	Description	Reset Value
DSC_nFCE	[27:26]	nFCE Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_nFRE	[25:24]	nFRE Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_nFWE	[23:22]	nFWE Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_ALE	[21:20]	ALE Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_CLE	[19:18]	CLE Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_RSMAVD	[15:14]	RSMAVD Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_RSMCLK	[13:12]	RSMCLK Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_DQM3	[11:10]	DQM3 Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_DQM2	[9:8]	DQM2 Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_DQM1	[7:6]	DQM1 Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_DQM0	[5:4]	DQM0 Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_DQS1	[3:2]	DQS1 Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00
DSC_DQS0	[1:0]	DQS0 Driver strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00

MSLCON (MEMORY SLEEP CONTROL REGISTER)

Select memory interface status when in SLEEP mode.

Register	Address	R/W	Description	Reset Value
MSLCON	0x560000cc	R/W	Memory I/F HiZ control register	0x0

MSLCON	Bit	Description	Reset Value
EN_PSCREG	[31]	Memory I/F HiZ control register enable at Normal mode	0
	[30]		
HizMemSel	[29:28]	High Z Memory Selection. Memory I/F High Z Out Control according to nXBREQ & nXBACK. 01 : ROM/NF/CF MEM I/F Selection 10 : SDRAM MEM I/F Selection	0
PSC_nSCLK	[27]	nSCLK pin status . 0: Inactive('1') 1: Hi-Z	0
PSC_SCK	[26]	SCLK,SCKE pin status. 0: Inactive('0') 1: Hi-Z	0
PSC_DQM	[25]	DQM[3:0] pin status, DQM[3:0]='0x3' 0: Inactive('0011') 1: Hi-Z	0
PSC_DQS	[24]	DQS[1:0] pin status. 0: Inactive('0') 1: Hi-Z	0
Reserved	[23]	–	0
PSC_nSWE	[22]	nSWE pin status. 0: Inactive('1') 1: Hi-Z	0
PSC_SDR	[21]	nSCAS, nSRAS pin status. 0: Inactive('1') 1: Hi-Z	0
PSC_nSCS1	[20]	nSCS1 pin status. 0: Inactive('1') 1: Hi-Z	0
PSC_nSCS0	[19]	nSCS0 pin status. 0: Inactive('1') 1: Hi-Z	0
PSC_SDATAH	[18]	SDATA[31:16] pin status. 0: Input 1: Hi-Z	0
PSC_SDATAL	[17]	SDATA[15:0] pin status. 0: Input 1: Hi-Z	0
PSC_SADDR	[16]	SADDR[15:0] pin status. 0: The last address, read or written 1: Hi-Z	0
Reserved	[15:12]	–	
PSC_NF1	[11]	nFCE, nFRE, nFWE pin status. 0: Inactive('1') 1: Hi-Z	0
PSC_NF0	[10]	ALE, CLE pin status. 0: Inactive('0') 1: Hi-Z	0

MSLCON	Bit	Description	Reset Value
PSC_nRWE	[9]	nRWE pin status. 0: Inactive(‘1’) 1: Hi-Z	0
PSC_nROE	[8]	nROE pin status 0: Inactive(‘1’) 1: Hi-Z	0
PSC_RSM	[7]	RSMCLK, RSMAVD pin status. 0: Inactive(‘0’) 1: Hi-Z	0
PSC_nRBE	[6]	nRBE0, 1 pin status. 0: Inactive(‘1’) 1: Hi-Z	0
PSC_nRCS51	[5]	nRCS5, 4, 3, 2, 1 pin status. 0: Inactive(‘1’) 1: Hi-Z	0
PSC_nRCS0	[4]	nRCS0 pin status. 0: Inactive(‘1’) 1: Hi-Z	0
PSC_RDATA	[3]	RADDR[15:0] pin status. 0: Inactive(‘0’) 1: Hi-Z	0
PSC_RADDRH	[2]	RADDR[25:16] pin status. 0: Inactive(‘0’) 1: Hi-Z	0
PSC_RADDRL	[1]	RADDR[15:1] pin status. 0: Inactive(‘0’) 1: Hi-Z	0
PSC_RADDR0	[0]	RADDR[0]] pin status. 0: Inactive(‘0’) 1: Hi-Z	0

SDATA / RDATA PULL-DOWN CONTROL REGISTERS (DATAPDEN)

Register	Address	R/W	Description	Reset Value
DATAPDEN	0x560000e8	R/W	pull-down control register for port S/RDATA	0x3F

DATAPDEN	Bit	Description
DATAPDEN0	[0]	RDATA[15:0] pull-down enable control. (1:disable, 0:enable)
DATAPDEN1	[1]	SDATA[15:0] pull-down enable control. (1:disable, 0:enable)
DATAPDEN2	[2]	SDATA[31:16] pull-down enable control. (1:disable, 0:enable)
DATAPDEN3	[3]	DQS[1:0] pull-down enable control. (1:disable, 0:enable)
DATAPDEN4	[4]	SCLK pull-down enable control. (1:disable, 0:enable)
DATAPDEN5	[5]	SCKE pull-down enable control. (1:disable, 0:enable)

GPIO Alive & Sleep Part

	Alive	Sleep
PAD	GPF[7:0](EINT[7:0]), GPG[7:0](EINT[15:8])	GPB, GPC, GPD, GPE, GPG[15:8](EINT[23:17]), GPH, GPJ, GPL, GPM
SFR	GPFCON[15;0], GPFDAT[7:0] GPGCON[15:0], GPGDAT[7:0] EXTINT0[31:0], EXINT1[31:0] GPACDL[15:0], GPACDH[15:0]	All registers except alive SFR GP*CON, GP*DAT, GP*UDP

NOTES

12 WATCHDOG TIMER

OVERVIEW

The S3C2443X watchdog timer is used to resume the controller operation whenever it is disturbed by malfunctions such as noise and system errors. It can be used as a normal 16-bit interval timer to request interrupt service. The watchdog timer generates the reset signal for 128 PCLK cycles.

FEATURES

- Normal interval timer mode with interrupt request
- Internal reset signal is activated for 128 PCLK cycles when the timer count value reaches 0 (time-out).

WATCHDOG TIMER OPERATION

BLOCK DIAGRAM

Figure 12-1 shows the functional block diagram of the watchdog timer. The watchdog timer uses only PCLK as its source clock. The PCLK frequency is prescaled to generate the corresponding watchdog timer clock, and the resulting frequency is divided again.

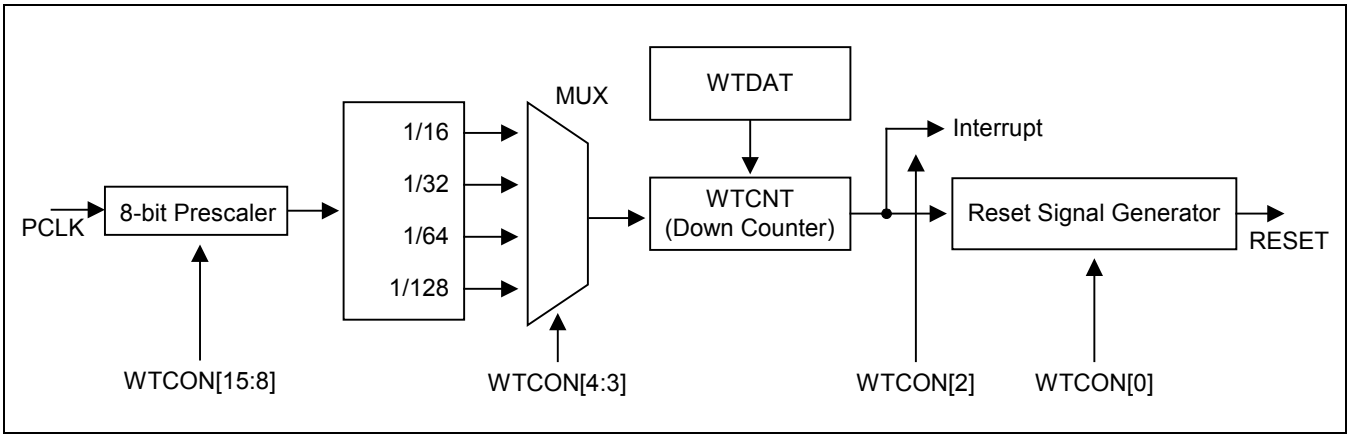


Figure 12-1. Watchdog Timer Block Diagram

The prescaler value and the frequency division factor are specified in the watchdog timer control (WTCON) register. Valid prescaler values range from 0 to 28-1. The frequency division factor can be selected as 16, 32, 64, or 128.

Use the following equation to calculate the watchdog timer clock frequency and the duration of each timer clock cycle:

t_watchdog = 1 / [PCLK / (Prescaler value + 1) / Division_factor]

WTDAT & WTCNT

Once the watchdog timer is enabled, the value of watchdog timer data (WTDAT) register cannot be automatically reloaded into the timer counter (WTCNT). In this reason, an initial value must be written to the watchdog timer count (WTCNT) register, before the watchdog timer starts.

CONSIDERATION OF DEBUGGING ENVIRONMENT

When the S3C2443X is in debug mode using Embedded ICE, the watchdog timer must not operate.

The watchdog timer can determine whether or not it is currently in the debug mode from the CPU core signal (DBGACK signal). Once the DBGACK signal in CPU core is asserted, the reset output of the watchdog timer is not activated as the watchdog timer is expired.

WATCHDOG TIMER SPECIAL REGISTERS

WATCHDOG TIMER CONTROL (WTCON) REGISTER

The WTCON register allows the user to enable/disable the watchdog timer, select the clock signal from 4 different sources, enable/disable interrupts, and enable/disable the watchdog timer output. The Watchdog timer is used to resume the S3C2443X restart on malfunction after its power on; if controller restart is not desired, the Watchdog timer should be disabled.

If the user wants to use the normal timer provided by the Watchdog timer, enable the interrupt and disable the Watchdog timer.

Register	Address	R/W	Description	Reset Value
WTCON	0x53000000	R/W	Watchdog timer control register	0x8021

WTCON	Bit	Description	Initial State
Prescaler value	[15:8]	Prescaler value. The valid range is from 0 to 255(28-1).	0x80
Reserved	[7:6]	Reserved. These two bits must be 00 in normal operation.	00
Watchdog timer	[5]	Enable or disable bit of Watchdog timer. 0 = Disable 1 = Enable	1
Clock select	[4:3]	Determine the clock division factor. 00: 16 01: 32 10: 64 11: 128	00
Interrupt generation	[2]	Enable or disable bit of the interrupt. 0 = Disable 1 = Enable	0
Reserved	[1]	Reserved. This bit must be 0 in normal operation.	0
Reset enable/disable	[0]	Enable or disable bit of Watchdog timer output for reset signal. 1: Assert reset signal of the S3C2443X at watchdog time-out 0: Disable the reset function of the watchdog timer.	1

WATCHDOG TIMER DATA (WTDAT) REGISTER

The WTDAT register is used to specify the time-out duration. The content of WTDAT cannot be automatically loaded into the timer counter at initial watchdog timer operation. However, using 0x8000 (initial value) will drive the first time-out. In this case, the value of WTDAT will be automatically reloaded into WTCNT.

Register	Address	R/W	Description	Reset Value
WTDAT	0x53000004	R/W	Watchdog timer data register	0x8000

WTDAT	Bit	Description	Initial State
Count reload value	[15:0]	Watchdog timer count value for reload.	0x8000

WATCHDOG TIMER COUNT (WTCNT) REGISTER

The WTCNT register contains the current count values for the watchdog timer during normal operation. Note that the content of the WTDAT register cannot be automatically loaded into the timer count register when the watchdog timer is enabled initially, so the WTCNT register must be set to an initial value before enabling it.

Register	Address	R/W	Description	Reset Value
WTCNT	0x53000008	R/W	Watchdog timer count register	0x8000

WTCNT	Bit	Description	Initial State
Count value	[15:0]	The current count value of the watchdog timer	0x8000

13 PWM TIMER

OVERVIEW

The S3C2443X has five 16-bit timers. Timer 0, 1, 2, and 3 have Pulse Width Modulation (PWM) function. Timer 4 has an internal timer only with no output pins. The timer 0 has a dead-zone generator, which is used with a large current device.

The timer 0 and 1 share an 8-bit prescaler, while the timer 2, 3 and 4 share other 8-bit prescaler. Each timer has a clock divider, which generates 5 different divided signals (1/2, 1/4, 1/8, 1/16, and TCLK). Each timer block receives its own clock signals from the clock divider, which receives the clock from the corresponding 8-bit prescaler. The 8-bit prescaler is programmable and divides the PCLK according to the loading value, which is stored in TCFG0 and TCFG1 registers.

The timer count buffer register (TCNTBn) has an initial value, which is loaded into the internal down-counter when the timer is enabled. The timer compare buffer register (TCMPBn) has an initial value, which is loaded into the internal compare register to be compared with the internal down-counter value. This double buffering feature of TCNTBn and TCMPBn makes the timer generate a stable output when the frequency and duty ratio are changed.

Each timer has its own 16-bit internal down counter, which is driven by the timer clock. When the internal down-counter reaches zero, the timer interrupt request is generated to inform the CPU that the timer operation has been completed. When the timer internal down-counter reaches zero, the value of corresponding TCNTBn is automatically loaded into the internal down-counter to continue the next operation. However, if the timer stops, for example, by clearing the timer enable bit of TCONn during the timer running mode, the value of TCNTBn will not be reloaded into the internal down-counter.

The value of TCMPBn is used for pulse width modulation (PWM). The timer control logic changes the output level when the internal down-counter value matches the value of the internal compare register in the timer control logic. Therefore, the internal compare register determines the turn-on time (or turn-off time) of a PWM output.

FEATURE

— Five 16-bit timers
— Two 8-bit prescalers & Two 4-bit divider
— Programmable duty control of output waveform (PWM)
— Auto reload mode or one-shot pulse mode
— Dead-zone generator

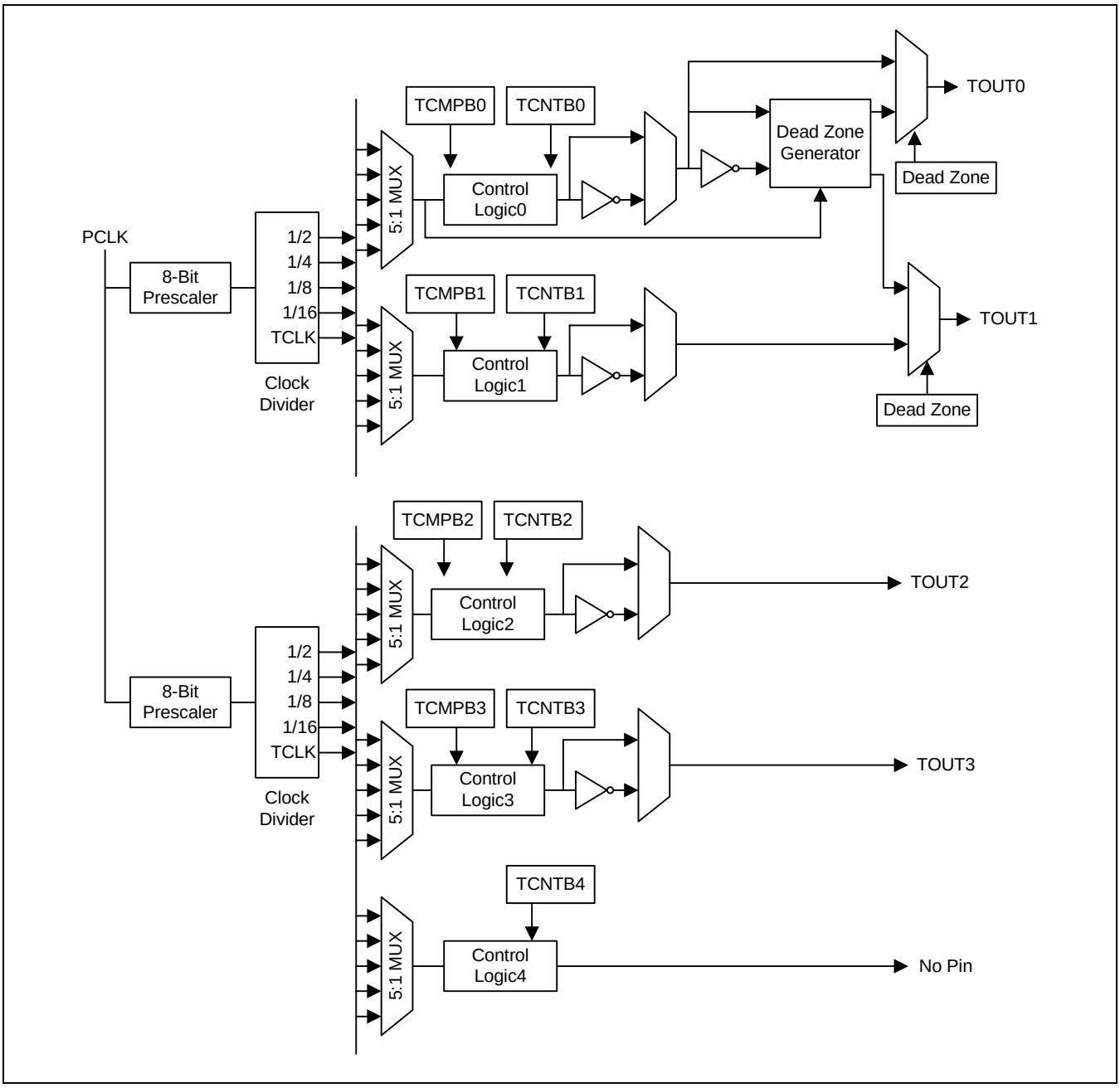


Figure 13-1. 16-bit PWM Timer Block Diagram

PWM TIMER OPERATION

PRESCALER & DIVIDER

An 8-bit prescaler and a 4-bit divider make the following output frequencies:

4-bit Divider Settings	Minimum Resolution (prescaler = 0)	Maximum Resolution (prescaler = 255)	Min. Interval (TCNTBn = 1)	Max. Interval (TCNTBn = 65535)
1/2 (PCLK = 50 MHz)	0.0400 us (25.000 MHz)	10.2400 us (97.6562 kHz)	0.0800 us	0.6710 sec
1/4 (PCLK = 50 MHz)	0.0800 us (12.500 MHz)	20.4800 us (48.8281 kHz)	0.1600 us	1.3421 sec
1/8 (PCLK = 50 MHz)	0.1600 us (6.250 MHz)	40.9601 us (24.4140 kHz)	0.3200 us	2.6843 sec
1/16 (PCLK = 50 MHz)	0.3200 us (3.125 MHz)	81.9188 us (12.2070 kHz)	0.6400 us	5.3686 sec

BASIC TIMER OPERATION

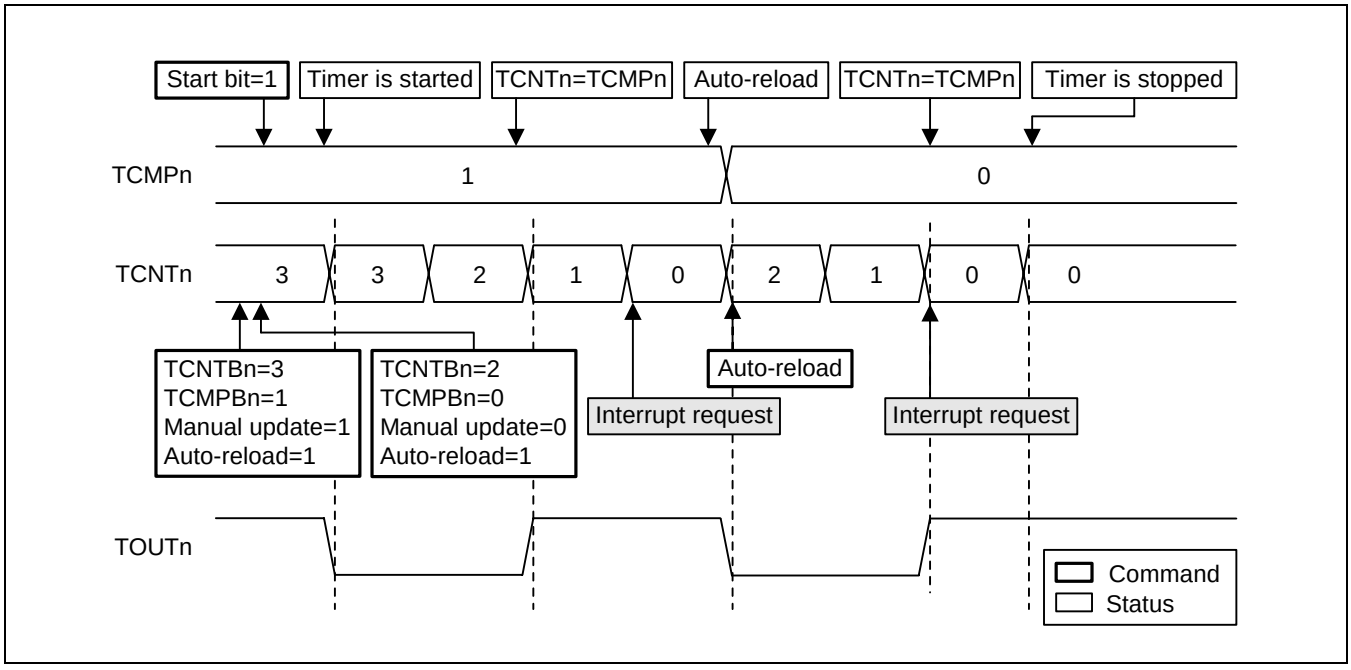


Figure 13-2. Timer Operations

A timer (except the timer ch-5) has TCNTBn, TCNTn, TCMPBn and TCMPn. The TCNTBn and the TCMPBn are loaded into the TCNTn and the TCMPn when the timer reaches 0. When the TCNTn reaches 0, an interrupt request will occur if the interrupt is enabled.

NOTE:

TCNTn and TCMPn are the names of the internal registers. (16bit Internal down-counter (register) and 16bit internal compare register, respectively.) The TCNTn register can be read from the TCNTOn register

AUTO RELOAD & DOUBLE BUFFERING

S3C2443X PWM Timers have a double buffering function, enabling the reload value changed for the next timer operation without stopping the current timer operation. So, although the new timer value is set, a current timer operation is completed successfully.

The timer value can be written into Timer Count Buffer register (TCNTBn) and the current counter value of the timer can be read from Timer Count Observation register (TCNTOn). If the TCNTBn is read, the read value does not indicate the current state of the counter but the reload value for the next timer duration.

The auto-reload operation copies the TCNTBn into TCNTn when the TCNTn reaches 0. The value, written into the TCNTBn, is loaded to the TCNTn only when the TCNTn reaches 0 and auto reload is enabled. If the TCNTn becomes 0 and the auto reload bit is 0, the TCNTn does not operate any further.

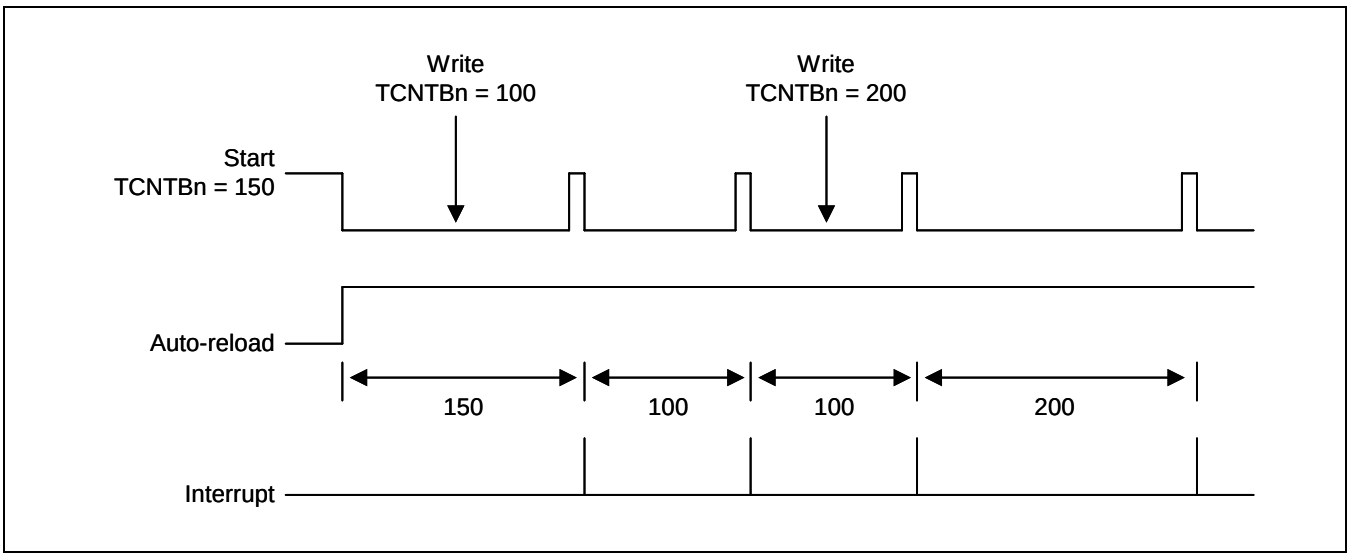


Figure 13-3. Example of Double Buffering Function

TIMER INITIALIZATION USING MANUAL UPDATE BIT AND INVERTER BIT

An auto reload operation of the timer occurs when the internal down-counter(TCNTn) reaches 0. So, a starting value of the TCNTn has to be defined by the user in advance. In this case, the starting value has to be loaded by the manual update bit. The following steps describe how to start a timer:

1) Write the initial value into TCNTBn and TCMPBn.
2) Set the manual update bit of the corresponding timer. It is recommended that you configure the inverter on/off bit. (Whether use inverter or not).
3) Set start bit of the corresponding timer to start the timer (and clear the manual update bit, configure the inverter on/off bit as you want).

If the timer is stopped by force, the TCNTn retains the counter value and is not reloaded from TCNTBn. If a new value has to be set, perform manual update.

NOTE:

Whenever TOUT inverter on/off bit is changed, the TOUTn logic value will also be changed whether the timer runs. Therefore, it is desirable that the inverter on/off bit is configured with the manual update bit.

TIMER OPERATION

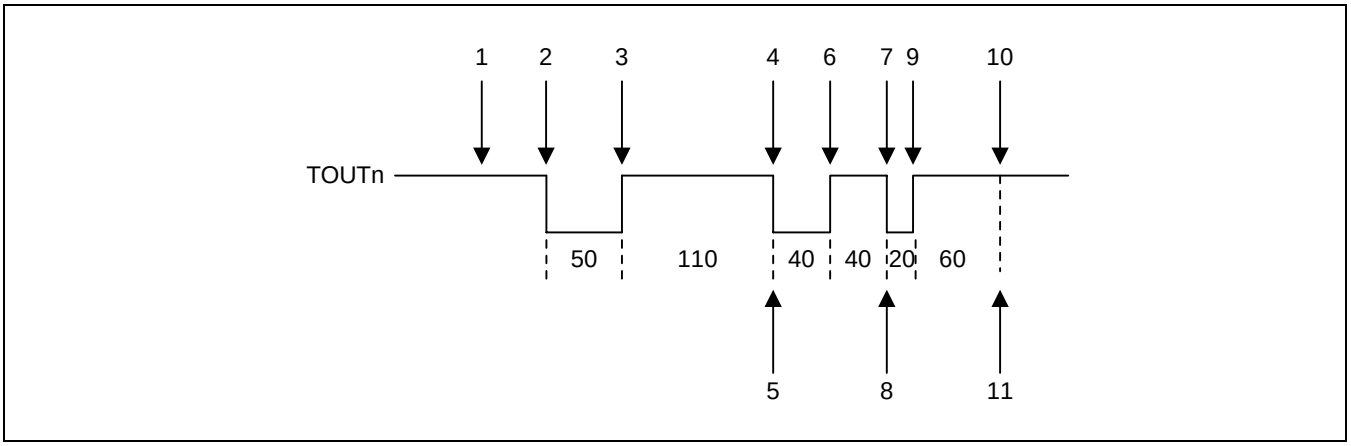


Figure 13-4. Example of a Timer Operation

The above Figure 13-4 shows the result of the following procedure:

1. Enable the auto re-load function. Set the TCNTBn to 160 (50+110) and the TCMPBn to 110. Set the manual update bit and configure the inverter bit (on/off). The manual update bit sets TCNTn and TCMPn to the values of TCNTBn and TCMPBn, respectively.

   And then, set the TCNTBn and the TCMPBn to 80 (40+40) and 40, respectively, to determine the next reload value.
2. Set the start bit, provided that manual_update is 0 and the inverter is off and auto reload is on. The timer starts counting down after latency time within the timer resolution.
3. When the TCNTn has the same value as that of the TCMPn, the logic level of the TOUTn is changed from low to high.
4. When the TCNTn reaches 0, the interrupt request is generated and TCNTBn value is loaded into a temporary register. At the next timer tick, the TCNTn is reloaded with the temporary register value (TCNTBn).
5. In Interrupt Service Routine (ISR), the TCNTBn and the TCMPBn are set to 80 (20+60) and 60, respectively, for the next duration.
6. When the TCNTn has the same value as the TCMPn, the logic level of TOUTn is changed from low to high.
7. When the TCNTn reaches 0, the TCNTn is reloaded automatically with the TCNTBn, triggering an interrupt request.
8. In Interrupt Service Routine (ISR), auto reload and interrupt request are disabled to stop the timer.
9. When the value of the TCNTn is same as the TCMPn, the logic level of the TOUTn is changed from low to high.
10. Even when the TCNTn reaches 0, the TCNTn is not any more reloaded and the timer is stopped because auto reload has been disabled.
11. No more interrupt requests are generated.

PULSE WIDTH MODULATION (PWM)

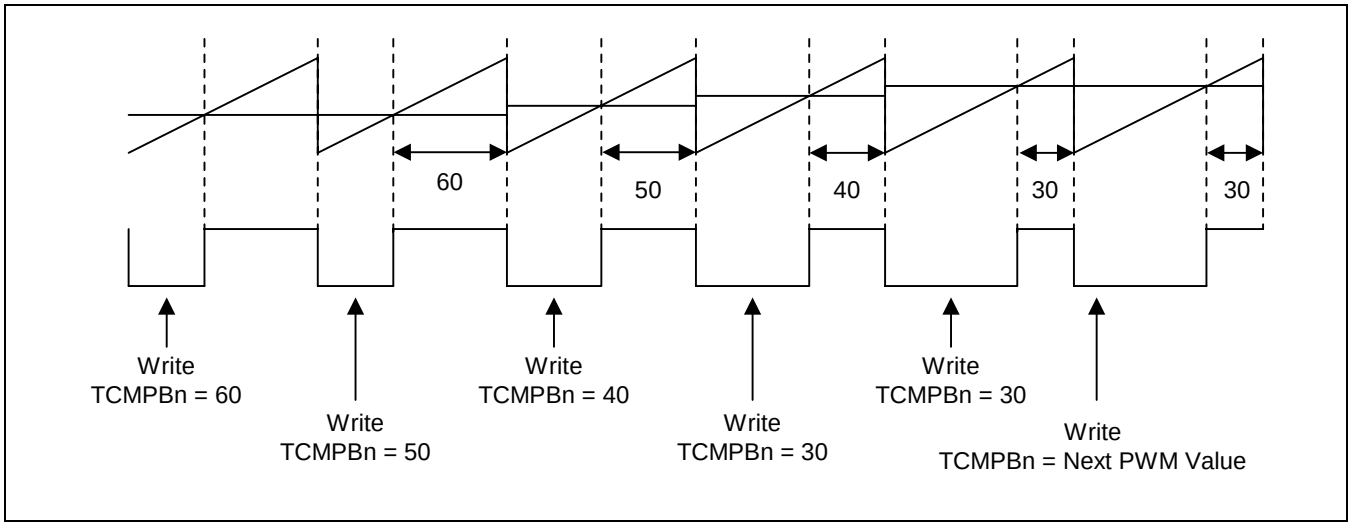


Figure 13-5. Example of PWM

PWM function can be implemented by using the TCMPBn. PWM frequency is determined by TCNTBn. Figure 13-5 shows a PWM value determined by TCMPBn.

For a higher PWM value, decrease the TCMPBn value. For a lower PWM value, increase the TCMPBn value. If an output inverter is enabled, the increment/decrement may be reversed.

The double buffering function allows the TCMPBn, for the next PWM cycle, written at any point in the current PWM cycle by ISR or other routine.

OUTPUT LEVEL CONTROL

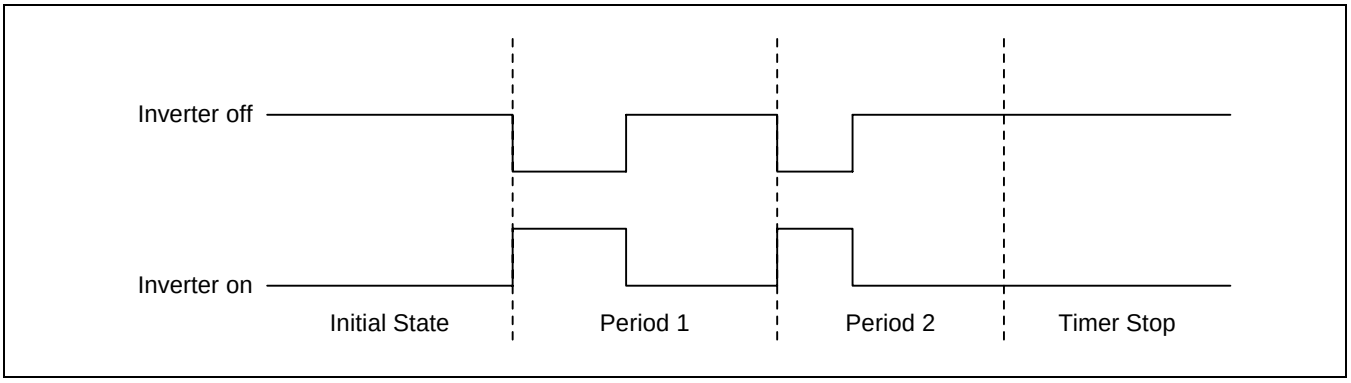


Figure 13-6. Inverter On/Off

The following procedure describes how to maintain TOUT as high or low (assume the inverter is off):

1. Turn off the auto reload bit. And then, the timer is stopped after the TCNTn reaches 0, TOUTn goes to high level (recommended).
2. Stop the timer by clearing the timer start/stop bit to 0. If TCNTn $\leq$ TCMPn at that moment, the output level is high. If TCNTn >TCMPn, the output level is low.
3. The TOUTn can be inverted by the inverter on/off bit in TCON. The inverter removes the additional circuit to adjust the output level.

DEAD ZONE GENERATOR

The Dead Zone is for the PWM control in a power device. This function enables the insertion of the time gap between a turn-off of a switching device and a turn on of another switching device. This time gap prohibits the two switching devices from being turned on simultaneously, even for a very short time.

TOUT0 is the PWM output. nTOUT0 is the inversion of the TOUT0. If the dead zone is enabled, the output wave form of TOUT0 and nTOUT0 will be TOUT0_DZ and nTOUT0_DZ, respectively. nTOUT0_DZ is routed to the TOUT1 pin.

In the dead zone interval, TOUT0_DZ and nTOUT0_DZ can never be turned on simultaneously.

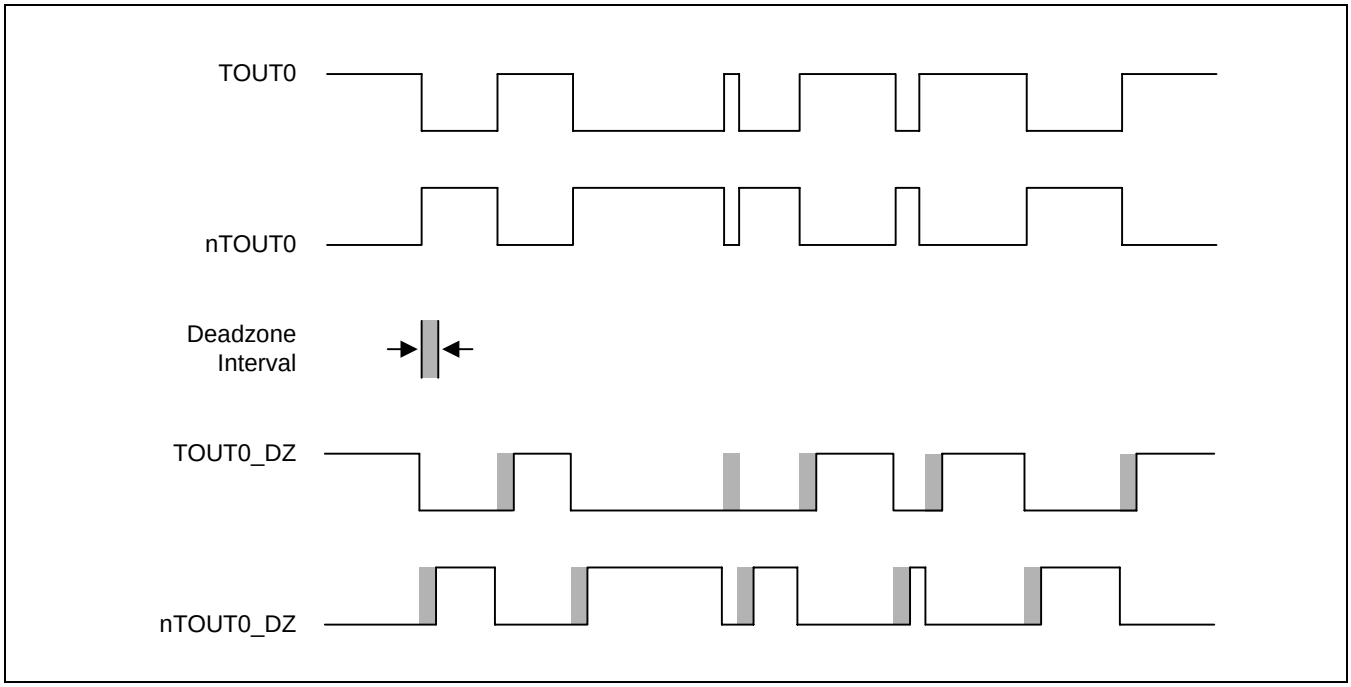


Figure 13-7. The Wave Form When a Dead Zone Feature is Enabled

DMA REQUEST MODE

The PWM timer can generate a DMA request at every specific time. The timer keeps DMA request signals (nDMA_REQ) low until the timer receives an ACK signal. When the timer receives the ACK signal, it makes the request signal inactive. The timer, which generates the DMA request, is determined by setting DMA mode bits (in TCFG1 register). If one of timers is configured as DMA request mode, that timer does not generate an interrupt request. The others can generate interrupt normally.

DMA mode configuration and DMA / interrupt operation

DMA Mode	DMA Request	Timer0 INT	Timer1 INT	Timer2 INT	Timer3 INT	Timer4 INT
0000	No select	ON	ON	ON	ON	ON
0001	Timer0	OFF	ON	ON	ON	ON
0010	Timer1	ON	OFF	ON	ON	ON
0011	Timer2	ON	ON	OFF	ON	ON
0100	Timer3	ON	ON	ON	OFF	ON
0101	Timer4	ON	ON	ON	ON	OFF
0110	No select	ON	ON	ON	ON	ON

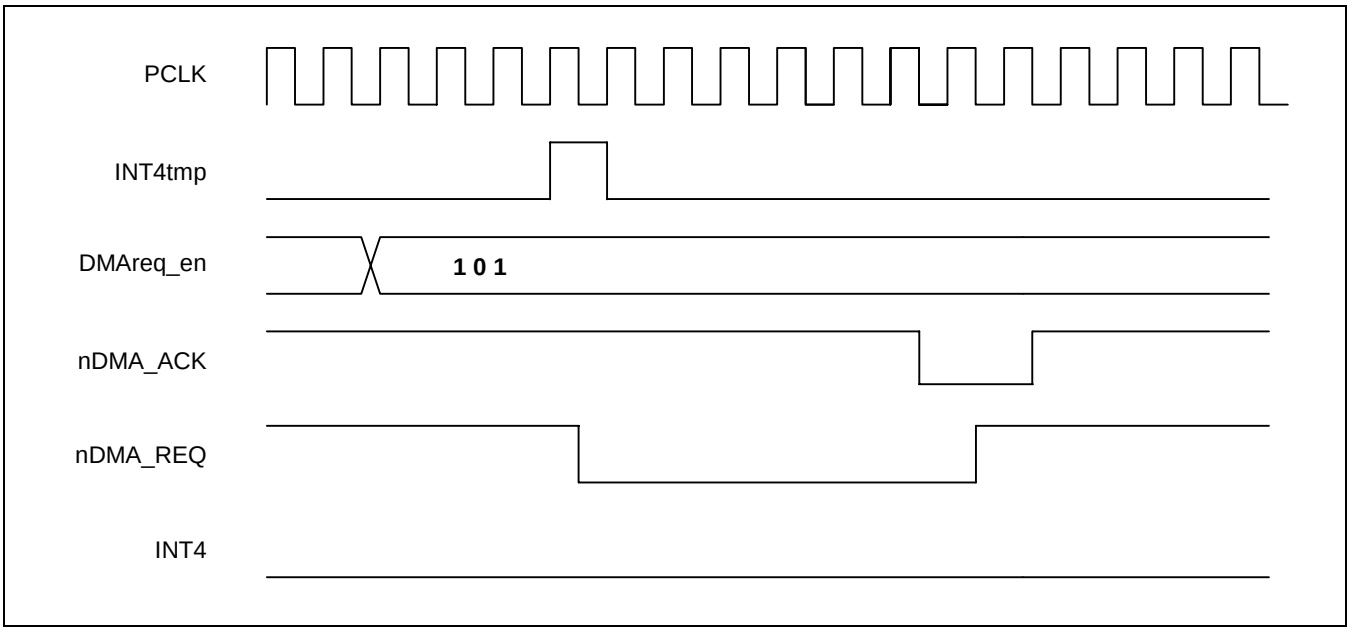


Figure 13-8. Timer4 DMA Mode Operation

PWM TIMER CONTROL REGISTERS

TIMER CONFIGURATION REGISTER0 (TCFG0)

Timer input clock Frequency = PCLK / {prescaler value+1} / {divider value}
{prescaler value} = 0~255
{divider value} = 2, 4, 8, 16

Register	Address	R/W	Description	Reset Value
TCFG0	0x51000000	R/W	Configures the two 8-bit prescalers	0x00000000

TCFG0	Bit	Description	Initial State
Reserved	[31:24]		0x00
Dead zone length	[23:16]	These 8 bits determine the dead zone length. The 1 unit time of the dead zone length is equal to that of timer 0.	0x00
Prescaler 1	[15:8]	These 8 bits determine prescaler value for Timer 2, 3 and 4.	0x00
Prescaler 0	[7:0]	These 8 bits determine prescaler value for Timer 0 and 1.	0x00

TIMER CONFIGURATION REGISTER1 (TCFG1)

Register	Address	R/W	Description	Reset Value
TCFG1	0x51000004	R/W	5-MUX & DMA mode selection register	0x00000000

TCFG1	Bit	Description	Initial State
Reserved	[31:24]		00000000
DMA mode	[23:20]	Select DMA request channel 0000 = No select (all interrupt) 0001 = Timer0 0010 = Timer1 0011 = Timer2 0100 = Timer3 0101 = Timer4 0110 = Reserved	0000
MUX 4	[19:16]	Select MUX input for PWM Timer4. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = External TCLK	0000
MUX 3	[15:12]	Select MUX input for PWM Timer3. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = External TCLK	0000
MUX 2	[11:8]	Select MUX input for PWM Timer2. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = External TCLK	0000
MUX 1	[7:4]	Select MUX input for PWM Timer1. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = External TCLK	0000
MUX 0	[3:0]	Select MUX input for PWM Timer0. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = External TCLK	0000

Notice) When you use External TCLK, duty of TOUT may show slight error. External TCLK is sampled by PCLK in PWM module. But External TCLK and PCLK is asynchronous clock. So External TCLK may not be sampled at exact time. This slight error can be reduced when External clock is slower than PCLK. So we recommend using External PCLK under 1MHz.

(Ex. When PCLK is 66MHz and External PCLK is 1MHz, duty or jitter error can be 1.5%. When PCLK is 66MHz and External PCLK is 0.5MHz, duty or jitter error can be 0.75%)

TIMER CONTROL (TCON) REGISTER

Register	Address	R/W	Description	Reset Value
TCON	0x51000008	R/W	Timer control register	0x00000000

TCON	Bit	Description	Initial state
Timer 4 auto reload on/off	[22]	Determine auto reload on/off for Timer 4. 0 = One-shot 1 = Interval mode (auto reload)	0
Timer 4 manual update (note)	[21]	Determine the manual update for Timer 4. 0 = No operation 1 = Update TCNTB4	0
Timer 4 start/stop	[20]	Determine start/stop for Timer 4. 0 = Stop 1 = Start for Timer 4	0
Timer 3 auto reload on/off	[19]	Determine auto reload on/off for Timer 3. 0 = One-shot 1 = Interval mode (auto reload)	0
Timer 3 output inverter on/off	[18]	Determine output inverter on/off for Timer 3. 0 = Inverter off 1 = Inverter on for TOUT3	0
Timer 3 manual update (note)	[17]	Determine manual update for Timer 3. 0 = No operation 1 = Update TCNTB3 & TCMPB3	0
Timer 3 start/stop	[16]	Determine start/stop for Timer 3. 0 = Stop 1 = Start for Timer 3	0
Timer 2 auto reload on/off	[15]	Determine auto reload on/off for Timer 2. 0 = One-shot 1 = Interval mode (auto reload)	0
Timer 2 output inverter on/off	[14]	Determine output inverter on/off for Timer 2. 0 = Inverter off 1 = Inverter on for TOUT2	0
Timer 2 manual update (note)	[13]	Determine the manual update for Timer 2. 0 = No operation 1 = Update TCNTB2 & TCMPB2	0
Timer 2 start/stop	[12]	Determine start/stop for Timer 2. 0 = Stop 1 = Start for Timer 2	0
Timer 1 auto reload on/off	[11]	Determine the auto reload on/off for Timer1. 0 = One-shot 1 = Interval mode (auto reload)	0
Timer 1 output inverter on/off	[10]	Determine the output inverter on/off for Timer1. 0 = Inverter off 1 = Inverter on for TOUT1	0
Timer 1 manual update (note)	[9]	Determine the manual update for Timer 1. 0 = No operation 1 = Update TCNTB1 & TCMPB1	0
Timer 1 start/stop	[8]	Determine start/stop for Timer 1. 0 = Stop 1 = Start for Timer 1	0

NOTE: The bits have to be cleared at next writing.

TIMER CONTROL (TCON) REGISTER (Continued)

TCON	Bit	Description	Initial state
Reserved	[7:5]	Reserved	
Dead zone enable	[4]	Determine the dead zone operation. 0 = Disable 1 = Enable	0
Timer 0 auto reload on/off	[3]	Determine auto reload on/off for Timer 0. 0 = One-shot 1 = Interval mode(auto reload)	0
Timer 0 output inverter on/off	[2]	Determine the output inverter on/off for Timer 0. 0 = Inverter off 1 = Inverter on for TOUT0	0
Timer 0 manual update (note)	[1]	Determine the manual update for Timer 0. 0 = No operation 1 = Update TCNTB0 & TCMPB0	0
Timer 0 start/stop	[0]	Determine start/stop for Timer 0. 0 = Stop 1 = Start for Timer 0	0

NOTE: The bit has to be cleared at next writing.

TIMER 0 COUNT BUFFER REGISTER & COMPARE BUFFER REGISTER (TCNTB0/TCMPB0)

Register	Address	R/W	Description	Reset Value
TCNTB0	0x5100000C	R/W	Timer 0 count buffer register	0x00000000
TCMPB0	0x51000010	R/W	Timer 0 compare buffer register	0x00000000

TCMPB0	Bit	Description	Initial State
Timer 0 compare buffer register	[15:0]	Set compare buffer value for Timer 0	0x00000000

TCNTB0	Bit	Description	Initial State
Timer 0 count buffer register	[15:0]	Set count buffer value for Timer 0	0x00000000

TIMER 0 COUNT OBSERVATION REGISTER (TCNTO0)

Register	Address	R/W	Description	Reset Value
TCNTO0	0x51000014	R	Timer 0 count observation register	0x00000000

TCNTO0	Bit	Description	Initial State
Timer 0 observation register	[15:0]	Set count observation value for Timer 0	0x00000000

TIMER 1 COUNT BUFFER REGISTER & COMPARE BUFFER REGISTER (TCNTB1/TCMPB1)

Register	Address	R/W	Description	Reset Value
TCNTB1	0x51000018	R/W	Timer 1 count buffer register	0x00000000
TCMPB1	0x5100001C	R/W	Timer 1 compare buffer register	0x00000000

TCMPB1	Bit	Description	Initial State
Timer 1 compare buffer register	[15:0]	Set compare buffer value for Timer 1	0x00000000

TCNTB1	Bit	Description	Initial State
Timer 1 count buffer register	[15:0]	Set count buffer value for Timer 1	0x00000000

TIMER 1 COUNT OBSERVATION REGISTER (TCNTO1)

Register	Address	R/W	Description	Reset Value
TCNTO1	0x51000020	R	Timer 1 count observation register	0x00000000

TCNTO1	Bit	Description	Initial State
Timer 1 observation register	[15:0]	Set count observation value for Timer 1	0x00000000

TIMER 2 COUNT BUFFER REGISTER & COMPARE BUFFER REGISTER (TCNTB2/TCMPB2)

Register	Address	R/W	Description	Reset Value
TCNTB2	0x51000024	R/W	Timer 2 count buffer register	0x00000000
TCMPB2	0x51000028	R/W	Timer 2 compare buffer register	0x00000000

TCMPB2	Bit	Description	Initial State
Timer 2 compare buffer register	[15:0]	Set compare buffer value for Timer 2	0x00000000

TCNTB2	Bit	Description	Initial State
Timer 2 count buffer register	[15:0]	Set count buffer value for Timer 2	0x00000000

TIMER 2 COUNT OBSERVATION REGISTER (TCNTO2)

Register	Address	R/W	Description	Reset Value
TCNTO2	0x5100002C	R	Timer 2 count observation register	0x00000000

TCNTO2	Bit	Description	Initial State
Timer 2 observation register	[15:0]	Set count observation value for Timer 2	0x00000000

TIMER 3 COUNT BUFFER REGISTER & COMPARE BUFFER REGISTER (TCNTB3/TCMPB3)

Register	Address	R/W	Description	Reset Value
TCNTB3	0x51000030	R/W	Timer 3 count buffer register	0x00000000
TCMPB3	0x51000034	R/W	Timer 3 compare buffer register	0x00000000

TCMPB3	Bit	Description	Initial State
Timer 3 compare buffer register	[15:0]	Set compare buffer value for Timer 3	0x00000000

TCNTB3	Bit	Description	Initial State
Timer 3 count buffer register	[15:0]	Set count buffer value for Timer 3	0x00000000

TIMER 3 COUNT OBSERVATION REGISTER (TCNTO3)

Register	Address	R/W	Description	Reset Value
TCNTO3	0x51000038	R	Timer 3 count observation register	0x00000000

TCNTO3	Bit	Description	Initial State
Timer 3 observation register	[15:0]	Set count observation value for Timer 3	0x00000000

TIMER 4 COUNT BUFFER REGISTER (TCNTB4)

Register	Address	R/W	Description	Reset Value
TCNTB4	0x5100003C	R/W	Timer 4 count buffer register	0x00000000

TCNTB4	Bit	Description	Initial State
Timer 4 count buffer register	[15:0]	Set count buffer value for Timer 4	0x00000000

TIMER 4 COUNT OBSERVATION REGISTER (TCNTO4)

Register	Address	R/W	Description	Reset Value
TCNTO4	0x51000040	R	Timer 4 count observation register	0x00000000

TCNTO4	Bit	Description	Initial State
Timer 4 observation register	[15:0]	Set count observation value for Timer 4	0x00000000

NOTES

14 REAL TIME CLOCK

OVERVIEW

The Real Time Clock (RTC) unit can be operated by the backup battery while the system power is off. The RTC can transmit 8-bit data to CPU as Binary Coded Decimal (BCD) values using the STRB/LDRB ARM operation. The data include the time by second, minute, hour, date, day, month, and year. The RTC unit works with an external 32.768 kHz crystal and also can perform the alarm function.

FEATURES

— BCD number: second, minute, hour, date, day, month, and year

— Leap year generator

— Alarm function: alarms interrupt or wake-up from power-off mode

— Year 2000 problem is removed.

— Independent power pin (RTCVDD)

— Supports millisecond tick time interrupt for RTOS kernel time tick.

— Power on Reset detect

REAL TIME CLOCK OPERATION

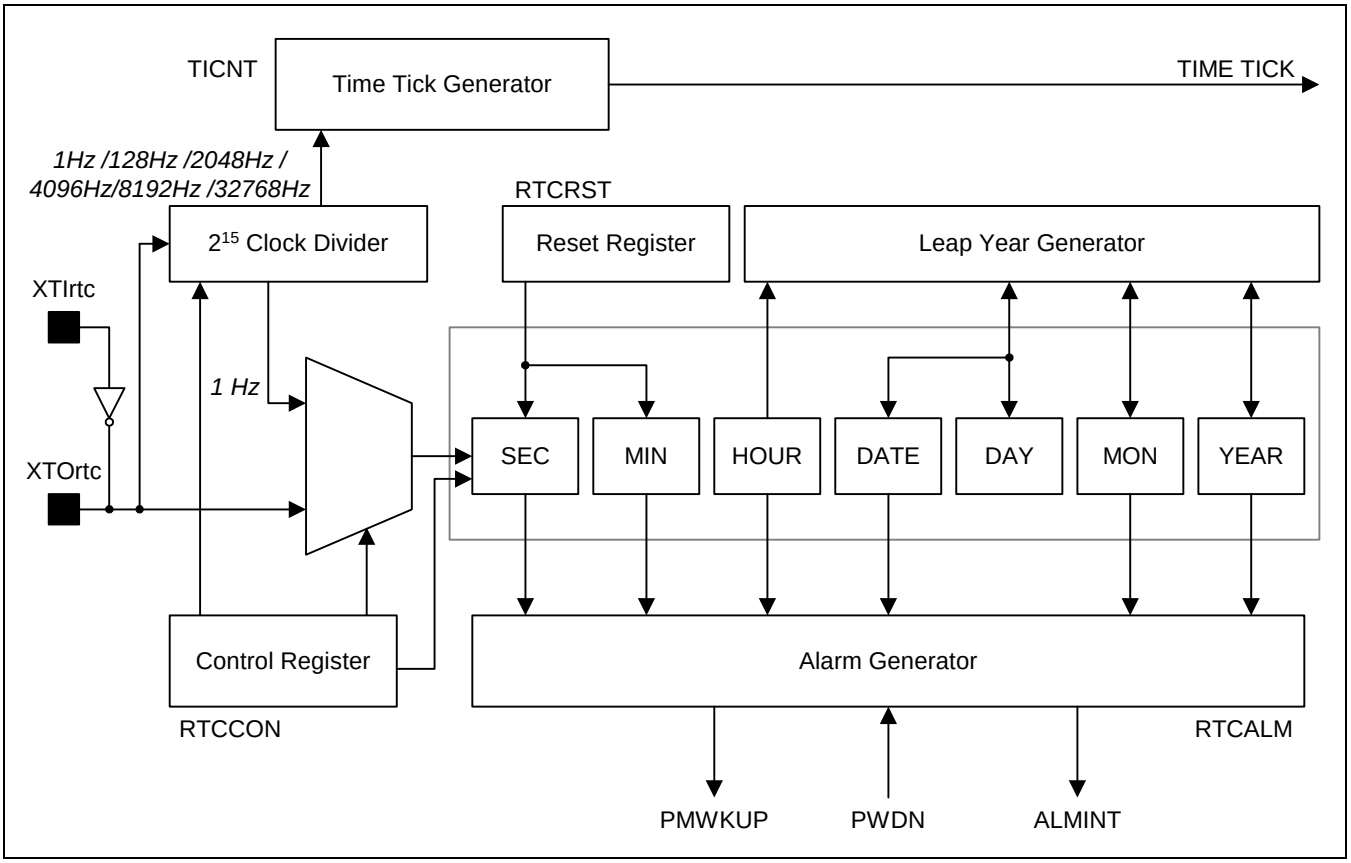


Figure 14-1. Real Time Clock Block Diagram

LEAP YEAR GENERATOR

The leap year generator can determine the last date of each month out of 28, 29, 30, or 31, based on data from BCDDATE, BCDMON, and BCDYEAR. This block considers leap year in deciding on the last date. An 8-bit counter can only represent 2 BCD digits, so it cannot decide whether "00" year (the year with its last two digits zeros) is a leap year or not. For example, it cannot discriminate between 1900 and 2000. To solve this problem, the RTC block in S3C2443X has hard-wired logic to support the leap year in 2000. Note 1900 is not leap year while 2000 is leap year. Therefore, two digits of 00 in S3C2443X denote 2000, not 1900.

READ/WRITE REGISTERS

Bit 0 of the RTCCON register must be set high in order to write the BCD register in RTC block. To display the second, minute, hour, date, month, and year, the CPU should read the data in BCDSEC, BCDMIN, BCDHOUR, BCDDAY, BCDDATE, BCDMON, and BCDYEAR registers, respectively, in the RTC block. However, a one second deviation may exist because multiple registers are read. For example, when the user reads the registers from BCDYEAR to BCDMIN, the result is assumed to be 2059 (Year), 12 (Month), 31 (Date), 23 (Hour) and 59 (Minute). When the user read the BCDSEC register and the value ranges from 1 to 59 (Second), there is no problem, but, if the value is 0 sec., the year, month, date, hour, and minute may be changed to 2060 (Year), 1 (Month), 1 (Date), 0 (Hour) and 0 (Minute) because of the one second deviation that was mentioned. In this case, the user should re-read from BCDYEAR to BCDSEC if BCDSEC is zero.

BACKUP BATTERY OPERATION

The RTC logic can be driven by the backup battery, which supplies the power through the RTCVDD pin into the RTC block, even if the system power is off. When the system is off, the interfaces of the CPU and RTC logic should be blocked, and the backup battery only drives the oscillation circuit and the BCD counters to minimize power dissipation.

ALARM FUNCTION

The RTC generates an alarm signal at a specified time in the power-off mode or normal operation mode. In normal operation mode, the alarm interrupt (ALMINT) is activated. In the power-off mode, the power management wakeup (PMWKUP) signal is activated as well as the ALMINT. The RTC alarm register (RTCALM) determines the alarm enable/disable status and the condition of the alarm time setting.

TICK TIME INTERRUPT

The RTC tick time is used for interrupt request. The TICNT1/2 register have an interrupt enable bit and the count value for the interrupt. When the internal count value reaches '0', the tick time interrupt occurs. Then the period of interrupt is as follows:

RTCCON[4]	RTCCON[7:5]	Tick clock source frequency (Hz)	Clock range (s)
1'b1	3'bxxx	32768 (2^15)	0 ~ 1
1'b0	3'b000	16384 (2^14)	0 ~ 2
1'b0	3'b001	8192 (2^13)	0 ~ 4
1'b0	3'b010	4096 (2^12)	0 ~ 8
1'b0	3'b011	2048 (2^11)	0 ~ 16
1'b0	3'b100	128 (2^7)	0 ~ 256
1'b0	3'b101	1	0 ~ 32768

NOTE: Tick time resolution can be extended by selecting the appropriate tick time clock source.

Tick clock source frequency	Resolution	Minimum interval (Tick count value=1)	Maximum interval (Tick count value=32767)
32768 Hz	0.03 ms	0.06 ms	1 s
16384 Hz	0.06 ms	0.12 ms	2 s
8192 Hz	0.12 ms	0.24 ms	4 s
4096 Hz	0.24 ms	0.49 ms	8 s
2048 Hz	0.49 ms	0.98 ms	16 s
128 Hz	7.81 ms	15.62 ms	256 s
1 Hz	1000 ms	2000 ms	32768 s

This RTC time tick may be used for real time operating system (RTOS) kernel time tick. If time tick is generated by the RTC time tick, the time related function of RTOS will always synchronized in real time.

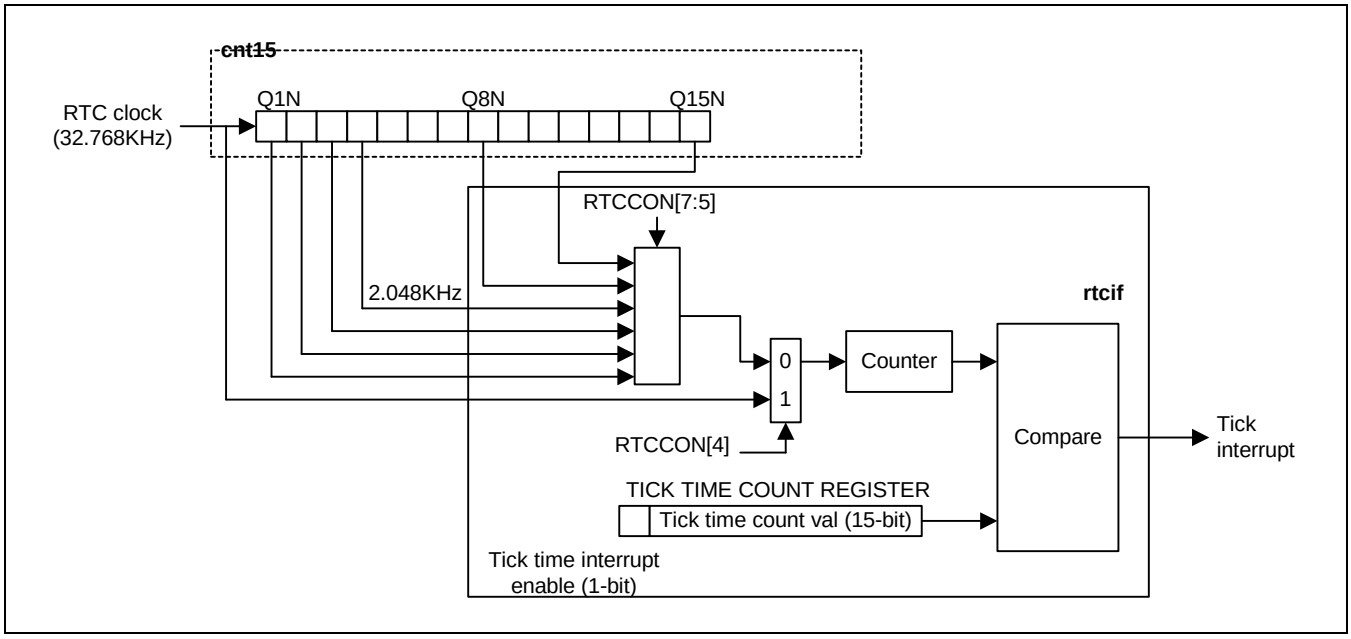


Figure 14-2. RTC tick interrupt clock scheme

32.768KHZ X-TAL CONNECTION EXAMPLE

The Figure 14-2 shows a circuit of the RTC unit oscillation at 32.768 kHz.

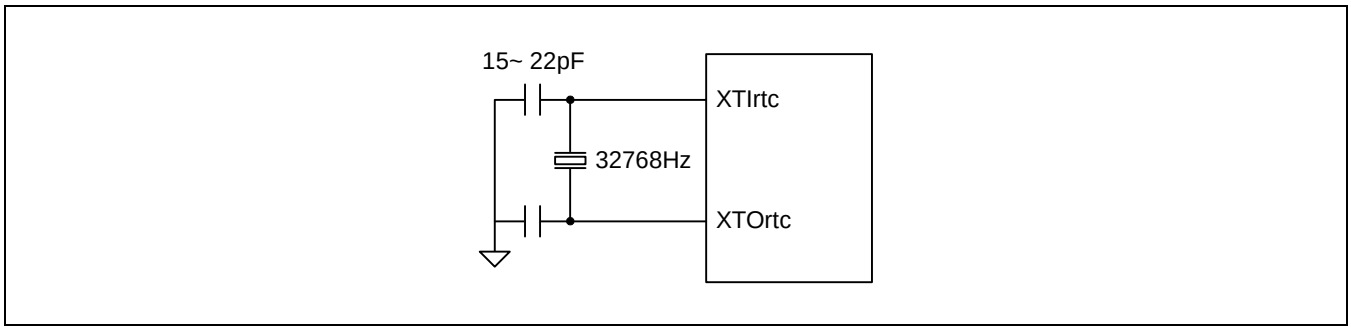


Figure 14-3. Main Oscillator Circuit Example

REAL TIME CLOCK SPECIAL REGISTERS

REAL TIME CLOCK CONTROL (RTCCON) REGISTER

The RTCCON register consists of 4 bits such as the RTCEN, which controls the write enable of the BCD registers, CLKSEL, CNTSEL, and CLKRST for testing.

RTCEN bit can control all interfaces between the CPU and the RTC, so it should be set to 1 in an RTC control routine to enable data write after a system reset. Also before power off, the RTCEN bit should be cleared to 0 to prevent inadvertent writing into RTC registers.

Register	Address	R/W	Description	Reset Value
RTCCON	0x57000040(L) 0x57000043(B)	R/W (by byte)	RTC control register	0x0

RTCCON	Bit	Description	Initial State
TICsel2	[7:5]	Tick Time clock select2. 0 = clock period of 1/16384 second 1 = clock period of 1/8192 second 2 = clock period of 1/4096 second 3 = clock period of 1/2048 second 4 = clock period of 1/128 second 5 = clock period of 1 second	0
TICsel	[4]	Tick Time clock select1. 0 = clock period select at TICsel2 1 = clock period of 1/32768 second	0
CLKRST	[3]	RTC clock count reset. 0 = No reset, 1 = Reset	0
CNTSEL	[2]	BCD count select. 0 = Merge BCD counters 1 = Reserved (Separate BCD counters)	0
CLKSEL	[1]	BCD clock select. 0 = XTAL 1/215 divided clock 1 = Reserved (XTAL clock only for test)	0
RTCEN	[0]	RTC control enable. 0 = Disable 1 = Enable **NOTE:** Only BCD time count and read operation can be performed when RTC control enable is 0 (Disabled)	0

NOTES:

1. All RTC registers have to be accessed for each byte unit using STRB and LDRB instructions or char type pointer.
2. (L): Little endian.
   (B): Big endian.

TICK TIME COUNT (TICNT0) REGISTER 0

Register	Address	R/W	Description	Reset Value
TICNT0	0x57000044(L) 0x57000047(B)	R/W (by byte)	Tick time count register	0x0

TICNT	Bit	Description	Initial State
TICK INT ENABLE	[7]	Tick time interrupt enable. 0 = Disable 1 = Enable	0
TICK TIME COUNT 0	[6:0]	Upper 7bits of 15 bit tick time count value	000000

TICK TIME COUNT (TICNT1) REGISTER 1

Register	Address	R/W	Description	Reset Value
TICNT1	0x5700004C(L) 0x5700004F(B)	R/W (by byte)	Tick time count register 1	0x0

TICNT	Bit	Description	Initial State
TICK TIME COUNT 1	[7:0]	Lower 8 bits of 15-bit tick time count value	000000

NOTE: Tick time count value = (TICK TIME COUNT 0) x 2^8 + (T ICK TIME COUNT 1)

RTC ALARM CONTROL (RTCALM) REGISTER

The RTCALM register determines the alarm enable and the alarm time. Note that the RTCALM register generates the alarm signal through both ALMINT and PMWKUP in power down mode, but only through ALMINT in the normal operation mode.

Register	Address	R/W	Description	Reset Value
RTCALM	0x57000050(L) 0x57000053(B)	R/W (by byte)	RTC alarm control register	0x0

RTCALM	Bit	Description	Initial State
Reserved	[7]	This bit must be tied as 0	0
ALMEN	[6]	Alarm functions enable. 0 = Disable, 1 = Enable	0
YEAREN	[5]	Year alarm enable. 0 = Disable, 1 = Enable	0
MONREN	[4]	Month alarm enable. 0 = Disable, 1 = Enable	0
DATEEN	[3]	Date alarm enable. 0 = Disable, 1 = Enable	0
HOUREN	[2]	Hour alarm enable. 0 = Disable, 1 = Enable	0
MINEN	[1]	Minute alarm enable. 0 = Disable, 1 = Enable	0
SECEN	[0]	Second alarm enable. 0 = Disable, 1 = Enable	0

ALARM SECOND DATA (ALMSEC) REGISTER

Register	Address	R/W	Description	Reset Value
ALMSEC	0x57000054(L) 0x57000057(B)	R/W (by byte)	Alarm second data register	0x0

ALMSEC	Bit	Description	Initial State
Reserved	[7]		0
SECDATA	[6:4]	BCD value for alarm second. 0 ~ 5	000
	[3:0]	0 ~ 9	0000

ALARM MIN DATA (ALMMIN) REGISTER

Register	Address	R/W	Description	Reset Value
ALMMIN	0x57000058(L) 0x5700005B(B)	R/W (by byte)	Alarm minute data register	0x00

ALMMIN	Bit	Description	Initial State
Reserved	[7]		0
MINDATA	[6:4]	BCD value for alarm minute. 0 ~ 5	000
	[3:0]	0 ~ 9	0000

ALARM HOUR DATA (ALMHOUR) REGISTER

Register	Address	R/W	Description	Reset Value
ALMHOUR	0x5700005C(L) 0x5700005F(B)	R/W (by byte)	Alarm hour data register	0x0

ALMHOUR	Bit	Description	Initial State
Reserved	[7:6]		00
HOURDATA	[5:4]	BCD value for alarm hour. 0 ~ 2	00
	[3:0]	0 ~ 9	0000

ALARM DATE DATA (ALMDATE) REGISTER

Register	Address	R/W	Description	Reset Value
ALMDATE	0x57000060(L) 0x57000063(B)	R/W (by byte)	Alarm date data register	0x01

ALMDAY	Bit	Description	Initial State
Reserved	[7:6]		00
DATEDATA	[5:4]	BCD value for alarm date, from 0 to 28, 29, 30, 31. 0 ~ 3	00
	[3:0]	0 ~ 9	0001

ALARM MON DATA (ALMMON) REGISTER

Register	Address	R/W	Description	Reset Value
ALMMON	0x57000064(L) 0x57000067(B)	R/W (by byte)	Alarm month data register	0x01

ALMMON	Bit	Description	Initial State
Reserved	[7:5]		00
MONDATA	[4]	BCD value for alarm month. 0 ~ 1	0
	[3:0]	0 ~ 9	0001

ALARM YEAR DATA (ALMYEAR) REGISTER

Register	Address	R/W	Description	Reset Value
ALMYEAR	0x57000068(L) 0x5700006B(B)	R/W (by byte)	Alarm year data register	0x0

ALMYEAR	Bit	Description	Initial State
YEARDATA	[7:0]	BCD value for year. 00 ~ 99	0x0

BCD SECOND (BCDSEC) REGISTER

Register	Address	R/W	Description	Reset Value
BCDSEC	0x57000070(L) 0x57000073(B)	R/W (by byte)	BCD second register	Undefined

BCDSEC	Bit	Description	Initial State
SECDATA	[6:4]	BCD value for second. 0 ~ 5	-
	[3:0]	0 ~ 9	-

BCD MINUTE (BCDMIN) REGISTER

Register	Address	R/W	Description	Reset Value
BCDMIN	0x57000074(L) 0x57000077(B)	R/W (by byte)	BCD minute register	Undefined

BCDMIN	Bit	Description	Initial State
MINDATA	[6:4]	BCD value for minute. 0 ~ 5	-
	[3:0]	0 ~ 9	-

BCD HOUR (BCDHOUR) REGISTER

Register	Address	R/W	Description	Reset Value
BCDHOUR	0x57000078(L) 0x5700007B(B)	R/W (by byte)	BCD hour register	Undefined

BCDHOUR	Bit	Description	Initial State
Reserved	[7:6]		-
HOURDATA	[5:4]	BCD value for hour. 0 ~ 2	-
	[3:0]	0 ~ 9	-

BCD DATE (BCDDATE) REGISTER

Register	Address	R/W	Description	Reset Value
BCDDATE	0x5700007C(L) 0x5700007F(B)	R/W (by byte)	BCD date register	Undefined

BCDDATE	Bit	Description	Initial State
Reserved	[7:6]		-
DATEDATA	[5:4]	BCD value for date. 0 ~ 3	-
	[3:0]	0 ~ 9	-

BCD DAY (BCDDAY) REGISTER

Register	Address	R/W	Description	Reset Value
BCDDAY	0x57000080(L) 0x57000083(B)	R/W (by byte)	BCD a day of the week register	Undefined

BCDDAY	Bit	Description	Initial State
Reserved	[7:3]		-
DAYDATA	[2:0]	BCD value for a day of the week. 1 ~ 7	-

BCD MONTH (BCDMON) REGISTER

Register	Address	R/W	Description	Reset Value
BCDMON	0x57000084(L) 0x57000087(B)	R/W (by byte)	BCD month register	Undefined

BCDMON	Bit	Description	Initial State
Reserved	[7:5]		-
MONDATA	[4]	BCD value for month. 0 ~ 1	-
	[3:0]	0 ~ 9	-

BCD YEAR (BCDYEAR) REGISTER

Register	Address	R/W	Description	Reset Value
BCDYEAR	0x57000088(L) 0x5700008B(B)	R/W (by byte)	BCD year register	Undefined

BCDYEAR	Bit	Description	Initial State
YEARDATA	[7:0]	BCD value for year. 00 ~ 99	-

TICK COUNTER (TICKCNT) REGISTER

Register	Address	R/W	Description	Reset Value
TICKCNT	0x57000090(L)	R	Internal tick time counter register	15'h0

BCDYEAR	Bit	Description	Initial State
TICKCNT	[14:0]	Internal tick counter. Only readable 0 ~ 32767	-

RTC LOWBAT CHECK (RTCLBAT) REGISTER

Register	Address	R/W	Description	Reset Value
RTCLBAT	0x57000094(L) 0x57000097(B)	R/W (by byte)	RTC Low Battry Check register	0x0

ALMYEAR	Bit	Description	Initial State
LOWBAT	[0]	1: Clear Low Battery register.	0

NOTES:

1. This is the bit for detecting low voltage. When the power source's voltage drops below 1.708V(max). This flag is set to "1". After the initial power on, it is set to 1. If this flag is set to 1 enter recovery from the backup state. This means during the backup the power was low, and all data need to be initialized. (LOWBAT bit clearing: write '1' to LOWBAT bit)
   (1) LOWBAT = "1" as result of initial supply of power
   (2) If LOWBAT bit is "1", clear the bit to "0" by after checking the RTCLBAT register.
   (3) When the power supply is low but voltage is not dropping to 1.708V, LOWBAT bit remained "0" with no change
   (4) When the power supply is low and voltage dropping below 1.708V, VL becames "1"
   (5) If LOWBAT bit is "1" clear the bit to "0" after checking the RTCLBAT register.
2. The register related to RTC did not reset by Power-On Reset when the RTC power supply keep the voltage above the VDDrtc minimum spec.
3. To write this bit, RTCEN (RTC control enable bit in RTCCON register) have to be enabled.

15 UART

OVERVIEW

The S3C2443X Universal Asynchronous Receiver and Transmitter (UART) provide four independent asynchronous serial I/O (SIO) ports, each of which can operate in Interrupt-based or DMA-based mode. In other words, the UART can generate an interrupt or a DMA request to transfer data between CPU and the UART. The UART can support bit rates up to 921.6Kbps bps using system clock. Each UART channel contains two 64-byte FIFOs for receiver and transmitter.

The S3C2443X UART includes programmable baud rates, infrared (IR) transmit/receive, one or two stop bit insertion, 5-bit, 6-bit, 7-bit or 8-bit data width and parity checking.

Each UART contains a baud-rate generator, transmitter, receiver and a control unit, as shown in Figure 15-1. The baud-rate generator can be clocked by PCLK, EXTUARTCLK or divided EPLL clock. The transmitter and the receiver contain 64-byte FIFOs and data shifters. Data is written to FIFO and then copied to the transmit shifter before being transmitted. The data is then shifted out by the transmit data pin (TxDn). Meanwhile, received data is shifted from the receive data pin (RxDn), and then copied to FIFO from the shifter.

FEATURES

— RxD0, TxD0, RxD1, TxD1, RxD2, TxD2, RxD3 and TxD3 with DMA-based or interrupt-based operation

— UART Ch 0, 1, 2 and 3 with IrDA 1.0 & 64-byte FIFO

— UART Ch 0, 1 and 2 with nRTS0, nCTS0, nRTS1, nCTS1, nRTS2 and nCTS2

— Supports handshake transmit/receive

BLOCK DIAGRAM

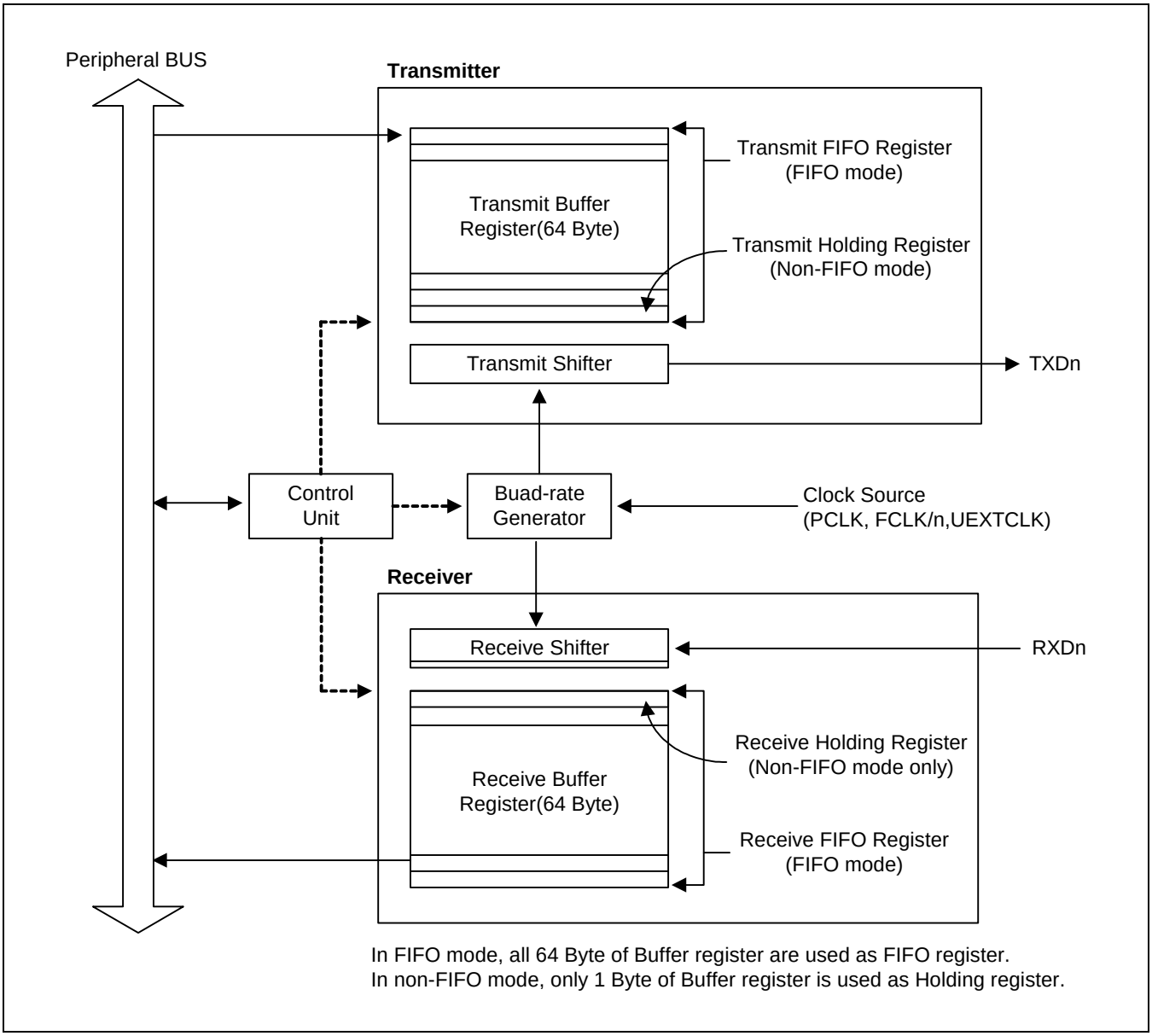


Figure 15-1. UART Block Diagram (with FIFO)

UART OPERATION

The following sections describe the UART operations that include data transmission, data reception, interrupt generation, baud-rate generation, Loopback mode, Infrared mode, and auto flow control.

Data Transmission

The data frame for transmission is programmable. It consists of a start bit, 5 to 8 data bits, an optional parity bit and 1 to 2 stop bits, which can be specified by the line control register (ULCONn). The transmitter can also produce the break condition, which forces the serial output to logic 0 state for one frame transmission time. This block transmits break signals after the present transmission word is transmitted completely. After the break signal transmission, it continuously transmits data into the Tx FIFO (Tx holding register in the case of Non-FIFO mode).

Data Reception

Like the transmission, the data frame for reception is also programmable. It consists of a start bit, 5 to 8 data bits, an optional parity bit and 1 to 2 stop bits in the line control register (ULCONn). The receiver can detect overrun error, parity error, frame error and break condition, each of which can set an error flag.

— The overrun error indicates that new data has overwritten the old data before the old data has been read.

— The parity error indicates that the receiver has detected an unexpected parity condition.

— The frame error indicates that the received data does not have a valid stop bit.

— The break condition indicates that the RxDn input is held in the logic 0 state for a duration longer than one frame transmission time.

Receive time-out condition occurs when it does not receive any data during the 3 word time (this interval follows the setting of Word Length bit) and the Rx FIFO is not empty in the FIFO mode.

Auto Flow Control (AFC)

The S3C2443X's UART 0, UART 1 and UART 2 support auto flow control with nRTS and nCTS signals. In case, it can be connected to external UARTs. If users want to connect a UART to a Modem, disable auto flow control bit in UMCONn register and control the signal of nRTS by software.

In AFC, nRTS depends on the condition of the receiver and nCTS signals control the operation of the transmitter. The UART's transmitter transfers the data in FIFO only when nCTS signals are activated (in AFC, nCTS means that other UART's FIFO is ready to receive data). Before the UART receives data, nRTS has to be activated when its receive FIFO has a spare more than 32-byte and has to be inactivated when its receive FIFO has a spare under 32-byte (in AFC, nRTS means that its own receive FIFO is ready to receive data).

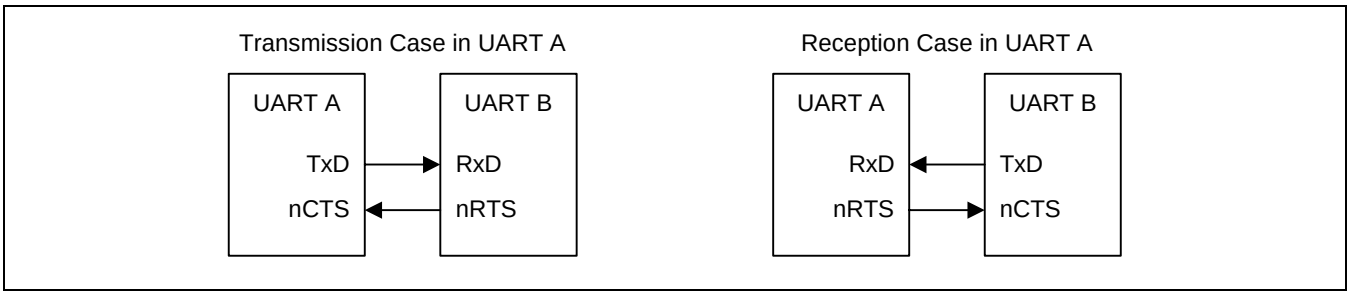


Figure 15-2. UART AFC interface

NOTE:

UART 3 does not support AFC function, because the S3C2443X has no nRTS 3 and nCTS 3.

Example of Non Auto-Flow Control (Controlling nRTS and nCTS by Software)

Rx Operation with FIFO

1. Select receive mode (Interrupt or DMA mode).
2. Check the value of Rx FIFO count in UFSTATn register. If the value is less than 32, users have to set the value of UMCONn[0] to '1' (activating nRTS), and if it is equal or larger than 32 users have to set the value to '0' (inactivating nRTS).
3. Repeat the Step 2.

Tx Operation with FIFO

1. Select transmit mode (Interrupt or DMA mode).
2. Check the value of UMSTATn[0]. If the value is '1' (activating nCTS), users write the data to Tx FIFO register.

RS-232C interface

If the user wants to connect the UART to modem interface (instead of null modem), nRTS, nCTS, nDSR, nDTR, DCD and nRI signals are needed. In this case, the users can control these signals with general I/O ports by software because the AFC does not support the RS-232C interface.

Interrupt/DMA Request Generation

Each UART of the S3C2443X has seven status (Tx/Rx/Error) signals: Overrun error, Parity error, Frame error, Break, Receive buffer data ready, Transmit buffer empty, and Transmit shifter empty, all of which are indicated by the corresponding UART status register (UTRSTATn/UERSTATn).

The overrun error, parity error, frame error and break condition are referred to as the receive error status. Each of which can cause the receive error status interrupt request, if the receive-error-status-interrupt-enable bit is set to one in the control register, UCONn. When a receive-error-status-interrupt-request is detected, the signal causing the request can be identified by reading the value of UERSTSTn.

When the receiver transfers the data of the receive shifter to the receive FIFO register in FIFO mode and the number of received data reaches Rx FIFO Trigger Level, Rx interrupt is generated. If the Receive mode is in control register (UCONn) and is selected as 1 (Interrupt request or polling mode). In the Non-FIFO mode, transferring the data of the receive shifter to receive holding register will cause Rx interrupt under the Interrupt request and polling mode.

When the transmitter transfers data from its transmit FIFO register to its transmit shifter and the number of data left in transmit FIFO reaches Tx FIFO Trigger Level, Tx interrupt is generated, if Transmit mode in control register is selected as Interrupt request or polling mode. In the Non-FIFO mode, transferring data from the transmit holding register to the transmit shifter will cause Tx interrupt under the Interrupt request and polling mode.

If the Receive mode and Transmit mode in control register are selected as the DMAn request mode then DMAn request occurs instead of Rx or Tx interrupt in the situation mentioned above.

Table 15-1. Interrupts in Connection with FIFO

Type	FIFO Mode	Non-FIFO Mode
Rx Interrupt	Generated whenever receive data reaches the trigger level of receive FIFO. Generated when the number of data in FIFO does not reaches Rx FIFO trigger Level and does not receive any data during 3 words time (receive time out). This interval follows the setting of Word Length bit.	Generated by the receiving holding register whenever receive buffer becomes full.
Tx Interrupt	Generated whenever transmit data reaches the trigger level of transmit FIFO (Tx FIFO trigger Level).	Generated by the transmitting holding register whenever transmit buffer becomes empty.
Error Interrupt	Generated when frame error, parity error, or break signal are detected. Generated when it gets to the top of the receive FIFO without reading out data in it (overrun error).	Generated by all errors. However if another error occurs at the same time, only one interrupt is generated.

UART Error Status FIFO

UART has the error status FIFO besides the Rx FIFO register. The error status FIFO indicates which data, among FIFO registers, is received with an error. The error interrupt will be issued only when the data, which has an error, is ready to read out. To clear the error status FIFO, the URXHn with an error and UERSTATn must be read out.

For example,

It is assumed that the UART Rx FIFO receives A, B, C, D and E characters sequentially and the frame error occurs while receiving 'B', and the parity error occurs while receiving 'D'.

The actual UART receive error will not generate any error interrupt because the character which is received with an error would have not been read. The error interrupt will occur once the character is read.

Figure 15-3 shows the UART receiving the five characters including the two errors.

Time	Sequence Flow	Error Interrupt	Note
#0	When no character is read out	–	
#1	A, B, C, D, and E is received	–	
#2	After A is read out	The frame error (in B) interrupt occurs.	The 'B' has to be read out.
#3	After B is read out	–	
#4	After C is read out	The parity error (in D) interrupt occurs.	The 'D' has to be read out.
#5	After D is read out	–	
#6	After E is read out	–	

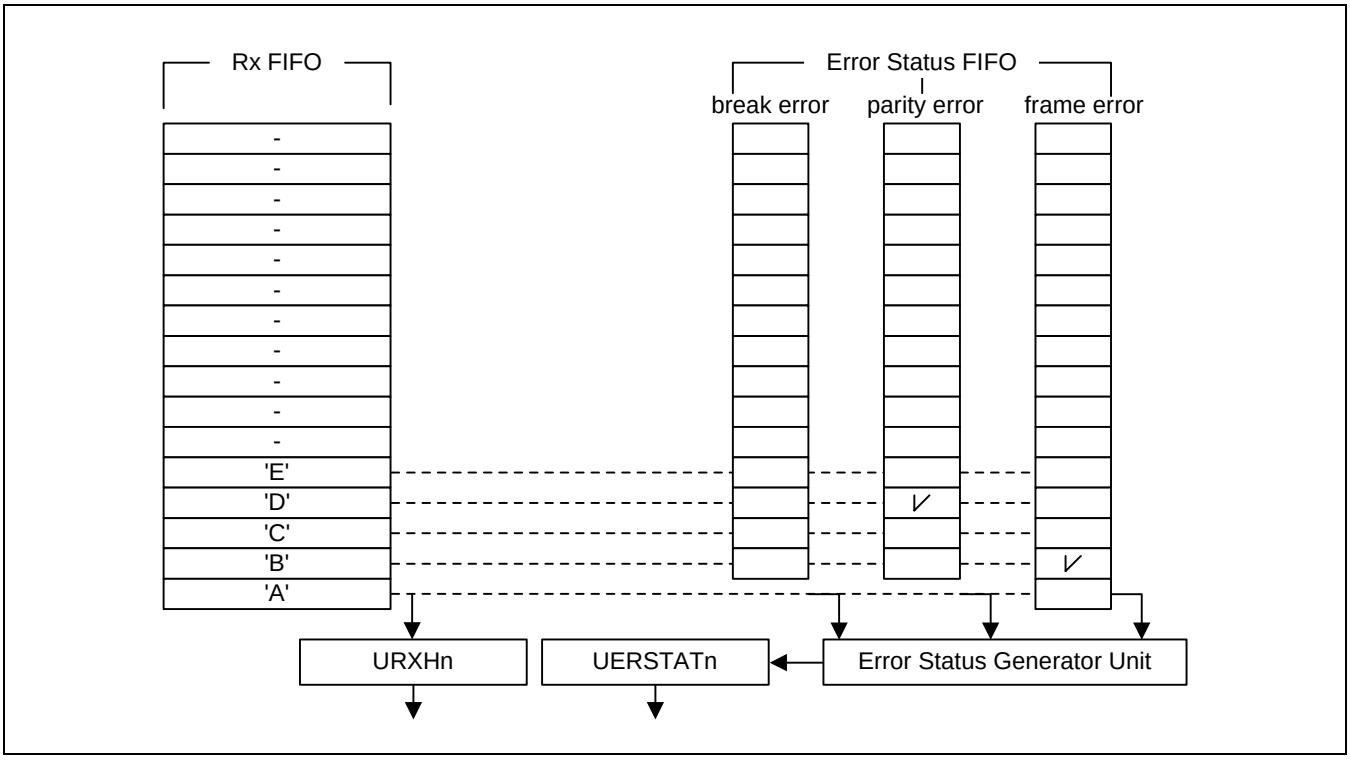


Figure 15-3. Example showing UART Receiving 5 Characters with 2 Errors

Baud-rate Generation

Each UART's baud-rate generator provides the serial clock for the transmitter and the receiver. The source clock for the baud-rate generator can be selected with the S3C2443X's internal system clock or EXTUARTCLK. In other words, dividend is selectable by setting Clock Selection of UCONn. The baud-rate clock is generated by dividing the source clock (PCLK or EXTUARTCLK) by 16. The value stored in the baud rate divisor register (UBRDIVn) and dividing slot register(UDIVSLOTn), are used to determine the serial Tx/Rx clock rate (baud rate) as follows:

DIV_VAL = UBRDIVn + (num of 1's in UDIVSLOTn)/16
= (SRCCLK / (baud rate x 16)) –1

(SRCCLK : PCLK, EXTUARTCLK or divided EPLL clock)

Where, DIV_VAL should be from 1 to (2^{16}-1), but can be set zero only using the EXTUARTCLK. The EXTUARTCLK and divided EPLL clock should be smaller than PCLK. Using UDIVSLOT which is the factor of floating point divisor, you can make more accurate baud rate.

For example, if the baud rate is 115200 bps and SRCCLK is 40 MHz, UBRDIVn and UDIVSLOTn are :

DIV_VAL = (40000000 / (115200 x 16)) -1
= 21.7 -1
= 20.7

* **UBRDIVn** = 20
(integer part of DIV_VAL)

(num of 1's in UDIVSLOTn)/16 = 0.7
(num of 1's in UDIVSLOTn) = 11
* **UDIVSLOTn** = 0xDDD5 (**11**0**1**_**11**0**1**_**11**0**1**_**1**0**1**0b)
(floating point part of DIV_VAL)

As a result, DIV_VAL = 20.6875

Baud-Rate Error Tolerance

UART Frame error should be less than 1.87%(3/160).

tUPCLK = (UBRDIVn + 1) x 16 x 1Frame / PCLK tUPCLK: Real UART Clock

tEXTUARTCLK = 1Frame / baud-rate tEXTUARTCLK: Ideal UART Clock

UART error = (tUPCLK – tEXTUARTCLK) / tEXTUARTCLK x 100%

NOTE:

1Frame = start bit + data bit + parity bit + stop bit.

Loopback Mode

The S3C2443X UART provides a test mode referred to as the Loopback mode, to aid in isolating faults in the communication link. This mode structurally enables the connection of RXD and TXD in the UART. In this mode, therefore, transmitted data is received to the receiver, via RXD. This feature allows the processor to verify the internal transmit and to receive the data path of each SIO channel. This mode can be selected by setting the loopback bit in the UART control register (UCONn).

Infrared (IR) Mode

The S3C2443X UART block supports infrared (IR) transmission and reception, which can be selected by setting the Infrared-mode bit in the UART line control register (ULCONn). Figure 15-4 illustrates how to implement the IR mode.

In IR transmit mode, the transmit pulse comes out at a rate of 3/16, the normal serial transmit rate (when the transmit data bit is zero); In IR receive mode, the receiver must detect the 3/16 pulsed period to recognize a zero value (see the frame timing diagrams shown in Figure 15-6 and 13-7).

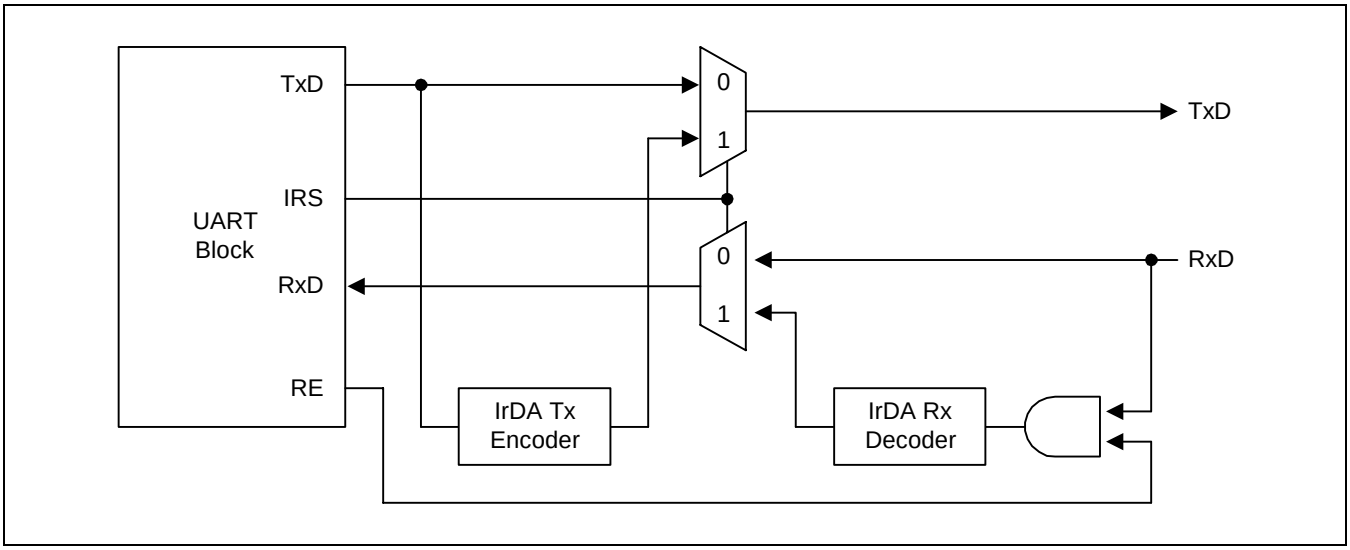


Figure 15-4. IrDA Function Block Diagram

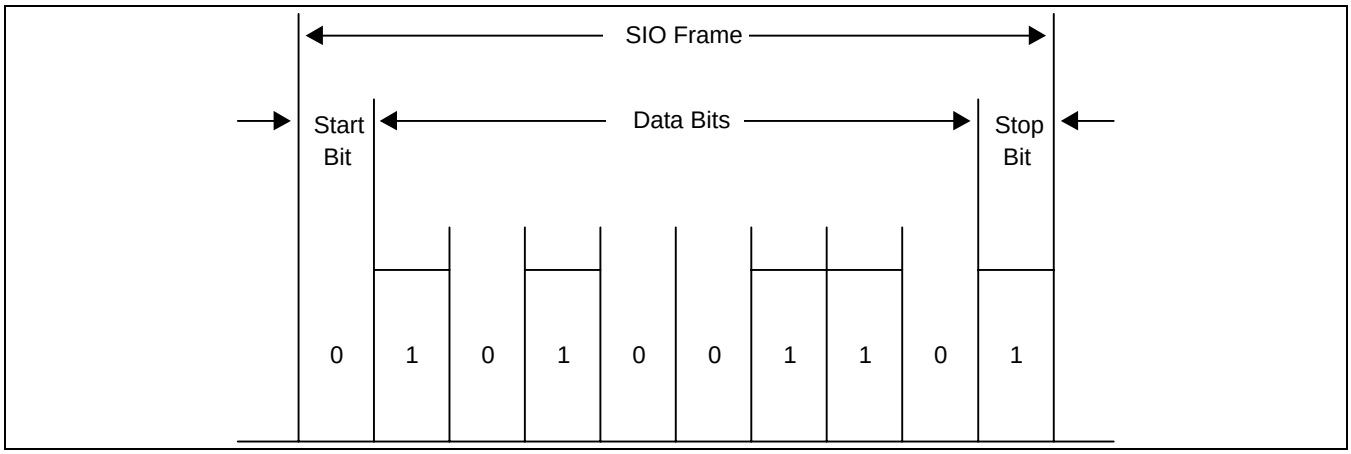


Figure 15-5. Serial I/O Frame Timing Diagram (Normal UART)

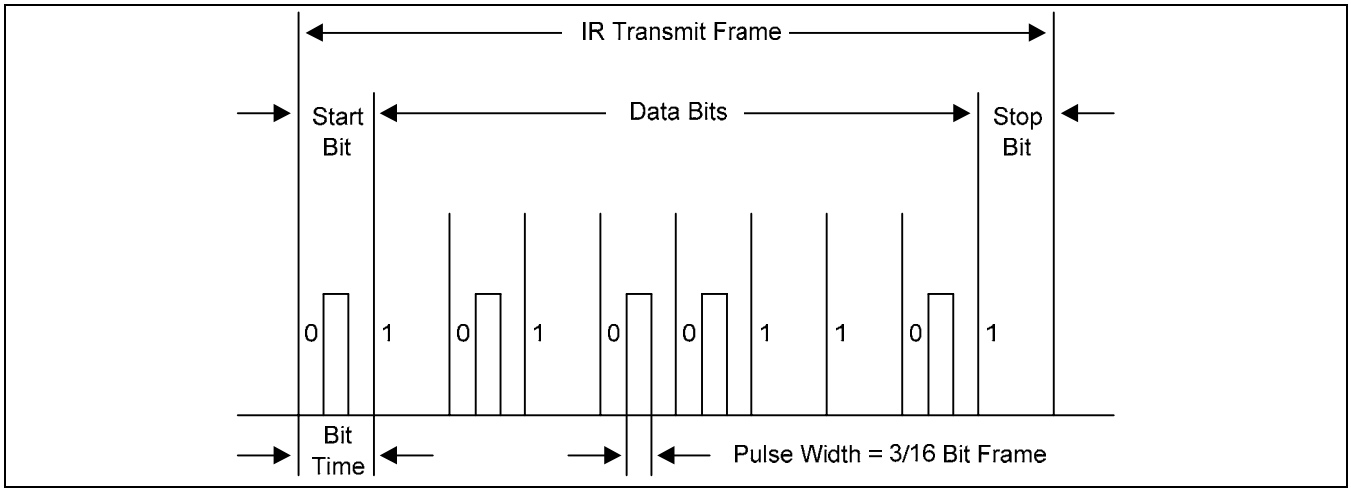


Figure 15-6. Infrared Transmit Mode Frame Timing Diagram

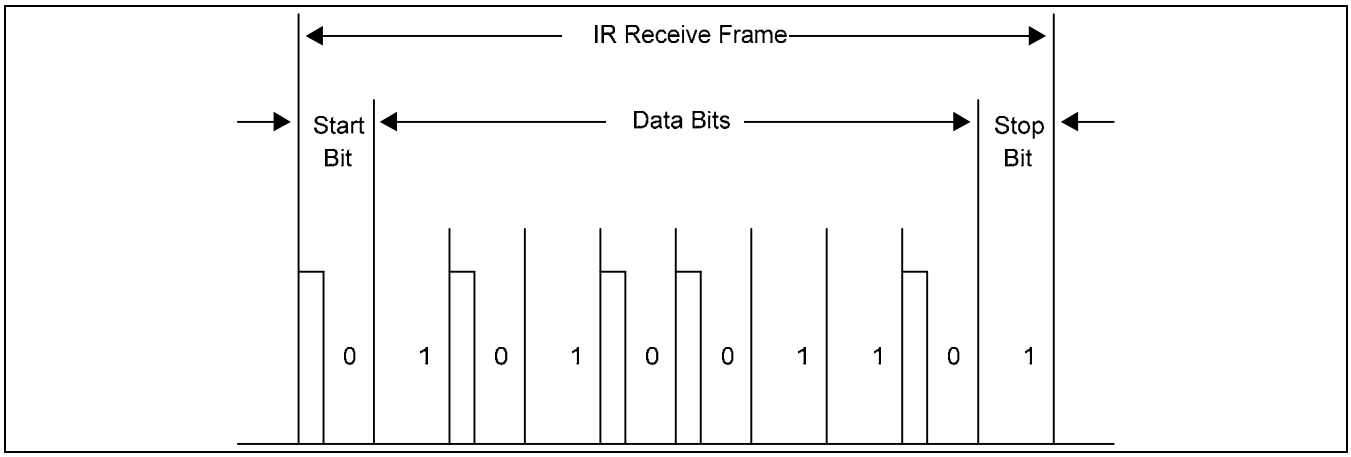


Figure 15-7. Infrared Receive Mode Frame Timing Diagram

UART SPECIAL REGISTERS

UART LINE CONTROL REGISTER

There are four UART line control registers including ULCON0, ULCON1, ULCON2 and ULCON3 in the UART block.

Register	Address	R/W	Description	Reset Value
ULCON0	0x50000000	R/W	UART channel 0 line control register	0x00
ULCON1	0x50004000	R/W	UART channel 1 line control register	0x00
ULCON2	0x50008000	R/W	UART channel 2 line control register	0x00
ULCON3	0x5000C000	R/W	UART channel 3 line control register	0x00

ULCONn	Bit	Description	Initial State
Reserved	[7]	–	0
Infrared Mode	[6]	Determine whether or not to use the Infrared mode. 0 = Normal mode operation 1 = Infrared Tx/Rx mode	0
Parity Mode	[5:3]	Specify the type of parity generation and checking during UART transmit and receive operation. 0xx = No parity 100 = Odd parity 101 = Even parity 110 = Parity forced/checked as 1 111 = Parity forced/checked as 0	000
Number of Stop Bit	[2]	Specify how many stop bits are to be used for end-of-frame signal. 0 = One stop bit per frame 1 = Two stop bit per frame	0
Word Length	[1:0]	Indicate the number of data bits to be transmitted or received per frame. 00 = 5-bits 01 = 6-bits 10 = 7-bits 11 = 8-bits	00

UART CONTROL REGISTER

There are four UART control registers including UCON0, UCON1, UCON2 and UCON3 in the UART block.

Register	Address	R/W	Description	Reset Value
UCON0	0x50000004	R/W	UART channel 0 control register	0x00
UCON1	0x50004004	R/W	UART channel 1 control register	0x00
UCON2	0x50008004	R/W	UART channel 2 control register	0x00
UCON3	0x5000C004	R/W	UART channel 3 control register	0x00

UART CONTROL REGISTER

UCONn	Bit	Description	Initial State
Clock Selection	[11:10]	Select PCLK, EXTUARTCLK(External UART clock) or divided EPLL clock for source clock of the UART. DIV_VAL[1)] = (SRCCLK / (buadrate x 16)) - 1 SRCCLK is selected as follows 00, 10 : PCLK 01 : EXTUARTCLK 11 : divided EPLL clock Refer to the Clock Source Control Register in system controller. EXTUARTCLK and EPLL clock should be smaller than PCLK.	0
Tx Interrupt Type	[9]	Interrupt request type. 0 = Pulse (Interrupt is requested as soon as the Tx buffer becomes empty in Non-FIFO mode or reaches Tx FIFO Trigger Level in FIFO mode.) 1 = Level (Interrupt is requested while Tx buffer is empty in Non-FIFO mode or reaches Tx FIFO Trigger Level in FIFO mode.)	0
Rx Interrupt Type	[8]	Interrupt request type. 0 = Pulse (Interrupt is requested the instant Rx buffer receives the data in Non-FIFO mode or reaches Rx FIFO Trigger Level in FIFO mode.) 1 = Level (Interrupt is requested while Rx buffer is receiving data in Non-FIFO mode or reaches Rx FIFO Trigger Level in FIFO mode.)	0
Rx Time Out Enable	[7]	Enable/Disable Rx time out interrupt when UART FIFO is enabled. The interrupt is a receive interrupt. 0 = Disable 1 = Enable	0
Rx Error Status Interrupt Enable	[6]	Enable the UART to generate an interrupt upon an exception, such as a break, frame error, parity error, or overrun error during a receive operation. 0 = Do not generate receive error status interrupt. 1 = Generate receive error status interrupt.	0

UART CONTROL REGISTER (Continued)

UCONn	Bit	Description	Initial State
Loopback Mode	[5]	Setting loopback bit to 1 causes the UART to enter the loopback mode. This mode is provided for test purposes only. 0 = Normal operation 1 = Loopback mode	0
Send break signal	[4]	Setting this bit causes the UART to send a break during 1 frame time. This bit is auto-cleared after sending the break signal 0 = Normal transmit 1 = Send break signal	0
Transmit Mode*	[3:2]	Determine which function is currently able to write Tx data to the UART transmit buffer register. 00 = Disable 01 = Interrupt request or polling mode 10 = DMA request(request signal 0) 11 = DMA request(request signal 1)	00
Receive Mode	[1:0]	Determine which function is currently able to read data from UART receive buffer register. 00 = Disable 01 = Interrupt request or polling mode 10 = DMA request(request signal 0) 11 = DMA request(request signal 1)	00

NOTE: When the UART does not reach the FIFO trigger level and does not receive data during 3 words time in DMA receive mode with FIFO, the Rx interrupt will be generated (receive time out), and the users should check the FIFO status and read out the rest.

NOTE: If Tx DMA request signal were 0, Rx DMA request signal should be 1. They can't share request signal 0 or 1 in common. (UCONn[3:2], UCONn[1:0]) **=** ("10b", "11b") or ("11b", "10b")

UART FIFO CONTROL REGISTER

There are four UART FIFO control registers including UFCON0, UFCON1, UFCON2 and UFCON3 in the UART block.

Register	Address	R/W	Description	Reset Value
UFCON0	0x50000008	R/W	UART channel 0 FIFO control register	0x0
UFCON1	0x50004008	R/W	UART channel 1 FIFO control register	0x0
UFCON2	0x50008008	R/W	UART channel 2 FIFO control register	0x0
UFCON3	0x5000C008	R/W	UART channel 3 FIFO control register	0x0

UFCONn	Bit	Description	Initial State
Tx FIFO Trigger Level	[7:6]	Determine the trigger level of transmit FIFO. 00 = Empty 01 = 16-byte 10 = 32-byte 11 = 48-byte	00
Rx FIFO Trigger Level	[5:4]	Determine the trigger level of receive FIFO. 00 = 1-byte 01 = 8-byte 10 = 16-byte 11 = 32-byte	00
Reserved	[3]	–	0
Tx FIFO Reset	[2]	Auto-cleared after resetting FIFO 0 = Normal 1 = Tx FIFO reset	0
Rx FIFO Reset	[1]	Auto-cleared after resetting FIFO 0 = Normal 1 = Rx FIFO reset	0
FIFO Enable	[0]	0 = Disable 1 = Enable	0

NOTE: When the UART does not reach the FIFO trigger level and does not receive data during 3 words time in DMA receive mode with FIFO, the Rx interrupt will be generated (receive time out), and the users should check the FIFO status and read out the rest.

UART MODEM CONTROL REGISTER

There are three UART MODEM control registers including UMCON0 and UMCON1 in the UART block.

Register	Address	R/W	Description	Reset Value
UMCON0	0x5000000C	R/W	UART channel 0 Modem control register	0x0
UMCON1	0x5000400C	R/W	UART channel 1 Modem control register	0x0
UMCON2	0x5000800C	R/W	UART channel 2 Modem control register	0x0
Reserved	0x5000C00C	–	Reserved	Undef

UMCONn	Bit	Description	Initial State
RTS trigger Level	[7:5]	When AFC bit is enabled, these bits determine when to inactivate nRTS signal. 000 = When RX FIFO contains 63 bytes. 001 = When RX FIFO contains 56 bytes. 010 = When RX FIFO contains 48 bytes. 011 = When RX FIFO contains 40 bytes. 100 = When RX FIFO contains 32 bytes. 101 = When RX FIFO contains 24 bytes. 110 = When RX FIFO contains 16 bytes. 111 = When RX FIFO contains 8 bytes.	000
Auto Flow Control (AFC)	[4]	0 = Disable 1 = Enable	0
Reserved	[3:1]	These bits must be 0's	00
Request to Send	[0]	If AFC bit is enabled, this value will be ignored. In this case the S3C2443X will control nRTS automatically. If AFC bit is disabled, nRTS must be controlled by software. 0 = 'H' level (Inactivate nRTS) 1 = 'L' level (Activate nRTS)	0

NOTES:

1. UART 3 does not support AFC function, because the S3C2443X has no nRTS3 and nCTS3.
2. If AFC bit is enabled and Time-out bit is disabled, RTS trigger level must be lager than Rx FIFO trigger level.

UART TX/RX STATUS REGISTER

There are four UART Tx/Rx status registers including UTRSTAT0, UTRSTAT1, UTRSTAT2 and UTRSTAT3 in the UART block.

Register	Address	R/W	Description	Reset Value
UTRSTAT0	0x50000010	R	UART channel 0 Tx/Rx status register	0x6
UTRSTAT1	0x50004010	R	UART channel 1 Tx/Rx status register	0x6
UTRSTAT2	0x50008010	R	UART channel 2 Tx/Rx status register	0x6
UTRSTAT3	0x5000C010	R	UART channel 3 Tx/Rx status register	0x6

UTRSTATn	Bit	Description	Initial State
Transmitter empty	[2]	Set to 1 automatically when the transmit buffer register has no valid data to transmit and the transmit shift register is empty. 0 = Not empty 1 = Transmitter (transmit buffer & shifter register) empty	1
Transmit buffer empty	[1]	Set to 1 automatically when transmit buffer register is empty. 0 =The buffer register is not empty 1 = Empty (In Non-FIFO mode, Interrupt or DMA is requested. In FIFO mode, Interrupt or DMA is requested, when Tx FIFO Trigger Level is set to 00 (Empty)) If the UART uses the FIFO, users should check Tx FIFO Count bits and Tx FIFO Full bit in the UFSTAT register instead of this bit.	1
Receive buffer data ready	[0]	Set to 1 automatically whenever receive buffer register contains valid data, received over the RXDn port. 0 = Empty 1 = The buffer register has a received data (In Non-FIFO mode, Interrupt or DMA is requested) If the UART uses the FIFO, users should check Rx FIFO Count bits and Rx FIFO Full bit in the UFSTAT register instead of this bit.	0

UART ERROR STATUS REGISTER

There are four UART Rx error status registers including UERSTAT0, UERSTAT1, UERSTAT2 and UERSTAT3 in the UART block.

Register	Address	R/W	Description	Reset Value
UERSTAT0	0x50000014	R	UART channel 0 Rx error status register	0x0
UERSTAT1	0x50004014	R	UART channel 1 Rx error status register	0x0
UERSTAT2	0x50008014	R	UART channel 2 Rx error status register	0x0
UERSTAT3	0x5000C014	R	UART channel 3 Rx error status register	0x0

UERSTATn	Bit	Description	Initial State
Break Detect	[3]	Set to 1 automatically to indicate that a break signal has been received. 0 = No break receive 1 = Break receive (Interrupt is requested.)	0
Frame Error	[2]	Set to 1 automatically whenever a frame error occurs during receive operation. 0 = No frame error during receive 1 = Frame error (Interrupt is requested.)	0
Parity Error	[1]	Set to 1 automatically whenever a parity error occurs during receive operation. 0 = No parity error during receive 1 = Parity error (Interrupt is requested.)	0
Overrun Error	[0]	Set to 1 automatically whenever an overrun error occurs during receive operation. 0 = No overrun error during receive 1 = Overrun error (Interrupt is requested.)	0

NOTE: These bits (UERSATn[3:0]) are automatically cleared to 0 when the UART error status register is read.

UART FIFO STATUS REGISTER

There are four UART FIFO status registers including UFSTAT0, UFSTAT1 UFSTAT2 and UFSTAT3 in the UART block.

Register	Address	R/W	Description	Reset Value
UFSTAT0	0x50000018	R	UART channel 0 FIFO status register	0x00
UFSTAT1	0x50004018	R	UART channel 1 FIFO status register	0x00
UFSTAT2	0x50008018	R	UART channel 2 FIFO status register	0x00
UFSTAT3	0x5000C018	R	UART channel 3 FIFO status register	0x00

UFSTATn	Bit	Description	Initial State
Reserved	[15]		0
Tx FIFO Full	[14]	Set to 1 automatically whenever transmit FIFO is full during transmit operation 0 = 0-byte ≤ Tx FIFO data ≤ 63-byte 1 = Full	0
Tx FIFO Count	[13:8]	Number of data in Tx FIFO	0
Reserved	[7]	–	0
Rx FIFO Full	[6]	Set to 1 automatically whenever receive FIFO is full during receive operation 0 = 0-byte ≤ Rx FIFO data ≤ 63-byte 1 = Full	0
Rx FIFO Count	[5:0]	Number of data in Rx FIFO	0

UART MODEM STATUS REGISTER

There are three UART modem status registers including UMSTAT0, UMSTAT1 in the UART block.

Register	Address	R/W	Description	Reset Value
UMSTAT0	0x5000001C	R	UART channel 0 modem status register	0x0
UMSTAT1	0x5000401C	R	UART channel 1 modem status register	0x0
UMSTAT2	0x5000801C	R	UART channel 2 modem status register	0x0
Reserved	0x5000C01C	–	Reserved	Undef

UMSTAT0	Bit	Description	Initial State
Delta CTS	[4]	Indicate that the nCTS input to the S3C2443X has changed state since the last time it was read by CPU. (Refer to Figure 15-8.) 0 = Has not changed 1 = Has changed	0
Reserved	[3:1]	–	0
Clear to Send	[0]	0 = CTS signal is not activated (nCTS pin is high) 1 = CTS signal is activated (nCTS pin is low)	0

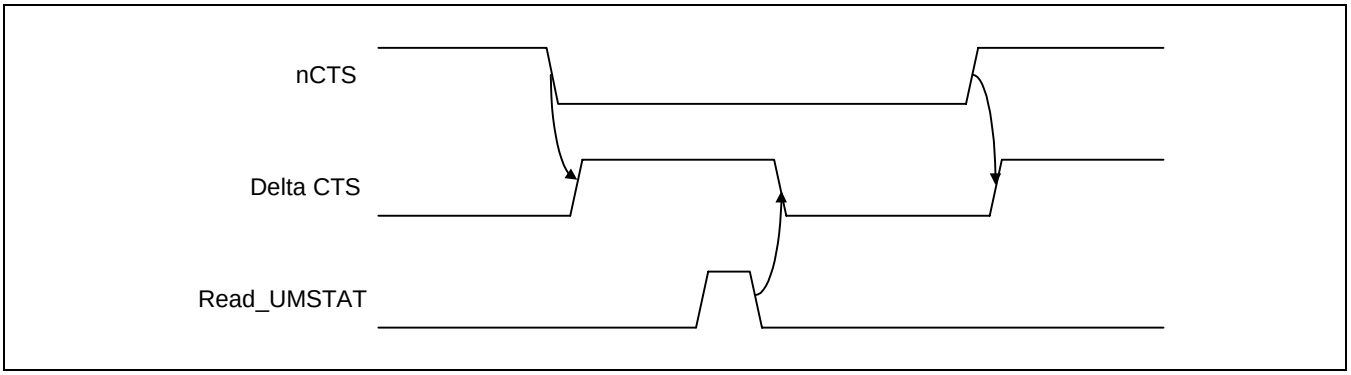


Figure 15-8. nCTS and Delta CTS Timing Diagram

UART TRANSMIT BUFFER REGISTER (HOLDING REGISTER & FIFO REGISTER)

There are four UART transmit buffer registers including UTXH0, UTXH1, UTXH2 and UTXH3 in the UART block. UTXHn has an 8-bit data for transmission data.

Register	Address	R/W	Description	Reset Value
UTXH0	0x50000020(L) 0x50000023(B)	W (by byte)	UART channel 0 transmit buffer register	–
UTXH1	0x50004020(L) 0x50004023(B)	W (by byte)	UART channel 1 transmit buffer register	–
UTXH2	0x50008020(L) 0x50008023(B)	W (by byte)	UART channel 2 transmit buffer register	–
UTXH3	0x5000C020(L) 0x5000C023(B)	W (by byte)	UART channel 3 transmit buffer register	–

UTXHn	Bit	Description	Initial State
TXDATAn	[7:0]	Transmit data for UARTn	–

NOTE: (L): The endian mode is Little endian.
(B): The endian mode is Big endian.

UART RECEIVE BUFFER REGISTER (HOLDING REGISTER & FIFO REGISTER)

There are four UART receive buffer registers including URXH0, URXH1, URXH2 and URXH3 in the UART block. URXHn has an 8-bit data for received data.

Register	Address	R/W	Description	Reset Value
URXH0	0x50000024(L) 0x50000027(B)	R (by byte)	UART channel 0 receive buffer register	–
URXH1	0x50004024(L) 0x50004027(B)	R (by byte)	UART channel 1 receive buffer register	–
URXH2	0x50008024(L) 0x50008027(B)	R (by byte)	UART channel 2 receive buffer register	–
URXH3	0x5000C024(L) 0x5000C027(B)	R (by byte)	UART channel 3 receive buffer register	–

URXHn	Bit	Description	Initial State
RXDATAn	[7:0]	Receive data for UARTn	–

NOTE: When an overrun error occurs, the URXHn must be read. If not, the next received data will also make an overrun error, even though the overrun bit of UERSTATn had been cleared.

UART BAUD RATE DIVISOR REGISTER

There are four UART baud rate divisor registers including UBRDIV0, UBRDIV1, UBRDIV2 and UBRDIV3 in the UART block. The value stored in the baud rate divisor register (UBRDIVn) and dividing slot register(UDIVSLOTn), are used to determine the serial Tx/Rx clock rate (baud rate) as follows:

DIV_VAL = UBRDIVn + (num of 1's in UDIVSLOTn)/16
= (SRCCLK / (baud rate x 16)) –1

(SRCCLK : PCLK, EXTUARTCLK or divided EPLL clock)

Where, DIV_VAL should be from 1 to (2^{16}-1), but can be set zero only using the EXTUARTCLK. The EXTUARTCLK and divided EPLL clock should be smaller than PCLK.

Using UDIVSLOT which is the factor of floating point divisor, you can make more accurate baud rate.

For example, if the baud rate is 115200 bps and SRCCLK is 40 MHz, UBRDIVn and UDIVSLOTn are :

DIV_VAL = (40000000 / (115200 x 16)) -1
= 21.7 -1
= 20.7

* **UBRDIVn** = 20
(integer part of DIV_VAL)

(num of 1's in UDIVSLOTn)/16 = 0.7
(num of 1's in UDIVSLOTn) = 11
* **UDIVSLOTn** = 0xEEEA(**111**0_**111**0_**111**0_**1**0**1**0b), 0xDDD5(**11**0**1**_**11**0**1**_**11**0**1**_**1**0**1**0b) or etc.
(floating point part of DIV_VAL)

As a result, DIV_VAL = 20.6875

We recommend to select UDIVSLOTn as following table.

Table 15-2 Recommended value table of DIVSLOTn register

Num of 1's	UDIVSLOTn	Num of 1's	UDIVSLOTn
0	0x0000(0000_0000_0000_0000b)	8	0x5555(0101_0101_0101_0101b)
1	0x0080(0000_0000_0000_1000b)	9	0xD555(1101_0101_0101_0101b)
2	0x0808(0000_1000_0000_1000b)	10	0xD5D5(1101_0101_1101_0101b)
3	0x0888(0000_1000_1000_1000b)	11	0xDDD5(1101_1101_1101_0101b)
4	0x2222(0010_0010_0010_0010b)	12	0xDDDD(1101_1101_1101_1101b)
5	0x4924(0100_1001_0010_0100b)	13	0xDFDD(1101_1111_1101_1101b)
6	0x4A52(0100_1010_0101_0010b)	14	0xDFDF(1101_1111_1101_1111b)
7	0x54AA(0101_0100_1010_1010b)	15	0xFFDF(1111_1111_1101_1111b)

Register	Address	R/W	Description	Reset Value
UBRDIV0	0x50000028	R/W	Baud rate divisior(integer place) register 0	–
UBRDIV1	0x50004028	R/W	Baud rate divisior(integer place) register 1	–
UBRDIV2	0x50008028	R/W	Baud rate divisior(integer place) register 2	–
UBRDIV3	0x5000C028	R/W	Baud rate divisior(integer place) register 3	–

UBRDIVn	Bit	Description	Initial State
UBRDIV	[15:0]	Baud rate division value of integer part UBRDIVn >0	–

Register	Address	R/W	Description	Reset Value
UDIVSLOT0	0x5000002C	R/W	Baud rate divisior(decimal place) register 0	0x0000
UDIVSLOT1	0x5000402C	R/W	Baud rate divisior(decimal place) register 1	0x0000
UDIVSLOT2	0x5000802C	R/W	Baud rate divisior(decimal place) register 2	0x0000
UDIVSLOT3	0x5000C02C	R/W	Baud rate divisior(decimal place) register 3	0x0000

UDIVSLOTn	Bit	Description	Initial State
UDIVSLOT	[15:0]	Select the slot number in table 15-2	–

NOTES

16 USB HOST CONTROLLER

OVERVIEW

S3C2443X supports 2-port USB host interface as follows:

- OHCI Rev 1.0 compatible
- USB Rev1.1 compatible
- Two down stream ports
- Support for both LowSpeed and FullSpeed USB devices

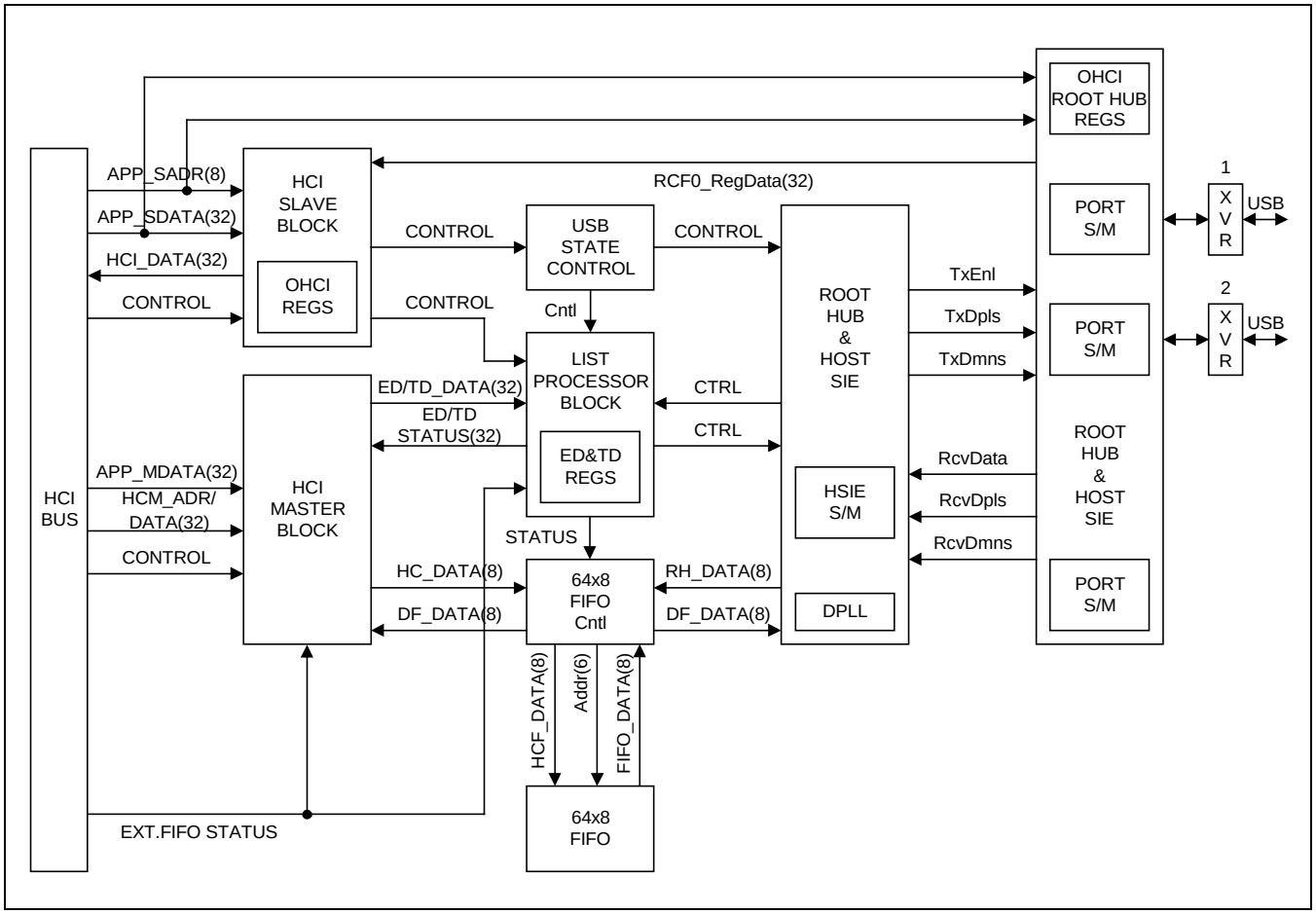


Figure 16-1. USB Host Controller Block Diagram

USB HOST CONTROLLER SPECIAL REGISTERS

The S3C2443X USB host controller complies with OHCI Rev 1.0. Refer to Open Host Controller Interface Rev 1.0 specification for detail information.

Table 16-1. OHCI Registers for USB Host Controller

Register	Base Address	R/W	Description	Reset Value
HcRevision	0x49000000	–	Control and status group	–
HcControl	0x49000004	–		–
HcCommonStatus	0x49000008	–		–
HcInterruptStatus	0x4900000C	–		–
HcInterruptEnable	0x49000010	–		–
HcInterruptDisable	0x49000014	–		–
HcHCCA	0x49000018	–	Memory pointer group	–
HcPeriodCuttentED	0x4900001C	–		–
HcControlHeadED	0x49000020	–		–
HcControlCurrentED	0x49000024	–		–
HcBulkHeadED	0x49000028	–		–
HcBulkCurrentED	0x4900002C	–		–
HcDoneHead	0x49000030	–		–
HcRmInterval	0x49000034	–	Frame counter group	–
HcFmRemaining	0x49000038	–		–
HcFmNumber	0x4900003C	–		–
HcPeriodicStart	0x49000040	–		–
HcLSThreshold	0x49000044	–		–
HcRhDescriptorA	0x49000048	–	Root hub group	–
HcRhDescriptorB	0x4900004C	–		–
HcRhStatus	0x49000050	–		–
HcRhPortStatus1	0x49000054	–		–
HcRhPortStatus2	0x49000058	–		–

17 USB 2.0 FUNCTION

OVERVIEW

The Samsung USB 2.0 Controller is designed to aid the rapid implementation of the USB 2.0 peripheral device. The controller supports both High and Full speed mode. Using the standard UTMI interface and AHB interface the USB 2.0 Controller can support up to 9 Endpoints (including Endpoint0) with programmable Interrupt, Bulk and Isochronous transfer mode.

FEATURE

— Compliant to USB 2.0 specification
— Supports FS/HS dual mode operation
— EP 0 FIFO: 64 bytes.
— EP 1/2/3/4 FIFO: 512 bytes double buffering
— EP 5/6/7/8 FIFO: 1024 bytes double buffering
— Convenient Debugging
— Support Interrupt, Bulk, Isochronous Transfer

BLOCK DIAGRAM

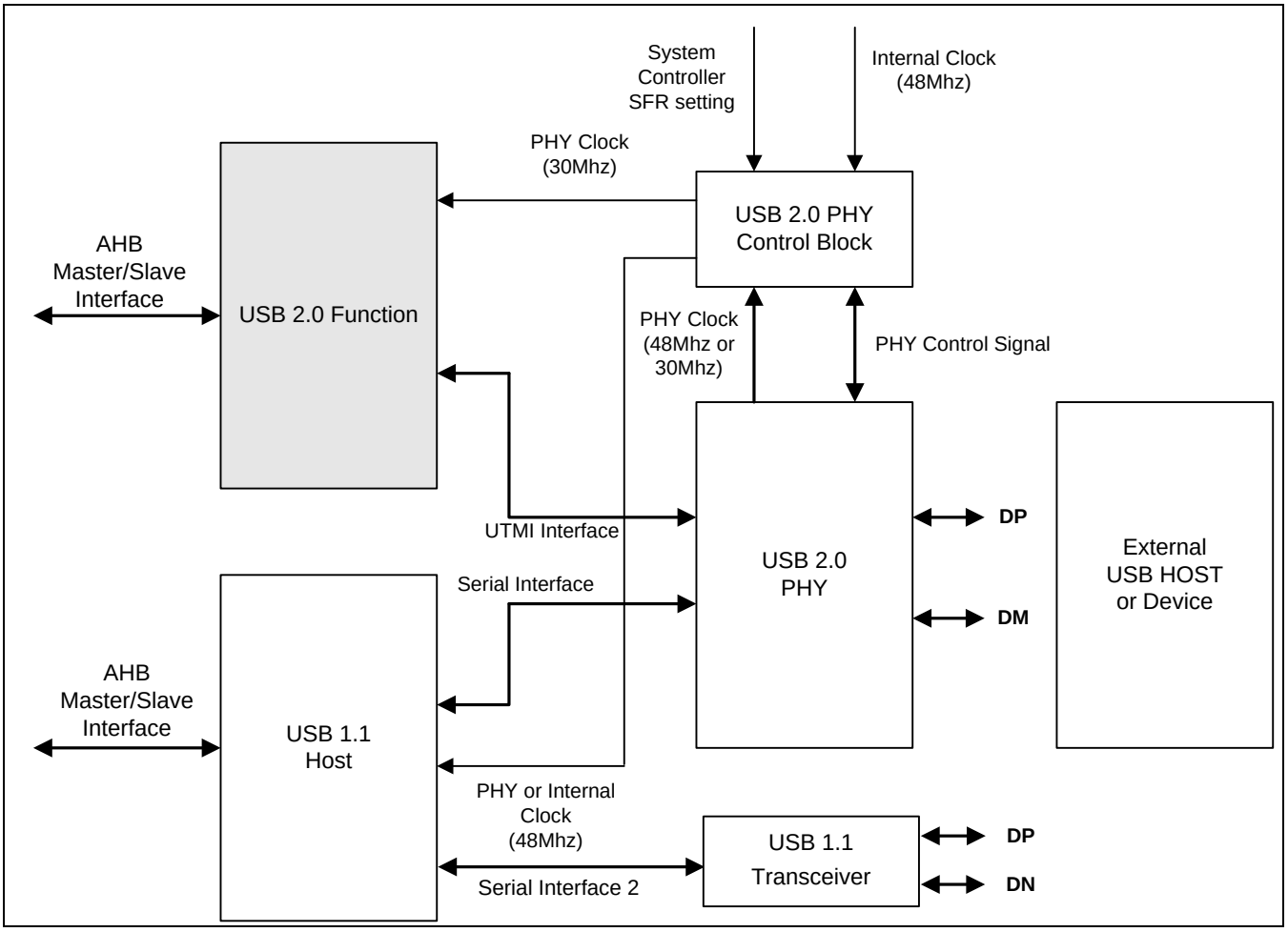


Figure 17-1. USB2.0 Block Diagram

USB2.0 Function has a AHB Slave which provides the microcontroller with read and write access to the Control and Status Registers. And also Function has an AHB Master to enable the link to transfer data on the AHB. The S3C2443x USB system shown as Figure 17-1, can be configured as following :

1. USB 1.1 Host 1 Port & USB 2.0 OTG 1 Port
2. USB 1.1 Host 2 Ports

TO ACTIVATE USB PORT1 FOR USB 2.0 FUNCTION

USB Function block of S3C2443X shares USB PORT1 with USB Host block. To activate USB PORT1 for USB Function, see USB control registers in System Controller Guide

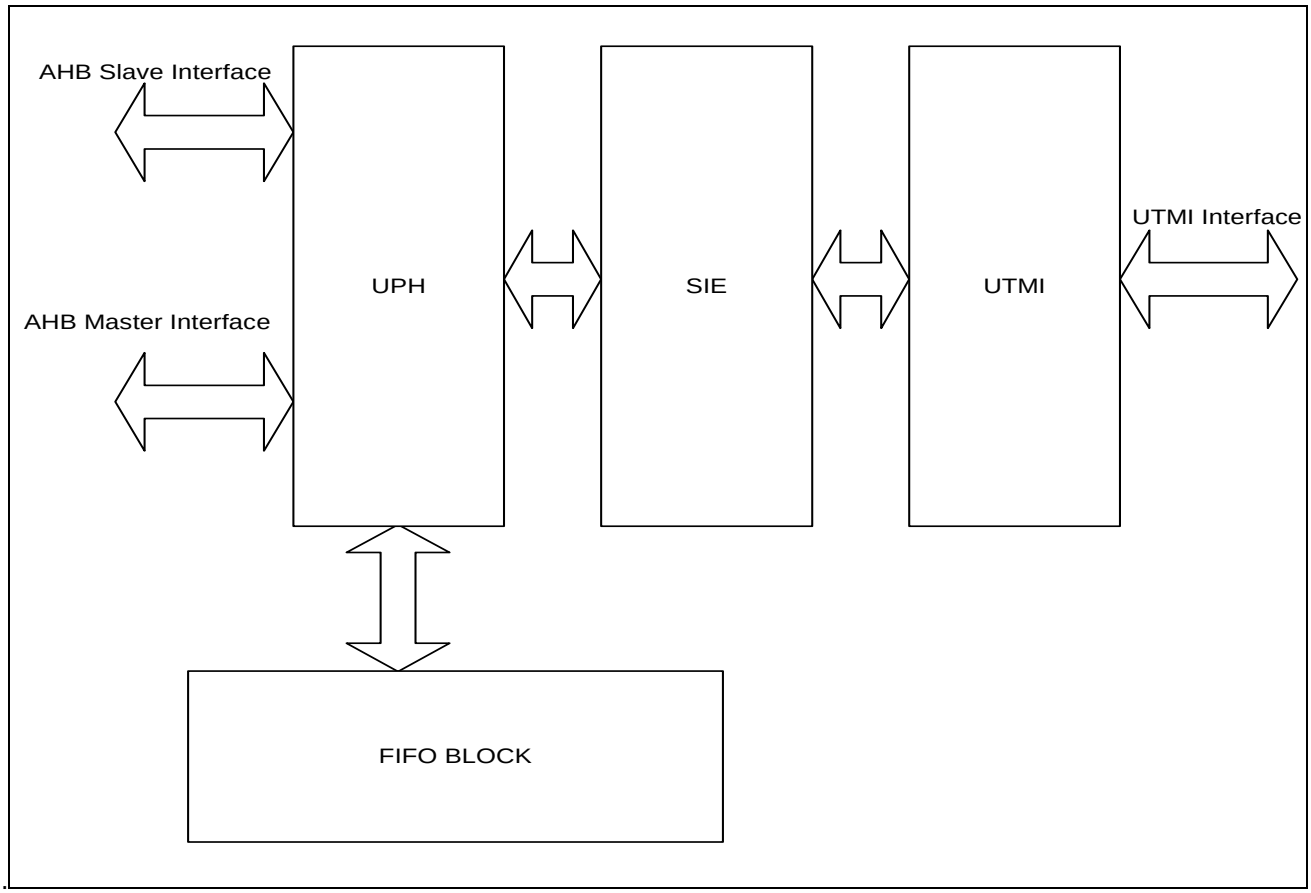


Figure 17-2. USB2.0 Function Block Diagram

SIE (SERIAL INTERFACE ENGINE)

This block handles NRZI decoding/encoding, CRC generation and checking, and bit-stuffing. It also provides the interface signals for USB Transceiver..

UPH (UNIVERSAL PROTOCOL HANDLER)

This block includes state machines and fifo control, control/status register and DMA control block of each direction endpoint.

UTMI (USB 2.0 TRANSCEIVER MACROCELL INTERFACE)

UTMI interface block connects 16 bit data bus and control signals to USB 2.0 PHY.

USB 2.0 FUNCTION CONTROLLER SPECIAL REGISTERS

The USB 2.0 controller includes several 16-bit registers for the endpoint programming and debugging. The registers can be grouped into two categories. Few of the indexed registers are related to endpoint 0, but most of them are utilized for the control and status monitoring of each data endpoint, including FIFO control and packet size configuration. The buffer register for TX/RX data buffering also belong to the indexed register/

The non-indexed registers are mainly used for the control and status checking of the system. The control and status registers of endpoint0 belong to these non-indexed registers.

Table 17-1. Non-Indexed Registers

Register	Address	R/W	Description
IR	0x4980_0000	R/W	Index Register
EIR	0x4980_0004	R/W	Endpoint Interrupt Register
EIER	0x4980_0008	R/W	Endpoint Interrupt Enable Register
FAR	0x4980_000C	R	Function Address Register
FNR	0x4980_0010	R	Frame Number Register
EDR	0x4980_0014	R/W	Endpoint Direction Register
TR	0x4980_0018	R/W	Test Register
SSR	0x4980_001C	R/W	System Status Register
SCR	0x4980_0020	R/W	System Control Register
EP0SR	0x4980_0024	R/W	EP0 Status Register
EP0CR	0x4980_0028	R/W	EP0 Control Register
EP0BR	0x4980_0060	R/W	EP0 Buffer Register
EP1BR	0x4980_0064	R/W	EP1 Buffer Register
EP2BR	0x4980_0068	R/W	EP2 Buffer Register
EP3BR	0x4980_006C	R/W	EP3 Buffer Register
EP4BR	0x4980_0070	R/W	EP4 Buffer Register
EP5BR	0x4980_0074	R/W	EP5 Buffer Register
EP6BR	0x4980_0078	R/W	EP6 Buffer Register
EP7BR	0x4980_007C	R/W	EP7 Buffer Register
EP8BR	0x4980_0080	R/W	EP8 Buffer Register
FCON	0x4980_0100	R/W	Burst FIFO-DMA Control
FSTAT	0x4980_0104	R/W	Burst FIFO status

Table 17-2. Indexed Registers

Register	Address	R/W	Description
ESR	0x4980_002C	R/W	Endpoints Status Register
ECR	0x4980_0030	R/W	Endpoints Control Register
BRCR	0x4980_0034	R	Byte Read Count Register
BWCR	0x4980_0038	R/W	Byte Write Count Register
MPR	0x4980_003C	R/W	Max Packet Register
DCR	0x4980_0040	R/W	DMA Control Register
DTCR	0x4980_0044	R/W	DMA Transfer Counter Register
DFCR	0x4980_0048	R/W	DMA FIFO Counter Register
DTTCR1	0x4980_004C	R/W	DMA Total Transfer Counter1 Register
DTTCR2	0x4980_0050	R/W	DMA Total Transfer Counter2 Register
MICR	0x4980_0084	R/W	Master Interface Control Register
MBAR	0x4980_0088	R/W	Memory Base Address Register
MCAR	0x4980_008C	R/W	Memory Current Address Register

REGISTERS

INDEX REGISTER (IR)

The index register is used for indexing a specific endpoint. In most cases, setting the index register value should precede any other operation.

Register	Address	R/W	Description	Reset Value
IR	0x4980_0000	R/W	Index Register	0x00

IR	Bit	R/W	Description	Initial State
	[7:4]		Reserved	0000
INDEX	[3:0]	R/W	Endpoint Number Select (0~6) 0000 = Endpoint0 0001 = Endpoint1 0010 = Endpoint2 0011 = Endpoint3 0100 = Endpoint4 0101 = Endpoint5 0110 = Endpoint6 0111 = Endpoint7 1000 = Endpoint8	0000

ENDPOINT INTERRUPT REGISTER (EIR)

The endpoint interrupt register lets the MCU knows what endpoint generates the interrupt. The source of an interrupt could be various, but, when an interrupt is detected, the endpoint status register should be checked to identify if it's related to specific endpoint. Clearing the bits can be accomplished by writing "1" to the bit position where the interrupt is detected.

Register	Address	R/W	Description	Reset Value
EIR	0x4980_0004	R/C	Endpoint Interrupt Register	0x00

EIR	Bit	R/W	Description	Initial State
	[31:9]		Reserved	0
EP8I	[8]	R/C	Endpoint 8 Interrupt Flag	0
EP7I	[7]	R/C	Endpoint 7 Interrupt Flag	0
EP6I	[6]	R/C	Endpoint 6 Interrupt Flag	0
EP5I	[5]	R/C	Endpoint 5 Interrupt Flag	0
EP4I	[4]	R/C	Endpoint 4 Interrupt Flag	0
EP3I	[3]	R/C	Endpoint 3 Interrupt Flag	0
EP2I	[2]	R/C	Endpoint 2 Interrupt Flag	0
EP1I	[1]	R/C	Endpoint 1 Interrupt Flag	0
EP0I	[0]	R/C	Endpoint 0 Interrupt Flag	0

ENDPOINT INTERRUPT ENABLE REGISTER (EIER)

Pairing with interrupt register, this register enables interrupt for each endpoints.

Register	Address	R/W	Description	Reset Value
EIER	0x4980_0008	R/W	Endpoint Interrupt Enable Register	0x00

EIER	Bit	R/W	Description	Initial State
	[31:9]		Reserved	
EP8IE	[8]	R/W	Endpoint 8 Interrupt Enable Flag	0
EP7IE	[7]	R/W	Endpoint 7 Interrupt Enable Flag	0
EP6IE	[6]	R/W	Endpoint 6 Interrupt Enable Flag	0
EP5IE	[5]	R/W	Endpoint 5 Interrupt Enable Flag	0
EP4IE	[4]	R/W	Endpoint 4 Interrupt Enable Flag	0
EP3IE	[3]	R/W	Endpoint 3 Interrupt Enable Flag	0
EP2IE	[2]	R/W	Endpoint 2 Interrupt Enable Flag	0
EP1IE	[1]	R/W	Endpoint 1 Interrupt Enable Flag	0
EP0IE	[0]	R/W	Endpoint 0 Interrupt Enable Flag 1 = EP0 Interrupt flag enable 0 = EP0 Interrupt flag disable	0

FUNCTION ADDRESS REGISTER (FAR)

This register holds the address of USB device.

Register	Address	R/W	Description	Reset Value
FAR	0x4980_000C	R	Function Address Register	32 bits

FAR	Bit	R/W	Description	Initial State
	[31:7]		Reserved	
FA	[6:0]	R	MCU can read a unique USB function address from this register. The address is transferred from USB Host through “set_address” command.	7’h0

FRAME NUMBER REGISTER (FNR)

The frame number register is used for the isochronous transaction.

Register	Address	R/W	Description	Reset Value
FNR	0x4980_0010	R	Frame Number Register	32 bits

FNR	Bit	R/W	Description	Initial State
	[31:15]		Reserved	
FTL	[14]	R	Frame Timer Lock FTL is activated when the device frame timer is locked to the host frame timer. When this bit is set, Frame Number is valid. This bit is set by USB after device receives two valid SOF.	0
SM	[13]	R	SOF Missing SM is activated when frame timer locking between device frame timer and Host frame timer fails.	0
	[12:11]		Reserved	
FN	[10:0]	R	[10:0] bits store the frame count number, which increases per every SOF packet.	0

ENDPOINT DIRECTION REGISTER (EDR)

USB 2.0 Core supports IN/OUT direction control for each endpoint. This direction can't be changed dynamically. Only by new enumeration, the direction can be altered. Since the endpoint 0 is bi-directional, there is no direction bit assigned to it.

Register	Address	R/W	Description	Reset Value
EDR	0x4980_0014	R/W	Endpoint Direction Register	32 bits

EDR	Bit	R/W	Description	Initial State
	[31:9]		Reserved	
EP8DS	[8]	R/W	Endpoint 8 Direction Select	0
EP7DS	[7]	R/W	Endpoint 7 Direction Select	0
EP6DS	[6]	R/W	Endpoint 6 Direction Select	0
EP5DS	[5]	R/W	Endpoint 5 Direction Select	0
EP4DS	[4]	R/W	Endpoint 4 Direction Select	0
EP3DS	[3]	R/W	Endpoint 3 Direction Select	0
EP2DS	[2]	R/W	Endpoint 2 Direction Select	0
EP1DS	[1]	R/W	Endpoint 1 Direction Select 0: Rx Endpoint 1: Tx Endpoint	0
	[0]		Reserved	

TEST REGISTER (TR)

The test register is used for the diagnostics. All bit are activated when 1 is written to and is cleared by 0 on them. Bit[3:0] are for the high speed device only.

Register	Address	R/W	Description	Reset Value
TR	0x4980_0018	R/W	Test Register	32 bits

TR	Bit	R/W	Description	Initial State
	[31:16]		Reserved	
VBUS	[15]	R	0 = Vbus OFF 1 = Vbus ON	0
	[14]		Reserved	
EUERR	[13]	R/C	EB UNDERRUN Error If error interrupt enable bit of SCR register is set to 1, EUERR is set to 1 when EB underrun error in transceiver is detected.	0
PERR	[12]	R/C	PID Error If error interrupt enable bit of SCR register is set to 1, PERR is set to 1 when PID error is detected.	0
	[11:5]		Reserved	
TMD	[4]	R/W	Test Mode. When TMD is set to 1. The core is forced into the test mode. Following TPS, TKS, TJS, TSNS bits are meaningful in test mode.	0
TPS	[3]	R/W	Test Packets. If this bit is set, the USB repetitively transmit the test packets to Host. The test packets are explained in 7.1.20 of USB 2.0 specification. This bit can be set when TMD bit is set.	0
TKS	[2]	R/W	Test K Select. If this bit is set, the transceiver port enters into the high-speed K state. This bit can be set when TMD bit is set.	0
TJS	[1]	R/W	Test J Select. If this bit is set, the transceiver port enters into the high-speed J state. This bit can be set when TMD bit is set.	0
TSNS	[0]	R/W	Test SE0 NAK Select If this bit is set, the transceiver enters into the high speed receive mode and must respond to any IN token with NAK handshake. This bit can be set when TMD bit is set.	0

SYSTEM STATUS REGISTER (SSR)

This register reports operational status of the USB 2.0 Function Core, especially about error status and power saving mode status. Except the line status, every status bits in the System Status Register could be an interrupt sources. When the register is read after an interrupt due to certain system status changes, MCU should write back 1 to the corresponding bits to clear it.

Register	Address	R/W	Description	Reset Value
SSR	0x4980_001C	R/C	Test Register	32 bits

SSR	Bit	R/W	Description	Initial State
	[31:16]		Reserved	
BAERR	[15]	R/C	Byte Align Error If error interrupt enable bit of SCR register is set to 1, BAERR is set to 1 when byte alignment error is detected.	0
TMERR	[14]	R/C	Timeout Error If error interrupt enable bit of SCR register is set to 1, TMERR is set to 1 when timeout error is detected.	0
BSERR	[13]	R/C	Bit Stuff Error If error interrupt enable bit of SCR register is set to 1, BSERR is set to 1 when bit stuff error is detected.	0
TCERR	[12]	R/C	Token CRC Error If error interrupt enable bit of SCR register is set to 1, BSERR is set to 1 when CRC error in token packet is detected.	
DCERR	[11]	R/C	Data CRC Error If error interrupt enable bit of SCR register is set to 1, DCERR is set to 1 when CRC error in data packet is detected.	0
EOERR	[10]	R/C	EB OVERRUN Error If error interrupt enable bit of SCR register is set to 1, EOERR is set to 1 when EB overrun error in transceiver is detected.	0
VBUSOFF	[9]	R/C	VBUS OFF If vbus off interrupt enable bit of SCR register is set to 1, VBUSOFF is set to 1 when VBUS is Low.	0
VBUSON	[8]	R/C	VBUS ON If vbus on interrupt enable bit of SCR register is set to 1, VBUSON is set to 1 when VBUS is High.	0
TBM	[7]	R/C	Toggle Bit Mismatch. If error interrupt enable bit of SCR register is set to 1, TBM is set to 1 when Toggle mismatch is detected.	0
DP	[6]	R	DP Data Line State DP informs the status of D+ Line	0

SSR	Bit	R/W	Description	Initial State
DM	[5]	R	DM Data Line State DM informs the status of D- Line	0
HSP	[4]	R	Host Speed 0 = Full Speed 1 = High Speed	0
SDE	[3]	R/C	Speed Detection End. SDE is set by the core when the HS Detect Handshake process is ended.	0
HFRM	[2]	R/C	Host Forced Resume. HFRM is set by the core in suspend state when host sends resume signaling.	0
HFSUSP	[1]	R/C	Host Forced Suspend HFSUSP is set by the core when the SUSPEND signaling from host is detected.	0
HFRES	[0]	R/C	Host Forced Reset. HFRES is set by the core when the RESET signaling from host is detected.	0

SYSTEM CONTROL REGISTER (SCR)

This register enables top-level control of the core. MCU should access this register for controls such as Power saving mode enable/disable.

Register	Address	R/W	Description	Reset Value
SCR	0x4980_0020	R/W	System Control Register	32 bits

SCR	Bit	R/W	Description	Initial State
	[31:15]		Reserved	
DTZIEN	[14]	R/W	DMA Total Counter Zero Interrupt Enable 0 = Disable 1 = Enable When set to 1, DMA total counter zero interrupt is generated.	0
	[13]		Reserved	
DIEN	[12]	R/W	DUAL Interrupt Enable 0 = Disable 1 = Enable When set to 1, Interrupt is activated until Interrupt source is cleared.	0
VBUSOFFEN	[11]	R/W	VBUS OFF Enable 0 = Disable 1 = Enable	0
VBUSONEN	[10]	R/W	VBUS ON Enable 0 = Disable 1 = Enable	0
RWDE	[9]	R/W	Reverse Write Data Enable 0 = High byte data is first send to Host 1 = Low byte data is first sent to Host (We don't support Low byte first, so must set to "0")	1
EIE	[8]	R/W	Error Interrupt Enable This bit must be set to 1 to enable error interrupt.	0
BIS	[7]	R/W	Bus Interface Select, The MCU bus width is selected by BIS. When set to 0, bus width is 8bit. When set to 1, bus width is set to 16bit. (Only Using 16bit mode. so must set to "1")	1
SPDEN	[6]	R/W	Speed Detect End Interrupt Enable When set to 1, Speed detection interrupt is generated.	0
RRDE	[5]	R/W	Reverse Read Data Enable 0 = First received byte is loaded in Low byte field. 1 = First received byte is loaded in High byte field. (We don't support Low byte first, so must set to "1")	0

SCR	Bit	R/W	Description	Initial State
IPS	[4]	R/W	Interrupt Polarity Select (must write “0”, don’t set to ”1”)	0
	[3]		Reserved	0
MFRM	[2]	R/W	Resume by MCU If this bit is set, the suspended core generates a resume signal. This bit is set when MCU writes 1. This bit is cleared when MCU writes 0.	0
HSUSPE	[1]	R/W	Suspend Enable When set to 1, core can respond to the suspend signaling by USB host.	0
HRESE	[0]	R/W	Reset Enable When set to 1, core can respond to the reset signaling by USB host.	0

NOTE: “Speed Detection Control“ register is deleted.

EP0 STATUS REGISTER (EP0SR)

This register stores status information of the Endpoint 0. These status information are set automatically by the core when corresponding conditions are met. After reading the bits, MCU should write 1 to clear them.

Register	Address	R/W	Description	Reset Value
EP0SR	0x4980_0024	R/W	EP0 Status Register	32 bits

EP0SR	Bit	R/W	Description	Initial State
	[31:7]		Reserved	
LWO	[6]	R	Last Word Odd LWO informs that the last word of a packet in FIFO has an invalid upper byte. This bit is cleared automatically after the MCU reads it from the FIFO.	0
	[5]		Reserved	
SHT	[4]	R/C	Stall Handshake Transmitted SHT informs that STALL handshake due to stall condition is sent to Host. This bit is an interrupt source. This bit is cleared when the MCU writes 1.	0
	[3:2]		Reserved	
TST	[1]	R/C	Tx successfully received TST is set by core after core sends TX data to Host and receives ACK successfully. TST is one of the interrupt sources.	0
RSR	[0]	R/C	Rx successfully received. RSR is set by core after core receives error free packet from Host and sent ACK back to Host successfully. RSR is one of the interrupt sources.	0

EP0 CONTROL REGISTER (EP0CR)]

EP0 control register is used for the control of endpoint 0. Controls such as enabling ep0 related interrupts and toggle controls can be handled by EP0 control register.

Register	Address	R/W	Description	Reset Value
EP0CR	0x4980_0028	R/W	EP0 Control Register	32 bits

EP0CR	Bit	R/W	Description	Initial State
	[31:7]		Reserved	
TTE	[3]	R/W	Tx Test Enable This bit can be used for Test. TTE enables MCU to control Tx data toggle bit and Tx zero length set bit. The Tx data toggle bit and Tx zero length set bit do not need to be set in normal operation. 0 = disable 1 = enable	0
TSS	[2]	R/W	Tx Toggle Set. TTS is useful for Test. TTS can be managed when Tx Test Enable (TTE) bit is set. 0 = DATA PID 0 1 = DATA PID 1	0
ESS	[1]	R/W	Endpoint Stall Set ESS is set by MCU when it intends to send STALL handshake to Host. This bit is cleared when the MCU writes 0 on it. ESS is needed to be set 0 after MCU writes 1 on it.	0
TZLS	[0]	R/W	Tx Zero Length Set. TZLS is set by MCU when it intends to send Tx zero length data to Host. TZLS is useful for core Test. TZLS can be managed when Tx Test Enable (TTE) bit is set. This bit is cleared when the MCU writes 0 on it	0

ENDPOINT# BUFFER REGISTER (EP#BR)

The buffer register is used to hold data for TX/RX transfer.

Register	Address	R/W	Description	Reset Value
EP0BR	0x4980_0060	R/W	EP0 Buffer Register	32 bits
EP1BR	0x4980_0064	R/W	EP1 Buffer Register	32 bits
EP2BR	0x4980_0068	R/W	EP2 Buffer Register	32 bits
EP3BR	0x4980_006C	R/W	EP3 Buffer Register	32 bits
EP4BR	0x4980_0070	R/W	EP4 Buffer Register	32 bits
EP5BR	0x4980_0074	R/W	EP5 Buffer Register	32 bits
EP6BR	0x4980_0078	R/W	EP6 Buffer Register	32 bits
EP7BR	0x4980_007C	R/W	EP7 Buffer Register	32 bits
EP8BR	0x4980_0080	R/W	EP8 Buffer Register	32 bits

EP#BR	Bit	R/W	Description	Initial State
	[31:16]		Reserved	
	[15:0]	R/W	Buffer register holds TX/RX data between MCU and the core	16hX

ENDPOINT STATUS REGISTER (ESR)

The endpoint status register reports current status of an endpoint (except EP0) to the MCU

Register	Address	R/W	Description	Reset Value
ESR	0x4980_002C	R/W	Endpoint Status Register	32 bits

ESR	Bit	R/W	Description	Initial State
	[31:16]		Reserved	
FUDR	[15]	R/C	FIFO underflow. FUDR is only used for ISO mode. FUDR is set when FIFO is empty and Host sends IN token. This bit is cleared when the MCU write 1.	0
FOVF	[14]	R/C	FIFO overflow. FOVF is only used for ISO mode. FOVF is set when FIFO is full and Host sends OUT data. This bit is cleared when the MCU writes 1.	0
	[13:12]		reserved	
FPID	[11]	R/W	First OUT Packet interrupt Disable in OUT DMA operation. First Received OUT packet generates interrupt if this bit is disabled and DEN in DMA control register is enabled 0 = Disable 1 = Enable	0
OSD	[10]	R/C	OUT Start DMA Operation. OSD is set when First OUT packet is received after Registers related DMA Operation are set.	0
DTCZ	[9]	R/C	DMA Total Count Zero DTCZ is set when DMA Operation Total Counter reach to 0. This bit is cleared when the MCU writes 1 on it.	0
SPT	[8]	R/C	Short Packet Received. SPT informs that OUT endpoint receives short packet during OUT DMA Operation. This bit is cleared when the MCU writes 1 on it.	0
DOM	[7]	R	Dual Operation Mode DOM is set when the max packet size of corresponding endpoint is equal to a half FIFO size. This bit is read only. Endpoint0 does not support dual mode.	0

ESR	Bit	R/W	Description	Initial State
FFS	[6]	R/C	FIFO Flushed. FFS informs that FIFO is flushed. This bit is an interrupt source. This bit is cleared when the MCU clears FLUSH bit in Endpoint Control Register.	0
FSC	[5]	R/C	Function Stall Condition. FSC informs that STALL handshake due to functional stall condition is sent to Host. This bit is set when endpoint stall set bit is set by the MCU. This bit is cleared when the MCU writes 1 on it.	0
LWO	[4]	R	Last Word Odd. LWO informs that the lower byte of last word is only valid. This bit is automatically cleared after the MCU reads packet data received Host.	0
PSIF	[3:2]	R	Packet Status In FIFO. 00 = No packet in FIFO 01 = One packet in FIFO 10 = Two packet in FIFO 11 = Invalid value	0
TPS	[1]	R/C	Tx Packet Success TPS is used for Single or Dual transfer mode. TPS is activated when one packet data in FIFO was successfully transferred to Host and received ACK from Host. This bit should be cleared by writing 1 on it after being read by the MCU.	0
RPS	[0]	R	Rx Packet Success. RPS is used for Single or Dual transfer mode. RPS is activated when the FIFO has a packet data to receive. RPS is automatically cleared when MCU reads all packets (one or two) from FIFO. MCU can identify the packet size through BYTE READ COUNT REGISTER (BRCR).	0

ENDPOINT CONTROL REGISTER (ECR)

The endpoint control register is useful for controlling an endpoint both in normal operation and test case. Putting an endpoint in specific operation mode can be accomplished through the endpoint control register.

Register	Address	R/W	Description	Reset Value
ECR	0x4980_0030	R/W	Endpoint Control Register	32 bits

ECR	Bit	R/W	Description	Initial State
	[31:13]		Reserved	
INPKTHLD	[12]	R/W	The MCU can control Tx FIFO status through this bit. If this bit is set to one, USB does not send IN data to Host. 0 = The USB can send IN data to Host according to IN FIFO status(normal operation) 1 = The USB sends NAK handshake to Host regardless of IN FIFO status.	0
OUTPKTHLD	[11]	R/W	The MCU can control Rx FIFO Status through this bit. If this bit is set to one, USB does not accept OUT data from Host. 0 = The USB can accept OUT data from Host according to OUT FIFO status(normal operation) 1 = The USB does not accept OUT data from Host.	0
TNPMF	[10:9]	R/W	Transaction Number Per Micro Frame. TNPMF is useful for ISO transfer. 00 = Invalid value 01 = 1 Transaction Per MicroFrame 10 = 2 Transaction Per MicroFrame 11 = 3 Transaction Per MicroFrame	0
IME	[8]	R/W	ISO mode Endpoint IME determines the transfer type of an endpoint. 0 = Bulk(Interrupt) mode 1 = ISO mode	0
DUEN	[7]	R/W	Dual FIFO mode Enable 0 = Dual Disable(Single mode) 1 = Dual Enable	0
FLUSH	[6]	R/W	FIFO Flush FIFO is flushed when this bit is set to 1. This bit is automatically cleared after MCU writes 1.	0
TTE	[5]	R/W	TX Toggle Enable. The MCU can force TX data toggle bit with TTE. This bit is useful for test. The TX data toggle bit changes automatically in normal operation. 0 = Disable 1 = Enable	0

ECR	Bit	R/W	Description	Initial State
TTS	[4:3]	R/W	TX Toggle Select TTS is used for test. This is valid when TX Toggle Enable (TTE) is set. 00 = DATA PID 0 01 = DATA PID 1 10 = DATA PID 2 (Only in ISO mode) 11 = DATA PID M (Only in ISO mode)	00
CDP	[2]	R/W	Clear Data PID In RX mode When this bit is set to 1, data toggle bit in core to be compared with the data PID of received packet is reset to 0. This bit is automatically cleared after MCU writes 1. In TX mode TX data PID to be transmitted to host is reset to 0 when this bit is set to 1. This bit is automatically cleared after MCU writes 1.	0
ESS	[1]	R/W	Endpoint Stall Set ESS is set by the MCU when the MCU intends to send STALL handshake to Host. This bit is cleared when the MCU writes 0 in it.	0
TZLS	[0]	R/W	TX Zero Length Set. This bit is used for Test. TZLS is set by the MCU when the MCU intends to send zero length TX data to Host. This bit is cleared when the MCU writes 0 in it.	0

BYTE READ COUNT REGISTER (BRCR)

The byte read count register keeps byte (half word) counts of a RX packet from USB host.

Register	Address	R/W	Description	Reset Value
BRCR	0x4980_0034	R	Byte Read Count Register	32 bits

BRCR	Bit	R/W	Description	Initial State
	[31:10]		Reserved	
RDCNT	[9:0]	R	FIFO Read Byte Count[9:0] RDCNT is read only. The BRCR inform the amount of received data from host. In 16-bit Interface, RDCNT informs the amount of data in half word (16-bit) unit. Through the LWO bit of EP0SR, the MCU can determine valid byte in last data word.	10'h

BYTE WRITE COUNT REGISTER (BWCR)

The byte write count register keeps the byte (half word) count value of a TX packet from MCU. The counter value will be used to determine the end of TX packet.

Register	Address	R/W	Description	Reset Value
BWCR	0x4980_0038	R/W	Byte Write Count Register	32 bits

BWCR	Bit	R/W	Description	Initial State
	[31:10]		Reserved	
WRCNT	[9:0]	R/W	Through BWCR, the MCU must load the byte counts of a TX data packet to the core. The core uses this count value to determine the end of packet. The count value to this register must be less than MAXP.	10'h

MAX PACKET REGISTER (MPR)

The byte write count register keeps the byte (half word) count value of a TX packet from MCU. The counter value will be used to determine the end of TX packet.

Register	Address	R/W	Description	Reset Value
MPR	0x4980_003C	R/W	MAX Packet Register	32 bits

MPR	Bit	R/W	Description	Initial State
	[31:11]		Reserved	
MAXP	[10:0]	R/W	MAX Packet [10:0] The max packet size of each endpoint is determined by MAX packet register. The range of max packet is from 0 to 1024 bytes. 000_0000_0000 = Max Packet 0 byte. 000_0000_1000 = Max Packet 8 bytes. 000_0001_0000 = Max Packet 16 bytes. 000_0010_0000 = Max Packet 32 bytes. 000_0100_0000 = Max Packet 64 bytes. 000_1000_0000 = Max Packet 128 bytes. 001_0000_0000 = Max Packet 256 bytes. 010_0000_0000 = Max Packet 512 bytes. 100_0000_0000 = Max Packet 1024 bytes.	11'h0

DMA CONTROL REGISTER (DCR)

The AHB Master Operation is controlled by the programming DMA Control Register and DMA IF Control Register.

Register	Address	R/W	Description	Reset Value
DCR	0x4980_0040	R/W	DMA Control Register	32 bits

DCR	Bit	R/W	Description	Initial State
	[31:6]		Reserved	
ARDRD	[5]	R/W	Auto Rx DMA Run set disable. 0 = set 1 = disable This bit is cleared when DMA operation is ended.	0
FMDE	[4]	R/W	Burst Mode Enable. This bit is used to run Burst Mode DMA Operation. 0 = Burst mode disable 1 = Burst mode enable	0
	[3]		Reserved	
TDR	[2]	R/W	Tx DMA Operation Run This bit is used to set start DMA operation for Tx Endpoint (IN endpoint) 0 = DMA operation stop 1 = DMA operation run	0
RDR	[1]	R/W	Rx DMA Operation Run This bit is used to start DMA operation for Rx Endpoint (OUT endpoint). This bit is automatically set when USB receives OUT packet data and DEN bit is set to 1 and ARDRD bit is set to 0. To operate DMA operation after OUT packet data received, MCU must set RDR to 1. 0 = DMA operation stop. 1 = DMA operation run.	0
DEN	[0]	R/W	DMA Operation Mode Enable This bit is used to set the DMA Operation mode 0 = Interrupt Operation mode 1 = DMA Operation mode	0

NOTE: fly/Demand mode DMA enable registers deleted.

DMA TRANSFER COUNTER REGISTER (DTCR)

The byte write count register keeps the byte (half word) count value of a TX packet from MCU. The counter value will be used to determine the end of TX packet.

Register	Address	R/W	Description	Reset Value
DTCR	0x4980_0044	R/W	DMA Transfer Counter Register	32 bits

MTCR	Bit	R/W	Description	Initial State
	[31:16]		Reserved	
DTCR	[15:0]	R/W	To operate single mode transfer, DTCR is needed to be set 16'h0002. In case of Burst mode, the MCU should set max packet value.	16'h0

DMA FIFO COUNTER REGISTER (DFCR)

This register has the byte number of data per DMA operation.
The max packet size is loaded in this register.

Register	Address	R/W	Description	Reset Value
DFCR	0x4980_0048	R/W	DMA FIFO Counter Register	32 bits

MFCR	Bit	R/W	Description	Initial State
	[31:16]		Reserved	
DFCR	[15:0]	R/W	In case of OUT Endpoint, the size value of received packet will be loaded in this register automatically when Rx DMA Run is enabled. In case of IN Endpoint, the MCU should set max packet value.	16'h0

DMA TOTAL TRANSFER COUNTER REGISTER 1/2 (DTTCR 1/2)

This register has the total byte number of data to transfer using DMA Interface.
When this counter register value is zero, DMA operation is ended.

Register	Address	R/W	Description	Reset Value
DTTCR1 DTTCR2	0x4980_004C 0x4980_0050	R/W	DMA Total Transfer Counter Register 1/2	32 bits

MTTCR#	Bit	R/W	Description	Initial State
	[31:16]		Reserved	
DTTCR	[15:0]	R/W	This register should have total byte size to be transferred using DMA Interface. DMA Total Transfer Counter1 : Low half word value DMA Total Transfer Counter2 : High half word value. The max value is up to 2^32	16'h0

DMA INTERFACE CONTROL REGISTER (DICR)

The AHB Master Operation is controlled by the programming DMA Control Register and DMA IF Control Register.

Register	Address	R/W	Description	Reset Value
DICR	0x4980_0084	R/W	DMA Interface Counter Register	32 bits

DICR	Bit	R/W	Description	Initial State
Reserved	[31:4]		Reserved	0
RELOAD_ MBAR	[4]	R/W	Select Reload Condiion 0 – Every end of Full DMA operation 1 – Every Packet transfer.	0
Reserved	[3]		Reserved	0
WORD_ SWAP	[2]	R/W	Half Word swapping 0 = normal 1 = swap	0
MAX_BURST	[1:0]	R/W	Max Burst Length 00 = Single transfer 01 = 4-beat incrementing burst transfer(INCR4) 10 = 8-beat incrementing burst transfer(INCR8) 11 = 16-beat incrementing burst transfer(INCR16)	00

MEMORY BASE ADDRESS REGISTER (MBAR)

Register	Address	R/W	Description	Reset Value
MBAR	0x4980_0088	R/W	Memory Base Address Register	32 bits

MBAR#	Bit	R/W	Description	Initial State
MBAR	[31:0]	R/W	This register should have memory base address to be transferred using DMA Interface.	32'h0

MEMORY CURRENT ADDRESS REGISTER (MCAR)

Register	Address	R/W	Description	Reset Value
MCAR	0x4980_008C	R	Memory Current Address Register	32 bits

MCAR#	Bit	R/W	Description	Initial State
MCAR	[31:0]	R	This register should have memory current address to be transferred using DMA Interface.	

BURST FIFO CONTROL REGISTER(FCON)

Register	Address	R/W	Description	Reset Value
FCON	0x4980_0100	R/W	Burst DMA transfer Control	32 bits

MBAR#	Bit	R/W	Description	Initial State
Reserved	[31:9]	R/W	Reserved	000000
DMAEN	[8]	R/W	DMA enable	0
Rreserved	[7:5]	R/W	Reserved	000
TF_CLR	[4]	R/W	TX fifo clear	0
Reserved	[3:1]	R/W	Reserved	000
RF_CLR	[0]	R/W	RX fifo clear	0

BURST FIFO STATUS REGISTER(FSTAT)

Register	Address	R/W	Description	Reset Value
FSTAT	0x4980_0104	R/W	Burst DMA transfer Status	32 bits

FSTAT	Bit	R/W	Description	Initial State
Reserved	[31:14]	R	Reserved	
TF_FULL	[13]	R	TX FIFO Full	0
TF_CNT	[12:8]	R	# of data in TX fifo	0
Reserved	[7:6]		Reserved	0
RF_FULL	[5]	R	RX FIFO Full	0
RF_CNT	[4:0]	R	# of data in RX fifo	0

AHB MASTER(DMA) OPERATION FLOW CHART

A. OUT Transfer Operation Flow

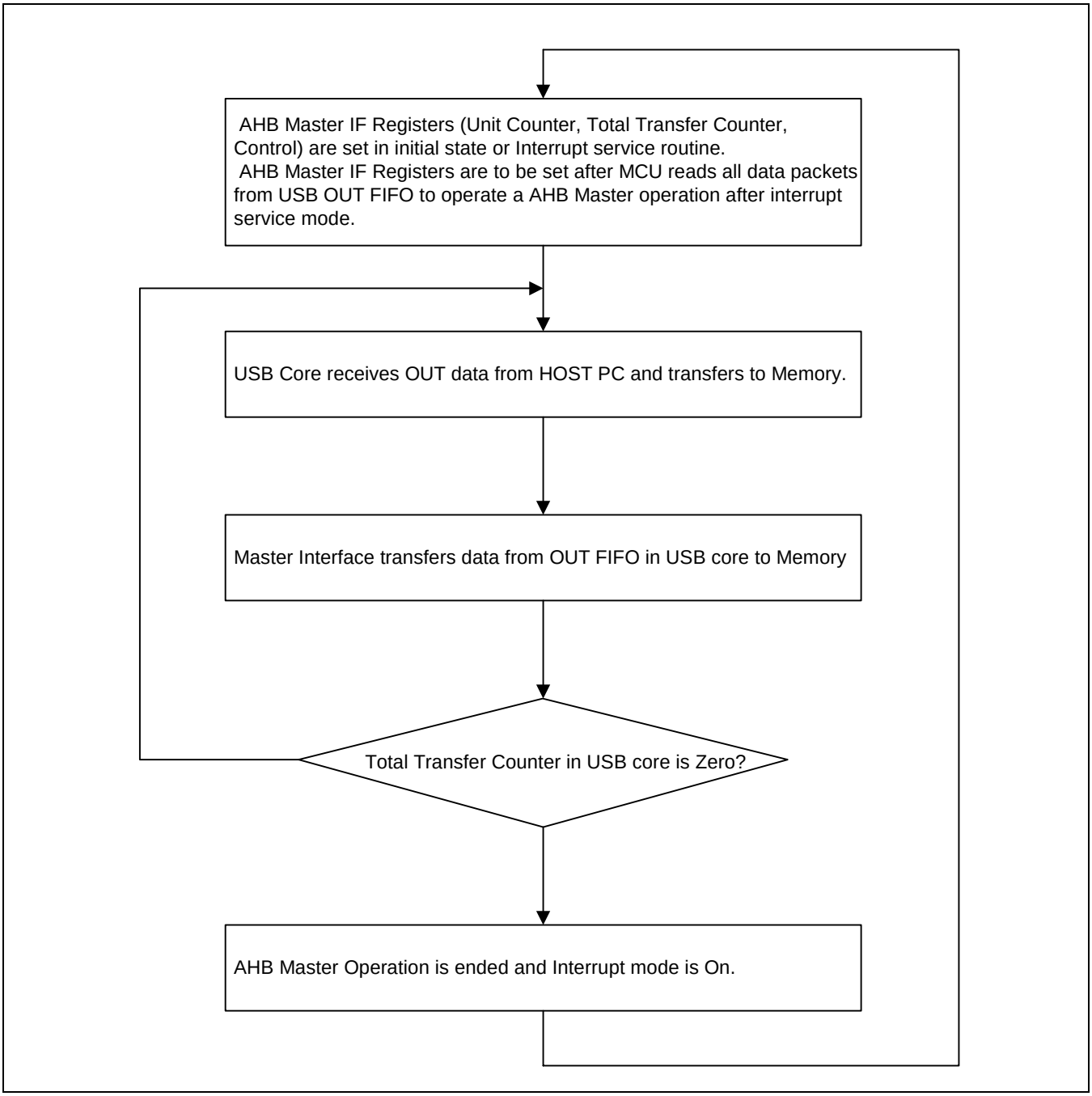


Figure 17-3. OUT Transfer Operation Flow

B. IN Transfer Operation Flow

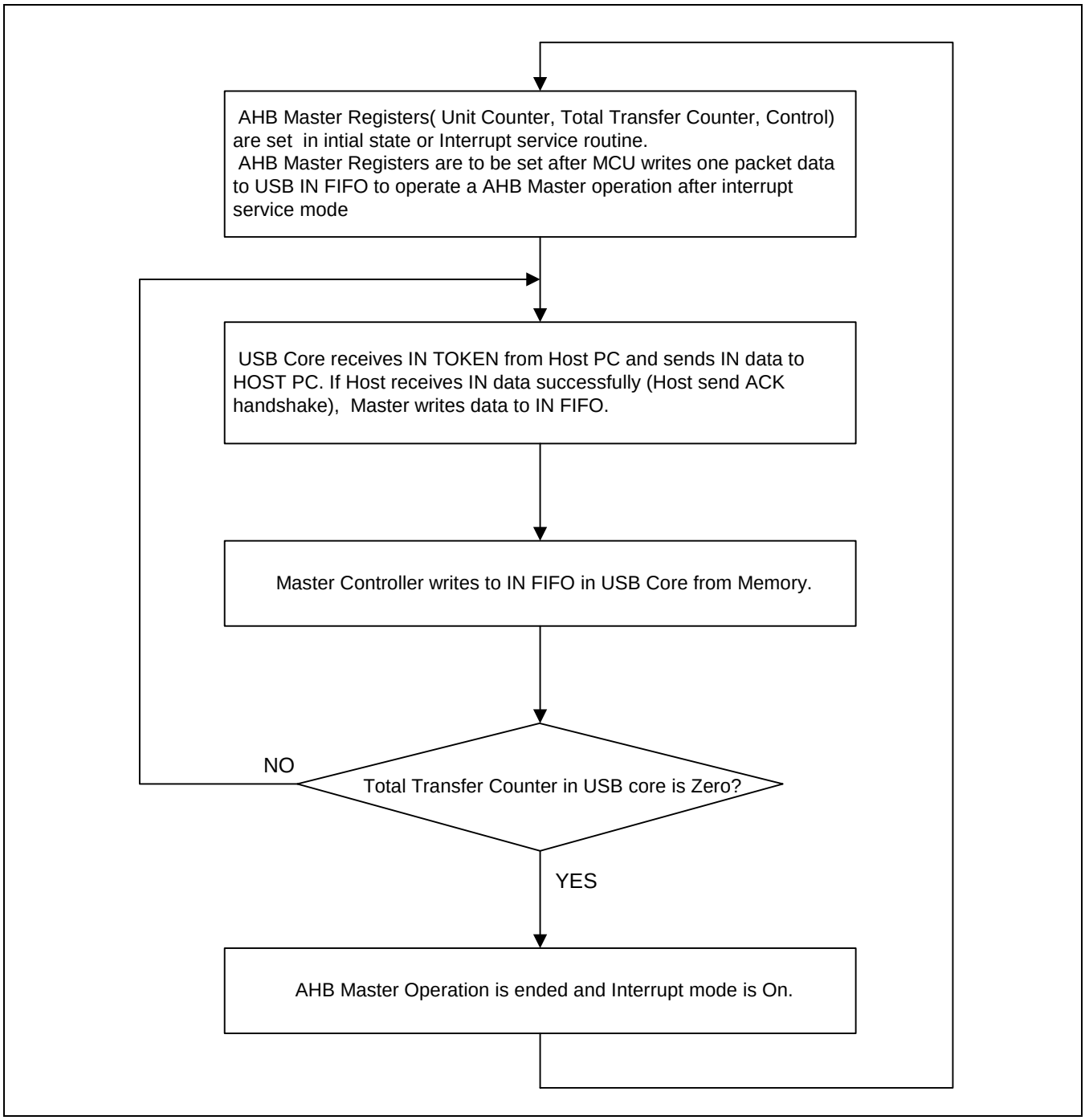


Figure 17-4. IN Transfer Operation Flow

NOTES

18 IIC-BUS INTERFACE

OVERVIEW

The S3C2443X RISC microprocessor can support a multi-master IIC-bus serial interface. A dedicated serial data line (SDA) and a serial clock line (SCL) carry information between bus masters and peripheral devices which are connected to the IIC-bus. The SDA and SCL lines are bi-directional.

In multi-master IIC-bus mode, multiple S3C2443X RISC microprocessors can receive or transmit serial data to or from slave devices. The master S3C2443X can initiate and terminate a data transfer over the IIC-bus. The IIC-bus in the S3C2443X uses Standard bus arbitration procedure.

To control multi-master IIC-bus operations, values must be written to the following registers:

— Multi-master IIC-bus control register, IICCON

— Multi-master IIC-bus control/status register, IICSTAT

— Multi-master IIC-bus Tx/Rx data shift register, IICDS

— Multi-master IIC-bus address register, IICADD

When the IIC-bus is free, the SDA and SCL lines should be both at High level. A High-to-Low transition of SDA can initiate a Start condition. A Low-to-High transition of SDA can initiate a Stop condition while SCL remains steady at High Level.

The Start and Stop conditions can always be generated by the master devices. A 7-bit address value in the first data byte, which is put onto the bus after the Start condition has been initiated, can determine the slave device which the bus master device has selected. The 8th bit determines the direction of the transfer (read or write).

Every data byte put onto the SDA line should be eight bits in total. The bytes can be unlimitedly sent or received during the bus transfer operation. Data is always sent from most-significant bit (MSB) first, and every byte should be immediately followed by acknowledge (ACK) bit.

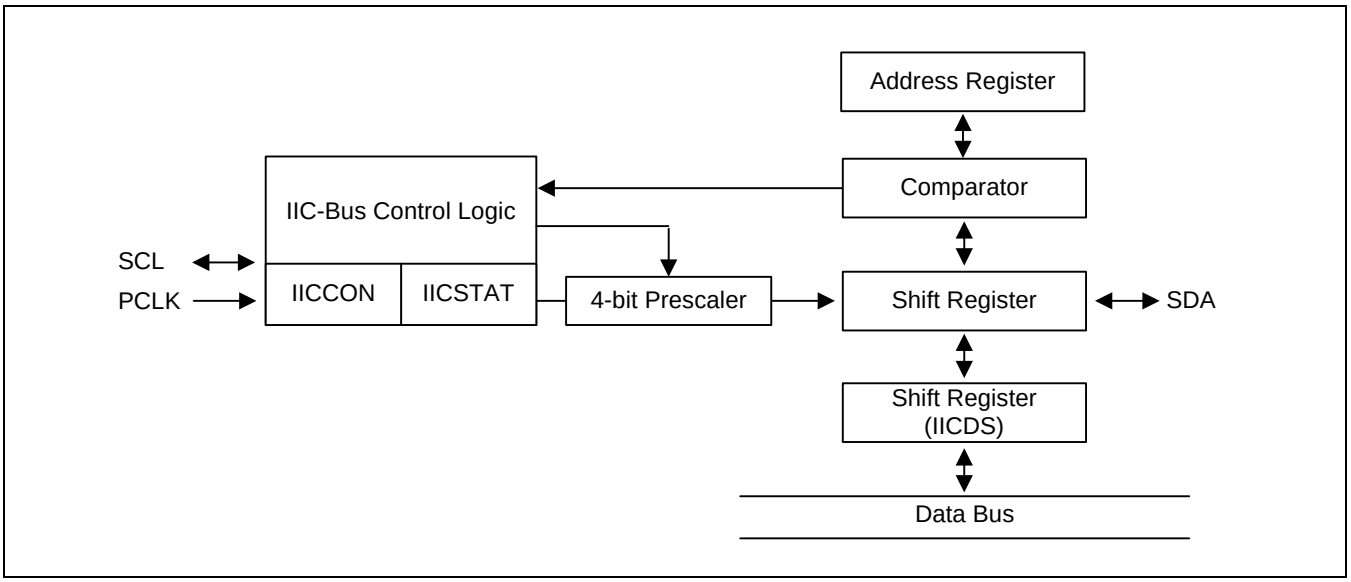


Figure 18-1. IIC-Bus Block Diagram

IIC-BUS INTERFACE

The S3C2443X IIC-bus interface has four operation modes:

— Master transmitter mode
— Master receive mode
— Slave transmitter mode
— Slave receive mode

Functional relationships among these operating modes are described below.

START AND STOP CONDITIONS

When the IIC-bus interface is inactive, it is usually in Slave mode. In other words, the interface should be in Slave mode before detecting a Start condition on the SDA line (a Start condition can be initiated with a High-to-Low transition of the SDA line while the clock signal of SCL is High). When the interface state is changed to Master mode, a data transfer on the SDA line can be initiated and SCL signal generated.

A Start condition can transfer a one-byte serial data over the SDA line, and a Stop condition can terminate the data transfer. A Stop condition is a Low-to-High transition of the SDA line while SCL is High. Start and Stop conditions are always generated by the master. The IIC-bus gets busy when a Start condition is generated. A Stop condition will make the IIC-bus free.

When a master initiates a Start condition, it should send a slave address to notify the slave device. One byte of address field consists of a 7-bit address and a 1-bit transfer direction indicator (showing write or read).
If bit 8 is 0, it indicates a write operation (transmit operation); if bit 8 is 1, it indicates a request for data read (receive operation).

The master will complete the transfer operation by transmitting a Stop condition. If the master wants to continue the data transmission to the bus, it should generate another Start condition as well as a slave address. In this way, the read-write operation can be performed in various formats.

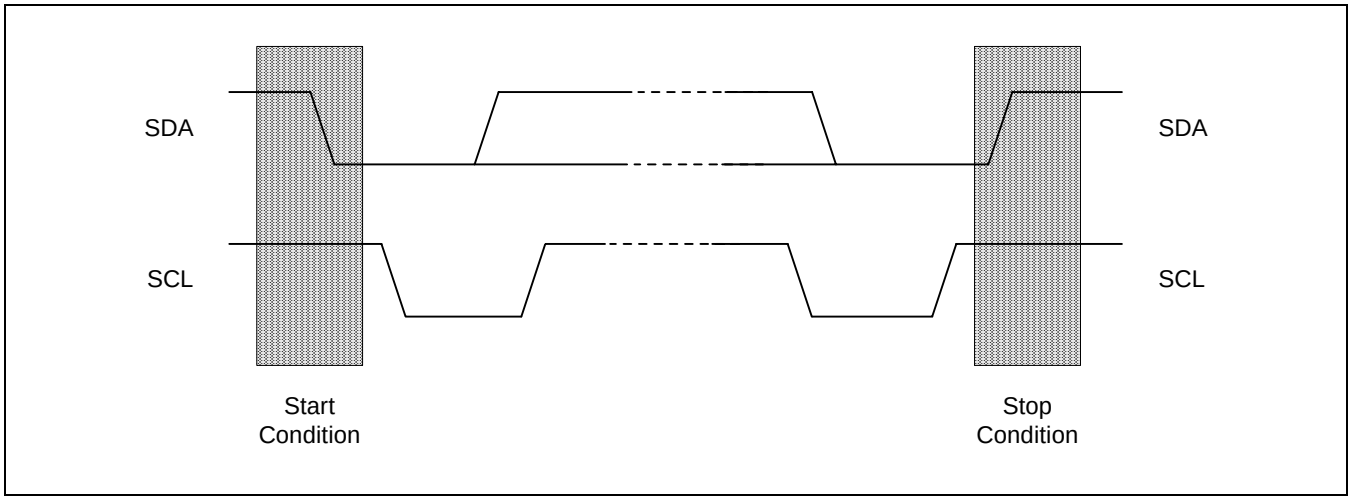


Figure 18-2. Start and Stop Condition

DATA TRANSFER FORMAT

Every byte placed on the SDA line should be eight bits in length. The bytes can be unlimitedly transmitted per transfer. The first byte following a Start condition should have the address field. The address field can be transmitted by the master when the IIC-bus is operating in Master mode. Each byte should be followed by an acknowledgement (ACK) bit. The MSB bit of the serial data and addresses are always sent first.

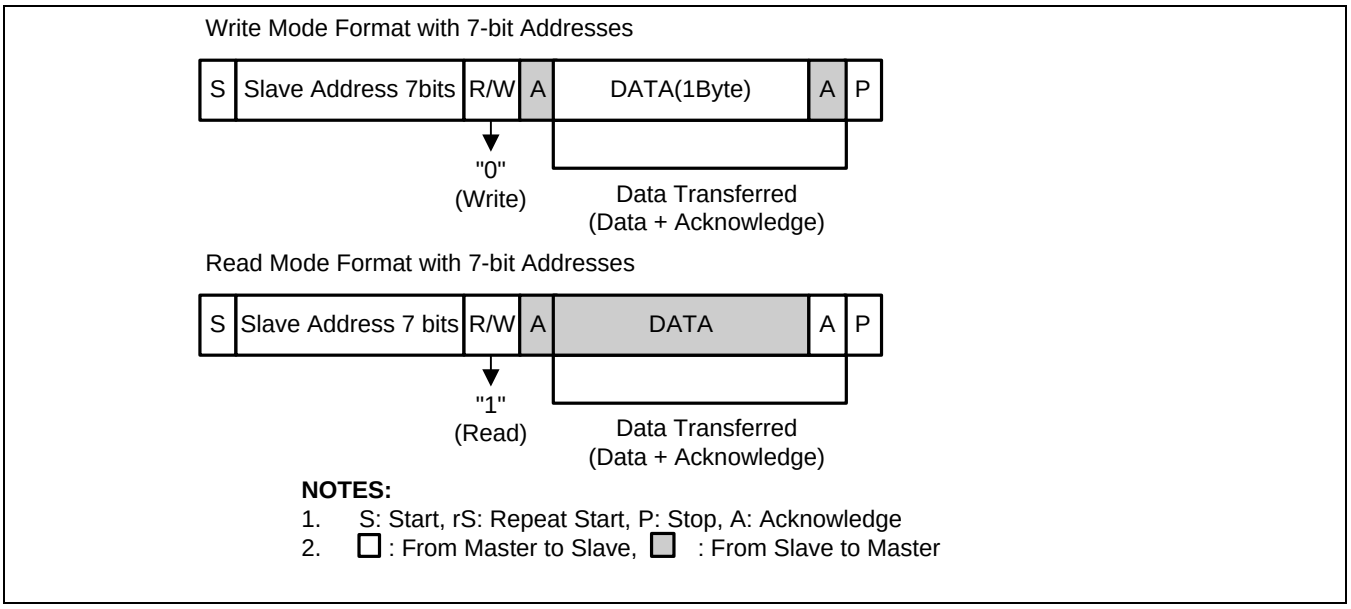


Figure 18-3. IIC-Bus Interface Data Format

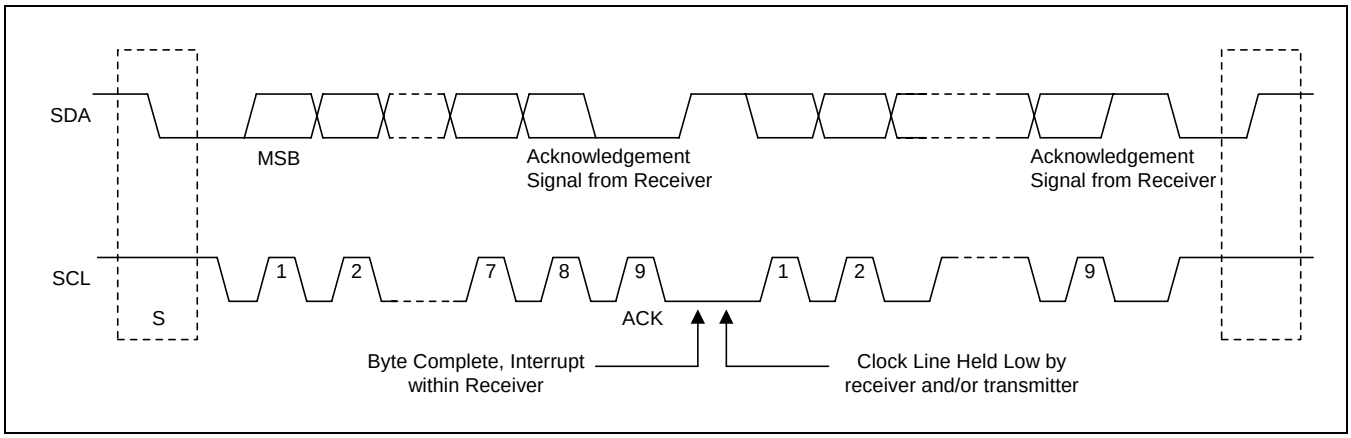


Figure 18-4. Data Transfer on the IIC-Bus

ACK SIGNAL TRANSMISSION

To complete a one-byte transfer operation, the receiver should send an ACK bit to the transmitter. The ACK pulse should occur at the ninth clock of the SCL line. Eight clocks are required for the one-byte data transfer. The master should generate the clock pulse required to transmit the ACK bit.

The transmitter should release the SDA line by making the SDA line High when the ACK clock pulse is received. The receiver should also drive the SDA line Low during the ACK clock pulse so that the SDA keeps Low during the High period of the ninth SCL pulse.

The ACK bit transmit function can be enabled or disabled by software (IICSTAT). However, the ACK pulse on the ninth clock of SCL is required to complete the one-byte data transfer operation.

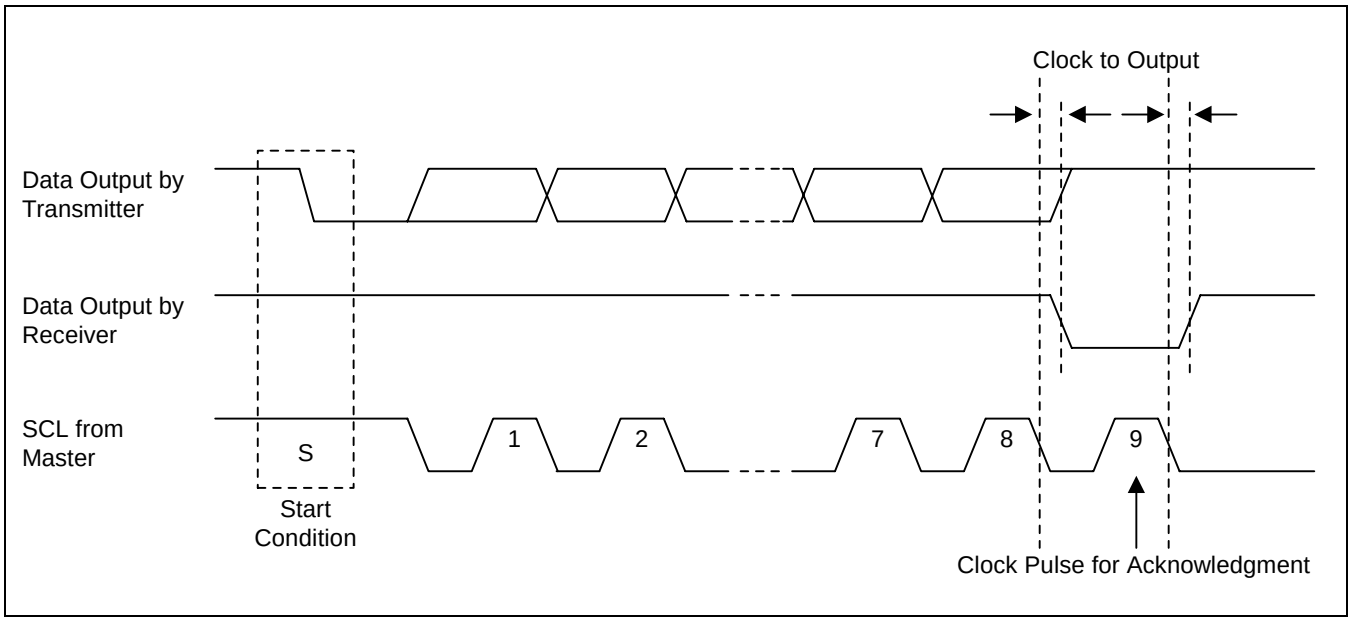


Figure 18-5. Acknowledge on the IIC-Bus

READ-WRITE OPERATION

In Transmitter mode, when the data is transferred, the IIC-bus interface will wait until IIC-bus Data Shift (IICDS) register receives a new data. Before the new data is written into the register, the SCL line will be held low, and then released after it is written. The S3C2443X should hold the interrupt to identify the completion of current data transfer. After the CPU receives the interrupt request, it should write a new data into the IICDS register, again.

In Receive mode, when data is received, the IIC-bus interface will wait until IICDS register is read. Before the new data is read out, the SCL line will be held low and then released after it is read. The S3C2443X should hold the interrupt to identify the completion of the new data reception. After the CPU receives the interrupt request, it should read the data from the IICDS register.

BUS ARBITRATION PROCEDURES

Arbitration takes place on the SDA line to prevent the contention on the bus between two masters. If a master with a SDA High level detects the other master with a SDA active Low level, it will not initiate a data transfer because the current level on the bus does not correspond to its own. The arbitration procedure will be extended until the SDA line turns High.

However, when the masters simultaneously lower the SDA line, each master should evaluate whether the mastership is allocated itself or not. For the purpose of evaluation is that each master should detect the address bits. While each master generates the slaver address, it should also detect the address bit on the SDA line because the SDA line is likely to get Low rather than to keep High. Assume that one master generates a Low as first address bit, while the other master is maintaining High. In this case, both masters will detect Low on the bus because the Low status is superior to the High status in power. When this happens, Low (as the first bit of address) generating master will get the mastership while High (as the first bit of address) generating master should withdraw the mastership. If both masters generate Low as the first bit of address, there should be arbitration for the second address bit, again. This arbitration will continue to the end of last address bit.

ABORT CONDITIONS

If a slave receiver cannot acknowledge the confirmation of the slave address, it should hold the level of the SDA line High. In this case, the master should generate a Stop condition and to abort the transfer.

If a master receiver is involved in the aborted transfer, it should signal the end of the slave transmit operation by canceling the generation of an ACK after the last data byte received from the slave. The slave transmitter should then release the SDA to allow a master to generate a Stop condition.

CONFIGURING IIC-BUS

To control the frequency of the serial clock (SCL), the 4-bit prescaler value can be programmed in the IICCON register. The IIC-bus interface address is stored in the IIC-bus address (IICADD) register. (By default, the IIC-bus interface address has an unknown value.)

FLOWCHARTS OF OPERATIONS IN EACH MODE

The following steps must be executed before any IIC Tx/Rx operations.

1. Write own slave address on IICADD register, if needed.
2. Set IICCON register.
   a) Enable interrupt
   b) Define SCL period
3. Set IICSTAT to enable Serial Output

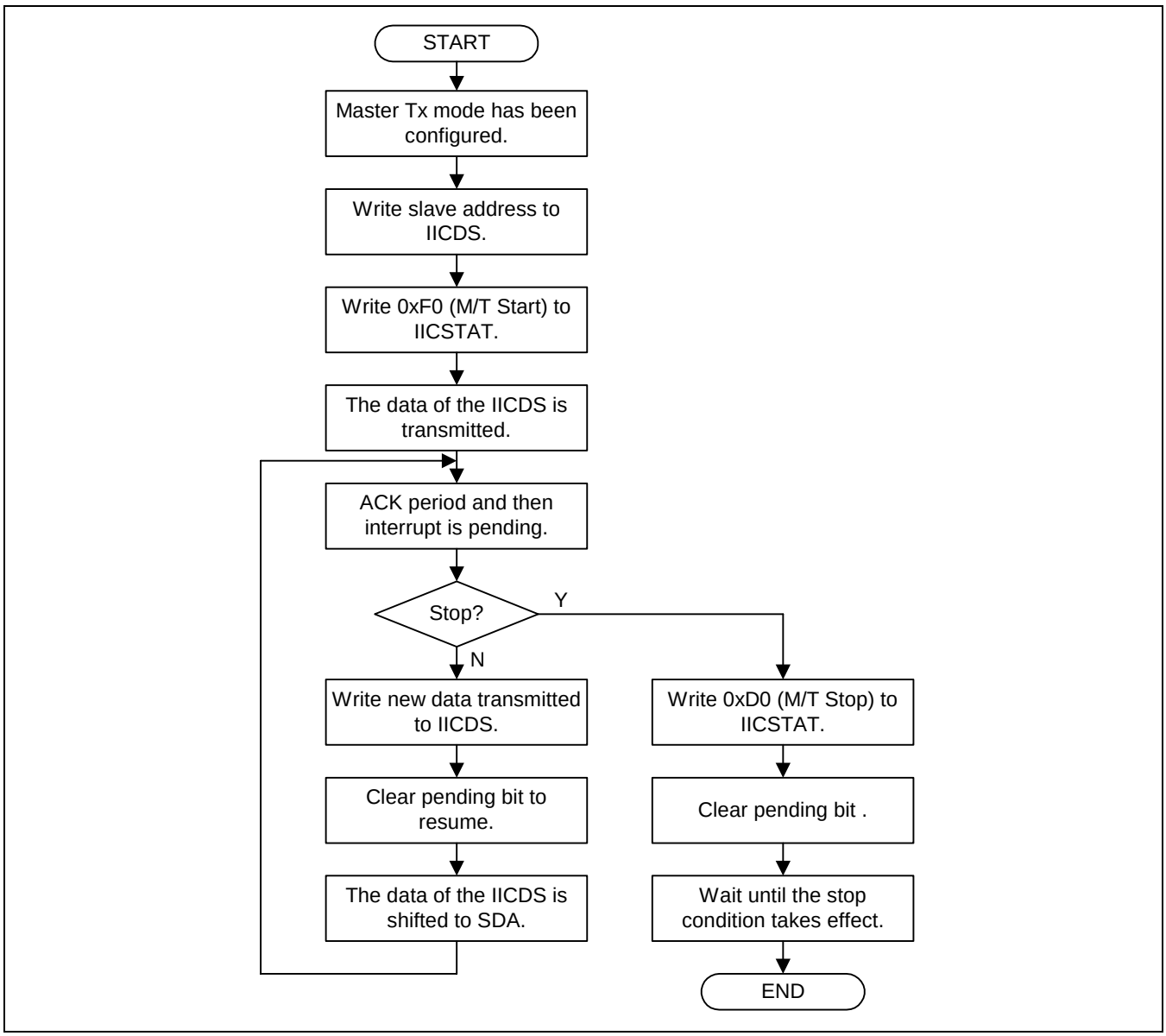


Figure 18-6. Operations for Master/Transmitter Mode

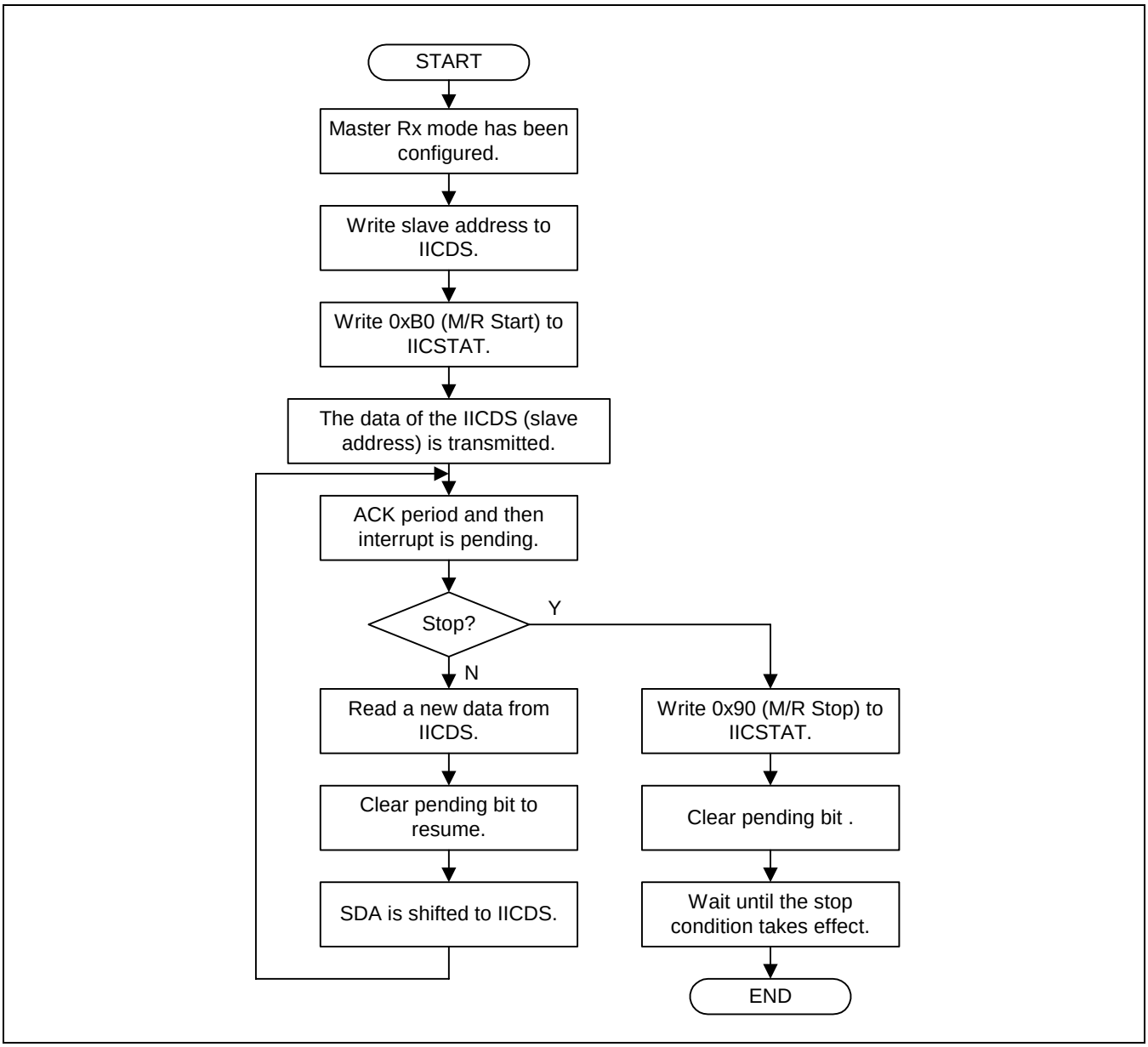


Figure 18-7. Operations for Master/Receiver Mode

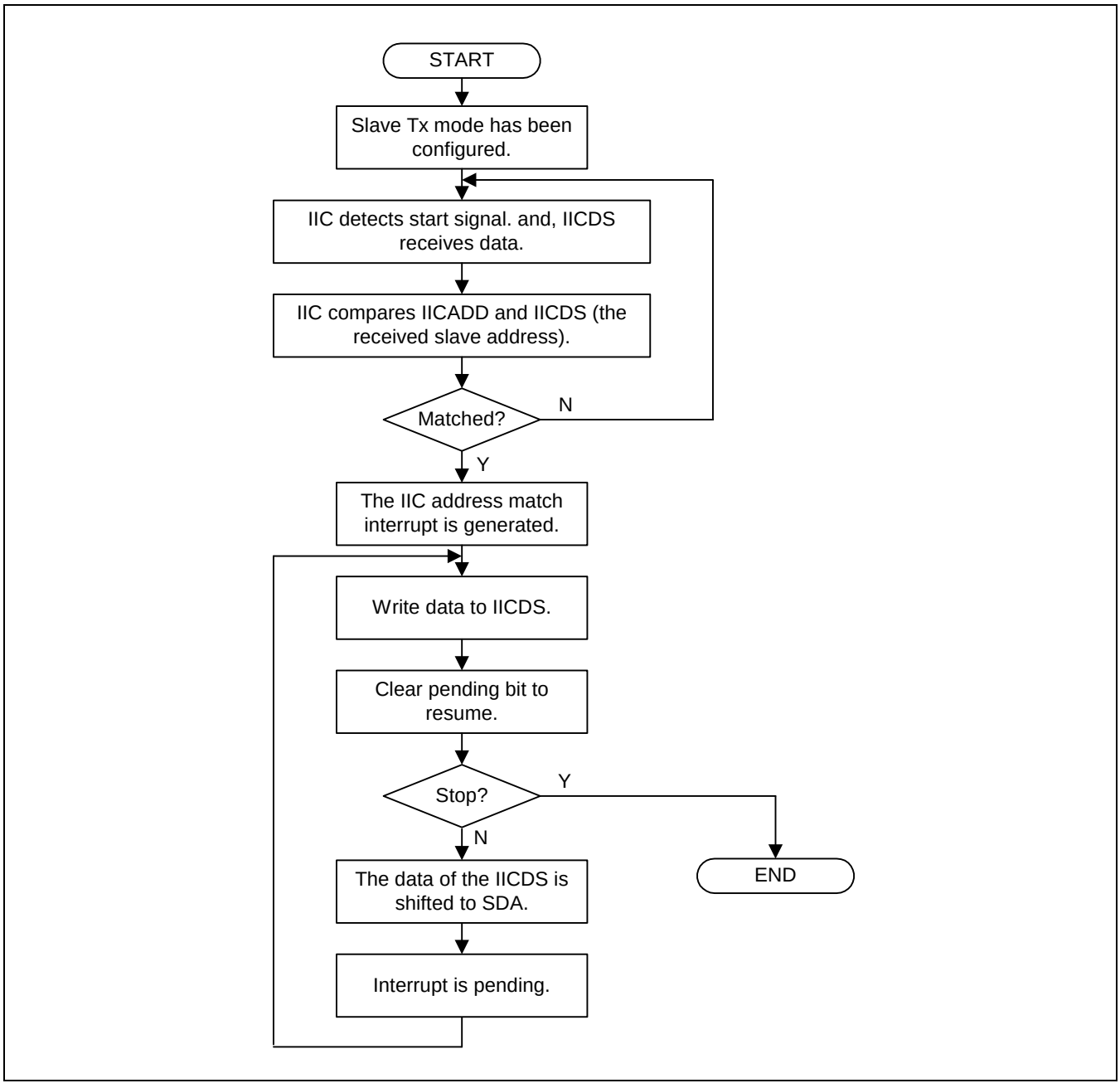


Figure 18-8. Operations for Slave/Transmitter Mode

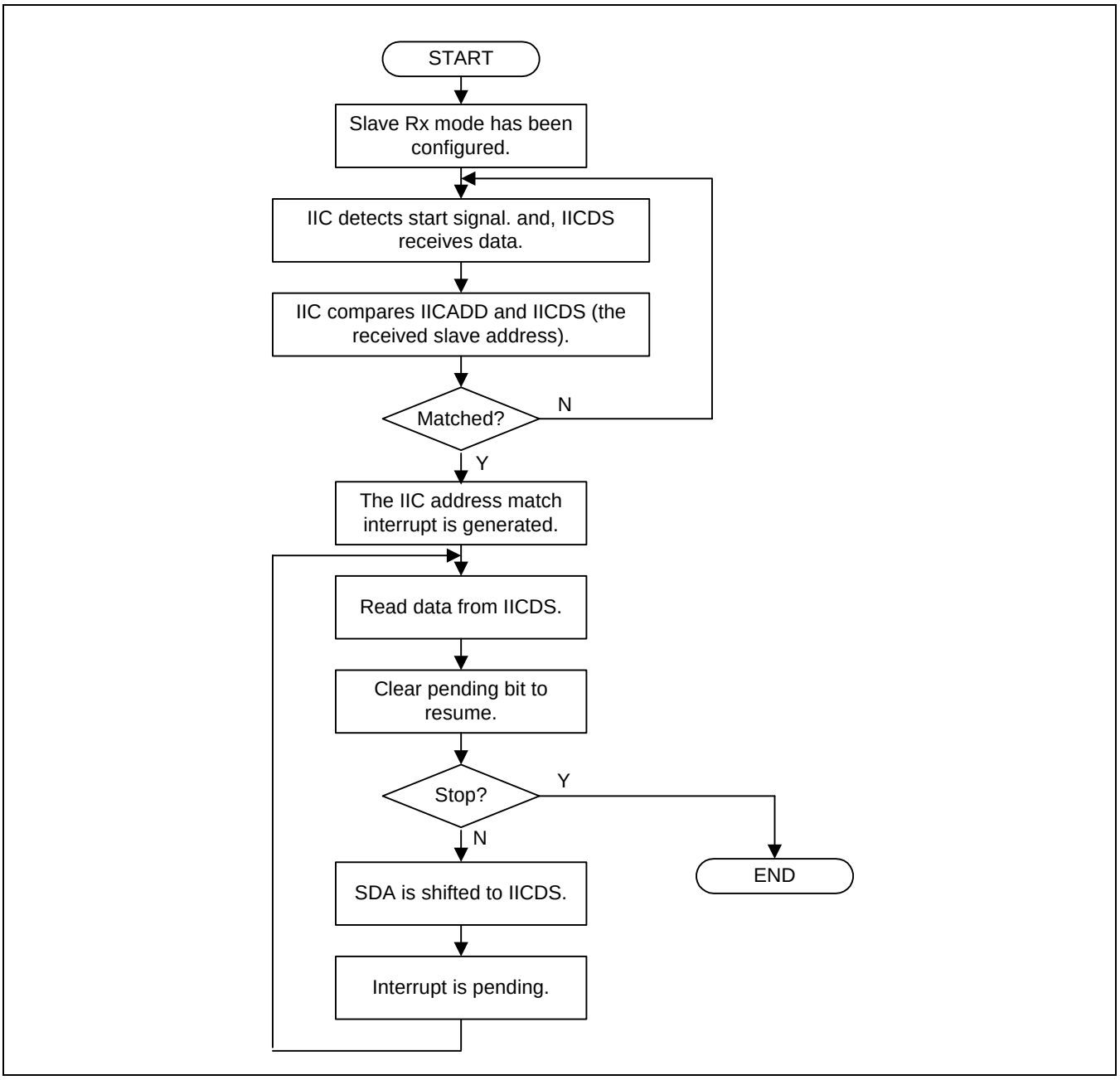


Figure 18-9. Operations for Slave/Receiver Mode

IIC-BUS INTERFACE SPECIAL REGISTERS

MULTI-MASTER IIC-BUS CONTROL (IICCON) REGISTER

Register	Address	R/W	Description	Reset Value
IICCON	0x54000000	R/W	IIC-Bus control register	0x0X

IICCON	Bit	Description	Initial State
Acknowledge generation (1)	[7]	IIC-bus acknowledge enable bit. 0: Disable 1: Enable In Tx mode, the IICSDA is free in the ack time. In Rx mode, the IICSDA is L in the ack time.	0
Tx clock source selection	[6]	Source clock of IIC-bus transmit clock prescaler selection bit. 0: IICCLK = PCLK /16 1: IICCLK = PCLK /512	0
Tx/Rx Interrupt (5)	[5]	IIC-Bus Tx/Rx interrupt enable/disable bit. 0: Disable, 1: Enable	0
Interrupt pending flag (2) (3)	[4]	IIC-bus Tx/Rx interrupt pending flag. This bit cannot be written to 1. When this bit is read as 1, the IICSCL is tied to L and the IIC is stopped. To resume the operation, clear this bit as 0. 0: 1) No interrupt pending (when read). 2) Clear pending condition & Resume the operation (when write). 1: 1) Interrupt is pending (when read) 2) N/A (when write)	0
Transmit clock value (4)	[3:0]	IIC-Bus transmit clock prescaler. IIC-Bus transmit clock frequency is determined by this 4-bit prescaler value, according to the following formula: Tx clock = IICCLK/(IICCON[3:0]+1).	Undefined

NOTES:

1. Interfacing with EEPROM, the ack generation may be disabled before reading the last data in order to generate the STOP condition in Rx mode.
2. An IIC-bus interrupt occurs 1) when a 1-byte transmits or receives operation is completed, 2) when a general call or a slave address match occurs, or 3) if bus arbitration fails.
3. To adjust the setup time of SDA before SCL rising edge, IICDS has to be written before clearing the IIC interrupt pending bit.
4. IICCLK is determined by IICCON[6].
   Tx clock can vary by SCL transition time.
   When IICCON[6]=0, IICCON[3:0]=0x0 or 0x1 is not available.
5. If the IICCON[5]=0, IICCON[4] does not operate correctly.
   So, It is recommended that you should set IICCON[5]=1, although you does not use the IIC interrupt.

MULTI-MASTER IIC-BUS CONTROL/STATUS (IICSTAT) REGISTER

Register	Address	R/W	Description	Reset Value
IICSTAT	0x54000004	R/W	IIC-Bus control/status register	0x0

IICSTAT	Bit	Description	Initial State
Mode selection	[7:6]	IIC-bus master/slave Tx/Rx mode select bits. 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode	00
Busy signal status / START STOP condition	[5]	IIC-Bus busy signal status bit. 0: read) Not busy (when read) write) STOP signal generation 1: read) Busy (when read) write) START signal generation. The data in IICDS will be transferred automatically just after the start signal.	0
Serial output	[4]	IIC-bus data output enable/disable bit. 0: Disable Rx/Tx, 1: Enable Rx/Tx	0
Arbitration status flag	[3]	IIC-bus arbitration procedure status flag bit. 0: Bus arbitration successful 1: Bus arbitration failed during serial I/O	0
Address-as-slave status flag	[2]	IIC-bus address-as-slave status flag bit. 0: Cleared when START/STOP condition was detected 1: Received slave address matches the address value in the IICADD	0
Address zero status flag	[1]	IIC-bus address zero status flag bit. 0: Cleared when START/STOP condition was detected 1: Received slave address is 00000000b.	0
Last-received bit status flag	[0]	IIC-bus last-received bit status flag bit. 0: Last-received bit is 0 (ACK was received). 1: Last-received bit is 1 (ACK was not received).	0

MULTI-MASTER IIC-BUS ADDRESS (IICADD) REGISTER

Register	Address	R/W	Description	Reset Value
IICADD	0x54000008	R/W	IIC-Bus address register	0xXX

IICADD	Bit	Description	Initial State
Slave address	[7:0]	7-bit slave address, latched from the IIC-bus. When serial output enable = 0 in the IICSTAT, IICADD is write-enabled. The IICADD value can be read any time, regardless of the current serial output enable bit (IICSTAT) setting. Slave address : [7:1] Not mapped : [0]	XXXXXXXX

MULTI-MASTER IIC-BUS TRANSMIT/RECEIVE DATA SHIFT (IICDS) REGISTER

Register	Address	R/W	Description	Reset Value
IICDS	0x5400000C	R/W	IIC-Bus transmit/receive data shift register	0xXX

IICDS	Bit	Description	Initial State
Data shift	[7:0]	8-bit data shift register for IIC-bus Tx/Rx operation. When serial output enable = 1 in the IICSTAT, IICDS is write-enabled. The IICDS value can be read any time, regardless of the current serial output enable bit (IICSTAT) setting.	XXXXXXXX

MULTI-MASTER IIC-BUS LINE CONTROL(IICLC) REGISTER

Register	Address	R/W	Description	Reset Value
IICLC	0x54000010	R/W	IIC-Bus multi-master line control register	0x00

IICLC	Bit	Description	Initial State
Filter enable	[2]	IIC-bus filter enable bit. When SDA port is operating as input, this bit should be High. This filter can prevent from occurred error by a glitch during double of PCLK time. 0: Filter disable 1: Filter enable	0
SDA output delay	[1:0]	IIC-Bus SDA line delay length selection bits. SDA line is delayed as following clock time(PCLK) 00: 0 clocks 01: 5 clocks 10: 10 clocks 11: 15 clocks	00

19 SPI INTERFACE

OVERVIEW

The S3C2443X Serial Peripheral Interface (SPI) can interface the serial data transfer. The SPI has two 8-bit shift registers for transmission and receiving. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). And SPI also supports Tx and Rx FIFO mode respectively for consecutive data transfer. 8-bit serial data at a frequency is determined by its corresponding control register settings. If you only want to transmit, received data can be dummy. Otherwise, if you only want to receive, you should transmit dummy '1' data.

There are 4 I/O pin signals associated with SPI transfers: the SCK (SPICLK1), the MISO (SPIMISO1) data line, the MOSI (SPIMOSI1) data line, and the active low /SS (nSS1) pin (input).

FEATURES

— SPI Protocol (ver. 2.11) compatible

— 8-bit Shift Register for transmit

— 8-bit Shift Register for receive

— Support 16-Byte Tx/Rx FIFO mode respectively

— 8-bit Prescaler logic

— Polling, Interrupt, and DMA transfer mode

BLOCK DIAGRAM

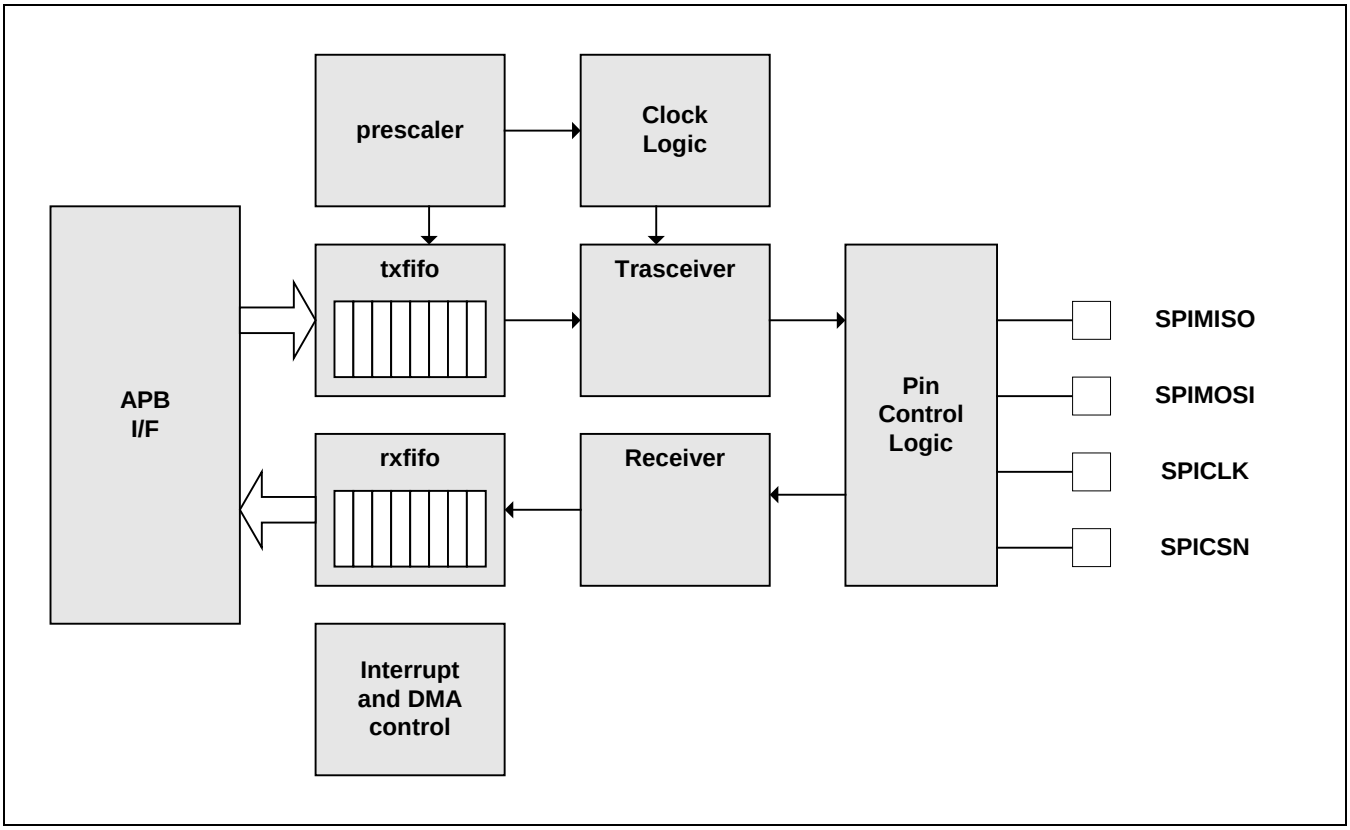


Figure 19-1. SPI Block Diagram

SPI OPERATION

Using the SPI interface, 8-bit data can be sent and received simultaneously to/from an external device. A serial clock line synchronizes shifting and sampling of the information on the two serial data lines. When SPI is the master, transmit frequency can be controlled by setting the appropriate bit to SPPREn register. User can modify its frequency to adjust the baud rate data register value. When SPI is used as a slave mode, external master supplies the operating clock. When a programmer writes byte data to SPTDATn register, SPI transmit and receive operation will start simultaneously. In some cases, nSS should be activated before writing byte data to SPTDATn.

PROGRAMMING PROCEDURE

When a byte data is written into the SPTDATn register, SPI starts to transmit if ENSCK and MSTR of SPCONn register are set. You can use a typical programming procedure to operate an SPI card.

To program the SPI modules, follow these basic steps:

1. Set Baud Rate Prescaler Register (SPPREn).
2. Set SPCONn to configure properly the SPI module.
3. Write data 0xFF to SPTDATn 10 times in order to initialize MMC or SD card.
4. Set a GPIO pin, which acts as nSS, low to activate the MMC or SD card.
5. Tx data → Check the status of Transfer Ready flag (REDY_org =1), and then write data to SPTDATn.
6. Rx data : SPCONn's TAGD bit enable = Tx Auto Garbage Data mode
   → confirm REDY to set, and then read data from Read Buffer (First 2 datas are garbages)
7. Set a GPIO pin, which acts as nSS, high to deactivate the MMC or SD card.

SPI Transfer Format

The S3C2443X supports 4 different format to transfer the data. Figure 19-2 shows four waveforms for SPICLK.

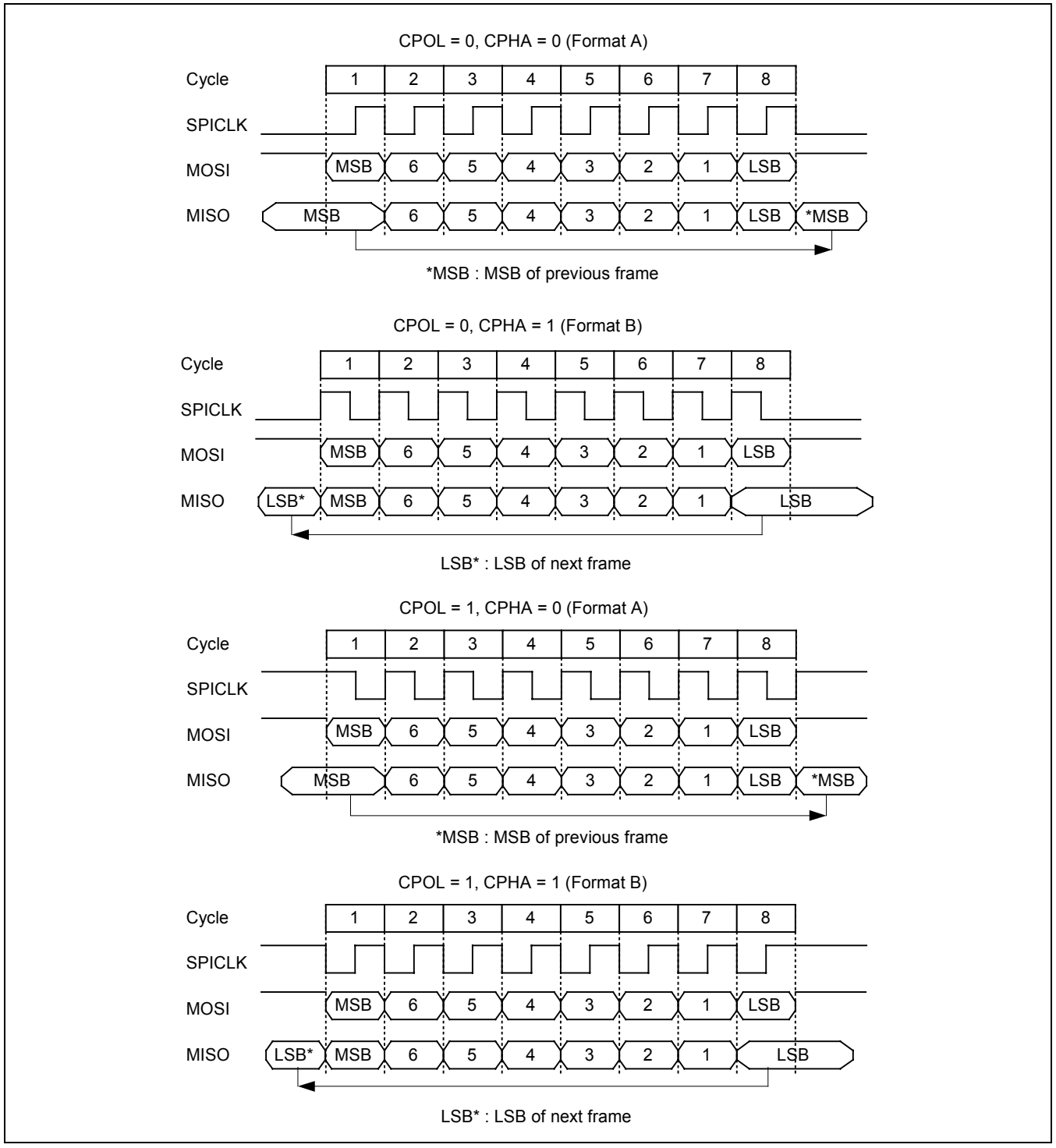


Figure 19-2. SPI Transfer Format

Transmitting Procedure by DMA

1. The SPI is configured as DMA mode.
2. SPI is configured as DMA mode.
3. SPI requests DMA service.
4. DMA transmits 1byte data to the SPI.
5. SPI transmits the data to card.
6. Return to Step 3 until DMA count becomes 0.
7. SPI is configured as interrupt or polling mode with SMOD bits.

Receiving Procedure by DMA

1. SPI is configured with TAGD bit set.
2. Read 2 times for dummy byte pull out.
3. SPI is configured as DMA start with SMOD bits.
4. DMA is configured properly.
5. SPI receives 1byte data from card.
6. SPI requests DMA service.
7. DMA receives the data from the SPI.
8. Write data 0xFF automatically to SPTDATn.
9. Return to Step 6 until DMA count becomes 0.
10. SPI is configured as polling mode with SMOD bits.
11. If SPSTAn's READY flag is set, then read the last byte data.

NOTE:

Total received data = the first 2 data in polling mode + DMA TC values + the last data in polling mode (Step 11).
The first two DMA received datas are dummy and the user can neglect it.
The last data can be neglected

SPI Slave Rx Mode with Format B

If the SPI slave Rx mode is activated and SPI format is set to format B, then SPI operation will be failed:

The READY signal, one of internal signals, becomes high before the SPI_CNT reaches 0. Therefore, in DMA mode, DATA_READ signal is generated before the last data is latched.

Guide

1) DMA mode: This mode cannot be used at SPI slave Rx mode with format B.
2) Polling mode:
   DATA_READ signal should be delayed by 1phase of SPICLK at SPI slave Rx mode with format B.
3) Interrupt mode:
   DATA_READ signal should be delayed 1phase of SPICLK at SPI slave Rx mode with format B.

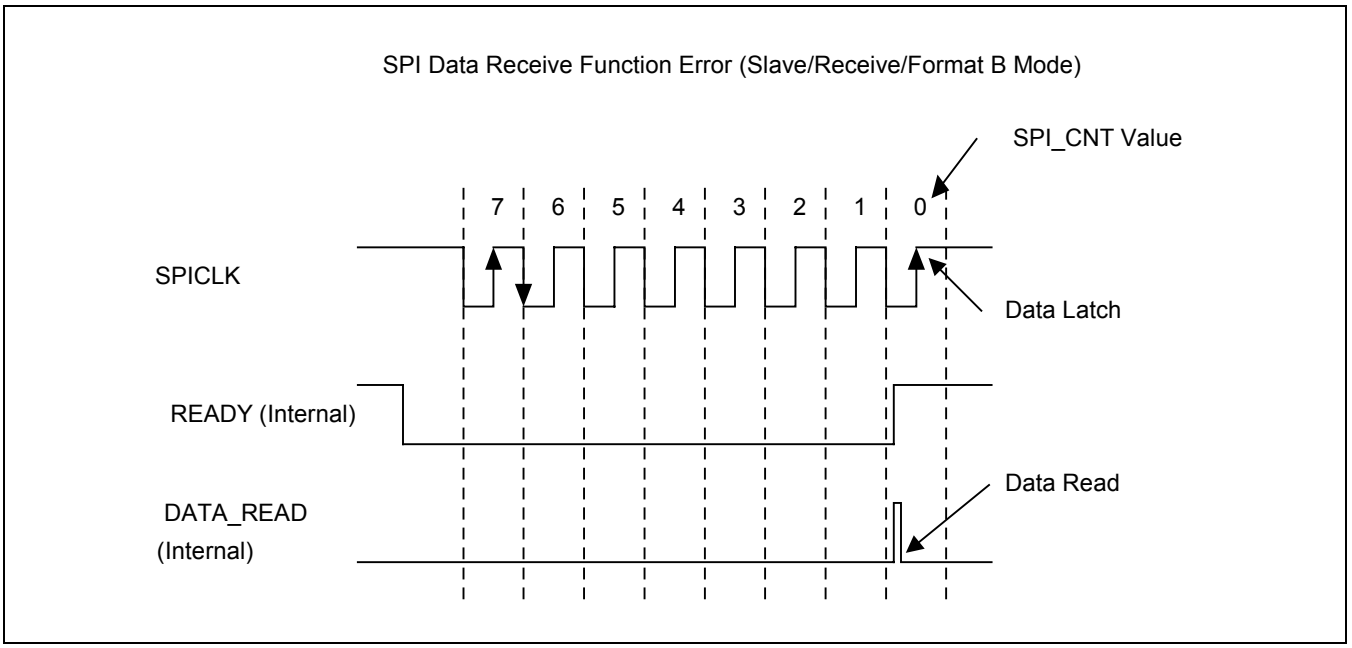


Figure 19-3. SPI Slave Rx mode with Format B (1-Byte Buffer mode)

SPI SPECIAL REGISTERS

SPI CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
SPCON1	0x59000000	R/W	SPI Channel 1 Control Register	0x0008

SPCONn	Bit	Description	Initial State
Reserved	[31:17]	-	
TBTOCEN	[16]	Rx FIFO Trailing Bytes Timeout Counter Enable 0=Disable, 1=Enable (Auto cleared when timeout counter reached the timeout value)	0
RXFIFORB	[15:14]	Rx FIFO Remaining Byte control (almost full control) ‘00’=2-byte, ‘01’=4-byte, ‘10’=12-byte, ‘11’=14-byte	00
TXFIFORB	[13:12]	Tx FIFO Remaining Byte control (almost empty control) ‘00’=2-byte, ‘01’=4-byte, ‘10’=12-byte, ‘11’=14-byte	00
RXFIFORST	[11]	Rx FIFO Reset control When set to 1 = Rx FIFO software reset, auto cleared	0
TXFIFORST	[10]	Tx FIFO Reset control When set to 1 = Tx FIFO software reset, auto cleared.	0
SPI Rx FIFO Enable (RXFIFOEN)	[9]	Rx FIFO Enable 0= Rx FIFO path disable (So, Rx path is for Byte Access mode) 1= Rx FIFO path enable	0
SPI Tx FIFO Enable (TXFIFOEN)	[8]	Tx FIFO Enable 0=Tx FIFO path disable (So, Tx path is for Byte Access mode) 1=Tx FIFO path enable	0
SPI Direction (DIRC)	[7]	Transfer Direction 0=Tx, 1=Rx 1) Byte Access mode : When Rx mode, this bit should be set to High 2) FIFO mode: When this bit is high, SPICLK out for receiving data	0
SPI Mode Select (SMOD)	[6:5]	Determines how and by what SPTDAT is read/written 00 = polling mode, 01 = interrupt mode 10 = Buffer DMA mode using DREQ_TXFIFO, DACK_TXFIFO ports, 11 = Buffer DMA mode using DREQ_RXFIFO, DACK_RXFIFO ports Note: When this buffer transmit DMA mode is used, the FIFO DMA should not be used.	00

SPCONn	Bit	Description	Initial State
SCK Enable (ENSCK)	[4]	Determines what you want SCK enable or not(only master) 0 = disable, 1 = enable	0
Master/Slave Select (MSTR)	[3]	Determines what mode you want master or slave 0 = slave, 1 = master **NOTE:** In slave mode, there should be set up time for master to initiate Tx / Rx.	1
Clock Polarity Select (CPOL)	[2]	Determines an active high or active low clock. 0 = active high, 1 = active low	0
Clock Phase Select(CPHA)	[1]	This bit selects one of two fundamentally different transfer formats. 0 = format A, 1 = format B	0
Tx Auto Garbage Data mode enable (TAGD)	[0]	This bit decides whether the receiving data only needs or not. 0 = normal mode, 1 = Tx auto garbage data mode **NOTE:** In normal mode, you only want to receive data, you should transmit dummy 0xFF data. 1) Byte Access mode : when this bit is 'H', SPI clock is out whenever read operation is done. When write operation, don't care 2) FIFO Access mode : don't care	0

NOTES :

1. Chip selection (nCSI) must be accomplished after CPOL and CPHA is chosen
2. RXFIFORST, TXFIFORST, RXFIFOEN, TXFIFOEN bit write access is allowed when the REDY_org (Status register bit 3) is high.
3. SMOD field should be set to polling mode(2'b00) when TX or RXFIFO DMA mode is used.

SPI STATUS REGISTER

Register	Address	R/W	Description	Reset Value
SPSTA1	0x59000004	R	SPI Channel 1 Status Register	0x00100439

SPSTAn	Bit	Description	Initial State
Reserved	[31:29]	-	0
RXFRAV	[28:24]	Rx FIFO read available byte count 0x00 = No byte remain, (Rx FIFO empty state) 0x01 ~ 0x0f = 1 ~ 15 byte remain in the RxFIFO 0x10 = 16 byte remain in the RxFIFO (Rx FIFO full state)	0x00
Reserved	[23:21]	-	
TXFWAV	[20:16]	Tx FIFO write available byte count 0x00 = No byte remain (Tx FIFO full state), 0x01 ~ 0x0f = 1 ~ 15 byte remain in the TxFIFO, 0x10 = 16 byte remain in the TxFIFO (Tx FIFO empty state)	0x10
Reserved	[15:13]	-	
TBTISTS	[12]	Rx FIFO Trailing Bytes Timeout interrupt status bit 0=Not occurred 1= Occurred trailing bytes timeout interrupt (Write to 1 cleared)	0
RXFIFOAF	[11]	Rx FIFO Almost Full Remaining bytes are RXFIFORB field in the SPCON[15:14] 0=Rx FIFO not almost full, 1=Rx FIFO almost full	0
TXFIFOAE	[10]	Tx FIFO Almost Empty Remaining bytes are TXFIFORB field in the SPCON[13:12] 0=Tx FIFO not almost empty, 1=Tx FIFO almost empty	1
RXFIFOFERR	[9]	Rx FIFO full error 0=nomal, 1=Rx FIFO full error Note : When Master mode, if RxFIFO is full, Rx block do not write to RxFIFO.	0
TXFIFOEERR	[8]	Tx FIFO empty error 0=nomal, 1=Tx FIFO empty error Note : When Master mode, if TxFIFO is empty, Tx block do not read from TxFIFO.	0
RXFIFOFULL	[7]	Rx FIFO full 0=Rx FIFO not full, 1=Rx FIFO full	0

SPSTAn	Bit	Description	Initial State
RXFIFO NEMPTY	[6]	Rx FIFO not empty 0=Rx FIFO empty, 1=Rx FIFO not empty	0
TXFIFONFULL	[5]	Tx FIFO not full 0=Tx FIFO full, 1=Tx FIFO not full	1
TXFIFOEMPTY	[4]	Tx FIFO empty 0=Tx FIFO not empty, 1=Tx FIFO empty	1
Transfer Ready Flag PRE (REDY_org)	[3]	Rx Pre Buffer Transfer Ready Flag This bit indicates that SPTDATn or SPRDATBn is ready to transmit or receive. This flag is automatically cleared by writing data to SPTDATn when Tx mode and by reading data from SPRDATBn when Rx mode. 0 = not ready, 1 = data Tx/Rx ready	1
Data Collision Error Flag(DCOL)	[2]	This flag is set if the SPTDATn is written or the SPRDATBn is read while a transfer is in progress and cleared by reading the SPSTAn. 0 = not detect, 1 = collision error detect	0
Reserved	[1]	Reserved	0
Transfer Ready Flag (REDY)	[0]	This bit indicates that SPRDATn(Rx 2nd buffer) is ready to receive. This flag is automatically cleared by writing data to SPTDATn when Tx mode and by reading data from SPRDATn when Rx mode. 0 = not ready, 1 = data Tx/Rx ready	1

NOTES:

1. **When Master Tx FIFO mode is used**, TXFIFOEERR field has no meaning.
2. **When Master Rx FIFO mode is used**, RXFIFOFERR field has no meaning.

SPI PIN CONTROL REGISTER

When the SPI system is enabled, the direction of pins is controlled by MSTR bit of SPCON1 register. If the SPI is configured as a Slave, nSS pin is used to chip select input pin by one master. If the SPI is configured as a Master, nSS pin can be used to chip select output pin to external slave device.

Register	Address	R/W	Description	Reset Value
SPPIN1	0x59000008	R/W	SPI Channel 1 Pin Control Register	0x02

SPPINn	Bit	Description	Initial State
Reserved	[7:5]	-	
FIFODOUTCTL	[4]	FIFO Data Out Control 0=Normal, 1=Data out byte extention enable	0
FDCKEN	[3]	Feedback Clock enable 0=Disable, 1=Enable Note : Only in master mode, Rx block may use feedback SPI clock.	0
Multi Master error detect Enable (ENMUL)	[2]	The /SS pin is used as an input to detect multi master error when the SPI system is a master. 0 = disable(general purpose), 1 = multi master error detect enable	0
CS out	[1]	Master mode Chip select output (active low) 0=Chip select active, 1=Chip select inactive Note : Only in master mode this bit is to output port.	1
Master Out Keep(KEEP)	[0]	Determines MOSI drive or release when 1byte transmit finish(only master) 0 = release, 1 = drive the previous level	0

The SPIMISO(MISO) and SPIMOSI(MOSI) data pins are used for transmitting and receiving serial data. When the SPI is configured as a master, SPIMISO(MISO) is the master data input line, SPIMOSI(MOSI) is the master data output line, SPISSN is the chip select output, and SPICLK(SCK) is the clock output line. When as a slave, these pins reverse roles.

SPI Baud Rate Prescaler Register

Register	Address	R/W	Description	Reset Value
SPPRE1	0x5900000C	R/W	SPI Cannel 1 Baud Rate Prescaler Register	0x00

SPPREn	Bit	Description	Initial State
Prescaler Value	[7:0]	Determines SPI clock rate as above equation. Baud rate = PCLK / 2 / (Prescaler value + 1)	0x00

NOTE: Baud rate should be less than 25 MHz.

SPI Tx Data Register

Register	Address	R/W	Description	Reset Value
SPTDAT1	0x59000010	R/W	SPI Channel 1 Tx Data Register	0x00

SPTDATn	Bit	Description	Initial State
Tx Data Register	[7:0]	This field contains the data byte to be transmitted over the SPI channel (when TxFIFO is not enabled)	0x00

SPI Rx Data Register

Register	Address	R/W	Description	Reset Value
SPRDAT1	0x59000014	R	SPI Channel 1 Rx Data Register	0x00

SPRDATn	Bit	Description	Initial State
Rx Data Register	[7:0]	This field contains the data to be received over the SPI channel (Second byte Rx Buffer)	0x00

SPI TxFIFO Data Register

Register	Address	R/W	Description	Reset Value
SPTXFIFO1	0x59000018	W	SPI Channel 1 Tx FIFO Register	0x00

SPRDATn	Bit	Description	Initial State
Tx FIFO Data Register	[7:0]	This field contains the data to be transferred when TXFIFO is enabled.	0x00

SPI RxFIFO Data Register

Register	Address	R/W	Description	Reset Value
SPRXFIFO1	0x5900001C	R	SPI Channel 1 Rx FIFO Register	0x00

SPRXFIFOn	Bit	Description	Initial State
Rx FIFO Data Register	[7:0]	This field contains the data to be transferred when TXFIFO is enabled.	0x00

SPI Pre-Data Register

Register	Address	R/W	Description	Reset Value
SPRDATB1	0x59000020	R	SPI Channel 1 Rx Data Register	0x00

SPRDATBn	Bit	Description	Initial State
Rx Data Register	[7:0]	This field contains the data to be received over the SPI channel : First byte Rx Buffer, before transmitted to SPRDAT register	0x00

SPI FIFO Interrupt/DMA Control Register

Register	Address	R/W	Description	Reset Value
SPFIC1	0x59000024	R/W	SPI Channel 1 FIFO Interrupt and DMA control Register	0x00

SPFICn	Bit	Description	Initial State
Reserved	[15:12]	-	0
RXFIFO DMACTL	[11:10]	Rx FIFO DMA Control register 00=disable, 01=RxFIFO not empty, 10=RxFIFO almost full 11=reserved	10
TXFIFO DMACTL	[9:8]	Tx FIFO DMA Control register 00=disable, 01=TxFIFO empty, 10=TxFIFO almost empty 11=reserved	10
TOCIE	[7]	Rx FIFO Time-out Counter Interrupt Enable 0=disable, 1=enable	0
RXFIFONEMIE	[6]	Rx FIFO Not Empty Interrupt Enable 0=disable, 1=enable	0
RXFIFOAFIE	[5]	Rx FIFO Almost Full Interrupt Enable 0=disable, 1=enable	0
TXFIFOAEIE	[4]	Tx FIFO Almost Empty Interrupt Enable 0=disable, 1=enable	0
RXFIFOFEIE	[3]	Rx FIFO Full Error Interrupt Enable Receiver tries to write into the Rx FIFO when full state. 0=disable, 1=enable	0
TXFIFOEEIE	[2]	Tx FIFO Empty Error Interrupt Enable Transmitter tries to read from the Tx FIFO when empty state. 0=disable, 1=enable	0
RXFIFOFLIE	[1]	Rx FIFO Full Interrupt Enable 0=disable, 1=enable	0
TXFIFOEMIE	[0]	Tx FIFO Empty Interrupt Enable 0=disable, 1=enable	0

Note : Tx FIFO DMA request condition

1. Tx FIFO empty
2. **Tx FIFO almost empty** : TxFIFO almost empty state is defined in the register field TxFIFORB (SPCON[13:12]), recommended setting is 4-byte.

Rx FIFO DMA request condition

3. Rx FIFO not empty
4. **Rx FIFO not almost full** : RxFIFO almost full state is defined in the register field RxFIFORB(SPCON[15:14]), recommended setting is 4-byte.

NOTE:

When Master Rx FIFO mode is used and RXFIFODMACTL is set to 2'b10 (RxFIFO almost full, 4-byte setting), 4-byte burst operation is requested to the DMA Controller. In this mode, DCON register APBANI field of the DMA Controller should be set to High (fixed address out when burst 4 mode). DMA Controller is external SPI module.

SPI Timeout Value Register

Register	Address	R/W	Description	Reset Value
SPTOV1	0x59000028	R/W	SPI Channel 1 Rx FIFO Timeout Value Register	0x00

SPTOCn	Bit	Description	Initial State
Reserved	[31:24]	-	0
TOV	[23:0]	Rx FIFO Timeout Counter Value register	000000

NOTES

20 HS_SPI CONTROLLER

OVERVIEW

The High Speed Serial Peripheral Interface (HS_SPI) can interface the serial data transfer. HS_SPI has two 8-bit shift registers for transmission and receiving, respectively. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). HS_SPI supports the protocols for National Semiconductor Microwire and Motorola Serial Peripheral Interface.

FEATURES

The features of the HS_SPI are:

- Supports full duplex
- 8-bit shift register for TX/RX
- 8-bit prescale logic
- 3 clock source
- Supports 8-bit/32-bit bus interface
- Supports the Motorola SPI protocol and National Semiconductor Microwire
- Two independent transmit and receive FIFOs, each 16 samples deep by 32-bits wide
- Master-mode and Slave-mode
- Receive-without-transmit operation

BLOCK DIAGRAM

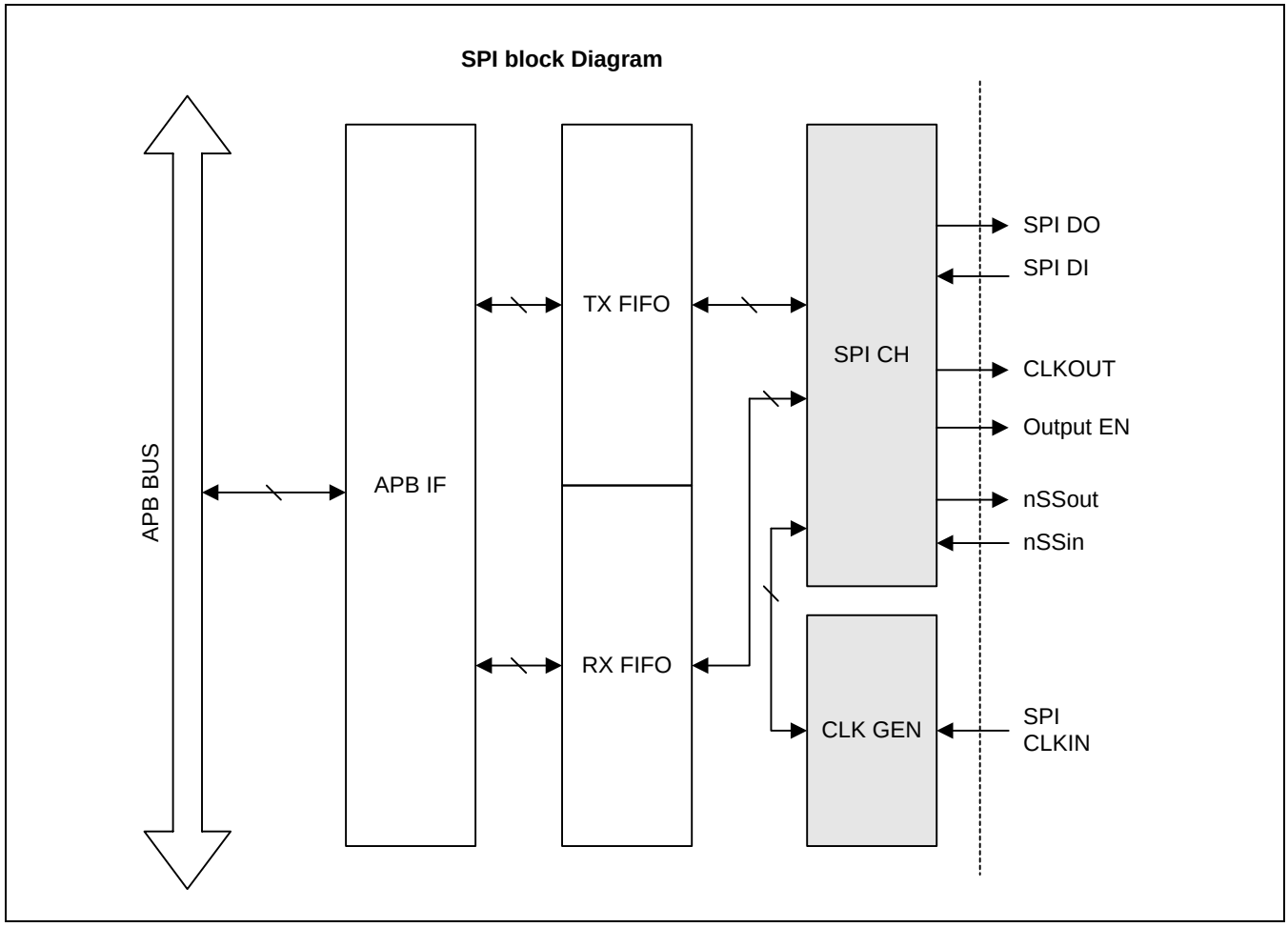


Figure 20-1. HS-SPI Interface block diagram

SIGNAL DESCRIPTION

The following table lists the external signals between the SPI and external device. All ports of the SPI can be used as General Purpose I/O ports when disable. See “General Purpose I/O” chapter for detailed pin configuration.

Table 20-1. External signals description

Name	Direction	Description
PSPICLK0	Inout	PSPICLK0 is the serial clock used to control time to transfer data.
PSPIMISO0	Inout	In Master mode, this port is to be input port to get data from slave output port. Data are transmitted to master through this port when in slave mode.
PSPIMOSI0	Inout	In Master mode, this port is to be output port to transfer data from master output port. Data are received from master through this port when in slave mode.
PSS	Inout	As to be slave selection signal, all data TX/RX sequences are executed when PSS is low.

OPERATION

The SPI in S3C2443x transfers 1-bit serial data between S3C2443x and external device. The SPI in S3C2443x supports that CPU or DMA can access to transmit or receive FIFOs separately and to transfer data in both direction simultaneously.

CPU(or DMA) should write data on the register SPI_TX_DATA to write data in FIFO. Data on the register are automatically moved to Tx FIFOs. To read data from Rx FIFOs, CPU(or DMA) should access the register SPI_RX_DATA and then data are automatically sent to the register SPI_RX_DATA.

FIFO access

The SPI in S3C2443x supports CPU access and DMA access to FIFOs. Data size of CPU access and DMA access to FIFOs can be selected either 8-bit or 32-bit data. If 8-bit data size is chosen, valid bits are from 0 bit to 7 bit. CPU accesses are normally on and off by trigger threshold user defines. The trigger level of each FIFOs is set from 0byte to 64bytes. TxDMAOn or RxDMAOn bit of SPI_MODE_CFG register should be set to use DMA access. DMA access supports only single transfer and 4 burst transfer. In TX FIFO, dma request signal is high until that FIFO is full. In RX FIFO, dma request signal is high if FIFO is not empty.

Trailing Bytes in the Rx FIFO

When the number of samples in Rx FIFO is less than the threshold value in INT mode or DMA 4 burst mode and no additional data is received, the remaining bytes are called trailing bytes. To remove these bytes in RX FIFO, internal timer and interrupt signal are used. The value of internal timer can be set up to 1024 clocks based on APB BUS clock. When timer value is to be zero, interrupt signal is occurred and CPU can remove trailing bytes in FIFO.

SPI TRANSFER FORMAT

The S3C2443X supports 4 different format to transfer the data. Figure 27-2 shows four waveforms for SPICLK.

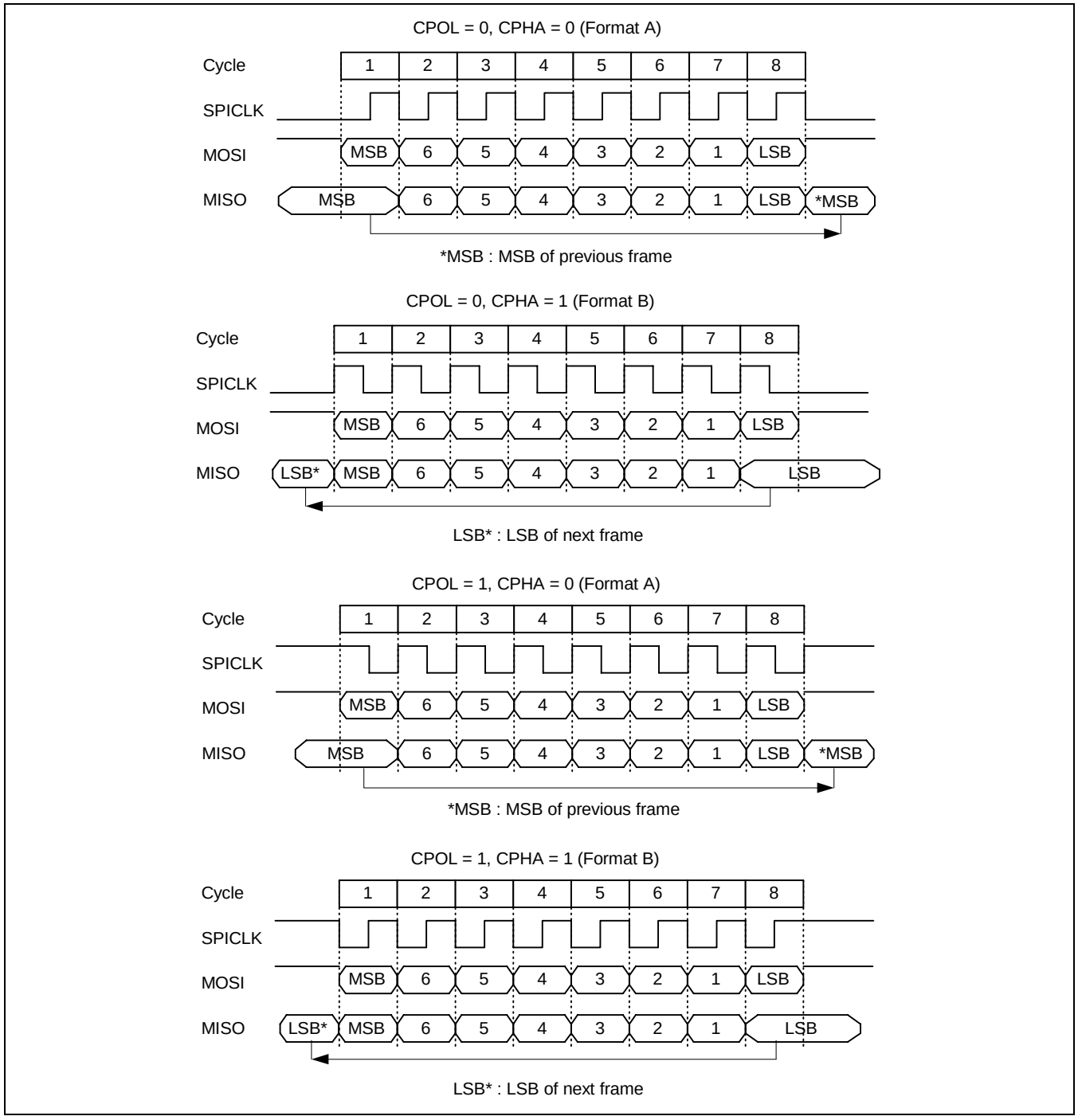


Figure 20-2. HS-SPI Transfer Format

SEQUENCE OF SPECIAL FUNCTION REGISTER

Special Function Register should be set as the following sequence.

1. Bit[31] of MISCCR register should be set to 1.
   (In GPIO chapter MISCELLANEOUS CONTROL REGISTER)
2. Set Transfer Type. (CPOL & CPHA set)
3. Set Clock configuration register.
4. Set SPI MODE configuration register.
5. Set SPI INT_EN register.
6. Set Packet Count configuration register if necessary.
7. Set Tx or Rx Channel on.
8. Set nSS low to start Tx or Rx operation.

REGISTER DESCRIPTIONS

Register	Address	R/W	Description	Reset Value
CH_CFG	0x52000000	R/W	SPI configuration register	0x0

CH_CFG	Bit	R/W	Description	Initial State
SW_RST	[5]	R/W	Software reset	1'b0
SLAVE	[4]	R/W	Whether SPI Channel is Master or Slave 0: Master 1: Slave	1'b0
CPOL	[3]	R/W	Determine an active high or active low clock 0: active high 1: active low	1'b0
CPHA	[2]	R/W	Select one of the two fundamentally different transfer format 0: format A 1: format B	1'b0
RxChOn	[1]	R/W	SPI Rx Channel On 0: Channel Off 1: Channel On	1'b0
TxChOn	[0]	R/W	SPI Tx Channel On 0: Channel Off 1: Channel On	1'b0

Register	Address	R/W	Description	Reset Value
Clk_CFG	0x52000004	R/W	Clock configuration register	0x0

Clk_CFG	Bit	R/W	Description	Initial State
ClkSel	[10:9]	R/W	Clock source selection to generate SPI clock-out 00 : PCLK 11 : Epll 10 : USBHOST clock	2'b0
ENCLK	[8]	R/W	Clock on/off 0 : disable 1 : enable	1'b0
Prescaler Value	[7:0]	R/W	SPI clock-out division rate SPI clock-out = Clock source / (2 x (Prescaler value +1))	8'h0

Register	Address	R/W	Description	Reset Value
MODE_CFG	0x52000008	R/W	SPI FIFO control register	0x0

MODE_CFG	Bit		Description	Initial State
Trailing Count	[28:19]	R/W	Count value from writing the last data in RX FIFO to flush trailing bytes in FIFO	10'b0
BUS transfer size	[18]	R/W	Transfer size between BUS and FIFO 0 : byte 1 : word	2'b0
FB_Clk_sel	[17]	-	Feedback clock additional delay 0 : 0 ns delay 1 : 2ns delay -	-
RxTrigger	[16:11]	R/W	Rx FIFO trigger level in INT mode. Trigger level is from 6'h0 to 6'h40. The value means byte number in RX FIFO	6'b0
TxTrigger	[10:5]	R/W	Tx FIFO trigger level in INT mode Trigger level is from 6'h0 to 6'h40. The value means byte number in TX FIFO	6'b0
Clk_term_en	[4]	R/W	Insertion 1 period of SPI clock-out between packet and packet 0 : continuous SPI clock-out 1 : discontinuous SPI clock-out	0
reserved	[3]	-	-	-
RxDMA On	[2]	R/W	DMA mode on/off 0 : DMA mode off 1 : DMA mode on	1'b0
TxDMA On	[1]	R/W	DMA mode on/off 0 : DMA mode off 1 : DMA mode on	1'b0
DMA transfer	[0]	R/W	DMA transfer type, single or 4 bust. 0 : single 1 : 4 burst DMA transfer size should be set as the same size in DMA as it in SPI.	1'b0

Register	Address	R/W	Description	Reset Value
Slave_slection_reg	0x5200000C	R/W	Slave selection signal	0x1

MODE_CFG	Bit		Description	Initial State
nSSout	[0]	R/W	Slave selection signal	1'b1

Register	Address	R/W	Description	Reset Value
SPI_INT_EN	0x52000010	R/W	SPI Interrupt Enable register	0x0

SPI_INT_EN	Bit		Description	Initial State
IntEnTrailing	[6]	R/W	Interrupt Enable for trailing count to be zero	1'b0
IntEnRxOverrun	[5]	R/W	Interrupt Enable for RxOverrun	1'b0
IntEnRx Underrun	[4]	R/W	Interrupt Enable for RxUnderrun	1'b0
IntEnTxOverrun	[3]	R/W	Interrupt Enable for TxOverrun	1'b0
IntEnTxUnderrun	[2]	R/W	Interrupt Enable for TxUnderrun	1'b0
IntEnRxFifoRdy	[1]	R/W	Interrupt Enable for RxFifoRdy(INT mode)	1'b0
IntEnTxFifoRdy	[0]	R/W	Interrupt Enable for TxFifoRdy(INT mode)	1'b0

Register	Address	R/W	Description	Reset Value
SPI_STATUS	0x52000014	R	SPI status register	0x0

SPI_STATUS	Bit		Description	Initial State
TX_DONE	[21]	R	Indication of transfer done in Shift register 0 : all case except blow case 1 : when tx fifo and shift register are empty	1'b0
Trailing_byte	[20]	R	Indication that trailing count is zero	1'b0
RxFifoLvl	[19:13]	R	Data level in RX FIFO 0 ~ 7'h40 byte	7'b0
TxFifoLvl	[12:6]	R	Data level in TX FIFO 0 ~ 7'h40 byte	7'b0
RxOverrun	[5]	R	Rx FIFO Overrun Error 0 : no error 1 : error	1'b0
RxUnderrun	[4]	R	Rx FIFO Underrun Error 0 : no error 1 : error	1'b0
TxOverrun	[3]	R	Tx FIFO Overrun Error 0 : no error 1 : error	1'b0
TxUnderrun	[2]	R	Tx FIFO Underrun Error 0 : no error 1 : error	1'b0
RxFifoRdy	[1]	R	0 : data in FIFO less than trigger level 1 : data in FIFO more than trigger level	1'b0
TxFifoRdy	[0]	R	0 : data in FIFO more than trigger level 1 : data in FIFO less than trigger level	1'b0

Register	Address	R/W	Description	Reset Value
SPI_TX_DATA	0x52000018	W	SPI TX DATA register	0x0

SPI_TX_DATA	Bit		Description	Initial State
TX_DATA	[31:0]	W	DATA to transmit through SPI Channel	32'b0

Register	Address	R/W	Description	Reset Value
SPI_RX_DATA	0x5200001C	R	SPI RX DATA register	0x0

SPI_RX_DATA	Bit		Description	Initial State
RX_DATA	[31:0]	R	DATA to transmit through SPI Channel	32'b0

Register	Address	R/W	Description	Reset Value
Packet_Count_reg	0x52000020	R/W	Count how many data master gets	0x0

Packet_Count_reg	Bit		Description	Initial State
Packet_Count_En	[16]	R/W	To select to count packet received or not 0 : not to count 1 : to count	1'b0
Count Value	[15:0]	R/W	The number of Packet to be received	16'b0

Register	Address	R/W	Description	Reset Value
Pending_clr_reg	0x52000024	R/W	Pending clear register	0x0

Packet_Count_ reg	Bit		Description	Initial State
TX_underrun_clr	[4]	R/W	TX underrun status clear bit 0 : not to clear 1 : to clear	1'b0
TX_overrun_clr	[3]	R/W	TX overrun status clear bit 0 : not to clear 1 : to clear	1'b0
RX_underrun_clr	[2]	R/W	RX underrun status clear bit 0 : not to clear 1 : to clear	1'b0
RX_overrun_clr	[1]	R/W	RX overrun status clear bit 0 : not to clear 1 : to clear	1'b0
Trailing_clr	[0]	R/W	Trailing status clear bit 0 : not to clear 1 : to clear	1'b0

NOTES

21 CSTN LCD DISPLAY CONTROLLER

OVERVIEW

The LCD controller in the S3C2443X01 consists of the logic for transferring LCD image data from a video buffer located in system memory to an external LCD driver.

The LCD controller supports monochrome, 2-bit per pixel (4-level gray scale) or 4-bit per pixel (16-level gray scale) mode on a monochrome LCD, using a time-based dithering algorithm and Frame Rate Control (FRC) method and it can be interfaced with a color LCD panel at 8-bit per pixel (256-level color) and 12-bit per pixel (4096-level color) for interfacing with STN LCD.

It can support 1-bit per pixel, 2-bit per pixel, 4-bit per pixel, and 8-bit per pixel for interfacing with the palletized TFT color LCD panel, and 16-bit per pixel and 24-bit per pixel for non-palletized true-color display.

The LCD controller can be programmed to support different requirements on the screen related to the number of horizontal and vertical pixels, data line width for the data interface, interface timing, and refresh rate.

FEATURES

STN LCD Displays:

— Supports 3 types of LCD panels: 4-bit dual scan, 4-bit single scan, and 8-bit single scan display type

— Supports the monochrome, 4 gray levels, and 16 gray levels

— Supports 256 colors and 4096 colors for color STN LCD panel

— Supports multiple screen size
Typical actual screen size: 640 x 480, 320 x 240, 160 x 160, and others
Maximum virtual screen size is 4Mbytes.
Maximum virtual screen size in 256 color mode: 4096 x 1024, 2048 x 2048, 1024 x 4096, and others

COMMON FEATURES

The LCD controller has a dedicated DMA that supports to fetch the image data from video buffer located in system memory. Its features also include:

— Dedicated interrupt functions (INT_FrSyn and INT_FiCnt)

— The system memory is used as the display memory.

— Supports Multiple Virtual Display Screen (Supports Hardware Horizontal/Vertical Scrolling)

— Programmable timing control for different display panels

— Supports little and big-endian byte ordering, as well as WinCE data formats

NOTE:

WinCE doesn't support the 12-bit packed data format.
Please check if WinCE can support the 12-bit color-mode.

EXTERNAL INTERFACE SIGNAL

STN
VFRAME (Frame sync. Signal)
VLINE (Line sync pulse signal)
VCLK (Pixel clock signal)
VD[23:0] (LCD pixel data output ports)
VM (AC bias signal for LCD driver)

BLOCK DIAGRAM

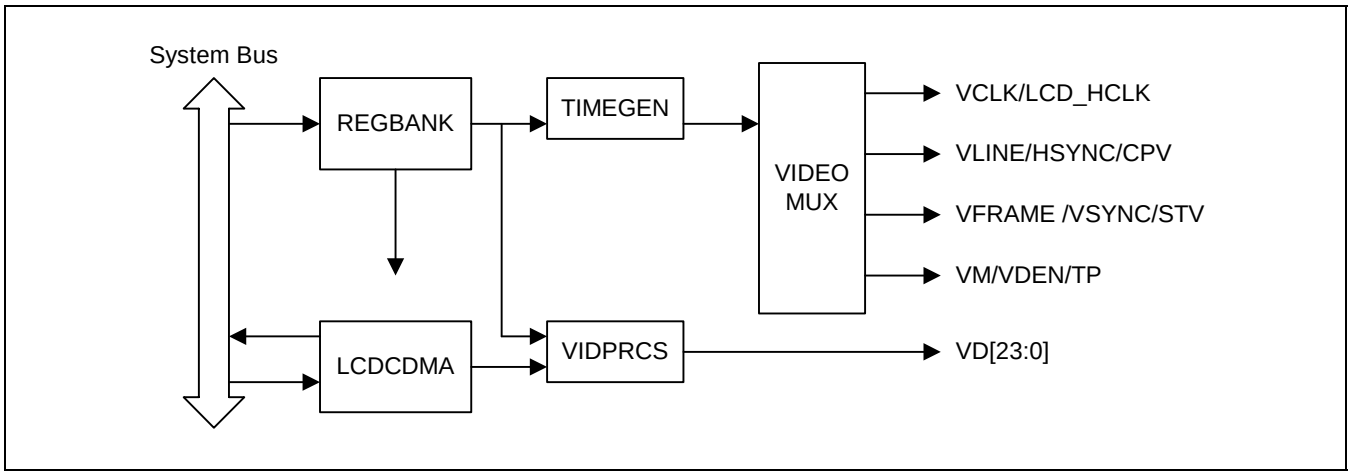


Figure 21-1. LCD Controller Block Diagram

The S3C2443X01 LCD controller is used to transfer the video data and to generate the necessary control signals, such as VFRAME, VLINE, VCLK, VM, and so on. In addition to the control signals, the S3C244X01 has the data ports for video data, which are VD[23:0] as shown in Figure 21-1. The LCD controller consists of a REGBANK, LCDCDMA, VIDPRCS, TIMEGEN (See the Figure 21-1 LCD Controller Block Diagram). The REGBANK has 17 programmable register sets and 256x16 palette memory which are used to configure the LCD controller. The LCDCDMA is a dedicated DMA, which can transfer the video data in frame memory to LCD driver automatically. By using this special DMA, the video data can be displayed on the screen without CPU intervention. The VIDPRCS receives the video data from the LCDCDMA and sends the video data through the VD[23:0] data ports to the LCD driver after changing them into a suitable data format, for example 4/8-bit single scan or 4-bit dual scan display mode. The TIMEGEN consists of programmable logic to support the variable requirements of interface timing and rates commonly found in different LCD drivers. The TIMEGEN block generates VFRAME, VLINE, VCLK, VM, and so on.

The description of data flow is as follows:

FIFO memory is present in the LCDCDMA. When FIFO is empty or partially empty, the LCDCDMA requests data fetching from the frame memory based on the burst memory transfer mode (consecutive memory fetching of 4 words (16 bytes) per one burst request without allowing the bus mastership to another bus master during the bus transfer). When the transfer request is accepted by bus arbitrator in the memory controller, there will be four successive word data transfers from system memory to internal FIFO. The total size of FIFO is 28 words, which consists of 12 words FIFOL and 16 words FIFOH, respectively. The S3C2443X01 has two FIFOs to support the dual scan display mode. In case of single scan mode, one of the FIFOs (FIFOH) can only be used.

STN LCD CONTROLLER OPERATION

TIMING GENERATOR (TIMEGEN)

The TIMEGEN generates the control signals for the LCD driver, such as VFRAME, VLINE, VCLK, and VM. These control signals are closely related to the configuration on the LCDCON1/2/3/4/5 registers in the REGBANK. Based on these programmable configurations on the LCD control registers in the REGBANK, the TIMEGEN can generate the programmable control signals suitable to support many different types of LCD drivers.

The VFRAME pulse is asserted for the duration of the entire first line at a frequency of once per frame. The VFRAME signal is asserted to bring the LCD's line pointer to the top of the display to start over.

The VM signal helps the LCD driver alternate the polarity of the row and column voltages, which are used to turn the pixel on and off. The toggling rate of VM signals depends on the MMODE bit of the LCDCON1 register and MVAL field of the LCDCON4 register. If the MMODE bit is 0, the VM signal is configured to toggle on every frame. If the MMODE bit is 1, the VM signal is configured to toggle on the every event of the elapse of the specified number of VLINE by the MVAL[7:0] value. Figure 21-4 shows an example for MMODE=0 and for MMODE=1 with the value of MVAL[7:0]=0x2. When MMODE=1, the VM rate is related to MVAL[7:0], as shown below:

VM Rate = VLINE Rate / (2 x MVAL)

The VFRAME and VLINE pulse generation relies on the configurations of the HOZVAL field and the LINEVAL field in the LCDCON2/3 registers. Each field is related to the LCD size and display mode. In other words, the HOZVAL and LINEVAL can be determined by the size of the LCD panel and the display mode according to the following equation:

HOZVAL = (Horizontal display size / Number of the valid VD data line)-1
In color mode: Horizontal display size = 3 x Number of Horizontal Pixel

In the 4-bit single scan display mode, the Number of valid VD data line should be 4. In case of 4-bit dual scan display, the Number of valid VD data lineshould also be 4 while in case of 8-bit single scan display mode, the Number of valid VD data line should be 8.

LINEVAL = (Vertical display size) -1: In case of single scan display type
LINEVAL = (Vertical display size / 2) -1: In case of dual scan display type

The rate of VCLK signal depends on the configuration of the CLKVAL field in the LCDCON1 register. Table 21-1 defines the relationship of VCLK and CLKVAL. The minimum value of CLKVAL is 2.

VCLK(Hz)=HCLK/(CLKVAL x 2)

The frame rate is the VFRAM signal frequency. The frame rate is closely related to the field of WLH[1:0](VLINE pulse width) WDLY[1:0] (the delay width of VCLK after VLINE pulse), HOZVAL, LINEBLANK, and LINEVAL in the LCDCON1/2/3/4 registers as well as VCLK and HCLK. Most LCD drivers need their own adequate frame rate. The frame rate is calculated as follows:

frame_rate(Hz) = 1 / [{ (1/VCLK) x (HOZVAL+1)+(1/HCLK) x (**A**+**B**+(LINEBLANK x 8)) } x (LINEVAL+1)]

$$\boldsymbol{A} = 2^{(4+WLH)},\ \boldsymbol{B} = 2^{(4+WDLY)}$$

Table 21-1. Relation Between VCLK and CLKVAL (STN, HCLK = 60MHz)

CLKVAL	60MHz/X	VCLK
2	60 MHz/4	15.0 MHz
3	60 MHz/6	10.0 MHz
:	:	:
1023	60 MHz/2046	29.3 kHz

VIDEO OPERATION

The S3C2443X01 LCD controller supports 8-bit color mode (256 color mode), 12-bit color mode (4096 color mode), 4 level gray scale mode, 16 level gray scale mode as well as the monochrome mode. For the gray or color mode, it is required to implement the shades of gray level or color according to time-based dithering algorithm and Frame Rate Control (FRC) method. The selection can be made following a programmable lockup table, which will be explained later. The monochrome mode bypasses these modules (FRC and lookup table) and basically serializes the data in FIFOH (and FIFOL if a dual scan display type is used) into 4-bit (or 8-bit if a 4-bit dual scan or 8-bit single scan display type is used) streams by shifting the video data to the LCD driver.

The following sections describe the operation on the gray and color mode in terms of the lookup table and FRC.

Lookup Table

The S3C2443X01 can support the lookup table for various selection of color or gray level mapping, ensuring flexible operation for users. The lookup table is the palette which allows the selection on the level of color or gray (Selection on 4-gray levels among 16 gray levels in case of 4 gray mode, selection on 8 red levels among 16 levels, 8 green levels among 16 levels and 4 blue levels among 16 levels in case of 256 color mode). In other words, users can select 4 gray levels among 16 gray levels by using the lookup table in the 4 gray level mode. The gray levels cannot be selected in the 16 gray level mode; all 16 gray levels must be chosen among the possible 16 gray levels. In case of 256 color mode, 3 bits are allocated for red, 3 bits for green and 2 bits for blue. The 256 colors mean that the colors are formed from the combination of 8 red, 8 green and 4 blue levels (8x8x4 = 256). In the color mode, the lookup table can be used for suitable selections. Eight red levels can be selected among 16 possible red levels, 8 green levels among 16 green levels, and 4 blue levels among 16 blue levels. In case of 4096 color mode, there is no selection as in the 256 color mode.

Gray Mode Operation

The S3C2443X01 LCD controller supports two gray modes: 2-bit per pixel gray (4 level gray scale) and 4-bit per pixel gray (16 level gray scale). The 2-bit per pixel gray mode uses a lookup table (BLUELUT), which allows selection on 4 gray levels among 16 possible gray levels. The 2-bit per pixel gray lookup table uses the BULEVAL[15:0] in Blue Lookup Table (BLUELUT) register as same as blue lookup table in color mode. The gray level 0 will be denoted by BLUEVAL[3:0] value. If BLUEVAL[3:0] is 9, level 0 will be represented by gray level 9 among 16 gray levels. If BLUEVAL[3:0] is 15, level 0 will be represented by gray level 15 among 16 gray levels, and so on. Following the same method as above, level 1 will also be denoted by BLUEVAL[7:4], the level 2 by BLUEVAL[11:8], and the level 3 by BLUEVAL[15:12]. These four groups among BLUEVAL[15:0] will represent level 0, level 1, level 2, and level 3. In 16 gray levels, there is no selection as in the 16 gray levels.

256 Level Color Mode Operation

The S3C2443X01 LCD controller can support an 8-bit per pixel 256 colors display mode. The color display mode can generate 256 levels of color using the dithering algorithm and FRC. The 8-bit per pixel are encoded into 3-bits for red, 3-bits for green, and 2-bits for blue. The color display mode uses separate lookup tables for red, green, and blue. Each lookup table uses the REDVAL[31:0] of REDLUT register, GREENVAL[31:0] of GREENLUT register, and BLUEVAL[15:0] of BLUELUT register as the programmable lookup table entries.

Similar to the gray level display, 8 group or field of 4 bits in the REDLUR register, i.e., REDVAL[31:28], REDLUT[27:24], REDLUT[23:20], REDLUT[19:16], REDLUT[15:12], REDLUT[11:8], REDLUT[7:4], and REDLUT[3:0], are assigned to each red level. The possible combination of 4 bits (each field) is 16, and each red level should be assigned to one level among possible 16 cases. In other words, the user can select the suitable red level by using this type of lookup table. For green color, the GREENVAL[31:0] of the GREENLUT register is assigned as the lookup table, as was done in the case of red color. Similarly, the BLUEVAL[15:0] of the BLUELUT register is also assigned as a lookup table. For blue color, 2 bits are allocated for 4 blue levels, different from the 8 red or green levels.

4096 Level Color Mode Operation

The S3C2443X01 LCD controller can support a 12-bit per pixel 4096 color display mode. The color display mode can generate 4096 levels of color using the dithering algorithm and FRC. The 12-bit per pixel are encoded into 4-bits for red, 4-bits for green, and 4-bits for blue. The 4096 colors display mode does not use lookup tables.

DITHERING AND FRAME RATE CONTROL

In case of STN LCD display (except monochrome), video data must be processed by a dithering algorithm. The DITHFRC block has two functions, such as Time-based Dithering Algorithm for reducing flicker and Frame Rate Control (FRC) for displaying gray and color level on the STN panel. The main principle of gray and color level display on the STN panel based on FRC is described. For example, to display the third gray (3/16) level from a total of 16 levels, the 3 times pixel should be on and 13 times pixel off. In other words, 3 frames should be selected among the 16 frames, of which 3 frames should have a pixel-on on a specific pixel while the remaining 13 frames should have a pixel-off on a specific pixel. These 16 frames should be displayed periodically. This is basic principle on how to display the gray level on the screen, so-called gray level display by FRC. The actual example is shown in Table 15-2. To represent the 14th gray level in the table, we should have a 6/7 duty cycle, which mean that there are 6 times pixel-on and one time pixel-off. The other cases for all gray levels are also shown in Table 21-2.

In the STN LCD display, we should be reminded of one item, i.e., Flicker Noise due to the simultaneous pixel-on and -off on adjacent frames. For example, if all pixels on first frame are turned on and all pixels on next frame are turned off, the Flicker Noise will be maximized. To reduce the Flicker Noise on the screen, the average probability of pixel-on and -off between frames should be the same. In order to realize this, the Time-based Dithering Algorithm, which varies the pattern of adjacent pixels on every frame, should be used. This is explained in detail. For the 16 gray level, FRC should have the following relationship between gray level and FRC. The 15th gray level should always have pixel-on, and the 14th gray level should have 6 times pixel-on and one times pixel-off, and the 13th gray level should have 4 times pixel-on and one times pixel-off, ,,,,,,,, , and the 0th gray level should always have pixel-off as shown in Table 21-2.

Table 21-2. Dither Duty Cycle Examples

Pre-Dithered Data (gray level number)	Duty Cycle	Pre-Dithered Data (gray level number)	Duty Cycle
15	1	7	1/2
14	6/7	6	3/7
13	4/5	5	2/5
12	3/4	4	1/3
11	5/7	3	1/4
10	2/3	2	1/5
9	3/5	1	1/7
8	4/7	0	0

Display Types

The LCD controller supports 3 types of LCD drivers: 4-bit dual scan, 4-bit single scan, and 8-bit single scan display mode. Figure 21-2 shows these 3 different display types for monochrome displays, and Figure 21-3 show these 3 different display types for color displays.

4-bit Dual Scan Display Type

A 4-bit dual scan display uses 8 parallel data lines to shift data to both the upper and lower halves of the display at the same time. The 4 bits of data in the 8 parallel data lines are shifted to the upper half and 4 bits of data is shifted to the lower half, as shown in Figure 21-2. The end of frame is reached when each half of the display has been shifted and transferred. The 8 pins (VD[7:0]) for the LCD output from the LCD controller can be directly connected to the LCD driver.

4-bit Single Scan Display Type

A 4-bit single scan display uses 4 parallel data lines to shift data to successive single horizontal lines of the display at a time, until the entire frame has been shifted and transferred. The 4 pins (VD[3:0]) for the LCD output from the LCD controller can be directly connected to the LCD driver, and the 4 pins (VD[7:4]) for the LCD output are not used.

8-bit Single Scan Display Type

An 8-bit single scan display uses 8 parallel data lines to shift data to successive single horizontal lines of the display at a time, until the entire frame has been shifted and transferred. The 8 pins (VD[7:0]) for the LCD output from the LCD controller can be directly connected to the LCD driver.

256 Color Displays

Color displays require 3 bits (Red, Green, and Blue) of image data per pixel, so the number of horizontal shift registers for each horizontal line corresponds to three times the number of pixels of one horizontal line. These results in a horizontal shift register of length 3 times the number of pixels per horizontal line. This RGB is shifted to the LCD driver as consecutive bits via the parallel data lines. Figure 21-3 shows the RGB and order of the pixels in the parallel data lines for the 3 types of color displays.

4096 Color Displays

Color displays require 3 bits (Red, Green, and Blue) of image data per pixel, and so the number of horizontal shift registers for each horizontal line corresponds to three times the number of pixels of one horizontal line. This RGB is shifted to the LCD driver as consecutive bits via the parallel data lines. This RGB order is determined by the sequence of video data in video buffers.

MEMORY DATA FORMAT (STN, BSWP = 0)

Mono 4-bit Dual Scan Display:

Video Buffer Memory:

	Address	Data
0000H	A[31:0]	
0004H	B[31:0]	
	•	
	•	
	•	
1000H	L[31:0]	
1004H	M[31:0]	
	•	
	•	
	•	

LCD Panel

A[31] A[30] ..... A[0] B[31] B[30] ..... B[0] .....

L[31] L[30] ..... L[0] M[31] M[30] ..... M[0] .....

Mono 4-bit Single Scan Display & 8-bit Single Scan Display:

Video Buffer Memory:

	Address	Data
0000H	A[31:0]	
0004H	B[31:0]	
0008H	C[31:0]	
	•	
	•	
	•	

LCD Panel

A[31] A[30] A[29] ..... A[0] B[31] B[30] ..... B[0] C[31] ..... C[0] .....

MEMORY DATA FORMAT (STN, BSWP=0) (Continued)

In 4-level gray mode, 2 bits of video data correspond to 1 pixel.

In 16-level gray mode, 4 bits of video data correspond to 1 pixel.

In 256 level color mode, 8 bits (3 bits of red, 3 bits of green, and 2 bits of blue) of video data correspond to 1 pixel. The color data format in a byte is as follows:

Bit [7:5]	Bit [4:2]	Bit[1:0]
Red	Green	Blue

In 4096 level color mode :

Packed 12 BPP color mode

12 bits (4 bits of red, 4 bits of green, 4 bits of blue) of video data correspond to 1 pixel. The following table shows color data format in words: (Video data must reside at 3 word boundaries (8 pixel), as follows)

RGB Order

DATA	[31:28]	[27:24]	[23:20]	[19:16]	[15:12]	[11:8]	[7:4]	[3:0]
Word #1	Red(1)	Green(1)	Blue(1)	Red(2)	Green(2)	Blue(2)	Red(3)	Green(3)
Word #2	Blue(3)	Red(4)	Green(4)	Blue(4)	Red(5)	Green(5)	Blue(5)	Red(6)
Word #3	Green(6)	Blue(6)	Red(7)	Green(7)	Blue(7)	Red(8)	Green(8)	Blue(8)

Unpacked 12 BPP color mode

12 bits (4 bits of red, 4 bits of green, 4 bits of blue) of video data correspond to 1 pixel. The following table shows color data format in words:

RGB Order

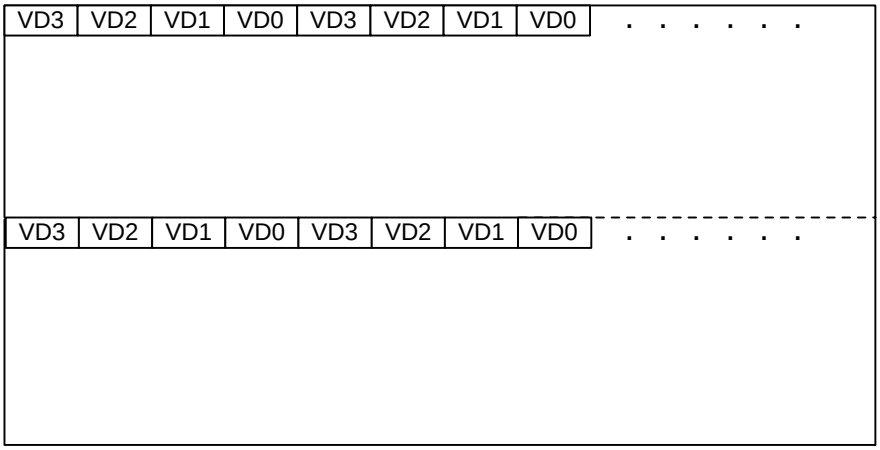
DATA	[31:28]	[27:24]	[23:20]	[19:16]	[15:12]	[11:8]	[7:4]	[3:0]
Word #1	–	Red(1)	Green(1)	Blue(1)	–	Red(2)	Green(2)	Blue(2)
Word #2	–	Red(3)	Green(3)	Blue(3)	–	Red(4)	Green(4)	Blue(4)
Word #3	–	Red(5)	Green(5)	Blue(5)	–	Red(6)	Green(6)	Blue(6)

16 BPP color mode

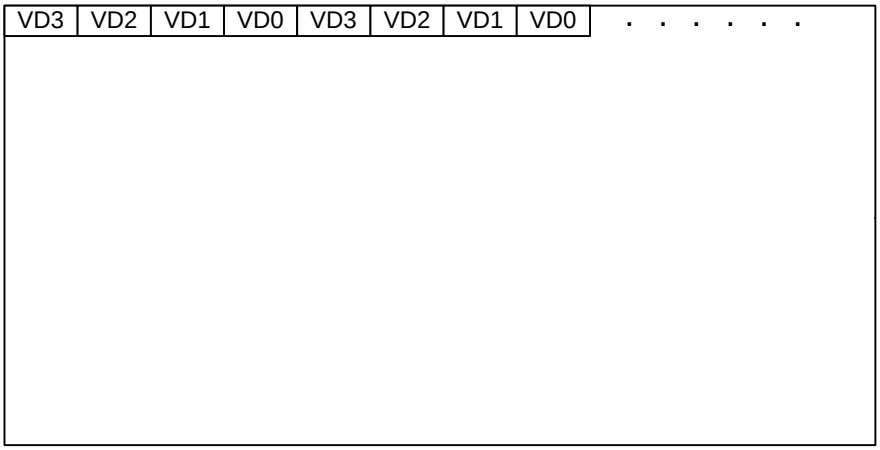
16 bits (5 bits of red, 6 bits of green, 5 bits of blue) of video data correspond to 1 pixel. But, stn controller will use only 12 bit color data. It means that only upper 4bit each color data will be used as pixel data (R[15:12], G[10:7], B[4:1]). The following table shows color data format in words:

RGB Order

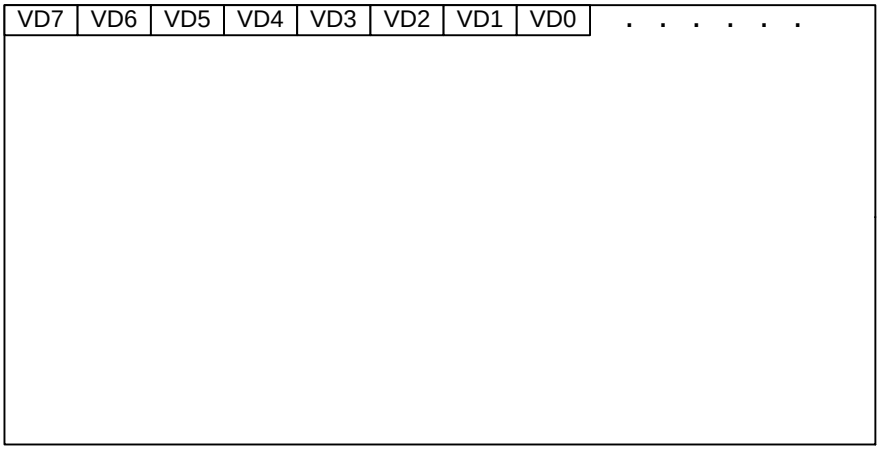
DATA	[31:28]	[27:21]	[20:16]	[15:11]	[10:5]	[4:0]
Word #1	Red(1)	Green(1)	Blue(1)	Red(2)	Green(2)	Blue(2)
Word #2	Red(3)	Green(3)	Blue(3)	Red(4)	Green(4)	Blue(4)
Word #3	Red(5)	Green(5)	Blue(5)	Red(6)	Green(6)	Blue(6)



4-bit Dual Scan Display

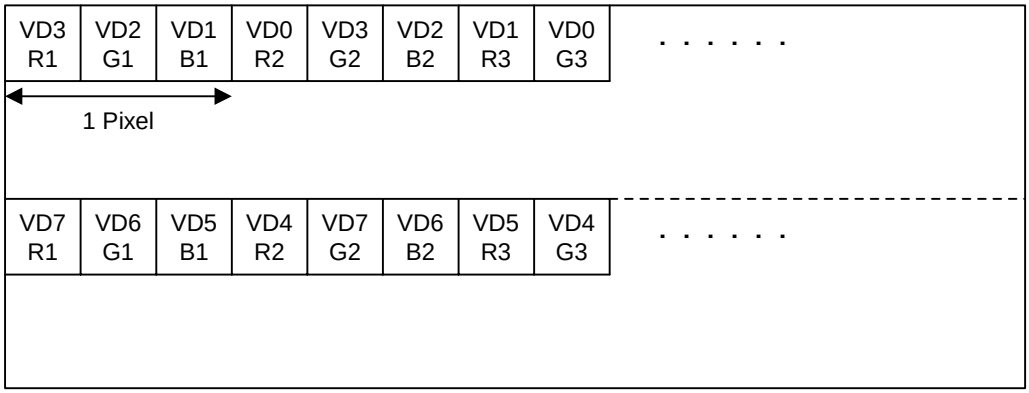


4-bit Single Scan Display

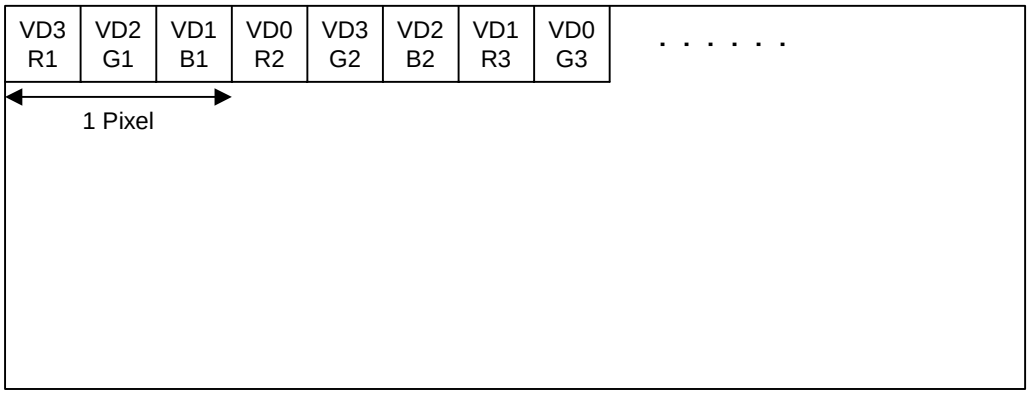


8-bit Single Scan Display

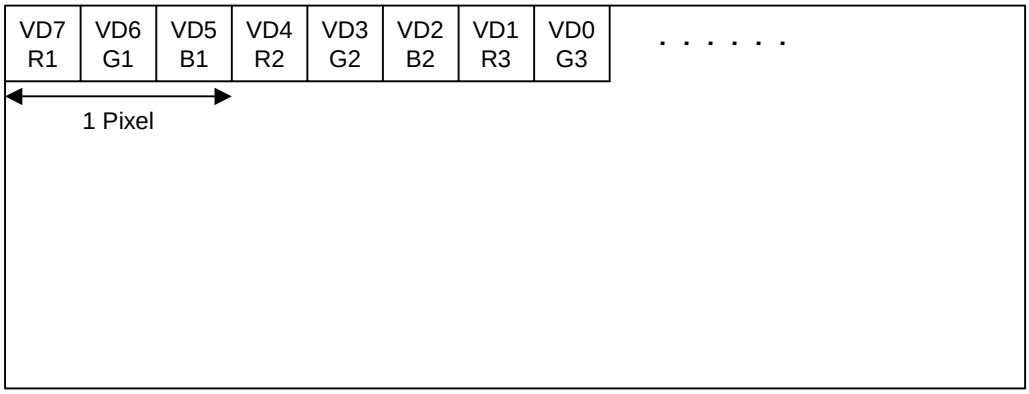
Figure 21-2. Monochrome Display Types (STN)



4-bit Dual Scan Display



4-bit Single Scan Display



8-bit Single Scan Display

Figure 21-3. Color Display Types (STN)

Timing Requirements

Image data should be transferred from the memory to the LCD driver using the VD[7:0] signal. VCLK signal is used to clock the data into the LCD driver's shift register. After each horizontal line of data has been shifted into the LCD driver's shift register, the VLINE signal is asserted to display the line on the panel.

The VM signal provides an AC signal for the display. The LCD uses the signal to alternate the polarity of the row and column voltages, which are used to turn the pixels on and off, because the LCD plasma tends to deteriorate whenever subjected to a DC voltage. It can be configured to toggle on every frame or to toggle every programmable number of VLINE signals.

Figure 21-4 shows the timing requirements for the LCD driver interface.

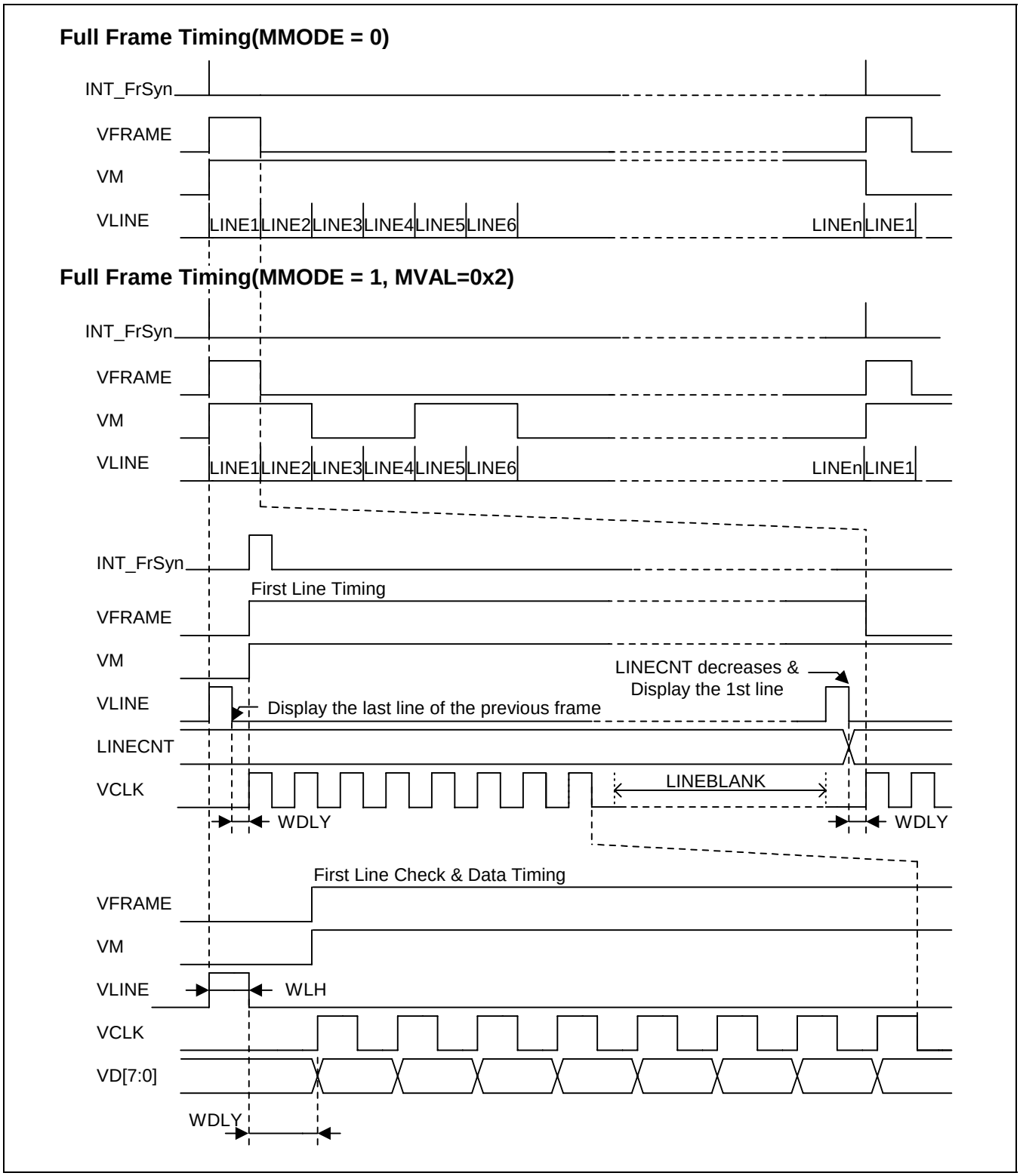


Figure 21-4. 8-bit Single Scan Display Type STN LCD Timing

-Virtual display (STN)

The S3C2443X01 supports hardware horizontal or vertical scrolling. If the screen is scrolled, the fields of LCDBASEU and LCDBASEL in LCDSADDR1/2 registers need to be changed (see Figure 21-8), except the values of PAGEWIDTH and OFFSIZE.
The video buffer in which the image is stored should be larger than the LCD panel screen in size.

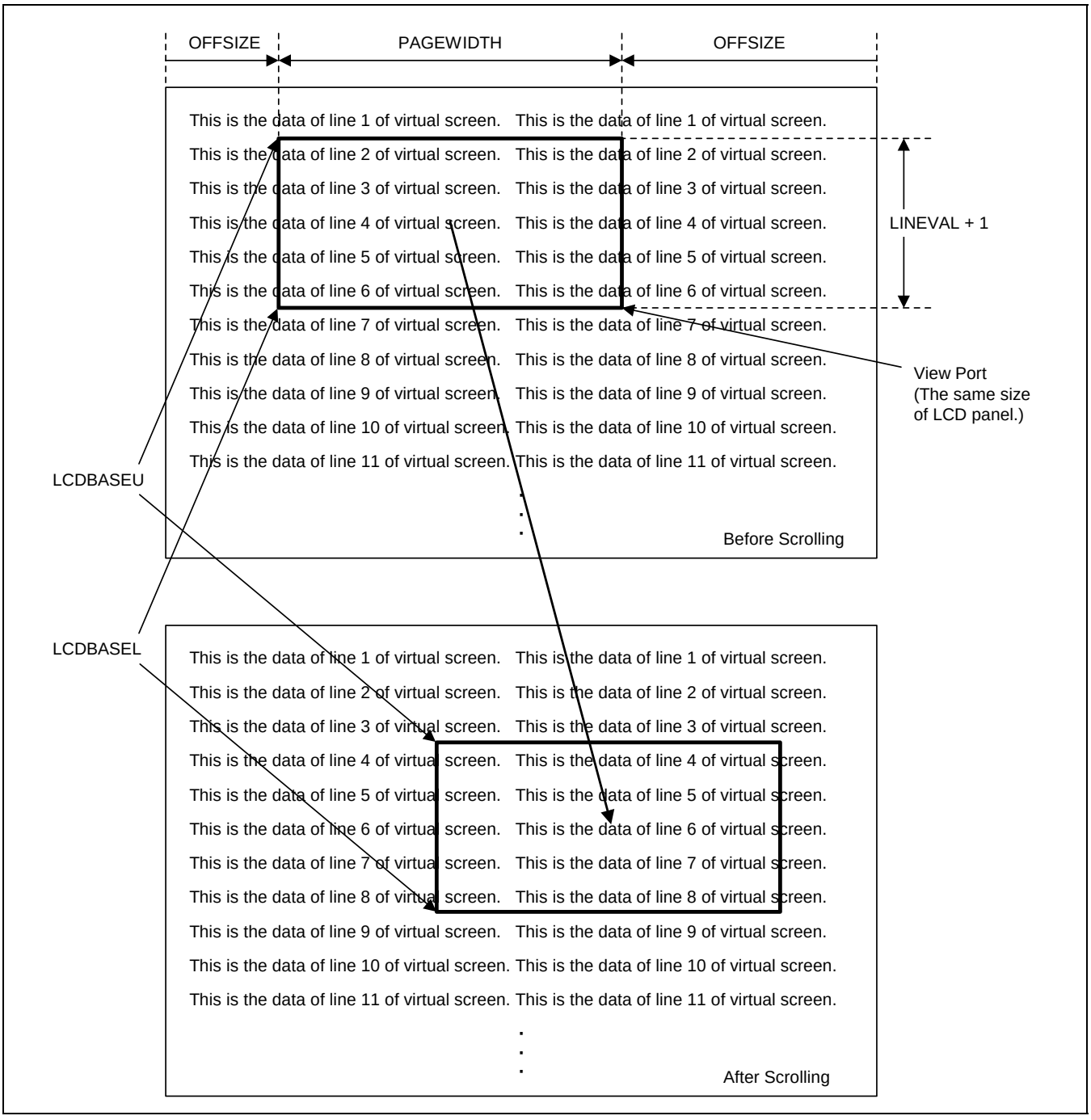


Figure 21-7. Example of Scrolling in Virtual Display (Single Scan)

PAD MUXING

Table 21-3. LCDCNTL (STN) / DISPCON (TFT) Port Muxing Table

PAD	VIDSEL	VIDOUT	Signals
LPC_VF	0	XX	LPC_RVSB / LPC_RVS / LPC_OE
	1	10	
		01	
		00	
VCLK	0	XX	LCD_VCLK
	1	10	SYS_WE
		01	VEN_FIELD
		00	RGB_VCLK
VLINE	0	XX	LCD_VLINE
	1	10	SYS_CS0
		01	VEN_HSYNC
		00	RGB_HSYNC
VFRAM	0	XX	LCD_VFRAME
	1	10	SYS_CS1
		01	VEN_VSYNC
		00	RGB_VSYNC
VM	0	XX	LCD_VM
	1	10	SYS_RS
		01	VEN_HREF
		00	RGB_VDEN
LEND	0	XX	LCD_LEND
	1	10	SYS_OE
		01	
		00	
VD	0	XX	LCD_VD
	1	10	VEN_DATA
		01	RGB_VD
		00	VDSYS

- VIDSEL register is defined in GPIO region
- VIDOUT registers are defined in VIDCON0[23:22] in DISPCON region

LCD CONTROLLER SPECIAL REGISTERS

MISCELLANEOUS control register (MISCCR) in GPIO (See GPIO SPECIAL REGISTERS Section)

Register	Address	R/W	Description	Reset Value
MISCCR	0x56000080	R/W	Miscellaneous control register	0x10020

MISCCR	Bit	Description	Reset Value
LCD_SEL	[28]	Select LCD controller (TFT / CSTN) for LCD output port 0: CSTN controller controls LCD output port. 1: TFT controller controls LCD output port.	0

LCD Control 1 Register

Register	Address	R/W	Description	Reset Value
LCDCON1	0X4D000000	R/W	LCD control 1 register	0x00000000

LCDCON1	Bit	Description	Initial State
LINECNT (read only)	[27:18]	Provide the status of the line counter. Down count from LINEVAL to 0	0000000000
CLKVAL	[17:8]	Determine the rates of VCLK and CLKVAL[9:0]. **STN**: VCLK = HCLK / (CLKVAL x 2) (CLKVAL ≥2)	0000000000
MMODE	[7]	Determine the toggle rate of the VM. 0 = Each Frame 1 = The rate defined by the MVAL	0
PNRMODE	[6:5]	Select the display mode. 00 = 4-bit dual scan display mode (STN) 01 = 4-bit single scan display mode (STN) 10 = 8-bit single scan display mode (STN) 11 = reserved	00
BPPMODE	[4:1]	Select the BPP (Bits Per Pixel) mode. 0000 = 1 bpp for STN, Monochrome mode 0001 = 2 bpp for STN, 4-level gray mode 0010 = 4 bpp for STN, 16-level gray mode 0011 = 8 bpp for STN, color mode (256 color) 0100 = packed 12 bpp for STN, color mode (4096 color) 0101 = unpacked 12 bpp for STN, color mode (4096 color) 0110 = 16 bpp for STN, color mode (4096 color)	0000
ENVID	[0]	LCD video output and the logic enable/disable. 0 = Disable the video output and the LCD control signal. 1 = Enable the video output and the LCD control signal.	0

LCD Control 2 Register

Register	Address	R/W	Description	Reset Value
LCDCON2	0X4D000004	R/W	LCD control 2 register	0x00000000

LCDCON2	Bit	Description	Initial State
VBPD	[31:24]	**STN**: These bits should be set to zero on STN LCD.	0x00
LINEVAL	[23:14]	**TFT/STN**: These bits determine the vertical size of LCD panel.	0000000000
VFPD	[13:6]	**STN**: These bits should be set to zero on STN LCD.	00000000
VSPW	[5:0]	**STN**: These bits should be set to zero on STN LCD.	000000

LCD Control 3 Register

Register	Address	R/W	Description	Reset Value
LCDCON3	0X4D000008	R/W	LCD control 3 register	0x00000000

LCDCON3	Bit	Description	Initial state
WDLY (STN)	[25:19]	**STN**: WDLY[1:0] bits determine the delay between VLINE and VCLK by counting the number of the HCLK. WDLY[7:2] are reserved. 00 = 16 HCLK, 01 = 32 HCLK, 10 = 48 HCLK, 11 = 64 HCLK	0000000
HOZVAL	[18:8]	**TFT/STN**: These bits determine the horizontal size of LCD panel. HOZVAL has to be determined to meet the condition that total bytes of 1 line are 4n bytes. If the x size of LCD is 120 dot in mono mode, x=120 cannot be supported because 1 line consists of 15 bytes. Instead, x=128 in mono mode can be supported because 1 line is composed of 16 bytes (2n). LCD panel driver will discard the additional 8 dot.	00000000000
LINEBLANK (STN)	[7:0]	**STN**: These bits indicate the blank time in one horizontal line duration time. These bits adjust the rate of the VLINE finely. The unit of LINEBLANK is HCLK x 8. Ex) If the value of LINEBLANK is 10, the blank time is inserted to VCLK during 80 HCLK.	0X00

Programming NOTE

: In case of STN LCD, (LINEBLANK + WLH + WDLY) value should be bigger than (14+12Tmax).

(LINEBLANK + WLH + WDLY) ¡ (14 + 8xT_{max1} + 4xT_{max2} = 14 + 12T_{max})

LEGEND:

(1) 14: SDRAM Auto refresh bus acquisition cycles

(2) 8x Tmax1 : Cache fill cycle X the Slowest Memory access time(Ex, ROM)

(3) 4x Tmax2 : 0xC~0xE address Frame memory Access time

LCD Control 4 Register

Register	Address	R/W	Description	Reset Value
LCDCON4	0X4D00000C	R/W	LCD control 4 register	0x00000000

LCDCON4	Bit	Description	Initial state
MVAL	[15:8]	**STN**: These bit define the rate at which the VM signal will toggle if the MMODE bit is set to logic '1'.	0X00
WLH(STN)	[7:0]	**STN**: WLH[1:0] bits determine the VLINE pulse's high level width by counting the number of the HCLK. WLH[7:2] are reserved. 00 = 16 HCLK, 01 = 32 HCLK, 10 = 48 HCLK, 11 = 64 HCLK	0X00

LCD Control 5 Register

Register	Address	R/W	Description	Reset Value
LCDCON5	0X4D000010	R/W	LCD control 5 register	0x00000000

LCDCON5	Bit	Description	Initial state
Reserved	[31:10]	This bit is reserved and the value should be '0'.	0
INVVCLK	[10]	**STN** : This bit controls the polarity of the VCLK active edge. 0 = The video data is fetched at VCLK falling edge 1 = The video data is fetched at VCLK rising edge	0
INVVLINE	[9]	**STN** : This bit indicates the VLINE/HSYNC pulse polarity. 0 = Normal 1 = Inverted	0
INVVFRAME	[8]	**STN** : This bit indicates the VFRAME/VSYNC pulse polarity. 0 = Normal 1 = Inverted	0
INVVD	[7]	**STN** : This bit indicates the VD (video data) pulse polarity. 0 = Normal 1 = VD is inverted.	0
Reserved	[6]	Reserved	0
INVPWREN	[5]	**STN**: This bit indicates the PWREN signal polarity. 0 = normal 1 = inverted	0
Reserved	[6]	Reserved	0
PWREN	[3]	**STN**: LCD_PWREN output signal enable/disable. 0 = Disable PWREN signal 1 = Enable PWREN signal	0
Reserved	[6]	Reserved	0
BSWP	[1]	**STN**: Byte swap control bit. 0 = Swap Disable 1 = Swap Enable	0
HWSWP	[0]	**STN**: Half-Word swap control bit. 0 = Swap Disable 1 = Swap Enable	0

FRAME Buffer Start Address 1 Register

Register	Address	R/W	Description	Reset Value
LCDSADDR1	0X4D000014	R/W	**STN/TFT**: Frame buffer start address 1 register	0x00000000

LCDSADDR1	Bit	Description	Initial State
LCDBANK	[29:21]	These bits indicate A[30:22] of the bank location for the video buffer in the system memory. LCDBANK value cannot be changed even when moving the view port. LCD frame buffer should be within aligned 4MB region, which ensures that LCDBANK value will not be changed when moving the view port. So, care should be taken to use the malloc() function.	0x00
LCDBASEU	[20:0]	For dual-scan LCD : These bits indicate A[21:1] of the start address of the upper address counter, which is for the upper frame memory of dual scan LCD or the frame memory of single scan LCD. For single-scan LCD : These bits indicate A[21:1] of the start address of the LCD frame buffer.	0x000000

FRAME Buffer Start Address 2 Register

Register	Address	R/W	Description	Reset Value
LCDSADDR2	0X4D000018	R/W	**STN/TFT**: Frame buffer start address 2 register	0x00000000

LCDSADDR2	Bit	Description	Initial State
LCDBASEL	[20:0]	For dual-scan LCD: These bits indicate A[21:1] of the start address of the lower address counter, which is used for the lower frame memory of dual scan LCD. For single scan LCD: These bits indicate A[21:1] of the end address of the LCD frame buffer. LCDBASEL = ((the frame end address) >>1) + 1 = LCDBASEU + (PAGEWIDTH+OFFSIZE) x (LINEVAL+1)	0x0000

NOTE: Users can change the LCDBASEU and LCDBASEL values for scrolling while the LCD controller is turned on. But, users must not change the value of the LCDBASEU and LCDBASEL registers at the end of FRAME by referring to the LINECNT field in LCDCON1 register, for the LCD FIFO fetches the next frame data prior to the change in the frame.
So, if you change the frame, the pre-fetched FIFO data will be obsolete and LCD controller will display an incorrect screen. To check the LINECNT, interrupts should be masked. If any interrupt is executed just after reading LINECNT, the read LINECNT value may be obsolete because of the execution time of Interrupt Service Routine (ISR).

FRAME Buffer Start Address 3 Register

Register	Address	R/W	Description	Reset Value
LCDSADDR3	0X4D00001C	R/W	**STN/TFT**: Virtual screen address set	0x00000000

LCDSADDR3	Bit	Description	Initial State
OFFSIZE	[21:11]	Virtual screen offset size (the number of half words). This value defines the difference between the address of the last half word displayed on the previous LCD line and the address of the first half word to be displayed in the new LCD line.	00000000000
PAGEWIDTH	[10:0]	Virtual screen page width (the number of half words). This value defines the width of the view port in the frame.	000000000

NOTE: The values of PAGEWIDTH and OFFSIZE must be changed when ENVID bit is 0.

Example 1. LCD panel = 320 x 240, 16gray, single scan
Frame start address = 0x0c500000
Offset dot number = 2048 dots (512 half words)

LINEVAL = 240-1 = 0xef
PAGEWIDTH = 320 x 4 / 16 = 0x50
OFFSIZE = 512 = 0x200
LCDBANK = 0x0c500000 >> 22 = 0x31
LCDBASEU = 0x100000 >> 1 = 0x80000
LCDBASEL = 0x80000 + (0x50 + 0x200) x (0xef + 1) = 0xa2b00

Example 2. LCD panel = 320 x 240, 16gray, dual scan
Frame start address = 0x0c500000
Offset dot number = 2048 dots (512 half words)

LINEVAL = 120-1 = 0x77
PAGEWIDTH = 320 x 4 / 16 = 0x50
OFFSIZE = 512 = 0x200
LCDBANK = 0x0c500000 >> 22 = 0x31
LCDBASEU = 0x100000 >> 1 = 0x80000
LCDBASEL = 0x80000 + (0x50 + 0x200) x (0x77 + 1) = 0x91580

Example 3. LCD panel = 320*240, color, single scan
Frame start address = 0x0c500000
Offset dot number = 1024 dots (512 half words)

LINEVAL = 240-1 = 0xef
PAGEWIDTH = 320 x 8 / 16 = 0xa0
OFFSIZE = 512 = 0x200
LCDBANK = 0x0c500000 >> 22 = 0x31
LCDBASEU = 0x100000 >> 1 = 0x80000
LCDBASEL = 0x80000 + (0xa0 + 0x200) x (0xef + 1) = 0xa7600

RED Lookup Table Register

Register	Address	R/W	Description	Reset Value
REDLUT	0X4D000020	R/W	**STN**: Red lookup table register	0x00000000

REDLUT	Bit	Description	Initial State
REDVAL	[31:0]	These bits define which of the 16 shades will be chosen by each of the 8 possible red combinations. 000 = REDVAL[3:0], 001 = REDVAL[7:4] 010 = REDVAL[11:8], 011 = REDVAL[15:12] 100 = REDVAL[19:16], 101 = REDVAL[23:20] 110 = REDVAL[27:24], 111 = REDVAL[31:28]	0x00000000

GREEN Lookup Table Register

Register	Address	R/W	Description	Reset Value
GREENLUT	0X4D000024	R/W	**STN**: Green lookup table register	0x00000000

GREENLUT	Bit	Description	Initial State
GREENVAL	[31:0]	These bits define which of the 16 shades will be chosen by each of the 8 possible green combinations. 000 = GREENVAL[3:0], 001 = GREENVAL[7:4] 010 = GREENVAL[11:8], 011 = GREENVAL[15:12] 100 = GREENVAL[19:16], 101 = GREENVAL[23:20] 110 = GREENVAL[27:24], 111 = GREENVAL[31:28]	0x00000000

BLUE Lookup Table Register

Register	Address	R/W	Description	Reset Value
BLUELUT	0X4D000028	R/W	**STN**: Blue lookup table register	0x0000

BULELUT	Bit	Description	Initial State
BLUEVAL	[15:0]	These bits define which of the 16 shades will be chosen by each of the 4 possible blue combinations. 00 = BLUEVAL[3:0], 01 = BLUEVAL[7:4] 10 = BLUEVAL[11:8], 11 = BLUEVAL[15:12]	0x0000

NOTE: Address from **0x14A0002C** to **0x14A00048** should not be used. This area is reserved for Test mode.

Dithering Mode Register

Register	Address	R/W	Description	Reset Value
DITHMODE	0X4D00004C	R/W	**STN**: Dithering mode register. This register reset value is 0x00000 But, user can change this value to 0x12210. (Refer to a sample program source for the latest value of this register.)	0x00000

DITHMODE	Bit	Description	Initial state
DITHMODE	[18:0]	Use one of following value for your LCD: 0x00000 or 0x12210	0x00000

LCD Interrupt Pending Register

Register	Address	R/W	Description	Reset Value
LCDINTPND	0X4D000054	R/W	Indicate the LCD interrupt pending register	0x0

LCDINTPND	Bit	Description	Initial state
INT_FrSyn	[1]	LCD frame synchronized interrupt pending bit. 0 = The interrupt has not been requested. 1 = The frame has asserted the interrupt request.	0
INT_FiCnt	[0]	LCD FIFO interrupt pending bit. 0 = The interrupt has not been requested. 1 = LCD FIFO interrupt is requested when LCD FIFO reaches trigger level.	0

LCD Source Pending Register

Register	Address	R/W	Description	Reset Value
LCDSRCPND	0X4D000058	R/W	Indicate the LCD interrupt source pending register	0x0

LCDSRCPND	Bit	Description	Initial state
INT_FrSyn	[1]	LCD frame synchronized interrupt source pending bit. 0 = The interrupt has not been requested. 1 = The frame has asserted the interrupt request.	0
INT_FiCnt	[0]	LCD FIFO interrupt source pending bit. 0 = The interrupt has not been requested. 1 = LCD FIFO interrupt is requested when LCD FIFO reaches trigger level.	0

LCD Interrupt Mask Register

Register	Address	R/W	Description	Reset Value
LCDINTMSK	0X4D00005C	R/W	Determine which interrupt source is masked. The masked interrupt source will not be serviced.	0x3

LCDINTMSK	Bit	Description	Initial state
FIWSEL	[2]	Determine the trigger level of LCD FIFO. 0 = 4 words 1 = 8 words	
INT_FrSyn	[1]	Mask LCD frame synchronized interrupt. 0 = The interrupt service is available. 1 = The interrupt service is masked.	1
INT_FiCnt	[0]	Mask LCD FIFO interrupt. 0 = The interrupt service is available. 1 = The interrupt service is masked.	1

Register Setting Guide (STN)

The LCD controller supports multiple screen sizes by special register setting.

The CLKVAL value determines the frequency of VCLK. This value has to be determined such that the VCLK value is greater than data transmission rate. The data transmission rate for the VD port of the LCD controller is used to determine the value of CLKVAL register.

The data transmission rate is given by the following equation:

Data transmission rate = HS x VS x FR x MV

— HS: Horizontal LCD size

— VS: Vertical LCD size

— FR: Frame rate

— MV: Mode dependent value

Table 21-4. MV Value for Each Display Mode

Mode	MV Value
Mono, 4-bit single scan display	1/4
Mono, 8-bit single scan display or 4-bit dual scan display	1/8
4 level gray, 4-bit single scan display	1/4
4 level gray, 8-bit single scan display or 4-bit dual scan display	1/8
16 level gray, 4-bit single scan display	1/4
16 level gray, 8-bit single scan display or 4-bit dual scan display	1/8
Color, 4-bit single scan display	3/4
Color, 8-bit single scan display or 4-bit dual scan display	3/8

The LCDBASEU register value is the first address value of the frame buffer. The lowest 4 bits must be eliminated for burst 4 word access. The LCDBASEL register value depends on LCD size and LCDBASEU. The LCDBASEL value is given by the following equation:

— LCDBASEL = LCDBASEU + LCDBASEL offset

Example 1:

160 x 160, 4-level gray, 80 frame/sec, 4-bit single scan display, HCLK frequency is 60 MHz WLH = 1, WDLY = 1.

Data transmission rate = 160 x 160 x 80 x 1/4 = 512 kHz

CLKVAL = 58, VCLK = 517KHz
HOZVAL = 39, LINEVAL = 159

LINEBLANK =10

LCDBASEL = LCDBASEU + 3200

NOTE:

The higher the system load is, the lower the CPU performance.

Example 2 (Virtual screen register):

4 -level gray, Virtual screen size = 1024 x 1024, LCD size = 320 x 240, LCDBASEU = 0x64, 4-bit dual scan.

1 halfword = 8 pixels (4-level gray),
Virtual screen 1 line = 128 halfword = 1024 pixels,
LCD 1 line = 320 pixels = 40 halfword,
OFFSIZE = 128 - 40 = 88 = 0x58,
PAGEWIDTH = 40 = 0x28

LCDBASEL = LCDBASEU + (PAGEWIDTH + OFFSIZE) x (LINEVAL +1) = 100 + (40 +88) x 120 = 0x3C64

Gray Level Selection Guide

The S3C2443X01 LCD controller can generate 16 gray level using Frame Rate Control (FRC). The FRC characteristics may cause unexpected patterns in gray level. These unwanted erroneous patterns may be shown in fast response LCD or at lower frame rates.

Because the quality of LCD gray levels depends on LCD's own characteristics, the user has to select an appropriate gray level after viewing all gray levels on user's own LCD.

Select the gray level quality through the following procedures:

1. Get the latest dithering pattern register value from SAMSUNG.
2. Display 16 gray bar in LCD.
3. Change the frame rate into an optimal value.
4. Change the VM alternating period to get the best quality.
5. As viewing 16 gray bars, select a good gray level, which is displayed well on your LCD.
6. Use only the good gray levels for quality.

LCD Refresh Bus Bandwidth Calculation Guide

The S3C2443X01 LCD controller can support various LCD display sizes. To select a suitable size (for the flicker free LCD system application), the user have to consider the LCD refresh bus bandwidth determined by the LCD display size, bit per pixel (bpp), frame rate, memory bus width, memory type, and so on.

LCD Data Rate (Byte/s) = bpp x (Horizontal display size) x (Vertical display size) x (Frame rate) /8
LCD DMA Burst Count (Times/s) = LCD Data Rate(Byte/s) /16(Byte) ; LCD DMA using 4words(16Byte) burst

Pdma means LCD DMA access period. In other words, the value of Pdma indicates the period of four-beat burst (4-words burst) for video data fetch. So, Pdma depends on memory type and memory setting.

Eventually, LCD System Load is determined by LCD DMA Burst Count and Pdma.

— LCD System Load = LCD DMA Burst Count x Pdma

Example 3:

640 x 480, 8bpp, 60 frame/sec, 16-bit data bus width, SDRAM (Trp=2HCLK / Trcd=2HCLK / CL=2HCLK) and HCLK frequency is 60 MHz

LCD Data Rate = 8 x 640 x 480 x 60 / 8 = 18.432Mbyte/s
LCD DMA Burst Count = 18.432 / 16 = 1.152M/s
Pdma = (Trp+Trcd+CL+(2 x 4)+1) x (1/60MHz) = 0.250ms
LCD System Load = 1.152 x 250 = 0.288

System Bus Occupation Rate = (0.288/1) x 100 = 28.8%

NOTES

22 TFT LCD

OVERVIEW

The Overlay/Display controller consists of logic for transferring image data from a video buffer located in system memory to an external LCD driver interface. LCD driver interface has two kind of interface. One is conventional RGB-interface and the other is i80-system interface. The display controller supports up to 2 overlay image windows, which support various color format, 16 level alpha blending, color key, x-y position control, soft scrolling, variable window size, and etc.

The display controller supports RGB color format (1bpp to 24bpp).

The display controller can be programmed to support the different requirements on the screen related to the number of horizontal and vertical pixels, data line width for the data interface, interface timing, and refresh rate.

The display controller is used to transfer the video data and to generate the necessary control signals such as, RGB_VSYNC, RGB_HSYNC, RGB_VCLK, RGB_VDEN, and SYS_CS0.... As well as the control signals, display controller has the data ports for video data, which are RGB_VD[23:0], SYS_VD, and VEN_VD as shown in Figure. 22-1.

TOP BLOCK DIAGRAM DISPLAY CONTROLLER

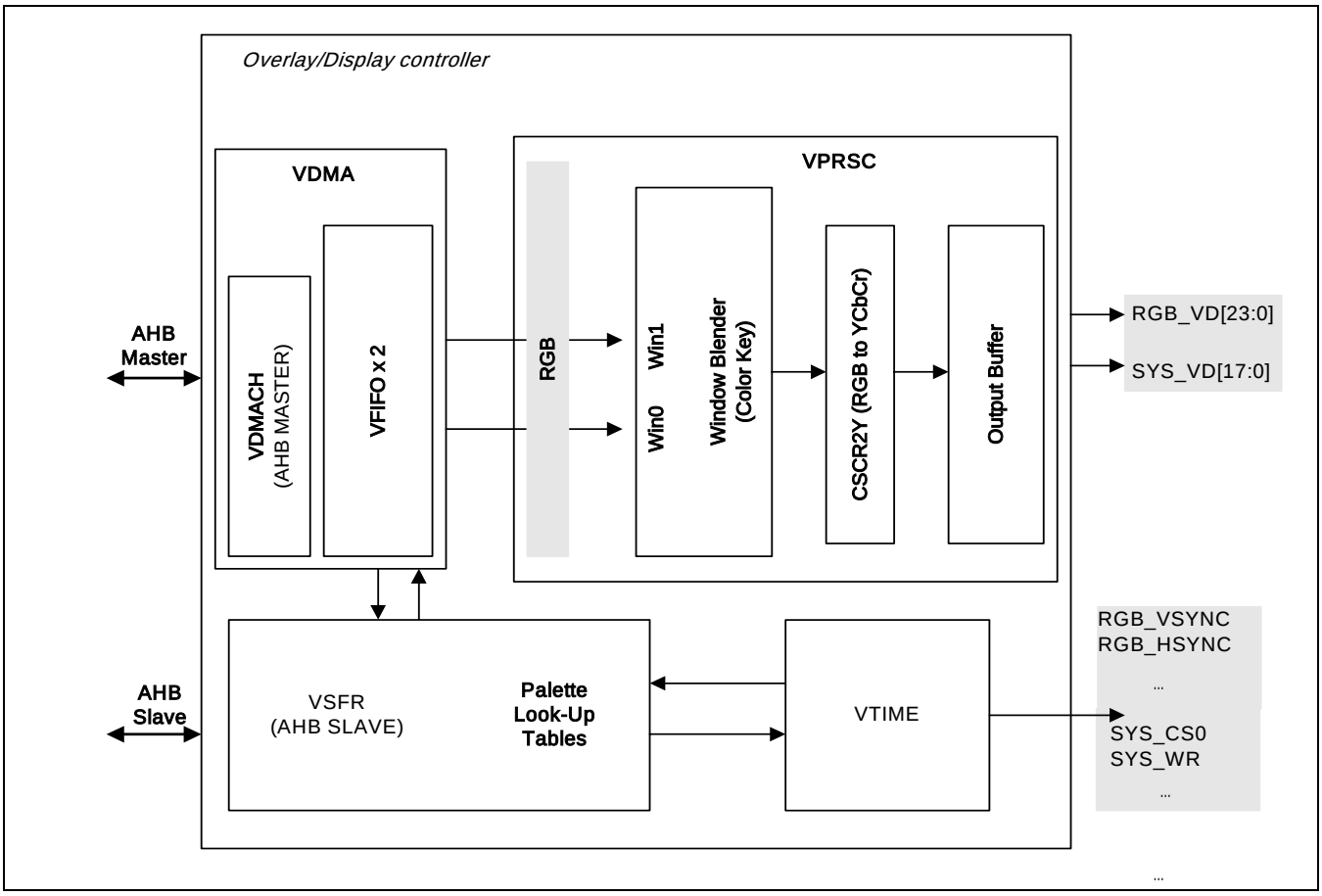


Figure 22-1. Top block diagram Display Controller

FEATURES

The features of the FIMD are:

• Bus Interface	32-bit AMBA AHB Master / AHB Slave
• Video Output Interface	RGB Parallel IF (24-bit) RGB Serial IF (8:8:8) CPU IF (i80-System)
• PIP (OSD) function	Supports 8-bpp (bit per pixel) palettized color Supports 16-bpp non-palettized color Supports unpacked 18-bpp non-palettized color Supports 24-bpp non-palettized color Supports X,Y indexed position Supports 4-bit Alpha blending : Plane / Pixel
• Source format	Window 0 Supports 1, 2, 4 or 8-bpp (bit per pixel) palettized color Supports 16, 18 or 24-bpp non-palettized color Window 1 Supports 1, 2, 4 or 8-bpp (bit per pixel) palettized color Supports 16, 18 or 24-bpp non-palettized color
• Configurable Burst Length	Programable 4 / 8 / 16 Burst DMA
• Palette/Look-up table	256 x 25(ARGB) bits palette (2ea for Window 0, Window1)
• Soft Scrolling	Horizontal : 1 Byte resloution Vertical : 1 pixel resolution
• Virtual Screen	Virtual image can has up to 1Mbyte image size.
• Transparent Overlay	Support Transparent Overlay
• Color Key (Chroma Key)	Support Color key function
• Duble Buffering	Frame buffer alternating by one control bit
• Dithering	Patented 4x4 dither matrix implemetation

FUNCTIONAL DESCRIPTION

BRIEF OF THE SUB-BLOCK

The display controller consists of a VSFR, VDMA, VPRCS, VTIME, and video clock generator. The VSFR has 71 programmable register sets and two-256x25 palette memory, which are used to configure the display controller. The VDMA is a dedicated display DMA, which it can transfer the video data in frame memory to VPRCS. By using this special DMA, the video data can be displayed on the screen without CPU intervention. The VPRCS receives the video data from VDMA and sends the video data through the data ports (RGB_VD, VEN_VD, or SYS_VD) to the display device (LCD) after changing them into a suitable data format, for example 8-bit per pixel mode (8 BPP Mode) or 16-bit per pixel mode (16 BPP Mode). The VTIME consists of programmable logic to support the variable requirement of interface timing and rates commonly found in different LCD drivers. The VTIME block generates RGB_VSYNC, RGB_HSYNC, RGB_VCLK, RGB_VDEN, SYS_CS1, SYS_CS0, and so on.

DATA FLOW

FIFO is present in the VDMA. When FIFO is empty or partially empty, VDMA requests data fetching from the frame memory based on the burst memory transfer mode(Consecutive memory fetching of 4 / 8 / 16 words per one burst request without allowing the bus mastership to another bus master during the bus transfer). When this kind of transfer request is accepted by bus arbitrator in the memory controller, there will be 4 /8 /16 successive word data transfers from system memory to internal FIFO. The each size of FIFO is 32, 16, or 8 words. The size of FIFO is determined by the data transfer rate, respectively. The display controller has seven FIFOs because it needs to support the overlay window display mode. In case of one screen display mode, the only one FIFO should be used. The data through FIFO is fetched by VPRCS which has a blending, scheduling function for the final image data. VPRCS supports overlay function which enables to overlay any image up to 2 window images whose is smaller or same size can be blended with main window image with programmable alpha blending or color (chroma) key function. Fig. 22-2 shows the data flow from system bus to the output buffer. VDMA has 2 DMA channels. Alpha values written in SFR determine the level of blending. Data from Output buffer will be appearing to the Video Data Port.

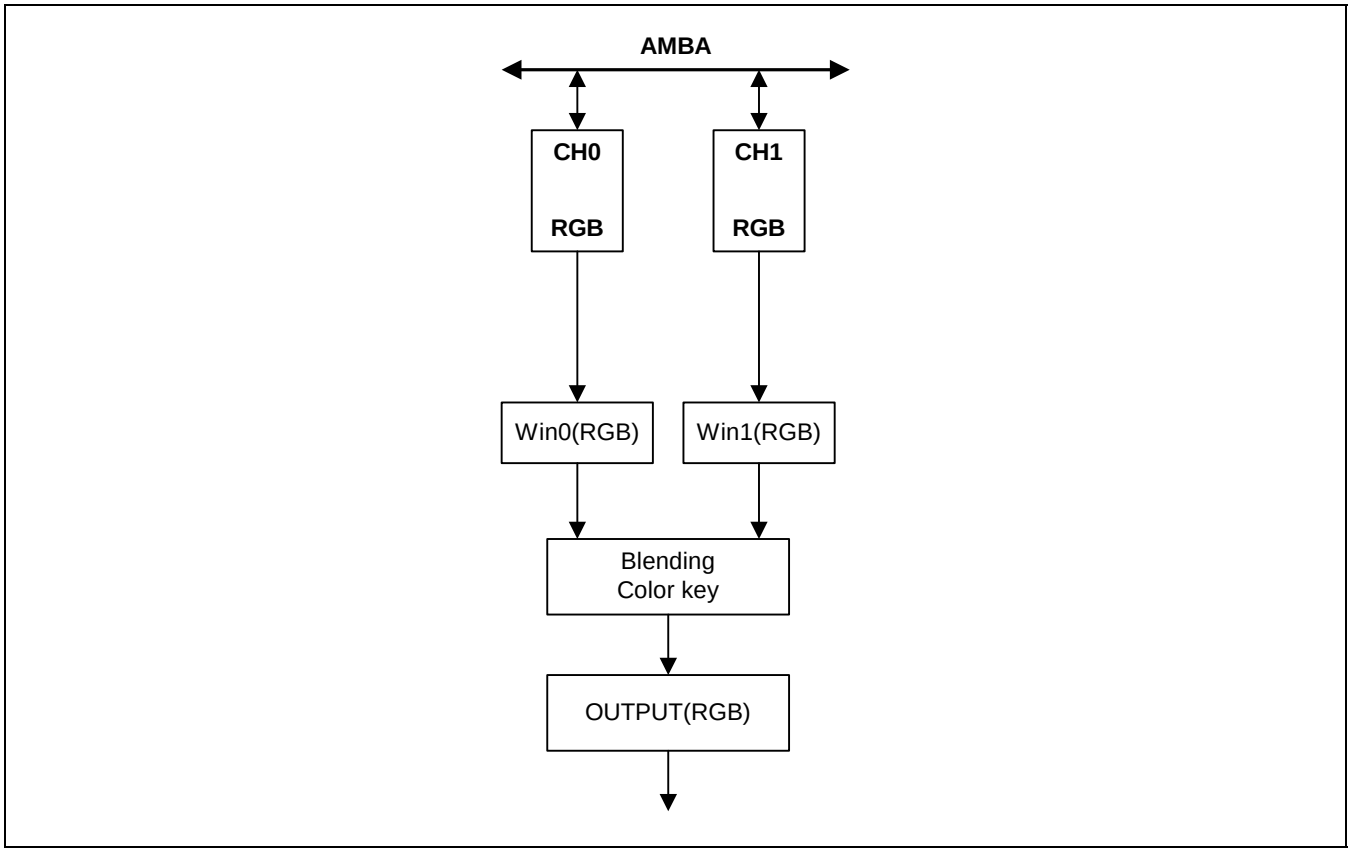


Figure 22-2. Block diagram of the Data Flow

Interface

Display controller supports 2 types of display device. One type is the conventional RGB-interface which uses RGB data, Vertical/horizontal sync, data valid signal and data sync clock. The Second type is i80-system interface which uses address, data, chip select, read/write control and register/status indicating signal. In this type of LCD driver it has a frame buffer and has the function of self-refresh, so display controller updates one still image by writing only one time to the LCD.

OVERVIEW OF THE COLOR DATA

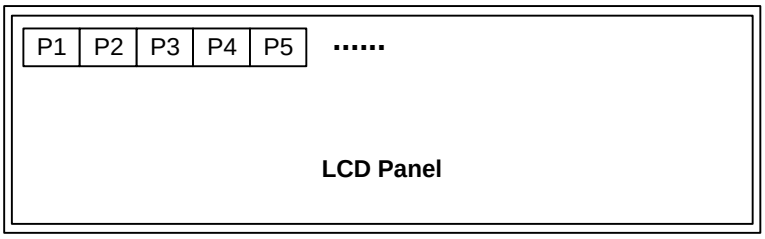
RGB Data format

The display controller requests the specified memory format of frame buffer. The next table shows some examples of each display mode.

25BPP display (A888)

(BSWP = 0, HWSWP = 0)

	D[31:25]	D[24]	D[23:0]
000H	Dummy Bit	AEN	P1
004H	Dummy Bit	AEN	P2
008H	Dummy Bit	AEN	P3
...			



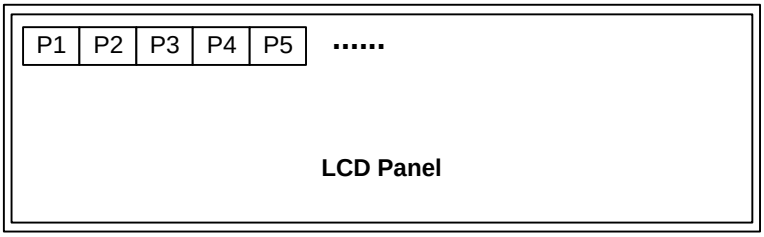
NOTES:

1. AEN : Transparency enable/disable control bit
   AEN = 0 : Alpha0 value is applied.
   AEN = 1 : Alpha1 value is applied.
   If transparency is enabled, then this pixel would be blended with lower window layer.
   Alpha value is selected by sfr value as ALPHA_R, ALPHA_G, ALPHAB, PIX_BEND and ALPHAPAL. Detail is in the description of SFR.
2. D[23:16] = Red data, D[15:8] = Green data, D[7:0] = Blue data

24BPP display (A887)

(BSWP = 0, HWSWP = 0)

	D[31:24]	D[23]	D[22:0]
000H	Dummy Bit	AEN	P1
004H	Dummy Bit	AEN	P2
008H	Dummy Bit	AEN	P3
...			



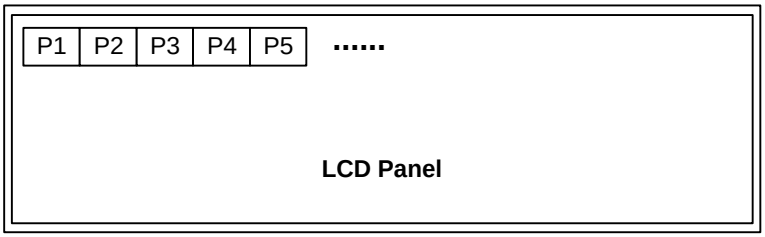
NOTES:

1. AEN : Transparency enable/disable control bit
   AEN = 0 : Alpha0 value is applied.
   AEN = 1 : Alpha1 value is applied.
   If transparency is enabled, then this pixel would be blended with lower window layer.
   Alpha value is selected by sfr value as ALPHA0_R, ALPHA0_G, ALPHA0_B, ALPHA1_R, ALPHA1_G, ALPHA1_B .
   Detail is in the description of SFR.
2. D[22:15] = Red data, D[14:7] = Green data, D[6:0] = Blue data

24BPP display (888)

(BSWP = 0, HWSWP = 0)

	D[31:24]	D[23:0]
000H	Dummy Bit	P1
004H	Dummy Bit	P2
008H	Dummy Bit	P3
...		

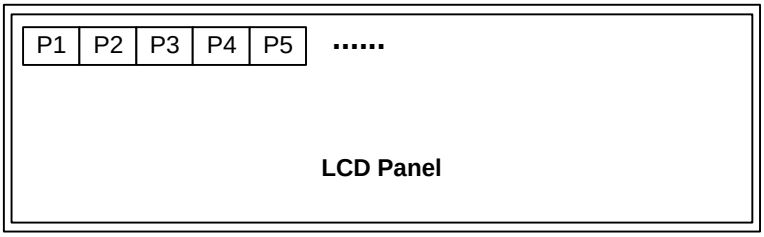


NOTE: D[23:16] = Red data, D[15:8] = Green data, D[7:0] = Blue data

19BPP display (A666)

(BSWP = 0, HWSWP = 0)

	D[31:19]	D[18]	D[17:0]
000H	Dummy Bit	AEN	P1
004H	Dummy Bit	AEN	P2
008H	Dummy Bit	AEN	P3
...			



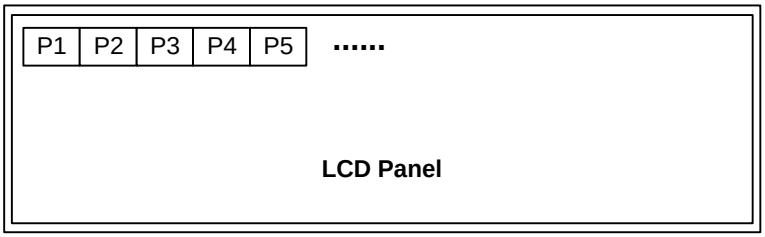
NOTES:

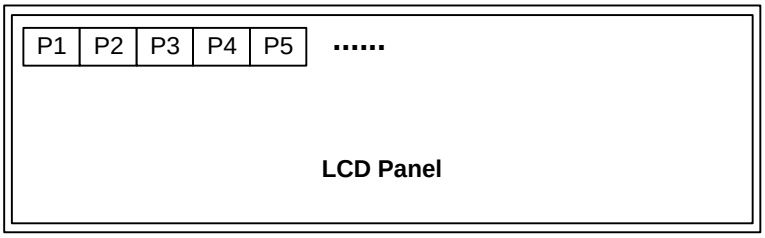
1. AEN : Transparency enable/disable control bit
   AEN = 0 : Alpha0 value is applied.
   AEN = 1 : Alpha1 value is applied.
   If transparency is enabled, then this pixel would be blended with lower window layer.
   Alpha value is selected by sfr value as ALPHA0_R, ALPHA0_G, ALPHA0_B, ALPHA1_R, ALPHA1_G, ALPHA1_B .
   Detail is in the description of SFR.
2. D[17:12] = Red data, D[11:6] = Green data, D[5:0] = Blue data

18BPP display (666)

(BSWP = 0, HWSWP = 0)

	D[31:18]	D[17:0]
000H	Dummy Bit	P1
004H	Dummy Bit	P2
008H	Dummy Bit	P3
...		





NOTE: D[17:12] = Red data, D[11:6] = Green data, D[5:0] = Blue data

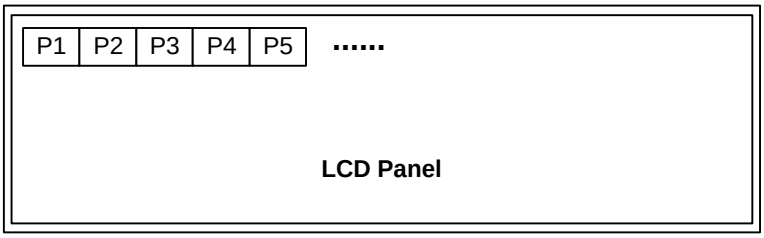
16BPP display (A555)

(BSWP = 0, HWSWP = 0)

	D[31]	D[30:16]	D[15]	D[14:0]
000H	AEN1	P1	AEN2	P2
004H	AEN3	P3	AEN4	P4
008H	AEN5	P5	AEN6	P6
...				

(BSWP = 0, HWSWP = 1)

	[31]	D[30:16]	D[15]	D[14:0]
000H	AEN2	P2	AEN1	P1
004H	AEN4	P4	AEN3	P3
008H	AEN6	P6	AEN5	P5
...				



NOTES:

1. AEN : Transparency enable/disable control bit
   AEN = 0 : Alpha0 value is applied.
   AEN = 1 : Alpha1 value is applied.
   If transparency is enabled, then this pixel would be blended with lower window layer.
   Alpha value is selected by sfr value as ALPHA0_R, ALPHA0_G, ALPHA0_B, ALPHA1_R, ALPHA1_G, ALPHA1_B .
   Detail is in the description of SFR.
2. D[14:10] = Red data, D[9:5] = Green data, D[4:0] = Blue data

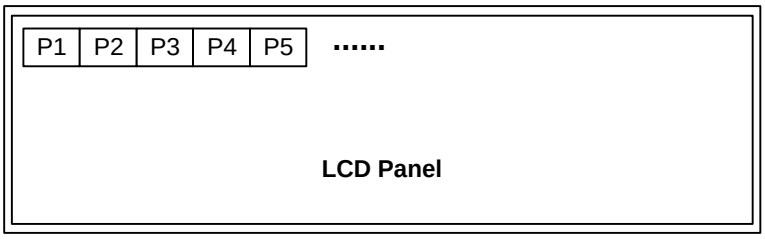
16BPP display (1555)

(BSWP = 0, HWSWP = 0)

	D[31:16]	D[15:0]
000H	P1	P2
004H	P3	P4
008H	P5	P6
...		

(BSWP = 0, HWSWP = 1)

	D[31:16]	D[15:0]
000H	P2	P1
004H	P4	P3
008H	P6	P5
...		



NOTE: 1. = {D[14:10], D[15] } = Red data, {D[9:5], D[15] } = Green data, {D[4:0], D[15]}= Blue data

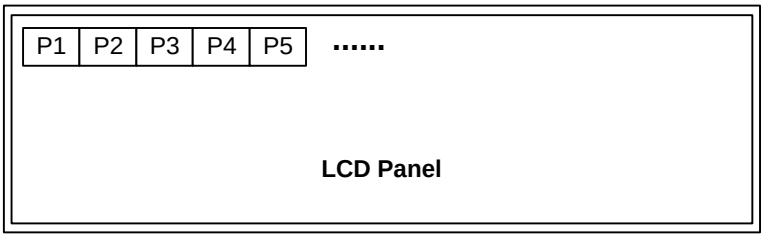
16BPP *display* (565)

(BSWP = 0, HWSWP = 0)

	D[31:16]	D[15:0]
000H	P1	P2
004H	P3	P4
008H	P5	P6
...		

(BSWP = 0, HWSWP = 1)

	D[31:16]	D[15:0]
000H	P2	P1
004H	P4	P3
008H	P6	P5
...		



NOTE: D[15:11] = Red data, D[10:5] = Green data, D[4:0] = Blue data

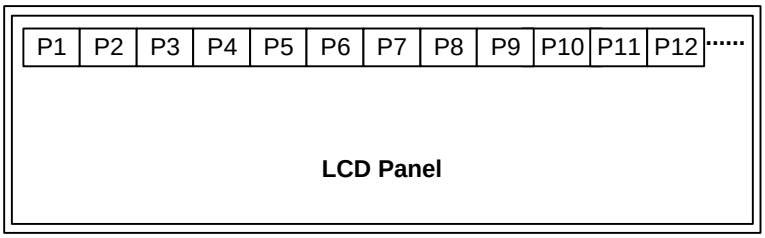
8BPP display(*A232*)

(BSWP = 0, HWSWP = 0)

	D[31]	D[30:24]	D[23]	D[22:16]	D[15]	D[14:8]	D[7]	D[6:0]
000H	AEN1	P1	AEN2	P2	AEN3	P3	AEN4	P4
004H	AEN5	P5	AEN6	P6	AEN7	P7	AEN8	P8
008H	AEN9	P9	AEN10	P10	AEN11	P11	AEN12	P12
...								

(BSWP = 1, HWSWP = 0)

	D[31]	D[30:24]	D[23]	D[22:16]	D[15]	D[14:8]	D[7]	D[6:0]
000H	AEN4	P4	AEN3	P3	AEN2	P2	AEN1	P1
004H	AEN8	P8	AEN7	P7	AEN6	P6	AEN5	P5
008H	AEN12	P12	AEN11	P11	AEN10	P10	AEN9	P9
...								



NOTES:

1. AEN : Transparency enable/disable control bit
   AEN = 0 : Alpha0 value is applied.
   AEN = 1 : Alpha1 value is applied.
   If transparency is enabled, then this pixel would be blended with lower window layer.
   Alpha value is selected by sfr value as ALPHA0_R, ALPHA0_G, ALPHA0_B, ALPHA1_R, ALPHA1_G, ALPHA1_B .
   Detail is in the description of SFR.
2. D[6:5] = Red data, D[4:2] = Green data, D[1:0] = Blue data

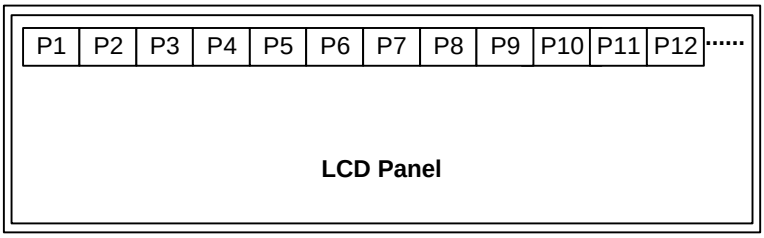
8BPP display(*Palette*)

(BSWP = 0, HWSWP = 0)

	D[31:24]	D[23:16]	D[15:8]	D[7:0]
000H	P1	P2	P3	P4
004H	P5	P6	P7	P8
008H	P9	P10	P11	P12
...				

(BSWP = 1, HWSWP = 0)

	D[31:24]	D[23:16]	D[15:8]	D[7:0]
000H	P4	P3	P2	P1
004H	P8	P7	P6	P5
008H	P12	P11	P10	P9
...				



NOTE: If ALPHAPAL is enabled, then the MSB of Palette memory is acting as a AEN bit.
AEN = 0 : Alpha0 value is applied.
AEN = 1 : Alpha1 value is applied.
If transparency is enabled, then this pixel would be blended with lower window layer.
Alpha value is selected by sfr value as ALPHA0_R, ALPHA0_G, ALPHA0_B, ALPHA1_R, ALPHA1_G, ALPHA1_B .
Detail is in the description of SFR.

4BPP display(Palette)

(BSWP = 0, HWSWP = 0)

	D[31:28]	D[27:24]	D[23:20]	D[19:16]	D[15:12]	D[11:8]	D[7:4]	D[3:0]
000H	P1	P2	P3	P4	P5	P6	P7	P8
004H	P9	P10	P11	P12	P13	P14	P15	P16
008H	P17	P18	P19	P20	P21	P22	P23	P24
...								

(BSWP = 1, HWSWP = 0)

	D[31:28]	D[27:24]	D[23:20]	D[19:16]	D[15:12]	D[11:8]	D[7:4]	D[3:0]
000H	P7	P8	P5	P6	P3	P4	P1	P2
004H	P15	P16	P13	P14	P11	P12	P9	P10
008H	P23	P24	P21	P22	P19	P20	P17	P18
...								

NOTE: If ALPHAPAL is enabled, then the MSB of Palette memory is acting as a AEN bit.
AEN = 0 : Alpha0 value is applied.
AEN = 1 : Alpha1 value is applied.
If transparency is enabled, then this pixel would be blended with lower window layer.
Alpha value is selected by sfr value as ALPHA0_R, ALPHA0_G, ALPHA0_B, ALPHA1_R, ALPHA1_G, ALPHA1_B .
Detail is in the description of SFR.

2BPP display(Palette)

(BSWP = 0, HWSWP = 0)

D	[31:30]	[29:28]	[27:26]	[25:24]	[23:22]	[21:20]	[19:18]	[17:16]
000H	P1	P2	P3	P4	P5	P6	P7	P8
004H	P17	P18	P19	P20	P21	P22	P23	P24
008H	P33	P34	P35	P36	P37	P38	P39	P40
...								

D	[15:14]	[13:12]	[11:10]	[9:8]	[7:6]	[5:4]	[3:2]	[1:0]
000H	P9	P10	P11	P12	P13	P14	P15	P16
004H	P25	P26	P27	P28	P29	P30	P31	P32
008H	P41	P42	P43	P44	P45	P46	P47	P48
...								

NOTE: If ALPHAPAL is enabled, then the MSB of Palette memory is acting as a AEN bit.
AEN = 0 : Alpha0 value is applied.
AEN = 1 : Alpha1 value is applied.
If transparency is enabled, then this pixel would be blended with lower window layer.
Alpha value is selected by sfr value as ALPHA0_R, ALPHA0_G, ALPHA0_B, ALPHA1_R, ALPHA1_G, ALPHA1_B .
Detail is in the description of SFR.

VD SIGNAL CONNECTION

VD Pin Descriptions at 24BPP RGB parallel

VD	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RED	7	6	5	4	3	2	1	0																
GREEN									7	6	5	4	3	2	1	0								
BLUE																	7	6	5	4	3	2	1	0

VD Pin Descriptions at 18BPP RGB parallel

VD	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RED	5	4	3	2	1	0																		
GREEN							NC		5	4	3	2	1	0	NC								NC	
BLUE																	5	4	3	2	1	0		

VD Pin Descriptions at 16BPP RGB parallel

(5:6:5)

VD	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RED	4	3	2	1	0																			
GREEN						NC			4	3	2	1	0	NC								NC		
BLUE																	4	3	2	1	0			

VD Pin Descriptions at 24BPP RGB Serial(8+8+8)

VD	23	22	21	20	19	18	17	16	[15:0]
1st time	7	6	5	4	3	2	1	0	NC
2nd time	7	6	5	4	3	2	1	0	
3rd time	7	6	5	4	3	2	1	0	

VD Pin Descriptions at 18BPP RGB Serial(6+6+6)

VD	23	22	21	20	19	18	[17:0]
1st time	5	4	3	2	1	0	NC
2nd time	5	4	3	2	1	0	
3rd time	5	4	3	2	1	0	

VD Pin Descriptions at 18BPP CPU Interface

VD	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RED	NC						5	4	3	2	1	0												
GREEN													5	4	3	2	1	0						
BLUE																			5	4	3	2	1	0

VD Pin Descriptions at 16BPP CPU Interface

VD	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RED	NC						4	3	2	1	0												NC	
GREEN												5	4	3	2	1	0							
BLUE																		4	3	2	1	0		

PALETTE USAGE

Palette Configuration and Format Control

The display controller can support the 256 colors palette for various selection of color mapping.

The user can select 256 colors from the 25-bit colors through these four formats.
256 colors palette consist of the 256(depth) × 25-bit DPSRAM. Palette supports 8:8:8, 6:6:6, 5:6:5(R:G:B), and etc format.
For example of A:5:5:5 format, write palette like Table 3 and then connect VD pin to TFT LCD panel(R(5)=VD[23:19], G(5)=VD[15:11], and B(5)=VD[7:3]). The AEN bit control the blending function enable or disable. At the last, Set WPALCON(**W0PAL, case window0)** register to 0'b101.

Table 22-1. 25(A:8:8:8) Palette Data Format

INDEX\ Bit Pos.	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00H	AEN	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
01H	AEN	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
.....	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…
FFH	AEN	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Number of VD	-	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 22-2. 19BPP (A:6:6:6) Palette Data Format

INDEX\Bit Pos.	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00H		-	-	-	-	-	AEN	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
01H		-	-	-	-	-	AEN	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
.....		-	-	-	-	-	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…
FFH		-	-	-	-	-	AEN	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Number of VD		-	-	-	-	-	-	23	22	21	20	19	18	15	14	13	12	15	14	7	6	5	4	3	2

Table 22-3. 16BPP(A:5:5:5) Palette Data Format

INDEX\Bit Pos.	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00H		-	-	-	-	-	-	-	-	AEN	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
01H		-	-	-	-	-	-	-	-	AEN	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
.....		-	-	-	-	-	-	-	-	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…
FFH		-	-	-	-	-	-	-	-	AEN	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
Number of VD		-	-	-	-	-	-	-	-	-	23	22	21	20	19	15	14	13	12	11	7	6	5	4	3

PALETTE READ/WRITE

It is prohibited to access Palette memory during the ACTIVE status of the VSTATUS (vertical status) register. When the user goes to do Read/Write operation on the palette, VSTATUS register must be checked.

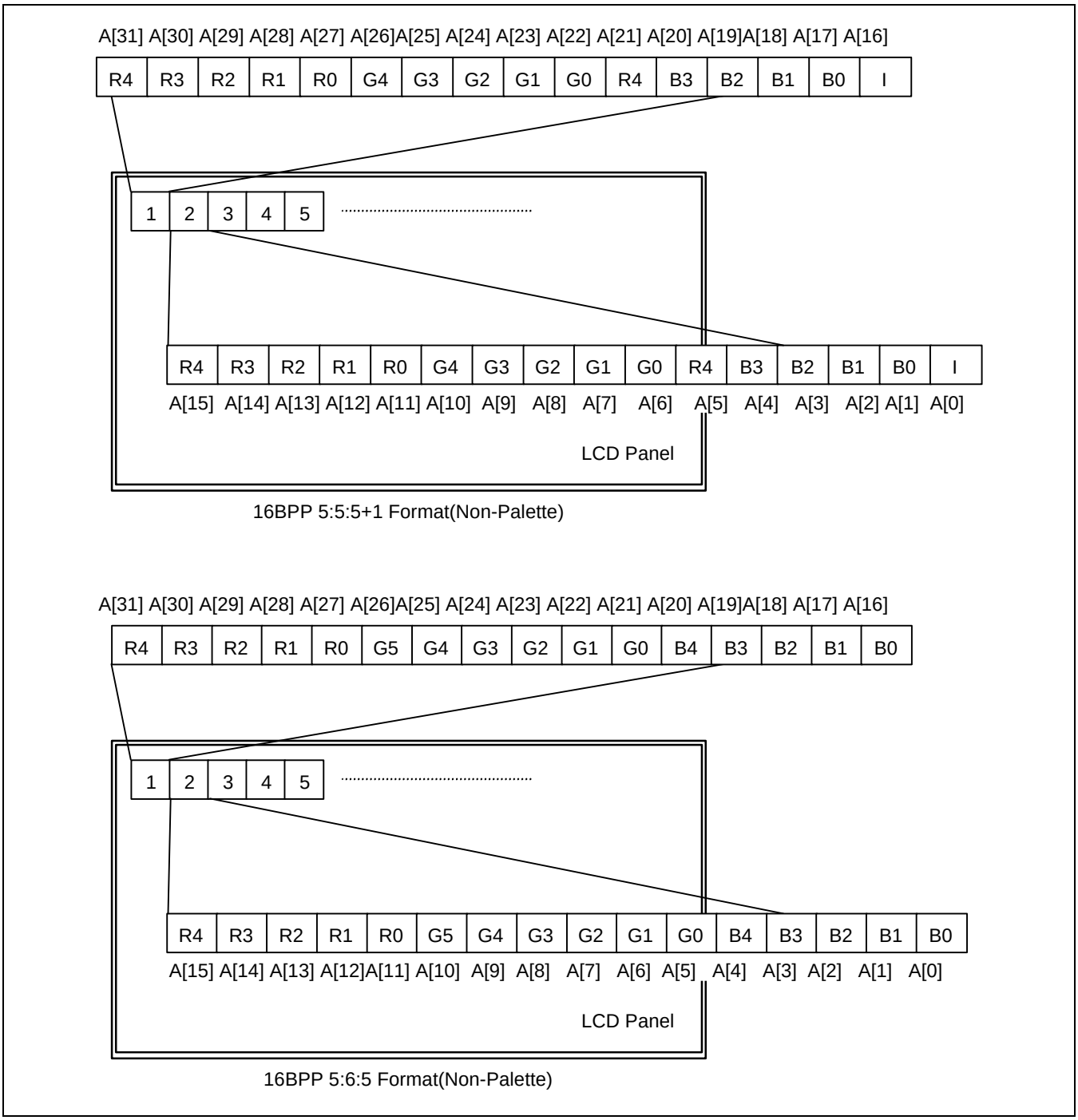


Figure 22-3. 16BPP(5:6:5) Display Types

WINDOW BLENDING

OVERVIEW

The main function of the VPRCS module is window blending function. Display controller has 2 window layer and the detail is described below. As a example of application, System can use win0 as a OS window, full TV screen window or etc. But, this feature enhances the system performance by reducing the data rate of total system.

Total 2 window

- win 0 (base) : RGB with palette
- win 1 (Overlay1) : RGB with palette

Overlay Priority

Win 1 > Win 0

Color Key

:The register value to ColorKey reg must be set by 24bit RGB format.

Blending equation

WinOut(R) = Win0(R) x (1-AR1) + Win1(R) x AR1

WinOut(G) = Win0(G) x (1-AG1) + Win1(G) x AR1

WinOu (B) = Win0(B) x (1-AB1) + Win1(B) x AR1

Where,

AR1 = Window 1's Red blending factor

AG1 = Window 1's Green blending factor

AB1 = Window 1's Blue blending factor

Blending Diagram/Details

Display controller could blend 5 Layer for the only one pixel at the same time. The Blending factor, alpha value is controlled by ALPHA0_R,ALPHA0_G,ALPHA0_B, ALPHA1_R,ALPHA1_G,ALPHA1_B register, which are implemented for each window layer and color(R,G,B). The illustration below is described as the example of the R (Red) output using ALPHA_R value of each windows.As a special feature, all window has two kinds of alpha blending value. One is alpha value for transparnacy enable (AEN value ==1), the other is alpha value for transparnacy disable(AEN value == 0). **If ENWIN_F is enabled and BLD_PIX is enabled** then AR will be choosen by the below equation.

AR = (Pixel(R)'s AEN value == 1'b1) ? Reg(ALPHA1_R) : Reg(ALPHA0_R);

AG = (Pixel(G)'s AEN value == 1'b1) ? Reg(ALPHA1_G) : Reg(ALPHA0_G);

AB = (Pixel(B)'s AEN value == 1'b1) ? Reg(ALPHA1_B) : Reg(ALPHA0_B);

(where, BLD_ PIX == 1)

If ENWIN_F is enabled and BLD_PIX is disabled then AR will be ALPHA0_R only. In this case blending facto AR is fixed by ALPHA0_R, not using the AEN bit information anymore.

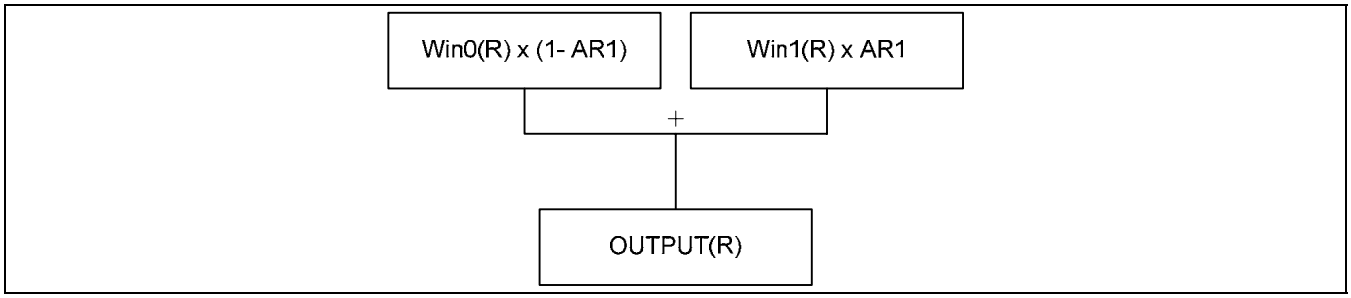


Figure 22-4. Blending Diagram

COLOR-KEY Function

The display controller can support color-key function for the various effect of image mapping. Color image of OSD layer, which is specified by COLOR-KEY register, will be substituted by back-ground image for special functionality, as cursor image or pre-view image of the camera.

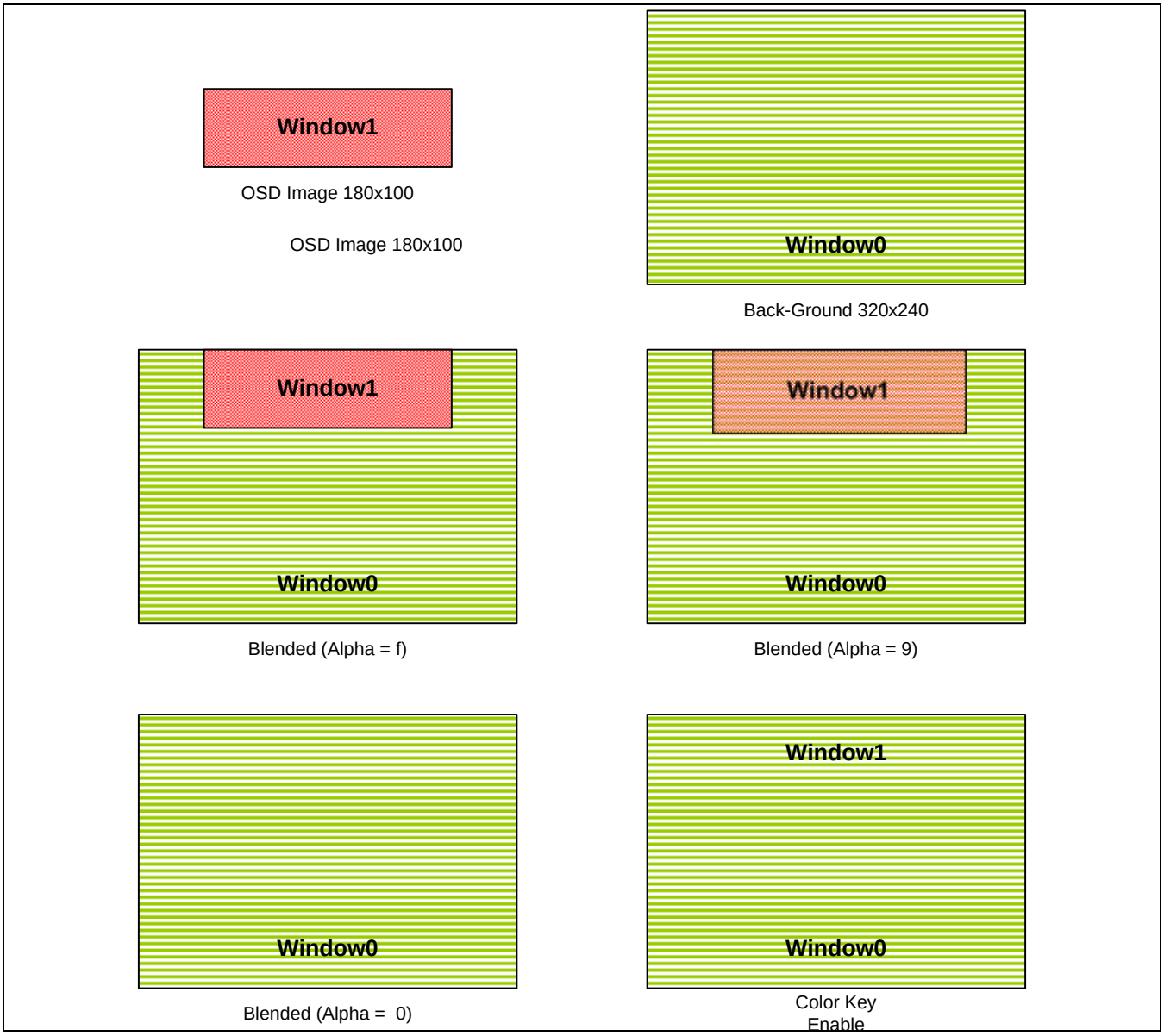


Figure 22-5. Color-key function configurations

VTIME CONTROLLER OPERATION

RGB INTERFACE CASE

The VTIME generates the control signals such as, RGB_VSYNC, RGB_HSYNC, RGB_VDEN and RGB_VCLK signal for RGB interface. These control signals are highly related with the configuration on the VIDTCON0/1/2 registers in the VSFR register. Base on these programmable configurations of the display control registers in VSFR, the VTIME module can generate the programmable control signals suitable for the support of many different types of display device.

The RGB_VSYNC signal is asserted to cause the LCD's line pointer to start over at the top of the display. The RGB_VSYNC and RGB_HSYNC pulse generation is controlled by the configuration of both the HOZVAL field and the LINEVAL registers. The HOZVAL and LINEVAL can be determined by the size of the LCD panel according to the following equations:

HOZVAL = (Horizontal display size) -1

LINEVAL = (Vertical display size) –1

The rate of RGB_VCLK signal can be controlled by the CLKVAL field in the VIDCON0 register. The table below defines the relationship of RGB_VCLK and CLKVAL. The minimum value of CLKVAL is 1.

RGB_VCLK (Hz) =HCLK/ [CLKVAL+1]

Table 22-4. Relation between VCLK and CLKVAL (TFT, Freq. of Video Clock Source=60MHz)

CLKVAL	60MHz/X	VCLK
1	60 MHz/2	30.0 MHz
2	60 MHz/3	15.0 MHz
:	:	:
63	60 MHz/64	938 kHz

The RGB_HSYNC and RGB_VSYNC signal is configured by VSYNC, VBPD, VFPD, HSYNC, HBPD, HFPD, HOZVAL and LINEVAL. Refer the Figure 22-8.

The frame rate is RGB_VSYNC signal frequency. The frame rate is related with the field of VSYNC, VBPD, VFPD, LINEVAL, HSYNC, HBPD, HFPD, HOZVAL, CLKVAL registers. Most LCD driver needs their own adequate frame rate. The frame rate is calculated as follows;

Frame Rate = 1/ [{ (VSPW+1) + (VBPD+1) + (LIINEVAL + 1) + (VFPD+1) } x {(HSPW+1) + (HBPD +1) + (HFPD+1) + (HOZVAL + 1) } x { (CLKVAL+1) / (Frequency of Clock source) }]

i80 System Interface

The VTIME generates the control signals such as, SYS_CS0, SYS_CS1, SYS_RS and SYS_WE signal for i80 System Interface. These signals are controlled by the LCDIFMODE, LCD_CS_SETUP, LCD_WAIT_WR and LCD_HOLD_WR registers. Refer figure 22-8.

VIRTUAL DISPLAY

The display controller supports the hardware horizontal or vertical scrolling. If the screen is scrolled, the fields of LCDBASEU and LCDBASEL registers need to be changed (refer to Figure 22-6) but not the values of PAGEWIDTH and OFFSIZE. The size of video buffer in which the image is stored should be larger than the LCD panel screen size.

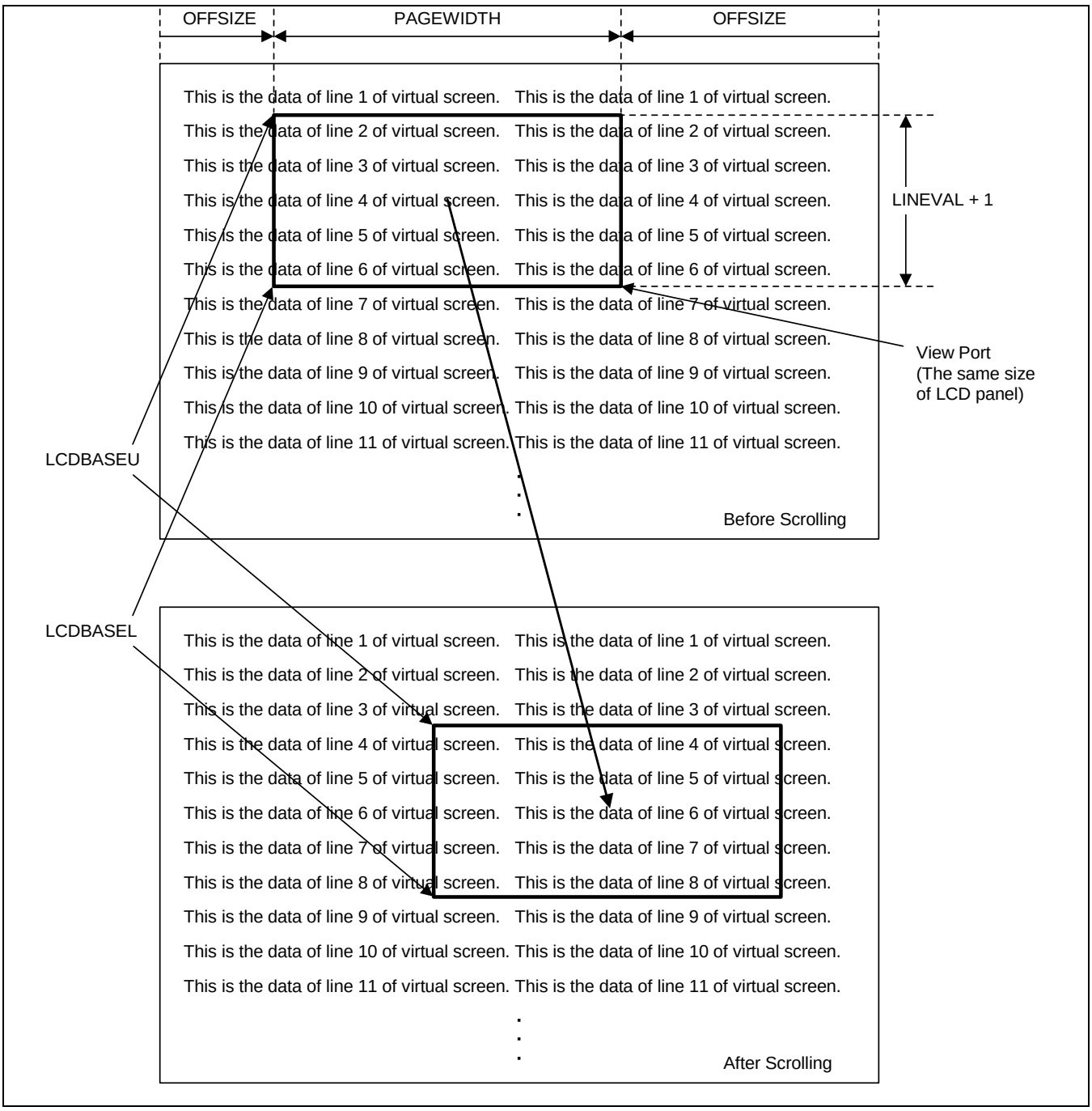


Figure 22-6. Example of Scrolling in Virtual Display

RGB INTERFACE SPEC

Signals

Name	Type	Source/Destination	Description
RGB_HSYNC	Output	Pad	Horizontal Sync. Signal
RGB_VSYNC	Output	Pad	Vertical Sync. Signal
RGB_VCLK	Output	Pad	LCD Video Clock
RGB_VDEN	Output	Pad	Data Enable
RGB_VD[23:0]	Output	Pad	RGB data output

Timing

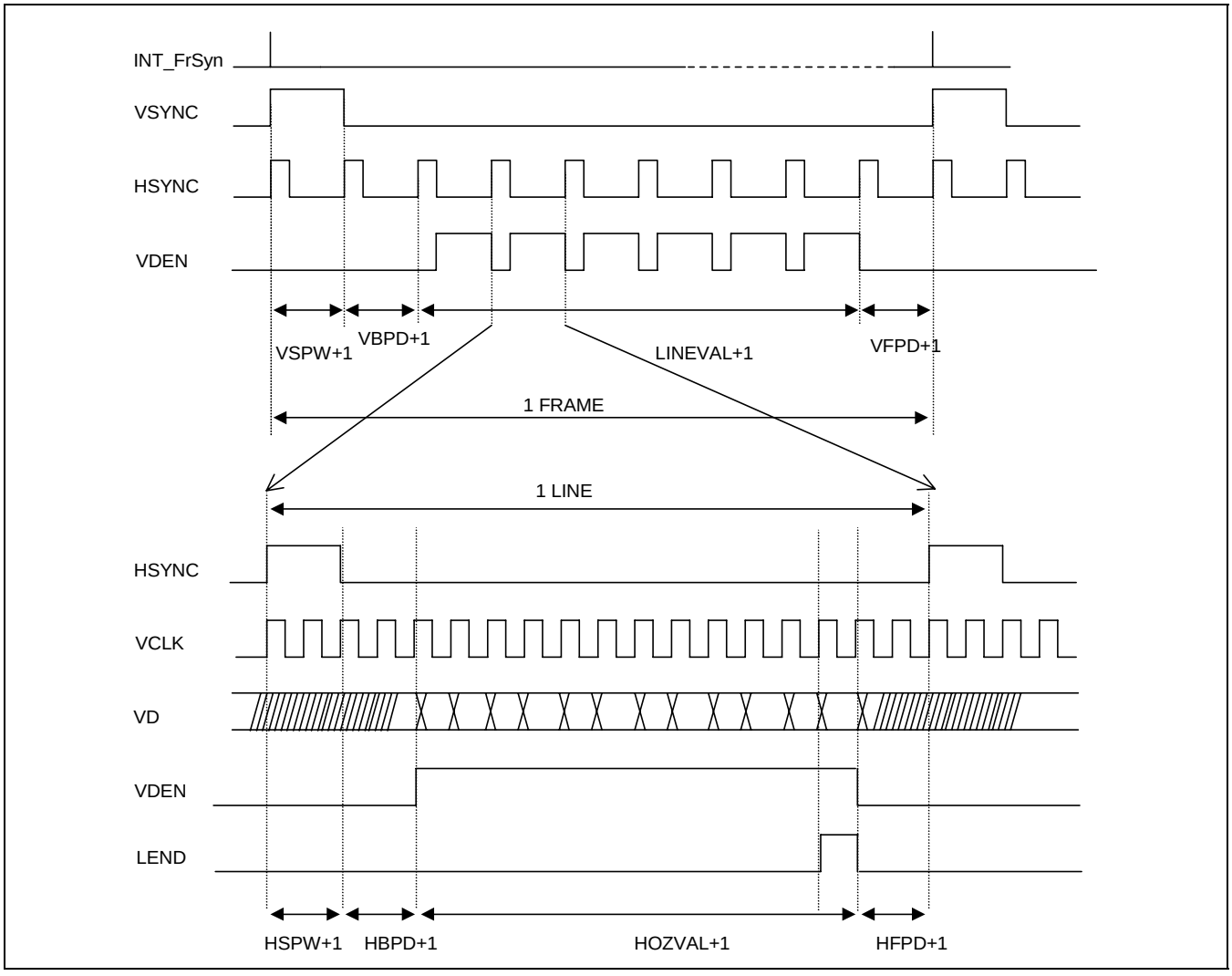


Figure 22-7. LCD RGB interface Timing

LCD CPU INTERFACE (I80-SYSTEM I/F)

Signals

Name	Type	Source/Destination	Description
SYS_VD[17:0]	InOut	Video Mux	Video Data
SYS_CS0	Output	Video Mux	Chip select for Main LCD
SYS_CS1	Output	Video Mux	Chip select for Sub LCD
SYS_WR	Output	Video Mux	Write enable
SYS_OE	Output	Video Mux	Output enable
SYS_RS	Output	Video Mux	Register/State select

Timing

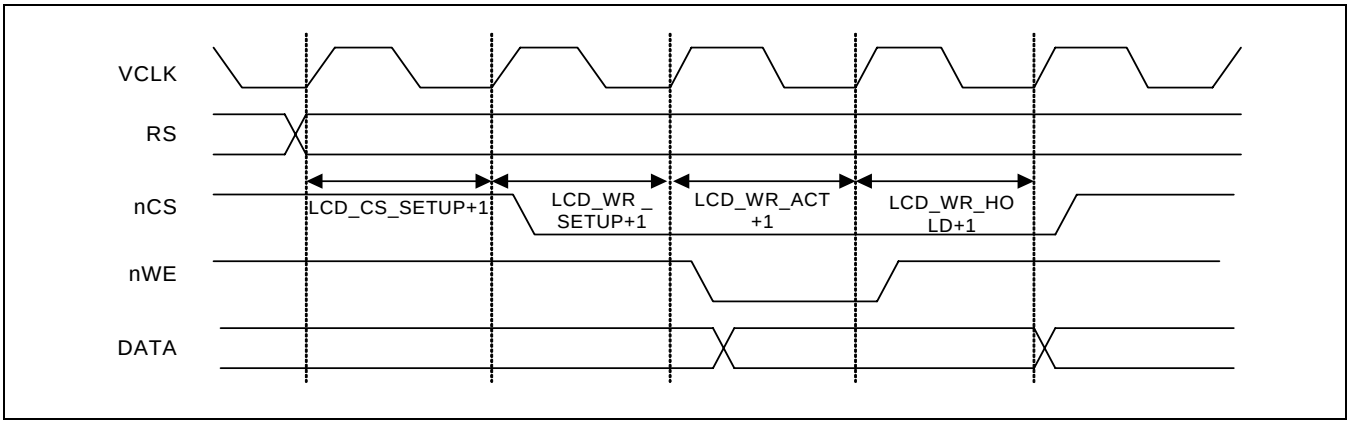


Figure 22-8. WRITE Cycle Timing

SIGNALS

Table 22-5. LCD RGB I/F signals

Name	Type	Source/Destination	Description
RGB_HSYNC	Output	Pad	Horizontal Sync. Signal
RGB_VSYNC	Output	Pad	Vertical Sync. Signal
RGB_VCLK	Output	Pad	LCD Video Clock
RGB_VDEN	Output	Pad	Data Enable
RGB_VD[23:0]	Output	Pad	RGB data output

Table 22-6. CPU I/F (i80-System Interface)

Name	Type	Source/Destination	Description
VDSYS[17:0]	InOut	Video Mux	CPU I/F Data
SYS_CS0	Output	Video Mux	CPU I/F Chip select 0
SYS_CS1	Output	Video Mux	CPU I/F Chip select 1
SYS_WR	Output	Video Mux	CPU I/F Chip Write Enable
SYS_OE	Output	Video Mux	CPU I/F Chip Output Enable
SYS_RS	Output	Video Mux	CPU I/F Chip RS(Register/Status) control

PAD MUXING

Table 22-7. LCDCNTL (STN) / DISPCON (TFT) Port Muxing Table

PAD	VIDSEL	VIDOUT	Signals
LPC_VF	0	XX	LPC_RVSB / LPC_RVS / LPC_OE
	1	10	
		01	
		00	
VCLK	0	XX	LCD_VCLK
	1	10	SYS_WE
		01	Reserved
		00	RGB_VCLK
VLINE	0	XX	LCD_VLINE
	1	10	SYS_CS0
		01	Reserved
		00	RGB_HSYNC
VFRAM	0	XX	LCD_VFRAME
	1	10	SYS_CS1
		01	Reserved
		00	RGB_VSYNC
VM	0	XX	LCD_VM
	1	10	SYS_RS
		01	Reserved
		00	RGB_VDEN
LEND	0	XX	LCD_LEND
	1	10	SYS_OE
		01	
		00	
VD	0	XX	LCD_VD
	1	10	VDSYS
		01	Reserved
		00	RGB_VD

- VIDSEL register is defined in GPIO region
- VIDOUT registers are defined in VIDCON0[23:22] in DISPCON region

PROGRAMMER'S MODEL

OVERVIEW

The following registers are used to configure display controller

1. VIDCON0: configure Video output format and display enable/disable.
2. VIDCON1: RGB I/F control signal.
3. SYSIFCONx: CPU I/F control signal.
4. VIDTCONx: configure Video output Timing and determine the size of display.
5. WINCONx: each window format setting
6. VIDOSDxA, VIDOSDxB: Window position setting
7. VIDOSDxC: alpha value setting
8. VIDWxxADDx: source image address setting
9. WxKEYCONx: Color key value register
10. WINxMAP: window color control
11. WPALCON: palette control register
12. WxPDATAxx: Window Palette Data of the each Index.

Register Descriptions

Base Address: 0x4C800000

Register	Address	R/W	Description	Reset Value
VIDCON0	0x4C800000	R/W	Video control 0 register	0x0000_0000
VIDCON1	0x4C800004	R/W	Video control 1 register	0x0000_0000
VIDTCON0	0x4C800008	R/W	Video time control 0 register	0x0000_0000
VIDTCON1	0x4C80000C	R/W	Video time control 1 register	0x0000_0000
VIDTCON2	0x4C800010	R/W	Video time control 2 register	0x0000_0000
WINCON0	0x4C800014	R/W	Window control 0 register	0x0000_0000
WINCON1	0x4C800018	R/W	Window control 1 register	0x0000_0000
VIDOSD0A	0x4C800028	R/W	Video Window 0's position control register	0x0000_0000
VIDOSD0B	0x4C80002C	R/W	Video Window 0's position control register	0x0000_0000
VIDOSD0C	0x4C800030	R/W	Video Window 0's position control register	0x0000_0000
VIDOSD1A	0x4C800034	R/W	Video Window 1's position control register	0x0000_0000
VIDOSD1B	0x4C800038	R/W	Video Window 1's position control register	0x0000_0000
VIDOSD1C	0x4C80003C	R/W	Video Window 1's position control register	0x0000_0000

Register	Address	R/W	Description	Reset Value
VIDW00ADD0B0	0x4C800064	R/W	Window 0's buffer start address register, buffer 0	0x0000_0000
VIDW00ADD0B1	0x4C800068	R/W	Window 0's buffer start address register, buffer 1	0x0000_0000
VIDW01ADD0	0x4C80006C	R/W	Window 1's buffer start address register	0x0000_0000
VIDW00ADD1B0	0x4C80007C	R/W	Window 0's buffer end address register, buffer 0	0x0000_0000
VIDW00ADD1B1	0x4C800080	R/W	Window 0's buffer end address register, buffer 1	0x0000_0000
VIDW01ADD1	0x4C800084	R/W	Window 1's buffer end address register	0x0000_0000
VIDW00ADD2B0	0x4C800094	R/W	Window 0's buffer size register, buffer 0	0x0000_0000
VIDW00ADD2B1	0x4C800098	R/W	Window 0's buffer size register, buffer 1	0x0000_0000
VIDW01ADD2	0x4C80009C	R/W	Window 1's buffer size register	0x0000_0000
VIDINTCON	0x4C8000AC	R/W	Indicate the Video interrupt control register	0x0000_0000
W1KEYCON0	0x4C8000B0	R/W	Color key control register	0x0000_0000
W1KEYCON1	0x4C8000B4	R/W	Color key value (transparent value) register	0x0000_0000
W2KEYCON0	0x4C8000B8	R/W	Color key control register	0x0000_0000
W2KEYCON1	0x4C8000BC	R/W	Color key value (transparent value) register	0x0000_0000
W3KEYCON0	0x4C8000C0	R/W	Color key control register	0x0000_0000
W3KEYCON1	0x4C8000C4	R/W	Color key value (transparent value) register	0x0000_0000
W4KEYCON0	0x4C8000C8	R/W	Color key control register	0x0000_0000
W4KEYCON1	0x4C8000CC	R/W	Color key value (transparent value) register	0x0000_0000
WIN0MAP	0x4C8000D0	R/W	Window color control	0x0000_0000
WIN1MAP	0x4C8000D4	R/W	Window color control	0x0000_0000
WPALCON	0x4C8000E4	R/W	Window Palette control register	0x0000_0000
SYSIFCON0	0x4C800130	R/W	System Interface control for Main LDI	0x0000_0000
SYSIFCON1	0x4C800134	R/W	System Interface control for Sub LDI	0x0000_0000
DITHMODE	0x4C800138	R/W	Dithering mode register.	0x0000_0000

Video Main Control 0 Register

Register	Address	R/W	Description	Reset Value
VIDCON0	0x4C800000	R/W	Video control 1 register	0x0000_0000

VIDCON0	Bit	Description	Initial State
Reserved	[31:24]	-	0x00
INTERLACE_F	[25]	Interlace or Progressive 0: Progressive scan 1: Interlace scan	0
-	[24]	Reserved	
VIDOUT	[23:22]	It determines the output format of Video Controller 00: RGB I/F 01: Reserved 10: System I/F for Main LDI 11: System I/F for Sub LDI	0
L1_DATA16	[21:19]	Select the mode of output data format of System I/F (Sub LDI.) (Only when, VIDOUT == 2'b11) 000 = 16-bit mode (16 bpp) 001 = 16 + 2 bit mode (18 bpp) 010 = 9 + 9 bit mode (18 bpp) 011 = 16 + 8 bit mode (24 bpp) 100 = 18-bit mode (18bpp)	000
L0_DATA16	[18:16]	Select the mode of output data format of System I/F (Main LDI.) (Only when, VIDOUT == 2'b10) 000 = 16 bit mode (16 bpp) 001 = 16 + 2 bit mode (18 bpp) 010 = 9 + 9 bit mode (18 bpp) 011 = 16 + 8 bit mode (24 bpp) 100 = 18 bit mode (18bpp)	000
Reserved	[15]	-	0
PNRMODE	[14:13]	Select the display mode. (Where, VIDOUT == 2'b00) 00 = RGB Parallel format (RGB) 01 = RGB Parallel format (BGR) 10 = Serial Format (R->G->B) 11 = Serial Format (B->G->R) Select the display mode. (Where, VIDOUT == 2'b1x) 00 = RGB Parallel format (RGB)	00

VIDCON0	Bit	Description	Initial State
CLKVALUP	[12]	Select CLKVAL_F Update timing control 0 = Always 1 = Start of a frame (Only once per frame)	0
CLKVAL_F	[11:6]	Determine the rates of VCLK and CLKVAL[5:0]. VCLK = HCLK / [CLKVAL+1] (CLKVAL ≥ 1)	0
VCLKEN	[5]	VCLK Enable Control 0 = Disable 1 = Enable	0
CLKDIR	[4]	Select the clock source as direct or divide using CLKVAL_F register. 0 = Direct clock (frequency of VCLK = frequency of Clock source) 1 = Divided using CLKVAL_F	0
CLKSEL_F	[3:2]	Select the Video Clock source 00 = HCLK 01 = LCD video Clock (from SYSCON EPLL) 10 = reserved 11 = reserved	0
ENVID	[1]	Video output and the logic immediately enable/disable. 0 = Disable the video output and the Display control signal. 1 = Enable the video output and the Display control signal.	0
ENVID_F	[0]	Video output and the logic enable/disable at current frame end. 0 = Disable the video output and the Display control signal. 1 = Enable the video output and the Display control signal. * If set on and off this bit, then you will read “H” and video controller enable until the end of current frame.	0

NOTE: Display On : ENVID & ENVID_F set to “1”
Direct Off : ENVID & ENVID_F set to “0” simultaneously
Per Frame Off: ENVID_F set “0” & ENVID set ”1”

Video Main Control 1 Register

Register	Address	R/W	Description	Reset Value
VIDCON1	0x4C800004	R/W	Video control 2 register	0x0000_0000

VIDCON1	Bit	Description	Initial state
LINECNT (read only)	[26:16]	Provide the status of the line counter (read only) Up count from 0 to LINEVAL	0
Reserved	[15]	Reserved	0
VSTATUS	[14:13]	Vertical Status (read only). 00 = VSYNC 01 = BACK Porch 10 = ACTIVE 11 = FRONT Porch	0
HSTATUS	[12:11]	Horizontal Status (read only). 00 = HSYNC 01 = BACK Porch 10 = ACTIVE 11 = FRONT Porch	0
-	[10:8]	Reserved	
IVCLK	[7]	This bit controls the polarity of the VCLK active edge. 0 = The video data is fetched at VCLK falling edge 1 = The video data is fetched at VCLK rising edge	0
IHSYNC	[6]	This bit indicates the HSYNC pulse polarity. 0 = normal 1 = inverted	0
IVSYNC	[5]	This bit indicates the VSYNC pulse polarity. 0 = normal 1 = inverted	0
IVDEN	[4]	This bit indicates the VDEN signal polarity. 0 = normal 1 = inverted	0
Reserved	[3:0]		0x0

VIDEO Time Control 0 Register

Register	Address	R/W	Description	Reset Value
VIDTCON0	0x4C800008	R/W	Video time control 1 register	0x0000_0000

VIDTCON0	Bit	Description	Initial State
VBPDE	[31:24]	Vertical back porch is the number of inactive lines at the start of a frame, after vertical synchronization period. (Only for the even field of YVU interface)	0x00
VBPD	[23:16]	Vertical back porch is the number of inactive lines at the start of a frame, after vertical synchronization period.	0x00
VFPD	[15:8]	Vertical front porch is the number of inactive lines at the end of a frame, before vertical synchronization period.	0x00
VSPW	[7:0]	Vertical sync pulse width determines the VSYNC pulse's high level width by counting the number of inactive lines.	0x00

Video Time Control 1 Register

Register	Address	R/W	Description	Reset Value
VIDTCON1	0x4C80000C	R/W	Video time control 2 register	0x0000_0000

VIDTCON1	Bit	Description	Initial state
VFPDE	[31:24]	Vertical front porch is the number of inactive lines at the end of a frame, before vertical synchronization period. (Only for the even field of YVU interface)	0
HBPD	[23:16]	Horizontal back porch is the number of VCLK periods between the falling edge of HSYNC and the start of active data. *Note. Set 0x10 for System Interface*	0000000
HFPD	[15:8]	Horizontal front porch is the number of VCLK periods between the end of active data and the rising edge of HSYNC.	0x00
HSPW	[7:0]	Horizontal sync pulse width determines the HSYNC pulse's high level width by counting the number of the VCLK.	0x00

VIDEO Time Control 2 Register

Register	Address	R/W	Description	Reset Value
VIDTCON2	0x4C800010	R/W	Video time control 3 register	0x0000_0000

VIDTCON2	Bit	Description	Initial state
LINEVAL	[21:11]	These bits determine the vertical size of display	0
HOZVAL	[10:0]	These bits determine the horizontal size of display	0

Window 0 Control Register

Register	Address	R/W	Description	Reset Value
WINCON0	0x4C800014	R/W	Window 0 control register	0x0000_0000

WINCON0	Bit	Description	Initial State
Reserved	[24]	Reserved (should be set “0”)	0
BUFSEL	[23]	Select Buffer set (0/1) 0 = buffer set 0 1 = buffer set 1	0
BUFAUTOEN	[22]	Double Buffer Auto control bit 0 = Fixed by BUFSEL, 1 = Auto changed by Trigger Input	0
BITSWP	[18]	Bit swap control bit. 0 = Swap Disable 1 = Swap Enable	0
BYTSWP	[17]	Byte swaps control bit. 0 = Swap Disable 1 = Swap Enable	0
HAWSWP	[16]	Half-Word swap control bit. 0 = Swap Disable 1 = Swap Enable	0
Reserved	[15:14]	Reserved	0
Reserved	[13]	Reserved	0
Reserved	[12:11]	Reserved	0
BURSTLEN	[10:9]	DMA’s Burst Length selection: 00: 16 word– burst 01: 8 word– burst 10: 4 word– burst	0
Reserved	[8:6]	-	0
BPPMODE_F	[5:2]	Select the BPP (Bits Per Pixel) mode Window image. 0000 = 1 bpp 0001 = 2 bpp 0010 = 4 bpp 0011 = 8 bpp (palletized) 0100 = reserved 0101 = 16 bpp (non-palletized, R: 5-G:6-B:5) 0110 = reserved 0111 = 16 bpp (non-palletized, I :1-R:5-G:5-B:5) 1000 = unpacked 18 bpp (non-palletized, R:6-G:6-B:6) 1001 = reserved 1010 = reserved 1011 = unpacked 24 bpp (non-palletized R:8-G:8-B:8) 11xx = reserved	0
Reserved	[1]	-	0
ENWIN_F	[0]	Video output and the logic immediately enable/disable. 0 = Disable the video output and the VIDEO control signal. 1 = Enable the video output and the VIDEO control signal.	0

Window 1 Control Register

Register	Address	R/W	Description	Reset Value
WINCON1	0x4C800018	R/W	Window control 1 register	0x0000_0000

WINCON1	Bit	Description	Initial State
BITSWP	[18]	Bit swap control bit. 0 = Swap Disable 1 = Swap Enable	0
BYTSWP	[17]	Byte swaps control bit. 0 = Swap Disable 1 = Swap Enable	0
HAWSWP	[16]	Half-Word swap control bit. 0 = Swap Disable 1 = Swap Enable	0
-	[15:11]	Reserved	0
BURSTLEN	[10:9]	DMA's Burst Length selection : 00 : 16 word– burst 01 : 8 word– burst 10 : 4 word– burst	0
Reserved	[8:7]	-	0
BLD_PIX	[6]	Select blending category 0 = Per plane blending 1 = Per pixel blending	0
BPPMODE_F	[5:2]	Select the BPP (Bits Per Pixel) mode Window image. 0000 = 1 bpp 0001 = 2 bpp 0010 = 4 bpp 0011 = 8 bpp (palletized) 0100 = 8 bpp (non-palletized, A: 1-R:2-G:3-B:2) 0101 = 16 bpp (non-palletized, R:5-G:6-B:5) 0110 = 16 bpp (non-palletized, A:1-R:5-G:5-B:5) 0111 = 16 bpp (non-palletized, I :1-R:5-G:5-B:5) 1000 = unpacked 18 bpp (non-palletized, R:6-G:6-B:6) 1001 = unpacked 18 bpp (non-palletized, A:1-R:6-G:6-B:5) 1010 = unpacked 19 bpp (non-palletized, A:1-R:6-G:6-B:6) 1011 = unpacked 24 bpp (non-palletized R:8-G:8-B:8) 1100 = unpacked 24 bpp (non-palletized A:1-R:8-G:8-B:7) 1101 = unpacked 25 bpp (non-palletized A:1-R:8-G:8-B:8) 111x = reserved *Note. 1101 = support unpacked 28 bpp (non-palletized A:4-R:8-G:8-B:8) for per frame blending.*	0
ALPHA_SEL	[1]	Select Alpha value by When Per plane blending case(BLD_PIX ==0) 0 = using ALPHA0_R/G/B values 1 = using ALPHA1_R/G/B values When Per pixel blending (BLD_PIX ==1) 0 = selected by AEN (A value) or chroma key 1 = using DATA[27:24] data ,only for 24bpp (8:8:8) mode	0
ENWIN_F	[0]	Video output and the logic immediately enable/disable. 0 = Disable the video output and the VIDEO control signal. 1 = Enable the video output and the VIDEO control signal.	0

Window 0 Position Control A Register

Register	Address	R/W	Description	Reset Value
VIDOSD0A	0x4C800028	R/W	Video Window 0's position control register	0x0

VIDOSD0A	Bit	Description	initial state
OSD_LeftTopX_F	[21:11]	Horizontal screen coordinate for left top pixel of OSD image	0
OSD_LeftTopY_F	[10:0]	Vertical screen coordinate for left top pixel of OSD image	0

Window 0 Position Control B Register

Register	Address	R/W	Description	Reset Value
VIDOSD0B	0x4C80002C	R/W	Video Window 0's position control register	0x0

VIDOSD0B	Bit	Description	initial state
OSD_RightBotX_F	[21:11]	Horizontal screen coordinate for right bottom pixel of OSD image	0
OSD_RightBotY_F	[10:0]	Vertical screen coordinate for right bottom pixel of OSD image	0

NOTE: Registers must have word boundary X position.
So, 24 Bpp mode should have X position by 1 pixel. (ex, X = 0,1,2,3….)
16 Bpp mode should have X position by 2 pixel. (ex, X = 0,2,4,6….)
8 Bpp mode should have X position by 4 pixel. (ex, X = 0,4,8,12….)

Window 1 Position Control A Register

Register	Address	R/W	Description	Reset Value
VIDOSD1A	0x4C800034	R/W	Video Window 1's position control 2 register	0x0

VIDOSD1A	Bit	Description	initial state
OSD_LeftTopX_F	[21:11]	Horizontal screen coordinate for left top pixel of OSD image	0
OSD_LeftTopY_F	[10:0]	Vertical screen coordinate for left top pixel of OSD image	0

Window 1 Position Control B Register

Register	Address	R/W	Description	Reset Value
VIDOSD1B	0x4C800038	R/W	Video Window 1's position control register	0x0

VIDOSD1B	Bit	Description	Initial state
OSD_RightBotX_F	[21:11]	Horizontal screen coordinate for right bottom pixel of OSD image	0
OSD_RightBotY_F	[10:0]	Vertical screen coordinate for right bottom pixel of OSD image	0

NOTE: Registers must have word boundary X position.
So, 24 Bpp mode should have X position by 1 pixel. (ex, X = 0,1,2,3….)
16 Bpp mode should have X position by 2 pixel. (ex, X = 0,2,4,6….)
8 Bpp mode should have X position by 4 pixel. (ex, X = 0,4,8,12….)

Window 1 Position Control C Register

Register	Address	R/W	Description	Reset Value
VIDOSD1C	0x4C80003C	R/W	Video Window 1's alpha control register	0x0

VIDOSD1C	Bit	Description	Initial state
-	[24]	Reserved	0
ALPHA0_R	[23:20]	Red Alpha value(case AEN == 0)	0
ALPHA0_G	[19:16]	Green Alpha value(case AEN == 0)	0
ALPHA0_B	[15:12]	Blue Alpha value(case AEN == 0)	0
ALPHA1_R	[11:8]	Red Alpha value(case AEN == 1)	0
ALPHA1_G	[7:4]	Green Alpha value(case AEN == 1)	0
ALPHA1_B	[3:0]	Blue Alpha value(case AEN == 1)	0

FRAME Buffer Address 0 Register

Register	Address	R/W	Description	Reset Value
VIDW00ADD0B0	0x4C800064	R/W	Window 0's buffer start address register, buffer 0	0x0
VIDW00ADD0B1	0x4C800068	R/W	Window 0's buffer start address register, buffer 1	0x0
VIDW01ADD0	0x4C80006C	R/W	Window 1's buffer start address register	0x0

VIDWxxADD0	Bit	Description	Initial State
VBANK_F	[31:24]	These bits indicate A[31:24] of the bank location for the video buffer in the system memory.	0
VBASEU_F	[23:0]	These bits indicate A[23:0] of the start address of the Video frame buffer.	0

FRAME Buffer Address 1 Register

Register	Address	R/W	Description	Reset Value
VIDW00ADD1B0	0x4C80007C	R/W	Window 0's buffer end address register, buffer 0	0x0
VIDW00ADD1B1	0x4C800080	R/W	Window 0's buffer end address register, buffer 1	0x0
VIDW01ADD1	0x4C800084	R/W	Window 1's buffer end address register	0x0

VIDWxxADD1	Bit	Description	Initial State
VBASEL_F	[23:0]	These bits indicate A[23:0] of the end address of the Video frame buffer. VBASEL = VBASEU + (PAGEWIDTH+OFFSIZE) x (LINEVAL+1)	0x0

FRAME Buffer Address 2 Register(Virtual screen)

Register	Address	R/W	Description	Reset Value
VIDW00ADD2B0	0x4C800094	R/W	Window 0's buffer size register, buffer 0	0x0
VIDW00ADD2B1	0x4C800098	R/W	Window 0's buffer size register, buffer 1	0x0
VIDW01ADD2	0x4C80009C	R/W	Window 1's buffer size register	0x0

VIDWxxADD2	Bit	Description	Initial State
OFFSIZE_F	[25:13]	Virtual screen offset size (the number of byte). This value defines the difference between the address of the last byte displayed on the previous Video line and the address of the first byte to be displayed in the new Video line. OFFSIZE_F must have value more than burst size value or 0.	0
PAGEWIDTH_F	[12:0]	Virtual screen page width (the number of byte). This value defines the width of the view port in the frame. PAGEWIDTH must have value which is multiple of the burst size.	0

VIDEO interrupt Control Register

Register	Address	R/W	Description	Reset Value
VIDINTCON	0x4C8000AC	R/W	Indicate the Video interrupt control register	0x3F00000

VIDINTCON	Bit	Description	Initial state
FIFOINTERVAL	[25:20]	These bits control the interval of the interval of the FIFO interrupt.	0x3F
SYSMAINCON	[19]	Sending complete interrupt enable bit to Main LCD 0 = Interrupt Disable. 1 = Interrupt Enable.	0
SYSSUBCON	[18]	Sending complete interrupt enable bit to Sub LCD 0 = Interrupt Disable. 1 = Interrupt Enable.	0
SYSIFDONE	[17]	System Interface Interrupt Enable control (only for System Interface mode). 0 = Interrupt Disable. 1 = Interrupt Enable.	0
FRAMESEL0	[16:15]	Video Frame Interrupt 0 at start of : 00 = BACK Porch 01 = VSYNC 10 = ACTIVE 11 = FRONT Porch	0
FRAMESEL1	[14:13]	Video Frame Interrupt 1 at start of : 00 = None 01 = BACK Porch 10 = VSYNC 11 = FRONT Porch	0
INTFRMEN	[12]	Video Frame interrupts Enable control bit. 0 = Video Frame Interrupt Disable 1 = Video Frame Interrupt Enable	0
FIFOSEL	[11:5]	FIFO Interrupt control bit, each bit has the meaning of [11:7] Reserved [6] Window 1 control (0: disable, 1: enable) [5] Window 0 control (0: disable, 1: enable)	0
FIFOLEVEL	[4:2]	Video FIFO Interrupt Level Select 000 = 25% left 001 = 50% left 010 = 75% left 011 = empty 100 = full	0
INTFIFOEN	[1]	Video FIFO interrupts Enable control bit. 0 = Video FIFO Level Interrupt Disable 1 = Video FIFO Level Interrupt Enable	0
INTEN	[0]	Video interrupts Enable control bit. 0 = Video Interrupt Disable 1 = Video Interrupt Enable	0

Win1 Color Key 0 Register

Register	Address	R/W	Description	Reset Value
W1KEYCON0	0x4C8000B0	R/W	Color key control register	0x00000

W1KEYCON0	Bit	Description	Initial state
KEYBLEN	[26]	Blending Enable control 0 = disable (blending operation disable) 1 = Blending using ALPHA0_x for non-key area, ALPHA1_x for key area (set BLD_PIX = 1and ALPHA_SEL =0, to use color key function)	0
KEYEN_F	[25]	Color Key (Chroma key) Enable control 0 = color key disable 1 = color key enable	0
DIRCON	[24]	Color key (Chroma key) direction control 0 = If the pixel value match fore-ground image with COLVAL, pixel from back-ground image is displayed (only in OSD area) 1 = If the pixel value match back-ground with COLVAL, pixel from fore-ground image is displayed (only in OSD area)	0
COMPKEY	[23:0]	Each bit is correspond to the COLVAL[23:0]. If some position bit is set then that position bit of COLVAL will be disabled.	0

WIN 1 Color key 1 Register

Register	Address	R/W	Description	Reset Value
W1KEYCON1	0x4C8000B4	R/W	**Color key value (transparent value) register**	0x0000_0000

W1KEYCON1	Bit	Description	Initial state
COLVAL	[23:0]	Color key value for the transparent pixel effect.	0

NoteS:

1. COLVAL and COMPKEY use 24bit color data at all bpp mode.
   @ BPP24 mode : 24 bit color value is valid.

   A. COLVAL
   - Red : COLVAL[23:17]
   - Green: COLVAL[15: 8]
   - Blue : COLVAL[7:0]

   B. COMPKEY
   - Red : COMPKEY[23:17]
   - Green: COMPKEY[15: 8]
   - Blue : COMPKEY[7:0]

   @ BPP16 (5:6:5) mode : 16 bit color value is valid

   A. COLVAL
   - Red : COLVAL[23:19]
   - Green: COLVAL[15: 10]
   - Blue : COLVAL[7:3]

   B. COMPKEY
   - Red : COMPKEY[23: 19]
   - Green: COMPKEY[15: 10]
   - Blue : COMPKEY[7: 3]

   - COMPKEY[18:16] must be 0x7.
   - COMPKEY[9: 8] must be 0x3.
   - COMPKEY[2:0] must be 0x7.

2. COMPKEY register must be set properly for the each bpp mode.

WIN0 Color MAP

Register	Address	R/W	Description	Reset Value
WIN0MAP	0x4C8000D0	R/W	Window color control	0x00000

WIN0MAP	Bit	Description	Initial state
MAPCOLEN_F	[24]	Window's color mapping control bit. If this bit is enabled then Video DMA will stop, and MAPCOLOR will be appear on back-ground image instead of original image. 0 = disable 1 = enable	0
MAPCOLOR	[23:0]	Color Value	0

WIN1 Color MAP

Register	Address	R/W	Description	Reset Value
WIN1MAP	0x4C8000D4	R/W	Window color control	0x00000

WIN1MAP	Bit	Description	Initial state
MAPCOLEN_F	[24]	Window's color mapping control bit . If this bit is enabled then Video DMA will stop, and MAPCOLOR will be appear on back-ground image instead of original image. 0 = disable 1 = enable	0
MAPCOLOR	[23:0]	Color Value	0

Window Palette control Register

Register	Address	R/W	Description	Reset Value
WPALCON	0x4C8000E4	R/W	Window Palette control register	0x0000_0000

WPALCON	Bit	Description	Initial state
PALUPDATEEN	[9]	0: Normal Mode 1: Enable (Palette Update)	0
W1PAL	[5:3]	This bit determines the size of the palette data format of Window 1 000 = 25-bit (A:8:8:8) 001 = 24-bit (8:8:8) 010 = 19-bit (A:6:6:6) 011 = 18-bit (A:6:6:5) 100 = 18-bit (6:6:6) 101 = 16-bit (A:5:5:5) 110 = 16-bit (5:6:5)	0
W0PAL	[2:0]	This bit determines the size of the palette data format of Window 0 000 = 25-bit (A:8:8:8) 001 = 24-bit (8:8:8) 010 = 19-bit (A:6:6:6) 011 = 18-bit (A:6:6:5) 100 = 18-bit (6:6:6) 101 = 16-bit (A:5:5:5) 110 = 16-bit (5:6:5)	0

Main LCD System Interface control

Register	Address	R/W	Description	Reset Value
SYSIFCON0	0x4C800130	R/W	System Interface control for Main LDI(LCD)	0x0
SYSIFCON1	0x4C800134	R/W	System Interface control for Sub LDI(LCD)	0x0

SYSIFCONx	Bit	Description	Initial State
Reserved	[23:20]	-	0
LCD_CS_ SETUP	[19:16]	Numbers of clock cycles for the active period of the address signal enable to the chip select enable.	0
LCD_WR _SETUP	[15:12]	Numbers of clock cycles for the active period of the CS signal enable to the write signal enable.	0
LCD_WR_ACT	[11:8]	Numbers of clock cycles for the active period of the chip select enable.	0
LCD_WR _HOLD	[7:4]	Numbers of clock cycles for the active period of the chip select disable to the write signal disable.	0
-	[3]	Reserved	0
RSPOL	[2]	The polarity of the RS Signal 0: Low 1: High * Set to 1 for normal access.	0
SUCCEUP	[1]	1: triggered mode(Should be 1)	0
SYSIFEN	[0]	LCD System Interface control 0: Disable 1: Enable	0

Dithering Control 1 Register

Register	Address	R/W	Description	Reset Value
DITHMODE	0x4C800138	R/W	Dithering mode register.	0x00000

DITHMODE	Bit	Description	Initial state
Reserved	[30:7]	Not used for normal access (Write not-zero values to these register make to come out abnormal result)	0
RDithPos	[6:5]	Red Dither bit control 00 : 5-bit 01 : 6-bit 10 : 8-bit	0
GDithPos	[4:3]	Green Dither bit control 00 : 5-bit 01 : 6-bit 10 : 8-bit	0
BDithPos	[2:1]	Blue Dither bit control 00 : 5-bit 01 : 6-bit 10 : 8-bit	0
DITHEN_F	[0]	Dithering Enable bit 0 = dithering disable 1 = dithering enable	0

System Interface Command Control 0

Register	Address	R/W	Description	Reset Value
SIFCCON0	0x4C80013C	R/W	System Interface Command Control	0x0

SIFCCON0	Bit	Description	Initial State
Reserved	[11:10]	-	0
SYS_nCS1_ CON	[9]	LCD System Interface nCS0 (main) Signal control 0: Disable (High) 1: Enable (Low)	0
SYS_nCS0_ CON	[8]	LCD System Interface nCS1 (sub) Signal control 0: Disable (High) 1: Enable (Low)	0
SYS_nOE_CON	[7]	LCD System Interface nOE Signal control 0: Disable (High) 1: Enable (Low)	0
SYS_nWE_CON	[6]	LCD System Interface nWE Signal control 0: Disable (High) 1: Enable (Low)	0
reserved	[5:2]	Reserved (Should be set be “0”)	0
SYS_RS_CON	[1]	LCD System Interface RS Signal control 0: Low 1: High	0
SCOMEN	[0]	LCD System Interface Command Mode Enable 0: Disable 1: Enable	

System Interface Command Control 1

Register	Address	R/W	Description	Reset Value
SIFCCON1	0x4C800140	R/W	System Interface Command Data Write Control	0x0

SIFCCON1	Bit	Description	Initial State
Reserved	[23:18]	-	0
SYS_WDATA	[17:0]	LCD System Interface Write Data Control	0

System Interface Command Control 2

Register	Address	R	Description	Reset Value
SIFCCON2	0x4C800144	R	System Interface Command Data Read Control	0x0

SIFCCON2	Bit	Description	Initial State
Reserved	[23:18]	-	0
SYS_RDATA	[17:0]	LCD System Interface Read Data Control	0

CPU IF TRIGGER CONTROL 2 Register

Register	Address	R/W	Description	Reset Value
CPUTRIGCON2	0x4C800160	R/W	Software-Based Trigger control register	0x0

CPUTRIGCON2	Bit	Description	Initial State
SWTRIG	[0]	Software-Based Trigger When this bit is set, trigger happens. This bit is automatically cleared. This flag must be set after display is on. To check display-on status, see VIDCON0 register.	0

WIN0 Palette Ram Access Address (not SFR)

Register	Address	R/W	Description	Reset Value
00	0x4C800400	R/W	Window 0 Palette entry 0 address	undefined
01	0x4C800404	R/W	Window 0 Palette entry 1 address	undefined
-	-	-	-	-
FF	0x4C8007FC	R/W	Window 0 Palette entry 255 address	undefined

WIN1 Palette Ram Access Address (not SFR)

Register	Address	R/W	Description	Reset Value
00	0x4C800800	R/W	Window 1 Palette entry 0 address	undefined
01	0x4C800804	R/W	Window 1 Palette entry 1 address	undefined
-	-	-	-	-
FF	0x4C800BFC	R/W	Window 1 Palette entry 255 -address	undefined

23 CAMERA INTERFACE

OVERVIEW

This specification defines the interface of camera. The CAMIF (Camera Interface) within the S3C2443X consists of eight parts. They are the pattern mux, capturing unit, MSDMA (Memory Scaling DMA), preview scaler, codec scaler, preview DMA, codec DMA, and SFR. The camera interface supports ITU R BT-601/656 YCbCr 8-bit standard and Memory. Maximum input size is 4096x4096 pixels (2048x2048 pixels for scaling).Two scalers exist. The one is the preview scaler, which is dedicated to generate smaller size image for preview. The other one is the codec scaler, which is dedicated to generate codec useful image like plane type YCbCr 4:2:0 or 4:2:2. Two master DMAs can do mirror and rotate the captured image for mobile environments. And test pattern generation can be used to calibration of input sync signals as HREF, VSYNC. Also, video sync signals and pixel clock polarity can be inverted in the camera interface side with using register setting.

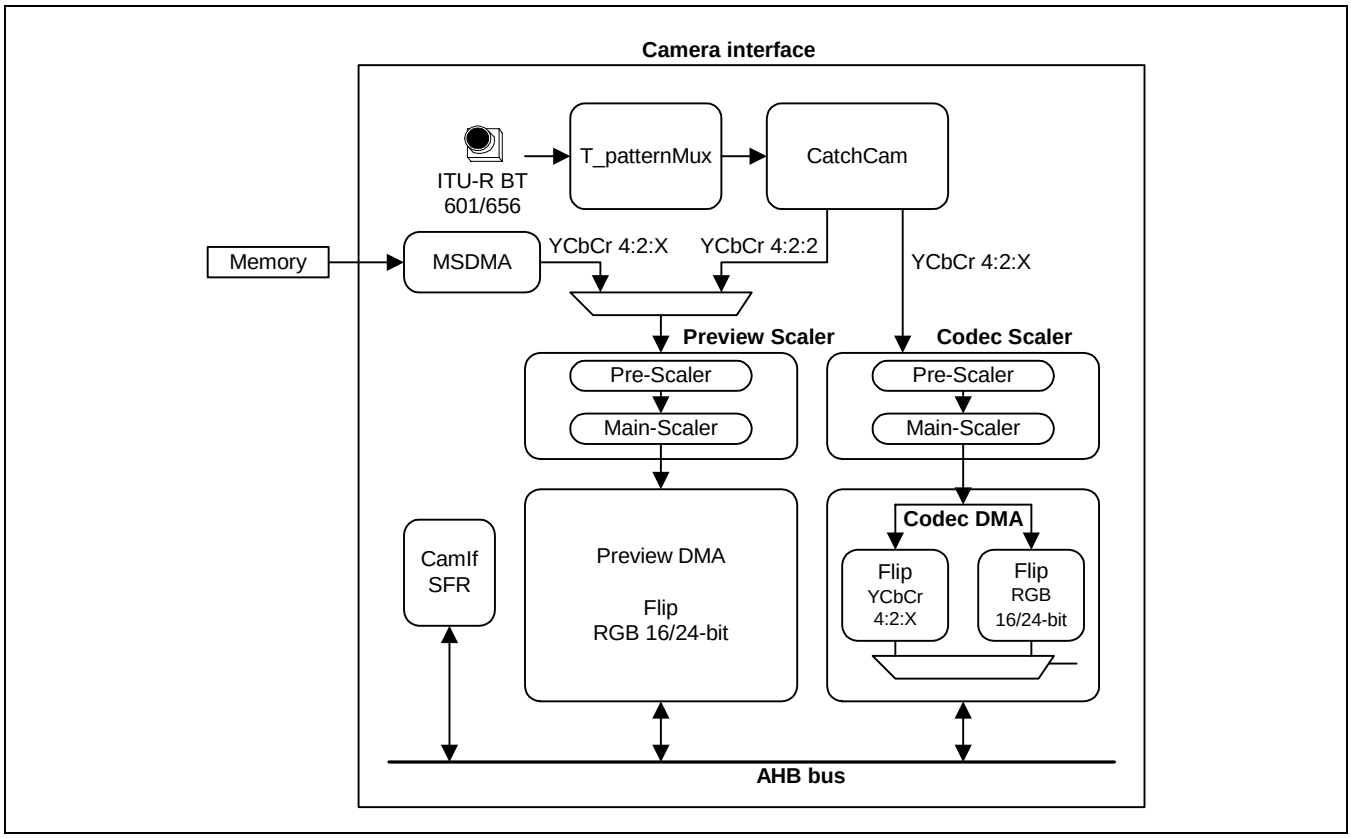


Figure 23-1. Camera interface overview

FEATURES

— ITU-R BT 601/656 8-bit mode support
— DZI (Digital Zoom In) capability
— Programmable polarity of video sync signals
— Max. 4096 x 4096 pixels input support (non-scaling)
— Max. 2048 x 2048 pixels input support for codec scaling and 640 x 480 pixels input support for preview scaling
— Image mirror and rotation (X-axis mirror, Y-axis mirror and 180° rotation)
— Preview DMA output image generation (RGB 16/24-bit format)
— Codec DMA output image generation (RGB 16/24-bit format or YCbCr 4:2:0/4:2:2 format)
— Capture frame control support in codec_path
— Scan line offset support in codec_path (YCbCr)
— YCbCr 4:2:2 codec image format interleave support
— MSDMA supports memory data for preview path input.
— Image effect

EXTERNAL INTERFACE

CAMIF can support the next video standards.

— ITU-R BT 601 YCbCr 8-bit mode
— ITU-R BT 656 YCbCr 8-bit mode

SIGNAL DESCRIPTION

Table 23-1. Camera interface signal description

Name	I/O	Active	Description
CAMPCLK	I	-	Pixel Clock, driven by the Camera processor
CAMVSYNC	I	H/L	Frame Sync, driven by the Camera processor
CAMHREF	I	H/L	Horizontal Sync, driven by the Camera processor
CAMDATA [7:0]	I	-	Pixel Data driven by the Camera processor
CAMCLKOUT	O	-	Master Clock to the Camera processors
CAMRESET	O	H/L	Software Reset or Power Down for the Camera processor

TIMING DIAGRAM

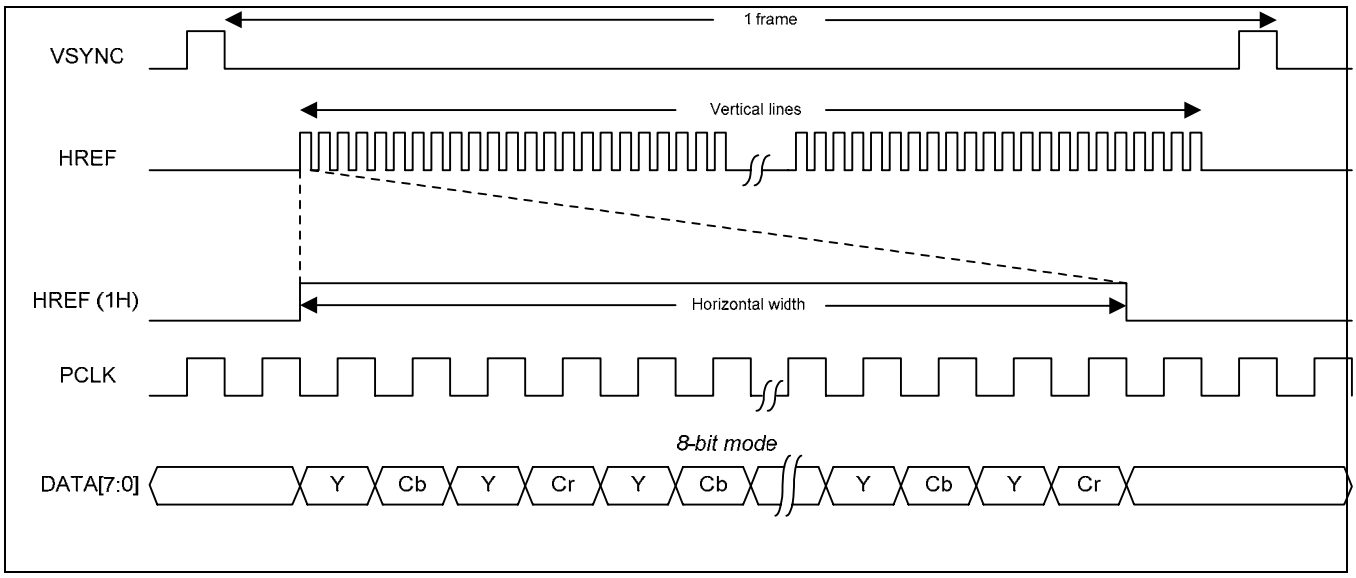


Figure 23-2. ITU-R BT 601 Input timing diagram

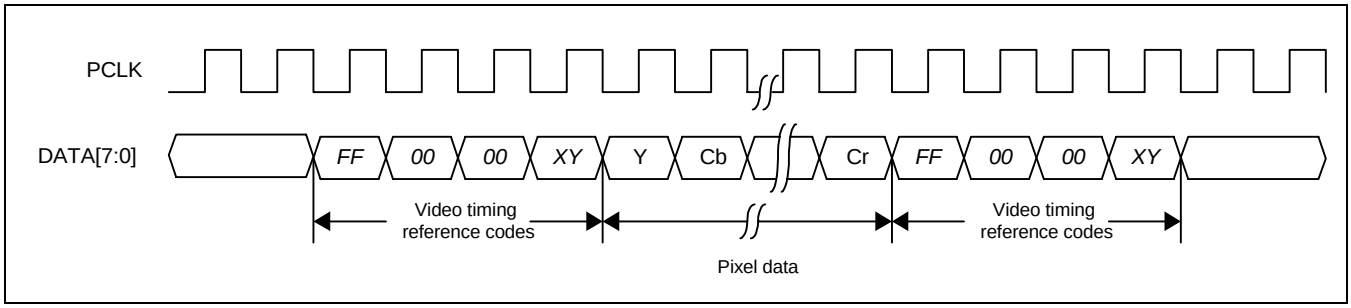


Figure 23-3. ITU-R BT 656 Input timing diagram

There are two timing reference signals in ITU-R BT 656 format, one at the beginning of each video data block (start of active video, SAV) and one at the end of each video data block(end of active video, EAV) as shown in Figure 23-3 and below table.

Table 23-2. Video timing reference codes of ITU-656 format

Data bit number	First word	Second word	Third word	Fourth word
9 (MSB)	1	0	0	1
8	1	0	0	F
7	1	0	0	V
6	1	0	0	H
5	1	0	0	P3
4	1	0	0	P2
3	1	0	0	P1
2	1	0	0	P0
1 (Note 1)	1	0	0	0
0	1	0	0	0

NOTE: For compatibility with existing 8-bit interfaces, the values of bits D1 and D0 are not defined.
F = 0 (during field 1), 1 (during field 2)
V = 0 (elsewhere), 1 (during field blanking)
H = 0 (in SAV : Start of Active Video), 1 (in EAV : End of Active Video)
P0, P1, P2, P3 = protection bit
Camera interface logic can catch the video sync bits like H(SAV,EAV) and V(Frame Sync) after reserved data as "FF-00-00".

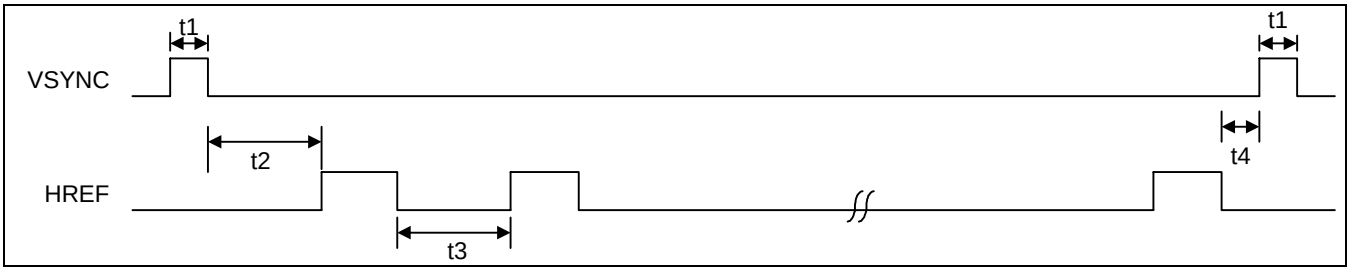


Figure 23-4 Sync signal timing diagram

Table 23-3. Sync signal timing requirement

	Minimum	Maximum
t1	12 cycles of Pixel clock	-
t2	12 cycles of Pixel clock	-
t3	2 cycles of Pixel clock	-
t4	12 cycles of Pixel clock	-

Note! (t4 + t1) must be long enough to finish DMA transactions if preview is enabled or output data format of codec is RGB. Because, DMA transaction for preview and codec RGB are delayed by 4 or 8 horizontal lines.

EXTERNAL/INTERNAL CONNECTION GUIDE

All CAMIF input signals should not occur inter-skewing to pixel clock line. Recommend next pin location and routing.

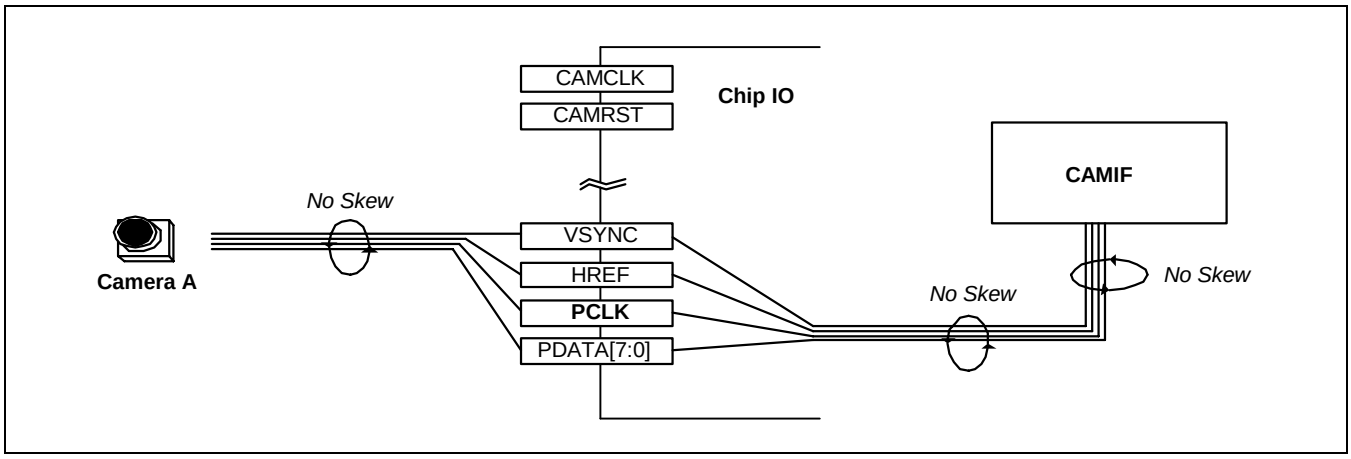


Figure 23-5. IO connection guide

CAMERA INTERFACE OPERATION

TWO DMA PORTS

CAMIF has two DMA port. P-port(Preview port) and C-port(Codec port) are separated from each other on AHB bus. At the view of system bus, two ports are independent. The P-port stores the RGB image data into memory for preview. The C-port stores the YCbCr 4:2:0 or 4:2:2 image data or RGB image data into memory for Codec as MPEG-4, H.263, etc. These two master ports support the variable applications like DSC (Digital Still Camera), MPEG-4 video conference, video recording, etc. For example, P-port image can be used as preview image, and C-port image can be used as JPEG image in DSC application. Also, the register setting can separately disable P-port or C-port.

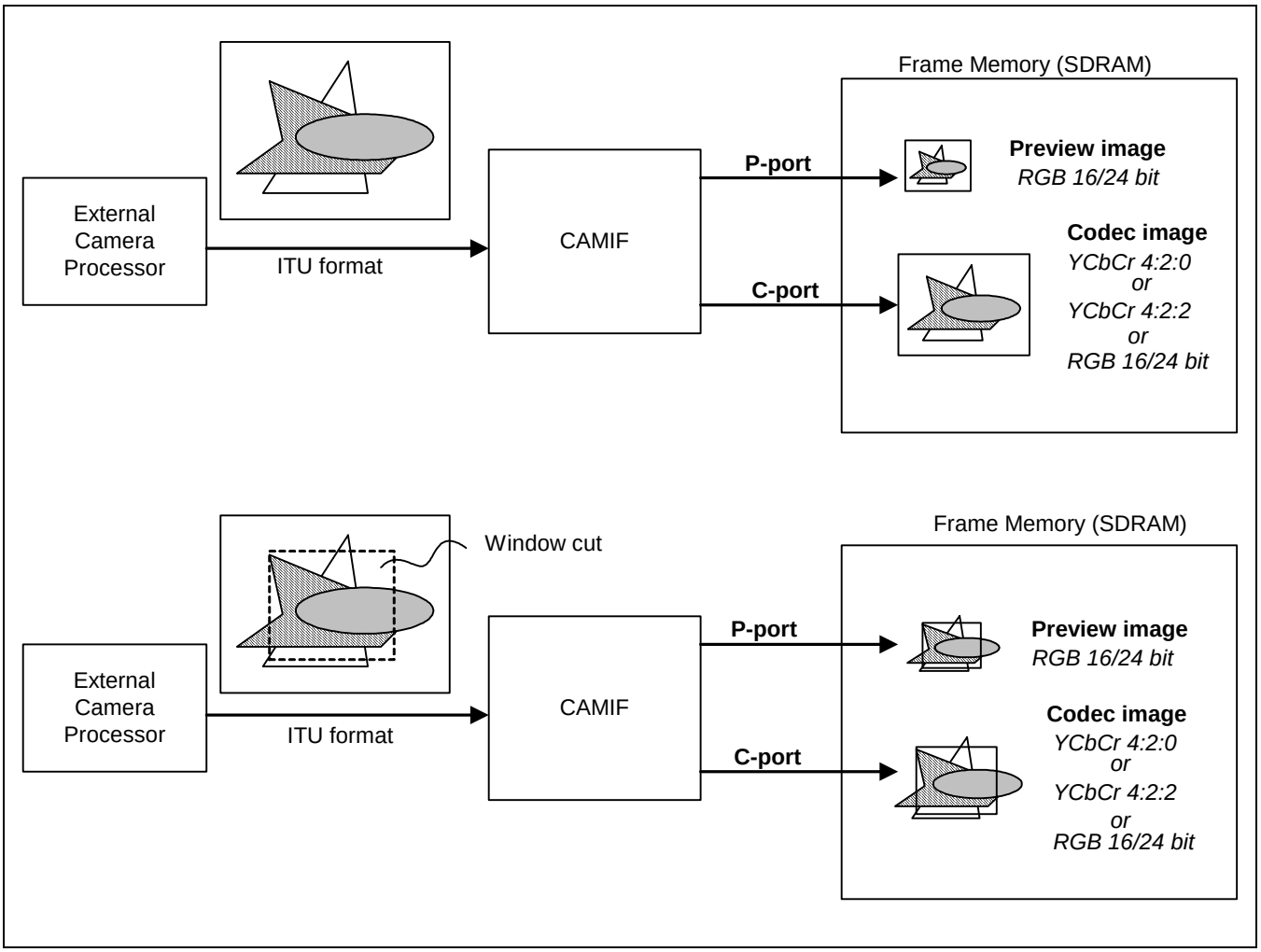


Figure 23-6. Two DMA ports

CLOCK DOMAIN

CAMIF has two clock domains. The one is the system bus clock, which is HCLK. The other is the pixel clock, which is PCLK. *The system clock must be faster than pixel clock*. As shown in figure 23-7, CAMCLK must be divided from the fixed frequency like USB PLL clock. If external clock oscillator were used, CAMCLK should be floated. Internal scaler clock is system clock. It is not necessary for two clock domains to be synchronized each other. Other signals as PCLK should be similarly connected to shimitt-triggered level shifter.

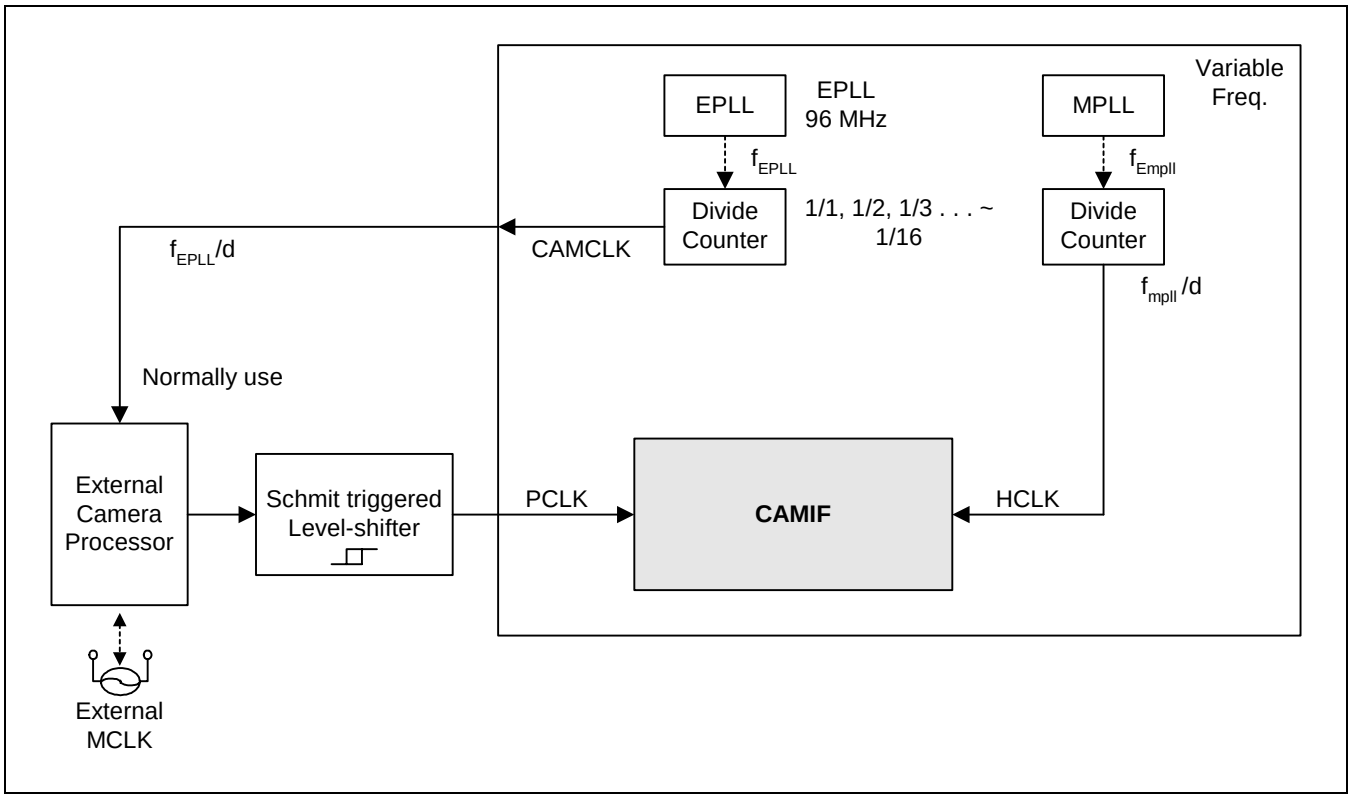


Figure 23-7. CAMIF clock generation

FRAME MEMORY HIRERARCHY

Frame memories consist of four ping-pong memories for each P- and C-ports. C-port ping-pong memories have three element memories that are luminance Y, chrominance Cb, and chrominance Cr. It is recommended that the arbitration priority of CAMIF must be higher than any other masters except LCD controller. It is strongly recommended that CAMIF priorities should be the fixed priorities, not rotation priorities. And in multi-AHB bus case, the priority of system bus including CAMIF must be higher than others. If AHB-bus is traffic enough that DMA operation is not ending during one horizontal period plus blank, it might be entered into mal-function. So, the priority of CAMIF must be separated to other round robin or circular arbitration priorities. Also, it is recommended that AHB bus which include CAMIF, should have higher priority than any other multi-AHB buses in memory matrix system. And CAMIF should not be the default master of AMBA AHB system.

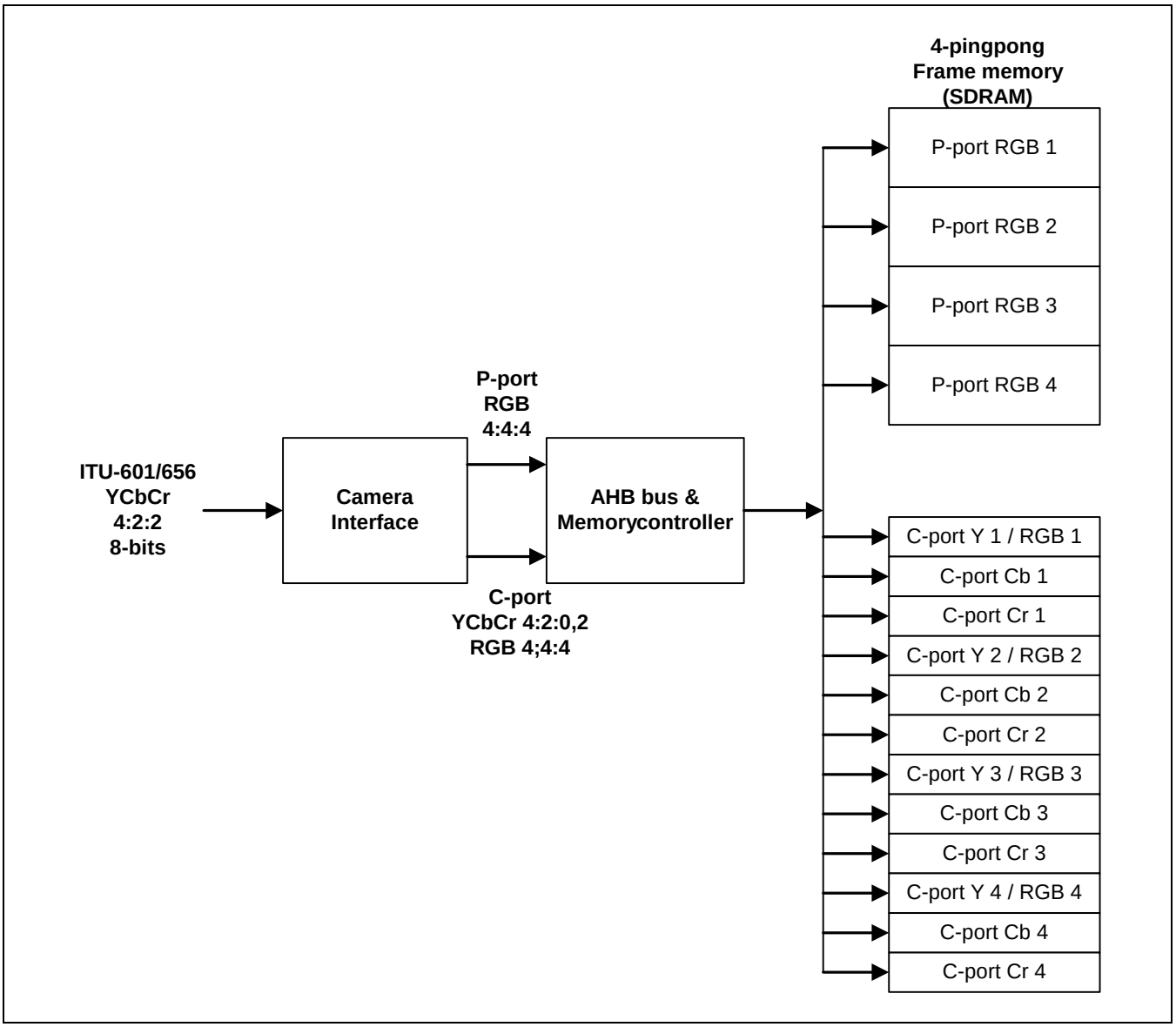


Figure 23-8. Ping-pong Memory Hierarchy

MEMORY STORING METHOD

The storing method to the frame memory is the little-endian method in codec path. The first entering pixels stored into LSB sides, and the last entering pixels stored into MSB sides. The carried data by AHB bus is 32-bit word. So, CAMIF make the each Y-Cb-Cr words by little endian style. For RGB format, two different formats exist. One pixel (Color 1 pixel) is one word for RGB 24-bit format. Otherwise, two pixels are one word for RGB 16-bit format. Refer to next diagram.

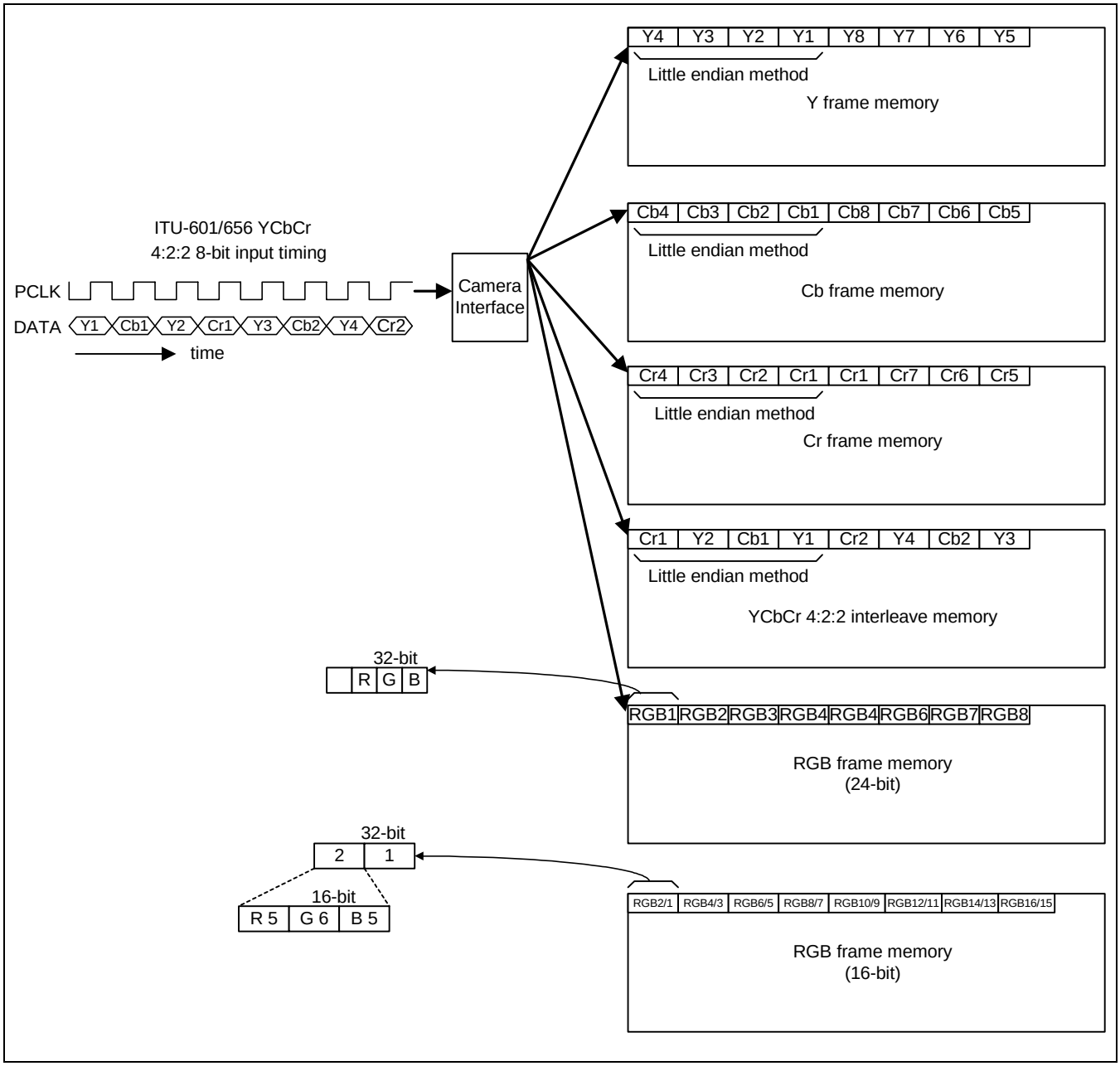


Figure 23-9. Memory storing style

TIMING DIAGRAM FOR REGISTER SETTING

The first register setting for frame capture command can be occurred in anywhere of frame period. But, it is recommend to do first setting at the VSYNC “L” state. VSYNC information can be read from status SFR. Refer to the below figure. All command include ImgCptEn, is valid at VSYNC falling edge. Be sure that except first SFR setting, all command should be programmed in ISR(Interrupt Service Routine). It is not allowed for target size information to be changed during capture operation. However, image mirror or rotation, windowing, and Zoom In settings are allowed to change in capturing operation. but, In case preview path select MSDMA input mode, all command should be programmed after MSDMA and Preview DMA operation end.

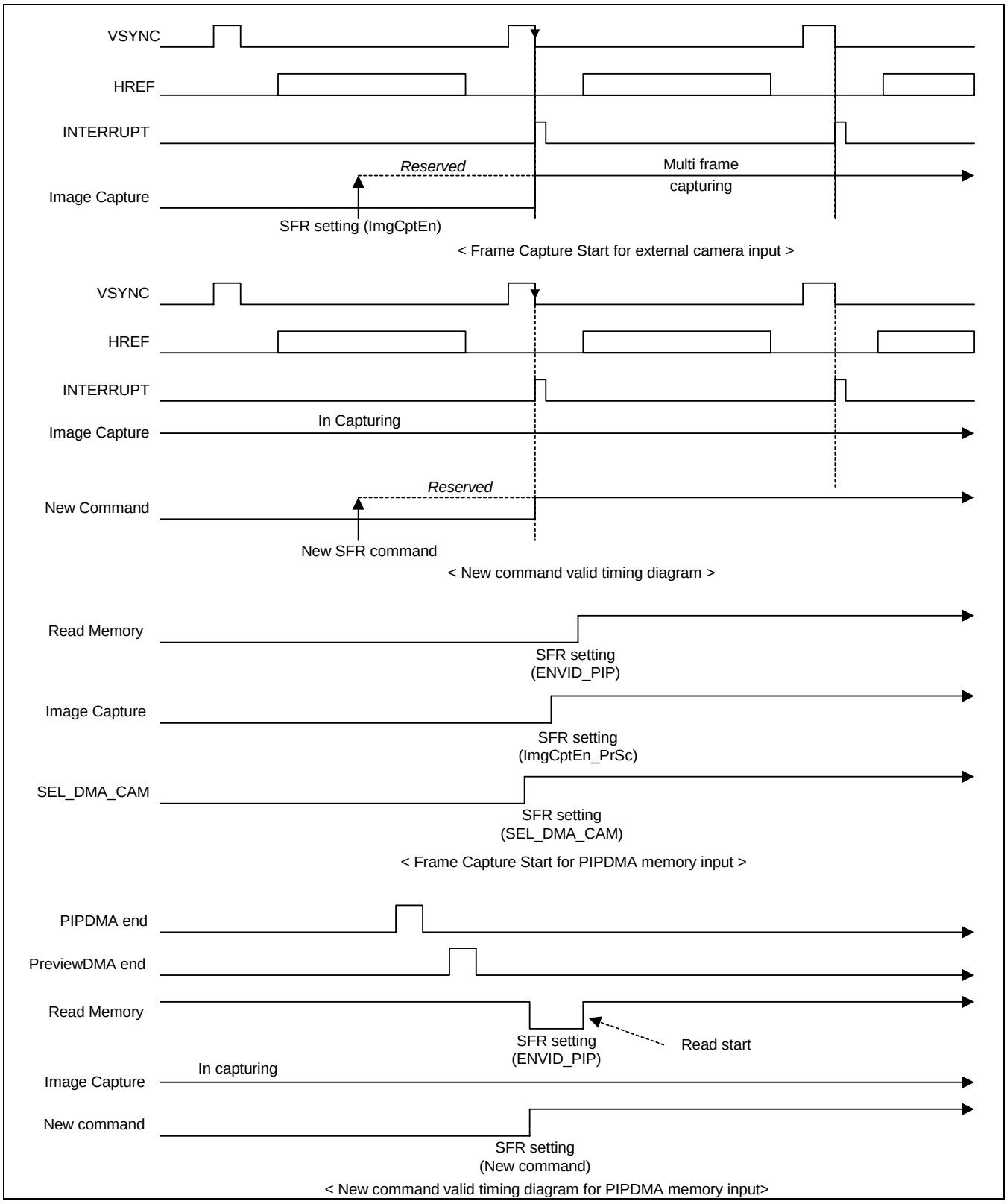
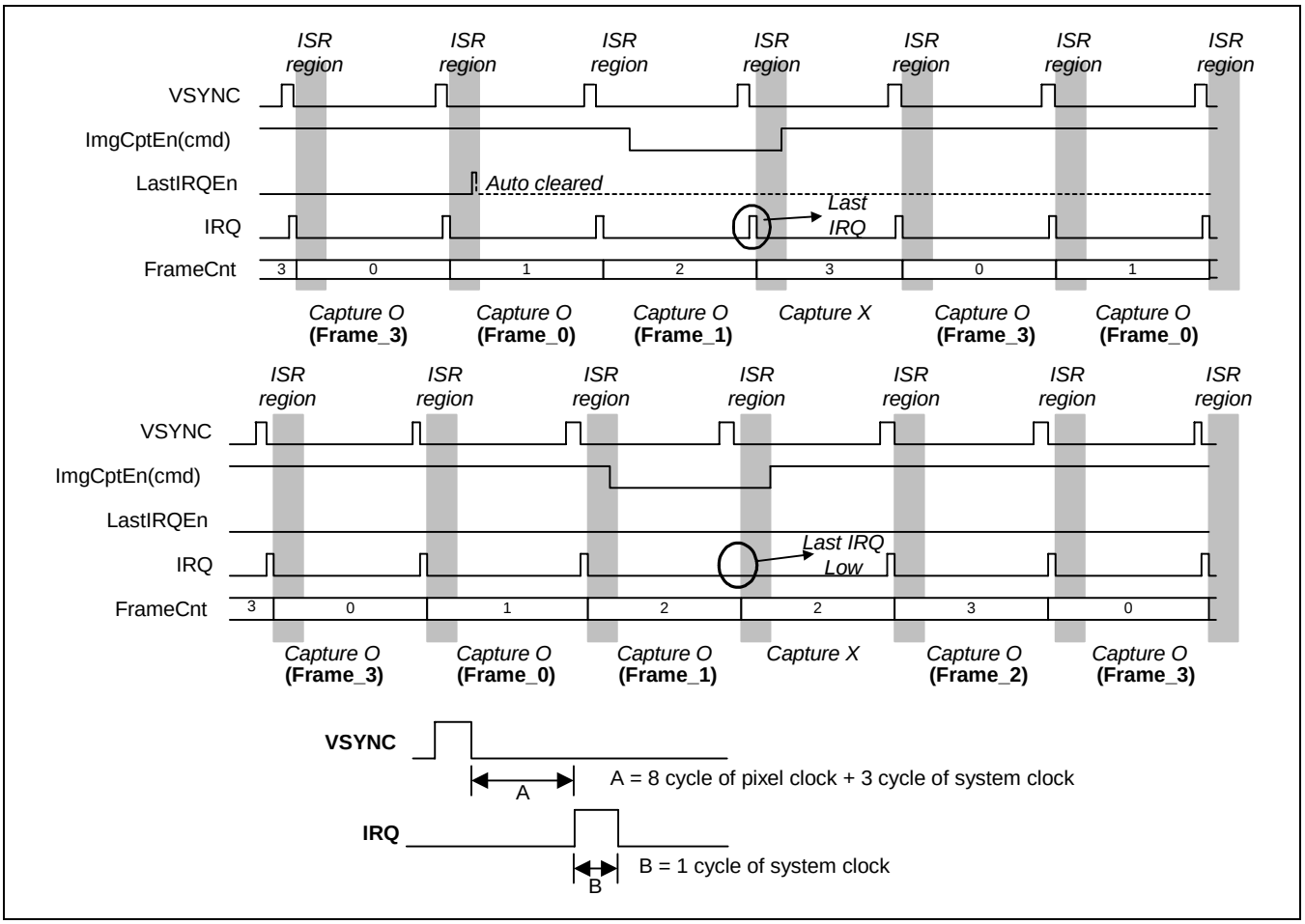


Figure 23-10. Timing diagram for register setting

Timing diagram for Last IRQ (Camera capture mode)

IRQ except LastIRQ is generated before image capturing. Last IRQ which means capture-end can be set by following timing diagram. LastIRQEn is auto-cleared and ,as mentioned, SFR setting in ISR is for next frame command. So, for adequate last IRQ, you should follow next sequence between LastIRQEn and ImgCptEn/ImgCptEn_CoSc/ImgCptEnPrSC. It is recommended that ImgCptEn/ImgCptEn_CoSc/ImgCptEnPrSC are set at same time and at last of SFR setting in ISR. FrameCnt which is read in ISR, means next frame count. On following diagram, last captured frame count is "1". That is, Frame 1 is the last-captured frame among frame 0~3. FrameCnt is increased by 1 at IRQ rising.

- Camera input capture path (applied both Preview & Codec path)



Timing diagram for IRQ (Memory data processing mode)

- MSDMA(Memory data input path) input is applied only preview path !!! when SFR SEL_DMA_CAM = '1'). Codec path doesn't care. codec path is applied a only camera capturing case. IRQ is generated after Preview DMA operation done per frame. This mode is aware of starting point by user's SFR setting (ENVID_MS '0' → '1'). so, this mode doesn't need IRQ of starting point and LastIRQ. FrameCnt is increased by 1 at ENVID_MS low to rising ('0' → '1') and ImgCptEn_PrSC '1'

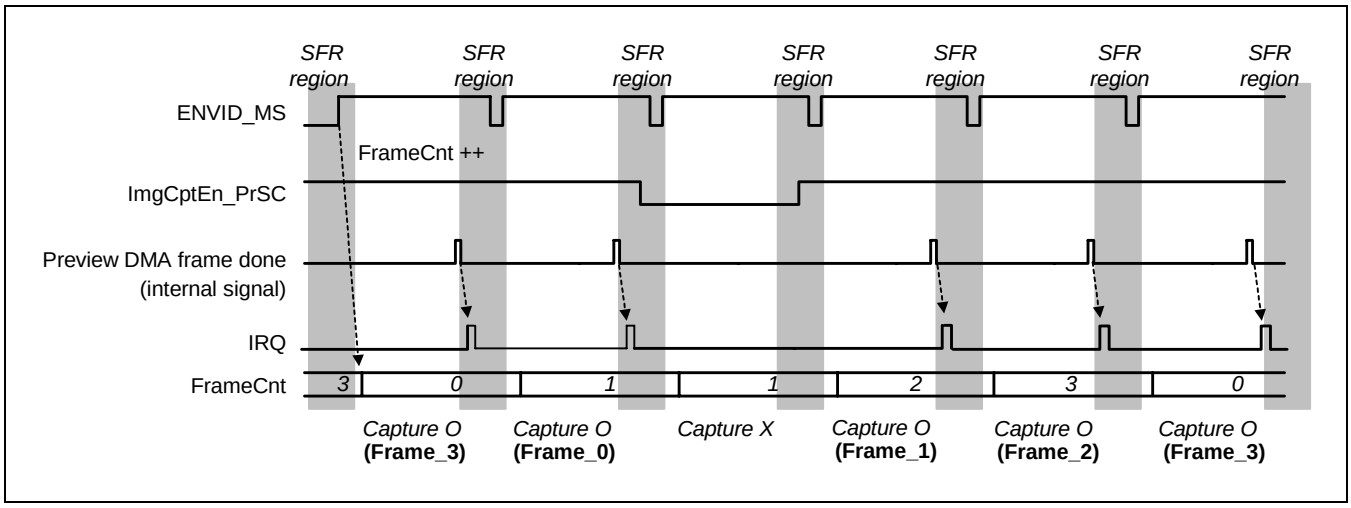


Figure 23-11. Timing diagram for last IRQ

MSDMA FEATURE

MSDMA supports memory data scaling. Camera interface has two input devices (only preview path). First is external camera. Second is Memory data. If MSDMA (reading the memory data) want to use in preview path. SFR SEL_DMA_CAM signal should be set '1'. This input path is called Memory Scaling DMA path.

NOTE: Only two image format support for MSDMA input. (= Saved memory format)

1. YCbCr 4:2:0
2. YCbCr 4:2:2 (Interleave)

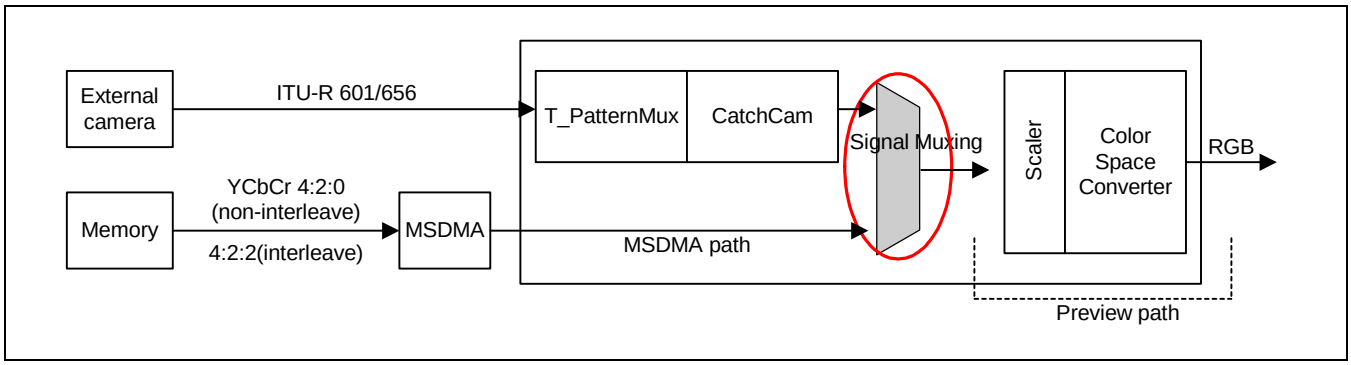


Figure 23-12. MSDMA or External Camera interface (only CAMIFpreview path)

SOFTWARE INTERFACE

CAMIF SFR (Special Function Register)

CAMERA INTERFACE SPECIAL REGISTERS

- When preview input use MSDMA path, the first column mark (v) sfr will be related to the preview operation.
- The last column means that each value can change by each VSYNC start during capture enable.
  (O : change , X : not change)

SOURCE FORMAT REGISTER

Register	Address	R/W	Description	Reset Value
CISRCFMT	0x4D80_0000	RW	Window offset register	0

CISRCFMT	Bit	Description	Initial State	Change State
ITU601_656n	[31]	1 : ITU-R BT.601 YCbCr 8-bit mode enable 0 : ITU-R BT.656 YCbCr 8-bit mode enable	0	X
UVOffset	[30]	Cb,Cr value offset control. 1 : +128 0 : +0 (normally used)	0	X
In16bit	[29]	This bit must be 0.	0	X
SourceHsize	[28:16]	Source horizontal pixel number (must be 8's multiple) (Also, must be 4's multiple of PreHorRatio if WinOfsEn is 0)	0	X
Order422	[15:14]	Input YCbCr order inform for input 8-bit mode **8-bit mode** 00 : YCbYCr 01 : YCrYCb 10 : CbYCrY 11 : CrYCbY	0	X
Reserved	[13]		0	X
SourceVsize	[12:0]	Source vertical pixel number. (Also, must be multiple of PreVerRatio when scale down if WinOfsEn is 0)	0	X

WINDOW OPTION REGISTER

Register	Address	R/W	Description	Reset Value
CIWDOFST	0x4D80_0004	RW	Window offset register	0

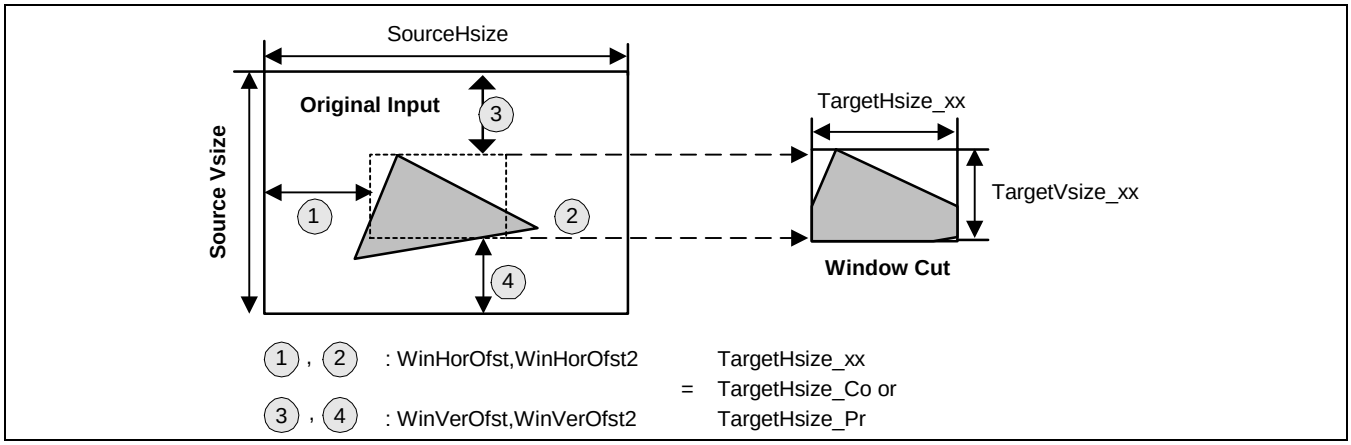


Figure 23-13. Window offset scheme
(WinHorOfst2 & WinVerOfst2 are assigned in the CIWDOFST2 register)

CIWDOFST	Bit	Description	Initial State	Change State
WinOfsEn	[31]	1: window offset enable 0: no offset	0	O
ClrOvCoFiY	[30]	1: clear the overflow indication flag of input CODEC FIFO Y 0: normal	0	X
Reserved	[29:27]		0	X
WinHorOfst	[26:16]	Window horizontal offset by pixel unit. (It should be 2's multiple) Caution: SourceHsize-WinHorOfst- WinHorOfst2 should be 8's multiple.	0	O
ClrOvCoFiCb	[15]	1: clear the overflow indication flag of input CODEC FIFO Cb 0: normal	0	X
ClrOvCoFiCr	[14]	1: clear the overflow indication flag of input CODEC FIFO Cr 0: normal	0	X
ClrOvPrFiCb	[13]	1: clear the overflow indication flag of input PREVIEW FIFO Cb 0: normal	0	X
ClrOvPrFiCr	[12]	1: clear the overflow indication flag of input PREVIEW FIFO Cr 0: normal	0	X
Reserved	[11]		0	X
WinVerOfst	[10:0]	Window vertical offset by pixel unit	0	O

NOTE: Clear bits should be set by zero after clearing the flags.
It should be as (WinHorOfst + WinHorOfst2) >= (SourceHsize – 640 * PreHorRatio_Pr)
Crop Hsize (= SourceHsize – WinHorOfst - WinHorOfst2) must be 4's multiple of PreHorRatio.

Crop Vsize (= SourceVsize – WinVerOfst - WinVerOfst2) must be multiple of PreVerRatio when scale down. and must be an even number if In422_Co = 0 and Out422_Co = 0

< Example >

Crop Hsize	Permitted Prescale_ratio	PreDstWidth_xx
8n	2	4n
16n	2 or 4	4n
32n	2, 4 or 8	4n

GLOBAL CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
CIGCTRL	0x4D80_0008	RW	Global control register	2000_0000

CIGCTRL	Bit	Description	Initial State	Change State
SwRst	[31]	Camera interface software reset. Before setting this bit, you should set the ITU601_656n bit of CISRCFMT as “1” temporarily at first SFR setting. Next sequence is recommended. (ITU601 case : ITU601_656n “1” → SwRst “1” → SwRst “0” for first SFR setting , ITU656 case : ITU601_656n “1” → SwRst “1” → SwRst “0” → ITU601_656n “0” for first SFR setting)	0	X
CamRst	[30]	External camera processor Reset or Power Down control	0	X
Reserved	[29]	Must be 1	1	X
TestPattern	[28:27]	This register should be set at only ITU-T 601 8-bit mode. Not allowed with ITU-T 656 mode. (max. 1280 X 1024) 00 : external camera processor input (normal) 01 : color bar test pattern 10 : horizontal increment test pattern 11 . vertical increment test pattern	0	X
InvPolPCLK	[26]	1 : inverse the polarity of PCLK 0 : normal	0	X
InvPolVSYNC	[25]	1 : inverse the polarity of VSYNC 0 : normal	0	X
InvPolHREF	[24]	1 : inverse the polarity of HREF 0 : normal	0	X
Non-use	[23]		0	X
IRQ_Ovfen	[22]	1 : Overflow interrupt enable (Interrupt is generated during overflow occurrence) 0 : Overflow interrupt disable (normal)	0	X
Href_mask	[21]	1 : mask out Href during Vsync high 0 : no mask	0	X
Reserved	[20:0]		0	X

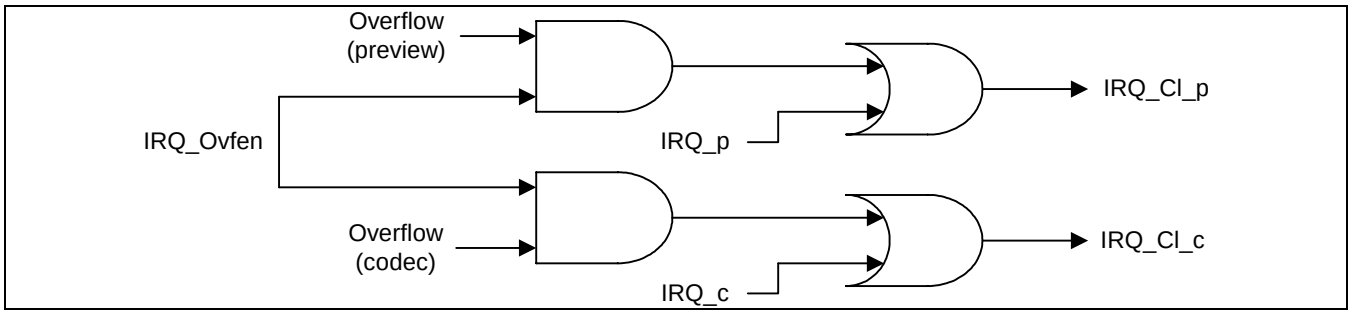


Figure 23-14 Interrupt generation scheme

WINDOW OPTION REGISTER 2

Register	Address	R/W	Description	Reset Value
CIDOWSFT2	0x4D80_0014	RW	Window option register 2	0

CIWDOFST2	Bit	Description	Initial State	Change State
Reserved	[31:27]		0	X
WinHorOfst2	[26:16]	Window horizontal offset2 by pixel unit. (It should be 2's multiple) **Caution** : SourceHsize-WinHorOfst- WinHorOfst2 should be 8's multiple.	0	O
Reserved	[15:11]		0	X
WinVerOfst2	[10:0]	Window vertical offset2 by pixel unit	0	O

Y1 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOYSA1	0x4D80_0018	RW	1st frame start address for codec DMA	0

CICOYSA1	Bit	Description	Initial State	Change State
CICOYSA1	[31:0]	Output format : YCbCr 4:2:2 or 4:2:0 → Y 1st frame start address Output format : RGB 16/24 bit → RGB 1st frame start address	0	X

Y2 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOYSA2	0x4D80_001C	RW	2nd frame start address for codec DMA	0

CICOYSA2	Bit	Description	Initial State	Change State
CICOYSA2	[31:0]	Output format : YCbCr 4:2:2 or 4:2:0 → Y 2nd frame start address Output format : RGB 16/24 bit → RGB 2nd frame start address	0	X

Y3 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOYSA3	0x4D80_0020	RW	3rd frame start address for codec DMA	0

CICOYSA3	Bit	Description	Initial State	Change State
CICOYSA3	[31:0]	Output format : YCbCr 4:2:2 or 4:2:0 → Y 3rd frame start address Output format : RGB 16/24 bit → RGB 3rd frame start address	0	X

Y4 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOYSA4	0x4D80_0024	RW	4th frame start address for codec DMA	0

CICOYSA4	Bit	Description	Initial State	Change State
CICOYSA4	[31:0]	Output format : YCbCr 4:2:2 or 4:2:0 → Y 4th frame start address Output format : RGB 16/24 bit → RGB 4th frame start address	0	X

CB1 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOCBSA1	0x4D80_0028	RW	Cb 1st frame start address for codec DMA	0

CICOCBSA1	Bit	Description	Initial State	Change State
CICOCBSA1	[31:0]	Cb 1st frame start address for codec DMA	0	X

CB2 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOCBSA2	0x4D80_002C	RW	Cb 2nd frame start address for codec DMA	0

CICOCBSA2	Bit	Description	Initial State	Change State
CICOCBSA2	[31:0]	Cb 2nd frame start address for codec DMA	0	X

CB3 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOCBSA3	0x4D80_0030	RW	Cb 3rd frame start address for codec DMA	0

CICOCBSA3	Bit	Description	Initial State	Change State
CICOCBSA3	[31:0]	Cb 3rd frame start address for codec DMA	0	X

CB4 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOCBSA4	0x4D80_0034	RW	Cb 4th frame start address for codec DMA	0

CICOCBSA4	Bit	Description	Initial State	Change State
CICOCBSA4	[31:0]	Cb 4thframe start address for codec DMA	0	X

CR1 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOCRSA1	0x4D80_0038	RW	Cr 1st frame start address for codec DMA	0

CICOCRSA1	Bit	Description	Initial State	Change State
CICOCRSA1	[31:0]	Cr 1st frame start address for codec DMA	0	X

CR2 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOCRSA2	0x4D80_003C	RW	Cr 2nd frame start address for codec DMA	0

CICOCRSA2	Bit	Description	Initial State	Change State
CICOCRSA2	[31:0]	Cr 2nd frame start address for codec DMA	0	X

CR3 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOCRSA3	0x4D80_0040	RW	Cr 3rd frame start address for codec DMA	0

CICOCRSA3	Bit	Description	Initial State	Change State
CICOCRSA3	[31:0]	Cr 3rd frame start address for codec DMA	0	X

CR4 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOCRSA4	0x4D80_0044	RW	Cr 4th frame start address for codec DMA	0

CICOCRSA4	Bit	Description	Initial State	Change State
CICOCRSA4	[31:0]	Cr 4thframe start address for codec DMA	0	X

CODEC TARGET FORMAT REGISTER

Register	Address	R/W	Description	Reset Value
CICOTRGFMT	0x4D80_0048	RW	Target image format of codec DMA	0

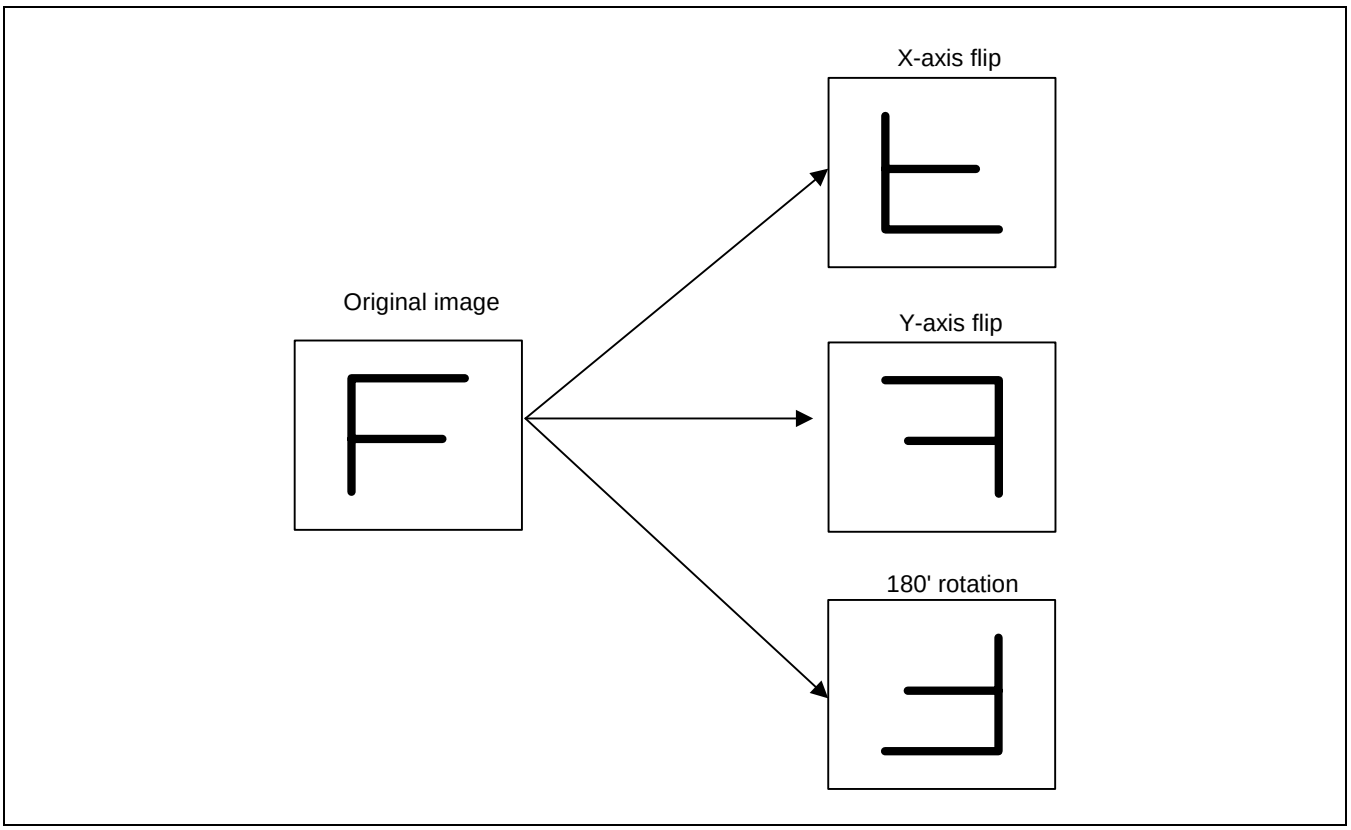


Figure 23-15. Codec image mirror and rotation

CICOTRGFMT	Bit	Description	Initial State	Change State
In422_Co	[31]	1 : YCbCr 4:2:2 codec scaler input image format. 0 : YCbCr 4:2:0 codec scaler input image format. In this case, horizontal line decimation is performed before codec scaler. (normal)	0	O
Out422_Co	[30]	1 : YCbCr 4:2:2 codec scaler output image format. This mode is mainly for S/W JPEG. 0 : YCbCr 4:2:0 codec scaler output image format. This mode is mainly for MPEG-4 codec and H/W JPEG DCT.(normal) It must not be set to 0 when In422_Co is set to 0.	0	O
Interleave_Co	[29]	1 : Interleave ON (support image format YCbCr 4:2:2 only) $Y_0Cb_0Y_1Cr_0Y_2Cb_1Y_3Cr_{1.....}$ 0 : Interleave OFF $Y_0Y_1Y_2Y_{3....}Cb_0Cb_{1....}Cr_0Cr_{1....}$	0	O
TargetHsize_Co	[28:16]	Horizontal pixel number of target image for codec DMA (16's multiple)	0	X
FlipMd_Co	[15:14]	Image mirror and rotation for codec DMA 00 : Normal 01 : X-axis mirror 10 : Y-axis mirror 11 : 180° rotation	0	O
Reserved	[13]		0	X
TargetVsize_Co	[12:0]	Vertical pixel number of target image for codec DMA(8's multiple when RGB mode is selected)	0	X

TargetHsize_Co and TargetVsize_Co should not be larger than SourceHsize and SourceVsize.

Caution! If TargetVsize_Co value is set to an odd number(N) and output format is YCbCr 4:2:0, The odd number(N) of Y lines and the (N-1)/2 of Cb, Cr lines are generated.

CODEC DMA CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
CICOCTRL	0x4D80_004C	RW	Codec DMA control related	0

CICOCTRL	Bit	Description	Initial State	Change State
Reserved	[31:24]		0	X
Yburst1_Co	[23:19]	Output format : YCbCr → Main burst length for codec Y frames Output format : RGB → Main burst length for RGB frame	0	X
Yburst2_Co	[18:14]	Output format : YCbCr → Remained burst length for codec Y frames Output format : RGB → Remained burst length for RGB frame	0	X
Cburst1_Co	[13:9]	Main burst length for codec Cb/Cr frames	0	X
Cburst2_Co	[8:4]	Remained burst length for codec Cb/Cr frames	0	X
Reserved	[3]		0	X
LastIRQEn_Co	[2]	1 : enable last IRQ at the end of frame capture (It is recommended to check the done signal of capturing image for JPEG. One pulse) 0 : normal	0	X
Order422_Co	[1:0]	Interleaved YCbCr 4:2:2 output order memory storing style 00 : $Y_0Cb_0Y_1Cr_0$ 01 : $Y_0Cr_0Y_1Cb_0$ 10 : $Cb_0Y_0Cr_0Y_1$ 11 : $Cr_0Y_0Cb_0Y_1$	0	X

- Interleaved burst length

Y burst length	2 , 4 , 8
C burst length (C burst length = Y burst length / 2)	1 , 2 , 4
Wanted burst length (= Y + 2C)	4 , 8 , 16

NOTE: When Codec output format is YCbCr 4:2:2 interleave ,ScalerBypass_Co = 0 and ScaleUp_V_Co = 1 , Wanted main burst length = 16 and Wanted remained burst length ≠ 16 is not allowed.

- Non-Interleaved burst length

Y	Main burst length = 4, 8, 16	Remained burst length = 4, 8, 16
C	Main burst length = 2, 4, 8, 16	Remained burst length = 2, 4, 8, 16

NOTE: When Interleave_Co = 1, there are some restricts in burst length setting as below.
Burst size calculations are done to determine the wanted burst length. After finding the wanted burst length.
The SFR fields are programmed as shown below,
Y : wanted Main burst length = 2 * Yburst1_Co, and wanted Remained burst length = 2 * Yburst2_Co.
Cb/Cr : wanted Main burst length = Yburst1_Co / 2 = Cburst1_Co, and wanted Remained burst length = Yburst2_Co / 2 = Cburst2_Co

Example 1. Target image size : QCIF (horizontal Y width = 176 pixels. 1 pixel = 1 Byte. 1 word = 4 pixel)
176 / 4 = 44 words , 44 % 8 = 4 → main burst = 8, remained burst = 4
If Interleave_Co = 1 and YCbCr = 4:2:2
176 x (1 word / 2 pixles) = 88 words , 88 % 16 = 8 → Wanted main burst = 16, Wanted remained burst = 8
Wanted main burst = 16 = 2 * Yburst1 = 4 * Cburst1, Wanted remained burst = 8 = 2 * Yburst2 = 4 * Cburst2
Yburst1_Co = 8, Yburst2_Co = 4

Example 2. Target image size : VGA (horizontal Y width = 640 pixels. 1 pixel = 1 Byte. 1 word = 4 pixel)
640 / 8 = 80 word , 160 % 8 = 0 → main burst = 8, remained burst = 8
If Interleave_Co = 1 , RGB565 mode
640 x (1 word / 2 pixel) = 320 words , 320 % 16 = 0 → Wanted main burst = 16, Wanted remained burst = 16
Yburst1_Co = 8, Yburst2_Co = 8
If Interleave_Co = 1 , RGB888 mode
640 x (1 word / 1 pixels) = 640 words, 640 % 16 = 0 → Wanted main burst = 16, Wanted remained burst = 16
Yburst1_Co = 8, Yburst2_Co = 8

Caution! CAMIF generate INCR (HBURST of AMBA) transfer type at abnormal burst length as 2, and at crossing 1024 address boundary by burst transfer. System controller including CAMIF, must support to treat INCR burst as several single transfer accesses. Watch over your memory controller and system arbiter specification!

REGISTER SETTING GUIDE FOR CODEC SCALER AND PREVIEW SCALER

SRC_Width and DST_Width satisfy the word boundary constraints such that the number of horizontal pixel can be represented to kn where n = 1,2,3, … and k = 1 / 2 / 8 for 24bppRGB / 16bppRGB / YCbCr420 image, respectively. TargetHsize should not be larger than SourceHsize. Similarly, TargetVsize should not be larger than SourceVsize.

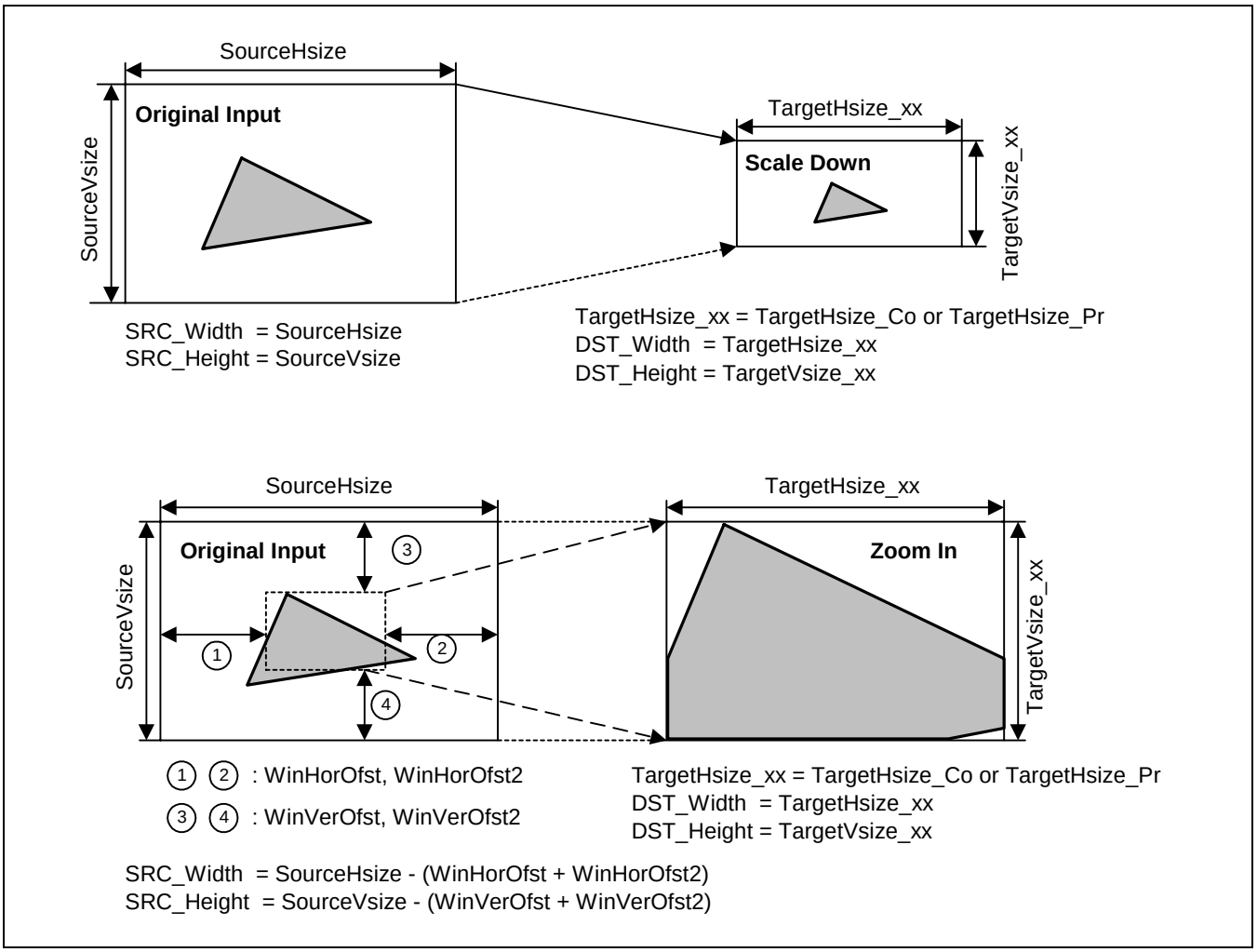


Figure 23-16. Scaling scheme

The other control registers of pre-scaled image size, pre-scale ratio, pre-scale shift ratio and main scale ratio are defined according to the following equations.

If (SRC_Width >= 64 × DST_Width) { Exit(-1); /* Out Of Horizontal Scale Range */ }

else if (SRC_Width >= 32 × DST_Width) { PreHorRatio_xx = 32; H_Shift = 5; }

else if (SRC_Width >= 16 × DST_Width) { PreHorRatio_xx = 16; H_Shift = 4; }

else if (SRC_Width >= 8 × DST_Width) { PreHorRatio_xx = 8; H_Shift = 3; }

else if (SRC_Width >= 4 × DST_Width) { PreHorRatio_xx = 4; H_Shift = 2; }

else if (SRC_Width >= 2 × DST_Width) { PreHorRatio_xx = 2; H_Shift = 1; }

else { PreHorRatio_xx = 1; H_Shift = 0; }

PreDstWidth_xx = SRC_Width / PreHorRatio_xx;

MainHorRatio_xx = (SRC_Width << 8) / (DST_Width << H_Shift);

```
If ( SRC_Height >= 64 × DST_Height ) {  Exit(-1);  /* Out Of Vertical Scale Range */  }
else if (SRC_Height >= 32 × DST_Height) { PreVerRatio_xx = 32;  V_Shift = 5; }
else if (SRC_Height >= 16 × DST_Height) { PreVerRatio_xx = 16;  V_Shift = 4; }
else if (SRC_Height >= 8 × DST_Height) { PreVerRatio_xx = 8;  V_Shift = 3; }
else if (SRC_Height >= 4 × DST_Height) { PreVerRatio_xx = 4;  V_Shift = 2; }
else if (SRC_Height >= 2 × DST_Height) { PreVerRatio_xx = 2;  V_Shift = 1; }
else { PreVerRatio_xx = 1;  V_Shift = 0; }
PreDstHeight_xx = SRC_Height / PreVerRatio_xx;
MainVerRatio_xx = ( SRC_Height << 8 ) / ( DST_Height << V_Shift);

SHfactor_xx = 10 – ( H_Shit + V_Shift);
```

Caution! In preview path, Pre-scaled H_width must be the less than 640. (The maximum size of preview path scaler's horizontal line buffer is 640.)

Example 1. Source image horizontal size : SRC_Width = 1280, Target image horizontal size : DST_Width = 480

(SRC_Width >= 2 × DST_Width) -> PreHorRatio_xx = 2

PreDstWidth_xx = SRC_Width / PreHorRatio_xx = 1280/2 = 640

PreDstWidth_xx = 640 <= 640(The maximum size of preview path scaler's horizontal line buffer)

Scaling is success.

Example 2. Source image horizontal size : SRC_Width = 720, Target image horizontal size : DST_Width = 480

(SRC_Width < 2 × DST_Width) PreHorRatio_xx = 1

PreDstWidth_xx = SRC_Width / PreHorRatio_xx = 720/1 = 720

PreDstWidth_xx = 720 > 640(The maximum size of preview path scaler's horizontal line buffer)

Scaling is failed.

Caution! In Zoom-In case, you should check the next equation.

((SourceHsize - (WinHorOfst + WinHorOfst2)) / PreHorRatio_Pr) <= 640

Caution! In preview memory data input path, you should not use Zoom-In, crop and image effect function.

(External camera input path use Zoom-In , crop and image effect function)

CODEC PRE-SCALER CONTROL REGISTER 1

Register	Address	R/W	Description	Reset Value
CICOSCPRERATIO	0x4D80_0050	RW	Codec pre-scaler ratio control	0

CICOSCPRERATIO	Bit	Description	Initial State	Change State
SHfactor_Co	[31:28]	Shift factor for codec pre-scaler	0	O
Reserved	[27:23]		0	X
PreHorRatio_Co	[22:16]	Horizontal ratio of codec pre-scaler	0	O
Reserved	[15:7]		0	X
PreVerRatio_Co	[6:0]	Vertical ratio of codec pre-scaler	0	O

CODEC PRE-SCALER CONTROL REGISTER 2

Register	Address	R/W	Description	Reset Value
CICOSCPREDST	0x4D80_0054	RW	Codec pre-scaler destination format	0

CICOSCPREDST	Bit	Description	Initial State	Change State
Reserved	[31:28]		0	X
PreDstWidth_Co	[27:16]	Destination width for codec pre-scaler	0	O
Reserved	[15:12]		0	X
Reserved	[31:28]		0	X
PreDstHeight_Co	[11:0]	Destination height for codec pre-scaler	0	O

CODEC MAIN-SCALER CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
CICOSCCTRL	0x4D80_0058	RW	Codec main-scaler control	0

CICOSCCTRL	Bit	Description	Initial State	Change State
ScalerBypass_Co	[31]	Codec scaler bypass for upper 2048 x 2048 size (In this case, ImgCptEn_CoSC and ImgCptEn_PrSC should be 0, but ImgCptEn should be 1. It is not allowed to capturing preview image. This mode is intended to capture JPEG input image for DSC application) In this case, input pixel buffering depends on only input FIFOs, so system bus should be not busy in this mode.	0	O
ScaleUp_H_Co	[30]	Horizontal scale up/down flag for codec scaler (In 1:1 scale ratio, this bit should be “1”) 1: up, 0:down	0	O
ScaleUp_V_Co	[29]	Vertical scale up/down flag for codec scaler (In 1:1 scale ratio, this bit should be “1”) 1: up, 0:down	0	O
Reserved	[28:25]		0	X
MainHorRatio_Co	[24:16]	Horizontal scale ratio for codec main-scaler	0	O
CoScalerStart	[15]	Codec scaler start	0	O
Reserved	[14:9]		0	X
MainVerRatio_Co	[8:0]	Vertical scale ratio for codec main-scaler	0	O

CODEC DMA TARGET AREA REGISTER

Register	Address	R/W	Description	Reset Value
CICOTAREA	0x4D80_005C	RW	Codec pre-scaler destination format	0

CICOTAREA	Bit	Description	Initial State	Change State
Reserved	[31:26]		0	X
CICOTAREA	[25:0]	Target area for codec DMA = Target H size x Target V size	0	X

CODEC STATUS REGISTER

Register	Address	R/W	Description	Reset Value
CICOSTATUS	0x4D80_0064	R	Codec path status	0

CICOSTATUS	Bit	Description	Initial State	Change State
OvFiY_Co	[31]	Overflow state of codec FIFO Y	0	X
OvFiCb_Co	[30]	Overflow state of codec FIFO Cb	0	X
OvFiCr_Co	[29]	Overflow state of codec FIFO Cr	0	X
VSYNC	[28]	Camera VSYNC (This bit can be referred by CPU for first SFR setting after external camera muxing. And, it can be seen in the ITU-R BT 656 mode)	0	X
FrameCnt_Co	[27:26]	Frame count of codec DMA (This counter value means the next frame number)	0	X
WinOfstEn_Co	[25]	Window offset enable status	0	X
FlipMd_Co	[24:23]	Flip mode of codec DMA	0	X
ImgCptEn_ CamIf	[22]	Image capture enable of camera interface	0	X
ImgCptEn_ CoSC	[21]	Image capture enable of codec path	0	X
VSYNC_A	[20]	External camera A VSYNC (polarity inversion was not adopted.)	X	X
VSYNC_B	[19]	External camera B VSYNC (polarity inversion was not adopted.)	X	X
Reserved	[18:0]		0	X

RGB1 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CIPRCLRSA1	0x4D80_006C	RW	RGB 1st frame start address for preview DMA	0

CIPRCLRSA1	Bit	Description	Initial State	Change State
CIPRCLRSA1 (v)	[31:0]	RGB 1st frame start address for preview DMA	0	X

RGB2 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CIPRCLRSA2	0x4D80_0070	RW	RGB 2nd frame start address for preview DMA	0

CIPRCLRSA2	Bit	Description	Initial State	Change State
CIPRCLRSA2 (v)	[31:0]	RGB 2nd frame start address for preview DMA	0	X

RGB3 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CIPRCLRSA3	0x4D80_0074	RW	RGB 3rd frame start address for preview DMA	0

CIPRCLRSA3	Bit	Description	Initial State	Change State
CIPRCLRSA3 (v)	[31:0]	RGB 3rd frame start address for preview DMA	0	X

RGB4 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CIPRCLRSA4	0x4D80_0078	RW	RGB 4th frame start address for preview DMA	0

CIPRCLRSA4	Bit	Description	Initial State	Change State
CIPRCLRSA4 (v)	[31:0]	RGB 4th frame start address for preview DMA	0	X

PREVIEW TARGET FORMAT REGISTER

Register	Address	R/W	Description	Reset Value
CIPRTRGFMT	0x4D80_007C	RW	Target image format of preview DMA	1000_0000

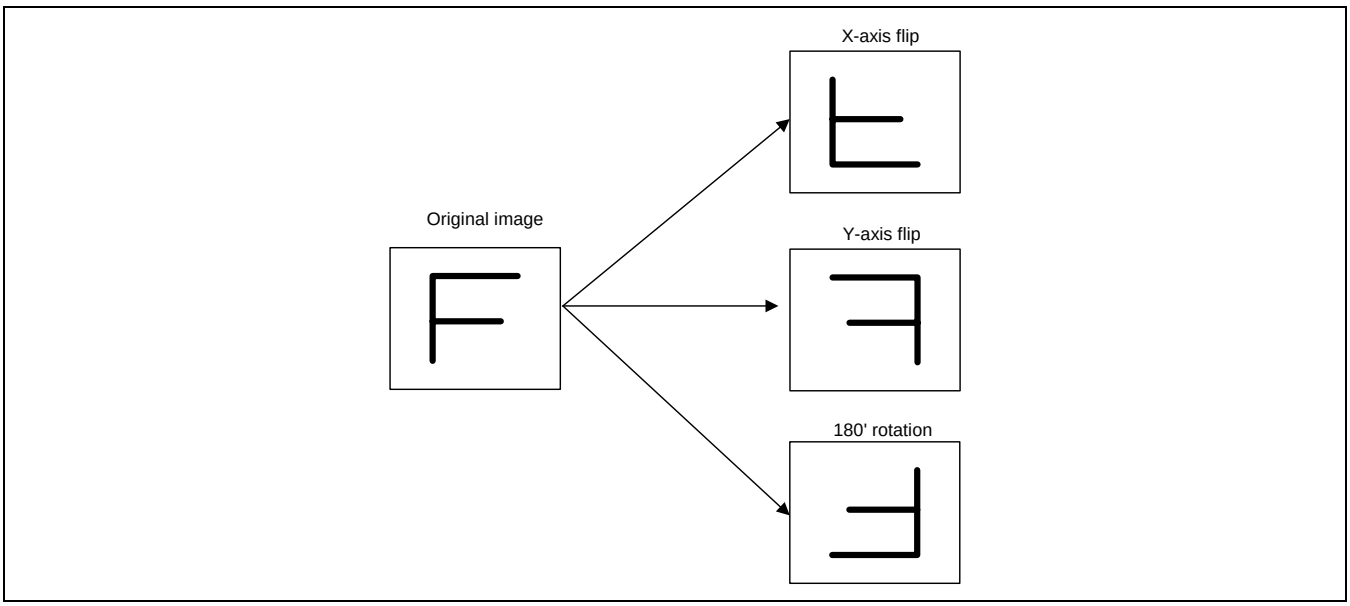


Figure 23-17. Preview image mirror and rotation

CIPRTRGFMT	Bit	Description	Initial State	Change State
CSCRange (v)	[31:30]	YCbCr Input Data Dynamic Range Selection for the Color Space Conversion 2'b11 : Forbidden 2'b10 : 0 < Y/Cb/Cr <255 (Recommended) 2'b01 : 16 <= Y <= 235, 16 <= Cb/Cr <= 240 2'b00 : Reserved	2'b10	O
Reserved	[29]		0	X
TargetHsize_Pr (v)	[28:16]	Horizontal pixel number of target image for preview DMA 16bppRGB:4n(n=1,2,3,…) 24bpp RGB : 2n(n=1,2,3, …)	0	X
FlipMd_Pr (v)	[15:14]	Image mirror and rotation for preview DMA 00 : normal 01 : x-axis mirror 10 : y-axis mirror 11 : 180° rotation	0	O
Reserved	[13]		0	X
TargetVsize_Pr (v)	[12:0]	Vertical pixel number of target image for preview DMA (8's multiple)	0	X

TargetHsize_Pr and TargetVsize_Pr should not be larger than SourceHsize and SourceVsize.

PREVIEW DMA CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
CIPRCTRL	0x4D80_0080	RW	Preview DMA control related	0

CIPRCTRL	Bit	Description	Initial State	Change State
Reserved	[31:24]		0	X
RGBburst1_Pr (v)	[23:19]	Main burst length for preview RGB frames	0	X
RGBburst2_Pr (v)	[18:14]	Remained burst length for preview RGB frames	0	X
Reserved	[13:3]		0	X
LastIRQEn_Pr (v)	[2]	1 : enable last IRQ at the end of frame capture (One pulse) 0 : normal	0	X
Reserved	[1:0]		0	X

Main burst lengths must be one of the 4,8,16 and Remained burst lengths must be one of the 2,4,8,16.

Example 1. Target image size : QCIF for RGB 32-bit format (horizontal width = 176 pixels. 1 pixel = 1 word)

176 pixel = 176 word.

176 % 16 = 0 → main burst = 16, remained burst = 16

Example 2. Target image size : VGA for RGB 16-bit format (horizontal width = 640 pixels. 2 pixel = 1 word)

640 / 2 = 320 word.

320 % 16 = 0 → main burst = 16, remained burst = 16

PREVIEW PRE-SCALER CONTROL REGISTER 1

Register	Address	R/W	Description	Reset Value
CIPRSCPRERATIO	0x4D80_0084	RW	Preview pre-scaler ratio control	0

CIPRSC PRERATIO	Bit	Description	Initial State	Change State
SHfactor_Pr (v)	[31:28]	Shift factor for preview pre-scaler	0	O
Reserved	[27:23]		0	X
PreHorRatio_Pr (v)	[22:16]	Horizontal ratio of preview pre-scaler	0	O
Reserved	[15:7]		0	X
PreVerRatio_Pr (v)	[6:0]	Vertical ratio of preview pre-scaler	0	O

PREVIEW PRE-SCALER CONTROL REGISTER 2

Register	Address	R/W	Description	Reset Value
CIPRSC PREDST	0x4D80_0088	RW	Preview pre-scaler destination format	0

CIPRSC PREDST	Bit	Description	Initial State	Change State
Reserved	[31:28]		0	X
PreDstWidth_Pr (v)	[27:16]	Destination width for preview pre-scaler	0	O
Reserved	[15:12]		0	X
PreDstHeight_Pr (v)	[11:0]	Destination height for preview pre-scaler	0	O

PREVIEW MAIN-SCALER CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
CIPRSCCTRL	0x4D80_008C	RW	Preview main-scaler control	0

CIPRSCCTRL	Bit	Description	Initial State	Change State
Sample_Pr (v)	[31]	Sampling method for format conversion. (normally 1)	0	O
RGBformat_Pr (v)	[30]	1 : 24-bit RGB , 0 : 16-bit RGB	0	O
ScaleUp_H_Pr (v)	[29]	Horizontal scale up/down flag for preview scaler (In 1:1 scale ratio, this bit should be “1”) 1: up, 0:down	0	O
ScaleUp_V_Pr (v)	[28]	Vertical scale up/down flag for preview scaler (In 1:1 scale ratio, this bit should be “1”) 1: up, 0:down	0	O
Reserved	[27:25]		0	X
MainHorRatio_Pr (v)	[24:16]	Horizontal scale ratio for preview main-scaler	0	O
PrScalerStart (v)	[15]	Preview scaler start	0	O
Reserved	[14:9]		0	X
MainVerRatio_Pr (v)	[8:0]	Vertical scale ratio for preview main-scaler	0	O

PREVIEW DMA TARGET AREA REGISTER

Register	Address	R/W	Description	Reset Value
CIPRTAREA	0x4D80_0090	RW	Preview pre-scaler destination format	0

CIPRTAREA	Bit	Description	Initial State	Change State
Reserved	[31:26]		0	X
CIPRTAREA (v)	[25:0]	Target area for preview DMA = Target H size x Target V size	0	X

PREVIEW STATUS REGISTER

Register	Address	R/W	Description	Reset Value
CIPRSTATUS	0x4D80_0098	R	Preview path status	0

CIPRSTATUS	Bit	Description	Initial State	Change State
OvFiCb_Pr	[31]	Overflow state of preview FIFO Cb	0	X
OvFiCr_Pr	[30]	Overflow state of preview FIFO Cr	0	X
Reserved	[29:28]		0	X
FrameCnt_Pr	[27:26]	Frame count of preview DMA	0	X
Reserved	[25]		0	X
FlipMd_Pr	[24:23]	Flip mode of preview DMA	0	X
Reserved	[22]		0	X
ImgCptEn_ PrSC	[21]	Image capture enable of preview path	0	X
Reserved	[20:0]		0	X

IMAGE CAPTURE ENABLE REGISTER

Register	Address	R/W	Description	Reset Value
CIIMGCPT	0x4D80_00A0	RW	Image capture enable command	0

CIIMGCPT	Bit	Description	Initial State	Change State
ImgCptEn	[31]	camera interface global capture enable	0	O
ImgCptEn_ CoSc	[30]	capture enable for codec scaler. This bit must be zero in scaler-bypass mode.	0	O
ImgCptEn_ PrSc (v)	[29]	capture enable for preview scaler. (applied both Memory data input path and External camera path in using preview) This bit must be zero in scaler-bypass mode.	0	O
Reserved	[28:27]		0	X
Cpt_CoDMA_ Sel	[26]	Codec DMA output format 1 : RGB 16/24 bit (Must be Out422_Co=1 , Interleave_Co=1) 0 : YCbCr 4:2:2 or 4:2:0	0	O
Cpt_CoDMA_ RGBFMT	[25]	Codec DMA RGB format 1 : RGB 24-bit 0 : RGB 16-bit	0	O
Cpt_CoDMA_ En	[24]	Capture codec dma frame control. It is also used for start signal of Codec image capture. Therefore, it must be set to ‘1’ if codec image is wanted. or it must be set to ‘0’ if codec image is not captured. 1 : Enable 0 : Disable	0	X
Cpt_CoDMA_ Ptr	[23:19]	Capture sequence turn-around pointer	0	X
Cpt_CoDMA_ Mod	[18]	Capture codec dma mode 1 : Apply Cpt_CoDMA_Cnt mode (capture Cpt_CoDMA_Cnt frames along the Cpt_CoDMA_Seq after Cpt_CoDMA_En becomes high) 0 : Apply Cpt_CoDMA_En mode (capture frames along the Cpt_CoDMA_Seq during Cpt_CoDMA_En is high)	0	X
Cpt_CoDMA_ Cnt	[17:10]	Wanted number of frames to be captured (when read, you will see the value of a shadow register which is downcounted when a frame is captured. That is, Cpt_CoDMA_Cnt has an initially loaded value still after a frame is captured.)	0	X
Reserved	[9:0]		0	X

CODEC CAPTURE SEQUENCE REGISTER

Register	Address	R/W	Description	Reset Value
CICOCPTSEQ	0x4D80_00A4	RW	Codec dma capture sequence related	0

CICOCPTSEQ	Bit	Description	Initial State
Cpt_CoDMA_Seq	[31:0]	Capture sequence pattern in Codec DMA	FFFF_FFFF

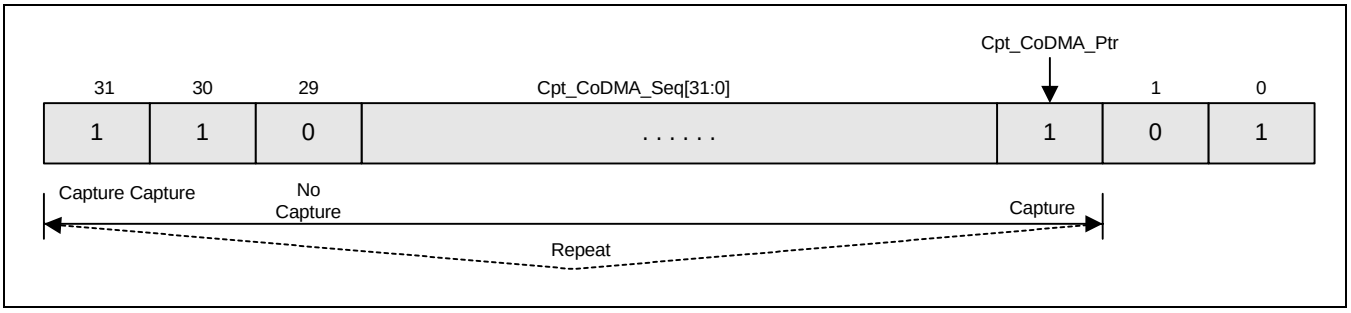


Figure 23-18 Capture codec dma frame control

- For skipped frmes, IRQ_CI_c is not generated. And FrameCnt_co is not increased

CODEC SCAN LINE OFFSET REGISTER

Register	Address	R/W	Description	Reset Value
CICOSCOS	0x4D80_00A8	RW	Codec scan line offset related	0

CICOSCOS	Bit	Description	Initial State	Change State
Reserved	[31:29]		0	X
Initial_offset_Co	[28:16]	The number of the skipped pixels for initial offset (should be even number for word boundary alignment). This value must be set to 0 when scanline offset is not used. And, scanline offset can be used only when Interleave_Co is set to 1.	0	O
Reserved	[15:13]		0	X
Line_offset_Co	[12:0]	The number of the skipped pixels in the screen of the target image when scan line is changed (should be even number for word boundary alignment). This value must be set to 0 when scanline offset is not used. And, scanline offset can be used only when Interleave_Co is set to 1.	0	O

- Scan line offset is allowed only when the output pixel format of codec path is Interleaved YCbCr422.

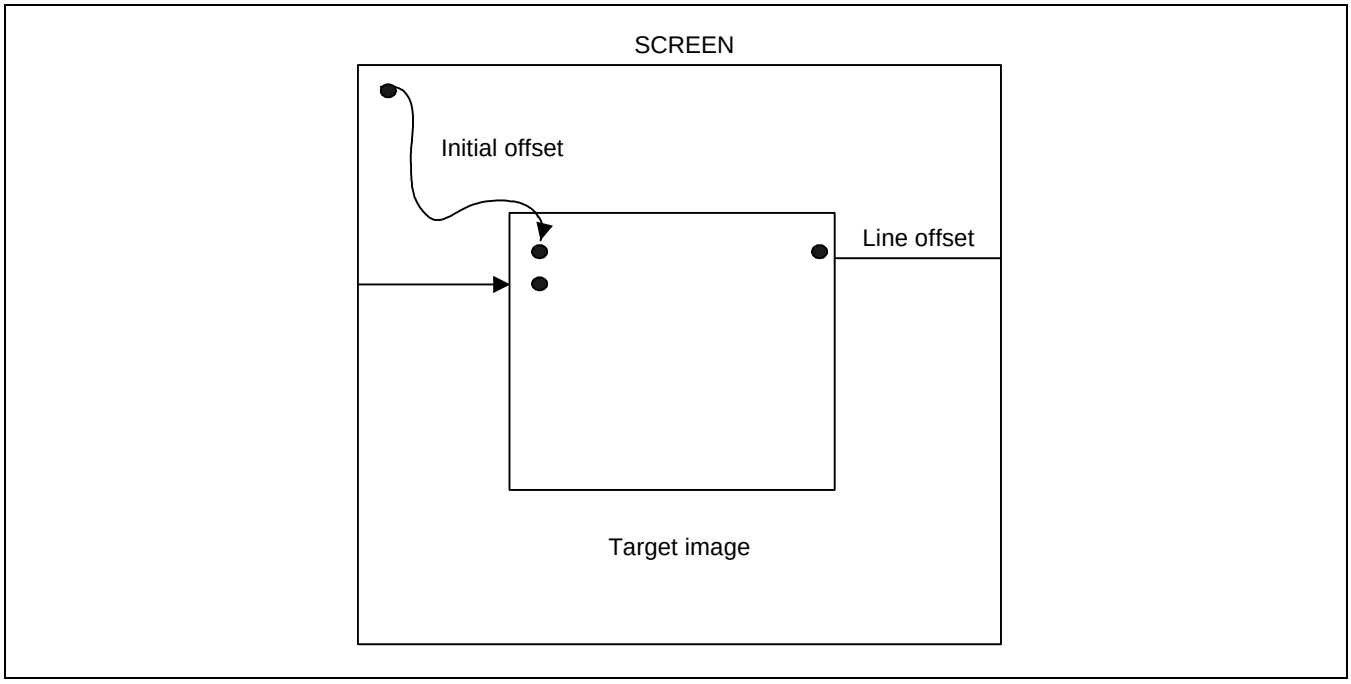


Figure 23-19. Scan line offset

IMAGE EFFECTS REGISTER

Register	Address	R/W	Description	Reset Value
CIIMGEFF	0x4D80_00B0	RW	Image Effects related	0010_0080

CIIMGEFF	Bit	Description	Initial State	Change State
Reserved	[31:29]		0	X
FIN	[28:26]	Image Effect selection 3'b000 : Bypass 3'b001 : Arbitrary Cb/Cr 3'b010 : Negative 3'b011 : Art Freeze 3'b100 : Embossing 3'b101 : Silhouette	0	O
Reserved	[25:21]		0	X
PAT_Cb	[20:13]	It is used only for FIN is Arbitrary Cb/Cr (PAT_Cb/Cr == 8'd128 for GRAYSCALE) 16 ≤ PAT_Cb ≤ 223	8'd128	O
Reserved	[12:8]		0	X
PAT_Cr	[7:0]	It is used only for FIN is Arbitrary Cb/Cr (PAT_Cb/Cr == 8'd128 for GRAYSCALE) 16 ≤ PAT_Cr ≤ 223	8'd128	O

Cf) sepia : PAT_Cb == 8'd115 , PAT_Cr == 8'd145

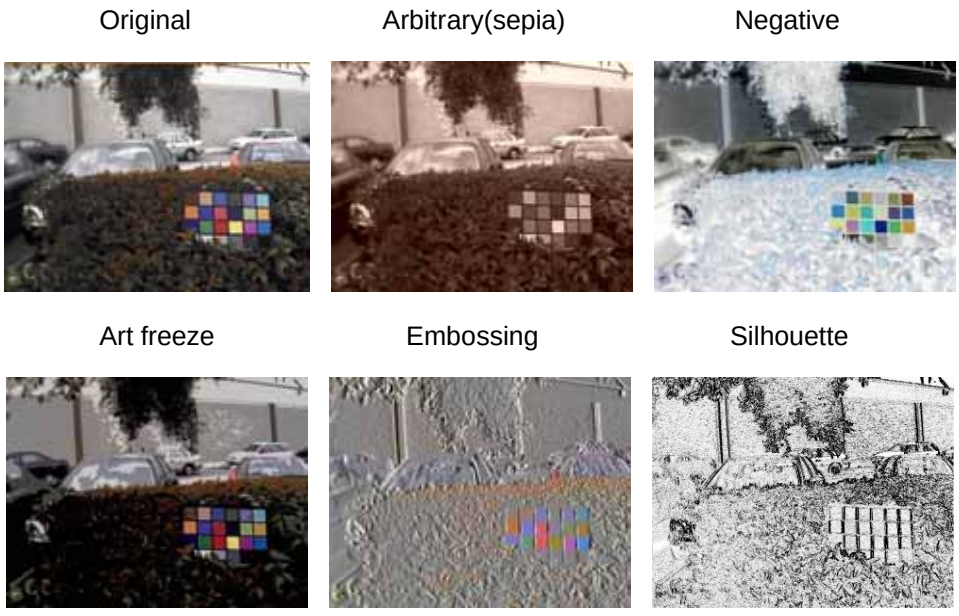


Figure 23-20. Image effect result

MSDMA Y START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CIMSYSA	0x4D80_00B4	RW	MSDMA Y start address related	0000_0000

CIMSYSA	Bit	Description	Initial State	Change State
Reserved	[31]		0	X
CIMSYSA (v)	[30:0]	DMA start address for Y component (YCbCr 4:2:0) DMA start address for YCbCr component (interleave 4:2:2)	0	X

MSDMA CB START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CIMSCBSA	0x4D80_00B8	RW	MSDMA Cb start address related	0000_0000

CIMSCBSA	Bit	Description	Initial State	Change State
Reserved	[31]		0	X
CIMSCBSA (v)	[30:0]	DMA start address for Cb component (YCbCr 4:2:0)	0	X

MSDMA CR START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CIMSCRSA	0x4D80_00BC	RW	MSDMA Cr start address related	0000_0000

CIMSCRSA	Bit	Description	Initial State	Change State
Reserved	[31]		0	X
CIMSCRSA (v)	[30:0]	DMA start address for Cr component (YCbCr 4:2:0)	0	X

MSDMA Y END ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CIMSYEND	0x4D80_00C0	RW	MSDMA Y end address related	0000_0000

CIMSYEND	Bit	Description	Initial State	Change State
Reserved	[31]		0	X
CIMSYEND (v)	[30:0]	DMA End address for Y component (YCbCr 4:2:0) DMA End address for YCbCr component (interleave 4:2:2)	0	X

MSDMA CB END ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CIMSCBEND	0x4D80_00C4	RW	MSDMA Cb end address related	0000_0000

CIMSCBEND	Bit	Description	Initial State	Change State
Reserved	[31]		0	X
CIMSCBEND (v)	[30:0]	DMA End address for Cb component (YCbCr 4:2:0)	0	X

MSDMA CR END ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CIMSCREND	0x4D80_00C8	RW	MSDMA Cr end address related	0000_0000

CIMSCREND	Bit	Description	Initial State	Change State
Reserved	[31]		0	X
CIMSCREND (v)	[30:0]	DMA End address for Cr component (YCbCr 4:2:0)	0	X

MSDMA Y OFFSET REGISTER

Register	Address	R/W	Description	Reset Value
CIMSYOFF	0x4D80_00CC	RW	MSDMA Y offset related	0000_0000

CIMSYOFF	Bit	Description	Initial State	Change State
Reserved	[31:24]		0	X
CIMSYOFF (v)	[23:0]	Offset of Y component for fetching source image	0	X

MSDMA CB OFFSET REGISTER

Register	Address	R/W	Description	Reset Value
CIMSCBOFF	0x4D80_00D0	RW	MSDMA Cb offset related	0000_0000

CIMSCBOFF	Bit	Description	Initial State	Change State
Reserved	[31:24]		0	X
CIMSCBOFF (v)	[23:0]	Offset of Cb component for fetching source image	0	X

MSDMA CR OFFSET REGISTER

Register	Address	R/W	Description	Reset Value
CIMSCROFF	0x4D80_00D4	RW	MSDMA Cr offset related	0000_0000

CIMSCROFF	Bit	Description	Initial State	Change State
Reserved	[31:24]		0	X
CIMSCROFF (v)	[23:0]	Offset of Cr component for fetching source image	0	X

MSDMA SOURCE IMAGE WIDTH REGISTER

Register	Address	R/W	Description	Reset Value
CIMSWIDTH	0x4D80_00D8	RW	MSDMA source image width related	0000_0000

CIMSWIDTH	Bit	Description	Initial State	Change State
Reserved	[31:12]		0	X
CIMSWIDTH (v)	[11:0]	MSDMA source Image Horizontal pixel size	0	X

- MSDMA Start address

Start address of ADDRStart_Y/Cb/Cr points the first word address where the corresponding component of Y/Cb/Cr is read. Each one should be aligned with word boundary (i.e. ADDRStart_X[1:0] = 00). ADDRStart_Cb and ADDRStart_Cr are valid only for the YCbCr420 source image format.

- MSDMA End address

1) ADDREnd_Y

= ADDRStart_Y + Memory size for the component of Y

= ADDRStart_Y + (SRC_Width × SRC_Height) × ByteSize_Per_Pixel + Offset_Y × (SRC_Height-1)

2) ADDREnd_Cb (Valid for YCbCr420 source format)

= ADDRStart_Cb + Memory size for the component of Cb

= ADDRStart_Cb + (SRC_Width/2 × SRC_Height/2) × ByteSize_Per_Pixel + Offset_Cb × (SRC_Height/2-1)

3) ADDREnd_ Cr (Valid for YCbCr420 source format)

= ADDRStart_ Cr + Memory size for the component of Cr

= ADDRStart_Cr + (SRC_Width/2 × SRC_Height/2) × ByteSize_Per_Pixel + Offset_Cr × (SRC_Height/2-1)

- MSDMA OFFSET

1) Offset_Y/Cb/Cr

= Memory size for offset per a horizontal line

= Number of pixel (or sample) in horizontal offset × ByteSize_Per_Pixel (or Sample)

Cf.) ByteSize_Per_Pixel = { 1 for YCbCr420
2 for YCbCr422 (interleave)

MSDMA CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
CIMSCTRL	0x4D80_00DC	RW	MSDMA control register	0000_0000

CIMSCTRL	Bit	Description	Initial State	Change State
Reserved	[31:7]		0	X
EOF_MS	[6]	MSDMA read the saved memory data. When this operation done, EOF will be generated. (read only)	0	X
Interleave_MS (v)	[5]	0 : Non-Interleaved format (Each component of Y, Cb and Cr is access by the word). 1 : Interleaved format (All components of Y, Cb and Cr are mixed inside single word).	0	X
Order422_MS (v)	[4:3]	When source MSDMA image is interleaved YCbCr 4:2:2, Interleaved YCbCr 4:2:2 input memory storing style. [4:3] LSB MSB 00 $Y_0Cb_0Y_1Cr_0$ 01 $Y_0Cr_0Y_1Cb_0$ 10 $Cb_0Y_0Cr_0Y_1$ 11 $Cr_0Y_0Cb_0Y_1$	0	X
SEL_DMA_CAM (v)	[2]	Preview path data selection. codec path don't care. 0 : External camera input path 1 : Memory data input path (MSDMA)	0	X
SRC420_MS (v)	[1]	Source image format for MSDMA 0 : YCbCr 4:2:2 (interleaved) 1 : YCbCr 4:2:0 (Non-interleaved)	0	X
ENVID_MS (v)	[0]	MSDMA operation start. Hardware doesn't clear automatically (When triggered Low to High by software setting) 1) SEL_DMA_CAM = '0' , ENVID_MS don't care (using external camera signal for preview path) 2) SEL_DMA_CAM = '1', ENVID_MS is set (0→1) then MSDMA operation start for preview. (external camera signal is valid for only codec_path)	0	X

NOTE: ENVID_MS SFR must be set at last. Starting order for using MSDMA input path.
SEL_DMA_CAM (others SFR setting) → Image Capture Enable SFR setting → ENVID_MS SFR setting.

Figure 23-21. ENVID_MS SFR setting when DMA start to read memory data

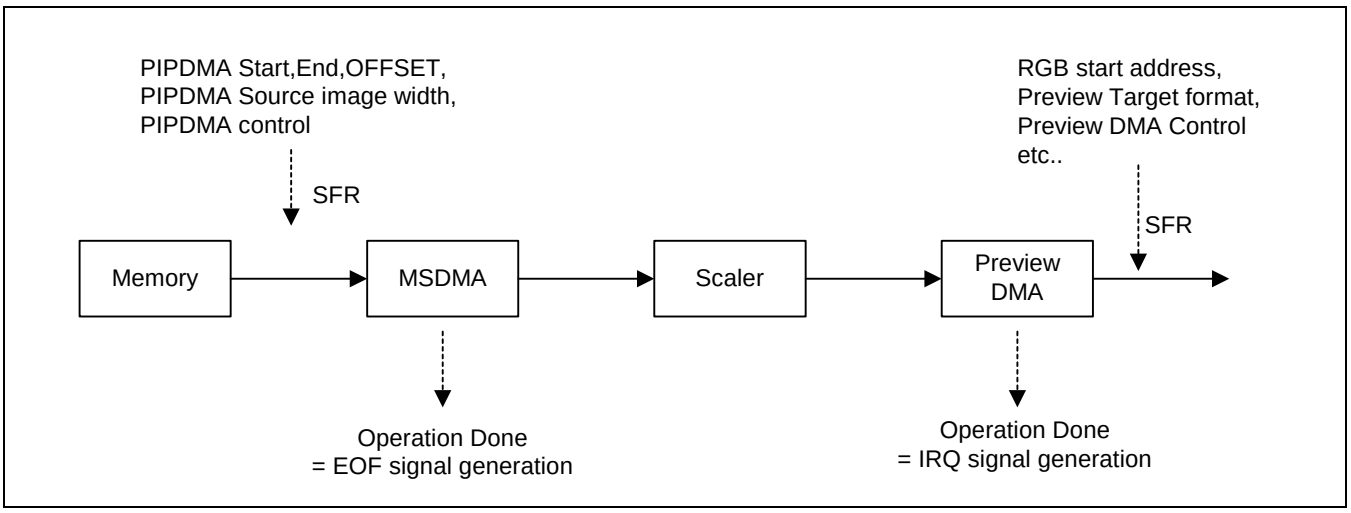


Figure 23-22. SFR & Operation (related each DMA when selected MSDMA input path)

24 ADC & TOUCH SCREEN INTERFACE

OVERVIEW

The 10-bit CMOS ADC (Analog to Digital Converter) is a recycling type device with 10-channel analog inputs. It converts the analog input signal into 10-bit binary digital codes at a maximum conversion rate of 500KSPS with 2.5MHz A/D converter clock. A/D converter operates with on-chip sample-and-hold function and power down mode is supported.

Touch Screen Interface can control/select pads(XP, XM, YP, YM) of the Touch Screen for X, Y position conversion. Touch Screen Interface contains Touch Screen Pads control logic and ADC interface logic with an interrupt generation logic.

FEATURES

- Resolution: 10-bit
- Differential Linearity Error: ± 1.0 LSB
- Integral Linearity Error: ± 2.0 LSB
- Maximum Conversion Rate: 500 KSPS
- Low Power Consumption
- Power Supply Voltage: 3.3V
- Analog Input Range: 0 ~ 3.3V
- On-chip Sample-and-hold Function
- Normal Conversion Mode
- Separate X/Y position conversion Mode
- Auto (Sequential) X/Y Position Conversion Mode
- Waiting for Interrupt Mode

ADC & TOUCH SCREEN INTERFACE OPERATION

BLOCK DIAGRAM

Figure 24-1 shows the functional block diagram of A/D converter and Touch Screen Interface. Note that the A/D converter device is a recycling type.

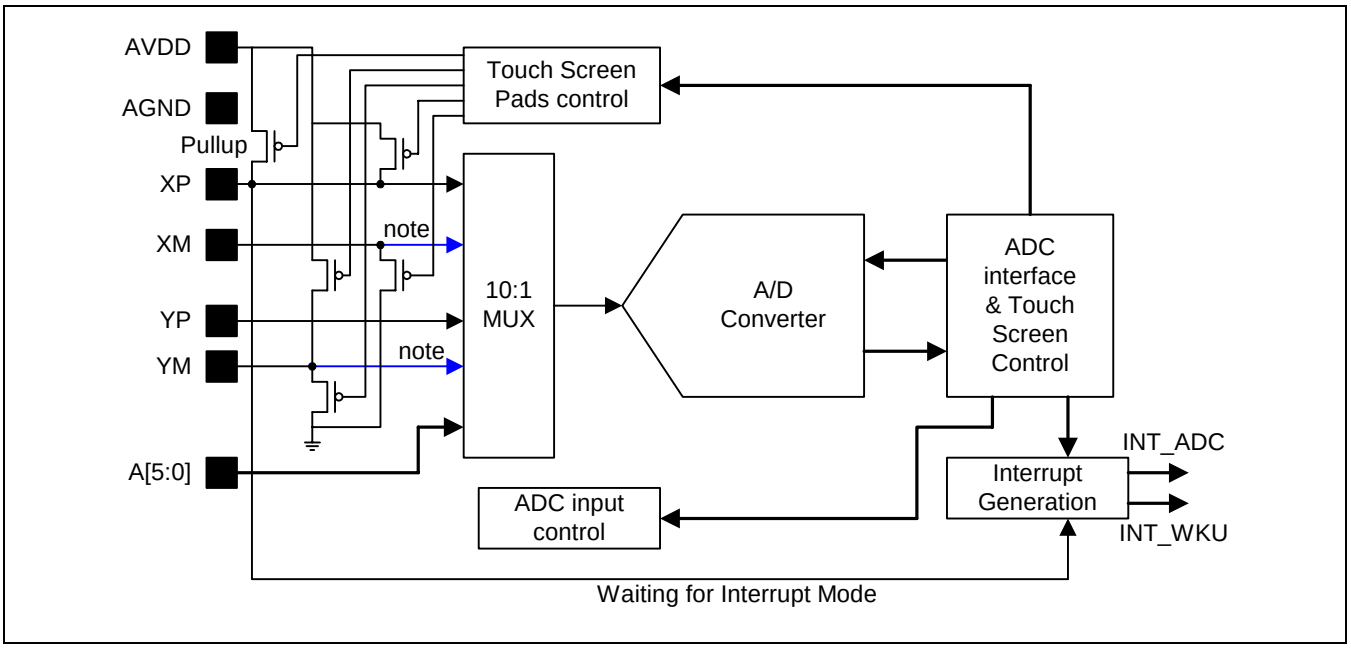


Figure 24-1. ADC and Touch Screen Interface Block Diagram

***NOTE:** (SYMBOL)

When Touch Screen device is used; XM or YM is only connected ground for Touch Screen I/F.
When Touch Screen device is not used, XM or YM is connected to Analog Input Signal for Normal ADC conversion.

FUNCTION DESCRIPTIONS

A/D Conversion Time

When the PCLK frequency is 50 MHz and the prescaler value is 49, total 10-bit conversion time is given:

A/D converter freq. = 50 MHz/(49+1) = 1 MHz

Conversion time = 1/(1 MHz / 5cycles) = 1/200 kHz = 5 us

NOTE:

This A/D converter is designed to operate at maximum 2.5 MHz clock, so the conversion rate can go up to 500 KSPS.

Touch Screen Interface Mode

1. Normal Conversion Mode

Single Conversion Mode is the most likely used for General Purpose ADC Conversion. This mode can be initialized by setting the ADCCON (ADC Control Register) and completed with a read and a write to the ADCDAT0 (ADC Data Register 0).

2. Separate X/Y position conversion Mode

Touch Screen Controller can be operated by one of two Conversion Modes. Separate X/Y Position Conversion Mode is operated as the following way. X-Position Mode writes X-Position Conversion Data to ADCDAT0, so Touch Screen Interface generates the Interrupt source to Interrupt Controller. Y-Position Mode writes Y-Position Conversion Data to ADCDAT1, so Touch Screen Interface generates the Interrupt source to Interrupt Controller.

	XP	XM	YP	YM
X Position Conversion	AVDD	GND	AIN[7]	Hi-Z
Y Position Conversion	AIN[9]	Hi-Z	AVDD	GND

Auto(Sequential) X/Y Position Conversion Mode

Auto (Sequential) X/Y Position Conversion Mode is operated as the following. Touch Screen Controller sequentially converts X-Position and Y-Position that is touched. After Touch controller writes X-measurement data to ADCDAT0 and writes Y-measurement data to ADCDAT1, Touch Screen Interface is generating Interrupt source to Interrupt Controller in Auto Position Conversion Mode.

	XP	XM	YP	YM
X Position Conversion	AVDD	GND	AIN[7]	Hi-Z
Y Position Conversion	AIN[9]	Hi-Z	AVDD	GND

Waiting for Interrupt Mode

Touch Screen Controller generates interrupt (INT_TC) signal when the Stylus is down. Waiting for Interrupt Mode setting value is rADCTSC=0xd3; // XP_PU, XP_Dis, XM_Dis, YP_Dis, YM_En.

After Touch Screen Controller generates interrupt signal (INT_TC), Waiting for interrupt Mode must be cleared. (XY_PST sets to the No operation Mode)

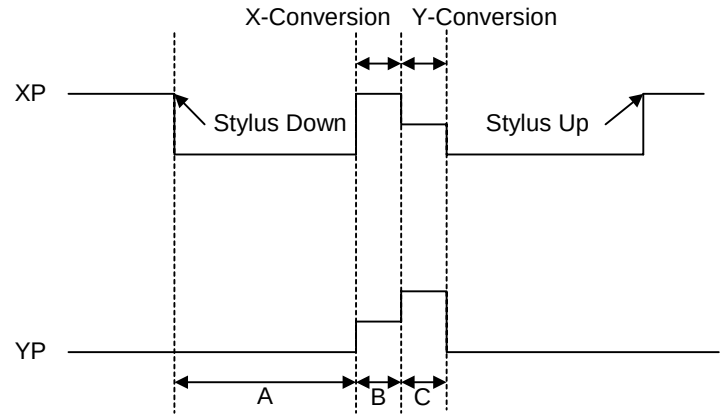
	XP	XM	YP	YM
Waiting for Interrupt Mode	AIN[9](Pull-up enable)	Hi-Z	AIN[7]	GND

Standby Mode

Standby mode is activated when ADCCON [2] is set to '1'. In this mode, A/D conversion operation is halted and ADCDAT0, ADCDAT1 register contains the previous converted data.

Programming Notes

1. The A/D converted data can be accessed by means of interrupt or polling method. With interrupt method, the overall conversion time - from A/D converter start to converted data read - may be delayed because of the return time of interrupt service routine and data access time. With polling method, by checking the ADCCON[15] - end of conversion flag-bit, the read time from ADCDAT register can be determined.
2. A/D conversion can be activated in different way: After ADCCON[1] - A/D conversion start-by-read mode-is set to 1, A/D conversion starts simultaneously whenever converted data is read.



A = D x (1/X-Tal Clock) or **A = D** x (1/External Clock)
B = D x (1/PCLK)
C = D x (1/PCLK)
D = DELAY value of ADCDLY Register

Figure 24-2. Timing Diagram in Auto (Sequential) X/Y Position Conversion Mode

ADC AND TOUCH SCREEN INTERFACE SPECIAL REGISTERS

ADC CONTROL (ADCCON) REGISTER

Register	Address	R/W	Description	Reset Value
ADCCON	0x58000000	R/W	ADC control register	0x3FC4

ADCCON	Bit	Description	Initial State
ECFLG	[15]	End of conversion flag (read only). 0 = A/D conversion in process 1 = End of A/D conversion	0
PRSCEN	[14]	A/D converter prescaler enable. 0 = Disable 1 = Enable	0
PRSCVL	[13:6]	A/D converter prescaler value. Data value: 1 ~ 255 Note that division factor is (N+1) when the prescaler value is N. **NOTE:** ADC frequency should be set less than PCLK by 5 times. (Ex. PCLK = 10MHz, ADC Frequency < 2MHz)	0xFF
	[5:3]	Reserved	0
STDBM	[2]	Standby mode select. 0 = Normal operation mode 1 = Standby mode	1
READ_ START	[1]	A/D conversion start by read. 0 = Disable start by read operation 1 = Enable start by read operation	0
ENABLE_ START	[0]	A/D conversion starts by setting this bit. If READ_START is enabled, this value is not valid. 0 = No operation 1 = A/D conversion starts and this bit is cleared after the start-up.	0

ADC TOUCH SCREEN CONTROL (ADCTSC) REGISTER

Register	Address	R/W	Description	Reset Value
ADCTSC	0x58000004	R/W	ADC touch screen control register	0x058

ADCTSC	Bit	Description	Initial State
UD_SEN	[8]	Detect Stylus Up or Down status. 0 = Detect Stylus Down Interrupt Signal. 1 = Detect Stylus Up Interrupt Signal.	0
YM_SEN	[7]	YM Switch Enable 0 = YM Output Driver Disable.(YM = Hi-z) 1 = YM Output Driver Enable.(YM = GND)	0
YP_SEN	[6]	YP Switch Enable 0 = YP Output Driver Enable.(YP = External Voltage) 1 = YP Output Driver Disable.(YP is connected with AIN[7])	1
XM_SEN	[5]	XM Switch Enable 0 = XM Output Driver Disable.(XM = Hi-z) 1 = XM Output Driver Enable.(XM = GND)	0
XP_SEN	[4]	XP Switch Enable 0 = XP Output Driver Enable.(XP = External Voltage) 1 = XP Output Driver Disable.(XP is connected with AIN[9])	1
PULL_UP	[3]	Pull-up Switch Enable 0 = XP Pull-up Enable. 1 = XP Pull-up Disable.	1
AUTO_PST	[2]	Automatically sequencing conversion of X-Position and Y-Position 0 = Normal ADC conversion. 1 = Auto Sequential measurement of X-position, Y-position.	0
XY_PST	[1:0]	Manually measurement of X-Position or Y-Position. 00 = No operation mode 01 = X-position measurement 10 = Y-position measurement 11 = Waiting for Interrupt Mode	0

NOTES:

1. While waiting for Touch screen Interrupt, XP_SEN bit should be set to '1'(XP Output disable) and PULL_UP bit should be set to '0'(XP Pull-up enable).
2. AUTO_PST bit should be set '1' only in Automatic & Sequential X/Y Position conversion.
3. XP, YP should be disconnected with GND source during sleep mode to avoid leakage current. Because XP, YP will be maintained as 'H' states in sleep mode.

Touch screen pin conditions in X/Y position conversion.

	XP	XM	YP	YM
X Position	AVDD	GND	AIN[7]	Hi-Z
Y Position	AIN[9]	Hi-Z	AVDD	GND

ADC START DELAY (ADCDLY) REGISTER

Register	Address	R/W	Description	Reset Value
ADCDLY	0x58000008	R/W	ADC start or interval delay register	0x00ff

ADCDLY	Bit	Description	Initial State
DELAY	[15:0]	1) Normal Conversion Mode, Separate X/Y Position Conversion Mode, and Auto (Sequential) X/Y Position Conversion Mode. → X/Y Position Conversion Delay Value. 2) Waiting for Interrupt Mode. When Stylus down occurs in Waiting for Interrupt Mode, this register generates Interrupt signal (INT_TC) at intervals of several ms for Auto X/Y Position conversion. **NOTE:** Do not use Zero value (0x0000)	00ff

ADC CONVERSION DATA (ADCDAT0) REGISTER

Register	Address	R/W	Description	Reset Value
ADCDAT0	0x5800000C	R	ADC conversion data register	-

ADCDAT0	Bit	Description	Initial State
UPDOWN	[15]	Up or down state of Stylus at Waiting for Interrupt Mode. 0 = Stylus down state 1 = Stylus up state	-
AUTO_PST	[14]	Automatic sequencing conversion of X-position and Y-position. 0 = Normal ADC conversion 1 = Sequencing measurement of X-position, Y-position	-
XY_PST	[13:12]	Manual measurement of X-position or Y-position. 00 = No operation mode 01 = X-position measurement 10 = Y-position measurement 11 = Waiting for Interrupt Mode	-
Reserved	[11:10]	Reserved	
XPDATA (Normal ADC)	[9:0]	X-position conversion data value. (include Normal ADC conversion data value) Data value: 0 ~ 3FF	-

ADC CONVERSION DATA (ADCDAT1) REGISTER

Register	Address	R/W	Description	Reset Value
ADCDAT1	0x58000010	R	ADC conversion data register	-

ADCDAT1	Bit	Description	Initial State
UPDOWN	[15]	Up or down state of Stylus at Waiting for Interrupt Mode. 0 = Stylus down state 1 = Stylus up state	-
AUTO_PST	[14]	Automatically sequencing conversion of X-position and Y-position. 0 = Normal ADC conversion 1 = Sequencing measurement of X-position, Y-position	-
XY_PST	[13:12]	Manual measurement of X-position or Y-position. 00 = No operation mode 01 = X-position measurement 10 = Y-position measurement 11 = Waiting for Interrupt Mode	-
Reserved	[11:10]	Reserved	
YPDATA	[9:0]	Y-position conversion data value Data value: 0 ~ 3FF	-

ADC TOUCH SCREEN UP-DOWN INT CHECK REGISTER (ADCUPDN)

Register	Address	R/W	Description	Reset Value
ADCUPDN	0x5800014	R/W	Stylus Up or Down Interrpt status register	0x0

ADCUPDN	Bit	Description	Initial State
TSC_UP	[1]	Stylus Up Interrupt. 0 = No stylus up status. 1 = Stylus up interrupt occurred.	0
TSC_DN	[0]	Stylus Down Interrupt. 0 = No stylus down status. 1 = Stylus down interrupt occurred.	0

ADC CHANNEL MUX REGISTER (ADCMUX)

Register	Address	R/W	Description	Reset Value
ADCMUX	0x5800018	R/W	Analog input channel select	0x0

ADCMUX	Bit	Description	Initial State
ADCMUX	[3:0]	Analog input channel select. 0000 = AIN 0 0001 = AIN 1 0010 = AIN 2 0011 = AIN 3 0100 = AIN 4 0101 = AIN 5 0110 = AIN 6 (YM) 0111 = AIN 7 (YP) 1000 = AIN8 (XM) 1001 = AIN9 (XP)	0

NOTE: When Touch Screen Pads(YM, YP, XM, XP) are disabled, these ports can be used as Analog input ports(AIN6, AIN7, AIN8, AIN9) for ADC.

NOTES

25 IIS-BUS INTERFACE

OVERVIEW

IIS (Inter-IC Sound) interface transmits or receives sound data from or to external stereo audio codec. For transmit and receive data, two 32x16 FIFOs (First-In-First-Out) data structures are included and DMA transfer mode for transmitting or receiving samples can be supported. IIS-specific clock can be supplied from internal system clock controller through IIS clock divider or direct clock source.

FEATURES

- 1-ch IIS-bus for audio interface with DMA-based operation
- Serial, 8-/16-bit per channel data transfers
- 128 Bytes (64-Byte + 64-Byte) FIFO for Tx/Rx
- Supports two IIS data format (MSB-justified or LSB-justified data format)

IIS CONTROLLER OPERATION

BLOCK DIAGRAM

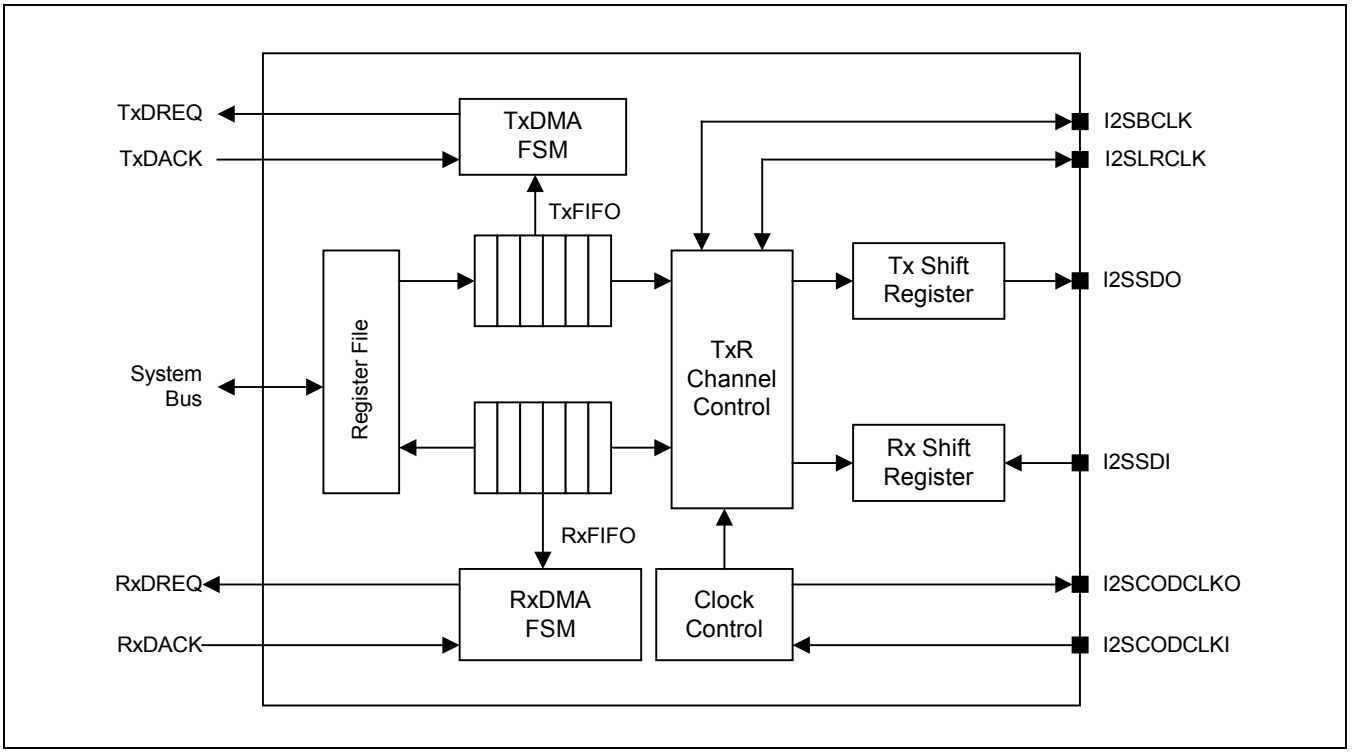


Figure 25-1. IIS-Bus Block Diagram

IIS interface consists of register bank, FIFOs, shift registers, clock control, DMA finite state machine, and channel control block as shown in Figure 25-1. Note that each FIFO has 32-bit width and 16 depth structure, which contains left/right channel data. So, FIFO access and data transfer are handled with left/right pair unit. Figure 25-1 shows the functional block diagram of IIS interface.

MASTER/SLAVE MODE

Master or slave mode can be chosen by setting IMS bits of I2SMOD register. There 2 modes in a master mode (internal master, external master). In internal master mode, I2SBCLK and I2SLRCLK are generated internally and supplied to external device. Therefore a root clock is needed for generating I2SBCLK and I2SLRCLK by dividing. The I2S pre-scaler (clock divider) is employed for generating a root clock with divided frequency from internal system clock. In external master mode, the root clock can be fed from I2S external directly. In slave mode, the I2SBCLK and I2SLRCLK are fed from chip external pin. So there is no need for generating root clock.

Figure 25-2 shows the route of the root clock with internal master or external master mode setting in the IIS clock control block & syscon. Note that RCLK indicates root clock and this clock can be provided to external IIS codec chip at internal master mode.

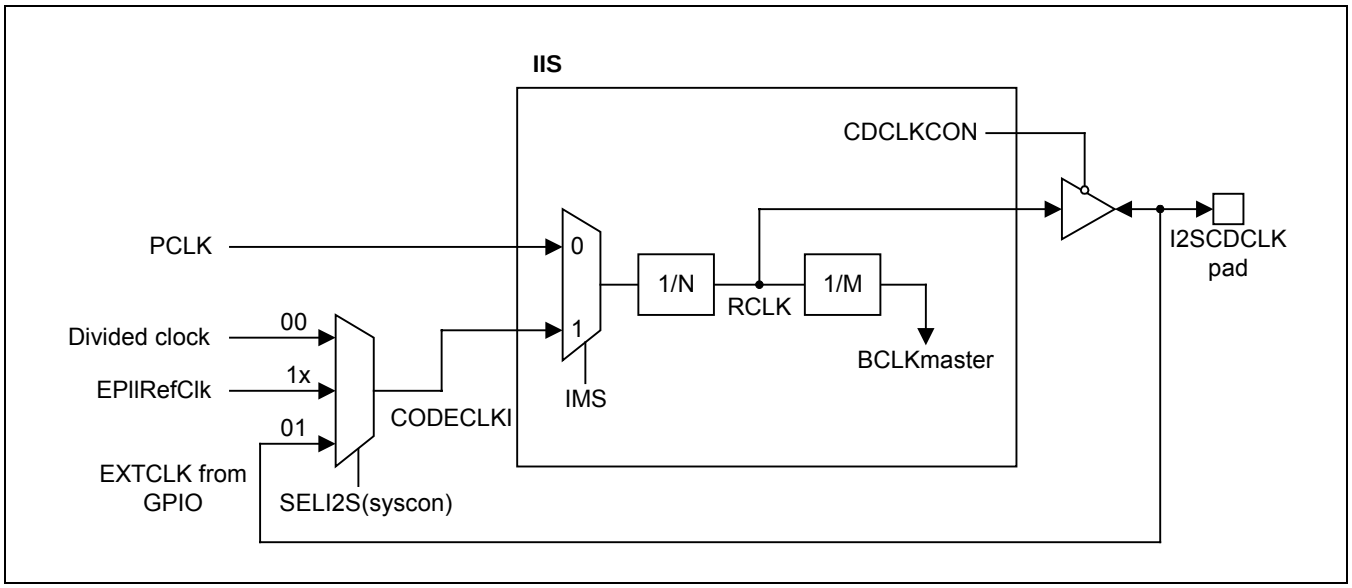


Figure 25-2. IIS Clock Control Block Diragram

SELI2S (14, 15th bits of CLKSRC SFR) is in syscon. Please refer syscon manual.
IMS (10, 11 th bit of I2SMOD SFR) select clock source in master mode. (Refer to I2SMOD register)
CDCLKCON (12th bit of I2SMOD SFR) controls codec clock source. When 0, internal codec clock source is used and fed to external chip. When 1, external codec clock is fed from external chip.
1/N is controlled by pre-scaler division value (refer I2SPSR register).
1/M is controlled by BFS and RFS (refer I2SMODE register)

DMA Transfer

In the DMA transfer mode, the transmitter or receiver FIFO are accessible by DMA controller. DMA service request is activated internally by the transmitter or receiver FIFO state. The FTXEMPT, FRXEMPT, FTXFULL, and FRXFULL bits of I2SCON register represent the transmitter or receiver FIFO data state. Especially, FTXEMPT and FRXFULL bit are the ready flag for DMA service request; the transmit DMA service request is activated when TxFIFO is not empty and the receiver DMA service request is activated when RxFIFO is not full.

The DMA transfer uses only handshaking method for single data. Note that during DMA acknowledge activation, the data read or write operation should be performed.

IIS-bus format

The IIS bus has four lines including serial data input I2SSDI, serial data output I2SSDO, left/right channel select clock I2SLRCLK, and serial bit clock I2SBCLK; the device generating I2SLRCLK and I2SBCLK is the master.

Serial data is transmitted in 2's complement with the MSB first with a fixed position, whereas the position of the LSB depends on the word length. The transmitter sends the MSB of the next word at one clock period after the I2SLRCLK is changed. Serial data sent by the transmitter may be synchronized with either the trailing or the leading edge of the clock signal. However, the serial data must be latched into the receiver on the leading edge of the serial clock signal, and so there are some restrictions when transmitting data that is synchronized with the leading edge.

The LR channel select line indicates the channel being transmitted. I2SLRCLK may be changed either on a trailing or leading edge of the serial clock, but it does not need to be symmetrical. In the slave, this signal is latched on the leading edge of the clock signal. The I2SLRCLK line changes one clock period before the MSB is transmitted. This allows the slave transmitter to derive synchronous timing of the serial data that will be set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next word.

MSB (Left) Justified

MSB-Justified (Left-Justified) format is similar to IIS bus format, except that in MSB-justified format, the transmitter always sends the MSB of the next word at the same time whenever the I2SLRCLK is changed.

LSB (Right) Justified

LSB-Justified (Right-Justified) format is opposite to the MSB-justified format. In other word, the transferring serial data is aligned with ending point of I2SLRCLK transition.

Figure 25-3 shows the audio serial format of IIS, MSB-justified, and LSB-justified. Note that in this figure, the word length is 16 bit and I2SLRCLK makes transition every 24 cycle of I2SBCLK (BFS is 48 fs, where fs is sampling frequency; I2SLRCLK frequency).

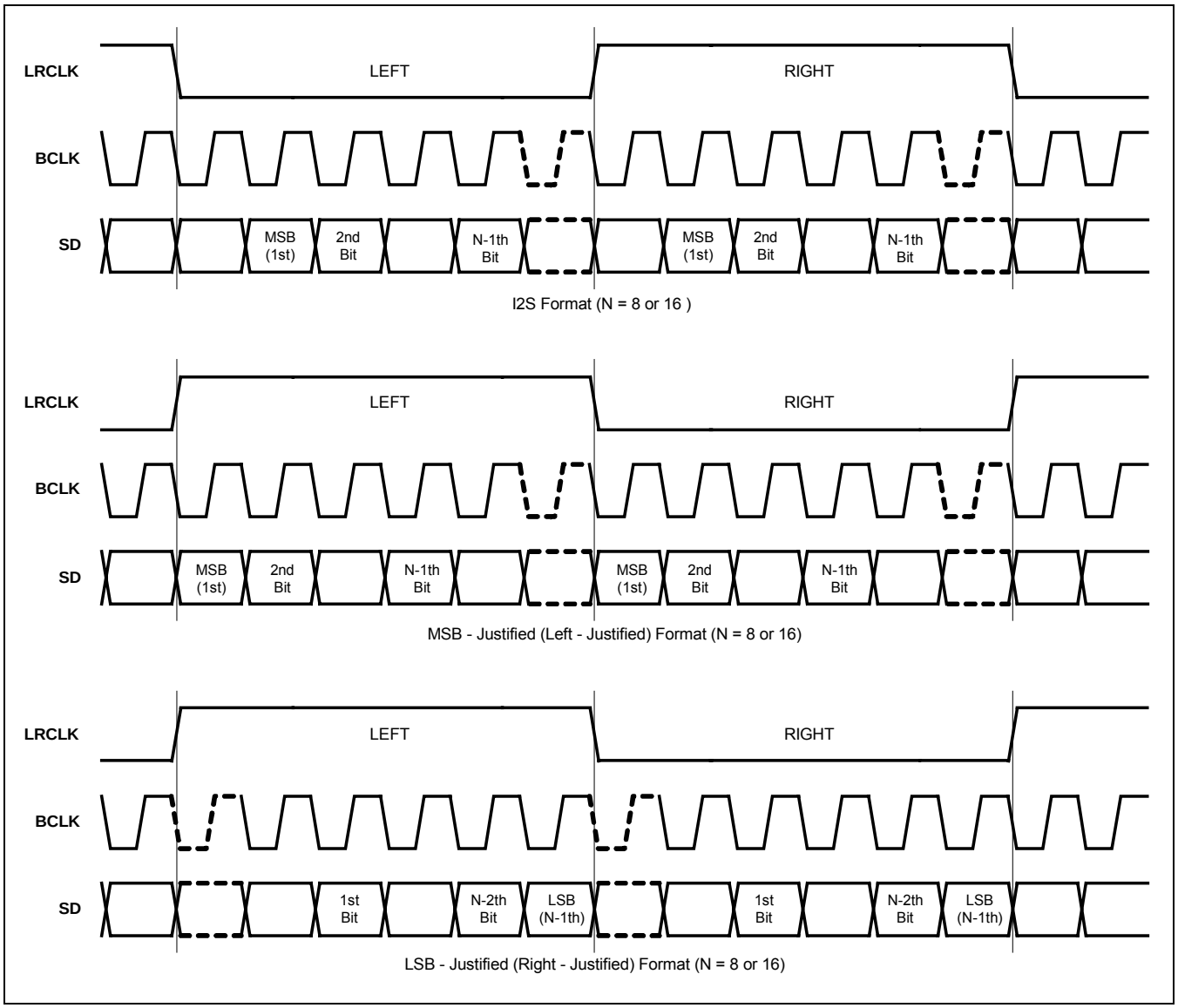


Figure 25-3. IIS Audio Serial Data Formats

SAMPLING FREQUENCY AND MASTER CLOCK

Master clock frequency (RCLK) can be selected by sampling frequency as shown in Table 25-1. Because RCLK is made by IIS prescaler, the prescaler value and RCLK type (256 or 384fs) should be determined properly.

Table 25-1. CODEC clock (CODECLK = 256, 384, 512 or 768fs)

IISLRCK (fs)	8.000 kHz	11.025 kHz	16.000 kHz	22.050 kHz	32.000 kHz	44.100 kHz	48.000 kHz	64.000 kHz	88.200 kHz	96.000 kHz
CODECLK (MHz)	256fs									
	2.0480	2.8224	4.0960	5.6448	8.1920	11.2896	12.2880	16.3840	22.5792	24.5760
	384fs									
	3.0720	4.2336	6.1440	8.4672	12.2880	16.9344	18.4320	24.5760	33.8688	36.8640
	512fs									
	4.0960	5.6448	8.1920	11.2900	16.3840	22.5790	24.5760	32.7680	45.1580	49.1520
	768fs									
	6.1440	8.4672	12.2880	16.9340	24.5760	33.8690	36.8640	49.1520	67.7380	73.7280

IIS CLOCK MAPPING TABLE

On selecting BFS, RFS, and BLC bits of I2SMOD register, user should refer to the following table. Table 25-2 shows the allowable clock frequency mapping relations.

Table 25-2. IIS clock mapping table

Clock Frequency		RFS			
		256 fs (00B)	512 fs (01B)	384 fs (10B)	768 fs (11B)
BFS	16 fs (10B)	(a)	(a)	(a)	(a)
	24 fs (11B)	-	-	(a)	(a)
	32 fs (00B)	(a) (b)	(a) (b)	(a) (b)	(a) (b)
	48 fs (01B)	-	-	(a) (b)	(a) (b)
Descriptions		(a) Allowed when BLC is 8-bit (b) Allowed when BLC is 16-bit			

IIS-BUS INTERFACE SPECIAL REGISTERS

IIS CONTROL REGISTER (I2SCON)

Register	Address	R/W	Description	Reset Value
I2SCON	0x55000000	R/W	IIS interface control register	0xE00

I2SCON	Bit	R/W	Description	Initial State
Reserved	[31:12]	R/W	Reserved. Program to zero.	0
LRI	[11]	R	Left/Right channel clock indication. Note that LRI meaning is dependent on the value of LRP bit of I2SMOD register. 0: Left (when LRP bit is low) or right (when LRP bit is high) 1: Right (when LRP bit is low) or left (when LRP bit is high)	1
FTXEMPT	[10]	R	Tx FIFO empty status indication. 0: FIFO is not empty (ready for transmit data to channel) 1: FIFO is empty (not ready for transmit data to channel)	1
FRXEMPT	[9]	R	Rx FIFO empty status indication. 0: FIFO is not empty 1: FIFO is empty	1
FTXFULL	[8]	R	Tx FIFO full status indication. 0: FIFO is not full 1: FIFO is full	0
FRXFULL	[7]	R	Rx FIFO full status indication. 0: FIFO is not full (ready for receive data from channel) 1: FIFO is full (not ready for receive data from channel)	0
TXDMAPAUSE	[6]	R/W	Tx DMA operation pause command. Note that when this bit is activated at any time, the DMA request will be halted after current on-going DMA transfer is completed. 0: No pause DMA operation 1: Pause DMA operation	0
RXDMAPAUSE	[5]	R/W	Rx DMA operation pause command. Note that when this bit is activated at any time, the DMA request will be halted after current on-going DMA transfer is completed. 0: No pause DMA operation 1: Pause DMA operation	0

I2SCON	Bit	R/W	Description	Initial State
TXCHPAUSE	[4]	R/W	Tx channel operation pause command. Note that when this bit is activated at any time, the channel operation will be halted after left-right channel data transfer is completed. 0: No pause operation 1: Pause operation	0
RXCHPAUSE	[3]	R/W	Rx channel operation pause command. Note that when this bit is activated at any time, the channel operation will be halted after left-right channel data transfer is completed. 0: No pause operation 1: Pause operation	0
TXDMACTIVE	[2]	R/W	Tx DMA active (start DMA request). Note that when this bit is set from high to low, the DMA operation will be forced to stop immediately. 0: Inactive, 1: Active	0
RXDMACTIVE	[1]	R/W	Rx DMA active (start DMA request). Note that when this bit is set from high to low, the DMA operation will be forced to stop immediately. 0: Inactive, 1: Active	0
I2SACTIVE	[0]	R/W	I2S interface active (start operation). 0: Inactive, 1:Active	0

NOTE: All registers of I2S interface are accessible by word unit with STR/LDR instructions.

IIS MODE REGISTER (I2SMOD)

Register	Address	R/W	Description	Reset Value
I2SMOD	0x55000004	R/W	IIS interface mode register	0x0

I2SMOD	Bit	R/W	Description	Initial State
Reserved	[31:13]	R/W	Reserved. Program to zero.	0
CDCLKCON	[12]	R/W	Determine codec clock source 0 : Use internal (2443) codec clock source 1 : Get codec clock source from external codec chip	0
IMS	[11:10]	R/W	I2S master or slave mode select. 00: Master mode (use PCLK for generating CODECLK) 01: Master mode (use CODECLKI for generating CODECLK) 1x: Slave mode (Please refer Figure 25-2)	0
TXR	[9:8]	R/W	Transmit or receive mode select. 00: Transmit only mode 01: Receive only mode 10: Transmit and receive simultaneous mode 11: Reserved	0
LRP	[7]	R/W	Left/Right channel clock polarity select. 0: Low for left channel and high for right channel 1: High for left channel and low for right channel	0
SDF	[6:5]	R/W	Serial data format. 00: I2S format 01: MSB-justified (left-justified) format 10: LSB-justified (right-justified) format 11: Reserved	0
RFS	[4:3]	R/W	I2S root clock (codec clock) frequency select. 00: 256 fs, where fs is sampling frequency 01: 512 fs 10: 384 fs 11: 768 fs	0
BFS	[2:1]	R/W	Bit clock frequency select. 00: 32 fs, where fs is sampling frequency 01: 48 fs 10:16 fs 11: 24 fs	0
BLC	[0]	R/W	Bit length per channel. 0: 16-bit, 1: 8-bit	0

IIS FIFO CONTROL REGISTER (I2SFIC)

Register	Address	R/W	Description	Reset Value
I2SFIC	0x55000008	R/W	IIS interface FIFO control register	0x0

I2SFIC	Bit	R/W	Description	Initial State
Reserved	[31:16]	R/W	Reserved. Program to zero.	0
TFLUSH	[15]	R/W	Tx FIFO flush command. 0: No flush, 1: Flush	0
Reserved	[14:13]	R/W	Reserved. Program to zero.	0
FTXCNT	[12:8]	R	Tx FIFO data count. FIFO has 16 dept, so value ranges from 0 to 16. N: Data count N of FIFO	0
RFLUSH	[7]	R/W	Rx FIFO flush command. 0: No flush, 1: Flush	0
Reserved	[6:5]	R/W	Reserved. Program to zero.	0
FRXCNT	[4:0]	R	Rx FIFO data count. FIFO has 16 dept, so value ranges from 0 to 16. N: Data count N of FIFO	0

IIS PRESCALER CONTROL REGISTER (I2SFIC)

Register	Address	R/W	Description	Reset Value
I2SPSR	0x5500000C	R/W	IIS interface prescaler(clock divider) control register	0x0

I2SPSR	Bit	R/W	Description	Initial State
Reserved	[31:16]	R/W	Reserved. Program to zero.	0
PSRAEN	[15]	R/W	Prescaler (Clock divider) A active. 0: Inactive, 1: Active	0
Reserved	[14:10]	R/W	Reserved. Program to zero.	0
PSVALA	[9:0]	R/W	Prescaler (Clock divider) A division value. N: Division factor is N+1	0

IIS TRANSMIT DATA REGISTER (I2STXD)

Register	Address	R/W	Description	Reset Value
I2STXD	0x55000010	W	IIS interface transmit data register	0x0

I2STXD	Bit	R/W	Description	Initial State
I2STXD	[31:0]	W	Tx FIFO write data. Note that the left/right channel data is allocated as the following bit fields. R[31:16], L[15:0] when 16-bit BLC R[23:16], L[7:0] when 8-bit BLC	0

IIS RECEIVE DATA REGISTER (I2SRXD)

Register	Address	R/W	Description	Reset Value
I2SRXD	0x55000014	R	IIS interface receive data register	0x0

I2SRXD	Bit	R/W	Description	Initial State
I2SRXD	[31:0]	R	Rx FIFO read data. Note that the left/right channel data is allocated as the following bit fields. R[31:16], L[15:0] when 16-bit BLC R[23:16], L[7:0] when 8-bit BLC	0

NOTES

26 AC97 CONTROLLER

OVERVIEW

The AC97 Controller Unit of the S3C2443 supports the AC97 revision 2.0 features. AC97 Controller communicates with AC97 Codec using audio controller link (AC-link). Controller sends the stereo PCM data to Codec. The external digital-to-analog converter (DAC) in the Codec then converts the audio sample to an analog audio waveform. Also, Controller receives the stereo PCM data and the mono Mic data from Codec then store in memories. This chapter describes the programming model for the AC97 Controller Unit. The information in this chapter requires an understanding of the AC97 revision 2.0 specifications.

FEATURES

- Independent channels for stereo PCM In, stereo PCM Out, mono MIC In.
- DMA-based operation and interrupt based operation.
- All of the channels support only 16-bit samples.
- Variable sampling rate AC97 Codec interface (48KHz and below)
- 16-bit, 16 entry FIFOs per channel
- Only primary Codec support

AC97 CONTROLLER OPERATION

BLOCK DIAGRAM

Figure 26-1 shows the functional block diagram of S3C2443 AC97 Controller. The AC97 signals form the AC-link, which is a point-to-point synchronous serial inter-connecting that supports full-duplex data transfers. All digital audio streams and command/status information are communicated over the AC-link.

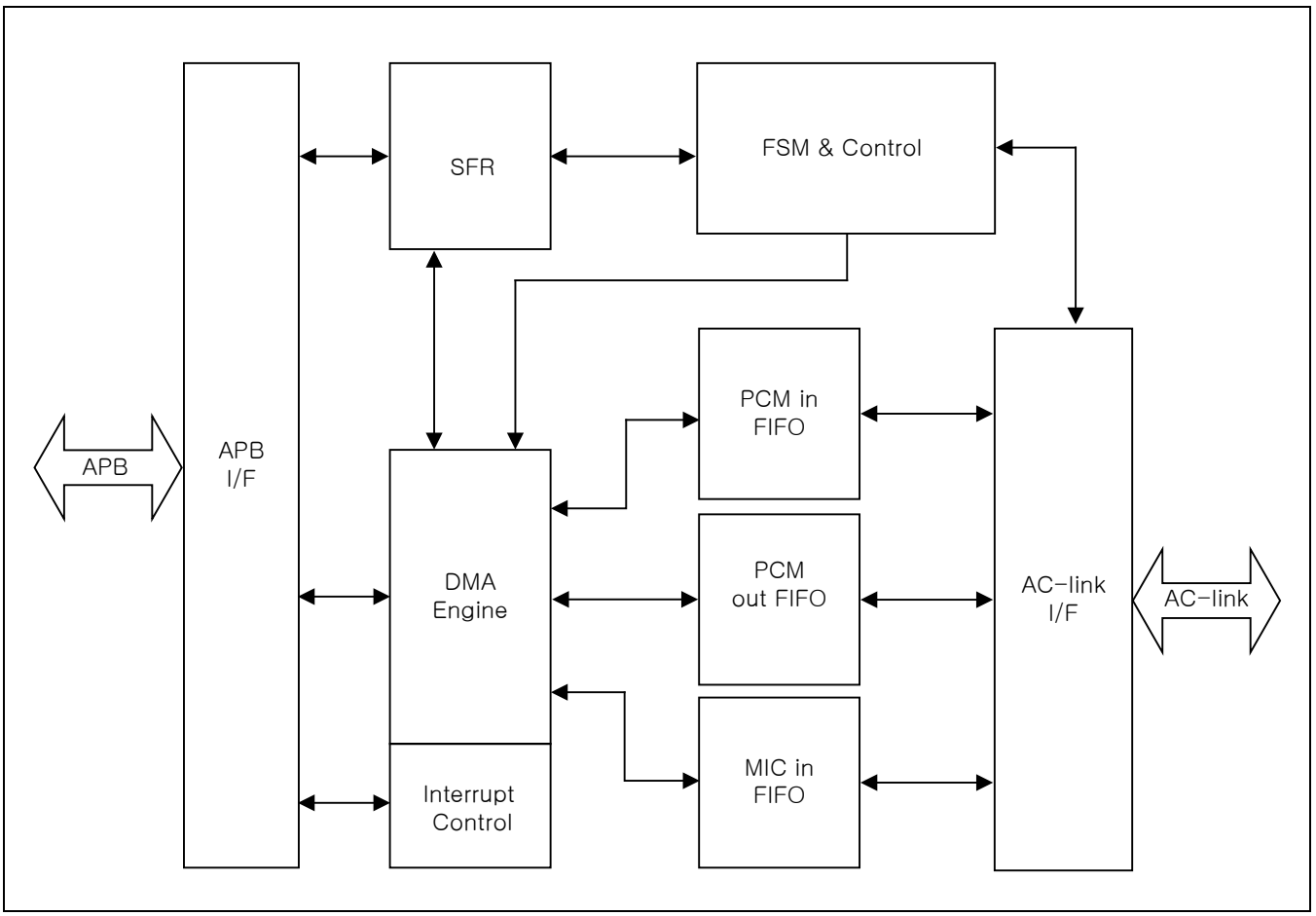


Figure 26-1. AC97 Block Diagram

INTERNAL DATA PATH

Figure 26-2 shows the internal data path of S3C2443 AC97 Controller. It has stereo Pulse Code Modulated (PCM) In, Stereo PCM Out and mono Mic-in buffers, which consist of 16-bit, 16 entries buffer. It also has 20-bit I/O shift register via AC-link.

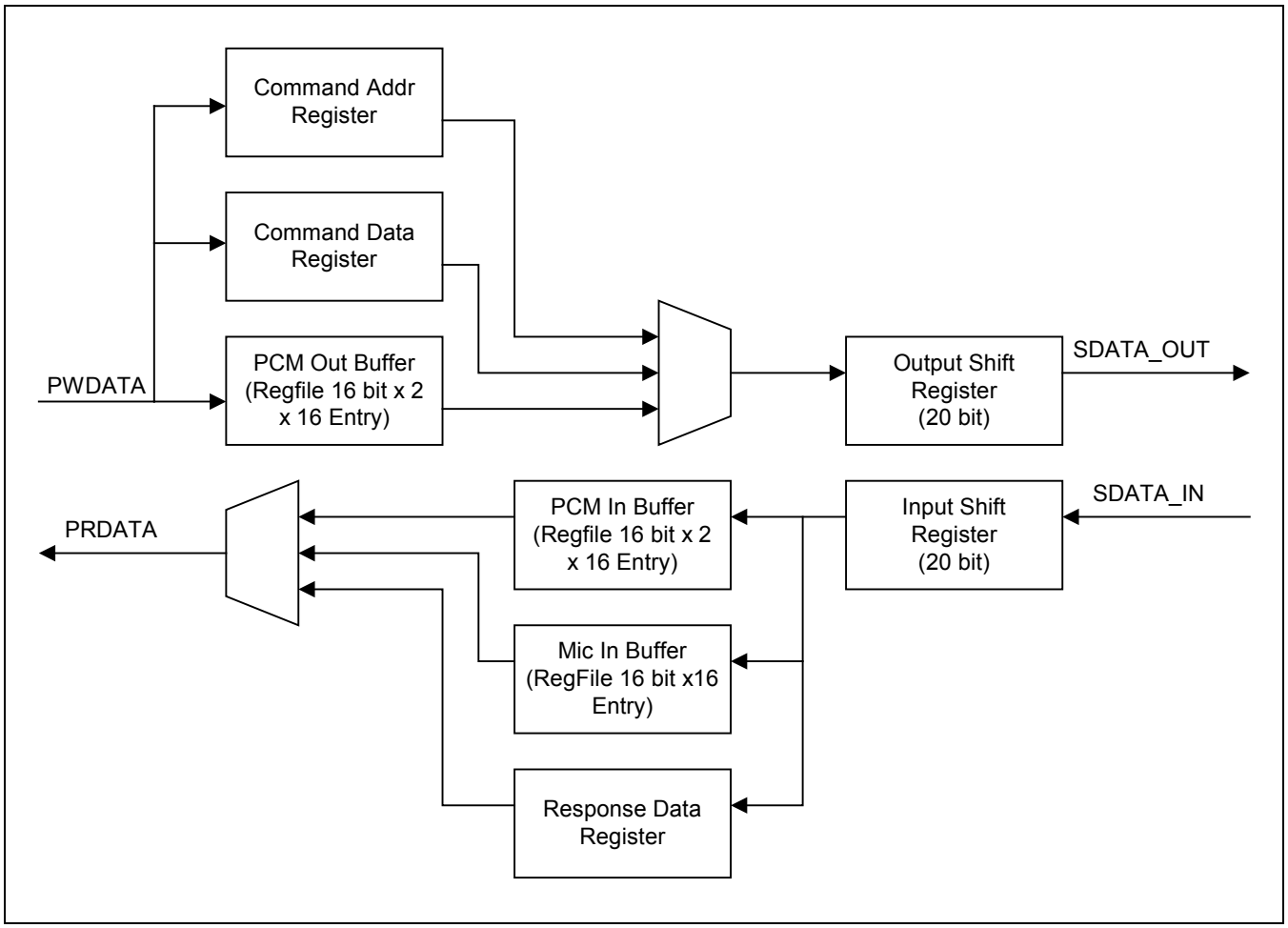


Figure 26-2. Internal Data Path

OPERATION FLOW CHART

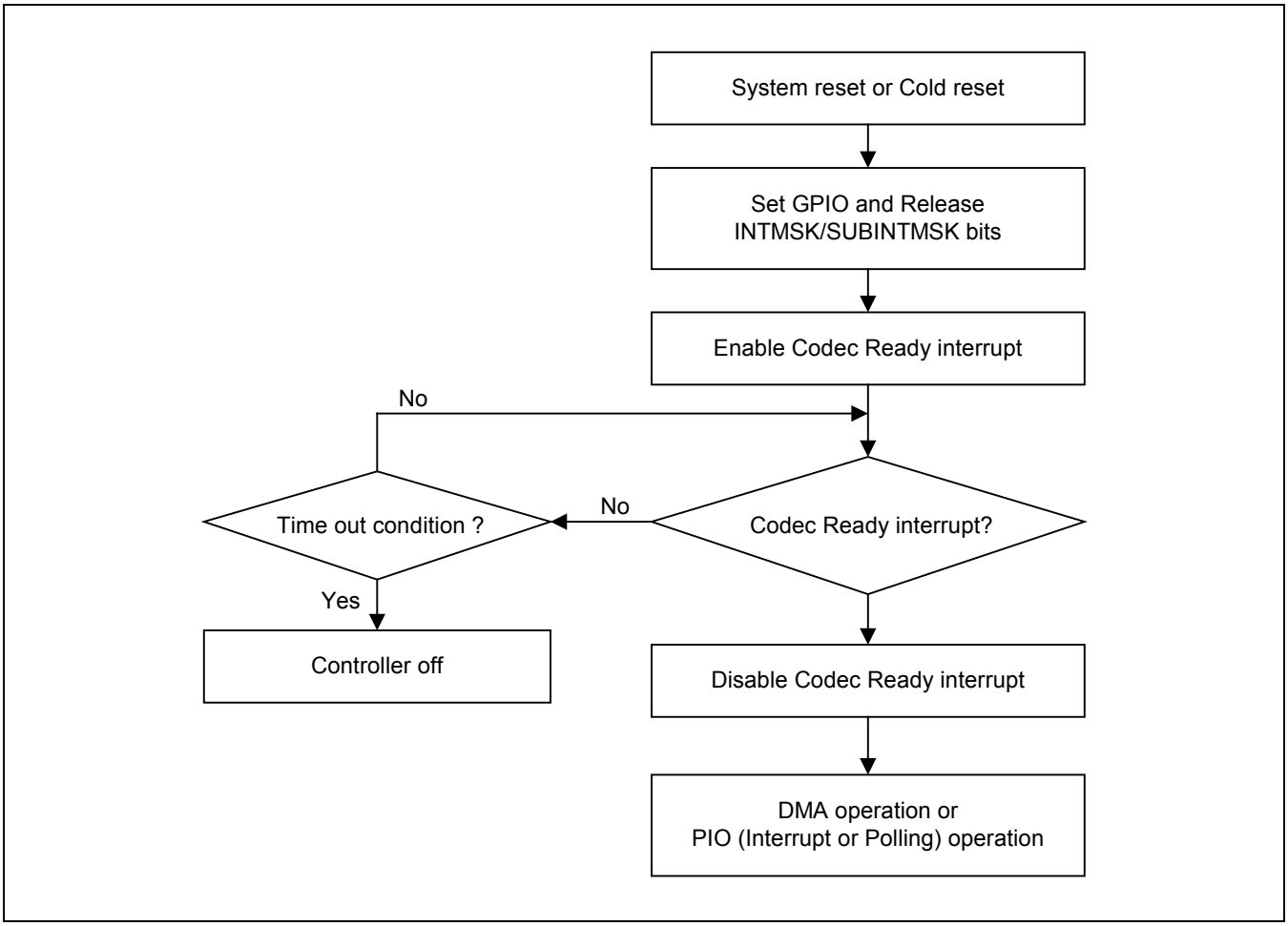


Figure 26-3. AC97 Operation Flow Chart

AC-LINK DIGITAL INTERFACE PROTOCOL

Each AC97 Codec incorporates a five-pin digital serial interface that links it to the S3C2443 AC97 Controller. AC-link is a full-duplex, fixed-clock, PCM digital stream. It employs a time division multiplexed (TDM) scheme to handle control register accesses and multiple input and output audio streams. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams. Each stream has 20-bit sample resolution and requires a DAC and an analog-to-digital converter (ADC) with a minimum 16-bit resolution.

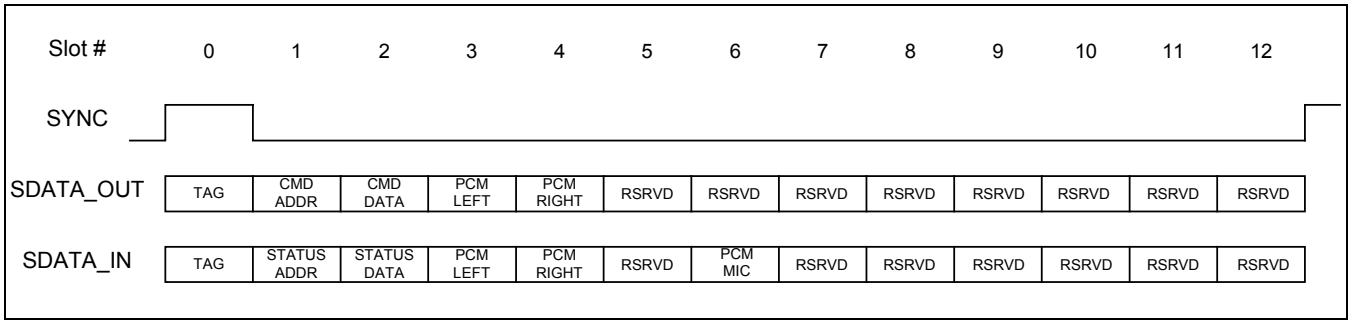


Figure 26-4. Bi-directional AC-link Frame with Slot Assignments

Figure 26-4 shows the slot definitions that the S3C2443 AC97 Controller supports. The S3C2443 AC97 Controller provides synchronization for all data transaction on the AC-link.

A data transaction is made up of 256 bits of information broken up into groups of 13 time slots and is called a frame. Time slot 0 is called the Tag Phase and is 16 bits long. The other 12 time slots are called the Data Phase. The Tag Phase contains one bit that identifies a valid frame and 12 bits that identify the time slots in the Data Phase that contain valid data. Each time slot in the Data Phase is 20 bits long. A frame begins when SYNC goes high. The amount of time that SYNC is high corresponds to the Tag Phase. AC97 frames occur at fixed 48 kHz intervals and are synchronous to the 12.288 MHz bit rate clock, BITCLK. The controller and the Codec use the SYNC and BITCLK to determine when to send transmit data and when to sample received data. A transmitter transitions the serial data stream on each rising edge of BITCLK and a receiver samples the serial data stream on falling edges of BITCLK. The transmitter must tag the valid slots in its serial data stream. The valid slots are tagged in slot 0. Serial data on the AC-link is ordered most significant bit (MSB) to least significant bit (LSB). The Tag Phase's first bit is bit 15 and the first bit of each slot in Data Phase is bit 19. The last bit in any slot is bit 0.

AC-LINK OUTPUT FRAME (SDATA_OUT)

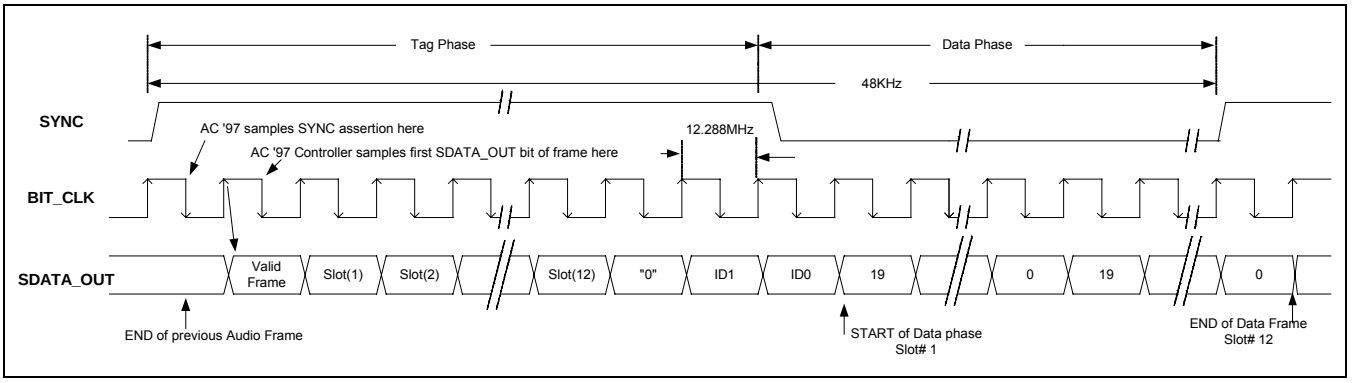


Figure 26-5. AC-link Output Frame

AC-LINK INPUT FRAME (SDATA_IN)

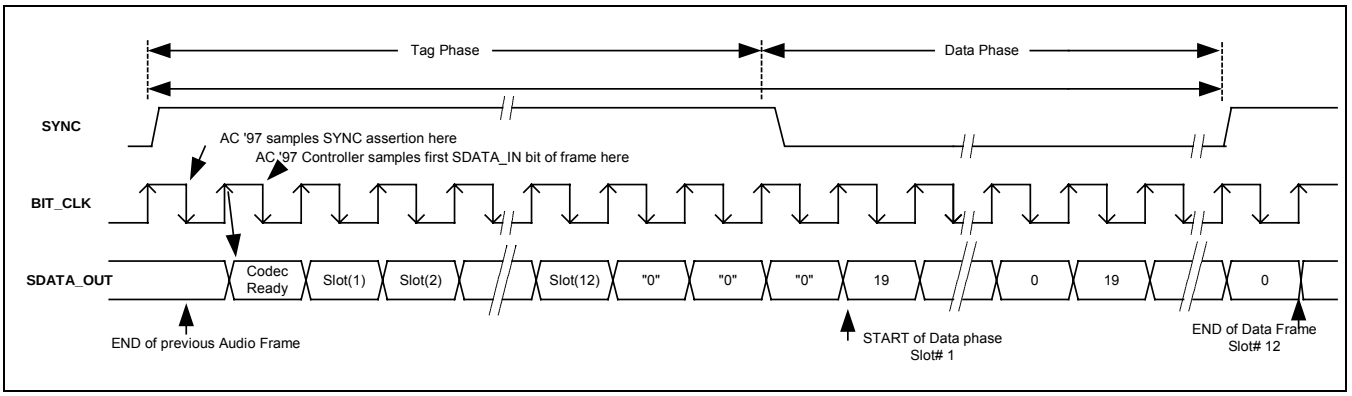


Figure 26-6. AC-link Input Frame

POWERING DOWN THE AC-LINK

The AC-link signals enter a low power mode when the AC97 Codec Powerdown register (0x26) bit PR4 is set to a 1 (by writing 0x1000). Then the Primary Codec drives both BITCLK and SDATA_IN to a logic low voltage level. The sequence follows the timing diagram shown in Figure 26-7.

The AC97 Controller transmits the write to Powerdown register (0x26) over the AC-link. Set up the AC97 Controller so that it does not transmit data to slots 3-12 when it writes to the Powerdown register bit PR4 (data 0x1000), and it does not require the Codec to process other data when it receives a power down request. When the Codec processes the request it immediately transitions BITCLK and SDATA_IN to a logic low level. The AC97 Controller drives SYNC and SDATA_OUT to a logic low level after programming the AC_GLBCTRL register.

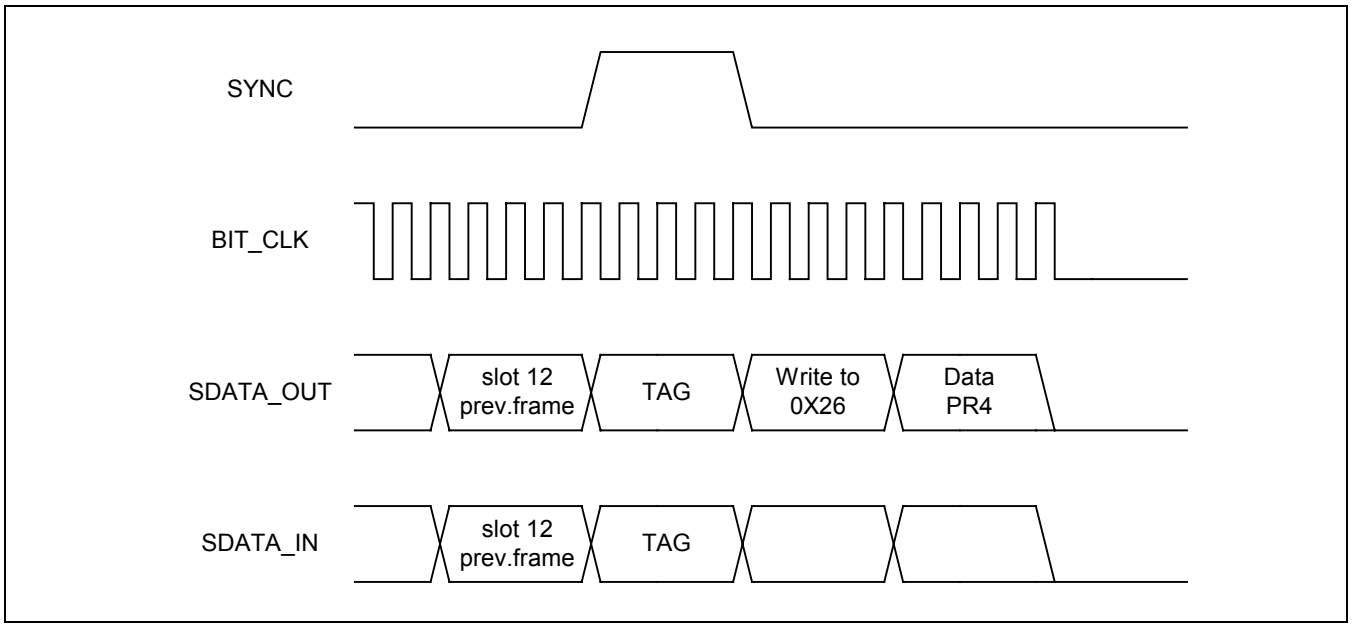


Figure 26-7. AC97 Powerdown Timing

WAKING UP THE AC-LINK - WAKE UP TRIGGERED BY THE AC97 CONTROLLER

AC-link protocol provides for a cold AC97 reset and a warm AC97 reset. The current power-down state ultimately dictates which AC97 reset is used. Registers must stay in the same state during all power-down modes unless a cold AC97 reset is performed. In a cold AC97 reset, the AC97 registers are initialized to their default values. After a power down, the AC-link must wait for a minimum of four audio frame times after the frame in which the power down occurred before it can be reactivated by reasserting the SYNC signal. When AC-link powers up, it indicates readiness through the Codec ready bit (input slot 0, bit 15).

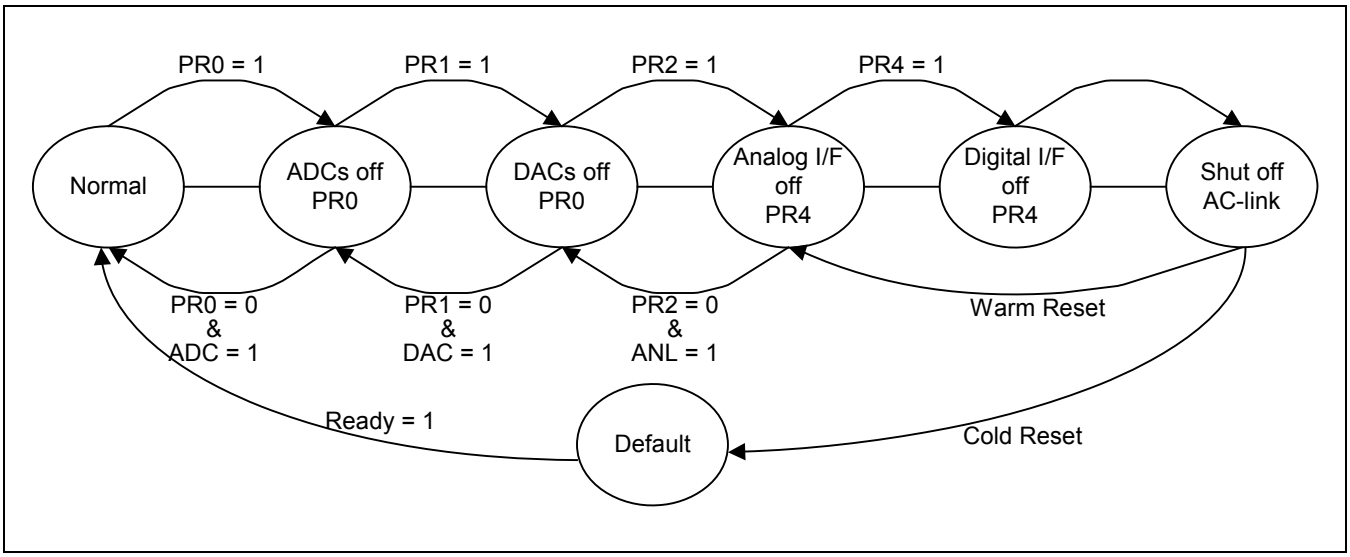


Figure 26-8 AC97 Power down/Power up Flow

COLD AC97 RESET

A cold reset is generated when the nRESET pin is asserted through the AC_GLBCTRL. Asserting and deasserting nRESET activates BITCLK and SDATA_OUT. All AC97 control registers are initialized to their default power on reset values. nRESET is an asynchronous AC97 input.

WARM AC97 RESET

A Warm AC97 reset reactivates the AC-link without altering the current AC97 register values. A warm reset is generated when BITCLK is absent and SYNC is driven high. In normal audio frames, SYNC is a synchronous AC97 input. When BITCLK is absent, SYNC is treated as an asynchronous input used to generate a warm reset to AC97.The AC97 Controller must not activate BITCLK until it samples SYNC low again. This prevents a new audio frame from being falsely detected.

AC97 CONTROLLER SPECIAL REGISTERS

AC97 GLOBAL CONTROL REGISTER (AC_GLBCTRL)

Register	Address	R/W	Description	Reset Value
AC_GLBCTRL	0x5B000000	R/W	AC97 Global Control Register	0x000000

AC_GLBCTRL	Bit	Description	Initial State
Reserved	[31:23]	Reserved.	0x00
Codec ready interrupt enable	[22]	0 : Disable 1 : Enable	0
PCM out channel under run interrupt enable	[21]	0 : Disable 1 : Enable (FIFO is empty)	0
PCM in channel overrun interrupt enable	[20]	0 : Disable 1 : Enable (FIFO is full)	0
Mic in channel overrun nterrupt enable	[19]	0 : Disable 1 : Enable (FIFO is full)	0
PCM out channel threshold interrupt enable	[18]	0 : Disable 1 : Enable (FIFO is half empty)	0
PCM in channel threshold interrupt enable	[17]	0 : Disable 1 : Enable (FIFO is half full)	0
MIC in channel threshold interrupt enable	[16]	0 : Disable 1 : Enable (FIFO is half full)	0
Reserved	[15:14]	Reserved.	00
PCM out channel transfer mode	[13:12]	00 : Off 01 : PIO 10 : DMA 11 : Reserved	00
PCM in channel transfer mode	[11:10]	00 : Off 01 : PIO 10 : DMA 11 : Reserved	00
MIC in channel transfer mode	[9:8]	00 : Off 01 : PIO 10 : DMA 11 : Reserved	00
Reserved	[7:4]	Reserved.	0000
Transfer data enable using AC-link	[3]	0 : Disable 1 : Enable	0
AC-Link on	[2]	0 : Off 1 : SYNC signal transfer to Codec	0
Warm reset	[1]	0 : Normal 1 : Wake up codec from power down	0
Cold reset	[0]	0 : Normal 1 : Reset Codec and Controller logic	0

AC97 GLOBAL STATUS REGISTER (AC_GLBSTAT)

Register	Address	R/W	Description	Reset Value
AC_GLBSTAT	0x5B000004	R	AC97 Global Status Register	0x00000000

AC_GLBSTAT	Bit	Description	Initial State
Reserved	[31:23]	Reserved.	0x00
Codec ready interrupt	[22]	0 : Not requested 1 : Requested	0
PCM out channel under run interrupt	[21]	0 : Not requested 1 : Requested	0
PCM in channel overrun interrupt	[20]	0 : Not requested 1 : Requested	0
MIC in channel overrun interrupt	[19]	0 : Not requested 1 : Requested	0
PCM out channel threshold interrupt	[18]	0 : Not requested 1 : Requested	0
PCM in channel threshold interrupt	[17]	0 : Not requested 1 : Requested	0
MIC in channel threshold interrupt	[16]	0 : Not requested 1 : Requested	0
Reserved	[15:3]	Reserved.	0x000
Controller main state	[2:0]	000 : Idle 001 : Init 010 : Ready 011 : Active 100 : LP 101 : Warm	000

AC97 CODEC COMMAND REGISTER (AC_CODEC_CMD)

Register	Address	R/W	Description	Reset Value
AC_CODEC_ CMD	0x5B000008	R/W	AC97 Codec Command Register	0x00000000

AC_CODEC_ CMD	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
Read enable	[23]	0 : Command write (1) 1 : Status read	0
Address	[22:16]	Codec command address	0x00
Data	[15:0]	Codec command data	0x0000

NOTE: When the commands are written on the AC_CODDEC_CMD register, It is recommended that the delay time between the command and the next command is more than 1 / 48KHz.

AC97 CODEC STATUS REGISTER (AC_CODEC_STAT)

Register	Address	R/W	Description	Reset Value
AC_CODEC_STAT	0x5B00000C	R	AC97 Codec Status Register	0x00000000

AC_CODEC_STAT	Bit	Description	Initial State
Reserved	[31:23]	Reserved.	0x00
Address	[22:16]	Codec status address	0x00
Data	[15:0]	Codec status data	0x0000

NOTES: If you want to read data from AC97 codec register via the AC_CODDEC_STAT register, you should follow the steps.

1. Write command address and data on the AC_CODEC_CMD register with Bit[23] =1.
2. Have a delay time.
3. Read command address and data from AC_CODEC_STAT register.

AC97 PCM OUT/IN CHANNEL FIFO ADDRESS REGISTER (AC_PCMADDR)

Register	Address	R/W	Description	Reset Value
AC_PCMADDR	0x5B000010	R	AC97 PCM Out/In Channel FIFO Address Register	0x00000000

AC_PCMADDR	Bit	Description	Initial State
Reserved	[31:28]	Reserved.	0x0
Out read address	[27:24]	PCM out channel FIFO read address	0x0
Reserved	[23:20]	Reserved.	0x0
In read address	[19:16]	PCM in channel FIFO read address	0x0
Reserved	[15:12]	Reserved.	0x0
Out write address	[11:8]	PCM out channel FIFO write address	0x0
Reserved	[7:4]	Reserved.	0x0
In write address	[3:0]	PCM in channel FIFO write address	0x0

AC97 MIC IN CHANNEL FIFO ADDRESS REGISTER (AC_MICADDR)

Register	Address	R/W	Description	Reset Value
AC_MICADDR	0x5B000014	R	AC97 Mic In Channel FIFO Address Register	0x00000000

AC_MICADDR	Bit	Description	Initial State
Reserved	[31:20]	Reserved.	0x00
Read address	[19:16]	MIC in channel FIFO read address	0x00
Reserved	[15:4]	Reserved.	0x00
Write address	[3:0]	MIC in channel FIFO write address	0x00

AC97 PCM OUT/IN CHANNEL FIFO DATA REGISTER (AC_PCMDATA)

Register	Address	R/W	Description	Reset Value
AC_PCMDATA	0x5B000018	R/W	AC97 PCM Out/In Channel FIFO Data Register	0x00000000

AC_PCMDATA	Bit	Description	Initial State
Right data	[31:16]	PCM out/in right channel FIFO data Read : PCM in right channel Write : PCM out right channel	0x0000
Left data	[15:0]	PCM out/in left channel FIFO data Read : PCM in left channel Write : PCM out left channel	0x0000

AC97 MIC IN CHANNEL FIFO DATA REGISTER (AC_MICDATA)

Register	Address	R/W	Description	Reset Value
AC_MICDATA	0x5B00001C	R/W	AC97 MIC In Channel FIFO Data Register	0x00000000

AC_MICDATA	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0x0000
Mono data	[15:0]	MIC in mono channel FIFO data	0x0000

27 MMC/SD/SDIO CONTROLLER

FEATURES

- SD Memory Card Spec (ver 1.0) / MMC Spec(2.11) compatible
- SDIO Card Spec (Ver 1.0) compatible
- 16 words (64 bytes) FIFO for data Tx/Rx
- 40-bit Command Register
- 136-bit Response Register
- 8-bit Prescaler logic (Freq = System Clock/(P + 1))
- Normal, and DMA data transfer mode(byte, halfword, word transfer)
- DMA burst4 access support(only word transfer)
- 1-bit/4-bit (wide bus) mode & block/stream mode switch support

BLOCK DIAGRAM

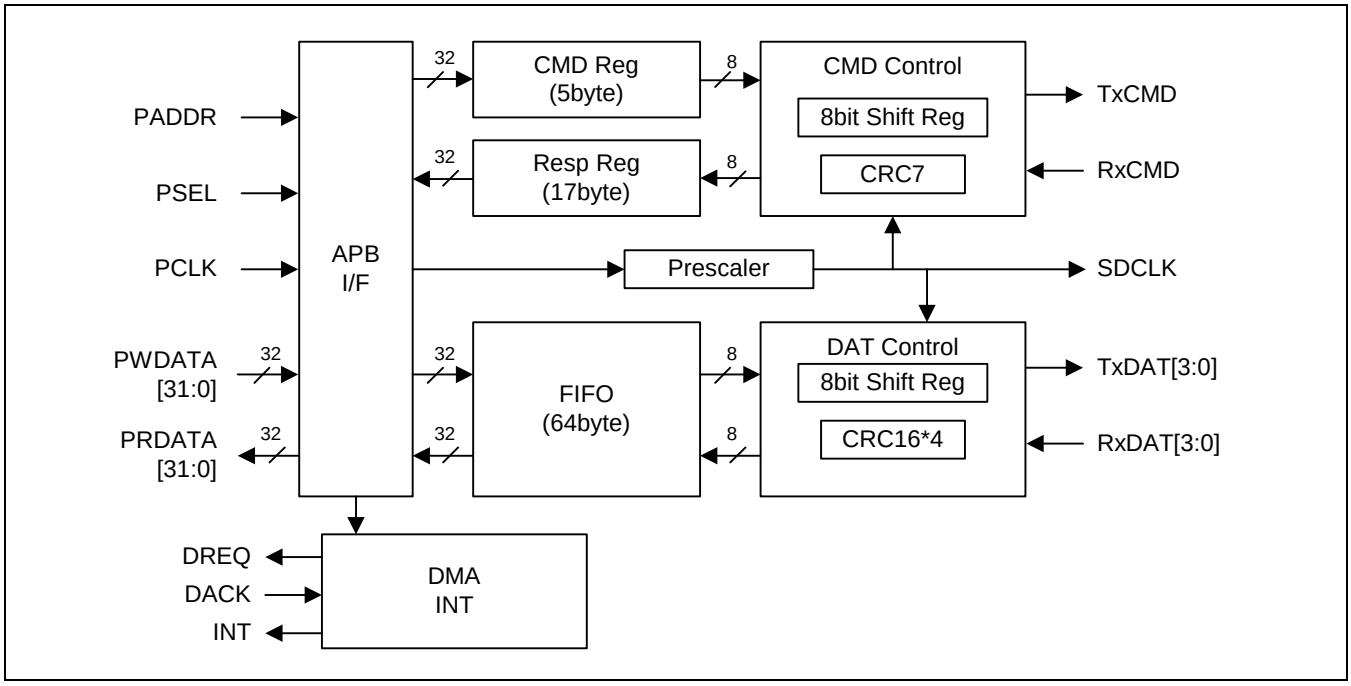


Figure 27-1. SD Interface block diagram

SD OPERATION

A serial clock line synchronizes shifting and sampling of the information on the five data lines. The transmission frequency is controlled by making the appropriate bit settings to the SDIPRE register. You can modify its frequency to adjust the baud rate data register value.

Programming Procedure (common)

To program the SDI modules, follow these basic steps:

1. Set SDICON to configure properly with clock & interrupt enable
2. Set SDIPRE to configure with a proper value.
3. Wait 74 SDCLK clock cycle in order to initialize the card.

CMD Path Programming

1. Write command argument 32bit to SDICmdArg.
2. Determine command types and start command transmit with setting SDICmdCon.
3. Confirm the end of SDI CMD path operation when the specific flag of SDICmdSta is set
4. The flag is CmdSent if command type is no response.
5. The flag is RspFin if command type is with response.
6. Clear the flags of SDICmdSta by writing '1' to the corresponding bit.

DAT Path Programming

1. Write data timeout period to SDIDTimer.
2. Write block size (block length) to SDIBSize(normally 0x80 word).
3. Determine the mode of block, wide bus, dma, etc and start data transfer with setting SDIDatCon.
4. Tx data → Write data to Data Register (SDIDAT) while Tx FIFO is available (TFDET is set), or half (TFHalf is set), or empty(TFEmpty is set).
5. Rx data → Read data from Data Register (SDIDAT) while Rx FIFO is available (RFDET is set), or full (RFFull is set), or half (RFHalf is set), or ready for last data(RFLast is set).
6. Confirm the end of SDI DAT path operation when DatFin flag of SDIDatSta is set
7. Clear the flags of SDIDatSta by writing '1' to the corresponding bit.

SDIO OPERATION

There are two functions of SDIO operation: SDIO Interrupt receiving and Read Wait Request generation. These two functions can operate when RcvIOInt bit and RwaitEn bit of SDICON register is activated respectively. And two functions have the steps and conditions like below.

SDIO Interrupt

In SD 1-bit mode, Interrupt is received through all range from RxDAT[1] pin.

In SD 4-bit mode, RxDAT[1] pin is shared between data receiving and interrupt receiving.
When interrupt detection range(Interrupt Period) is:

1. Single Block: The time between A and B
   – A: 2clocks after the completion of a data packet
   – B: The completion of sending the end bit of the next withdata command
2. Multi Block, PrdType = 0: The time between A and B, restart at C
   – A: 2clocks after the completion of a data packet
   – B: 2clocks after A
   – C: 2clocks after the end bit of the abort command response
3. Multi Block, PrdType = 1: The time between A and B, restart at A
   – A: 2clocks after the completion of a data packet
   – B: 2clocks after A
   – In case of last block, interrupt period begins at A, but not ends at B (CMD53 case)

Read Wait Request

Regardless of 1bit or 4-bit mode, Read Wait Request signal transmits to TxDAT[2] pin in condition of below.

— In read multiple operation, request signal transmission begins at 2clocks after the end of the data block

— Transmission ends when user sets to one RwaitReq bit of SDIDatSta register

SDI SPECIAL REGISTERS

SDI CONTROL REGISTER (SDICON)

Register	Address	R/W	Description	Reset Value
SDICON	0x5A000000	R/W	SDI control register	0x0

SDICON	Bit	Description	Initial Value
Reserved	[31:9]	–	
SDMMC Reset (SDreset)	[8]	Reset whole sdmmc block. This bit is automatically cleared. 0 = Normal mode, 1 = SDMMC reset	0
Reserved	[7:6]		0
Clock Type (CTYP)	[5]	Determines which clock type is used as SDCLK. 0 = SD type, 1 = MMC type	0
Byte Order Type(ByteOrder)	[4]	Determines byte order type when you read(write) data from(to) sd host FIFO with word boundary. 0 = Type A, 1 = Type B	0
Receive SDIO Interrupt from card (RcvIOInt)	[3]	Determines whether sd host receives SDIO Interrupt from the card or not(for SDIO). 0 = Ignore, 1 = Receive SDIO Interrupt	0
Read Wait Enable (RWaitEn)	[2]	Determines read wait request signal generate when sd host waits the next block in multiple block read mode. This bit needs to delay the next block to be transmitted from the card(for SDIO). 0 = Disable(no generate), 1 = Read wait enable(use SDIO)	0
Reserved	[1]		
Clock Out Enable (ENCLK)	[0]	Determines whether SDCLK Out enable or not 0 = Disable (prescaler off), 1 = Clock enable	0

NOTE: Byte Order Type
Type A: (Access by Word) D[7:0] → D[15:8] → D[23:16] → D[31:24]
(Access by Halfword) D[7:0] → D[15:8]
Type B: (Access by Word) D[31:24] → D[23:16] → D[15:8] → D[7:0]
(Access by Halfword) D[15:8] → D[7:0]

SDI BAUD RATE PRESCALER REGISTER (SDIPRE)

Register	Address	R/W	Description	Reset Value
SDIPRE	0x5A000004	R/W	SDI buad rate prescaler register	0x01

SDIPRE	Bit	Description	Initial Value
Prescaler Value	[7:0]	Determines SDI clock(SDCLK) rate as above equation. Baud rate = PCLK / (Prescaler value + 1)	0x01

NOTE: Prescaler Value should be greater than zero.

SDI COMMAND ARGUMENT REGISTER (SDICMDARG)

Register	Address	R/W	Description	Reset Value
SDICmdArg	0x5A000008	R/W	SDI command argument register	0x0

SDICmdArg	Bit	Description	Initial Value
CmdArg	[31:0]	Command argument	0x00000000

SDI COMMAND CONTROL REGISTER (SDICMDCON)

Register	Address	R/W	Description	Reset Value
SDICmdCon	0x5A00000C	R/W	SDI command control register	0x0

SDICommand	Bit	Description	Initial Value
Reserved	[31:13]	–	
Abort Command (AbortCmd)	[12]	Determines whether command type is for abort (for SDIO). 0 = Normal command, 1 = Abort command (CMD12, CMD52)	0
Command with Data (WithData)	[11]	Determines whether command type is with data(for SDIO). 0 = Without data, 1 = With data	0
LongRsp	[10]	Determines whether host receives a 136-bit long response or not 0 = Short response, 1 = Long response	0
WaitRsp	[9]	Determines whether host waits for a response or not 0 = No response, 1 = Wait response	0
Command Start(CMST)	[8]	Determines whether command operation starts or not. . This bit is automatically cleared. 0 = Command ready, 1 = Command start	0
CmdIndex	[7:0]	Command index with start 2-bit (8-bit)	0x00

SDI COMMAND STATUS REGISTER (SDICMDSTA)

Register	Address	R/W	Description	Reset Value
SDICmdSta	0x5A000010	R/(C)	SDI command status register	0x0

SDICmdSta	Bit	Description	Initial Value
Reserved	[31:13]	–	–
Response CRC Fail(RspCrc)	[12] R/C	CRC check failed when command response received. This flag is cleared by setting to one this bit. 0 = Not detect, 1 = CRC fail	0
Command Sent (CmdSent)	[11] R/C	Command sent(not concerned with response). This flag is cleared by setting to one this bit. 0 = Not detect, 1 = Command end	0
Command Time Out (CmdTout)	[10] R/C	Command response timeout (64CLK). This flag is cleared by setting to one this bit. 0 = Not detect, 1 = Timeout	0
Response Receive End (RspFin)	[9] R/C	Command response received. This flag is cleared by setting to one this bit. 0 = Not detect, 1 = Response end	0
CMD line progress On (CmdOn)	[8]	Command transfer in progress 0 = Not detect, 1 = In progress	0
RspIndex	[7:0]	Response index 6-bit with start 2-bit (8-bit)	0x00

SDI RESPONSE REGISTER 0 (SDIRSP0)

Register	Address	R/W	Description	Reset Value
SDIRSP0	0x5A000014	R	SDI response register 0	0x0

SDIRSP0	Bit	Description	Initial Value
Response0	[31:0]	Card status[31:0](short), card status[127:96](long)	0x00000000

SDI RESPONSE REGISTER 1 (SDIRSP1)

Register	Address	R/W	Description	Reset Value
SDIRSP1	0x5A000018	R	SDI response register 1	0x0

SDIRSP1	Bit	Description	Initial Value
RCRC7	[31:24]	CRC7(with end bit, short), card status[95:88](long)	0x00
Response1	[23:0]	unused(short), card status[87:64](long)	0x000000

SDI RESPONSE REGISTER 2 (SDIRSP2)

Register	Address	R/W	Description	Reset Value
SDIRSP2	0x5A00001C	R	SDI Response Register 2	0x0

SDIRSP2	Bit	Description	Initial Value
Response2	[31:0]	unused(short), card status[63:32](long)	0x00000000

SDI RESPONSE REGISTER 3 (SDIRSP3)

Register	Address	R/W	Description	Reset Value
SDIRSP3	0x5A000020	R	SDI response register 3	0x0

SDIRSP3	Bit	Description	Initial Value
Response3	[31:0]	unused(short), card status[31:0](long)	0x00000000

SDI DATA / BUSY TIMER REGISTER (SDIDTIMER)

Register	Address	R/W	Description	Reset Value
SDIDTimer	0x5A000024	R/W	SDI data / busy timer register	0x0

SDIDTimer	Bit	Description	Initial Value
Reserved	[31:23]	–	–
DataTimer	[22:0]	Data / busy timeout period	0x10000

SDI BLOCK SIZE REGISTER (SDIBSIZE)

Register	Address	R/W	Description	Reset Value
SDIBSize	0x5A000028	R/W	SDI block size register	0x0

SDIBSize	Bit	Description	Initial Value
Reserved	[31:12]	–	–
BlkSize	[11:0]	Block size value (0~4095 byte), don't care when stream mode	0x000

NOTE: In Case of multi block, BlkSize must be aligned to word(4byte) size.(BlkSize[1:0] = 00)

SDI DATA CONTROL REGISTER (SDIDATCON)

Register	Address	R/W	Description	Reset Value
SDIDatCon	0x5A00002C	R/W	SDI data control register	0x0

SDIDatCon	Bit	Description	Initial Value
Reserved	[31:25]	–	–
Burst4 enable (Burst4)	[24]	Enable Burst4 mode in DMA mode. This bit should be set only when Data Size is word. 0 = Disable, 1 = Burst4 enable	0
Data Size (DataSize)	[23:22]	Indicates the size of the transfer with FIFO, which is typically byte, halfword or word. 00 = Byte transfer, 01 = Halfword transfer 10 = Word transfer, 11 = Reserved	0
SDIO Interrupt Period Type (PrdType)	[21]	Determines whether SDIO Interrupt period is 2 cycle or extend more cycle when data block last is transferred (for SDIO). 0 = Exactly 2 cycle, 1 = More cycle (likely single block)	0
Transmit After Response (TARSP)	[20]	Determines when data transmit start after response receive or not 0 = Directly after DatMode set, 1 = After response receive (assume DatMode sets to 2'b11)	0
Receive After Command (RACMD)	[19]	Determines when data receive start after command sent or not 0 = Directly after DatMode set, 1 = After command sent (assume DatMode sets to 2'b10)	0
Busy After Command (BACMD)	[18]	Determines when busy receive start after command sent or not 0 = Directly after DatMode set, 1 = After command sent (assume DatMode sets to 2'b01)	0
Block mode (BlkMode)	[17]	Data transfer mode 0 = Stream data transfer, 1 = Block data transfer	0
Wide bus enable (WideBus)	[16]	Determines enable wide bus mode 0 = Standard bus mode(only SDIDAT[0] used), 1 = Wide bus mode(SDIDAT[3:0] used)	0
DMA Enable (EnDMA)	[15]	Enable DMA 0 = Disable(polling), 1 = Dma enable When DMA operation is completed, this bit should be disabled.	0
Data Transfer Start(DTST)	[14]	Determines whether data transfer start or not. . This bit is auto-matically cleared. 0 = Data ready, 1 = Data start	0
Data Transfer Mode (DatMode)	[13:12]	Determines which direction of data transfer 00 = No operation, 01 = Only busy check mode 10 = Data receive mode, 11 = Data transmit mode	00
BlkNum	[11:0]	Block Number (0~4095), don't care when stream mode	0x000

NOTE: If you want one of TARSP, RACMD, BACMD bits(SDIDatCon[20:18]) to "1", you need to write on SDIDatCon register ahead of on SDICmdCon register.(always need for SDIO)

SDI DATA REMAIN COUNTER REGISTER (ADIDATCNT)

Register	Address	R/W	Description	Reset Value
SDIDatCnt	0x5A000030	R	SDI data remain counter register	0x0

SDIDatCnt	Bit	Description	Initial Value
Reserved	[31:24]	–	–
BlkNumCnt	[23:12]	Remaining block number	0x000
BlkCnt	[11:0]	Remaining data byte of 1 block	0x000

SDI DATA STATUS REGISTER (ADIDATSTA)

Register	Address	R/W	Description	Reset Value
SDIDatSta	0x5A000034	R/(C)	SDI data status register	0x0

SDIDatSta	Bit	Description	Initial Value
Reserved	[31:12]	–	–
No busy (NoBusy)	[11] R/C	Busy is not active during 16cycle after cmd packet transmitted in only busy check mode. This flag is cleared by setting to 1 this bit. 0 = Not detect, 1 = No busy signal	0
Read wait request occur (RWaitReq)	[10] R/C	Read wait request signal transmits to sd card. The request signal is stopped and this flag is cleared by setting to one this bit. 0 = Not occur, 1 = Read wait request occur	0
SDIO interrupt detect (IOIntDet)	[9] R/C	SDIO interrupt detect. This flag is cleared by setting to one this bit. 0 = Not detect, 1 = SDIO interrupt detect	0
Reserved	[8]	–	
CRC status fail (CrcSta)	[7] R/C	CRC Status error when data block sent(CRC check failed). This flag is cleared by setting to one this bit. 0 = Not detect, 1 = Crc status fail	0
Data receive CRC fail (DatCrc)	[6] R/C	Data block received error(CRC check failed). This flag is cleared by setting to one this bit. 0 = Not detect, 1 = Receive crc fail	0
Data time out (DatTout)	[5] R/C	Data / Busy receive timeout. This flag is cleared by setting to one this bit. 0 = Not detect, 1 = Timeout	0
Data transfer finish (DatFin)	[4] R/C	Data transfer completes(data counter is zero). This flag is cleared by setting to one this bit. 0 = Not detect, 1 = Data finish detect	0
Busy finish (BusyFin)	[3] R/C	Only busy check finish. This flag is cleared by setting to one this bit 0 = Not detect, 1 = Busy finish detect	0
Reserved	[2]		0
Tx data progress on (TxDatOn)	[1]	Data transmit in progress 0 = Not active, 1 = Data Tx in progress	0
Rx data progress on (RxDatOn)	[0]	Data receive in progress 0 = Not active, 1 = Data Rx in progress	0

SDI FIFO STATUS REGISTER (SDIFSTA)

Register	Address	R/W	Description	Reset Value
SDIFSTA	0x5A000038	R/(C)	SDI FIFO status register	0x0

SDIFSTA	Bit	Description	Initial State
Reserved	[31:16]	–	–
FIFO reset(FRST)	[16] C	Reset FIFO value. This bit is automatically cleared. 0 = Normal mode, 1 = FIFO reset	0
FIFO fail error (FFfail)	[15:14] R/C	FIFO fail error when FIFO occurs overrun / underrun data saving. This flag is cleared by setting to one these bits. 00 = Not detect, 01 = FIFO fail 10 = FIFO fail in the last transfer (only FIFO reset need) 11 = Reserved	0
FIFO available detect for Tx (TFDET)	[13]	This bit indicates that FIFO data is available for transmit when DatMode is data transmit mode. If DMA mode is enable, sd host requests DMA operation. 0 = Not detect(FIFO full), 1 = Detect ($0 \leq$ FIFO ≤ 63)	0
FIFO available detect for Rx (RFDET)	[12]	This bit indicates that FIFO data is available for receive when DatMode is data receive mode. If DMA mode is enable, sd host requests DMA operation. 0 = Not detect(FIFO empty), 1 = Detect ($1 \leq$ FIFO ≤ 64)	0
Tx FIFO half full (TFHalf)	[11]	This bit sets to 1 whenever Tx FIFO is less than 33byte. 0 = $33 \leq$ Tx FIFO ≤ 64, 1 = $0 \leq$ Tx FIFO ≤ 32	0
Tx FIFO empty (TFEmpty)	[10]	This bit sets to 1 whenever Tx FIFO is empty. 0 = $1 \leq$ Tx FIFO ≤ 64, 1 = Empty (0byte)	0
Rx FIFO last data ready (RFLast)	[9] R/C	This bit sets to 1 when Rx FIFO occurs to behave last data of all block. This flag is cleared by setting to one this bit. 0 = Not received yet, 1 = Rx FIFO gets Last data	0
Rx FIFO full (RFFull)	[8]	This bit sets to 1 whenever Rx FIFO is full. 0 = $0 \leq$ Rx FIFO ≤ 63, 1 = Full (64byte)	0
Rx FIFO half full (RFHalf)	[7]	This bit sets to 1 whenever Rx FIFO is more than 31byte. 0 = $0 \leq$ Rx FIFO ≤ 31, 1 = $32 \leq$ Rx FIFO ≤ 64	0
FIFO count (FFCNT)	[6:0]	Number of data(byte) in FIFO	0000000

NOTE: Although the last Rx data size is lager than remained count of FIFO data, you could read this data. If this event happens, you should clear FFfail field, and FIFO reset field

SDI INTERRUPT MASK REGISTER (SDIINTMSK)

Register	Address	R/W	Description	Reset Value
SDIIntMsk	0x5A00003C	R/W	SDI interrupt mask register	0x0

SDIIntMsk	Bit	Description	Initial Value
Reserved	[31:19]	–	–
NoBusy Interrupt Enable (NoBusyInt)	[18]	Determines SDI generate an interrupt if busy signal is not active 0 = Disable, 1 = Interrupt enable	0
RspCrc Interrupt Enable (RspCrcInt)	[17]	Determines SDI generate an interrupt if response CRC check fails 0 = Disable, 1 = Interrupt enable	0
CmdSent Interrupt Enable (CmdSentInt)	[16]	Determines SDI generate an interrupt if command sent(no response required) 0 = Disable, 1 = Interrupt enable	0
CmdTout Interrupt Enable (CmdToutInt)	[15]	Determines SDI generate an interrupt if command response timeout occurs 0 = Disable, 1 = Interrupt enable	0
RspEnd Interrupt Enable (RspEndInt)	[14]	Determines SDI generate an interrupt if command response received 0 = Disable, 1 = Interrupt enable	0
RWaitReq Interrupt Enable (RWReqInt)	[13]	Determines SDI generate an interrupt if read wait request occur. 0 = Disable, 1 = Interrupt enable	0
IOIntDet Interrupt Enable (IntDetInt)	[12]	Determines SDI generate an interrupt if sd host receives SDIO Interrupt from the card(for SDIO). 0 = Disable, 1 = Interrupt enable	0
FFfail Interrupt Enable (FFfailInt)	[11]	Determines SDI generate an interrupt if FIFO fail error occurs 0 = Disable, 1 = Interrupt enable	0
CrcSta Interrupt Enable (CrcStaInt)	[10]	Determines SDI generate an interrupt if CRC status error occurs 0 = Disable, 1 = Interrupt enable	0
DatCrc Interrupt Enable (DatCrcInt)	[9]	Determines SDI generate an interrupt if data receive CRC failed 0 = Disable, 1 = Interrupt enable	0
DatTout Interrupt Enable (DatToutInt)	[8]	Determines SDI generate an interrupt if data receive timeout occurs 0 = Disable, 1 = Interrupt enable	0
DatFin Interrupt Enable (DatFinInt)	[7]	Determines SDI generate an interrupt if data counter is zero 0 = Disable, 1 = Interrupt enable	0

SDI INTERRUPT MASK REGISTER (SDIINTMSK) (Continued)

SDIIntMsk	Bit	Description	Initial Value
BusyFin Interrupt Enable (BusyFinInt)	[6]	Determines SDI generate an interrupt if only busy check completes 0 = Disable, 1 = Interrupt enable	0
Reserved	[5]	–	0
TFHalf Interrupt Enable (TFHalfInt)	[4]	Determines SDI generate an interrupt if Tx FIFO fills half 0 = Disable, 1 = Interrupt enable	0
TFEmpty Interrupt Enable (TFEmptInt)	[3]	Determines SDI generate an interrupt if Tx FIFO is empty 0 = Disable, 1 = Interrupt enable	0
RFLast Interrupt Enable (RFLastInt)	[2]	Determines SDI generate an interrupt if Rx FIFO has last data 0 = Disable, 1 = Interrupt enable	0
RFFull Interrupt Enable (RFFullInt)	[1]	Determines SDI generate an interrupt if Rx FIFO fills full 0 = Disable, 1 = Interrupt enable	0
RFHalf Interrupt Enable (RFHalfInt)	[0]	Determines SDI generate an interrupt if Rx FIFO fills half 0 = Disable, 1 = Interrupt enable	0

SDI DATA REGISTER (SDIDAT)

Register	Address	R/W	Description	Reset Value
SDIDAT	0x5A000040, 44, 48, 4C(Li/W, Li/HW, Li/B, Bi/W) 0x5A000041(Bi/HW), 0x5A000043(Bi/B)	R/W	SDI data register	0x0

SDIDAT	Bit	Description	Initial State
Data Register	[31:0]	This field contains the data to be transmitted or received over the SDI channel	0x00000000

NOTE:

— (Li/W, Li/HW, Li/B): Access by Word/HalfWord//Byte unit when endian mode is Little
— (Bi/W): Access by Word unit when endian mode is Big
— (Bi/HW): Access by HalfWord unit when endian mode is Big
— (Bi/B): Access by Byte unit when endian mode is Big

28 HIGH-SPEED MMC CONTROLLER

OVERVIEW

The HSMMC(High-speed MMC) SDMMC is a combo host for Secure Digital card and MultiMedia Card. This host is compatible for SD Association's (SDA) Host Standard Specification.

You can interface your system with SD card and MMC card. This performance of this host is very powerful, you would get 52Mhz clock rate and access 8-bit data pin simultaneously.

FEATURES

- SD Standard Host Spec(ver 1.0) compatible
- SD Memory Card Spec(ver 2.1) / MMC Memory card Spec(4.2) compatible
- SDIO Card Spec(Ver 1.0) compatible
- 512 bytes FIFO for data Tx/Rx
- 48-bit Command Register
- 136-bit Response Register
- CPU Interface and DMA data transfer mode
- 1-bit / 4-bit / 8-bit mode switch support
- Auto CMD12 support
- Suspend / Resume support
- Read Wait operation support
- Card Interrupt support
- CE-ATA mode support

BLOCK DIAGRAM

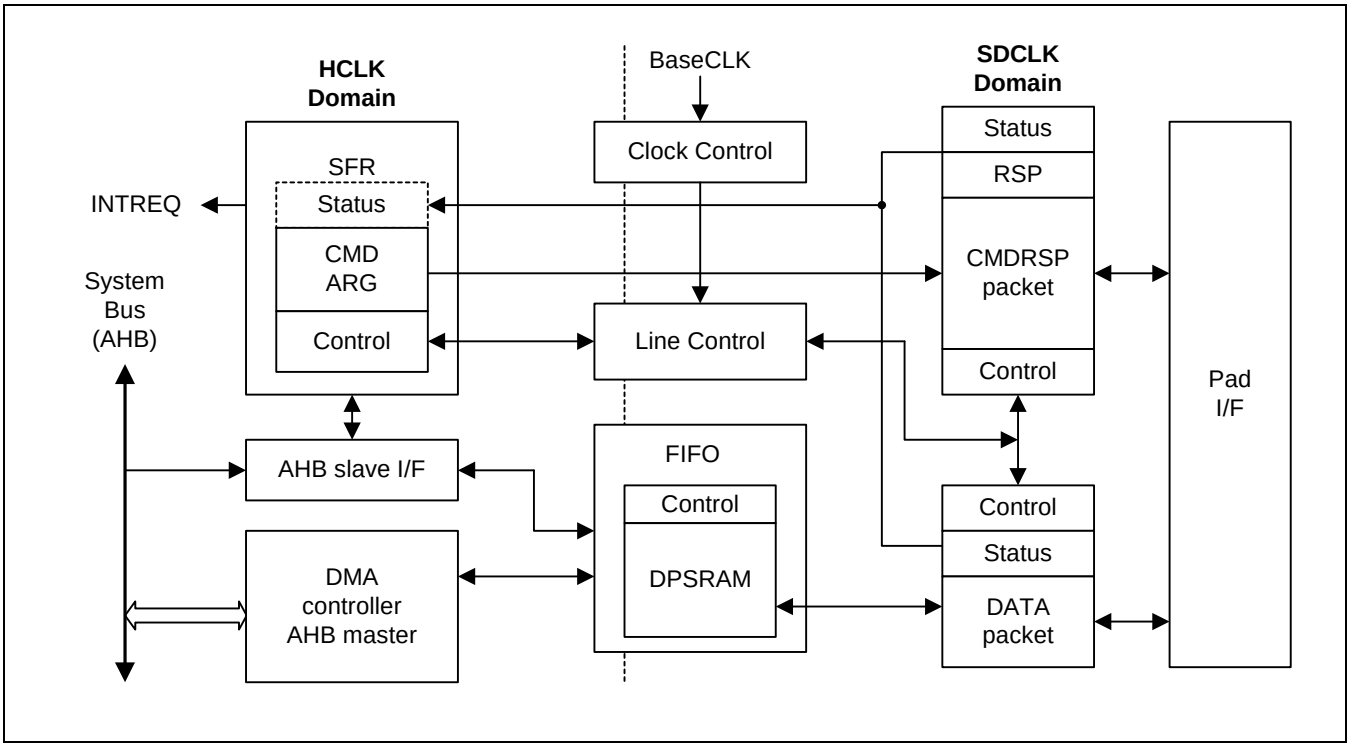


Figure 28-1. HSMMC block diagram

SDI SPECIAL REGISTERS

CONFIGURATION REGISTER TYPES

Configuration register fields are assigned one of the attributes described below :

Register Attribute	Description
RO	Read-only register: Register bits are read-only and cannot be altered by software or any reset operation**.** Writes to these bits are ignored.
ROC	Read-only status : These bits are initialized to zero at reset. Writes to these bits are ignored.
RW or R/W	Read-write register : Register bits are read-write and may be either set or cleared by software to the desired state.
RW1C	Read-only status, Write-1-to-clear status: Register bits indicate status when read, a set bit indicating a status event may be cleared by writing a 1. Writing a 0 to RW1C bits has no effect.
RWAC	Read-Write, automatic clear register: The Host Driver requests a Host Controller operation by setting the bit. The Host Controllers shall clear the bit automatically when the operation of complete. Writing a 0 to RWAC bits has no effect.
HWInit	Hardware Initialized: Register bits are initialized by firmware or hardware mechanisms such as pin strapping or serial EEPROM. Bits are read-only after initialization, and writes to these bits are ignored.
Rsvd or Reserved	Reserved. These bits are initialized to zero, and writes to them are ignored.

SYSTEM ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
SYSAD	0x4A800000	R/W	SDI control register	0x0

This register contains the physical system memory address used for DMA transfers.

Name	Bit	Description	Initial Value
SYSAD	[31:0]	**DMA System Address** This register contains the system memory address for a DMA transfer. When the Host Controller stops a DMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value. The Host Driver shall initialize this register before starting a DMA transaction. After DMA has stopped, the next system address of the next contiguous data position can be read from this register. The DMA transfer waits at the every boundary specified by the **Host DMA Buffer Boundary** in the *Block Size* register. The Host Controller generates **DMA Interrupt** to request the Host Driver to update this register. The Host Driver set the next system address of the next data position to this register. When the most upper byte of this register (003h) is written, the Host Controller restart the DMA transfer. When restarting DMA by the Resume command or by setting **Continue Request** in the *Block Gap Control* register, the Host Controller shall start at the next contiguous address stored here in the *System Address* register.	0x00

BLOCK SIZE REGISTER

This register is used to configure the number of bytes in a data block.

Register	Address	R/W	Description	Reset Value
BLKSIZE	0x4A800004	R/W	Host DMA Buffer Boundary and Transfer Block Size Register	0x0

Name	Bit	Description	Initial Value
	[15]	Reserved	0
	[14:12]	**Host DMA Buffer Boundary** The large contiguous memory space may not be available in the virtual memory system. To perform long DMA transfer, *System Address* register shall be updated at every system memory boundary during DMA transfer. These bits specify the size of contiguous buffer in the system memory. The DMA transfer shall wait at the every boundary specified by these fields and the Host Controller generates the **DMA Interrupt** to request the Host Driver to update the *System Address* register. In case of this register is set to 0 (buffer size = 4K bytes), lower 12-bit of byte address points data in the contiguous buffer and the upper 20-bit points the location of the buffer in the system memory. The DMA transfer stops when the Host Controller detects carry out of the address from bit 11 to 12. These bits shall be supported when the **DMA Support** in the *Capabilities* register is set to 1 and this function is active when the **DMA Enable** in the *Transfer Mode* register is set to 1. 000b = 4K bytes (Detects A11 carry out) 001b = 8K bytes (Detects A12 carry out) 010b = 16K Bytes (Detects A13 carry out) 011b = 32K Bytes (Detects A14 carry out) 100b = 64K bytes (Detects A15 carry out) 101b = 128K Bytes (Detects A16 carry out) 110b = 256K Bytes (Detects A17 carry out) 111b = 512K Bytes (Detects A18 carry rry out)	0
	[11:0]	**Transfer Block Size** This register specifies the block size of data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. Values ranging from 1 up to the maximum buffer size can be set. In case of memory, it shall be set up to 512 bytes. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value, and write operations shall be ignored. 0200h = 512 Bytes 01FFh = 511 Bytes … … 0004h = 4 Bytes 0003h = 3 Bytes 0002h = 2 Bytes 0001h = 1 Byte 0000h = No data transfer	0

BLOCK COUNT REGISTER

This register is used to configure the number of data blocks.

Register	Address	R/W	Description	Reset Value
BLKCNT	0x4A800006	R/W	Blocks Count For Current Transfer	0x0

Name	Bit	Description	Initial Value
	[15:0]	**Blocks Count For Current Transfer** This register is enabled when **Block Count Enable** in the *Transfer Mode* register is set to 1 and is valid only for multiple block transfers. The Host Driver shall set this register to a value between 1 and the maximum block count. The Host Controller decrements the block count after each block transfer and stops when the count reaches zero. Setting the block count to 0 results in no data blocks being transferred. This register should be accessed only when no transaction is executing (i.e., after transactions are stopped). During data transfer, read operations on this register may return an invalid value and write operations are ignored. When saving transfer context as a result of a Suspend command, the number of blocks yet to be transferred can be determined by reading this register. When restoring transfer context prior to issuing a Resume command, the Host Driver shall restore the previously saved block count. FFFFh = 65535 blocks … … 0002h = 2 blocks 0001h = 1 block 0000h = Stop Count	0

ARGUMENT REGISTER

This register contains the SD Command Argument.

Register	Address	R/W	Description	Reset Value
ARGUMENT	0x4A800008	R/W	Command Argument Register	0x0

Name	Bit	Description	Initial Value
ARG	[31:0]	**Command Argument** The SD Command Argument is specified as bit39-8 of Command-Format in the SD Memory Card Physical Layer Specification.	0

TRANSFER MODE REGISTER

This register is used to control the operation of data transfers. The Host Driver shall set this register before issuing a command which transfers data (see **Data Present Select** in the *Command* register), or before issuing a Resume command. The Host Driver shall save the value of this register when the data transfer is suspended (as a result of a Suspend command) and restore it before issuing a Resume command. To prevent data loss, the Host Controller shall implement write protection for this register during data transactions. Writes to this register shall be ignored when the **Command Inhibit (DAT)** in the *Present State* register is 1.

Register	Address	R/W	Description	Reset Value
TRNMOD	0x4A80000C	R/W	Transfer Mode Setting Register	0x0

Name	Bit	Description	Initial Value
	[15:10]	**Reserved**	0
	[9:8]	**Command Completion Signal Control** ‘00’ = No CCS Operation (Normal operation) ’01’ = Read or Write data transfer CCS enable ’10’ = Without data transfer CCS enable ’11’ = Abort Completion Signal (ACS) generation	0
	[7:6]	**Reserved**	0
	[5]	**Multi / Single Block Select** This bit enables multiple block DAT line data transfers. For any other commands, this bit shall be set to 0. If this bit is 0, it is not necessary to set the *Block Count* register. (Refer to Table 2-8) 1 Multiple Block 0 Single Block	0

Name	Bit	Description	Initial Value
	[4]	**Data Transfer Direction Select** This bit defines the direction of DAT line data transfers. The bit is set to 1 by the Host Driver to transfer data from the SD card to the SD Host Controller and it is set to 0 for all other commands. 1 Read (Card to Host) 0 Write (Host to Card)	0
	[3]	**Reserved**	0
	[2]	**Auto CMD12 Enable** Multiple block transfers for memory require CMD12 to stop the transaction. When this bit is set to 1, the Host Controller shall issue CMD12 automatically when last block transfer is completed. The Host Driver shall not set this bit to issue commands that do not require CMD12 to stop data transfer. In particular, secure commands defined in the Part 3 File Security specification do not require CMD12. 1 Enable 0 Disable	0
	[1]	**Block Count Enable** This bit is used to enable the *Block Count* register, which is only relevant for multiple block transfers. When this bit is 0, the *Block Count* register is disabled, which is useful in executing an infinite transfer. (Refer to Table 2-8) 1 Enable 0 Disable	0
	[0]	**DMA Enable** This bit enables DMA functionality as described in section 1.4. DMA can be enabled only if it is supported as indicated in the **DMA Support** in the *Capabilities* register. If DMA is not supported, this bit is meaningless and shall always read 0. If this bit is set to 1, a DMA operation shall begin when the Host Driver writes to the upper byte of *Command* register (00Fh). 1 Enable 0 Disable	0

Table below shows the summary of how register settings determine types of data transfer.

Table 28-1. Determination of Transfer Type

Multi/Single Block Select	Block Count Enable	*Block Count*	Function
0	Don't care	Don't care	Single Transfer
1	0	Don't care	Infinite Transfer
1	1	Not Zero	Multiple Transfer
1	1	Zero	Stop Multiple Transfer

NOTE: For CE-ATA access, (Auto) CMD12 should be issued after Command Completion Signal Disable

COMMAND REGISTER

This register contains the SD Command Argument.

Register	Address	R/W	Description	Reset Value
CMDREG	0x4A80000E	R/W	Command Register	0x0

The Host Driver shall check the **Command Inhibit (DAT)** bit and **Command Inhibit (CMD)** bit in the *Present State* register before writing to this register. Writing to the upper byte of this register triggers SD command generation. The Host Driver has the responsibility to write this register because the Host Controller does not protect for writing when **Command Inhibit (CMD)** is set.

Name	Bit	Description	Initial Value
	[15:14]	**Reserved**	
	[13:8]	**Command Index** These bits shall be set to the command number (CMD0-63, ACMD0-63) that is specified in bits 45-40 of the Command-Format in the SD Memory Card Physical Layer Specification and SDIO Card Specification.	
	[7:6]	**Command Type** There are three types of special commands: Suspend, Resume and Abort. These bits **shall** be set to 00b for all other commands. • Suspend Command If the Suspend command succeeds, the Host Controller shall assume the SD Bus has been released and that it is possible to issue the next command which uses the ***DAT*** line. The Host Controller shall de-assert Read Wait for read transactions and stop checking busy for write transactions. The interrupt cycle shall start, in 4-bit mode. If the Suspend command fails, the Host Controller shall maintain its current state, and the Host Driver shall restart the transfer by setting **Continue Request** in the *Block Gap Control* register. (Refer to Suspend Sequence section) • Resume Command The Host Driver re-starts the data transfer by restoring the registers in the range of 000-00Dh. (Refer to Figure 1-4 in section 1.6 for the register map.) The Host Controller shall check for busy before starting write transfers. • Abort Command If this command is set when executing a read transfer, the Host Controller shall stop reads to the buffer. If this command is set when executing a write transfer, the Host Controller shall stop driving the ***DAT*** line. After issuing the Abort command, the Host Driver should issue a software reset. (Refer to Abort Transaction) 11b = Abort CMD12, CMD52 for writing “I/O Abort” in CCCR 10b = Resume CMD52 for writing “Function Select” in CCCR 01b = Suspend CMD52 for writing “Bus Suspend” in CCCR 00b = Normal Other commands	

Name	Bit	Description	Initial Value
	[5]	**Data Present Select** This bit is set to 1 to indicate that data is present and shall be transferred using the ***DAT*** line. It is set to 0 for the following: (1) Commands using only ***CMD*** line (ex. CMD52). (2) Commands with no data transfer but using busy signal on ***DAT***[0] line (R1b or R5b ex. CMD38) (3) Resume command 1 = Data Present 0 = No Data Present	
	[4]	**Command Index Check Enable** If this bit is set to 1, the Host Controller shall check the Index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked. 1 = Enable 0 = Disable	
	[3]	**Command CRC Check Enable** If this bit is set to 1, the Host Controller shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. The number of bits checked by the CRC field value changes according to the length of the response. (Refer to D01-00 and Table 2-10 below.) 1 = Enable 0 = Disable	
	[2]	**Reserved**	
	[1:0]	**Response Type Select** 00 = No Response 01 = Response Length 136 10 = Response Length 48 11 = Response Length 48 check Busy after response	

Table 28-2. Relation Between Parameters and the Name of Response Type

Response Type	Index Check Enable	CRC Check Enable	Name of Response Type
00	0	0	No Response
01	0	1	R2
10	0	0	R3, R4
10	1	1	R1, R6, R5
11	1	1	R1b, R5b

These bits determine Response types.

NOTES:
1. In the SDIO specification, response type notation of R5b is not defined. R5 includes R5b in the SDIO specification. But R5b is defined in this specification to specify the Host Controller shall check busy after receiving response. For example, usually CMD52 is used as R5 but I/O abort command shall be used as R5b.
2. For CMD52 to read BS after writing "Bus Suspend," Command Type should be "Suspend" as well.

RESPONSE REGISTER

This register is used to store responses from SD cards.

Register	Address	R/W	Description	Reset Value
RSPREG0	0x4A800010	ROC	Response Register 0	0x0
RSPREG1	0x4A800014	ROC	Response Register 1	0x0
RSPREG2	0x4A800018	ROC	Response Register 2	0x0
RSPREG3	0x4A80001C	ROC	Response Register 3	0x0

Name	Bit	Description	Initial Value
	[127:0]	**Command Response** The Table below describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the *Response* register. 128-bit Response bit order: {RSPREG3, RSPREG2, RSPREG1, RSPREG0}	

Table 28-3. Response Bit Definition for Each Response Type.

Kind of Response	Meaning of Response	Response Field	Response Register
R1, R1b (normal response)	Card Status	R [39:8]	REP [31:0]
R1b (Auto CMD12 response)	Card Status for Auto CMD12	R [39:8]	REP [127:96]
R2 (CID, CSD register)	CID or CSD reg. incl.	R [127:8]	REP [119:0]
R3 (OCR register)	OCR register for memory	R [39:8]	REP [31:0]
R4 (OCR register)	OCR register for I/O etc	R [39:8]	REP [31:0]
R5,R5b	SDIO response	R [39:8]	REP [31:0]
R6 (Published RCA response)	New published RCA[31:16] etc	R [39:8]	REP [31:0]

The Response Field indicates bit positions of “Responses” defined in the PHYSICAL LAYER SPECIFICATION Version 1.01. The Table (upper) shows that most responses with a length of 48 (R[47:0]) have 32 bits of the response data (R[39:8]) stored in the *Response* register at REP[31:0]. Responses of type R1b (Auto CMD12 responses) have response data bits R[39:8] stored in the *Response* register at REP[127:96]. Responses with length 136 (R[135:0]) have 120 bits of the response data (R[127:8]) stored in the *Response* register at REP[119:0].

To be able to read the response status efficiently, the Host Controller only stores part of the response data in the *Response* register. This enables the Host Driver to efficiently read 32 bits of response data in one read cycle on a 32-bit bus system. Parts of the response, the Index field and the CRC, are checked by the Host Controller (as specified by the **Command Index Check Enable** and the **Command CRC Check Enable** bits in the *Command* register) and generate an error interrupt if an error is detected. The bit range for the CRC check depends on the response length. If the response length is 48, the Host Controller shall check R[47:1], and if the response length is 136 the Host Controller shall check R[119:1].

Since the Host Controller may have a multiple block data DAT line transfer executing concurrently with a CMD_wo_DAT command, the Host Controller stores the Auto CMD12 response in the upper bits (REP[127:96]) of the *Response* register. The CMD_wo_DAT response is stored in REP[31:0]. This allows the Host Controller to avoid overwriting the Auto CMD12 response with the CMD_wo_DAT and vice versa.

When the Host Controller modifies part of the *Response* register, as shown in the Table above, it shall preserve the unmodified bits.

BUFFER DATA PORT REGISTER

32-bit data port register to access internal buffer.

Register	Address	R/W	Description	Reset Value
BDATA	0x4A800020	R/W	Buffer Data Register	0x0

Name	Bit	Description	Initial Value
		Buffer Data The Host Controller buffer can be accessed through this 32-bit *Data Port* register.	0

Detailed documents are to be copied from SD Host Standard Spec.

PRESENT STATE REGISTER

This register contains the SD Command Argument.

Register	Address	R/W	Description	Reset Value
PRNSTS	0x4A800024	RO/ROC	Present State Register	0x0

Name	Bit	Description	Initial Value
	[31:25]	**Reserved**	0
	[24]	**CMD Line Signal Level** (RO) This status is used to check the ***CMD*** line level to recover from errors, and for debugging. Note : ***CMD*** port is mapped to ***SD0_CMD*** pin	0
	[23:20]	**DAT[3:0] Line Signal Level** (RO) This status is used to check the ***DAT*** line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from ***DAT***[0]. D23 : DAT[3] D22 : DAT[2] D21 : DAT[1] D20 : DAT[0] Note : ***DAT*** port is mapped to ***SD0_DAT*** pin	Line State
	[19]	**Write Protect Switch Pin Level** (RO) The Write Protect Switch is supported for memory and combo cards. This bit reflects the ***SDWP#*** pin. 1 = Write enabled (***SDWP#***=1) 0 = Write protected (***SDWP#***=0) Note : ***SDWP#*** port is mapped to ***SD0_nWP*** pin	Line State

Name	Bit	Description	Initial Value
	[18]	**Card Detect Pin Level** (RO) This bit reflects the inverse value of the ***SDCD#*** pin. Debouncing is not performed on this bit. This bit may be valid when **Card State Stable** is set to 1, but it is not guaranteed because of propagation delay. Use of this bit is limited to testing since it must be debounced by software. 1 = Card present (***SDCD#***=0) 0 = No card present (***SDCD#***=1) Note : ***SDCD#*** port is mapped to ***SD0_nCD*** pin	Line State
	[17]	**Card State Stable** (RO) This bit is used for testing. If it is 0, the **Card Detect Pin Level** is not stable. If this bit is set to 1, it means the **Card Detect Pin Level** is stable. No Card state can be detected by this bit is set to 1 and **Card Inserted** is set to 0. The **Software Reset For All** in the *Software Reset* register shall not affect this bit. 1 = No Card or Inserted 0 = Reset or Debouncing	0
	[16]	**Card Inserted** (RO) This bit indicates whether a card has been inserted. The Host Controller shall debounce this signal so that the Host Driver will not need to wait for it to stabilize. Changing from 0 to 1 generates a **Card Insertion** interrupt in the *Normal Interrupt Status* register and changing from 1 to 0 generates a **Card Removal** interrupt in the *Normal Interrupt Status* register. The **Software Reset For All** in the *Software Reset* register shall not affect this bit. If a card is removed while its power is on and its clock is oscillating, the Host Controller shall clear **SD Bus Power** in the *Power Control* register and **SD Clock Enable** in the *Clock Control* register. When this bit is changed from 1 to 0, the Host Controller shall immediately stop driving ***CMD*** and ***DAT[3:0]*** (tri-state). In addition, the Host Driver should clear the Host Controller by the **Software Reset For All** in *Software Reset* register. The card detect is active regardless of the **SD Bus Power**. 1 = Card Inserted 0 = Reset or Debouncing or No Card	0
	[15:14]	**Reserved**	
DIFF4W	[13]	**FIFO Pointer Difference 4-Word (ROC)** When the difference of the address pointer between AHB side and SD side is more than or equal to 4-word, this status bit is set to HIGH. When others clears automatically. Write(Tx) mode : when this bit is HIGH, more than or equal to 4-word can be written by CPU side. Read(Rx) mode : when this bit is HIGH, more than or equal to 4-word can be read by CPU side.	0

Name	Bit	Description	Initial Value
DIFF1W	[12]	**FIFO Pointer Difference 1-Word (ROC)** When the difference of the address pointer between AHB side and SD side is more than or equal to 1-word, this status bit is set to HIGH. When others clears automatically. Write(Tx) mode : when this bit is HIGH, more than or equal to 1-word can be written by CPU side. Read(Rx) mode : when this bit is HIGH, more than or equal to 1-word can be read by CPU side.	0
	[11]	**Buffer Read Enable** (ROC) This status is used for non-DMA read transfers. The Host Controller may implement multiple buffers to transfer data efficiently. This read only flag indicates that valid data exists in the host side buffer status. If this bit is 1, readable data exists in the buffer. A change of this bit from 1 to 0 occurs when all the block data is read from the buffer. A change of this bit from 0 to 1 occurs when block data is ready in the buffer and generates the **Buffer Read Ready** interrupt. 1 = Read enable 0 = Read disable	0
	[10]	**Buffer Write Enable** (ROC) This status is used for non-DMA write transfers. The Host Controller can implement multiple buffers to transfer data efficiently. This read only flag indicates if space is available for write data. If this bit is 1, data can be written to the buffer. A change of this bit from 1 to 0 occurs when all the block data is written to the buffer. A change of this bit from 0 to 1 occurs when top of block data can be written to the buffer and generates the **Buffer Write Ready** interrupt. 1 = Write enable 0 = Write disable	0
	[9]	**Read Transfer Active** (ROC) This status is used for detecting completion of a read transfer. This bit is set to 1 for either of the following conditions: (1) After the end bit of the read command. (2) When writing a 1 to **Continue Request** in the *Block Gap Control* register to restart a read transfer. This bit is cleared to 0 for either of the following conditions:: (1) When the last data block as specified by block length is transferred to the System. (2) When all valid data blocks have been transferred to the System and no current block transfers are being sent as a result of the **Stop At Block Gap Request** being set to 1. **A Transfer Complete** interrupt is generated when this bit changes to 0. 1 = Transferring data 0 = No valid data	0

Name	Bit	Description	Initial Value
	[8]	**Write Transfer Active** (ROC) This status indicates a write transfer is active. If this bit is 0, it means no valid write data exists in the Host Controller. Refer to Section 3.11.4 for more details on the sequence of events. This bit is set in either of the following cases: (1) After the end bit of the write command. (2) When writing a 1 to **Continue Request** in the *Block Gap Control* register to restart a write transfer. This bit is cleared in either of the following cases: (1) After getting the CRC status of the last data block as specified by the transfer count (Single and Multiple) (2) After getting the CRC status of any block where data transmission is about to be stopped by a **Stop At Block Gap Request**. During a write transaction, a **Block Gap Event** interrupt is generated when this bit is changed to 0, as result of the **Stop At Block Gap Request** being set. This status is useful for the Host Driver in determining when to issue commands during write busy. 1 = Transferring data 0 = No valid data	0
	[7:3]	**Reserved**	0

Name	Bit	Description	Initial Value
	[2]	**DAT Line Active** (ROC) This bit indicates whether one of the DAT line on SD Bus is in use. **(a) In the case of read transactions** This status indicates if a read transfer is executing on the SD Bus. Changes in this value from 1 to 0 between data blocks generates a Block Gap Event interrupt in the Normal Interrupt Status register. This bit shall be set in either of the following cases: (1) After the end bit of the read command. (2) When writing a 1 to Continue Request in the Block Gap Control register to restart a read transfer. This bit shall be cleared in either of the following cases: (1) When the end bit of the last data block is sent from the SD Bus to the Host Controller. (2) When beginning a wait read transfer at a stop at the block gap initiated by a Stop At Block Gap Request. The Host Controller shall wait at the next block gap by driving Read Wait at the start of the interrupt cycle. If the Read Wait signal is already driven (data buffer cannot receive data), the Host Controller can wait for current block gap by continuing to drive the Read Wait signal. It is necessary to support Read Wait in order to use the suspend / resume function. **(b) In the case of write transactions** This status indicates that a write transfer is executing on the SD Bus. Changes in this value from 1 to 0 generate a Transfer Complete interrupt in the Normal Interrupt Status register. This bit shall be set in either of the following cases: (1) After the end bit of the write command. (2) When writing to 1 to Continue Request in the Block Gap Control register to continue a write transfer. This bit shall be cleared in either of the following cases: (1) When the SD card releases write busy of the last data block the Host Controller shall also detect if output is not busy. If SD card does not drive busy signal for 8 SD Clocks, the Host Controller shall consider the card drive “Not Busy”. (2) When the SD card releases write busy prior to waiting for write transfer as a result of a Stop At Block Gap Request. 1 = DAT Line Active 0 = DAT Line Inactive	0

Name	Bit	Description	Initial Value
	[1]	**Command Inhibit (DAT)** (ROC) (ROC) This status bit is generated if either the **DAT Line Active** or the **Read Transfer Active** is set to 1. If this bit is 0, it indicates the Host Controller can issue the next SD Command. Commands with busy signal belong to **Command Inhibit (DAT)** (ex. R1b, R5b type). Changing from 1 to 0 generates a **Transfer Complete** interrupt in the *Normal Interrupt Status* register. Note: The SD Host Driver can save registers in the range of 000-00Dh for a suspend transaction after this bit has changed from 1 to 0. 1 = Cannot issue command which uses the ***DAT*** line 0 = Can issue command which uses the ***DAT*** line	0
	[0]	**Command Inhibit (CMD)** (ROC) If this bit is 0, it indicates the ***CMD*** line is not in use and the Host Controller can issue a SD Command using the ***CMD*** line. This bit is set immediately after the *Command* register (00Fh) is written. This bit is cleared when the command response is received. Even if the **Command Inhibit (DAT)** is set to 1, Commands using only the ***CMD*** line can be issued if this bit is 0. Changing from 1 to 0 generates a **Command** **Complete** interrupt in the *Normal Interrupt Status* register. If the Host Controller cannot issue the command because of a command conflict error (Refer to **Command CRC Error**) or because of **Command Not Issued By Auto CMD12 Error**, this bit shall remain 1 and the **Command Complete** is not set. Status issuing Auto CMD12 is not read from this bit. 1 = Cannot issue commandb 0 = Can issue command using only ***CMD*** line	0

NOTE: Buffer Write Enable in Present register should not be asserted for DMA transfers since it generates Buffer Write Ready interrupt

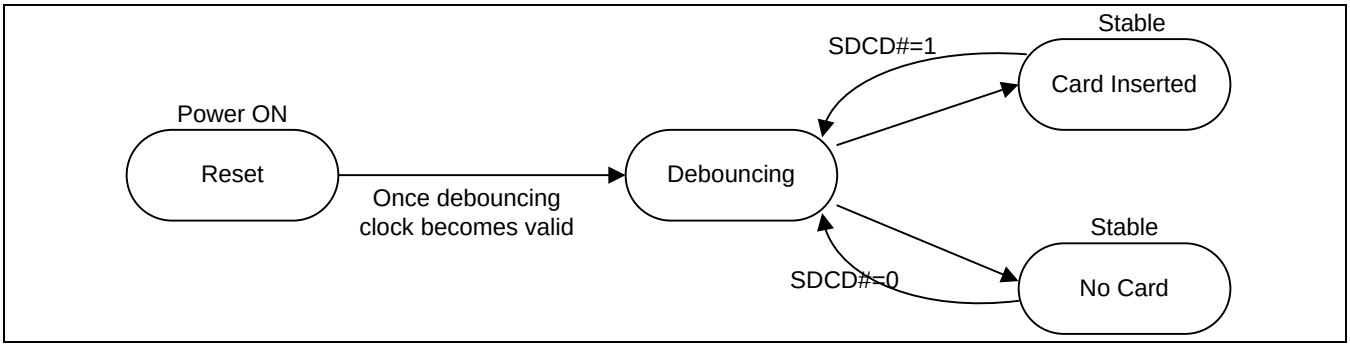


Figure 28-2. Card Detect State

Upper figure shows the state definitions of hardware that handles “Debouncing”.

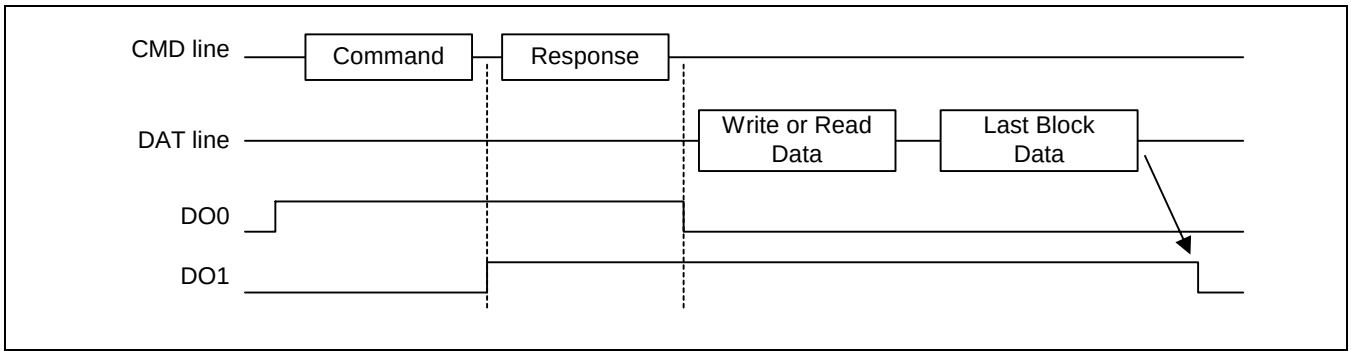


Figure 28-3. Timing of Command Inhibit (DAT) and Command Inhibit (CMD) with data transfer

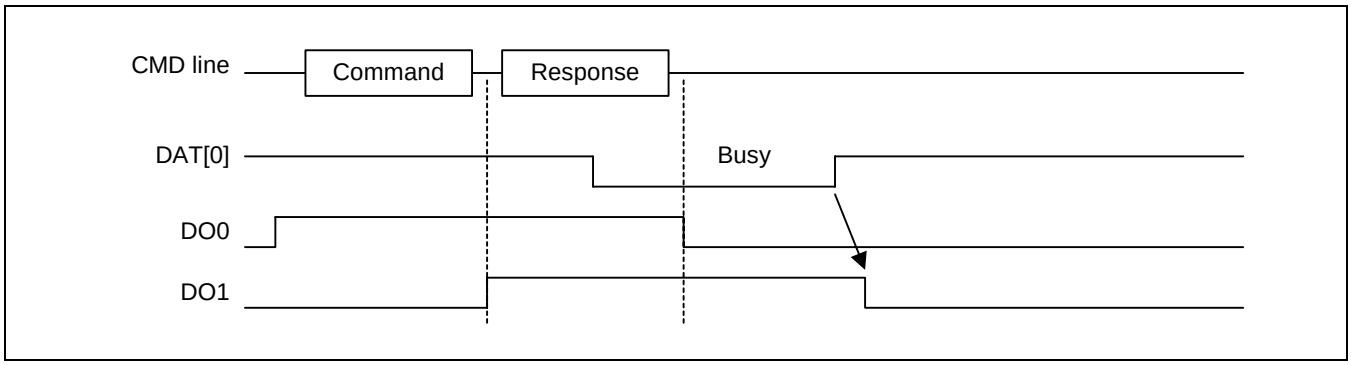


Figure 28-4. Timing of Command Inhibit (DAT) for the case of response with busy

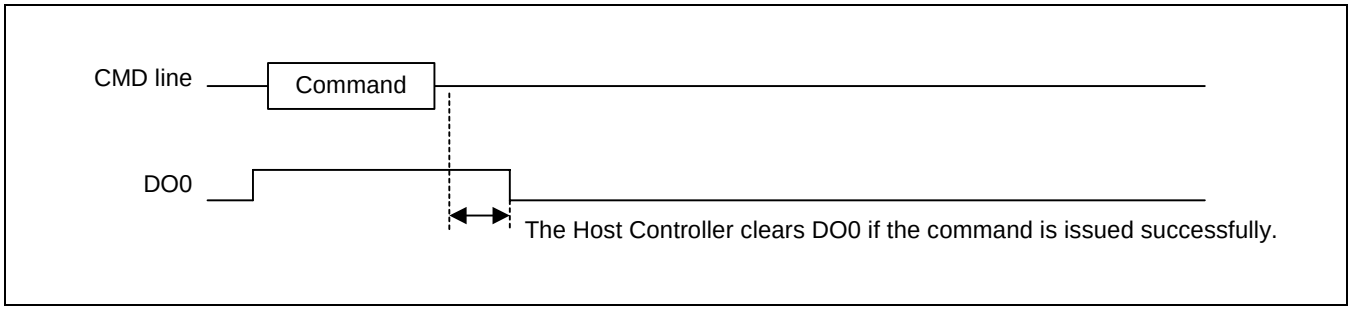


Figure 28-5. Timing of Command Inhibit (CMD) for the case of no response command

HOST CONTROL REGISTER

This register contains the SD Command Argument.

Register	Address	R/W	Description	Reset Value
HOSTCTL	0x4A800028	R/W	Present State Register	0x0

Name	Bit	Description	Initial Value
CDSig Sel	[7]	**Card Detect Signal Selection** This bit selects source for the card detection. '1' = The Card Detect Test Level is selected (for test purpose) '0' = SDCD# is selected (for normal use)	0
CDTest Lvl	[6]	**Card Detect Test Level** This bit is enabled while the Card Detect Signal Selection is set to 1 and it indicates card inserted or not. '1' = Card Inserted '0' = No Card	0
Wide8	[5]	**Extended Data Transfer Width** (It is for MMC 8bit card.) '1' = 8 bit operation '0' = the bit width is designated by the bit 1 (Data Transfer Width)	0
	[4:3]	**Reserved**	0
	[2]	**High Speed Enable** This bit is optional. Before setting this bit, the Host Driver shall check the **High Speed Support** in the *Capabilities* register. If this bit is set to 0 (default), the Host Controller outputs ***CMD*** line and ***DAT*** lines at the falling edge of the SD Clock (up to 25MHz). If this bit is set to 1, the Host Controller outputs ***CMD*** line and ***DAT*** lines at the rising edge of the SD Clock (up to 50MHz). '1' = High Speed mode '0' = Normal Speed mode	0
	[1]	**Data Transfer Width** This bit selects the data width of the Host Controller. The Host Driver shall set it to match the data width of the SD card. '1' = 4-bit mode '0' = 1-bit mode	0
	[0]	**LED Control** This bit is used to caution the user not to remove the card while the SD card is being accessed. If the software is going to issue multiple SD commands, this bit can be set during all these transactions. It is not necessary to change for each transaction. '1' = LED on '0' = LED off Note : ***LED*** port is mapped to ***SD0_LED*** pin	0

NOTE: Card Detect Pin Level does not simply reflect SDCD# pin, but chooses from SDCD, DAT[3], or CDTestlvl depending on CDSSigSel and SDCDSel values.

POWER CONTROL REGISTER

This register contains the SD Command Argument.

Register	Address	R/W	Description	Reset Value
PWRCON	0x4A800029	R/W	Present State Register	0x0

Name	Bit	Description	Initial Value
	[7:4]	Reserved	
	[3:1]	**SD Bus Voltage Select** By setting these bits, the Host Driver selects the voltage level for the SD card. Before setting this register, the Host Driver shall check the **Voltage Support** bits in the *Capabilities* register. If an unsupported voltage is selected, the Host System shall not supply SD Bus voltage. '111b' = 3.3V (Typ.) '110b' = 3.0V (Typ.) '101b' = 1.8V (Typ.) '100b' – '000b' = Reserved	0
	[0]	**SD Bus Power** Before setting this bit, the SD Host Driver shall set **SD Bus Voltage Select**. If the Host Controller detects the No Card state, this bit shall be cleared. If this bit is cleared, the Host Controller shall immediately stop driving ***CMD*** and ***DAT[3:0]*** (tri-state) and drive ***SDCLK*** to low level. '1' = Power on '0' = Power off	0

BLOCK GAP CONTROL REGISTER

This register contains the SD Command Argument.

Register	Address	R/W	Description	Reset Value
BLKGAP	0x4A80002A	R/W	Block Gap Control Register	0x0

Name	Bit	Description	Initial Value
	[7:4]	Reserved	0
	[3]	**Interrupt At Block Gap** This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. Setting to 0 disables interrupt detection during a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the Host Driver detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. (RW) '1' = Enabled '0' = Disabled	0
	[2]	**Read Wait Control** The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using the ***DAT***[2] line. Otherwise the Host Controller has to stop the SD Clock to hold read data, which restricts commands generation. When the Host Driver detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. If the card does not support read wait, this bit shall never be set to 1 otherwise ***DAT*** line conflict may occur. If this bit is set to 0, Suspend/Resume cannot be supported. (RW) '1' = Enable Read Wait Control '0' = Disable Read Wait Control	0
	[1]	**Continue Request** This bit is used to restart a transaction which was stopped using the **Stop At Block Gap Request**. To cancel stop at the block gap, set **Stop At Block Gap Request** to 0 and set this bit 1 to restart the transfer. The Host Controller automatically clears this bit in either of the following cases: (1) In the case of a read transaction, the **DAT Line Active** changes from 0 to 1 as a read transaction restarts. (2) In the case of a write transaction, the **Write Transfer Active** changes from 0 to 1 as the write transaction restarts. Therefore it is not necessary for Host Driver to set this bit to 0. If **Stop At Block Gap Request** is set to 1, any write to this bit is ignored. (RWAC) '1' = Restart '0' = Not affect	0

Name	Bit	Description	Initial Value
	[0]	**Stop At Block Gap Request** This bit is used to stop executing a transaction at the next block gap for both DMA and non-DMA transfers. Until the **Transfer Complete** is set to 1, indicating a transfer completion the Host Driver shall leave this bit set to 1. Clearing both the **Stop At Block Gap Request** and **Continue Request** shall not cause the transaction to restart. Read Wait is used to stop the read transaction at the block gap. The Host Controller shall honor **Stop At Block Gap Request** for write transfers, but for read transfers it requires that the SD card support Read Wait. Therefore the Host Driver shall not set this bit during read transfers unless the SD card supports Read Wait and has set **Read Wait Control** to 1. In the case of write transfers in which the Host Driver writes data to the *Buffer Data Port* register, the Host Driver shall set this bit after all block data is written. If this bit is set to 1, the Host Driver shall not write data to *Buffer Data Port* register. This bit affects **Read Transfer Active**, **Write Transfer Active**, **DAT Line Active** and **Command Inhibit (DAT)** in the *Present State* register. Regarding detailed control of bits D01 and D00. (RW) '1' = Stop '0' = Transfer	0

There are three cases to restart the transfer after stop at the block gap. Which case is appropriate depends on whether the Host Controller issues a Suspend command or the SD card accepts the Suspend command.

(1) If the Host Driver does not issue a Suspend command, the **Continue Request** shall be used to restart the transfer.

(2) If the Host Driver issues a Suspend command and the SD card accepts it, a Resume command shall be used to restart the transfer.

(3) If the Host Driver issues a Suspend command and the SD card does not accept it, the **Continue Request** shall be used to restart the transfer.

Any time **Stop At Block Gap Request** stops the data transfer, the Host Driver shall wait for **Transfer Complete** (in the *Normal Interrupt Status* register) before attempting to restart the transfer. When restarting the data transfer by **Continue Request**, the Host Driver shall clear **Stop At Block Gap Request** before or simultaneously.

NOTE:

After setting **Stop At Block Gap Request** field, which should not be cleared unless Block Gap Event or Transfer Complete interrupt occurs. Otherwise, the module hangs.

WAKEUP CONTROL REGISTER

This register is mandatory for the Host Controller, but wakeup functionality depends on the Host Controller system hardware and software. The Host Driver shall maintain voltage on the SD Bus, by setting **SD Bus Power** to 1 in the *Power Control* register, when wakeup event via Card Interrupt is desired.

Register	Address	R/W	Description	Reset Value
WAKCON	0x4A80002B	R/W	Wakeup Control Register	0x0

Name	Bit	Description	Initial Value
	[7:3]	Reserved	0
	[2]	**Wakeup Event Enable On SD Card Removal** This bit enables wakeup event via **Card Removal** assertion in the *Normal Interrupt Status* register. **FN_WUS** (Wake Up Support) in CIS does not affect this bit. (RW) '1' = Enable '0' = Disable	0
	[1]	**Wakeup Event Enable On SD Card Insertion** This bit enables wakeup event via **Card Insertion** assertion in the *Normal Interrupt Status* register. **FN_WUS** (Wake Up Support) in CIS does not affect this bit. (RW) '1' = Enable '0' = Disable	0
	[0]	**Wakeup Event Enable On Card Interrupt** This bit enables wakeup event via **Card Interrupt** assertion in the *Normal Interrupt Status* register. This bit can be set to 1 if **FN_WUS** (Wake Up Support) in CIS is set to 1. (RW) '1' = Enable '0' = Disable	0

CLOCK CONTROL REGISTER

At the initialization of the Host Controller, the Host Driver shall set the **SDCLK Frequency Select** according to the *Capabilities* register.

Register	Address	R/W	Description	Reset Value
CLKCON	0x4A80002C	R/W	Command Register	0x0

Name	Bit	Description	Initial Value
	[15:8]	**SDCLK Frequency Select** This register is used to select the frequency of ***SDCLK*** pin. The frequency is not programmed directly; rather this register holds the divisor of the **Base Clock Frequency For SD Clock** in the *Capabilities* register. Only the following settings are allowed. 80h: base clock divided by 256 40h: base clock divided by 128 20h: base clock divided by 64 10h: base clock divided by 32 08h: base clock divided by 16 04h: base clock divided by 8 02h: base clock divided by 4 01h: base clock divided by 2 00h: base clock (10MHz-63MHz) Setting 00h specifies the highest frequency of the SD Clock. When setting multiple bits, the most significant bit is used as the divisor. But multiple bits should not be set. The two default divider values can be calculated by the frequency that is defined by the **Base Clock Frequency For SD Clock** in the *Capabilities* register. (1) 25MHz divider value (2) 400KHz divider value According to the SD Physical Specification Version 1.01 and the SDIO Card Specification Version 1.0, maximum SD Clock frequency is 25MHz, and shall never exceed this limit. The frequency of SDCLK is set by the following formula: Clock Frequency = (Base Clock) / divisor Thus, choose the smallest possible divisor which results in a clock frequency that is less than or equal to the target frequency. For example, if the **Base Clock Frequency For SD Clock** in the *Capabilities* register has the value 33MHz, and the target frequency is 25MHz, then choosing the divisor value of 01h will yield 16.5MHz, which is the nearest frequency less than or equal to the target. Similarly, to approach a clock value of 400KHz, the divisor value of 40h yields the optimal clock value of 258KHz.	0
	[7:4]	**Reserved**	

Name	Bit	Description	Initial Value
	[3]	**External Clock Stable** This bit is set to 1 when SD Clock output is stable after writing to **SD Clock Enable** in this register to 1. The SD Host Driver shall wait to issue command to start until this bit is set to 1. **(ROC)** '1' = Ready '0' = Not Ready	0
	[2]	**SD Clock Enable** The Host Controller shall stop ***SDCLK*** when writing this bit to 0. **SDCLK Frequency Select** can be changed when this bit is 0. Then, the Host Controller shall maintain the same clock frequency until ***SDCLK*** is stopped (Stop at ***SDCLK***=0). If the **Card Inserted** in the *Present State register* is cleared, this bit shall be cleared. **(RW)** '1' = Enable '0' = Disable	0
	[1]	**Internal Clock Stable** This bit is set to 1 when SD Clock is stable after writing to **Internal Clock Enable** in this register to 1. The SD Host Driver shall wait to set **SD Clock Enable** until this bit is set to 1. Note: This is useful when using PLL for a clock oscillator that requires setup time. **(ROC)** '1' = Ready '0' = Not Ready	0
	[0]	**Internal Clock Enable** This bit is set to 0 when the Host Driver is not using the Host Controller or the Host Controller awaits a wakeup interrupt. The Host Controller should stop its internal clock to go very low power state. Still, registers shall be able to be read and written. Clock starts to oscillate when this bit is set to 1. When clock oscillation is stable, the Host Controller shall set **Internal Clock Stable** in this register to 1. This bit shall not affect card detection. **(RW)** '1' = Oscillate '0' = Stop	

TIMEOUT CONTROL REGISTER

At the initialization of the Host Controller, the Host Driver shall set the **Data Timeout Counter Value** according to the *Capabilities* register.

Register	Address	R/W	Description	Reset Value
TIMEOUTCON	0x4A80002E	R/W	Timeout Control Register	0x0

Name	Bit	Description	Initial Value
	[7:4]	Reserved	0
	[3:0]	**Data Timeout Counter Value** This value determines the interval by which DAT line timeouts are detected. Refer to the **Data Timeout Error** in the *Error Interrupt Status* register for information on factors that dictate timeout generation. Timeout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the **Data Timeout Error Status Enable** (in the *Error Interrupt tatus Enable* register) 1111b Reserved 1110b TMCLK x 2^{27} 1101b TMCLK x 2^{26} …….. … 0001b TMCLK x 2^{14} 0000b TMCLK x 2^{13}	0

SOFTWARE RESET REGISTER

A reset pulse is generated when writing 1 to each bit of this register. After completing the reset, the Host Controller shall clear each bit. Because it takes some time to complete software reset, the SD Host Driver shall confirm that these bits are 0.

Register	Address	R/W	Description	Reset Value
SWRST	0x4A80002F	R/W	Software Reset Register	0x0

Name	Bit	Description	Initial Value
	[7:3]	Reserved	0
	[2]	**Software Reset For DAT Line.** Only part of data circuit is reset. DMA circuit is also reset. (RWAC) The following registers and bits are cleared by this bit: *Buffer Data Port register* **Buffer is cleared and initialized.** ***Present State register*** **Buffer Read Enable** **Buffer Write Enable** **Read Transfer Active** **Write Transfer Active** **DAT Line Active** **Command Inhibit (DAT)** *Block Gap Control register* **Continue Request** **Stop At Block Gap Request** *Normal Interrupt Status register* **Buffer Read Ready** **Buffer Write Ready** **DMA Interrupt** **Block Gap Event** **Transfer Complete** '1' = Reset '0' = Work	0
	[1]	**Software Reset For CMD Line** Only part of command circuit is reset. (RWAC) The following registers and bits are cleared by this bit: *Present State* register **Command Inhibit (CMD)** *Normal Interrupt Status* register **Command Complete** '1' = Reset '0' = Work	0
	[0]	**Software Reset For All** This reset affects the entire Host Controller except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared to 0. During its initialization, the Host Driver shall set this bit to 1 to reset the Host Controller. The Host Controller shall reset this bit to 0 when capabilities registers are valid and the Host Driver can read them. Additional use of **Software Reset For All may** not affect the value of the C*apabilities* registers. If this bit is set to 1, the SD card shall reset itself and must be reinitialized by the Host Driver. (RWAC) '1' = Reset '0' = Work	0

NORMAL INTERRUPT STATUS REGISTER

The *Normal Interrupt Status Enable* affects reads of this register, but *Normal Interrupt Signal Enable* does not affect these reads. An interrupt is generated when the Normal Interrupt Signal Enable is enabled and at least one of the status bits is set to 1. For all bits except **Card Interrupt** and **Error Interrupt**, writing 1 to a bit clears it; writing to 0 keeps the bit unchanged. More than one status can be cleared with a single register write. The **Card Interrupt** is cleared when the card stops asserting the interrupt; that is, when the Card Driver services the interrupt condition.

Register	Address	R/W	Description	Reset Value
NORINTSTS	0x4A800030	ROC/RW1C	Normal Interrupt Status Register	0x0

Name	Bit	Description	Initial Value
	[15]	**Error Interrupt** If any of the bits in the *Error Interrupt Status* register are set, then this bit is set. Therefore the Host Driver can efficiently test for an error by checking this bit first. This bit is read only. (ROC) '0' = No Error '1' = Error	0
StaFIA3	[14]	FIFO SD Address Pointer Interrupt 3 Status (RW1C) '1' = Occurred '0' = Not Occurred	0
StaFIA2	[13]	FIFO SD Address Pointer Interrupt 2 Status (RW1C) '1' = Occurred '0' = Not Occurred	0
StaFIA1	[12]	FIFO SD Address Pointer Interrupt 1 Status (RW1C) '0' = Not Occurred '1' = Occurred	0
StaFIA0	[11]	FIFO SD Address Pointer Interrupt 0 Status (RW1C) '1' = Occurred '0' = Not Occurred	0
StaRWaitInt	[10]	Read Wait Interrupt Status (RW1C) '1' = Read Wait Interrupt Occurred '0' = Read Wait Interrupt Not Occurred Note : After checking response for the suspend command, release Read Wait interrupt status manually if BS = 0	0
StaCCS	[9]	CCS Interrupt Status (RW1C) Command Complete Singal Interrupt Status bit is for CE-ATA interface mode. '1' = CCS Interrupt Occurred '0' = CCS Interrupt Not Occurred	0

Name	Bit	Description	Initial Value
	[8]	**Card Interrupt** Writing this bit to 1 does not clear this bit. It is cleared by resetting the SD card interrupt factor. In 1-bit mode, the Host Controller shall detect the **Card Interrupt** without SD Clock to support wakeup. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the SD card and the interrupt to the Host System. It is necessary to define how to handle this delay. When this status has been set and the Host Driver needs to start this interrupt service, **Card Interrupt Status Enable** in the *Normal Interrupt Status Enable* register shall be set to 0 in order to clear the card interrupt statuses latched in the Host Controller and to stop driving the interrupt signal to the Host System. After completion of the card interrupt service (It should reset interrupt factors in the SD card and the interrupt signal may not be asserted), set **Card Interrupt Status Enable** to 1 and start sampling the interrupt signal again. (ROC, RW1C) '1' = Generate Card Interrupt '0' = No Card Interrupt	0
	[7]	**Card Removal** This status is set if the **Card Inserted** in the *Present State* register changes from 1 to 0. When the Host Driver writes this bit to 1 to clear this status, the status of the Card Inserted in the Present State register should be confirmed. Because the card detect state may possibly be changed when the Host Driver clear this bit and interrupt event may not be generated. (RW1C) '1' = Card removed '0' = Card state stable or Debouncing	0
	[6]	**Card Insertion** This status is set if the **Card Inserted** in the *Present State* register changes from 0 to 1. When the Host Driver writes this bit to 1 to clear this status, the status of the Card Inserted in the Present State register should be confirmed. Because the card detect state may possibly be changed when the Host Driver clear this bit and interrupt event may not be generated. (RW1C) '1' = Card inserted '0' = Card state stable or Debouncing	0
	[5]	**Buffer Read Ready** This status is set if the **Buffer Read Enable** changes from 0 to 1. Refer to the **Buffer Read Enable** in the *Present State* register. (RW1C) '1' = Ready to read buffer '0' = Not ready to read buffer	0

Name	Bit	Description	Initial Value
	[4]	**Buffer Write Ready** This status is set if the **Buffer Write Enable** changes from 0 to 1. Refer to the **Buffer Write Enable** in the *Present State* register. (RW1C) '1' = Ready to write buffer '0' = Not ready to write buffer	0
	[3]	**DMA Interrupt** This status is set if the Host Controller detects the Host DMA Buffer boundary during transfer. Refer to the **Host DMA Buffer Boundary** in the *Block Size* register. Other DMA interrupt factors may be added in the future. This interrupt shall not be generated after the **Transfer Complete**. (RW1C) '1' = **DMA Interrupt** is generated '0' = No **DMA Interrupt**	0
	[2]	**Block Gap Event** If the **Stop At Block Gap Request** in the *Block Gap Control* register is set, this bit is set when both a read / write transaction is stopped at a block gap. If **Stop At Block Gap Request** is not set to 1, this bit is not set to 1. (1) In the case of a Read Transaction This bit is set at the falling edge of the **DAT Line Active** Status (When the transaction is stopped at SD Bus timing. The Read Wait must be supported in order to use this function. Refer to Section 3.11.3 about the detail timing. (2) Case of Write Transaction This bit is set at the falling edge of **Write Transfer Active** Status (After getting CRC status at SD Bus timing). Refer to Section 3.11.4 for more details on the sequence of events. '1' = Transaction stopped at block gap '0' = No **Block Gap Event**	0

<table>
<tr><th>Name</th><th>Bit</th><th>Description</th><th>Initial Value</th></tr>
<tr><td></td><td>[1]</td><td>Transfer Complete
This bit is set when a read / write transfer is completed.
(1) In the case of a Read Transaction
This bit is set at the falling edge of Read Transfer Active Status. There are two cases in which this interrupt is generated. The first is when a data transfer is completed as specified by data length (After the last data has been read to the Host System). The second is when data has stopped at the block gap and completed the data transfer by setting the Stop At Block Gap Request in the Block Gap Control register (After valid data has been read to the Host System). Refer to Section 3.11.3 for more details on the sequence of events.
(2) In the case of a Write Transaction
This bit is set at the falling edge of the DAT Line Active Status. There are two cases in which this interrupt is generated. The first is when the last data is written to the SD card as specified by data length and the busy signal released. The second is when data transfers are stopped at the block gap by setting Stop At Block Gap Request in the Block Gap Control register and data transfers completed. (After valid data is written to the SD card and the busy signal released). Refer to Section 3.11.4 for more details on the sequence of events. (RW1C)
The table below shows that Transfer Complete has higher priority than Data Timeout Error. If both bits are set to 1, the data transfer can be considered complete.
Relation between Transfer Complete and Data
<table>
<tr><th>Transfer Complete</th><th>Data Timeout Error</th><th>Meaning of the status</th></tr>
<tr><td>0</td><td>0</td><td>Interrupted by another factor</td></tr>
<tr><td>0</td><td>1</td><td>Timeout occur during transfer</td></tr>
<tr><td>1</td><td>Don’t care</td><td>Data transfer complete</td></tr>
</table>
‘1’ = Data Transfer Complete
‘0’ = No transfer complete</td><td>0</td></tr>
<tr><td></td><td>[0]</td><td>Command Complete
This bit is set when get the end bit of the command response. (Except Auto CMD12) Refer to Command Inhibit (CMD) in the Present State register.
The table below shows that Command Timeout Error has higher priority than Command Complete. If both bits are set to 1, it can be considered that the response was not received correctly.
<table>
<tr><th>Command complete</th><th>Command Timeout Error</th><th>Meaning of the status</th></tr>
<tr><td>0</td><td>0</td><td>Interrupted by another factor</td></tr>
<tr><td>Don’t care</td><td>1</td><td>Response not received within 64 SDCLK cycles.</td></tr>
<tr><td>1</td><td>0</td><td>Response received</td></tr>
</table>
‘1’ = Command Complete
‘0’ = No command complete</td><td>0</td></tr>
</table>

NOTES :

1. Host Driver may check if interrupt is actually cleared by polling or monitoring the INTREQ port. If HCLK is much faster than SDCLK, it takes long time to be cleared for the bits actually.
2. Card Interrupt status bit keeps previous value until next card interrupt period (level interrupt) and can be cleared when write to 1 (RW1C).

ERROR INTERRUPT STATUS REGISTER

Signals defined in this register can be enabled by the *Error Interrupt Status Enable* register, but not by the *Error Interrupt Signal Enable* register. The interrupt is generated when the *Error Interrupt Signal Enable* is enabled and at least one of the statuses is set to 1. Writing to 1 clears the bit and writing to 0 keeps the bit unchanged. More than one status can be cleared at the one register write.

Register	Address	R/W	Description	Reset Value
ERRINTSTS	0x4A800032	ROC/ RW1C	Error Interrupt Status Register	0x0

Name	Bit	Description	Initial Value
	[15:9]	**Reserved**	0
	[8]	**Auto CMD12 Error** Occurs when detecting that one of the bits in *Auto CMD12 Error Status* register has changed from 0 to 1. This bit is set to 1,not only when the errors in Auto CMD12 occur but also when Auto CMD12 is not executed due to the previous command error. ‘1’ = Error ‘0’ = No Error	0
	[7]	**Current Limit Error** Not implemented in this version. Always 0.	0
	[6]	**Data End Bit Error** Occurs either when detecting 0 at the end bit position of read data which uses the ***DAT*** line or at the end bit position of the CRC Status. ‘1’ = Error ‘0’ = No Error	0
	[5]	**Data CRC Error** Occurs when detecting CRC error when transferring read data which uses the ***DAT*** line or when detecting the Write CRC status having a value of other than "010". ‘1’ = Error ‘0’ = No Error	0
	[4]	**Data Timeout Error** Occurs when detecting one of following timeout conditions. (1) Busy timeout for R1b, R5b type (2) Busy timeout after Write CRC status (3) Write CRC Status timeout (4) Read Data timeout. ‘1’ = Timeout ‘0’ = No Error	0

Name	Bit	Description	Initial Value
	[3]	**Command Index Error** Occurs if a Command Index error occurs in the command response. '1' = Error '0' = No Error	0
	[2]	**Command End Bit Error** Occurs when detecting that the end bit of a command response is 0. '1' = End bit Error generated '0' = No Error	
	[1]	**Command CRC Error** Command CRC Error is generated in two cases. (1) If a response is returned and the **Command Timeout Error** is set to 0 (indicating no timeout), this bit is set to 1 when detecting a CRC error in the command response. (2) The Host Controller detects a ***CMD*** line conflict by monitoring the ***CMD*** line when a command is issued. If the Host Controller drives the ***CMD*** line to 1 level, but detects 0 level on the ***CMD*** line at the next SDCLK edge, then the Host Controller shall abort the command (Stop driving ***CMD*** line) and set this bit to 1. The Command Timeout Error shall also be set to 1 to distinguish ***CMD*** line conflict (Refer to Table 33). '1' = CRC Error generated '0' = No Error	0
	[0]	**Command Timeout Error** Occurs only if no response is returned within 64 ***SDCLK*** cycles from the end bit of the command. If the Host Controller detects a ***CMD*** line conflict, in which case **Command CRC Error shall** also be set as shown in Table 33, this bit **shall** be set without waiting for 64 ***SDCLK*** cycles because the command will be aborted by the Host Controller. '1' = Timeout '0' = No Error	0

The relation between **Command CRC Error** and **Command Timeout Error** is shown in Table below.

Table 28-4. The relation between Command CRC Error and Command Timeout Error

Command CRC Error	Command Timeout Error	Kinds of error
0	0	No Error
0	1	Response Timeout Error
1	0	Response CRC Error
1	1	***CMD*** line conflict

NORMAL INTERRUPT STATUS ENABLE REGISTER

Setting to 1 enables Interrupt Status.

Register	Address	R/W	Description	Reset Value
NORINTSTSEN	0x4A800034	R/W	Normal Interrupt Status Enable Register	0x0

Name	Bit	Description	Initial Value
	[15]	**Fixed to 0** The Host Driver shall control error interrupts using the *Error Interrupt Status Enable* register. *(RO)*	0
EnStaFIA3	[14]	**FIFO SD Address Pointer Interrupt 3 Status Enable** '1' = Enabled '0' = Masked	0
EnStaFIA2	[13]	**FIFO SD Address Pointer Interrupt 2 Status Enable** '1' = Enabled '0' = Masked	0
EnStaFIA1	[12]	**FIFO SD Address Pointer Interrupt 1 Status Enable** '1' = Enabled '0' = Masked	0
EnStaFIA0	[11]	**FIFO SD Address Pointer Interrupt 0 Status Enable** '1' = Enabled '0' = Masked	0
EnStaRWait	[10]	**Read Wait interrupt status enable** '1' = Enabled '0' = Masked	0
EnStaCCS	[9]	**CCS Interrupt Status Enable** '1' = Enabled '0' = Masked	0
	[8]	**Card Interrupt Status Enable** If this bit is set to 0, the Host Controller shall clear interrupt request to the System. The **Card Interrupt** detection is stopped when this bit is cleared and restarted when this bit is set to 1. The Host Driver should clear the **Card Interrupt Status Enable** before servicing the **Card Interrupt** and should set this bit again after all interrupt requests from the card are cleared to prevent inadvertent interrupts. '1' = Enabled '0' = Masked	0

Name	Bit	Description	Initial Value
	[7]	**Card Removal Status Enable** '1' = Enabled '0' = Masked	0
	[6]	**Card Insertion Status Enable** '1' = Enabled '0' = Masked	0
	[5]	**Buffer Read Ready Status Enable** '1' = Enabled '0' = Masked	0
	[4]	**Buffer Write Ready Status Enable** '1' = Enabled '0' = Masked	0
	[3]	**DMA Interrupt Status Enable** '1' = Enabled '0' = Masked	0
	[2]	**Block Gap Event Status Enable** '1' = Enabled '0' = Masked	0
	[1]	**Transfer Complete Status Enable** '1' = Enabled '0' = Masked	0
	[0]	**Command Complete Status Enable** '1' = Enabled '0' = Masked	0

ERROR INTERRUPT STATUS ENABLE REGISTER

Setting to 1 enables Error Interrupt Status.

Register	Address	R/W	Description	Reset Value
ERRINTSTSEN	0x4A800036	R/W	Error Interrupt Status Enable Register	0x0

Name	Bit	Description	Initial Value
	[15:9]	Reserved	0
	[8]	**Auto CMD12 Error Status Enable** '1' = Enabled '0' = Masked	0
	[7]	**Current Limit Error Status Enable** This function is not implemented in this version. '1' = Enabled '0' = Masked	0
	[6]	**Data End Bit Error Status Enable** '1' = Enabled '0' = Masked	0
	[5]	**Data CRC Error Status Enable** '1' = Enabled '0' = Masked	0
	[4]	**Data Timeout Error Status Enable** '1' = Enabled '0' = Masked	0
	[3]	**Command Index Error Status Enable** '1' = Enabled '0' = Masked	0
	[2]	**Command End Bit Error Status Enable** '1' = Enabled '0' = Masked	0
	[1]	**Command CRC Error Status Enable** '1' = Enabled '0' = Masked	0
	[0]	**Command Timeout Error Status Enable** '1' = Enabled '0' = Masked	0

NORMAL INTERRUPT SIGNAL ENABLE REGISTER

This register is used to select which interrupt status is indicated to the Host System as the interrupt. These status bits all share the same1 bit interrupt line. Setting any of these bits to 1 enables interrupt generation.

Register	Address	R/W	Description	Reset Value
NORINTSIGEN	0x4A800038	R/W	Normal Interrupt Signal Enable Register	0x0

Name	Bit	Description	Initial Value
	[15]	**Fixed to 0** The Host Driver shall control error interrupts using the *Error Interrupt Signal Enable* register.	0
EnSigFIA3	[14]	**FIFO SD Address Pointer Interrupt 3 Signal Enable** '1' = Enabled '0' = Masked	0
EnSigFIA2	[13]	**FIFO SD Address Pointer Interrupt 2 Signal Enable** '1' = Enabled '0' = Masked	0
EnSigFIA1	[12]	**FIFO SD Address Pointer Interrupt 1 Signal Enable** '1' = Enabled '0' = Masked	0
EnSigFIA0	[11]	**FIFO SD Address Pointer Interrupt 0 Signal Enable** '1' = Enabled '0' = Masked	0
EnSigRWait	[10]	**Read Wait Interrupt Signal Enable** '1' = Enabled '0' = Masked	0
EnSigCCS	[9]	**CCS Interrupt Signal Enable** Command Complete Singal Interrupt Status bit is for CE-ATA interface mode. '1' = Enabled '0' = Masked	0
	[8]	**Card Interrupt Signal Enable** '1' = Enabled '0' = Masked	0
	[7]	**Card Removal Signal Enable** '1' = Enabled '0' = Masked	0
	[6]	**Card Insertion Signal Enable** '1' = Enabled '0' = Masked	0

Name	Bit	Description	Initial Value
	[5]	**Buffer Read Ready Signal Enable** '1' = Enabled '0' = Masked	0
	[4]	**Buffer Write Ready Signal Enable** '1' = Enabled '0' = Masked	0
	[3]	**DMA Interrupt Signal Enable** '1' = Enabled '0' = Masked	0
	[2]	**Block Gap Event Signal Enable** '1' = Enabled '0' = Masked	0
	[1]	**Transfer Complete Signal Enable** '1' = Enabled '0' = Masked	0
	[0]	**Command Complete Signal Enable** '1' = Enabled '0' = Masked	0

ERROR INTERRUPT SIGNAL ENABLE REGISTER

This register is used to select which interrupt status is notified to the Host System as the interrupt. These status bits all share the same 1 bit interrupt line. Setting any of these bits to 1 enables interrupt generation.

Register	Address	R/W	Description	Reset Value
ERRINTSIGEN	0x4A80003A	R/W	Error Interrupt Signal Enable Register	0x0

Name	Bit	Description	Initial Value
	[15:9]	Reserved	0
	[8]	**Auto CMD12 Error Signal Enable** '1' = Enabled '0' = Masked	0
	[7]	**Current Limit Error Signal Enable** This function is not implemented in this version. '1' = Enabled '0' = Masked	0
	[6]	**Data End Bit Error Signal Enable** '1' = Enabled '0' = Masked	0
	[5]	**Data CRC Error Signal Enable** '1' = Enabled '0' = Masked	0
	[4]	**Data Timeout Error Signal Enable** '1' = Enabled '0' = Masked	0
	[3]	**Command Index Error Signal Enable** '1' = Enabled '0' = Masked	0
	[2]	**Command End Bit Error Signal Enable** '1' = Enabled '0' = Masked	0
	[1]	**Command CRC Error Signal Enable** '1' = Enabled '0' = Masked	0
	[0]	**Command Timeout Error Signal Enable** '1' = Enabled '0' = Masked	0

Detailed documents are to be copied from SD Host Standard Spec.

AUTOCMD12 ERROR STATUS REGISTER

When *Auto CMD12 Error Status* is set, the Host Driver shall check this register to identify what kind of error Auto CMD12 indicated. This register is valid only when the **Auto CMD12 Error** is set.

Register	Address	R/W	Description	Reset Value
ACMD12ERRSTS	0x4A80003C	ROC	Auto CMD12 Error Status Register	0x0

Name	Bit	Description	Initial Value
	[15:8]	Reserved	0
	[7]	**Command Not Issued By Auto CMD12 Error** Setting this bit to 1 means CMD_wo_DAT is not executed due to an Auto CMD12 Error (D04-D01) in this register. '1' = Not Issued '0' = No error	0
	[6:5]	**Reserved**	0
	[4]	**Auto CMD12 Index Error** Occurs if the Command Index error occurs in response to a command. '1' = Error '0' = No Error	0
	[3]	**Auto CMD12 End Bit Error** Occurs when detecting that the end bit of command response is 0. '1' = End Bit Error Generated '0' = No Error	0
	[2]	**Auto CMD12 CRC Error** Occurs when detecting a CRC error in the command response. '1' = CRC Error Generated '0' = No Error	0
	[1]	**Auto CMD12 Timeout Error** Occurs if no response is returned within 64 ***SDCLK*** cycles from the end bit of command. If this bit is set to1, the other error status bits (D04-D02) are meaningless. '1' = Time out '0' = No Error	0
	[0]	**Auto CMD12 Not Executed** If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. Setting this bit to 1 means the Host Controller cannot issue Auto CMD12 to stop memory multiple block data transfer due to some error. If this bit is set to 1, other error status bits (D04-D01) are meaningless. '1' = Not executed '0' = Executed	0

The relation between Auto CMD12 CRC Error and Auto CMD12 Timeout Error is shown below.

Table 28-5. The relation between Command CRC Error and Command Timeout Error

Auto CMD12 CRC Error	Auto CMD12 Timeout Error	Kinds of error
0	0	No Error
0	1	Response Timeout Error
1	0	Response CRC Error
1	1	***CMD*** line conflict

The timing of changing *Auto CMD12 Error Status* can be classified in three scenarios:

(1) When the Host Controller is going to issue Auto CMD12

Set D00 to 1 if Auto CMD12 cannot be issued due to an error in the previous command.

Set D00 to 0 if Auto CMD12 is issued.

(2) At the end bit of an Auto CMD12 response

Check received responses by checking the error bits D01, D02, D03 and D04.

Set to 1 if error is detected.

Set to 0 if error is not detected.

(3) Before reading the Auto CMD12 Error Status bit D07

Set D07 to 1 if there is a command cannot be issued

Set D07 to 0 if there is no command to issue

Timing of generating the **Auto CMD12 Error** and writing to the *Command* register are asynchronous. Then D07 shall be sampled when driver never writing to the *Command* register. So just before reading the *Auto CMD12 Error Status* register is good timing to set the D07 status bit. An Auto CMD12 Error Interrupt is generated when one of the error bits D00 to D04 is set to 1. The **Command Not Issued By Auto CMD12 Error** does not generate an interrupt.

CAPABILITIES REGISTER

This register provides the Host Driver with information specific to the Host Controller implementation. The Host Controller may implement these values as fixed or loaded from flash memory during power on initialization. Refer to **Software Reset For All** in the *Software Reset* register for loading from flash memory and completion timing control.

Register	Address	R/W	Description	Reset Value
CAPAREG	0x4A800040	HWInit	Capabilities Register	0x0

Name	Bit	Description	Initial Value
	[31:27]	Reserved	
	[26]	**Voltage Support 1.8V** (HWInit) '1'=1.8V Supported '0'=1.8V Not Supported	1
	[25]	**Voltage Support 3.0V** (HWInit) '1'=3.0V Supported '0'=3.0V Not Supported	0
	[24]	**Voltage Support 3.3V** (HWInit) '1'=3.3V Supported '0'=3.3V Not Supported	1
	[23]	**Suspend/Resume Support** (HWInit) This bit indicates whether the Host Controller supports Suspend / Resume functionality. If this bit is 0, the Suspend and Resume mechanism (Refer to 2.6) are not supported and the Host Driver shall not issue either Suspend or Resume commands. '1'=Supported '0'=Not Supported	1
	[22]	**DMA Support** (HWInit) This bit indicates whether the Host Controller is capable of using DMA to transfer data between system memory and the Host Controller directly. '1'=DMA Supported '0'=DMA Not Supported	1
	[21]	**High Speed Support** (HWInit) This bit indicates whether the Host Controller and the Host System support High Speed mode and they can supply SD Clock frequency from 25MHz to 50MHz. '1'=High Speed Supported '0'= High Speed Not Supported	1
	[20:18]	**Reserved**	0

Name	Bit	Description	Initial Value
	[17:16]	**Max Block Length** (HWInit) This value indicates the maximum block size that the Host Driver can read and write to the buffer in the Host Controller. The buffer shall transfer this block size without wait cycles. Three sizes can be defined as indicated below. '00'=512-byte, '01'=1024-byte, '10'=2048-byte, '11'=Reserved	0
	[15:14]	**Reserved**	0
	[13:8]	**Base Clock Frequency For SD Clock** (HWInit) This value indicates the base (maximum) clock frequency for the SD Clock. Unit values are 1MHz. If the real frequency is 16.5MHz, the lager value shall be set 01 0001b (17MHz) because the Host Driver use this value to calculate the clock divider value (Refer to the **SDCLK Frequency Select** in the *Clock Control* register.) and it shall not exceed upper limit of the SD Clock frequency. The supported clock range is 10MHz to 63MHz. If these bits are all 0, the Host System has to get information via another method. Not '0'=1MHz to 63MHz 000000b = Get information via another method	0
	[7]	**Timeout Clock Unit** (HWInit) This bit shows the unit of base clock frequency used to detect **Data Timeout Error**. '0'=KHz, '1'=MHz	1
	[6]	**Reserved**	0
	[5:0]	**Timeout Clock Frequency** (HWInit) This bit shows the base clock frequency used to detect **Data Timeout Error**. The **Timeout Clock Unit** defines the unit of this field value. **Timeout Clock Unit** =0 [KHz] unit: 1KHz to 63KHz **Timeout Clock Unit** =1 [MHz] unit: 1MHz to 63MHz Not 0 = 1KHz to 63KHz or 1MHz to 63MHz 00 0000b = Get information via another method	0

MAXIMUM CURRENT CAPABILITIES REGISTER

These registers indicate maximum current capability for each voltage. The value is meaningful if **Voltage Support** is set in the *Capabilities* register. If this information is supplied by the Host System via another method, all *Maximum Current Capabilities* register shall be 0.

Register	Address	R/W	Description	Reset Value
MAXCURR	0x4A800048	HWInit	Maximum Current Capabilities Register	0x0

Name	Bit	Description	Initial Value
	[31:24]	Reserved	
	[23:16]	**Maximum Current for 1.8V** (HWInit)	0
	[15:8]	**Maximum Current for 3.0V** (HWInit)	0
	[7:0]	**Maximum Current for 3.3V** (HWInit)	0

This register measures current in 4mA steps. Each voltage level's current support is described using the Table below.

Table 28-6. Maximum Current Value Definition

Register Value	Current Value
0	Get information via another method
1	4mA
2	8mA
3	12mA
…	…
255	1020mA

CONTROL REGISTER 2

This register contains the SD Command Argument.

Register	Address	R/W	Description	Reset Value
CONTROL2	0x4A800080	R/W	Control register 2	0x0

Name	Bit	Description	Initial Value
Reserved	[31:30]	Reserved	0x00
CDInvRXD	[29]	**Card Detect signal inversion for RX_DAT[3]** 0=Disable, 1=Enable	0
SelCardOut	[28]	**Card Removed Condition Selection** 0=Normal operation, 1=No card state is using debounce filter operation	0
FltClkSel	[27:24]	**Filter Clock (iFLTCLK) Selection** Filter Clock period = 2^(FltClkSel + 5) x iSDCLK period 0000 = 25 x iSDCLK, 0001 = 26 x iSDCLK … 1111 = 220 x iSDCLK	0
LvlDAT	[23:16]	**DAT line level** Bit[23]=DAT[7], BIT[22]=DAT[6], BIT[21]=DAT[5], BIT[20]=DAT[4], Bit[19]=DAT[3], BIT[18]=DAT[2], BIT[17]=DAT[1], BIT[16]=DAT[0] (Read Only)	Line state
EnFBCLKT	[15]	**Feedback Clock Enable for Tx Data/Command Clock** ‘0’=Disable, ‘1’=Enable	0
EnFBCLKR	[14]	**Feedback Clock Enable for Rx Data/Command Clock** ‘0’=Disable, ‘1’=Enable	0
SDCDSel	[13]	**SD Card Detect Signal Selection** Card Detect Pin Level does not simply reflect SDCD# pin, but chooses from SDCD, DAT[3], or CDTestlvl depending on CDSigSel and this field (SDCDSel) values ‘0’=nSDCD is used for SD Card Detect Signal ‘1’=DAT[3] is used for SD Card Detect Signal	0
CardSync	[12]	**SD Card Detect Sync Support** This field is used not to clear SD Bus Power bit, when being set. ‘0’=No Sync, no switch output enable signal (Command, Data) ‘1’=Sync, control output enable signal (Command, Data)	0
TxBStartEn	[11]	**CE-ATA I/F mode** Busy state check before Tx Data start state 0=Disable, 1=Enable	0

Name	Bit	Description	Initial Value
DFCnt	[10:9]	**Debounce Filter Count** Debounce Filter Count setting register for Card Detect signal input (SDCD#) 00=No use debounce filter, 01=4 iSDCLK, 10=16 iSDCLK, 11=64 iSDCLK	0
EnSCHold	[8]	**SDCLK Hold Enable** The enter and exit of the SDCLK Hold state is done by Host Controller. 0=Disable, 1=Enable	0
RwaitMode	[7]	**Read Wait Release Control** 0=Read Wait state is released by the Host Controller (Auto) 1=Read Wait state is released by the Host Device (Manual)	0
DisBufRD	[6]	**Buffer Read Disable** 0=Normal mode, user can read buffer(FIFO) data using 0x20 register 1=User cannot read buffer(FIFO) data using 0x20 register. In this case, the buffer memory only can be read through memory area. (Debug purpose)	0
SelBaseClk	[5:4]	**Base Clock Source Select** 00 or 01 =HCLK, 10=EPLL out Clock (from SYSCON), 11=External Clock source (XTI or XEXTCLK)	00
PwrSync	[3]	**SD OP Power Sync Support with SD Card** 0=No Sync (no switch power off) 1=Sync (control power ON/OFF with SD card)	0
ModePwrPin	[2]	**Power Pin Use mode select** 0=SDPWR33, SDPWR18 pin mode 1=SDPWRon, SDPWRlvl pin mode	0
EnSDCLKmsk	[1]	**SDCLK output clock masking when Card Insert cleared** This field when High is used not to stop SDCLK when No Card state. '0'=Disable, '1'=Enable	0
HwInitFin	[0]	**SD Host Controller Hardware Initialization Finish** 0=Not Finish, 1=Finish	0

NOTES:

1. Ensure to always set SDCLK Hold Enable (EnSCHold) if the card does not support Read Wait to guarantee for Receive data not overwrtten to the internal FIFO memory.
2. CMD_wo_DAT issue is prohibited during READ transfer when SDCLK Hold Enable is set

CONTROL REGISTER 3 REGISTER

Register	Address	R/W	Description	Reset Value
CONTROL3	0x4A800084	R/W	FIFO Interrupt Control (Control Register 3)	0x0

Name	Bit	Description	Initial Value
FCSel3	[31]	**Feedback Clock Select [3]** Reference Note (1)	0x0
FIA3	[30:24]	**FIFO Interrupt Address register 3** FIFO (512Byte Buffer memory, word address unit) Initial value(0x7F) generates at 512-byte(128-word) position.	0x7F
FCSel2	[23]	**Feedback Clock Select [2]** Reference Note (1)	0x0
FIA2	[22:16]	**FIFO Interrupt Address register 2** FIFO (512Byte Buffer memory, word address unit) Initial value(0x5F) generates at 384-byte(96-word) position.	0x5F
FCSel1	[15]	**Feedback Clock Select [1]** Reference Note (2)	0x0
FIA1	[14:8]	**FIFO Interrupt Address register 1** FIFO (512Byte Buffer memory, word address unit) Initial value(0x3F) generates at 256-byte(64-word) position.	0x3F
FCSel0	[7]	**Feedback Clock Select [0]** Reference Note (2)	0x0
FIA0	[6:0]	**FIFO Interrupt Address register 0** FIFO (512Byte Buffer memory, word address unit) Initial value(0x1F) generates at 128-byte(32-word) position.	0x1F

Notes:
1. FCSel[3:2] : Tx Feedback Clock Delay Control
   '00'=Delay1 (less delay), '01'=Delay2, '10'=Delay3, '11'=Delay4 (more delay)
2. FCSel[1:0] : Rx Feedback Clock Delay Control
   '00'=Delay1 (less delay), '01'=Delay2, '10'=Delay3, '11'=Delay4 (more delay)

HOST CONTROLLER VERSION REGISTER

This register contains the SD Command Argument.

Register	Address	R/W	Description	Reset Value
HCVER	0x4A8000FE	HWInit	Host Controller Version Register	0x0300

Name	Bit	Description	Initial Value
	[15:8]	**Vendor Version Number** This status is reserved for the vendor version number. The Host Driver should not use this status. 0x3 : SDMMC3.0 Host Controller	0x03
	[7:0]	**Specification Version Number** This status indicates the Host Controller Spec. Version. The upper and lower 4-bit indicate the version. ‘00’ = SD Host Specification Version 1.0 Ohters = Reserved	0

NOTES

29 ELECTRICAL DATA

ABSOLUTE MAXIMUM RATINGS

Table 29-1. Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
DC Supply Voltage	VDDi, VDDiarm, VDDalive, VDDA_MPLL, VDDA_EPLL, VDDI_UDEV	-0.5	1.8	V
	VDD_OP1,VDD_OP2,VDD_RTC, VDD_SDRAM,VDD_SRAM, VDD_CAM,VDD_SD,VDDA_ADC,VDDA33x	-0.5	4.8	
DC Input Voltage	VIN	-0.5	4.8	
DC Output Voltage	VOUT	-0.5	4.8	
DC Input Current	IIN	± 200		mA
Storage Temperature	TSTG	– 65 to 150		^{o}C

RECOMMENDED OPERATING CONDITIONS

Table 29-2. Recommended Operating Conditions (400MHz)

Parameter	Symbol		Min	Typ	Max	Unit
DC Supply Voltage for Alive Block	VDDalive		1.15	1.2	1.25	V
DC Supply Voltage for Core Block	ARMCLK / HCLK					
	400/133 MHz	VDDarm VDDi VDD_MPLL VDD_EPLL	1.25	1.3	1.35	
	133/133 MHz	VDDarm VDDi VDD_MPLL VDD_EPLL	1.05	1.1	1.35	
	66/66 MHz	VDDarm VDDi VDD_MPLL VDD_EPLL	0.95	1.0	1.35	
DC Supply Voltage for I/O Block1	VDD_OP1		2.3	2.5 /3.3	3.6	
DC Supply Voltage for I/O Block2	VDD_OP2		1.7	1.8 / 2.5 / 3.3	3.6	
DC Supply Voltage for Memory Interface	VDD_SRAM VDD_SDRAM		1.7	1.8 / 2.5 /3.3	3.6	
DC Supply Voltage for RTC	VDD_RTC		2.5	3.0	3.6	
DC Supply Voltage for CAM/SD/LCD	VDD_CAM VDD_SD		1.7	1.8 / 2.5 / 3.3	3.6	
	VDD_LCD		2.3	2.5 /3.3	3.6	
DC Supply Voltage for USB Phy 3.3V	VDDA33x		3.3-5%	3.3	3.3+5%	
DC Supply Voltage for USB Phy 1.2V	VDDI_UDEV		1.2-5%	1.2	1.2+5%	
DC Supply Voltage for ADC	VDDA_ADC		3.0	3.3	3.6	
DC Input Voltage	VIN		3.0	3.3	3.6	
			2.3	2.5	2.7	
			1.65	1.8	1.95	
DC Output Voltage	VOUT		3.0	3.3	3.6	
			2.3	2.5	2.7	
			1.65	1.8	1.95	
Operating Temperature	TA		Industrial	-40 to 85		^{o}C
			Commercial	0 to 70		

Table 29-2. Recommended Operating Conditions (533MHz)

Parameter	Symbol		Min	Typ	Max	Unit
DC Supply Voltage for Alive Block	VDDalive		1.15	1.2	1.25	V
DC Supply Voltage for Core Block	ARMCLK / HCLK					
	533/133 MHz	VDDarm	1.325	1.375	1.425	
		VDDi VDD_MPLL VDD_EPLL	1.1	1.15	1.2	
	133/133 MHz	VDDarm	0.95	1.0	1.425	
		VDDi VDD_MPLL VDD_EPLL	0.95	1.0	1.2	
	66/66 MHz	VDDarm	0.85	0.9	1.425	
		VDDi VDD_MPLL VDD_EPLL	0.85	0.9	1.2	
DC Supply Voltage for I/O Block1	VDD_OP1		2.3	2.5 /3.3	3.6	
DC Supply Voltage for I/O Block2	VDD_OP2		1.7	1.8 / 2.5 / 3.3	3.6	
DC Supply Voltage for Memory Interface	VDD_SRAM VDD_SDRAM		1.7	1.8 / 2.5 / 3.3	3.6	
DC Supply Voltage for RTC	VDD_RTC		2.5	3.0	3.6	
DC Supply Voltage for CAM/SD/LCD	VDD_CAM VDD_SD		1.7	1.8 / 2.5 / 3.3	3.6	
	VDD_LCD		2.3	2.5 /3.3	3.6	
DC Supply Voltage for USB Phy 3.3V	VDDA33x		3.3-5%	3.3	3.3+5%	
DC Supply Voltage for USB Phy 1.2V	VDDI_UDEV		1.2-5%	1.2	1.2+5%	
DC Supply Voltage for ADC	VDDA_ADC		3.0	3.3	3.6	
DC Input Voltage	VIN		3.0	3.3	3.6	
			2.3	2.5	2.7	
			1.65	1.8	1.95	
DC Output Voltage	VOUT		3.0	3.3	3.6	
			2.3	2.5	2.7	
			1.65	1.8	1.95	
Operating Temperature	TA		Industrial	-40 to 85		^{o}C
			Commercial	0 to 70		

D.C. ELECTRICAL CHARACTERISTICS

Table 29-3. Normal I/O PAD DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Unit	Note
VDD_OP(1)	Output Supply Voltage	3.3V	3.0	3.3	3.6	V	
		2.5V	2.3	2.5	2.7		
		1.8V	1.65	1.8	1.95		
VDDi	Internal Core Voltage	400MHz	1.25	1.3	1.35	V	
		533MHz	1.1	1.15	1.2		
Temp	Ambient Temperature		-40	25	85	°C	
Vih	dc Input Logic High		0.7VDD_OP			V	
Vil	dc Input Logic Low				0.3VDD_OP	V	
VT	Switching threshold			0.5VDD_OP		V	
VT+	Schmitt trigger, positive-going threshold				0.7VDD_OP	V	
VT-	Schmitt trigger, negative-going threshold		0.3VDD_OP			V	
Iih	High Level Input Current		-10		10	uA	
Iil	Low Level Input Current		-10		10	uA	
Iih	High Level Input Current (with Pull Down)	Vext=3.3V	10	33	72	uA	
		Vext=2.5V	5	18	40		
		Vext=1.8V	1	9	25		
Iil	Low Level Input Current (with Pull Up)	Vext=3.3V	-72	-33	-10	uA	
		Vext=2.5V	-40	-18	-5		
		Vext=1.8V	-25	-9	-1		
Voh	Output High Voltage(@Ioh=-100uA)		VDD_OP-0.2V			V	
Vol	Output Low Voltage(@Iol=100uA)				0.2V	V	

Note :

1. VDD_OP=VDD_OP1+VDD_OP2+VDD_LCD+VDD_SD+VDD_CAM
   The Minimum operating voltage of VDDOP1 is 2.3V (refer to Table 29-2)

Table 29-4. Special Memory DDR I/O PAD DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Unit	Note
VDD_ sdram	Output supply voltage		1.70	1.8	1.90	V	
VDDi	Internal Core Voltage	400MHz	1.25	1.3	1.35	V	
		533MHz	1.1	1.15	1.2		
Temp	Ambient Temperature		-40	25	85	°C	
Vih	dc Input Logic High		0.8*VDD sdram	-	-	V	
Vil	dc Input Logic Low		-	-	0.2*VDD sdram	V	
Iih	High Level Input Current		-10	-	10	uA	
Iil	Low Level Input Current		-10	-	10	uA	
Iih	High Level Input Current (with Pull Down)		20	-	60	uA	
Iil	Low Level Input Current (with Pull Up)		-60	-	-20	uA	
Voh	Output High Voltage(@Ioh=-100uA)		VDDsdram -0.2V	-	-	V	
Vol	Output Low Voltage(@Iol=100uA)		-	-	0.2V	V	

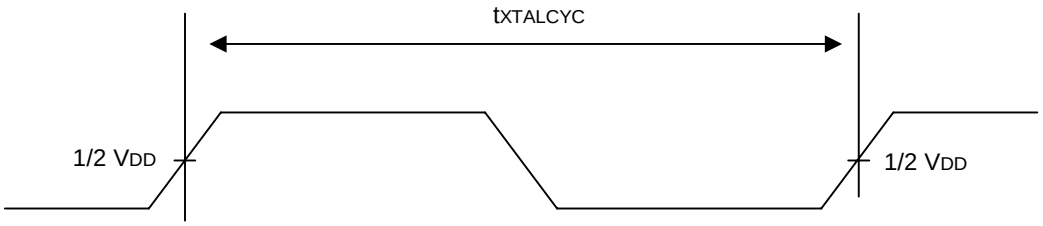
Table 29-5. USB DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
VIH	High level input voltage		2.5		V
VIL	Low level input voltage			0.8	V
IIH	High level input current	Vin = 3.3V	-10	10	μA
IIL	Low level input current	Vin = 0.0V	-10	10	μA
VOH	Static Output High	15K to GND	2.8	3.6	V
VOL	Static Output Low	1.5K to 3.6V		0.3	V

Table 29-6. RTC OSC DC Electrical Characteristics

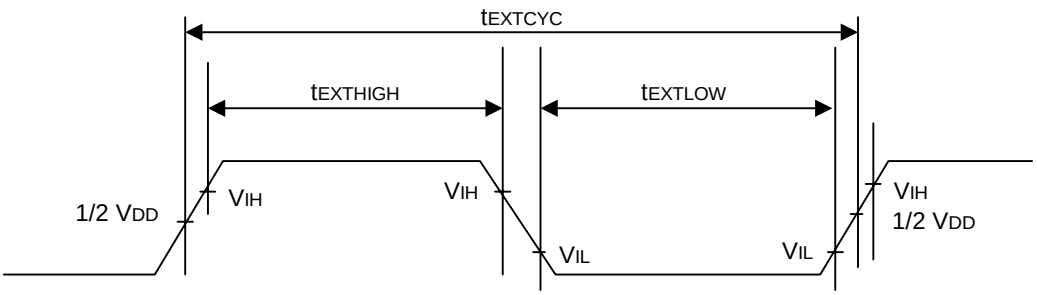
Symbol	Parameter	Min	Typ	Max	Unit
VDD_RTC	Output supply voltage	2.5	3.0	3.6	V
V_{IH}	DC input logic high	0.8*VDDrtc			V
V_{IL}	DC input logic low			0.2*VDDrtc	V
IIH	High level input current	-10		10	μA
IIL	Low level input current	-10		10	μA

A.C. ELECTRICAL CHARACTERISTICS



NOTE: The clock input from the XTIpll pin.

Figure 29-1. XTIpll Clock Timing



NOTE: The clock input from the EXTCLK pin.

Figure 29-2. EXTCLK Clock Input Timing

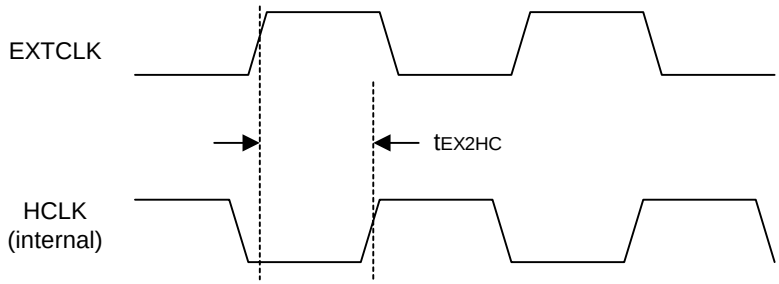


Figure 29-3. EXTCLK/HCLK in case that EXTCLK is used without the PLL

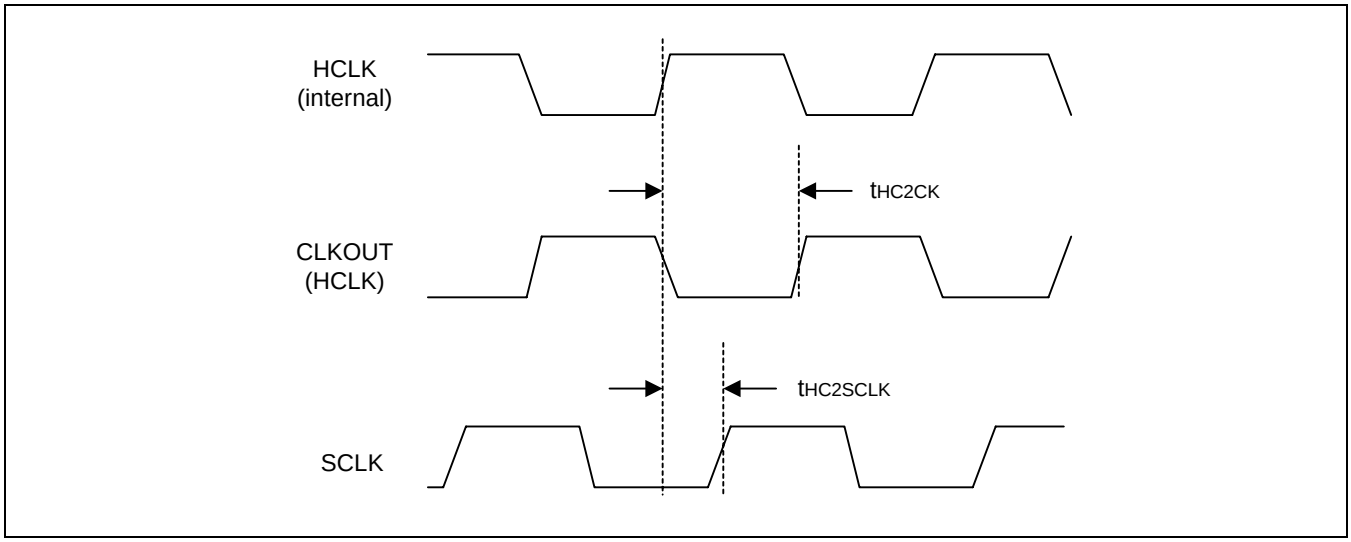


Figure 29-4. HCLK/CLKOUT/SCLK in case that EXTCLK is used

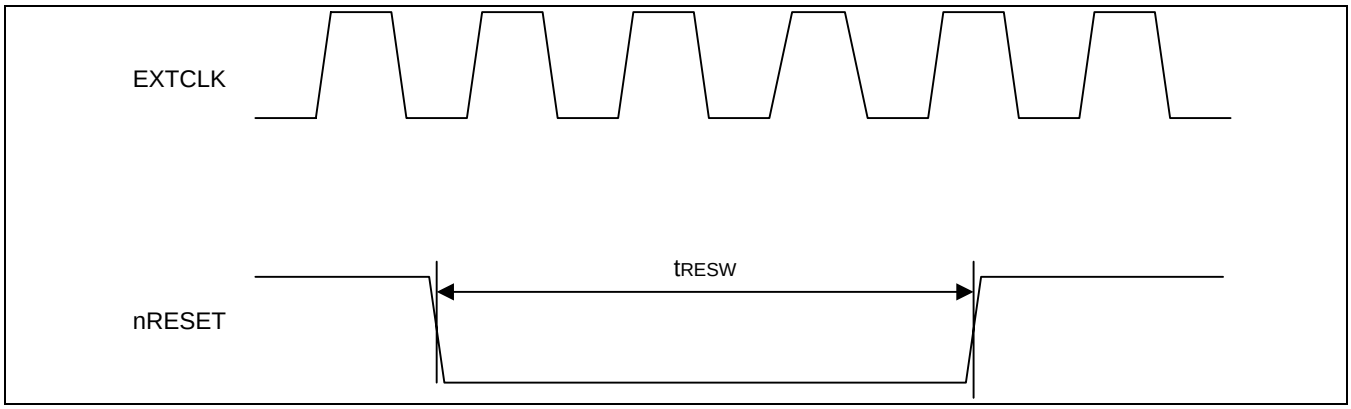


Figure 29-5. Manual Reset Input Timing

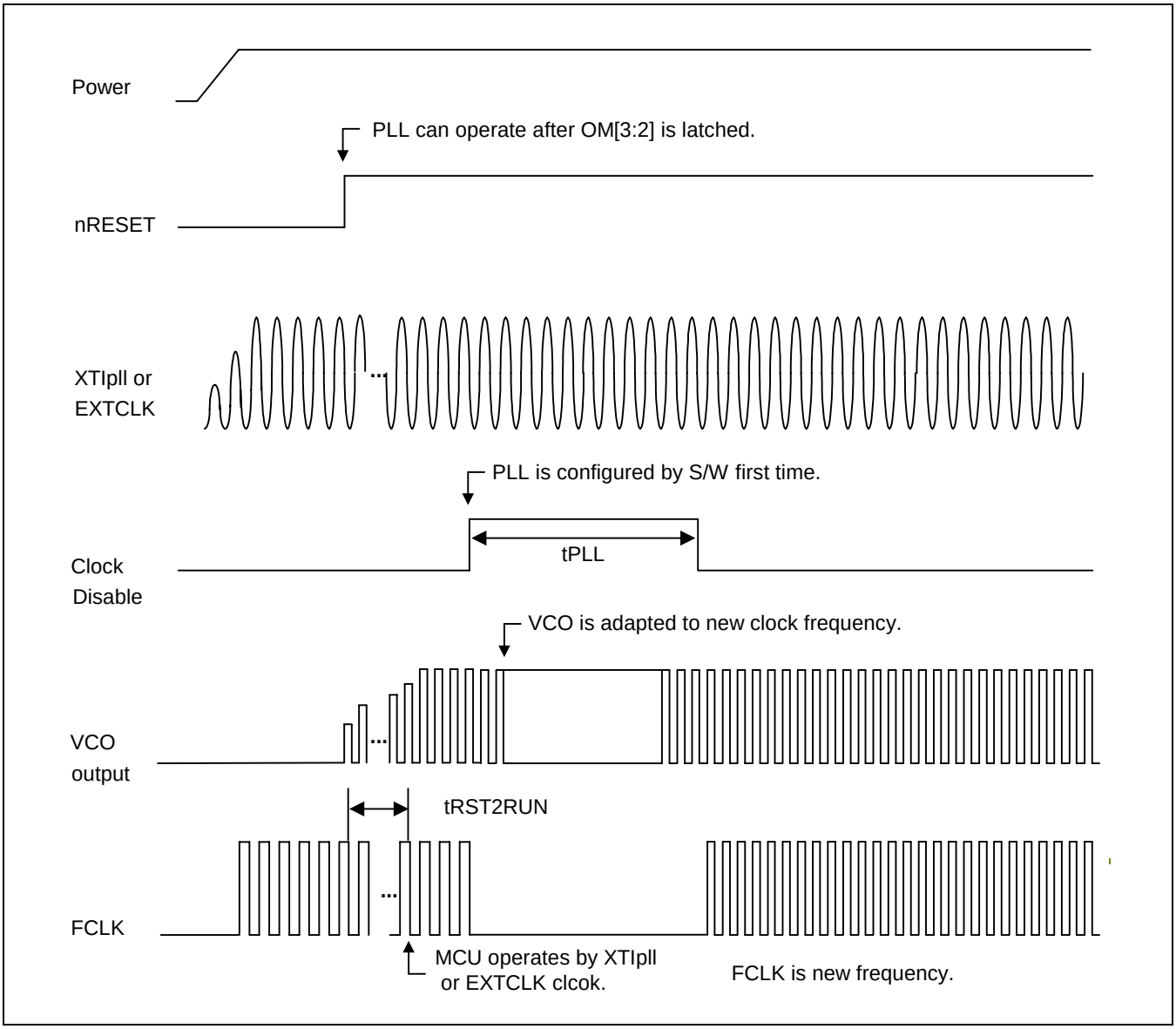


Figure 29-6. Power-On Oscillation Setting Timing

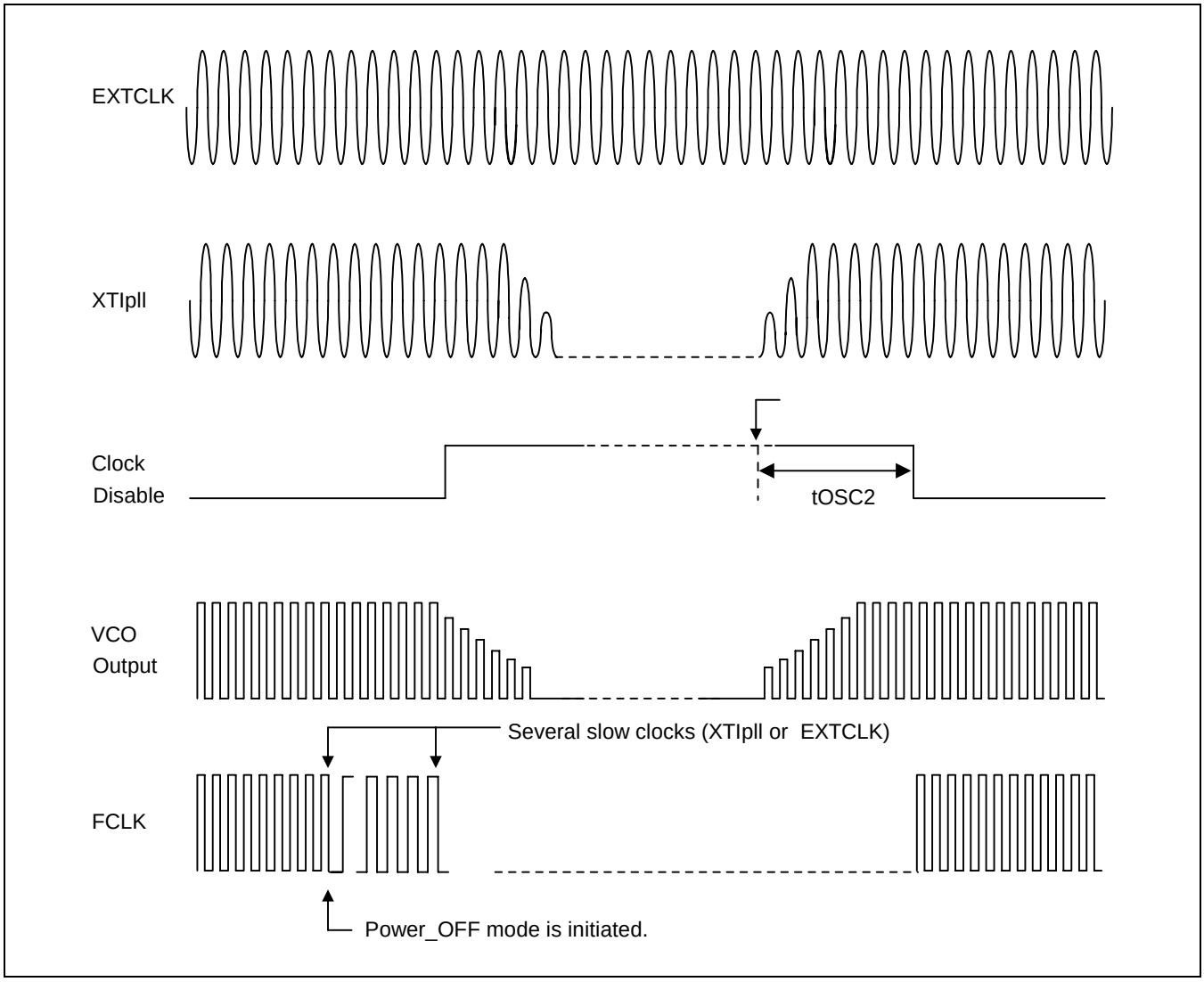


Figure 29-7. Sleep Mode Return Oscillation Setting Timing

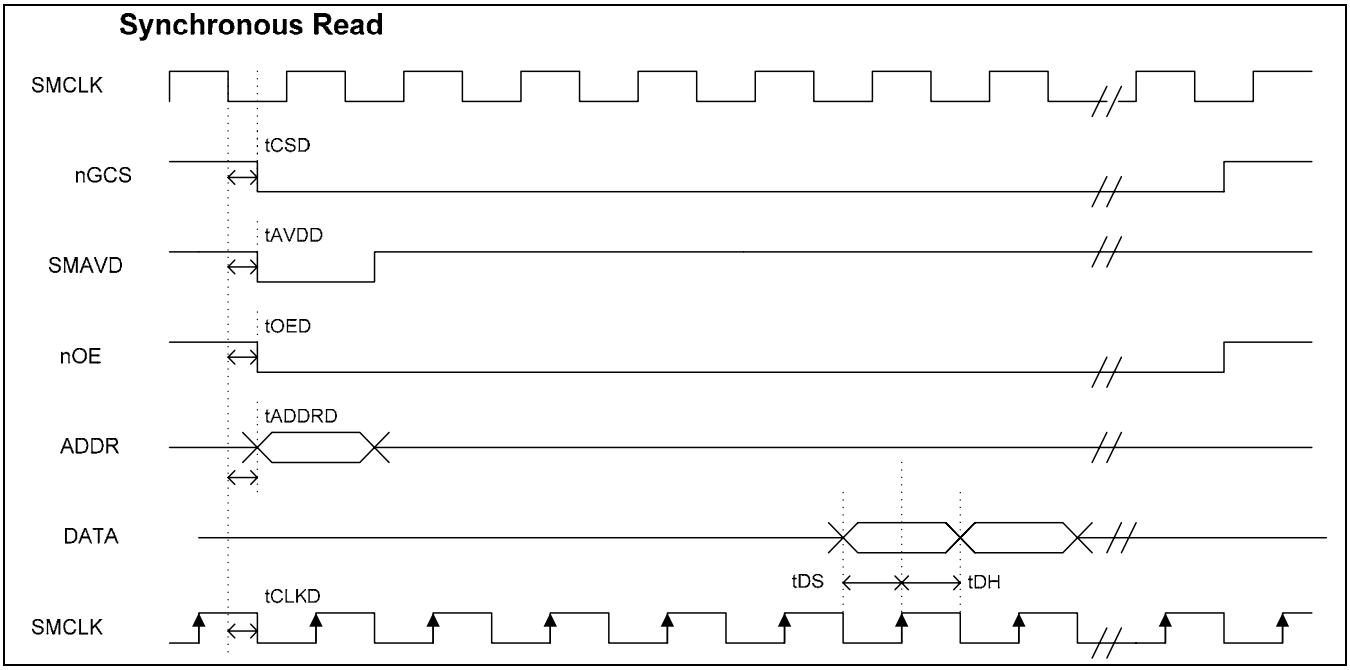


Figure 29-8. SMC Synchronous Read Timing

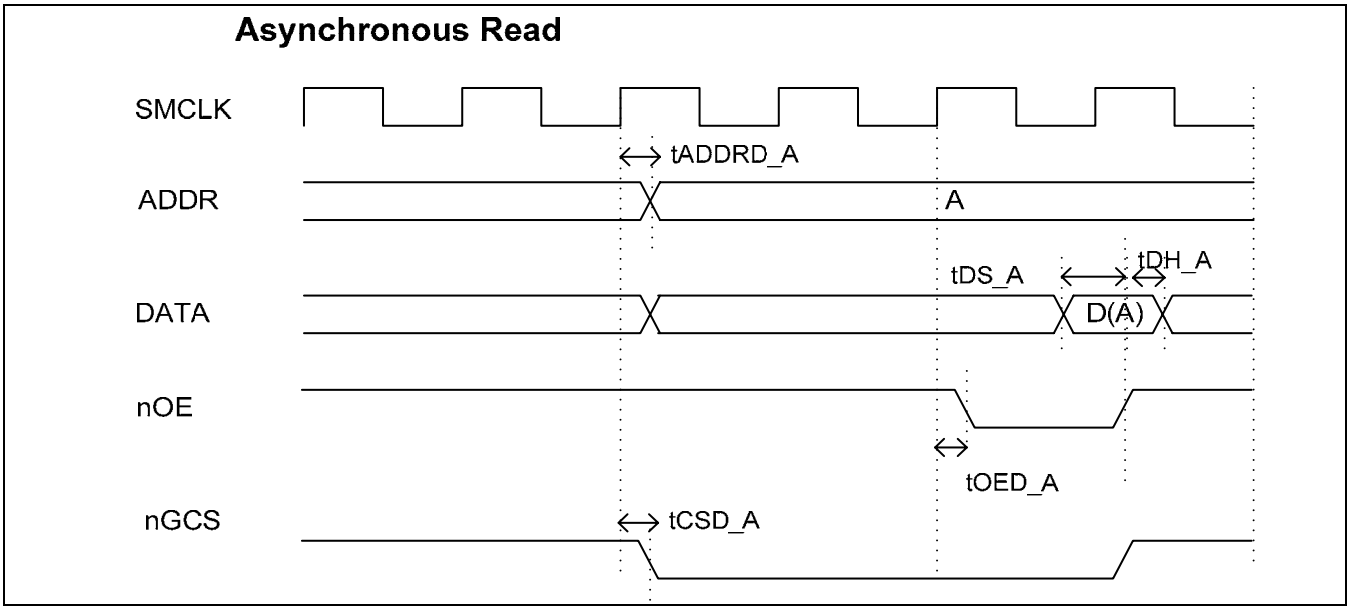


Figure 29-9. SMC Asynchronous Read Timing

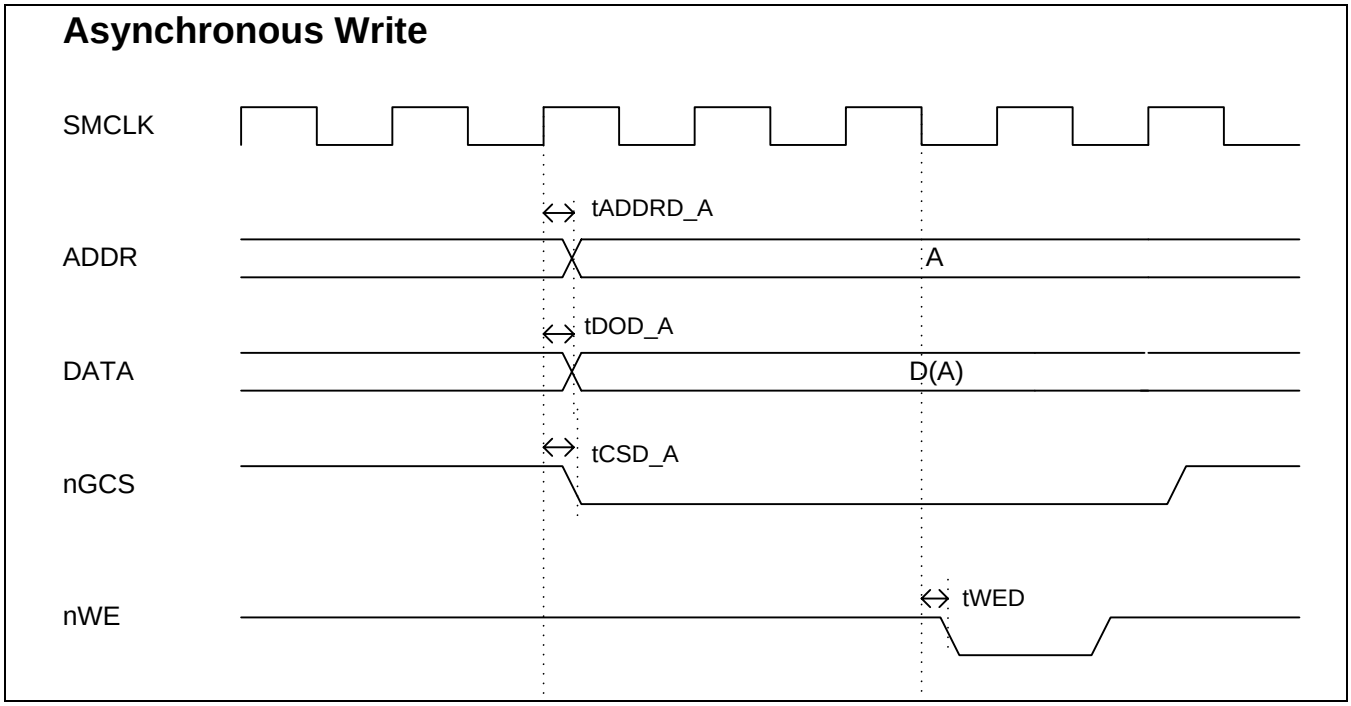


Figure 29-10. SMC Asynchronous Write Timing

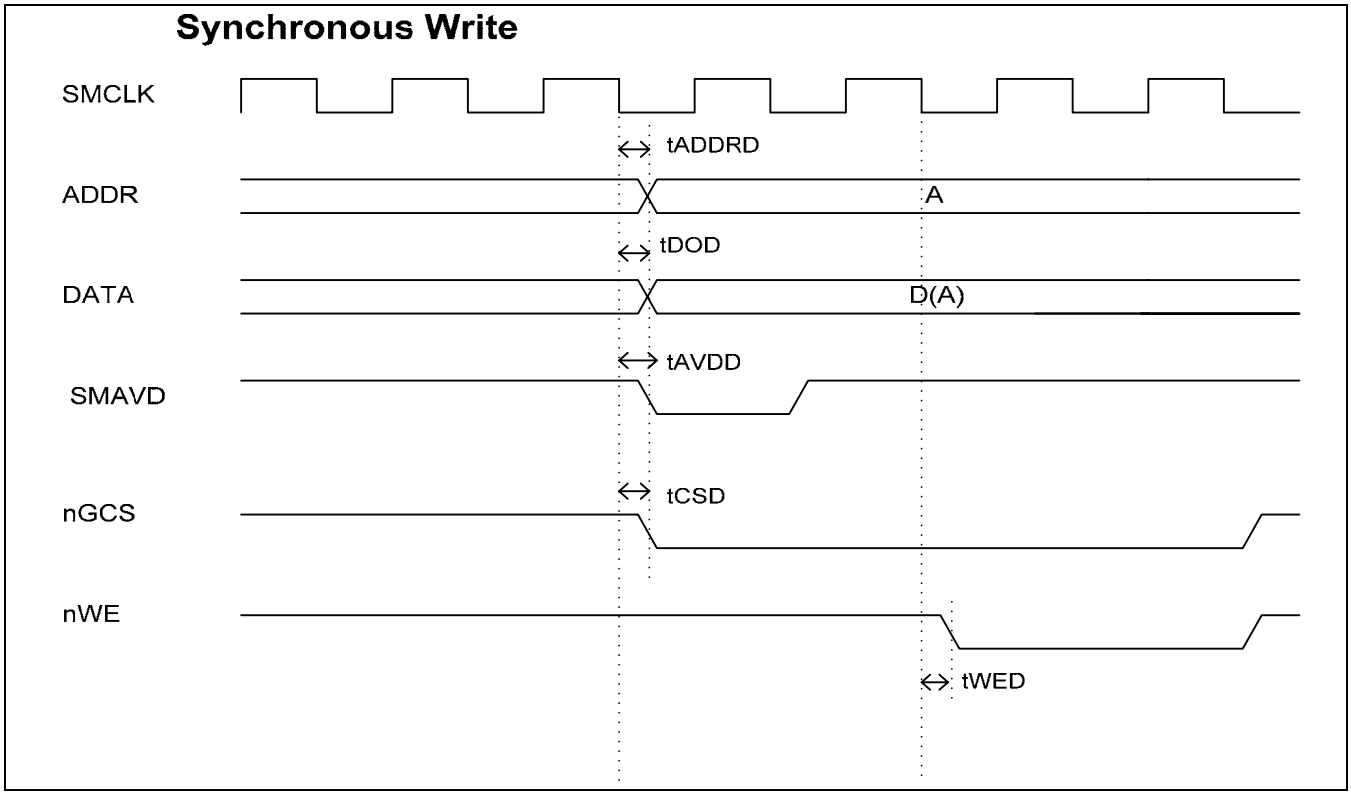


Figure 29-11. SMC Synchronous Write Timing

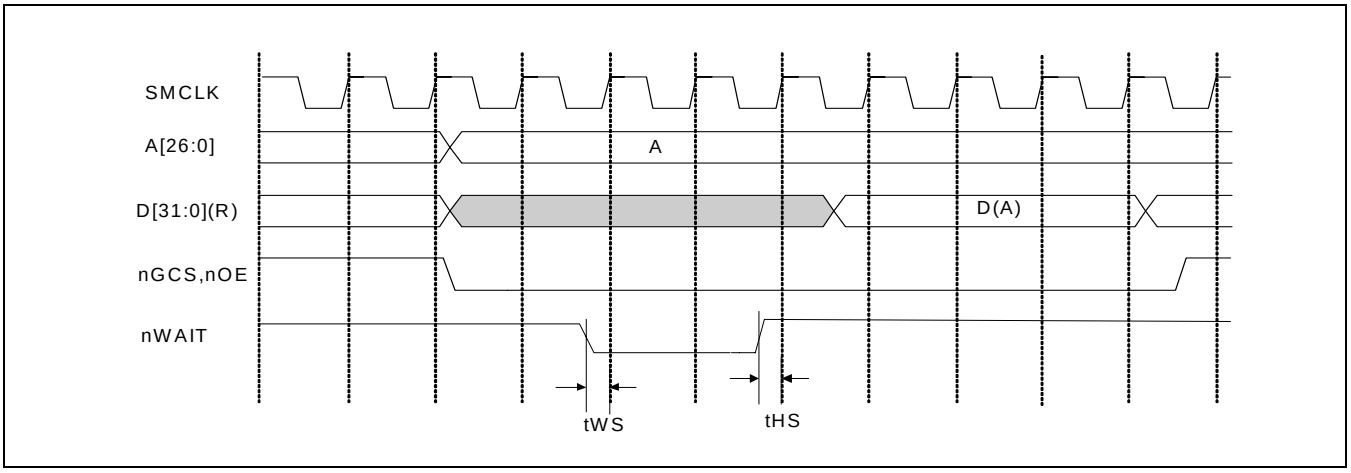


Figure 29-12. SMC Wait Timing

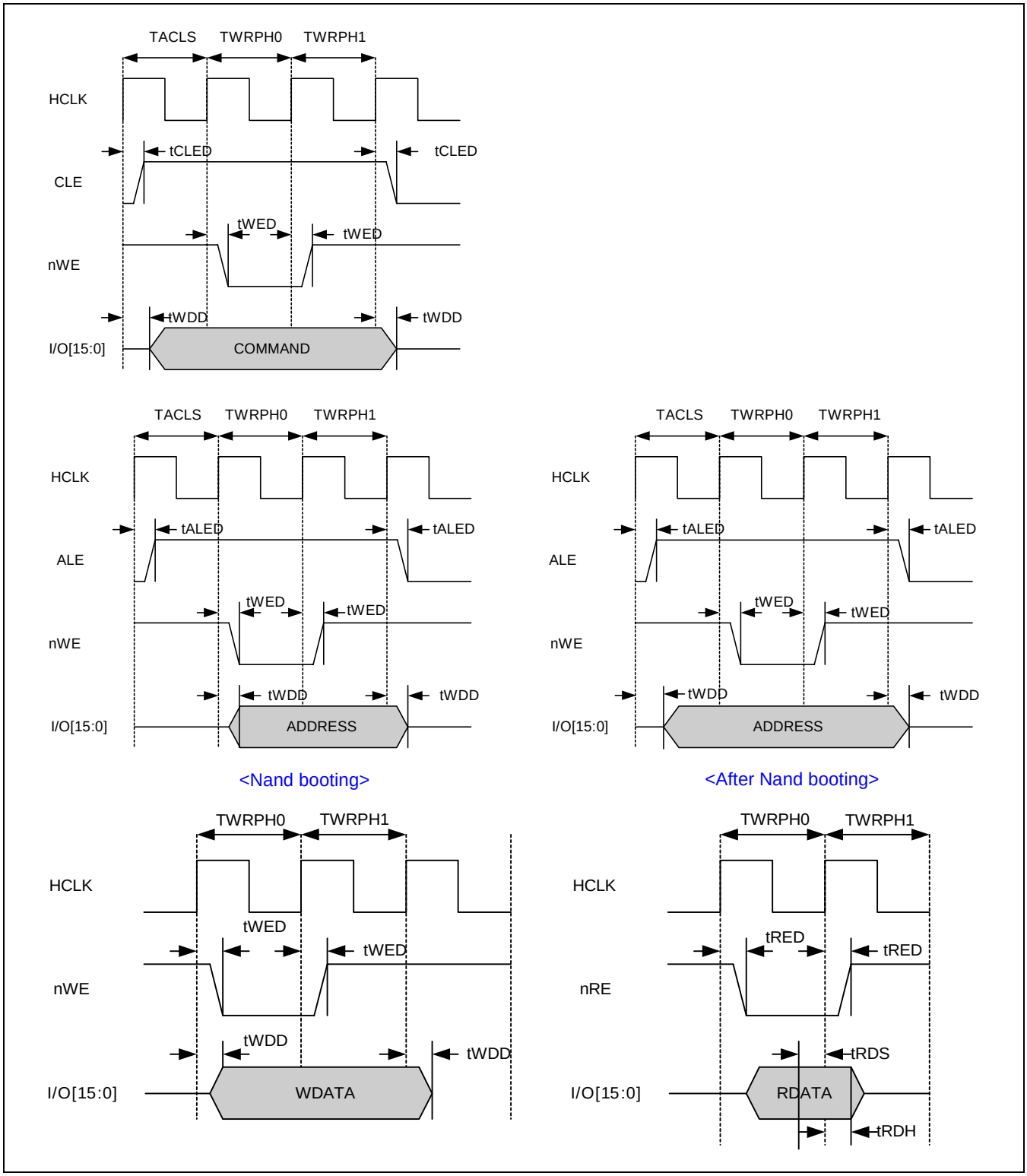


Figure 29-13. Nand Flash Timing

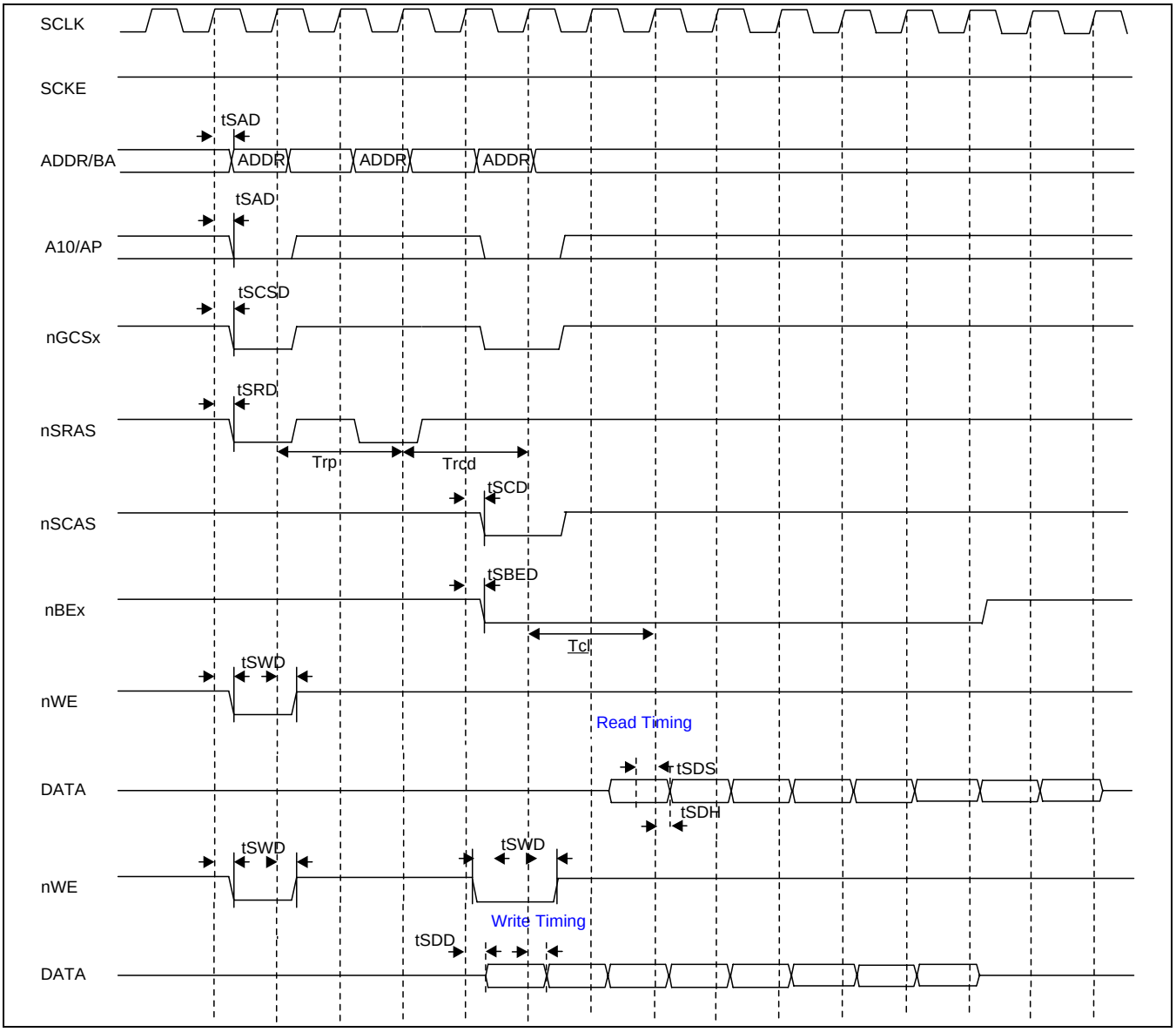


Figure 29-14. SDRAM READ / WRITE Timing (Trp = 2, Trcd = 2, Tcl = 2, DW = 16-bit)

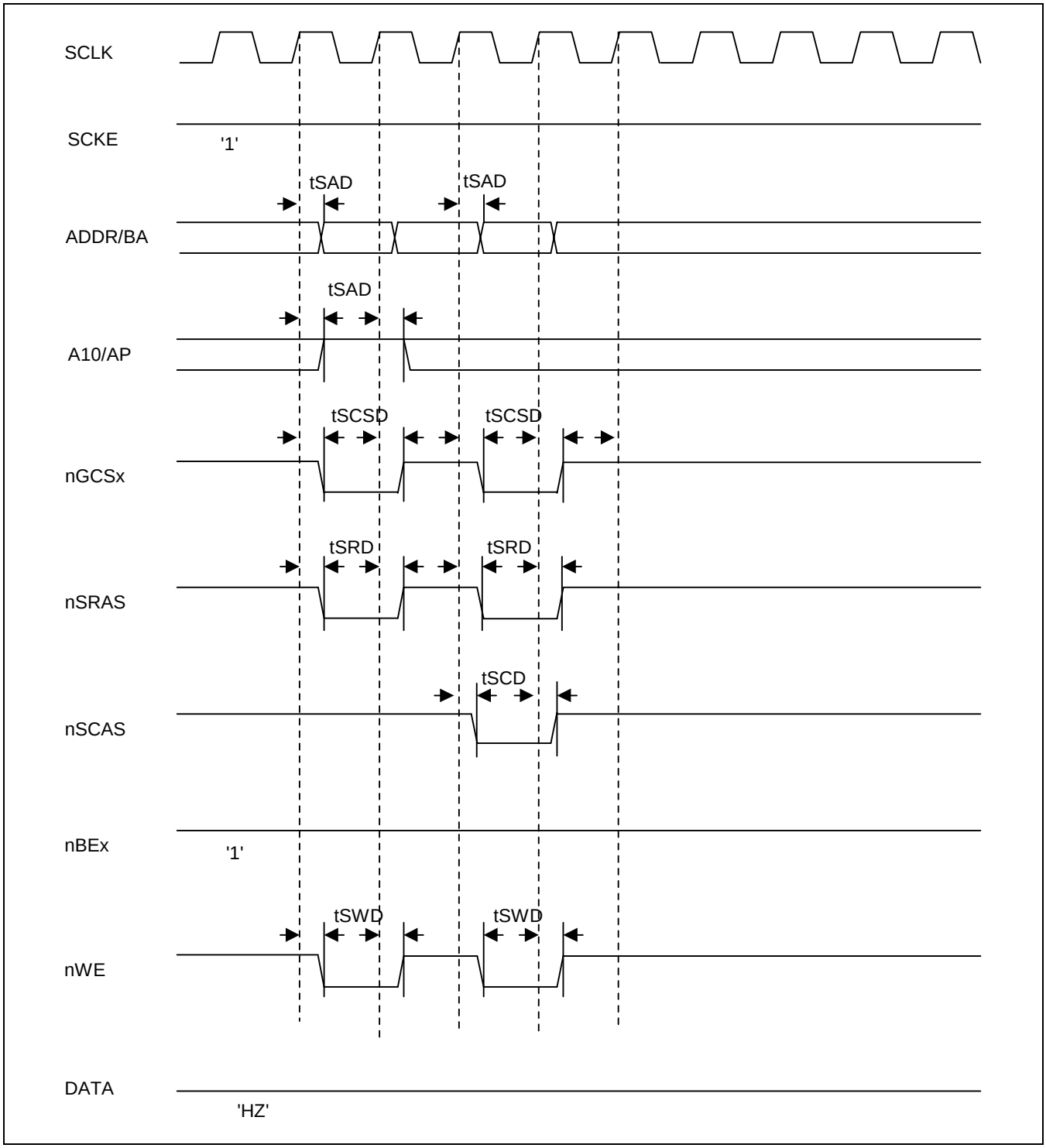
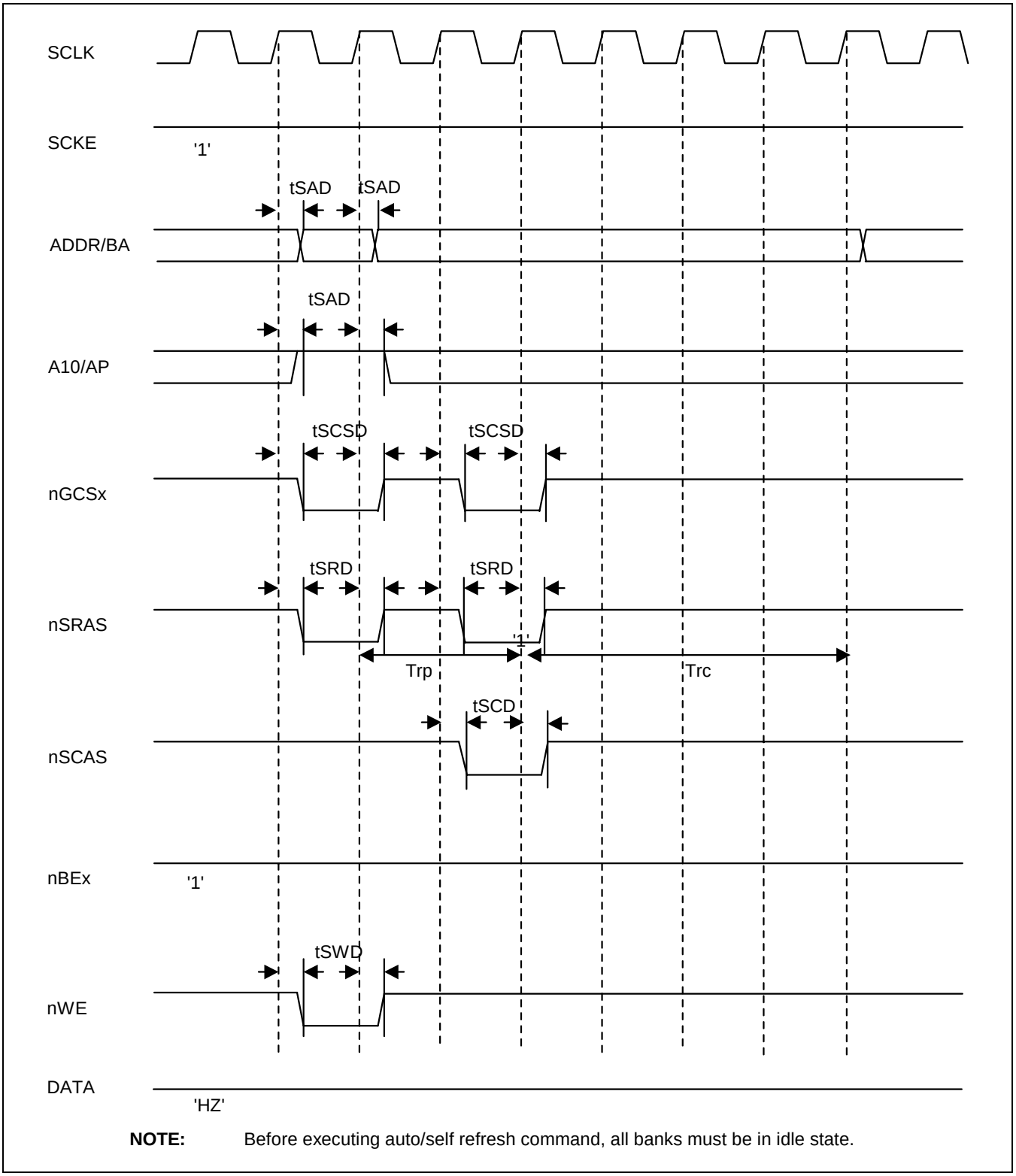


Figure 29-15. SDRAM MRS Timing



NOTE: Before executing auto/self refresh command, all banks must be in idle state.

Figure 29-16. SDRAM Auto Refresh Timing (Trp = 2, Trc = 4)

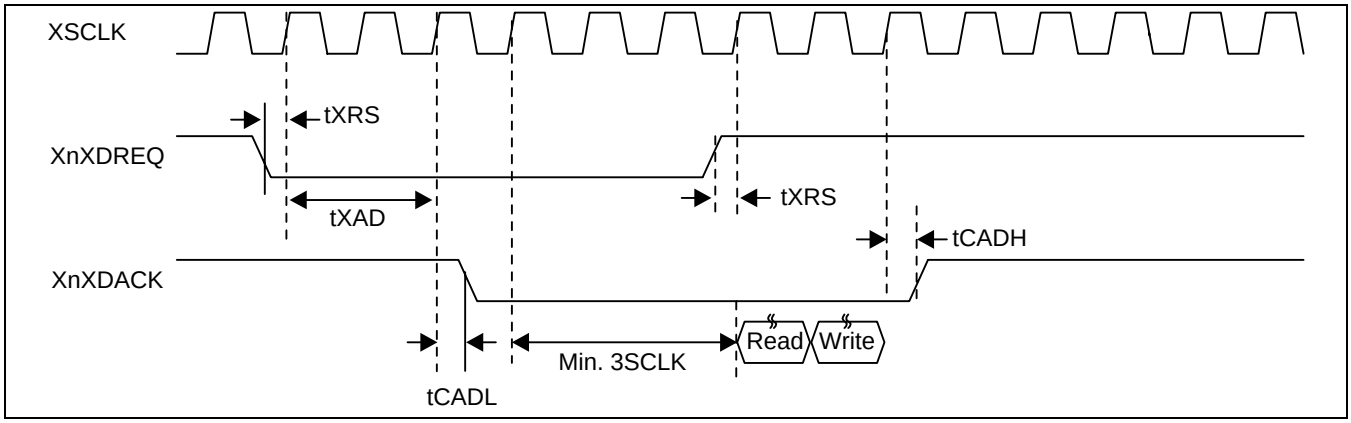


Figure 29-17. External DMA Timing (Handshake, Single transfer)

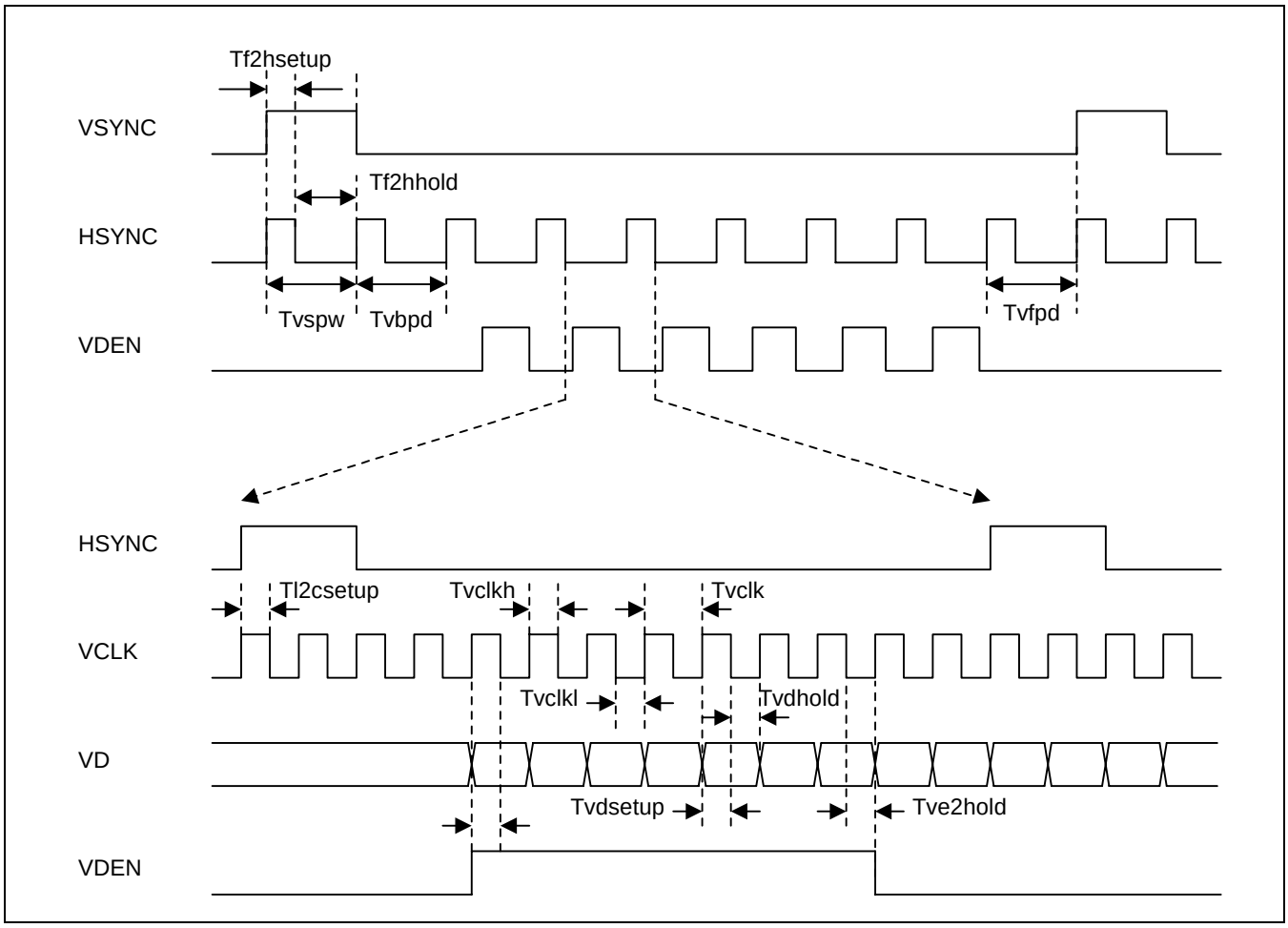


Figure 29-18. TFT LCD Controller Timing

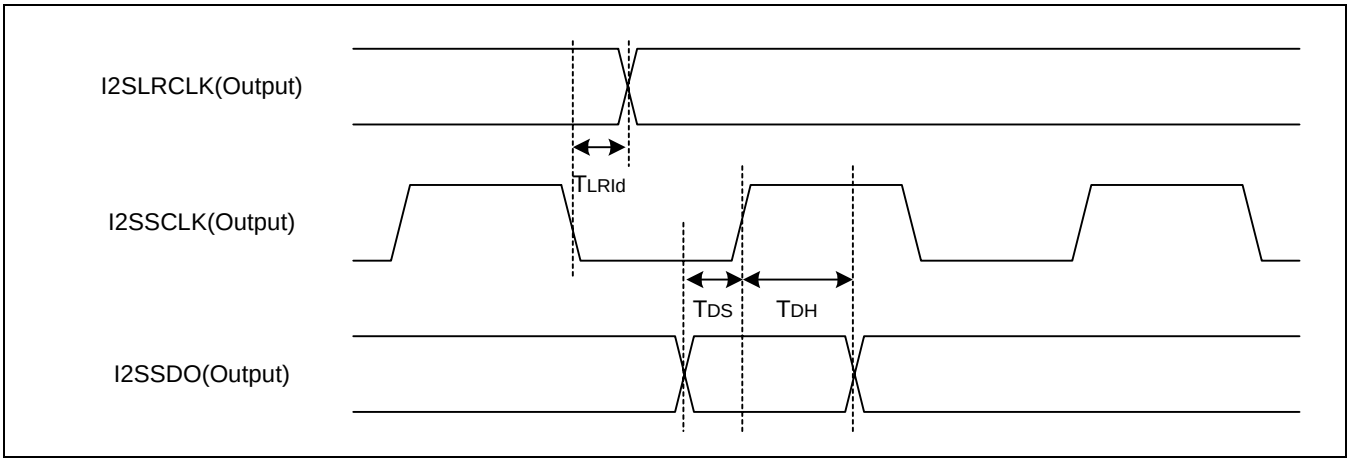


Figure 29-19. IIS Interface Timing (I2S Master Mode Only)

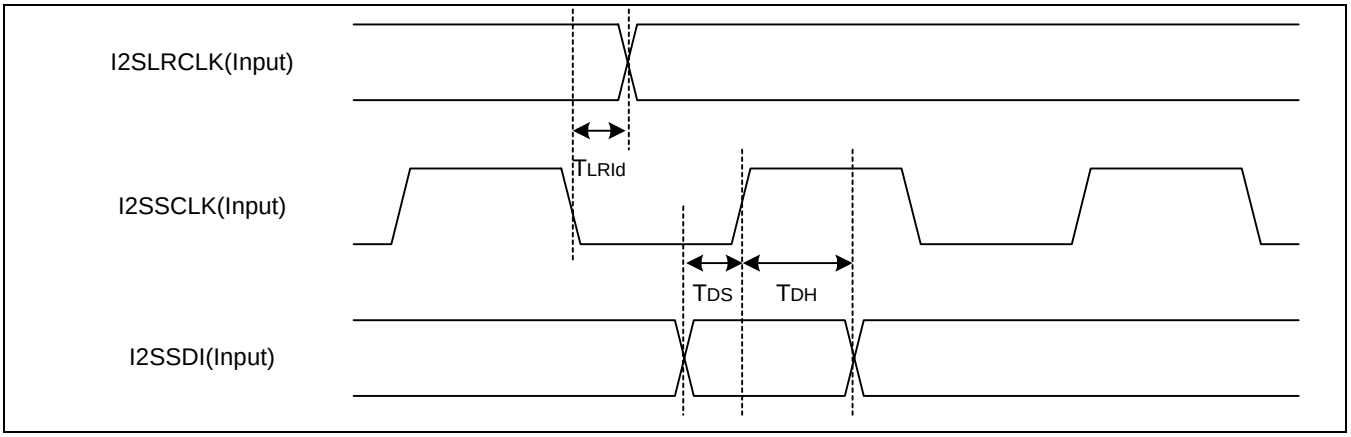


Figure 29-20. IIS Interface Timing (I2S Slave Mode Only)

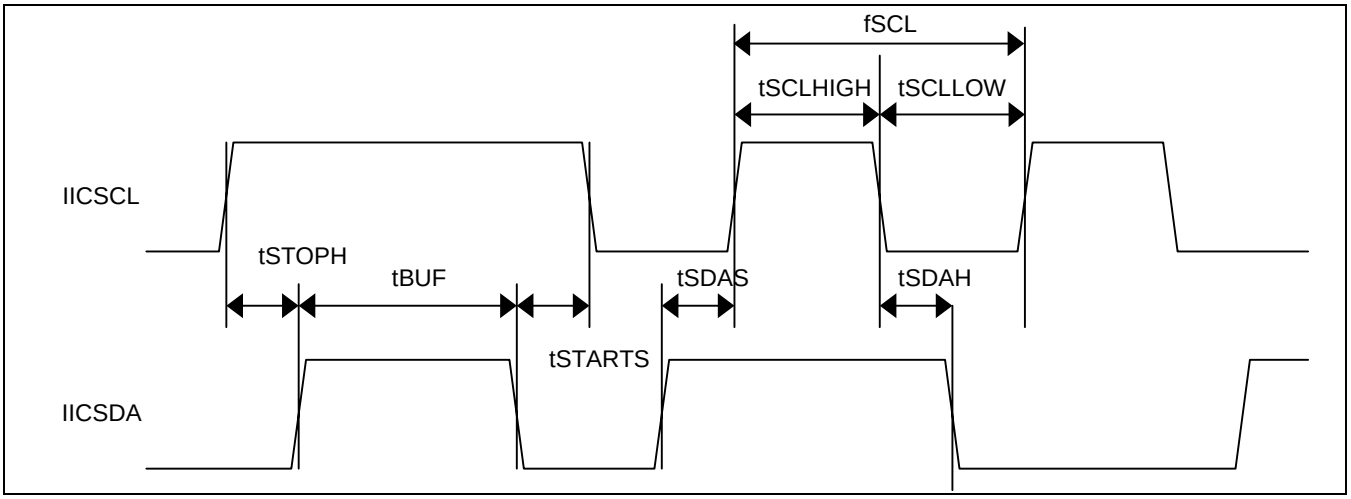


Figure 29-21. IIC Interface Timing

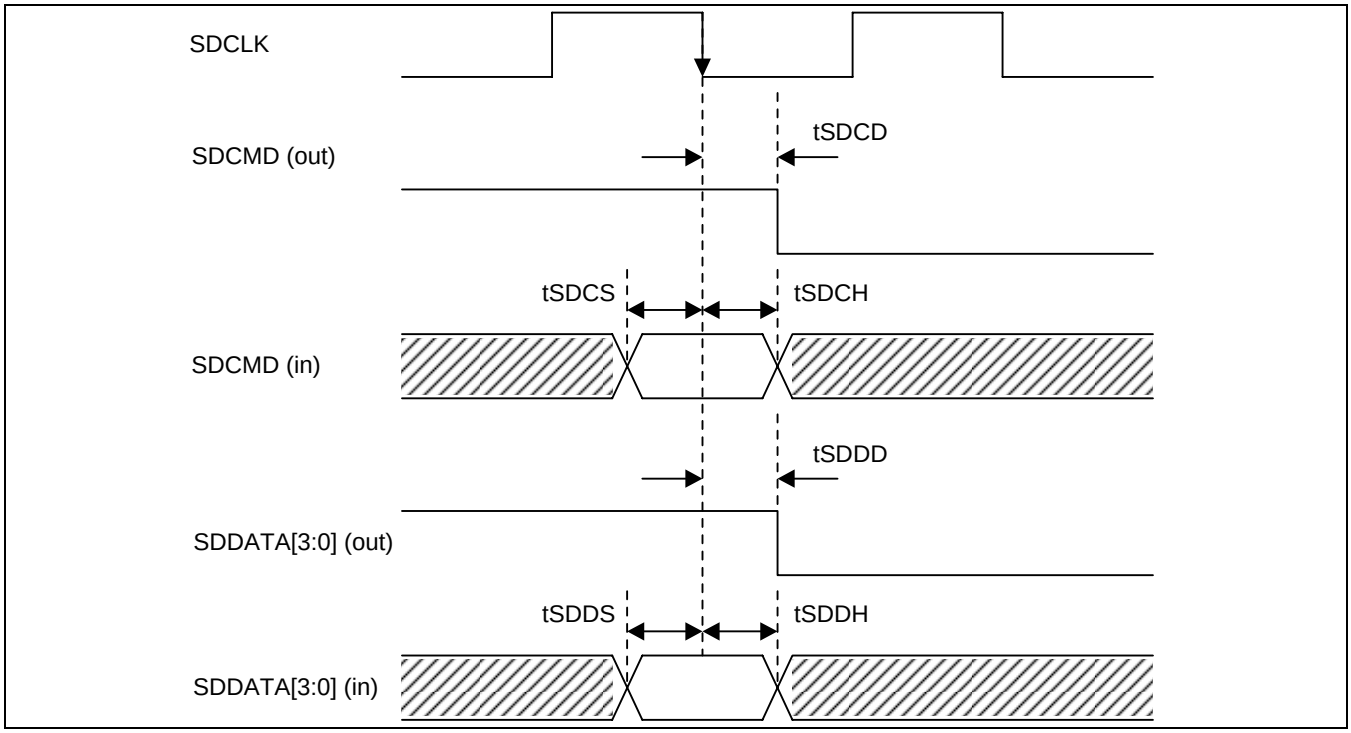


Figure 29-22. SD/MMC Interface Timing

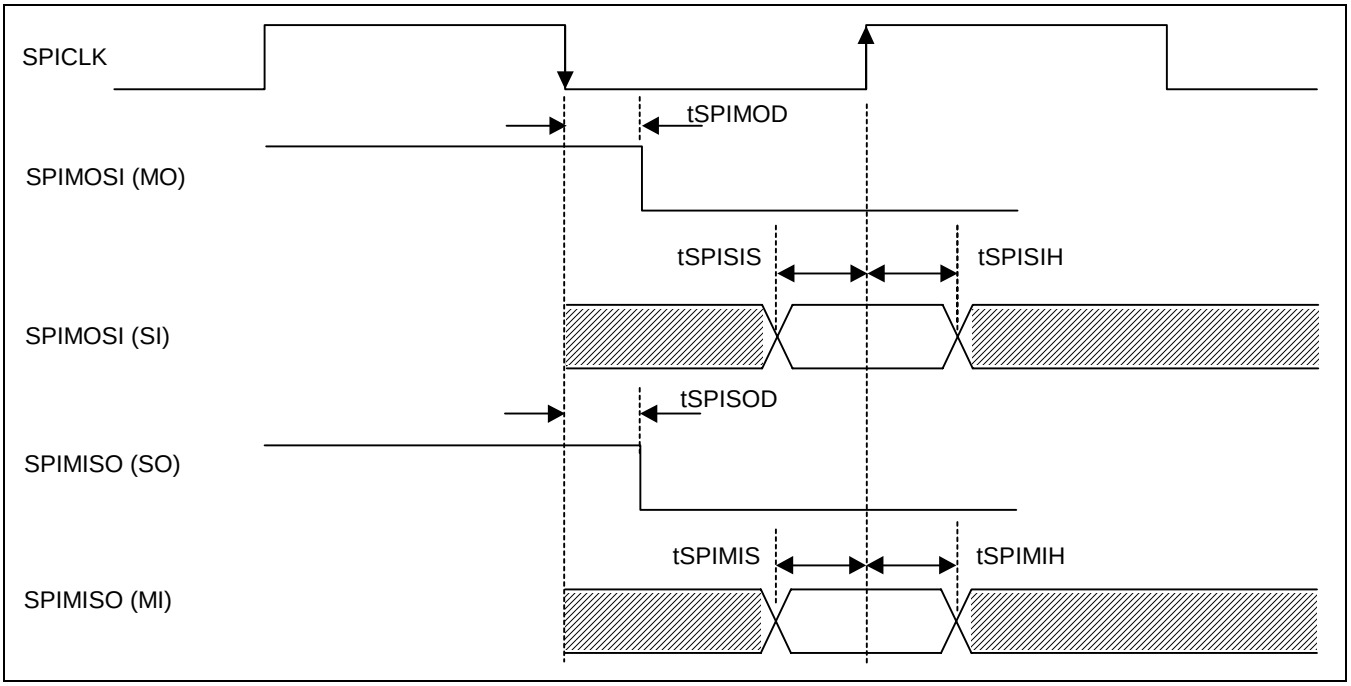


Figure 29-23. SPI Interface Timing (CPHA = 1, CPOL = 1)

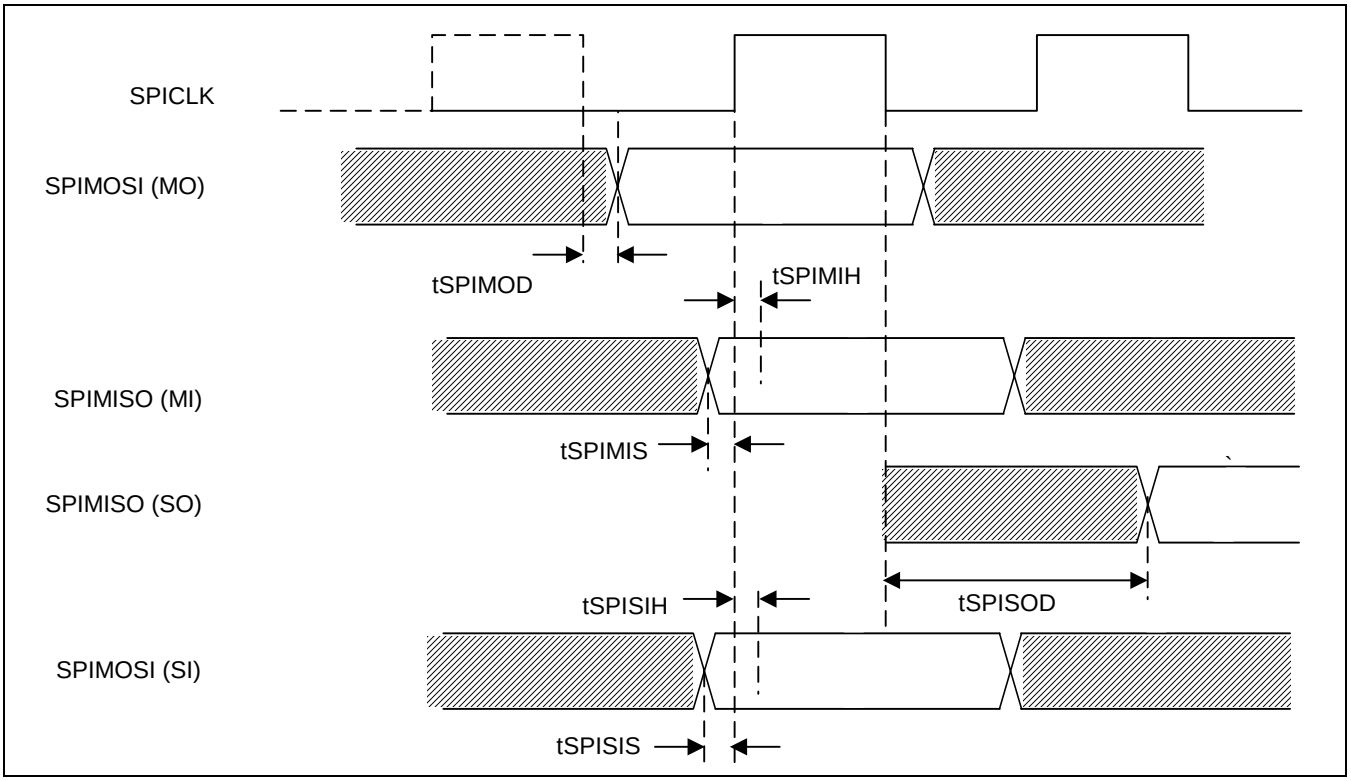


Figure 29-24. High Speed SPI Interface Timing (CPHA = 0, CPOL = 0)

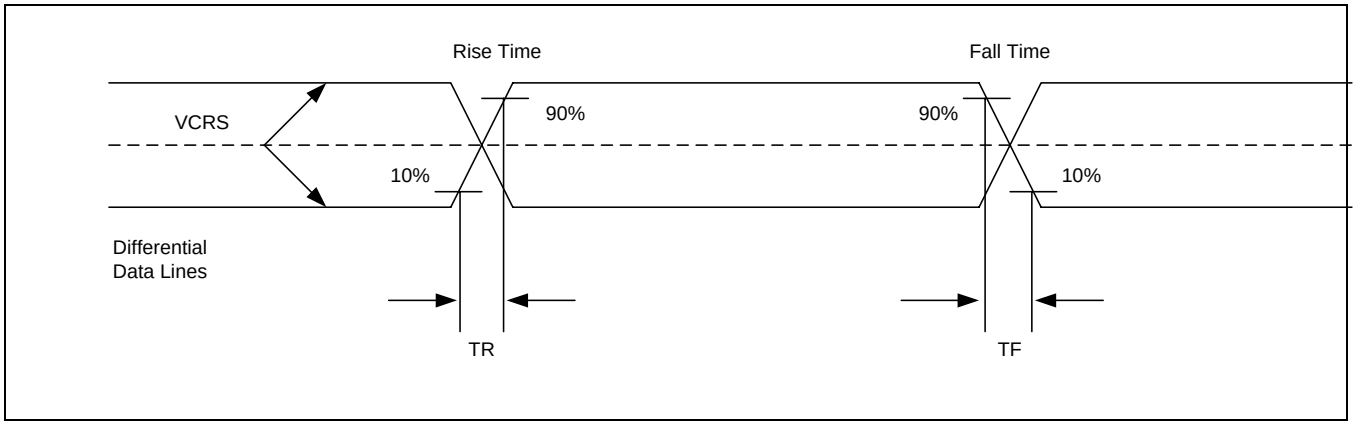


Figure 29-25. USB Timing (Data signal rise/fall time)

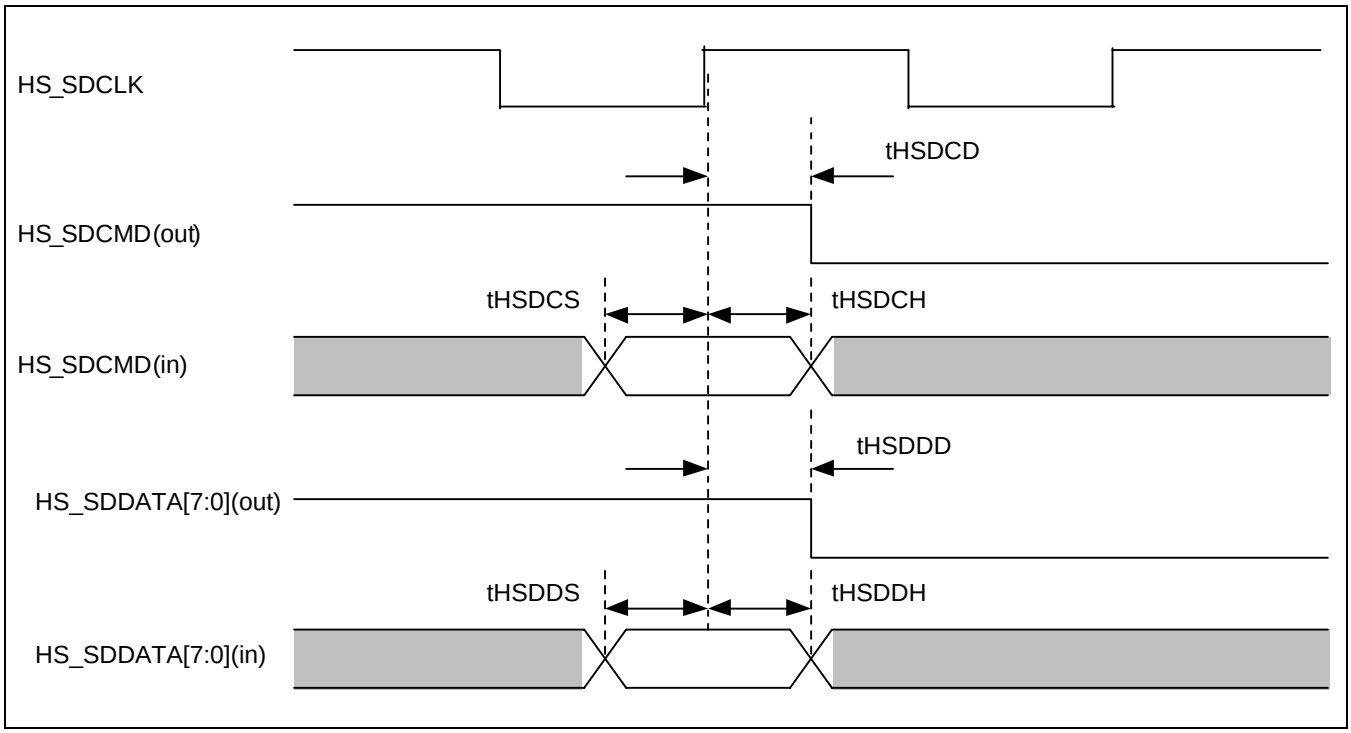


Figure 29-26. High Speed SDMMC Interface Timing

Table 29-12. Clock Timing Constants

(VDDi= 1.3V± 0.05V (400MHz), VDDi= 1.15V± 0.05V (533MHz), TA = -40 to 85°C, VDD_OP1 = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Crystal clock input frequency	f_{XTAL}	10	-	30	MHz
Crystal clock input cycle time	$t_{XTALCYC}$	33	-	100	ns
External clock input frequency (1)	f_{EXT}	10		133	MHz
External clock input cycle time(1)	t_{EXTCYC}	7.5		100	ns
External clock input low level pulse width	t_{EXTLOW}	3.5		-	ns
External clock input high level pulse width	$t_{EXTHIGH}$	3.5		-	ns
External clock to HCLK (without PLL)	t_{EX2HC}	5		13	ns
HCLK (internal) to CLKOUT	t_{HC2CK}	3.3		8.8	ns
HCLK (internal) to SCLK	$t_{HC2SCLK}$	1.9		5.8	ns
Reset assert time after clock stabilization	t_{RESW}	4		-	XTIpll or EXTCLK
PLL Lock Time	t_{PLL}	300		-	us
Sleep mode return oscillation setting time. (2)	t_{OSC2}	2		524290	XTIpll or EXTCLK
The interval before CPU runs after nRESET is released.	$t_{RST2RUN}$	5		-	XTIpll or EXTCLK

NOTE: (1) If does not use MPLL, External clock input range is 10MHz ~ 133MHz but if use MPLL , External clock input range is 10MHz ~ 30MHz

(2) tOSC2 is programmable by setting the PWRSETCNT bits in Reset Count register.
tOSC2 = PWRSETCNT * 2^11 + 2

Table 29-13. SSMC Timing Constants

(VDDi= 1.3V± 0.05V (400MHz), VDDi= 1.15V± 0.05V (533MHz), TA = -40 to 85°C, VDD_SRAM = 1.8V ± 0.1V)

Parameter	Symbol		Min	Typ	Max	Unit
SSMC Chip Select Delay	tCSD	bank0	2.4	–	7.3	ns
		bank1	2.4		7.2	
		bank2	2.5		7.6	
		bank3	2.5		7.2	
		bank4	2.3		6.9	
		bank5	2.4		7.1	
SSMC Output Enable Delay	tOED		2.1	–	6.3	ns
SSMC Write Enable Delay	tWED		2.2	–	6.3	ns
SSMC Address Delay	tADDRD		2.5	–	7.3	ns
SSMC Data Output Delay	tDOD		3.1	–	8.9	ns
SSMC nWAIT setup time	tWS		2.3	–	5	ns
SSMC nWAIT hold time	tWH		0	–	0	ns

Table 29-14. NFCON Bus Timing Constants

(VDDi= 1.3V± 0.05V (400MHz), VDDi= 1.15V± 0.05V (533MHz), TA = -40 to 85°C, VDD_SRAM = 1.8V ± 0.1V)

Parameter	Symbol	Min	Max	Unit
NFCON Chip Enable delay	t_{CED}	-	7.83	ns
NFCON CLE delay	t_{CLED}	-	8.96	ns
NFCON ALE delay	t_{ALED}	-	8.38	ns
NFCON Write Enable delay	t_{WED}	-	9.42	ns
NFCON Read Enable delay	t_{RED}	-	10.03	ns
NFCON Write Data delay	t_{WDD}	-	8.78	ns
NFCON Read Data Setup requirement time	t_{RDS}	1.00	-	ns
NFCON Read Data Hold requirement time	t_{RDH}	0.20	-	ns

Table 29-15. Memory Interface Timing Constants (SDRAM)

(VDDi= 1.3V± 0.05V (400MHz), VDDi= 1.15V± 0.05V (533MHz), TA = -40 to 85°C, VDD_SDRAM = 1.8V ± 0.1V, 133MHz, CL = 25pF)

Parameter	Symbol	Min	Max	Unit
SDRAM Address Delay	t_{SAD}	1.58	5.61	ns
SDRAM Chip Select Delay	t_{SCSD}	1.98	5.27	ns
SDRAM Row active Delay	t_{SRD}	1.88	4.67	ns
SDRAM Column active Delay	t_{SCD}	1.63	3.96	ns
SDRAM Byte Enable Delay	t_{SBED}	1.80	4.58	ns
SDRAM Write enable Delay	t_{SWD}	2.13	5.51	ns
SDRAM read Data Setup time	t_{SDS}	1.50	-	ns
SDRAM read Data Hold time	t_{SDH}	1.50	-	ns
SDRAM output Data Delay	t_{SDD}	1.59	5.65	ns
SDRAM Clock Enable Delay	t_{CKED}	1.62	4.11	ns

NOTE: If CL increase over the 25pF, operation conditions follow the guide table

Load Capacitance (CL)	Bus clock	Voltage
< 25 pF	133MHz	1.8V± 0.1V
25 pF < CL < 50 pF	100MHz	
50 pF < CL < 70 pF	90MHz	

Table 29-16. DMA Controller Module Signal Timing Constants

(VDDi= 1.3V± 0.05V (400MHz), VDDi= 1.15V± 0.05V (533MHz), TA = -40 to 85°C, VDD_OP2 = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
eXternal Request Setup	t_{XRS}	6.4/6.4	–	9.9/9.9	ns
aCcess to Ack Delay when Low transition	t_{CADL}	3.1/2.8		7.8/7.1	ns
aCcess to Ack Delay when High transition	t_{CADH}	2.8/2.5		7.8/6.9	ns
eXternal Request Delay	t_{XAD}	2	–	–	HCLK

Table 29-17. TFT LCD Controller Module Signal Timing Constants

(VDDi= 1.3V± 0.05V (400MHz), VDDi= 1.15V± 0.05V (533MHz), TA = -40 to 85°C, VDD_LCD = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Units
VCLK pulse width	Tvclk	18	200	–	ns
VCLK pulse width high	Tvclkh	0.3	–	–	Pvclk(1)
VCLK pulse width low	Tvclkl	0.3	–	–	Pvclk
Vertical sync pulse width	Tvspw	VSPW + 1	–	–	Phclk(2)
Vertical back porch delay	Tvbpd	VBPD+1	–	–	Phclk
Vertical front porch dealy	Tvfpd	VFPD+1	–	–	Phclk
Hsync setup to VCLK falling edge	Tl2csetup	0.3	–	–	Pvclk
VDEN set up to VCLK falling edge	Tde2csetup	0.3	–	–	Pvclk
VDEN hold from VCLK falling edge	Tde2chold	0.3	–	–	Pvclk
VD setup to VCLK falling edge	Tvd2csetup	0.3	–	–	Pvclk
VD hold from VCLK falling edge	Tvd2chold	0.3	–	–	Pvclk
VSYNC setup to HSYNC falling edge	Tf2hsetup	HSPW + 1	–	–	Pvclk
VSYNC hold from HSYNC falling edge	Tf2hhold	HBPD + HFPD + HOZVAL + 3	–	–	Pvclk

NOTES :

1. VCLK period
2. HSYNC period

Table 29-18. IIS Controller Module Signal Timing Constants(I2S Master Mode Only)

(VDDi= 1.3V± 0.05V (400MHz), VDDi= 1.15V± 0.05V (533MHz), TA = –40 to 85 °C, VDD_OP2 = 3.3V ± 0.3V)

Parameter	Symbol	Min.	Typ.	Max	Unit
LR Clock Input Delay	TLRId	5	-	13	ns
Serial Data Setup Time	TDS	10	-		ns
Serial Data Hold Time	TDH	10	-		ns

Table 29-19. IIS Controller Module Signal Timing Constants(I2S Slave Mode Only)

(VDDi= 1.3V± 0.05V (400MHz), VDDi= 1.15V± 0.05V (533MHz), TA = –40 to 85 °C, VDD_OP2 = 3.3V ± 0.3V)

Parameter	Symbol	Min.	Typ.	Max	Unit
LR Clock Input Delay	TLRId	0	-		ns
Serial Data Setup Time	TDS	10	-		ns
Serial Data Hold Time	TDH	10	-		ns

Table 29-20. IIC BUS Controller Module Signal Timing

(VDDi= 1.3V± 0.05V (400MHz), VDDi= 1.15V± 0.05V (533MHz), TA = -40 to 85°C, VDD_OP2 = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ.	Max	Unit
SCL clock frequency	f_{SCL}	–	–	std. 100 fast 400	kHz
SCL high level pulse width	$t_{SCLHIGH}$	std. 4.0 fast 0.6	–	–	μs
SCL low level pulse width	t_{SCLLOW}	std. 4.7 fast 1.3	–	–	μs
Bus free time between STOP and START	t_{BUF}	std. 4.7 fast 1.3	–	–	μs
START hold time	t_{STARTS}	std. 4.0 fast 0.6	–	–	μs
SDA hold time	t_{SDAH}	std. 0 fast 0	–	std. - fast 0.9	μs
SDA setup time	t_{SDAS}	std. 250 fast 100	–	–	ns
STOP setup time	t_{STOPH}	std. 4.0 fast 0.6	–	–	μs

NOTES: Std. means Standard Mode and fast means Fast Mode.

1. The IIC data hold time(tSDAH) is minimum 0ns.
   (IIC data hold time is minimum 0ns for standard/fast bus mode in IIC specification v2.1.)
   Please check the data hold time of your IIC device if it's 0 nS or not.
2. The IIC controller supports only IIC bus device(standard/fast bus mode), not C bus device.

Table 29-21. SD/MMC Interface Transmit/Receive Timing Constants

(VDDi= 1.3V± 0.05V (400MHz), VDDi= 1.15V± 0.05V (533MHz), TA = -40 to 85°C, VDD_SD = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ.	Max	Unit
SD Command output Delay time	t_{SDCD}	0	–	0.1	ns
SD Command input Setup time	t_{SDCS}	15.0	–	–	ns
SD Command input Hold time	t_{SDCH}	-	–	0.1	ns
SD Data output Delay time	t_{SDDD}	0.1	–	0.36	ns
SD Data input Setup time	t_{SDDS}	15.5	–	–	ns
SD Data input Hold time	t_{SDDH}	-	–	0.1	ns

Table 29-22. SPI Interface Transmit/Receive Timing Constants

(VDDi= 1.3V± 0.05V (400MHz), VDDi= 1.15V± 0.05V (533MHz), TA = -40 to 85°C, VDD_SD = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ.	Max	Unit
SPI MOSI Master Output Delay time	t_{SPIMOD}	0	–	1.3	ns
SPI MOSI Slave Input Setup time	t_{SPISIS}	0.0	–	0.0	ns
SPI MOSI Slave Input Hold time	t_{SPISIH}	0.0	–	0.0	ns
SPI MISO Slave output Delay time	t_{SPISOD}	4.4	–	15.0	ns
SPI MISO Master Input Setup time	t_{SPIMIS}	0 / 13.0 *	–	–	ns
SPI MISO Master Input Hold time	t_{SPIMIH}	0.0	–	0.0	ns

NOTE: * tSPIMIS value is 0 when the feedback clock use mode

Table 29-23. High Speed SPI Interface Transmit/Receive Timing Constants

(VDDi= 1.3V± 0.05V (400MHz), VDDi= 1.15V± 0.05V (533MHz), TA = -40 to 85°C, VDD_SD = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ.	Max	Unit
SPI MOSI Master Output Delay time	t_{SPIMOD}	0.9	–	3.4	ns
SPI MOSI Slave Input Setup time	t_{SPISIS}	1	–	1	ns
SPI MOSI Slave Input Hold time	t_{SPISIH}	1	–	1	ns
SPI MISO Slave output Delay time	t_{SPISOD}	6.6	–	17.5	ns
SPI MISO Master Input Setup time	t_{SPIMIS}	1	–	2	ns
SPI MISO Master Input Hold time	t_{SPIMIH}	1	–	1	ns

Table 29-24. USB Electrical Specifications

(VDD12V = 1.2V ± 5%, TA = -40 to 85°C, VDDA33x = 3.3V ± 0.3V)

Parameter	Symbol	Condition	Min	Max	Unit
Supply Current					
Suspend Device	ICCS				µA
Leakage Current					
Hi-Z state Input Leakage	ILO	0V < VIN < 3.3V	-10	10	µA
Input Levels					
Differential Input Sensitivity	VDI	| (D+) – (D-) |	0.2		V
Differential Common Mode Range	VCM	Includes VDI range	0.8	2.5	
Single Ended Receiver Threshold	VSE		0.8	2.0	
Output Levels					
Static Output Low	VOL	RL of 1.5Kohm to 3.6V		0.3	V
Static Output High	VOH	RL of 15Kohm to GND	2.8	3.6	
Capacitance					
Transceiver Capacitance	CIN	Pin to GND		20	pF

Table 29-25. USB Full Speed Output Buffer Electrical Characteristics

(VDDi= 1.3V± 0.05V (400MHz), VDDi= 1.15V± 0.05V (533MHz), TA = -40 to 85°C, VDDA33x = 3.3V ± 0.3V)

Parameter	Symbol	Condition	Min	Max	Unit
Driver Characteristics					
Transition Time Rise Time Fall Time	 TR TF	 CL = 50pF CL = 50pF	 4.0 4.0	 20 20	 ns
Rise/Fall Time Matching	TRFM	(TR / TF)	90	110	%
Output Signal Crossover Voltage	VCRS		1.3	2.0	V
Drive Output Resistance	ZDRV	Steady state drive	28	43	ohm

Table 29-26. USB High Speed Output Buffer Electrical Characteristics

(VDDi= 1.3V± 0.05V (400MHz), VDDi= 1.15V± 0.05V (533MHz), TA = -40 to 85°C, VDDA33x = 3.3V ± 0.3V)

Parameter	Symbol	Condition	Min	Max	Unit
Driver Characteristics					
Transition Time Rising Time Falling Time	 TR TF	 	 500 500	 	 ps ps
Drive Output Resistance	ZDRV	Steady state drive	40.5	49.5	ohm

Table 29-27. High Speed SDMMC Interface Transmit/Receive Timing Constants

(VDDi= 1.3V± 0.05V (400MHz), VDDi= 1.15V± 0.05V (533MHz), TA = -40 to 85°C, VDD_SD = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ.	Max	Unit
SD Command output Delay time	t_{SDCD}	0.4	–	6.8	ns
SD Command input Setup time	t_{SDCS}	12.2	–	–	ns
SD Command input Hold time	t_{SDCH}	-	–	0.1	ns
SD Data output Delay time	t_{SDDD}	0.4	–	6.6	ns
SD Data input Setup time	t_{SDDS}	12.3	–	–	ns
SD Data input Hold time	t_{SDDH}	-	–	0.1	ns

NOTES

30 MECHANICAL DATA

PACKAGE DIMENSIONS

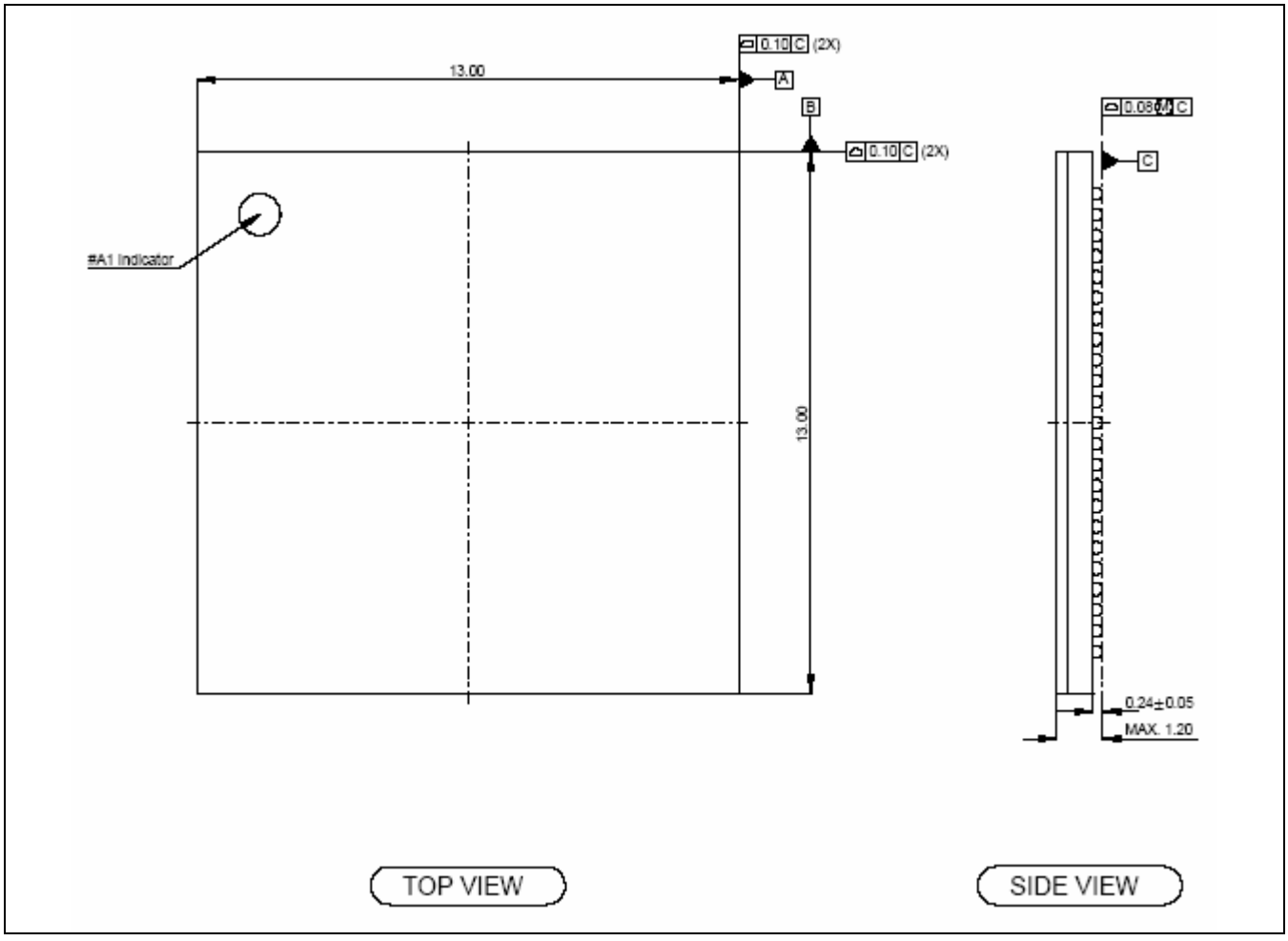


Figure 30-1. 400-FBGA-1313 Package Dimension 1 (Top View)

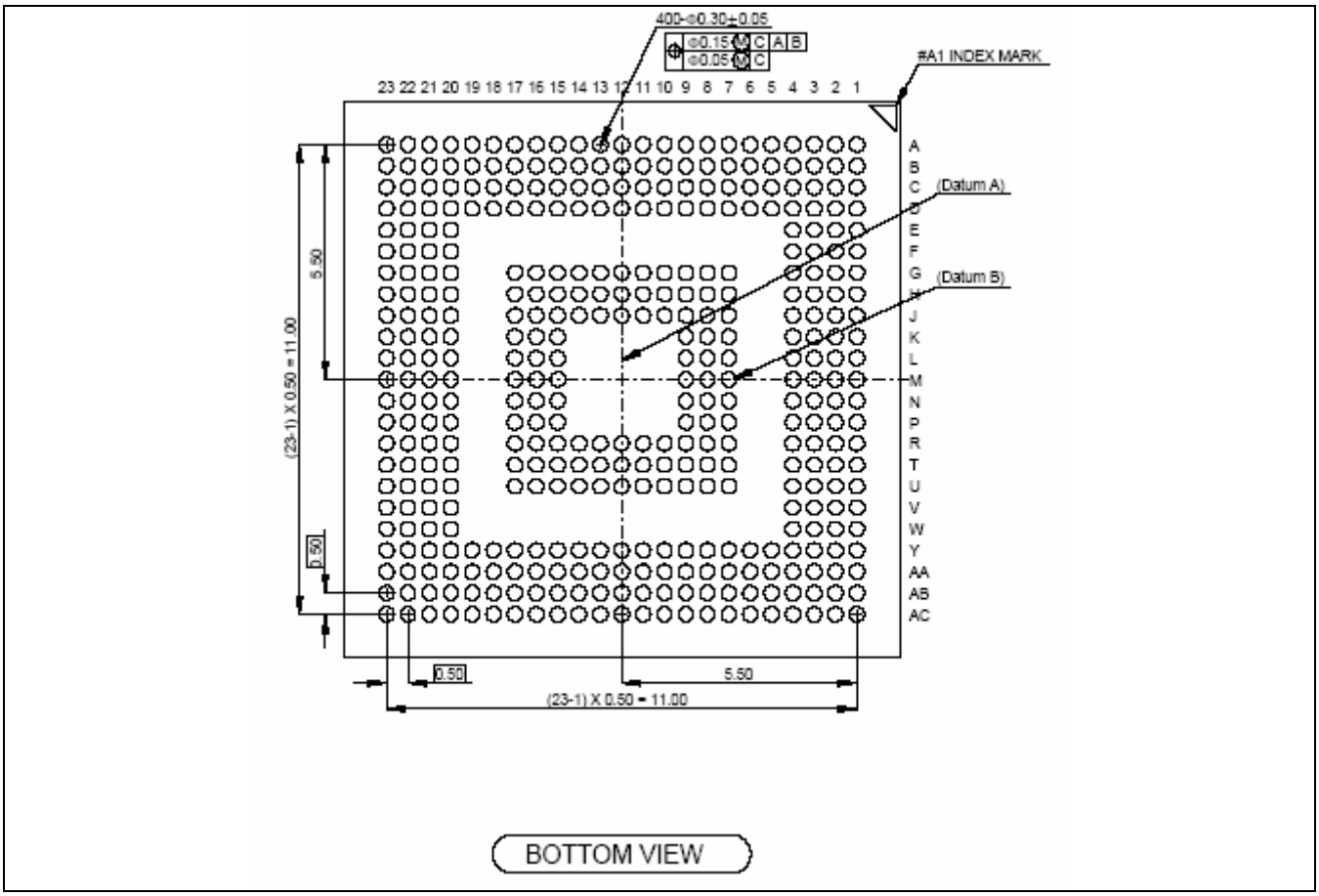


Figure 30-2. 400-FBGA-1313 Package Dimension 2 (Bottom View)