phyCORE-TC1130

Preliminary

Hardware Manual

Preliminary Version: April 2005

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Preface

This phyCORE-TC1130 Hardware Manual describes the board's design and functions. Precise specifications for Infineon's TC1130 Tricore microcontroller series controller can be found in the enclosed microcontroller Data Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration of Electro Magnetic Conformance of the PHYTEC phyCORE-TC1130

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformance only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-TC1130 is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports all common 8- and 16-bit as well as selected 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional micro-, mini- and phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware, design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The phyCORE-TC1130 belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled Microvias are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-TC1130 is a subminiature (72 x 57 mm) insert-ready Single Board Computer populated with Infineon's TC1130 Tricore microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density pitch (0.635 mm) connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or Data Sheet. The descriptions in this manual are based on the Infineon TC1130 Tricore microcontroller. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-TC1130.

The phyCORE-TC1130 offers the following features:

- subminiature SBC in phyCORE dimensions 72 x 57 mm with two 160-pin high-density (0.635 mm) Molex connectors, enabling it to be plugged like a “big chip” into target application
- Processor: Infineon Tricore TC1130, 20 MHz external clock
- **Internal Components of the phyCORE-TC1130:**
  - High performance 32-bit TriCORE CPU
  - Memory Management Unit (MMU)
  - DMA Controller
  - two synchronous serial interfaces
  - three UARTs
  - MultiCAN 2.0B (4 Nodes)
  - Capture and Compare units
  - Fast Ethernet Interface
  - General Purpose Timer Unit (GPTU) with three 32-bit timers
  - Multi-purpose I/O signals
- **Memory Configuration[1]:**
  - DRAM (2 Banks): 128 MByte maximum
  - Flash-ROM: 32 MByte Intel Strata Flash maximum;
  - I^2C memory: 4 kByte EEPROM (up to 32 kByte) (optional I^2C FRAM (512 Byte), or I^2C SRAM (256 Byte) can be used)
  - SPI memory: EEPROM for Bootstrap code
- I^2C Real-Time Clock with calendar and alarm functions
- Ethernet PHY 10/100 MBit TP
- UART: RS-232 transceiver for two channels (RxD/TxD); TTL level can be configured
- MultiCAN port: SN65HVD23x transceiver for all channels; TTL level can be configured
- JTAG/Debug port
- Option: Lattice PLD LC4064 / MAX 7301 port expander
- Available in standard- (0...+70° C) temperature range

[1]: Please contact PHYTEC for more information about additional modul configurations.

1.1 Block Diagram

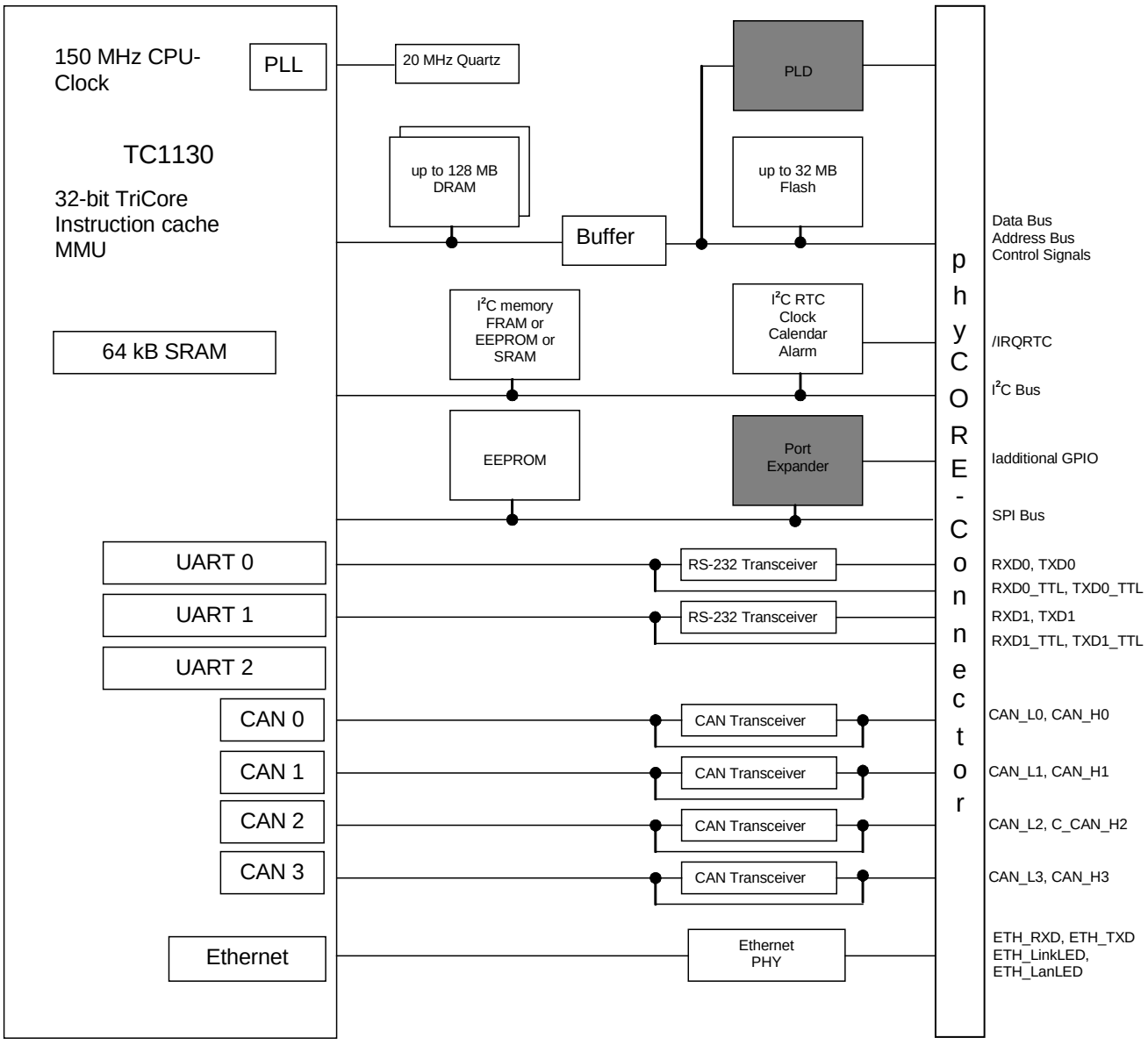


Figure 1: Block Diagram phyCORE-TC1130

1.2 View of the phyCORE-TC1130

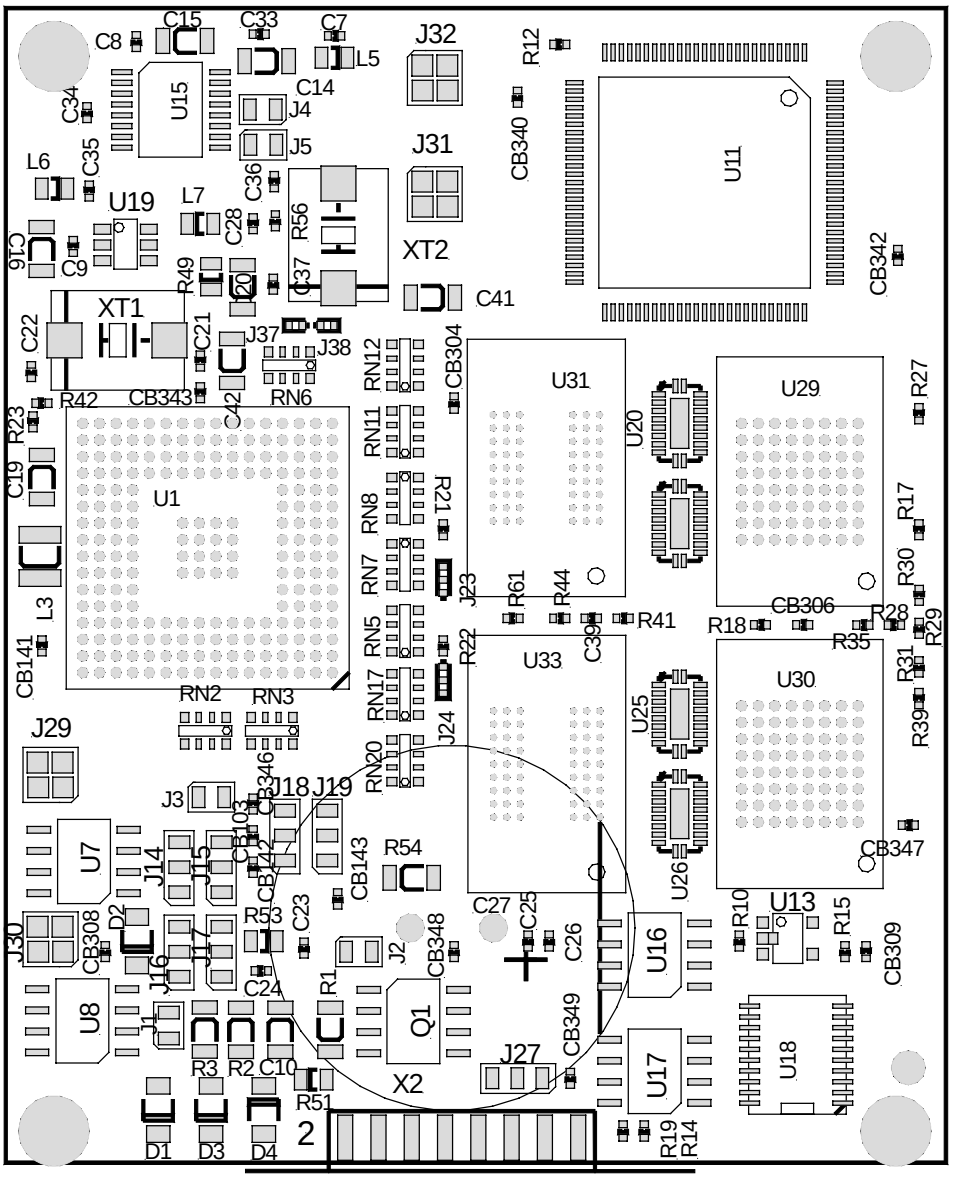


Figure 2: View of the phyCORE-TC1130 (Controller Side)

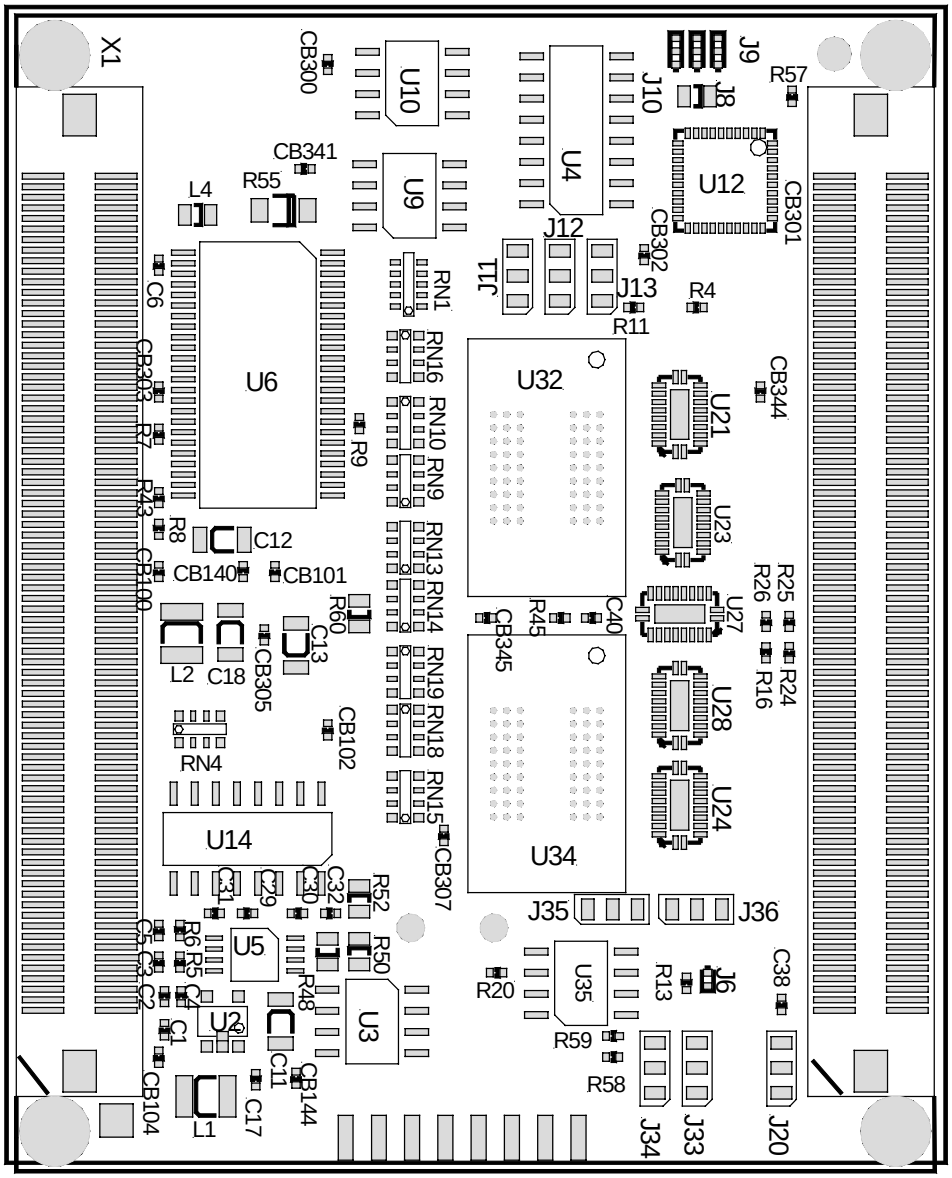


Figure 3: View of the phyCORE-TC1130 (Connector Side)

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 4* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as phyCORE-connector). This allows the phyCORE-TC1130 to be plugged into any target application like a "big chip".

A new numbering scheme for the pins on the phyCORE-connector has been introduced with the phyCORE specifications. This enables quick and easy identification of desired pins and minimizes errors when matching pins on the phyCORE module with the phyCORE-connector on the appropriate PHYTEC Development Board or in user target circuitry.

The numbering scheme for the phyCORE-connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number. Pin 1A, for example, is always located in the upper left hand corner of the matrix. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (*refer to Figure 4*).

The numbered matrix can be aligned with the phyCORE-TC1130 (viewed from above; phyCORE-connector pointing down) or with the socket of the corresponding phyCORE Development Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin 1A) is thus covered with the corner of the phyCORE-TC1130 marked with a white triangle. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module's phyCORE-connector as well as mating connectors on the phyCORE Development Board or target hardware, thereby considerably reducing the risk of pin identification errors.

Since the pins are exactly defined according to the numbered matrix previously described, the phyCORE-connector is usually assigned a single designator for its position (X1 for example). In this manner the phyCORE-connector comprises a single, logical unit regardless of the fact that it could consist of more than one physical socketed connector. The location of row 1 on the board is marked by a white triangle on the PCB to allow easy identification.

The following figure (*Figure 4*) illustrates the numbered matrix system. It shows a phyCORE-TC1130 with SMT phyCORE-connectors on its underside.

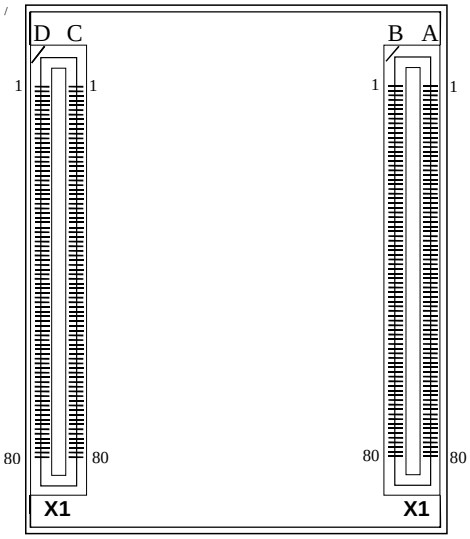


Figure 4: Pinout of the phyCORE-Connector (Connector Side)

Many of the controller port pins accessible at the connectors along the edges of the board have been assigned alternate functions that can be activated via software.

Table 1 provides an overview of the pinout of the phyCORE-connector , as well as descriptions of possible alternative functions. *Please refer to the Infineon TC1130 User's Manual/Data Sheet for details on the functions and features of controller signals and port pins*.

Pin Number	Signal	I/O	PU/ PD	Description
Pin Row X1A				
1A	NC	-	-	not connected
2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A	GND	-	-	Ground 0 V
3A	P09	I/O	PUC	Controller port 0.9, can be configured as external interrupt input Alternative use: TXDCAN0 (*refer to J14*)
4A	/NMI	I	PUC	/NMI Interrupt of the controller
5A	x/CS3	O	PUC	Bufferd Chip Select output
6A	xALE	O	PDC	Bufferd Address latch enable
8A	x/BC0	O	PUC	Bufferd Byte Control signal for data lines D[0..7].
9A, 10A, 11A, 13A, 14A, 15A, 16A, 18A, 24A, 25A, 26A, 28A	xA1, xA2, xA4, xA7, xA9, xA10, xA12, xA15, xA17, xA18, xA20, xA23	O	PUC	Bufferd Address lines, are used to access on-board flash and external memory devices
19°, 20A, 21A, 23A, 29A, 30A, 31A, 33A, 38A, 39A, 40A, 41A, 43A, 44A, 45A, 46A	xD1, xD2, xD4, xD7, xD9, xD10, xD12, xD15, xD18, xD19, xD20, xD22, xD25, xD27, xD28, xD30	I/O	PUC	Bufferd Data lines, are used to access on-board flash and external memory devices
34A	x/WAIT	I	PUC PUM	Microcontroller's wait signal
35A	FL_VPEN	I	PUM	Write protect of on board flash
36A	P06	I/O	PUC	GPTU I/O line 6 Alternative use: - SPI-Chip Select signal 0 - Hold acknowledge I/O of the processor
48A	PLD_TMS	I	PUM	TMS-Signal of the PLD JTAG-Interface
49A	x/WR	O	PUC	Bufferd Microcontroller's write signal
50A	xBFCLKI	I	-	Bufferd burst flash clock input (clock feedback)

Pin Number	Signal	I/O	PU/ PD	Description	
Pin Row X1A					
51A	xBFCLKO	O	-	Burst flash clock output	
53A	PLD_TCK	I	PDM	TCK signal of the PLD JTAG-interface	
54A	PLD_TDO	O	-	TDO signal of the PLD JTAG-interface	
		I/O	-	PLD	Port-expander
55A,	EGPIO40,			89,	-
56A,	EGPIO38,			29,	-
58A,	EGPIO35,			34,	-
59A,	EGPIO34,			34,	-
60A,	EGPIO32,			37,	-
61A,	EGPIO30,			65,	-
63A,	EGPIO27,			69,	29,
64A,	EGPIO26,			70,	27,
65A,	EGPIO24,			72,	23,
66A,	EGPIO22,			79,	21,
68A,	EGPIO19,			84,	17,
69A,	EGPIO18,			85,	16,
70A,	EGPIO16,			87,	14,
71A,	EGPIO14,			60,	13,
73A,	EGPIO11,			56,	8,
74A,	EGPIO10,			55,	6,
75A,	EGPIO8,			53,	2,
76A,	EGPIO6,			49,	5,
78A,	EGPIO3,			44,	24,
79A,	EGPIO2,			43,	26,
80A	EGPIO0			41	30

Pin Number	Signal	I/O	PU/ PD	Description
Pin Row X1B				
1B	RTC_CLKOUT	O	-	Realtime Clock Clockout (*refer to jumper J20*)
2B	P08	I/O	PUC	Processor's port 0.8, can be configured as external interrupt input Alternative: RXDCAN0_A (*refer to jumper J15*)
3B	P010	I/O	PUC	Processor's port 0.10, can be configured as external interrupt input Alternative: RXDCAN1_A (*refer to jumper J17*)
4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B	GND			Ground 0 V
5B	x/CS2	O	PUC	Bufferd Processor's Chip Select signal. Free to use if the second DRAM-Bank is NOT populated
6B	P011	I/O	PUC	Processor's port 0.11, can be configured as external interrupt input Alternative: TXDCAN1_A
7B	x/RD	O	PUC	Bufferd Processor's read signal
8B, 10B, 11B, 12B, 13B, 15B, 16B, 17B, 23B, 25B, 26B, 27B	xA0, xA3, xA5, xA6, xA8, xA11, xA13, xA14, xA16, xA19, xA21, xA22	O	PUC	Bufferd Address lines, are used to access on-board memory
18B, 20B, 21B, 22B, 28B, 30B, 31B, 32B, 37B, 38B, 40B, 41B, 42B, 43B, 45B, 46B	xD0, xD3, xD5, xD6, xD8,xD11, xD13, xD14, xD16, xD17, xD21, xD23, xD24, xD26, xD29, xD31	I/O	PUC	Bufferd Data lines, are used to access on-board memory
33B	x/BC1	O	PUC	Bufferd Byte control signal for data lines D[8..15].
35B	P05	I/O	PUC	Processor's port 0.5 Alternative: Processor's hold request input
36B	P07	I/O	PUC	Processor's port 0.7
47B	/CSCOMB	O	PUC	Processor's Chip Select Output for combination function
48B	xMR/W	O	PUC	Bufferd Processor's Motorola-style Read/Write output
50B	x/ADV	O		Buffers Processor's address valid output

Pin Number	Signal	I/O	PU/ PD	Description	
Pin Row X1B					
51B	x/BAA	O	PUC	Bufferd Burst address advance output	
52B	x/BC2	O	PUC	Bufferd Byte control signal for data lines D[16..23].	
53B	/BC3	O	PUC	Bufferd Byte control signal for data lines D[24..31].	
55B	PLD_TDI	I	-	TDI signal of the PLD JTAG-interface	
		I/O	-	PLD	Port-expander
56B,	EGPIO39,			88,	-
57B,	EGPIO37,			30,	-
58B,	EGPIO36,			31,	-
60B,	EGPIO33,			36,	-
61B,	EGPIO31,			64,	-
62B,	EGPIO29,			66,	-
63B,	EGPIO28,			67,	-
65B,	EGPIO25,			71,	25,
66B,	EGPIO23,			78,	22,
67B,	EGPIO21,			80,	19,
68B,	EGPIO20,			81,	18,
70B,	EGPIO17,			86,	15,
71B,	EGPIO15,			61,	13,
72B,	EGPIO13,			59,	10,
73B,	EGPIO12,			58,	9,
75B,	EGPIO9,			54,	4,
76B,	EGPIO7,			50,	7,
77B,	EGPIO5,			48,	3,
78B,	EGPIO4,			47,	1,
80B	EGPIO1			42	28

Pin Number	Signal	I/O	PU/ PD	Description
Pin Row X1C				
1C, 2C	+3V3_IN	I	-	Supply voltage +3.3 VDC
3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C	GND	-	-	Ground 0 V
4C, 5C	NC	-	-	not connected
6C	VBAT_IN	I	-	Supply voltage for the RTC
8C	RESOUT	O	-	High active Reset-output of the voltage supervisor
9C	/BOOT	I	PUM	Following a power-on reset (/PORESET) the Boot configuration of the processor is read over the inputs HWCFG[2..0]. The state of these inputs is determined via the /BOOT signal . /BOOT = low => Boot config. via J11-J13 /BOOT = high => Boot config via J8-J10
10C	/HDRESET	I/O	PUC	System's hard-reset signal, /HDRESET is controlled by open-drain drivers
11C	/PORESET	I	PUC	Processor's power-on reset, the boot configuration is fetched following a power-on reset
13C, 14C, 15C	P00, P03, P02	I/O		I/O port P0 Alternative: signals of ASC 1/2 (TTL) RXD1B TXD1B RXD2B
16C	/SPIEEPWP	I	PUM	Drive low to enable write protection of SPI-EEPROM
18C	CAN_H1	I/O	-	CANH output of the CAN transceiver for the 2nd CAN node
19C	RXD1_TTL	I	-	Receive line (A) of the 2nd TC1130 UART Alternative: port P2.8. If the alternative function is used, solder jumper J19 must be open in order to disconnect the RS-232 transceiver from the signal
20C	TXD1_TTL	O	-	Transmit line (A) of the 2nd TC1130 UART Alternative: port P2.9
21C	RxD1	I	-	RxD input of the RS-232 transceiver for the 2nd serial interface, J19 must be closed to use this interface
23C	TxD1	O	-	TxD output of the RS-232 transceiver for the 2nd serial interface, J18 must be closed to use this interface

Pin Number	Signal	I/O	PU/ PD	Description
Pin Row X1C				
24C	SDA1	I/O	-	IIC Data Line 1 Alternative: port P2.14
25C	SCL1	O		IIC clock line 1 Alternative: port P2.15
26C	MRST1	I/O	PUC	Master transmit / slave receive output / input of the 2nd synchronous serial interface Alternative: port P2.5
28C	MTSR1	I/O	PUC	Master receive / slave transmit input / output of the 2nd synchronous serial interface Alternative: port P2.6
29C	SCLK1	I/O	PUC	SSC1 clock input/output of the 2nd synchronous serial interface Alternative: poert P2.7
30C	/E_INT	O	PUM	Interrupt output of the Ethernet PHY
31C	SCL0	I/O	-	IIC clock signal Alternative: port P2.13
33C	E_LINK	O	-	Link Good signal from the on-board Ethernet PHY
34C	E_SPEED	O	-	Speed indication from the on-board Ethernet PHY
35C	E_RX-	I	-	RxD- input of the 100BASE-T receiver from the on-board Ethernet PHY
36C	E_TX-	O	-	TxD- output of the 100BASE-T transmitter from the on-board Ethernet PHY
38C	/TRCLK	O	-	Processor´s Trace Clock for OCDS_L2 lines
39C	/BRKIN	I	PUC	Processors OCDS Break Input (please refer to chapter 5 “Power-On-Reset Characteristics “)
40C	/BRKOUT_A	I/O	PUC	Processors OCDS Break (A) Out Alternative: port 4.7
41C	/TRST	I	PDC	Processors JTAG Reset Input
43C	CAN_L2	I/O	PUC	CANL output of the CAN transceiver for the 3rd CAN node Alternative: port 0.12
44C	CAN_H2	I/O	PUC	CANH output of the CAN transceiver for the 3rd CAN node Alternative: port 0.13
45C	CAN_L3	I/O	PUC	CANL output of the CAN transceiver for the 4th CAN node Alternative: port 0.14

Pin Number	Signal	I/O	PU/ PD	Description
Pin Row X1C				
46C, 48C, 49C, 50C	USB 1.1 USBCLK VMI VMO USBOE	I/O	PUC	USB-Interface Alternative: port 4.0 4.3 4.5 4.6
51C, 53C, 54C, 55C, 56C, 58C, 59C, 60C	P31 P34 P36 P37 P39 P312 P314 P315	I/O	PUC	I/O port 3
61C	xHWCFG1	I	PUC	Processor´s hardware configuration input 1 The status of these Pin will be latched after Reset, if Signal /BOOT is low. (please refer to chapter 5 “Power-On-Reset Characteristics “)
63C	IICEEPWP	I	PDM	Drive high to enable write protection of the on-board IIC-EEPROM
64C	MII_TXCLK	I	PDC	Processor´s MII-Interface Transmit Clock
65C, 66C, 68C, 69C, 70C; 71C, 73C, 74C	P114 P112 P19 P18 P16 P14 P11 P10	I/O	PUC	I/O port 1
75C	DAC0	O	-	Output of the on-board DAC-converter
76C, 78C 79C, 80C	AN14, AN11 AN9, AN8 AN6, AN3 AN1, AN0	I	-	Analog inputs of the on-board ADC Alternative: none
77C	GNDA	-	-	Analog Ground 0V for the on-board ADC. GNDA is connected with GND via solder jumper J4

Pin Number	Signal	I/O	PU/ PD	Description
Pin Row X1D				
1D, 2D	+3.3 V	I	-	Supply voltage +3.3 VDC
3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D,	GND	-	-	Ground 0 V
4D, 5D, 6D, 7D	NC	-	-	Not connected
8D	Tout	O	PUM	Alarm signal of the temperature sensor
10D	/RESIN	I	PUM	Reset input, controls the system reset /PORESET
11D, 12D	P211 P210	I/O	PUC	I/O port P2 Alternative: UART2 TTL TxD2_A_TTL RxD2_A_TTL
13D, 15D	P01 P04	I/O	PUC	I/O port P0 Alternative: TxD1_B_TTL BREQ (EBU Bus request)
16D	RXD0_TTL	I	-	Receive line of first TC1130 UART Alternative: port P20 If the alternative function is used, solder jumper J3 must be open in order to disconnect the RS-232 transceiver from the signal
17D	TXD0_TTL	O	-	Transmit line of first TC1130 UART. Alternative: port P21, TESTMODE select input, state latched duiring Reset (please refer to chapter 5 “Power-On-Reset Characteristics “)
18D	CAN_L1	I/O	-	CANL output of the CAN transceiver for the 2nd CAN node
20D	CAN_L0	I/O	-	CANL output of the CAN transceiver for the first CAN node
21D	CAN_H0	I/O	-	CANH output of the CAN transceiver for the first CAN intercace
22D	RxD0	I	-	RxD input of the RS-232 trans-ceiver for the first serial interface, J3 must be closed to use this interface

23D	TxD0	O	-	TxD output of the RS-232 transceiver for the first serial interface
25D	E_DUPLEX	O	-	Full-Duplex LED output of the on-board PHY
26D	E_NWAYEN	O	-	Collision LED output of the on-board PHY
27D	MRST0	I/O	PUC	Master transmit / slave receive output / input of the first synchronous serial interface Alternative: port 2.2
28D	MTSR0	I/O	PUC	Master receive / slave transmit input / output of the first synchronous serial interface Alternative: port 2.3

Pin Number	Signal	I/O	PU/ PD	Description
Pin Row X1D				
30D	SCLK0	I/O	PUC	Clock input/output of the first synchronous serial interface Alternative: port 2.4
31D	/E_PD	I	PUM	Power-Down Enable of the on-board PHY
32D	SDA0	I/O	-	Data line of the first IIC bus
33D	/IRQRTC	O	-	RTC interrupt output
35D	E_RX+	I	-	RxD+ input of the 100BASE-T on-board Ethernet PHY
36D	E_TX+	O	-	TxD+ output of the 100BASE-T on-board Ethernet PHY
37D	D+	I/O	-	USB D+ data line
38D	D-	I/O	-	USB D- data line
 40D, 41D, 42D, 43D	 TDI TDO TMS TCK	 I O I I	 PUC - PUC PUC	Processor´s JTAG Interface Data Input Data output State machine control clock
45D	CAN_H3	I/O	-	CANH output of the CAN transceiver for the third CAN intercace Alternative: Port 0.15, J32 must be closed and Can-Tranciever U10 must not be populated
 46D, 47D, 48D	USB 1.1 RVCI VPI VPO	I/O	PUC	USB-Interface Alternative: port 4.1 4.2 4.4
50D, 51D, 52D, 55D, 56D, 57D, 58D	P30, P32, P33, P35, P38, P310, P311, P313	I/O	PUC	I/O port P3 Alternative: Trace output for OCDS2 Debugging
60D, 61D	xHWCFG1, xHWCFG2	I	PUC	Processor´s hardware configuration input 2 and 3. The status of these Pins will be latched after Reset, if Signal /BOOT is low. (please refer to chapter 5 “Power-On-Reset Characteristics “)
 62D, 63D	 MII_MDIO, MII_RXCLK	 I/O I	 PDC PDC	Processor´s MII-Interface Data In/Out Receive Clock
65D, 66D, 67D, 68D, 70D, 71D, 72D, 73D	P115, P113, P111, P110, P17, P15, P13, P12	I/O	PUC	I/O port P1

Pin Number	Signal	I/O	PU/ PD	Description
Pin Row X1D				
75D, 76D 77D, 78D	ADC7, ADC5, ADC4, ADC2	I		Analog inputs of the on-board ADC Alternative: none
74D, 79D	GNDA	-		Analog Ground 0V for the on-board ADC. GNDA is connected with GND via solder jumper J4
80D	REFA	-		Reference voltage input for the on-board ADC, max. +3,3 VDC Pre-connected to 3V3 via solder jumper J5

Table 1: Pinout of the phyCORE-Connector X1

3 Jumpers

For configuration purposes, the phyCORE-TC1130 has 37 solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the jumper pads, while *Figure 6* and *Figure 7* indicate the location of the jumpers on the module.

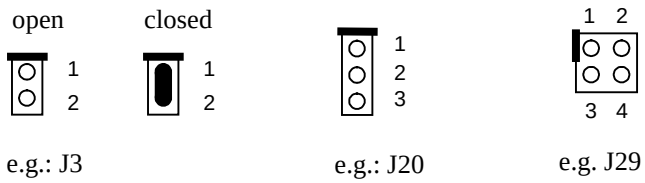


Figure 5: Numbering of the Jumper Pads

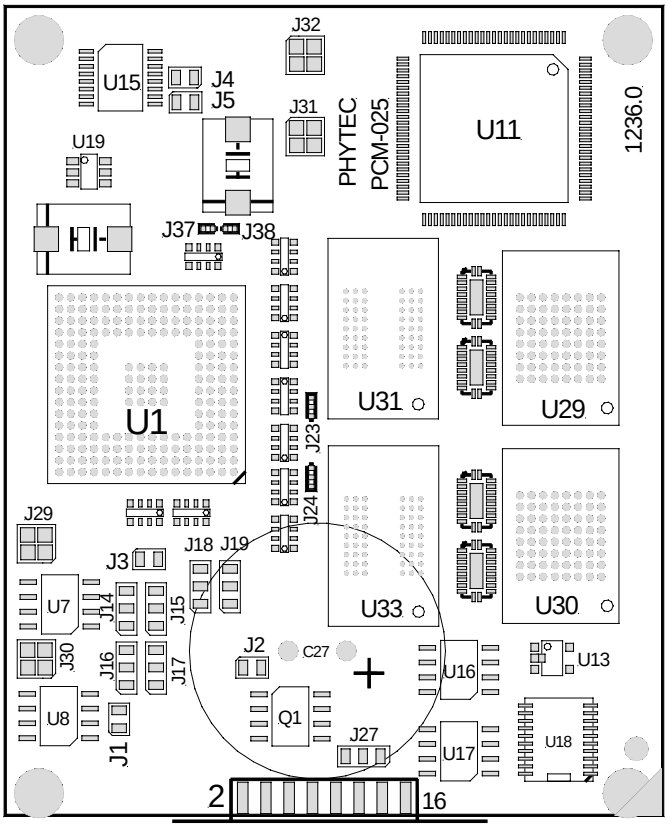


Figure 6: Location of the Jumpers (Controller Side)

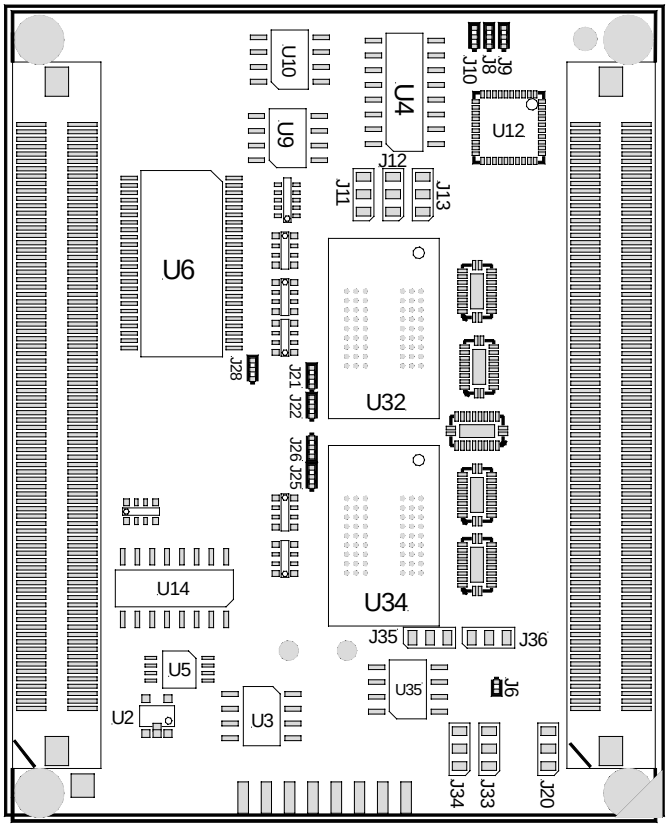


Figure 7: Location of the Jumpers (Connector Side)

The jumpers (J = solder jumper) have the following functions:

Jumper	Default	Function
J1		**reserverd, Do not change !**
open	**X**	
footprint		0R / SMD 0805
J2		**reserverd, Do not change !**
open	**X**	
footprint		0R / SMD 0805
J3		Connects the input of the first asynchronous serial interface on the TC1130 (RXD0) with the RS-232 transceiver at U14.
open		RxD0 can be used as port P2.0, no connection to RS-232 transceiver.
closed	**X**	RxD0 used as RS-232 input and conneted to U14.
footprint		0R / SMD 0805
J4, J5		These Jumpers can be used to connect the reference voltage inputs for the on-chip analog to digital converter (ADC) with the 3,3 V supply voltage of the modul.
closed closed	**X**	The reference voltage input REFA is connected with the 3,3 V supply of the module and GNDA with GND
open open		External reference voltage source can be supplied via pins 80D, 79D of the phyCORE connector.
footprint		0R / SMD 0805
J6		**reserverd, Do not change !**
closed	**X**	
footprint		0R / SMD 0805
J8, J9, J10		Following a power-on-reset, the desired standard boot configuration for the TC1130 configured with these jumpers is latched. The boot configuration selects from which Code memory to fetch instructions and which processing interface to use.
2+3, 2+3, 1+2	**X**	Start out of the external memory at address A0000000H (HWCFG[2:0] = 110)
		Please refer to the TC1130 Manual for alternative settings.
footprint		0R / SMD 0402
J11, J12, J13		An alternative boot configuration is latched via these jumpers if the /BOOT signal is active. The boot configuration selects from which Code memory to fetch instructions and which processing interface to use.
1+2, 1+2, 1+2	**X**	Start out of the internal Boot-ROM. Bootstrap via ASC0
		Please refer to the TC1130 Manual for alternative settings.
footprint		0R / SMD 0805

Jumper	Default	Fuonction
J14, J15		Roote the signals of the first CAN-Node
1+2, 1+2	**X**	Port P0.8 and P0.9 are connected to CAN driver U7
2+3, 2+3		Port P1.0 and P1.1 are connected to CAN driver U7
footprint		0R / SMD 0805
J16, J17		Roote the signals of the second CAN-Node
1+2, 1+2	**X**	Port P0.10 and P0.11 are connected to CAN driver U8
2+3, 2+3		Port P1.2 and P1.3 are connected to CAN driver U8
footprint		0R / SMD 0805
J18, J19		Roote the signals of the second ASC-Interface
1+2, 1+2	**X**	Port P2.8 und P2.9 are connected to the RS232 driver U14
2+3, 2+3		Port P0.0 und P0.1 are connected to the RS232 driver U14
footprint		0R / SMD 0805
J20		Clokout function of the RTC at U18
1+2	**X**	RTC-Clockout disabled
2+3		RTC-Clockout enabled
footprint		0R / SMD 0805
J21, J22, J23		SDRAM configuration Bank A **reserverd, Do not change !**
footprint		0R / SMD 0402
J24, J25, J26		SDRAM configuration Bank B **reserverd, Do not change !**
footprint		0R / SMD 0402
J21, J22, J23		SDRAM configuration Bank A **reserverd, Do not change !**
footprint		0R / SMD 0402

Jumper	Default	Function
J27		Rooting of OCDS1-Signal /BRKOUT (X2)
1+2	**X**	/BRKOUT connected to port P4.7
2+3		/BRKOUT connected to port P0.5
footprint		0R / SMD 0805
J28		**reserverd, Do not change !**
1+2	**X**	
footprint		0R / SMD 0402
J29, J30, J31, J32		These jumpers connect the TTL_CAN signals with the phyCORE connector pins, for connection to external CAN transceivers, or if CAN outputs are used as standard port pins. U7 => CAN Node 0; U8 => CAN Node 1 U9 => CAN Node 2; U10 => CAN Node 3
open	**X**	The on-board CAN transceivers U7, U8, U9, U10 are used.
closed		On-board CAN transceivers not populated.
footprint		0R / SMD 0805
J33, J34		J33 and J34 configure the I^2C bus slave address (A2 und A1) of the serial memory at U17. The slave ID for I^2C memory chips is encode in the high-nibble of the address and set to 0xA. The low-nibble is created by A2, A1, A0 and the R/W bit. A0 is connected to GND. Please note that the RTC at U18 and the themperature sensor at U35 are also connected to the I^2C bus. The RTC address is preconfigured in the chip and set to 0xA2/ 0xA3.
1+2, 2+3		A2 = 0, A1 = 0, A0 = 0 (0xA0 / 0xA1)
1+2, 1+2		A2 = 1, A1 = 0, A0 = 0 (0xA8 / 0xA9)
2+3, 2+3		A2 = 0, A1 = 1, A0 = 0 (0xA4 / 0xA5)
2+3, 1+2	**X**	A2 = 1, A1 = 1, A0 = 0 (0xAC / 0xAD) I^2C slave address 0xAC for write operations and 0xAE for read access.
footprint		0R / SMD 0805

Jumper	Default	Function
J35, J36		J34 and J36 configure the I^2C bus slave address (A2 und A1) of the themprature sensor U35. (refer to chapter 10)
1+2, 2+3		A2 = 0, A1 = 0, A0 = 0 (0xA0 / 0xA1)
1+2, 1+2		A2 = 1, A1 = 0, A0 = 0 (0xA8 / 0xA9)
2+3, 2+3	**X**	A2 = 0, A1 = 1, A0 = 0 (0xA4 / 0xA5)
2+3, 1+2		A2 = 1, A1 = 1, A0 = 0 (0xAC / 0xAD) I^2C slave address 0xAC for write operations and 0xAD for read access.
footprint		0R / SMD 0805
J37, J38		**reserverd, Do not change !** Preset depending on the TC11xx derivat populated
footprint		0R / SMD 0402

Table 2: Jumper Settings

4 Power System and Reset Behavior

Operation of the phyCORE-TC1130 requires only one supply voltage.

Supply voltage: +3.3 V

Circuitry on the module ensures that the power-on sequence as specified in the controller datasheet is met. This means that the 1,5 V core supply is turned on first, followed by the 3,3 V gpio supply.

Once all voltages have reached their target level the voltage supervisory circuit keeps the /PORESET reset signal at low level (low is the active level) for additional 200 ms. Then the /PORESET signal switches to high level (inactive) and the controller's boot sequenz starts.

5 Power-On-Reset Characteristics

When the TC1130 is reset, it needs to know the type of configuration required to start after the reset sequence is finished. The internal state is usually cleared through a reset. This is especially true in the case of a power-up reset. Thus, boot configuration information needs to be applied by the external world through input pins.

Boot configuration information is required for:
• the start location of the code execution
• activation of special modes and conditions

For the start of code execution and activation of special mode, the TC1130 implements two basic booting schemes:
a hardware booting scheme that is invoked through external pins and a software booting scheme in which software can determine the boot options, overriding the externally applied options.

The hardware configuration pins HWCFG[2:0] together with the BRKIN pin, and the TESTMODE pin choose the boot mode and boot location
(*see System Unit User's Manual for the TC1130, section "Booting Scheme"*).

Start Address following Power-On-Reset

Selection between two pre-configured start addressses is possible with the help of the /BOOT signal:

/BOOT = 1 (inactive)

Jumper (default)	**HWCFG [2..0]**	**Boot Source**	**PC Start Address**
JP8 = 2 + 3 JP9 = 1 + 2 JP10 = 2 + 3	011	external memory (non cached)	A000 0000H

/BOOT = 0 (active)

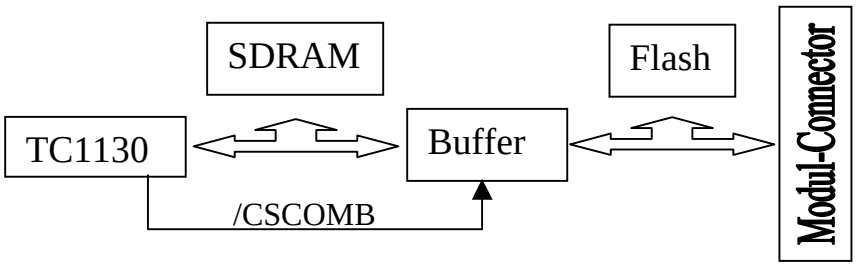
Jumper	HWCFG[2..0]	Boot Source	PC Start Address
JP13 = 1+2 JP12 = 1+2 JP11 = 1+2	000b (default)	ASC0 Bootstrap Loader	D400 0000H
JP13 = 2+3 JP12 = 1+2 JP11 = 1+2	001b	CAN Bootstrap Loader	D400 0000H
JP13 = 1+2 JP12 = 2+3 JP11 = 1+2	010b	SSC Bootstrap Loader	D400 0000H
JP13 = open JP12 = open JP11 = open	External modul pins 61D, 61C, 60D	*see System Unit User's Manual for the TC1130, section "Reset and Boot Operation"*	

If "System Start beginning at address A000 0000h" was chosen, then the controller will perform a "blind-read" from address 0x000004 of the memory device attached to /CS0, in order to read the "EBU boot configuration word" (32Bit) (*see section 14.6.3 of the TC1130 Systems Units Manual*). This first read access occurs with the fixed standard values, which support the reading of as many different memory devices as possible. The " EBU boot configuration word " that was read must have valid values for the read access to the memory connected to /CS0, so that the subsequent accesses occur with the correct timing. The values relevant for the timing are subsequently copied to the register BUSCON0. From this point on there is a valid configuration for read accesses to the external Flash memory, and the program execution can begin at address A0000000h.

The valid boot memory configuration word for the phyCORE-TC1130 is 0xTBD

6 System Memory

The data/address bus of the phyCORE-TC1130 is divided into a fast and a slow range. The two ranges are separated by 74LVCH245ABQ driver devices. The drivers are activated by the /CSCOMB signal. The /CSCOMB signal is generated by the CPU and represents a logical AND connection for the Chip Select signals configured for this purpose. The fast portion of the data/address bus does not extend to external connectors. It is connected exclusively to the SDRAM chips at bank A and B. The slow portion of the data/address bus is connected to the on-board Flash and extends to the module's connectors. If additional memory devices are connected externally, it is important to make sure that the /CSCOMB signal is configured to contain all /CSCOMB signals required to control the slow portion of the memory connected to the data/address bus. *(See System Unit User's Manual for the TC1130).*



In principle, two different memory models are available. The first memory model is the one that is active after a reset. The run time memory model, in contrast, is configured via software by the application.

6.1 Memory Model following Reset

The internal Chip Select logic provided by the TC1130 controller is used exclusively on the phyCORE-TC1130. Hence the memory model as described in the TC1130 User's Manual is valid after reset.

6.2 Runtime Memory Model

The runtime memory model is configured via software using the internal registers of the TC1130. There is a register set containing a BUSCON, BUSAP and ADDSEL register for each of the controllers Chip Select signals. The values in the Bus Configuration Registers (EBU_BUSCON0-3 and EBU_BUSAP0-3) inform the processor of how it should access the connected memory devices (wait states, bus width, etc.). The Address Selection Registers (EBU_ADDSEL0-3) define the address range in which the corresponding Chip Select signal is active. The following list shows the settings for the Chip Select signal assignment.

/CS0	on-board burst-mode Flash memory
/CS1	on-board SDRAM bank A
/CS2	free (or SDRAM bank B)
/CS3	free
/CSCOMB	enable signal for the on-board Bus-Buffer devices

The runtime memory model is application-dependent. The following table (*Table 3*) shows an example of how such a runtime model can be configured.

Address Range	Capacity	Periphery	TC1130 Register
0 x A000 0000 0 x		on-board Flash (/CS0)	EBU_BUSCON0= TBD EBU_BUSAP0= TBD EBU_ADDSEL0= TBD
0 x B000 0000 0 x		on-board SDRAM (/CS1)	EBU_BUSCON1= TBD EBU_BUSAP1= TBD EBU_ADDSEL1= TBD
0 x B010 0000 0 x		on-board SDRAM /CS2 or freely available	EBU_BUSCON2= TBD EBU_BUSAP2= TBD EBU_ADDSEL2= TBD
0 x B020 0000 0 x		freely available	EBU_BUSCON3= TBD EBU_BUSAP3= TBD EBU_ADDSEL3= TBD

Table 3: Runtime Memory Map

/CSCOMB in Register EBU_CON (14-130) und SCU_CON (4-12), hier noch den einzustellenden Wert hinschreiben.

The register values for /CS2 depend on the connected peripheral device. Numbers shown an "X" define the bus interface properties, such as bus width, bus type, wait states etc.

Note:
Table ??? in the TC1130 System Units Manual shows possible values for the address ranges. You can find the values in the column "No. of Address Bits compared..." as hexadecimal values. These values can be put directly into bits 4-7 of the corresponding EBU_ADDSEL register.

6.3 Flash Memory

Use of Flash as non-volatile memory on the phyCORE-TC1130 provides an easily reprogrammable means of code storage.

The Flash memory operates in 16-bit mode and has 32-bit organization on the module. The phyCORE-TC1130 offers the option of populating up to 64 MByte Flash at U29 and U30. /CS0 is connected to the Flash memory bank. With this configuration this memory bank is active following power-on reset.

6.4 Burst-Mode Flash

In order to process code quickly, the TC1130 is equipped with an internal instruction cache and offers the possibility of addressing burst-mode Flash. Intel Burst-mode Flash type RC28F256K3 is optionally implemented on the phyCORE-TC1130. This Flash has a initial access time of 120 ns and a burst-mode access time of 13 ns. No external programming voltage is required.

The concept of burst-mode Flash is to shorten the access time to the Flash contents by reducing access cycles. This means that the Flash auto-increments the address independently, whereby address setup times are eliminated. Since in burst-mode entire code blocks with a maximum size of 16 words are read, this method is most effective for coherent code areas.

7 PLD ispMAC 4000V (U11)

The phyCORE-TC1130 also offers as the option of populating a Lattice ispMACH4000V series PLD at U11. Various PLD options are available: 4064V, 4128V and 4256V. These devices differ only in the number of macro cells they contain. The PLD circuitry is shown in Figure ???, whereby an “x” in front of the signal name indicates that the signal in question is routed over the bus buffer and therefore belongs to the slow portion of the data/address bus. If you want to address the PLD over the data/address bus, you have to make sure that the Chip Select signal /CSCOMB is configured so that it contains /CS0 as well as the /CSx signal used for access to the PLD (*refer to section 6, "System Memory"*). The EGPIOx signals are connected to the module connectors and can be used as desired (*refer to section 2, "Pin Description"*). All PLD pins are 5V tolerant.

8 Serial Interfaces

8.1 RS-232 Interface (U18)

One dual-channel RS-232 transceiver is located on the phyCORE-TC1130 at U18. This device converts the signal levels for the RXD0_TTL and TXD0_TTL lines, as well as those of the second serial interface, RXD1_TTL and TXD1_TTL from TTL level to RS-232 level. The RS-232 interface enables connection of the module to a COM port on a host-PC. In this instance the RxD0 line of the transceiver is connected to the TxD line of the COM port; while the TxD0 line is connected to the RxD line of the COM port. The Ground potential of the phyCORE-TC1130 circuitry needs to be connected to the applicable Ground pin on the COM port as well.

The microcontroller's on-chip UART does not support handshake signal communication. However, depending on user needs, handshake communication can be software emulated using port pins on the microcontroller. Use of an RS-232 signal level in support of hand-shake communication requires use of an external RS-232 transceiver not located on the module.

Furthermore there is the possibility of using the TTL signals of al three UART channels externally. These are available on the phyCORE-connector at X1D12, X1D11 (RXD2_TTL, TXD2_TTL), X1C19, X1C20 (RXD1_TTL, TXD1_TTL) and X1D16, X1D17 (RXD0_TTL, TXD0_TTL). This becomes necessary if galvanic isolation of the interface signals is required.

The TTL transceiver outputs of the on-board RS-232 device can be decoupled from the receive signals RXD0_TTL and RXD1_TTL via solder jumpers J3 and J19. This is necessary so that no external transceivers drive signals against the on-board transceiver. The transmit signals TXD0_TTL / TXD1_TTL, in contrast, can be connected parallel to the transceiver inputs, without causing a collision.

The signals of the second UART are routable CPU internal. This means, that you could choose via configuration register which port Pins are used. Jumper J18 and J19 must be set according to your configuration in order to connect the right pins to the RS-232 tranciever.

J18,J19 = 1+2 => P2.8 (RxD1_A) , P2.9 (TxD1_A)
J18,J19 = 2+3 => P0.0 (RxD1_B) , P0.1 (TxD1_B)

8.2 CAN Interface

The phyCORE-TC1130 is designed to house four CAN transceivers at U7, U8, U9 and U10 (SN65HVD23x). The CAN bus transceiver devices support signal conversion of the CAN transmit (CANTx) and receive (CANRx) lines. The CAN transceiver supports up to 120 nodes on a single CAN bus. Data transmission occurs with differential signals between CANH and CANL. A Ground connection between nodes on a CAN bus is not required, yet is recommended to better protect the network from electromagnetic interference (EMI). In order to ensure proper message transmission via the CAN bus, a 120 Ohm termination resistor must be connected to each end of the CAN bus.

Furthermore, it is required that the CANH and CANL input/output voltages do not exceed the limiting values specified for the corresponding CAN transceiver (for the SN65HVD23x -4 VDC / +16 VDC). If the CAN bus system exceeds these limiting values optical isolation of the CAN signals is required.

For larger CAN bus systems, an external opto-coupler should be implemented to galvanically separate the CAN transceiver and the phyCORE-TC1130. This requires purchasing a module without the on-board CAN transceivers installed. Instead, the TxDCANx/RxDCANx signals are routed to the phyCORE-connector with their TTL level. This requires Jumpers closed (*refer to section 3 for details*). For connection of the CANTx and CANRx lines to an external transceiver we recommend using a Hewlett Packard HCPL06xx or a Toshiba TLP113 HCPL06xx fast opto-coupler. Parameters for configuring a proper CAN bus system can be found in the DS102 norms from the CiA[1] (CAN in Automation) User and Manufacturer's Interest Group.

1: CiA: CAN in Automation. Founded in March 1992, CiA provides technical, product and marketing information with the aim of fostering Controller Area Network's image and providing a path for future developments of the CAN protocol.

8.3 On-Chip Debug Support

The TC1130 offers access to its internal OCDS (OCDS = On-Chip Debug Support) module via an expanded JTAG interface. The JTAG interface enables external access to the system without requiring that some sort of service software (i.e. monitor program) run on the target. Standard cross development systems/debug interfaces, such as the GNU TriCore Development Suite from Hightec offer the possibility of setting breakpoints as well as access to the controller's internal registers via the JTAG interface.

The OCDS1/JTAG interface on the TC1130 extends to the phyCORE-connector and a 16-pin connector at X2 located on the edge of the phyCORE module. An external converter (Wiggler, etc.) can be connected at X2, which allows for connectivity of the TC1130 to a host PC.

The phyCORE-TriCORE Develoment Board (article number PCM-993) integrates such a converter, thus allowing direct connectivity with a development computer .

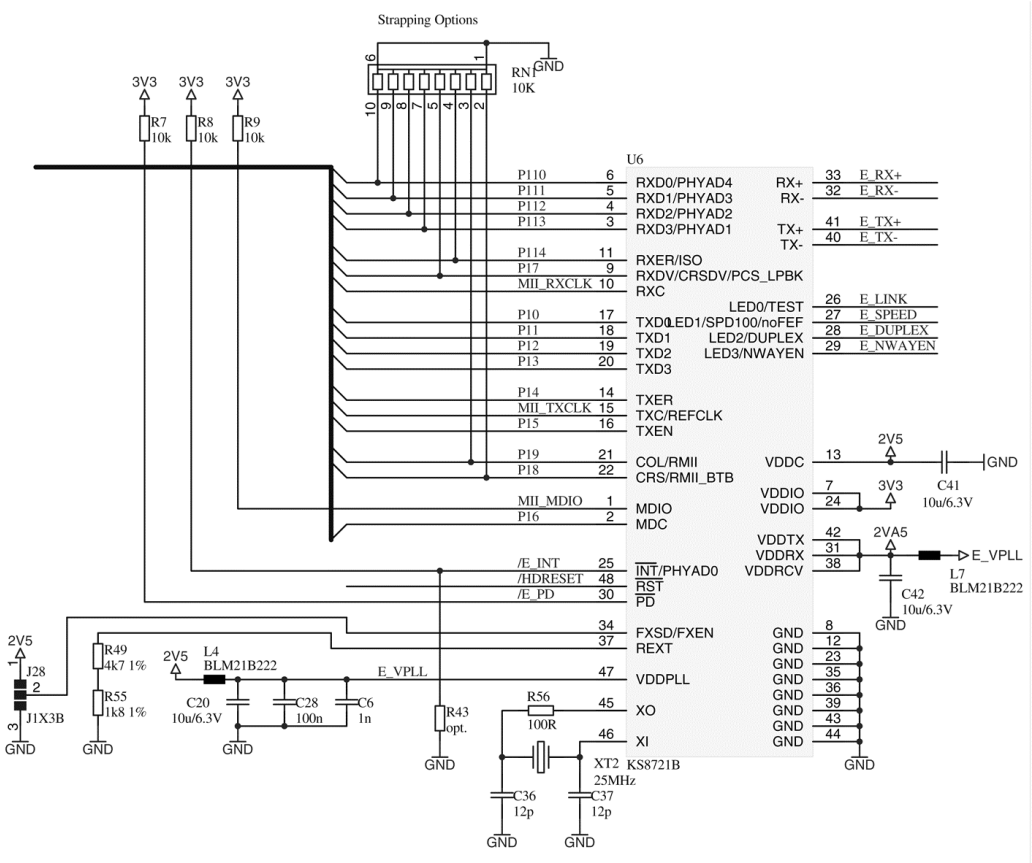
Signal	phyCORE-connector	X2	Description
TMS	42D	1	JTAG module state machine control input
3V3	1C	2	Supply voltage for external wiggler
TDO	41D	3	JTAG module serial data output
GND	44D	4	Ground
/TRCLK	38C	5	Trace Clock for OCDS_2 lines
GND	37C	6	Ground
TDI	40D	7	JTAG module serial data input
/PORESET	11C	8	Power-on reset input
/TRST	41C	9	JTAG module reset/enable input
/BRKOUT	40C / 35B (ref. J27)	10	OCDS break output
TCK	43D	11	JTAG module clock input
GND	39D	12	Ground
/BRKIN	39C	13	OCDS break output
nc		14	not connected
nc		15	not connected
nc		16	not connected

Table 4: OCDS1 Connector X2 Pin Assignment

Note:
Special care must be take when implementing your own external converter in order to ensure the applicable 3.3 VDC supply voltage is applied at pin 2 of connector X2.

9 Ethernet Controller (PHY U6)

The TC1130 offers an integrated fast Ethernet controller with 10/100 MBit MII-based physical devices support. The MII-Interface is connected to the on-board 100BASE-TX/10BASE-T Ethernet PHY KS8721B from Micrel (U6). Since the PHY offers a “Strapping Options” feature where it latches the state of several Pins into its internal registers after reset, the following picture shows the pullup/pulldown resistors connected to the PHY.



Please refer to the datasheets of the TC1130 and Ethernet-PHY for informations, how to initialize and program the Ethernet-interface.

It is possible to connect another PHY device externally or, if the on-board PHY is not populated, to use the MII-interface as general purpose I/O port (Port 1).

9.1 MAC Address

In a computer network such as a "local area network" (LAN), the MAC (Media Access Control) address is a ***unique*** computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyCORE-TC1130 is located on the bar code sticker attached to the module. This number is a 12-position HEX value. The MAC address has already been programmed into the serial I²C-EEPROM and should be used by your application.

The location of the MAC address in the EEPROM is from 0x00 to 0x0C. Where the most significant byte is address 0x00 and the least significant byte is at 0x0C.

10 IIC-BUS

The TC1130 on-chip IIC interface supports a certain protocol to allow devices to communicate directly with each other via two wires. One line is responsible for clock transfer and synchronization (SCL), the other is responsible for the data transfer (SDA). The on-chip IIC Bus module connects the platform buses to other external controllers and/or peripherals via the two-line serial IIC interface. The IIC Bus module provides communication at data rates of up to 400 kbit/s and features 7-bit addressing as well as 10-bit addressing. This module is fully compatible to the IIC (I²C) bus protocol.

Depending on the module's configuration there are multiple I²C devices connected to the CPU pins P2.12 (SDA0) and P2.13 (SCL0) on the phyCORE-TC1130. To avoid collisions when addressing the devices, each device is to be assigned a unique address. The following table provides an overview. If you want to connect additional I²C devices externally to SDA0 and SCL0, it is important to note the aforementioned address assignment and also to make sure that the baud rate used for data transfer is adjusted to the slowest device.

I²C Device	Address (default)
A/D Converter	0x90/0x91
Temperature Sensor	0x94/0x95
D/A Converter	0x98/0x99
EEPROM	0xA4/0xA5
Real Time Clock	0xA2/0xA3

Table 5: I²C Devices and Default Addresses

10.1 Serial Memory, EEPROM/FRAM (U17)

The phyCORE-TC1130 features a non-volatile memory with an I^2C interface. This memory can be used for storage of configuration data or operating parameters, that must not be lost in the event of a power interruption. Depending on the module's configuration, this memory can be in the form of an EEPROM or FRAM. The available capacity ranges from 512 Byte to 32 kByte. The memory is connected to the first IIC-chanel of the TC1130.

Chapter 9.1 provides an overview of compatible components for U17 at the time this manual was printed.

Type	**Capacity**	**I^2C Clock**	**Address Pins**	**Write Cycles**	**Data Retention**	**Component**	**Manuf.**
EEPROM	256/512 Byte	400 kHz	A2, A1, A0	1 000 000	100 years	CAT24WC02/04	Catalyst
	1/ 2 kByte	400 kHz	A2, A1, A0	1 000 000	100 years	CAT24WC08/16	Catalyst
	4/8 kByte	400 kHz	A2, A1, A0	1 000 000	100 years	CAT24WC32/64	Catalyst
	32 kByte	1 MHz	A1, A0	100 000	100 years	CAT24WC256	Catalyst
FRAM	512 Byte	400 kHz	A2, A1	10 Billion	10 years	FM24C04	Ramtron
	8 kByte	1 MHz	A2, A1, A0	10 Billion	10 years	FM24C64	Ramtron

Table 6: Memory Device Options for U17

The following configuration options are available:

I²C Address	**J33 A1**	**J34 A2**
0xA0 / 0xA1	1 + 2	2 + 3
0xA4 / 0xA5 (default)	2 + 3	2 + 3
0xA8 / 0xA9	1 + 2	1 + 2
0xAC / 0xAD	2 + 3	1 + 2

Table 7: I²C Addresses configuration for I²C Memory

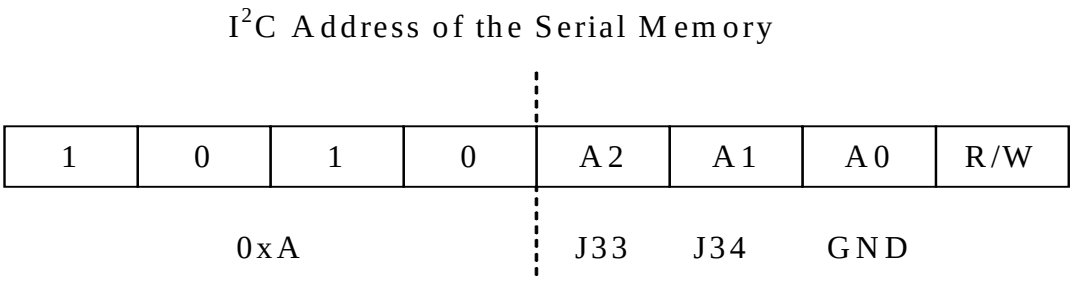


Figure 8: I²C Slave Address of the I²C Memory

Address lines A1 and A2 are not always made available by certain serial memory types. This should be noted when configuring the I²C bus slave address.

10.2 Real-Time Clock RTC-8564 (U18)

For real-time or time-driven applications, the phyCORE-TC1130 is equipped with an RTC-8564 Real-Time Clock at U18. This RTC device provides the following features:

- Serial input/output bus (I^2C), address 0xA2
- Power consumption

  Bus active (400 kHz): < 1 mA

  Bus inactive, CLKOUT inactive: < 1 µA
- Clock function with four year calendar
- Century bit for year 2000-compliance
- Universal timer with alarm and overflow indication
- 24-hour format
- Automatic word address incrementing
- Programmable alarm, timer and interrupt functions

If the phyCORE-TC1130 is supplied with a +3VDC voltage at Pin X1C6C (VBAT_IN), the Real-Time Clock runs independently of the board's power supply.

Programming the Real-Time Clock is done via the first controller integrated I^2C bus chanel (address 0xA2/0xA3).

The Real-Time Clock also provides an interrupt output that extends to the phyCORE connector X1D33D. An interrupt occurs in case of a clock alarm, timer alarm, timer overflow and event counter alarm. An interrupt must be cleared by software. With the interrupt function, the Real-Time Clock can be utilized in various applications. *For more information on the features of the RTC-8564, refer to the corresponding Data Sheet.*

Note:
After connection of the supply voltage, or after a reset, the Real-Time Clock generates **no** interrupt. The RTC must first be initialized (*see RTC Data Sheet for more information*)

10.3 AD-Converter (U15)

The ADS7828 at U15 is a 12-bit data acquisition device that features a serial I²C interface and an 8-channel multiplexer. The Analog-to-Digital (A/D) converter features a sample-and-hold amplifier and internal, asynchronous clock. It is addressed via the fixed I²C address 0x90/0x91. The reference voltage input could either be connected to the +3,3V supply voltage (J4 and J5 closed) or to the phyCORE connector pins REFA / GNDA. Please refer to chapter 2 to see the connections to the phyCORE connector in more detail.

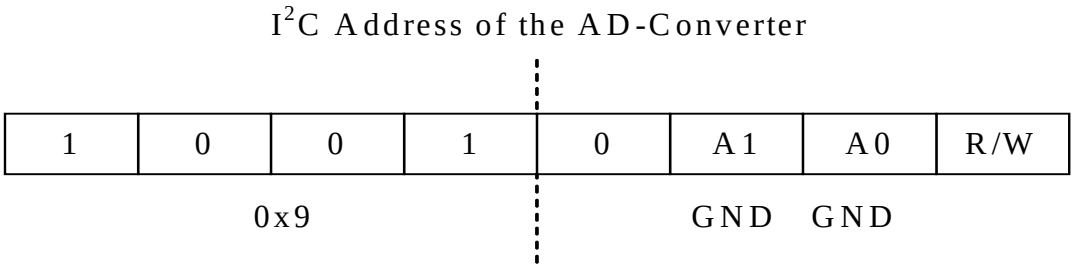


Figure ?: I²C Slave Address of the AD-Converter

10.4 DA-Converter (U19)

The DAC7571 is a single channel, 12-bit buffered voltage output DAC. Its on-chip precision output amplifier allows rail-to-rail output swing to be achieved. The DAC7571 utilizes an I2C compatible two wire serial interface that operates at clock up to 3.4 Mbps. It is addressed via the fixed I²C address 0x98/0x99. The output voltage range of the DAC is set to VDD = +3,3V. The DAC7571 incorporates a power-on-reset circuit that ensures that the DAC output powers up at zero volts and remains there until a valid write to the device takes place. The DAC output is connected to the phyCORE connector X1C75C.

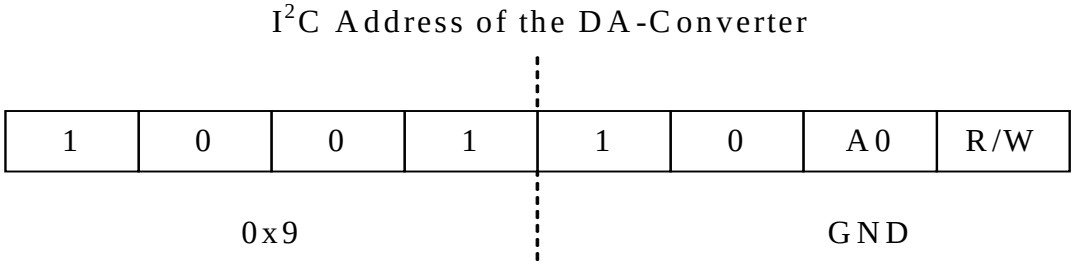


Figure ?: I²C Slave Address of the DA-Converter

10.5 Temperatur Sensor (U35)

Reading the actual temperatur and generating a alarm signal when the temperature exceeds a programmable limit is the feature of the optional populated sensor LM75. The overtemperature open drain output is connected to the phyCORE connector at X1D8D and can externally be wired to any input you desire.

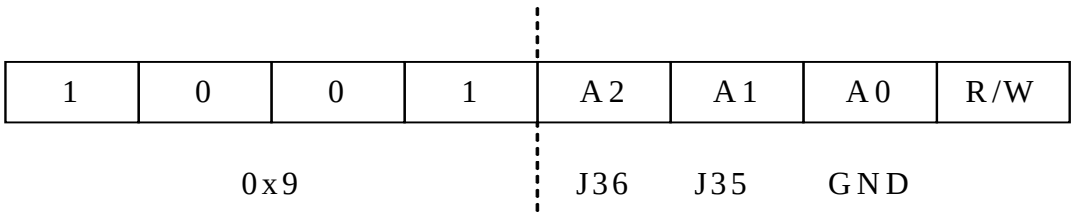


Figure ?: I²C Slave Address of the Serial Memory

The following configuration options are available:

I²C Address	**J345 A1**	**J36 A2**
0x90 / 0x91	1 + 2	2 + 3
0x94 / 0x95 (default)	2 + 3	2 + 3
0x98 / 0x99	1 + 2	1 + 2
0x9C / 0x9D	2 + 3	1 + 2

Table 8: I²C Addresses for Serial Temperature Sensor LM75

11 phyTRACE-TC1130

In einigen zeitkritischen Aplikationen werden für das Debugging bzw. Zeitverhalten-Analyse die Trace-Signale des TC1130 benötigt. Diese Signale stehen über die OCDS2-Schnittstelle zur Verfügung, die wahlweise über den CPU-Port P1 oder P3 herausgeführt werden. Der phyTRACE-TC1130-Adapter wurde entwickelt, um dem Anwender auch in der eigenen Aplikation den Anschluss eines OCDS2 fähigen Debuggers zu erlauben. Der phyTRACE-TC1130 wird zwischen phyCORE und Basisplatine gesteckt und beinhaltet neben Jumpern für das Routing der OCDS2-Signale einen Highspeed Steckverbinder für den Debugger Anschluss. Der Anschluss X3 kann als „combined“ Variante verwendet werden, wobei sowohl die OCDS1-, wie auch die OCDS2-Signale abgegriffen werden. Alternativ wird OCDS1 am phyCORE selbst und OCDS2 am phyTRACE abgegriffen. Der als OCDS2-Interface definierte Prozessorport wird NICHT weiter zur Basisplatine durchgereicht (RNx nicht bestückt).

Jumper	Default	Function
J1		Indicates if this is a OCDS1+OCDS2 combined connector
closed	**X**	Use only phyTRACE X3 for debugging (combined)
open		Use OCDS1 from phyCORE and OCDS2 from phyTRACE X3 for debugging (splitted)
footprint		0R / SMD 0805
J2-J17		Select the TC1130 port for OCDS2 signals
1+2	X	Trace signals via Port 1 (RN1-RN4 not populated)
2+3		Trace signals via Port 3 (RN5-RN8 not populated)
footprint		0R / SMD 0805
J18		Select the source of the /BRKOUT signal
1+2	X	Port pin P4.7
2+3		Port Pin P0.5
footprint		0R / SMD 0805

Please note that the phyTRACE-TC1130 is slightly larger than the standard phyCORE-TC1130 module due to the debugging connector.

Please note that when using the Trace port (OCDS2) port 1/3 of the controllers is no longer available for other functions.

11.1 Components of the phyTRACE

As described previously, the phyTRACE-TC1130 represents a adapter which expands the phyCORE-TC1130 with a OCDS2 connector.

The following components are available for simple debugging:

- Reset button
- one 60-pin SMD-connectors (X3), OCDS level 2

The following figure shows the positions of the components and the size.

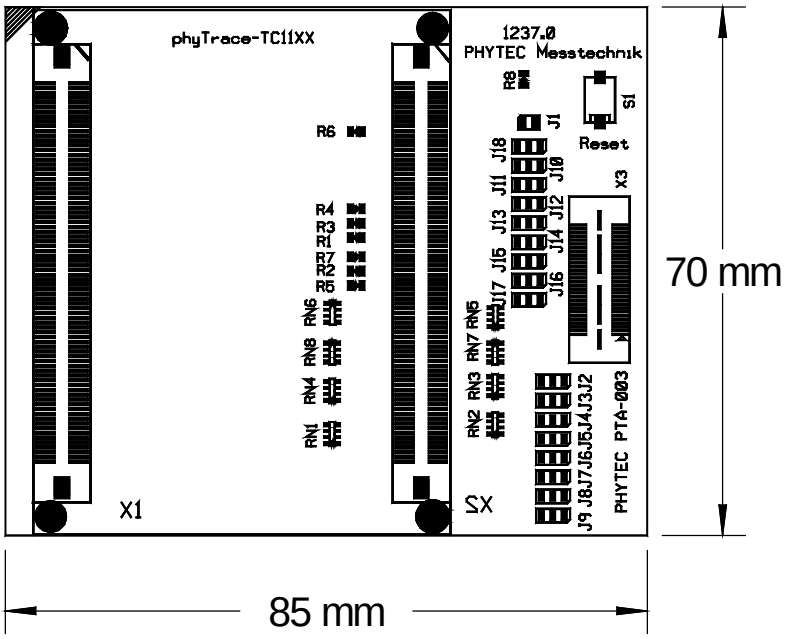


Figure 9: Positions of the Components on the phyTRACE-TC1130

11.2 Connecting an Emulator

11.2.1 OCDS1 debugging

The 2 mm pin header connector at X2 is used for connection of an emulator, which is designed for use with the internal JTAG interface (OCDS level 1) of the TriCore-TC1130 controller. It is then possible to transfer program code to the module and debug this code with the help of standard debug functions such as breakpoints, single step, etc. The signals available at X2 are connected directly from the processor. Only the configuration of jumper in *chapter 3* is required. Pin 1 of the JTAG connector is marked by a black pad on the connector side of the PCB.

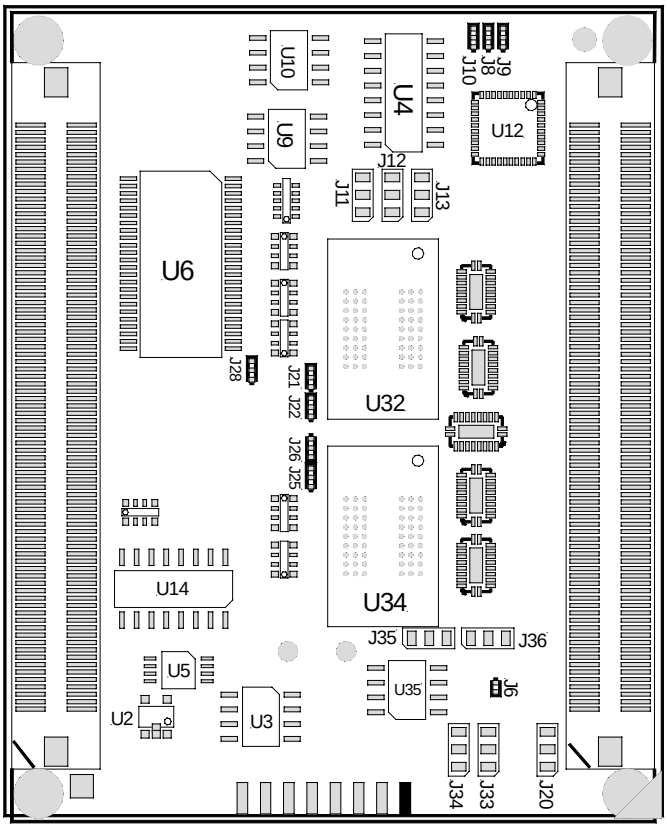


Figure 10: Connecting an Emulator

11.2.2 OCDS2 debugging

For OCDS2 debugging the CPU's trace signals are required in addition to the OCDS1 signals. Using the phyTRACE-TC1130 adapter, both OCDS interfaces can be accessed easily over the 60-pin high-speed connector at X3.

Figure 11 shows the phyTRACE-TC1130 adapter in combination with the phyCORE-TC1130.

(1) = OCDS1 connector
(2) = Combined OCDS1/2 connector
(3) = Molex connector on the phyTRACE

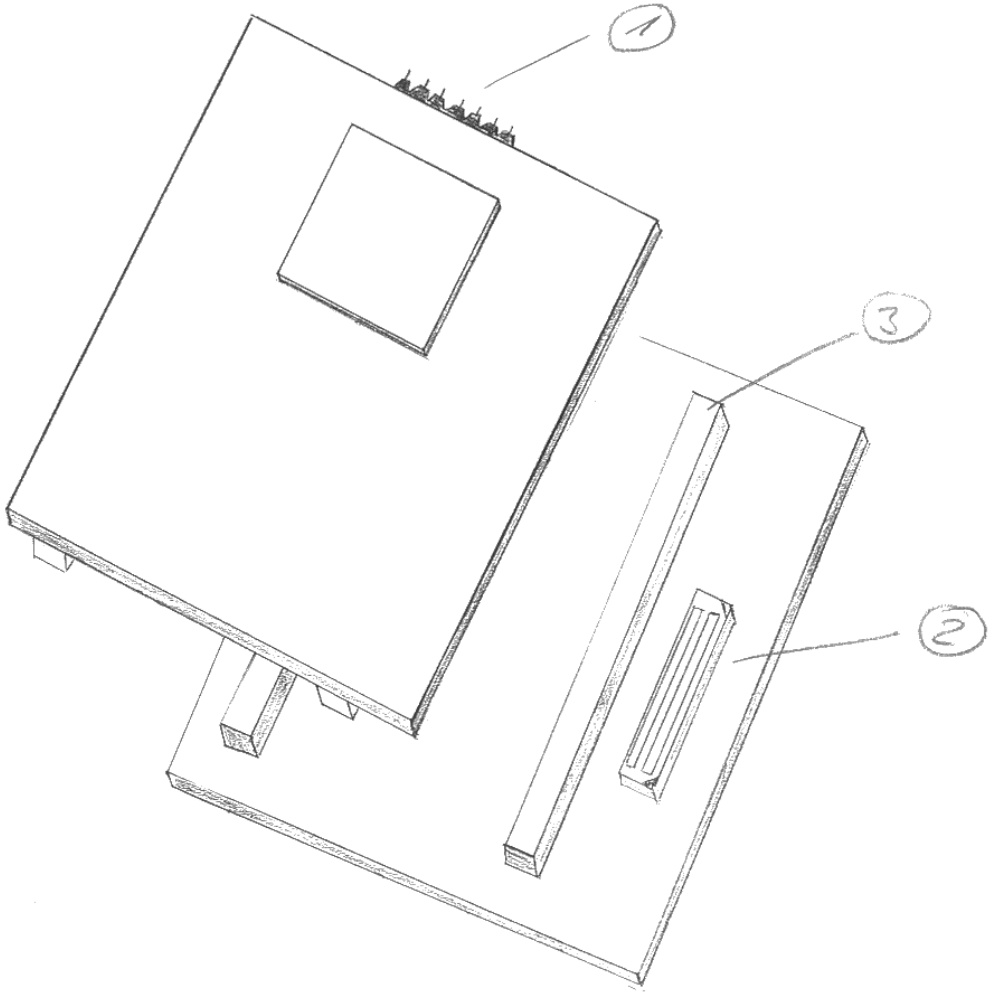


Figure 11: phyTRACE-TC1130 Adapter

If your emulator is not equipped with a trace input, it is usually possible to obtain this trace port as an expansion from your emulator manufacturer.

Please note that when using the Trace port (OCDS2) port 1 or 3 of the controllers is no longer available for other I/O functions.

12 Technical Specifications

The physical dimensions of the phyCORE-TC1130 are represented in *Figure 12*. The module's profile is ca. TBD mm thick, with a maximum component height of TBD mm on the backside of the PCB and approximately TBD mm on the front side. The board itself is approximately TBD mm thick.

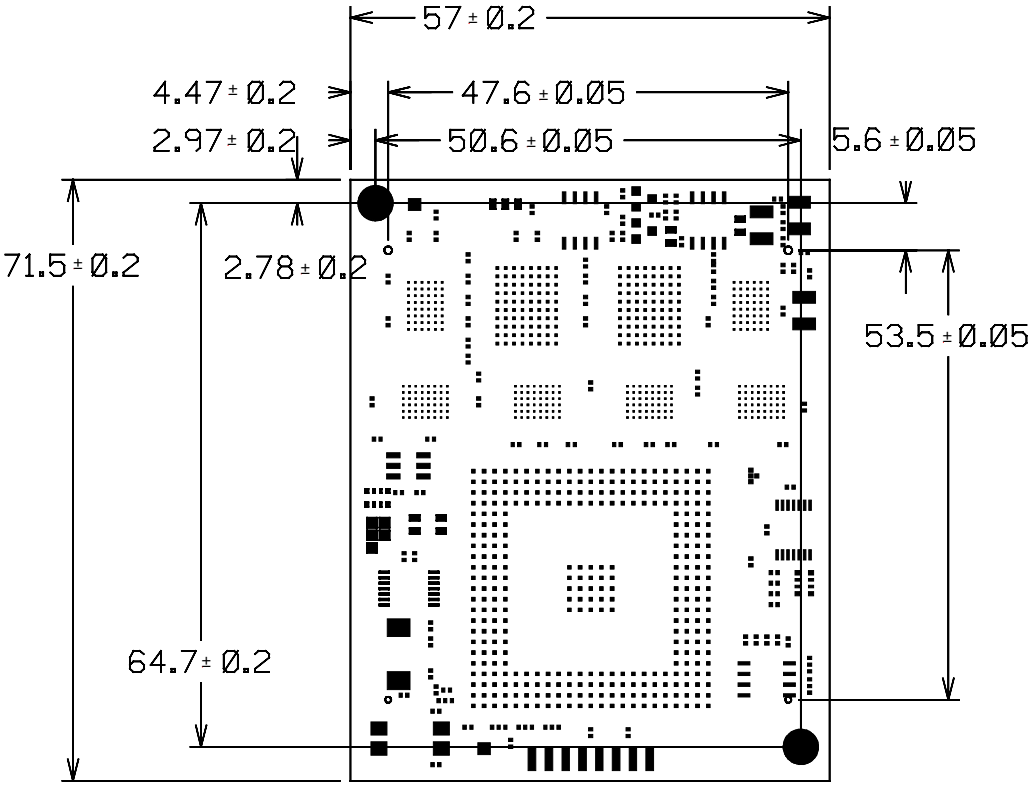


Figure 12: *Physical Dimensions*

Preliminary technical specifications:

• Dimensions:	72 mm x 57 mm
• Weight:	approximately TBD g with all optional components mounted on the circuit board
• Storage temperature:	-40°C to +90°C
• Operating temperature:	standard: 0°C to +90°C
• Humidity:	95 % r.F. not condensed
• Operating voltages:	3.3 V ±10 % SONDZEICHENVBAT 3 V ±5 %
• Power consumption:	Conditions: 150 MHz clock, 128 MByte RAM , 64 MByte Flash, 20°C
3.3 V voltage	typ. TDB mA
Battery current draw Real-Time Clock supply	Conditions: VBAT = 3 V 3.3 V voltage=off, 20°C TBD µA

These specifications describe the standard configuration of the phyCORE-TC1130 as of the printing of this manual.

Connectors on the phyCORE-TC1130:

Manufacturer	Molex
Number of pins per connector row	160 (2 rows of 80 pins each)
Molex type number	52760 (receptacle)

Two different heights are offered for the receptacle sockets that correspond to the connectors populating the underside of the phyCORE-TC1130. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (TBD mm) on the underside of the phyCORE must be subtracted.

- Height 6 mm

Manufacturer	Molex
Number of pins per connector row	160 (2 rows of 80 pins each)
Molex type number	55091 (plug)

- Height 10 mm

Manufacturer	Molex
Number of pins per connector row	160 (2 rows of 80 pins each)
Molex type number	53553 (plug)

Please refer to the coresponding data sheets and mechanical specifications provided by Molex (www.molex.com).

13 Hints for Handling the phyCORE-TC1130

Removal of components is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Integrating the phyCORE-TC1130 in application circuitry

Successful integration in user target circuitry depends on whether the layout for the GND connections matches those of the phyCORE module. It is recommended that the target application circuitry is equipped with one layer dedicated to carry the GND potential. In any case, be sure to connect all GND pins neighboring signals which are used in the application circuitry. For the supply voltage, there must be contact with at least six of the GND pins neighboring the supply voltage pins.

14 Revision History

Date	Version numbers	Changes in this manual
15-April-2005	Manual L-665e_1 PCM-025 PCB# 1236.0-001 PCM-993 PCB# 1182.0-002	Preliminary edition.

Index

Document: phyCORE-TC1130
Document number: L-665e_0, Preliminary, April 2005

How would you improve this manual?

Did you find any mistakes in this manual? page

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