# User's Manual

**for**

**A Sequencing LSI for Stepper Motors**

# PCD4511/4521/4541

NPM: Nippon Pulse Motor Co., Ltd.

A Sequencing LSI for Stepper Motors

# PCD4511/4521/4541


The PCD4511/4521/4541 are excitation control LSIs designed for 2-phase stepper motors.
With just one of these LSIs and a stepper motor driver IC (e.g. NP-7026), you can easily construct a stepper motor control system.
Data and commands entered from a CPU enable this LSI to control the speed and position of a stepper motor. Since the LSI has a pulse signal generation circuit, it can also control a motor driver that relies on the number of pulses supplied.
Users can select the 4511 (single-axis model), 4521 (2 axes model), or 4541 (4 axes model) PCD to drive their motors.

## 1. Functions

1) Continuous operation (constant speed, linear and S-curve acceleration and deceleration).
2) Preset operation (constant speed, linear and S-curve acceleration and deceleration).
3) Zero return operation (constant speed, linear and S-curve acceleration and deceleration).
4) Timer operation
5) Excitation output sequencing for 2-phase stepper motors
   - 2-2 phase / 1-2 phase
   - Unipolar / bipolar
6) Idling pulse output (0 to 7 pulses)
7) Deceleration by specifying a ramping-down point.
8) Change speed while operating.
9) Change to constant speed in the middle of an acceleration or deceleration.
10) Deceleration stop and immediate stop.
11) Output external start and stop signals for other equipment.
12) Input external signals from other equipment ($\pm\overline{SD}$, $\pm\overline{EL}$, $\overline{ORG}$)
13) Output an interrupt signal ($\overline{INT}$).
14) Status monitoring signal for each operation.
15) Available in standard mounting packages
   - PCD4511: 44-pin QFP
   - PCD4521: 64-pin QFP
   - PCD4541: 100-pin QFP

## 2. Software settings

2-1. Address lines

Relationship between address lines (A1, A0) and $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$.

| $\overline{CS}$ | $\overline{RD}$ | $\overline{WR}$ | A1 | A0 | Detail | |
|---|---|---|---|---|---|---|
| L | H | L | L | L | Data bus -> Command buffer | Writing |
| L | H | L | L | H | Data bus -> Register (bits 7 to 0: lower bit) | |
| L | H | L | H | L | Data bus -> Register (bit 15 to 8: Medium bit) | |
| L | H | L | H | H | Data bus -> Register (bit 23 to 16: Upper bit) | |
| L | L | H | L | L | Data bus <- Status 0 | Reading |
| L | L | H | L | H | Data bus <- Internal data (lower) | |
| L | L | H | H | L | Data bus <- Internal data (medium) | |
| L | L | H | H | H | Data bus <- Internal data (upper) | |

Relationship between address lines (A3, A2) and the axes controlled by a PCD4521/4541.

| PCD4521 | | |
|---|---|---|
| A2 setting | A2=0 | A2=1 |
| Selected axis | X axis | Y axis |

| PCD4541 | | | | |
|---|---|---|---|---|
| A2, A3 setting | A3=0, A2=0 | A3=0, A2=1 | A3=1, A2=0 | A3=1, A2=1 |
| Selected axis | X axis | Y axis | Z axis | U axis |

2-2. Command buffer

In order to operate this LSI, data is written into the command buffer and each data register through the 8-bit data bus.

Commands can be classified into four groups, and the upper 2 bits in each command are used to specify the group. Each command is latched until the same group command is written a second time. Each bit in a command represents a specific function. Functions do not have individual commands.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C1 | C0 | | | | | | |

| C1 | C0 | Command group |
|---|---|---|
| 0 | 0 | Start mode |
| 0 | 1 | Control mode |
| 1 | 0 | Select register |
| 1 | 1 | Output mode |

2-3. Bit details for each command

1) Start mode command

| | | |
|---|---|---|
| D7 | 0 | |
| D6 | 0 | |
| D5 | | -> Enable/disable interrupt output while stopping. |
| D4 | | -> Start control |
| D3 | | -> Stop control |
| D2 | | -> Select operating mode: Constant speed or acceleration/deceleration. |
| D1 | | -> Enable/disable external $\overline{\text{STA}}$ control |
| D0 | | -> Select FL or FH speed |

2) Control mode command

| | | |
|---|---|---|
| D7 | 0 | |
| D6 | 1 | |
| D5 | | -> Select linear or S-curve acceleration and deceleration |
| D4 | | -> Control the output of general purpose OTS terminal |
| D3 | | -> Select the feed direction for output pulses |
| D2 | | -> Enable/disable preset operation |
| D1 | | -> Enable/disable $\overline{\text{SD}}$ signal |
| D0 | | -> Enable/disable the $\overline{\text{ORG}}$ signal |

3) Register select command

| | | |
|---|---|---|
| D7 | 1 | |
| D6 | 0 | |
| D5 | | -> Enable/disable external start interrupt signal |
| D4 | | -> Enable/disable ramping-down point interrupt signal |
| D3 | | -> Enable/disable preset counter |
| D2 | | Register selection (R0 to R7) |
| D1 | | |
| D0 | | |

4) Output mode command

| | | |
|---|---|---|
| D7 | 1 | |
| D6 | 1 | |
| D5 | | -> Select between standard and extension monitor modes |
| D4 | | -> Set the sensitivity of the $\overline{\text{ORG}}$, $\overline{\text{EL}}$, and $\overline{\text{STP}}$ signals (noise filters) |
| D3 | | -> Change to a constant speed in the middle of an acceleration or deceleration |
| D2 | | -> Mask the excitation sequencing output |
| D1 | | -> Mask the pulse output |
| D0 | | -> Select the pulse output logic (negative/positive (normal ON/OFF)) |

2-4. Table of registers

| D2 | D1 | D0 | Register | Details | R/W | Bit length | Setting range |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | R0 | Preset counter data | R/W | 24 | 0 to FFFFFF |
| 0 | 0 | 1 | R1 | FL speed | W (R) | 13 | 1 to 1FFF |
| 0 | 1 | 0 | R2 | FH speed | W (R) | 13 | 1 to 1FFF |
| 0 | 1 | 1 | R3 | Rate of accel/decel | W (R) | 10 | 2 to 3FF |
| 1 | 0 | 0 | R4 | Magnification | W (R) | 10 | 2 to 3FF |
| 1 | 0 | 1 | R5 | Ramping-down point | W (R) | 16 | 0 to FFFF |
| 1 | 1 | 0 | R6 | Number of idling pulses | W (R) | 3 | 0 to 7 |
| 1 | 1 | 1 | R7 | Environmental data (PCD4541 only) | W (R) | 1 | 0 to (1) |

* D2, D1, and D0: Bits used to select the register

(R): Can be read by enabling the extension monitor

## 3. Examples of operation settings

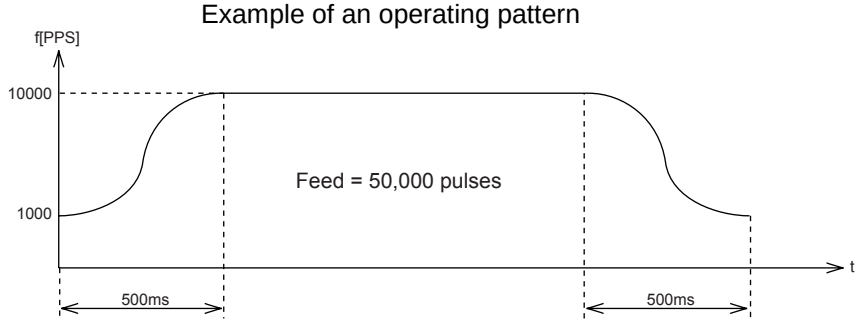
3-1. Command setting example

This LSI is operated by specifying one of 4 types of commands and by entering values for registers R0 to R7.

1) Specify the control mode command details ($64_{HEX}$) --- Preset operation, S-curve rate of accel/decel, + direction, disable SD/ORG.
2) Specify the register select command details --- See the setting details in section 3-2 above.
3) Specify the output mode command details ($D1_{HEX}$) --- Excitation sequencing output, pulse output positive logic, enable filter.
4) Specify the start command details ($15_{HEX}$) --- Start and accelerate at FL speed, and operate at FH speed.
   By specifying the start command, the LSI will start operation.

3-2. Example of setting a register

Example of an operating pattern




Initial speed (FL) = 1,000 PPS, operating speed (FH) = 10,000 PPS, accel/decel time = 500 mS, reference clock = 4.9152 MHz

1) Set the number of pulses as a preset amount (R0): Stop after outputting 50,000 pulses

R0 = 50,000

To write data into a register, first specify the register (R0) using the register select command ($80_{HEX}$). Then, write the data as three bytes in the following order: upper bits, middle bits, and lower bits.

2) Set the multiplication of the output frequency (R4): Select 2x for the LSI outputs (10,000 PPS in this example).

$$\text{R4 set value} = \frac{\text{Reference clock frequency [Hz]}}{\text{Magnification x 8192}} = \frac{4915200}{2 \times 8192} = 300$$

R4 = 300

3) Set the FL frequency (R1): Since the initial speed is set to 1,000 PPS in the 2x mode, R1 = 500.

4) Set the FH frequency (R2): Since the initial speed is set to 10,000 PPS in the 2x mode, R2 = 5,000.

5) Set the accel/decel time constant (R3): Since S-curve accel/decel is selected with an accel/decel time of 500 mS.

$$\text{R3 set value} = \frac{\text{(Accel/decel time [Sec.]) x (Reference clock frequency [Hz])}}{\text{((R2 set value) } - \text{ (R1 set value)) x 2}}$$

[S-curve rate of accel/decel]

$$\text{R3} = \frac{0.5 \times 4915200}{(5000 - 500) \times 2} = 273.07 \quad 273$$

R3 =273

6) Set the number of pulses for the ramping-down point (R5):
By setting the ramping-down point register (R5) while in the preset operation mode, you can specify the number of pulses remaining at which to start deceleration.

$$\text{R5 set value [pulses]} = \frac{((\text{R2 set value})^2 - (\text{R1 set value})^2) \times (\text{R3 set value})}{(\text{R4 set value}) \times 8192}$$

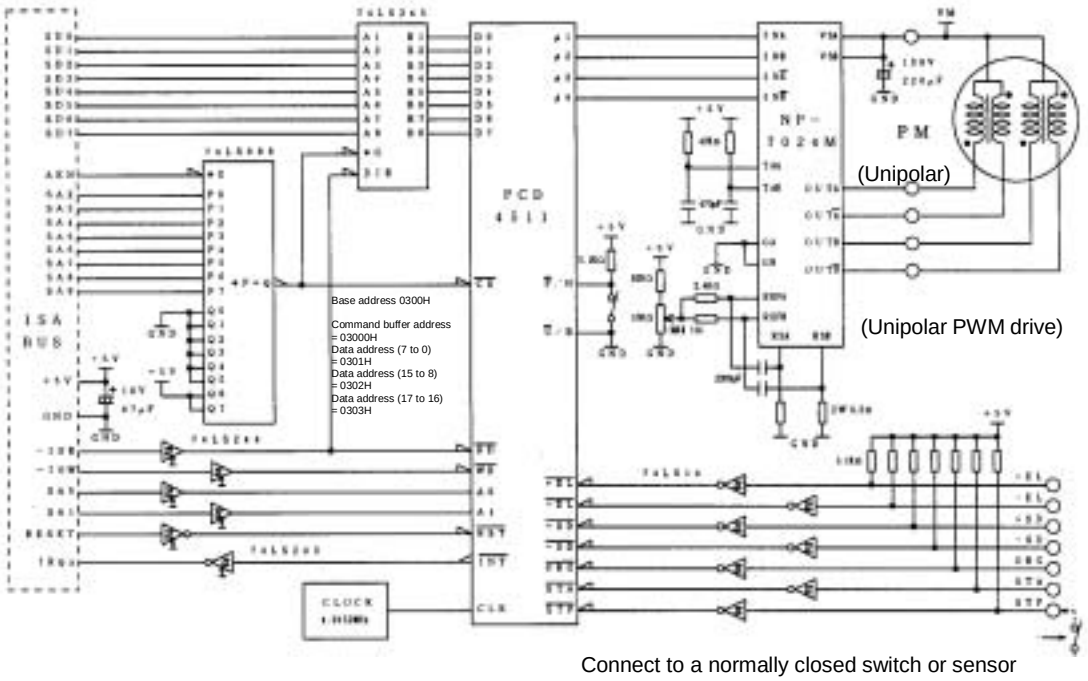
[S-curve accel/decel]

$$\text{R5} = \frac{(5000^2 - 500^2) \times 273}{300 \times 8192} = 2749.33 \quad 2750$$

R5=2750

## 4. Connection example

Connection example using an ISA_BUS -> PCD4511 -> NP-7024(6) M




Connect to a normally closed switch or sensor

# User's Manual

**for**

**A Sequencing LSI for Stepper Motors**

# PCD4511/4521/4541

## Preface

Thank you for considering the use of our "PCD45X1 series."
Before using one of the PCD45X1 LSIs, read this manual carefully and become familiar with the product.
The "Handling precautions" for mounting these ICs are in the last part of this manual.

## Precautions

1) Transmission or copying of all or part of this manual is prohibited without prior written approval.
2) The specifications provided in this manual may be changed without prior notice to improve our product's performance or quality.
3) This manual was created with the utmost care. However, if you have any questions, find problems or believe important material is missing from the manual, please let us know.
4) NMP is not liable for any results of using this product, even if a problem or error has been reported.

**Description of the expressions and symbols used in this manual.**

1. "x," "y," "z," and "u" on the terminal assignment drawings at the end of this manual or in parenthesis ( ) in the terminal tables refer to the X axis, Y axis, Z axis, and U axis, respectively.
2. Terminals with a line above the terminal name, like $\overline{\text{RST}}$, mean that the terminal uses negative logic (normally ON).

## Table of contents

## 1. Outline and features

[Outline]
The PCD4511/4521/4541 are excitation control LSIs designed for 2-phase stepper motors.
With just one of these LSIs and a stepper motor driver IC (e.g. NP-7026), you can easily construct a stepper motor control system.
Data and commands entered from a CPU enable this LSI to control the speed and position of a stepper motor. Since the LSI has a pulse signal generation circuit, it can also control a motor driver that relies on the number of pulses supplied.

[Features]
- Excitation sequencing output for a 2-phase stepper motor.
- Linear and S-curve acceleration/deceleration control.
- CW and CCW pulse output.
- External start and stop control
- Zero return operation
- Outputs idling pulses
- 400 KPPS maximum output frequency
- Available in single axis (PCD4511), 2-axis (PCD4521), and 4-axis (PCD4541) models.

## 2. Specifications

| Item | Description |
|---|---|
| Power source | +5V ±10% |
| Reference clock | 4.9152 MHz standard (10 MHz max.) |
| Range of settable positioning pulses | 0 to 16,777,215 pulses |
| Range of settable speeds | 1 to 8,191 steps |
| Recommended speed magnification range* | 1x to 2x (Using a standard 4.9152 MHz clock)<br>When 1x: will deliver 1 to 8,191 PPS<br>When 2x: will deliver 2 to 16,382 PPS |
| Number of registers for setting the speed | Two (FL and FH) |
| Ramping-down point setting range | 0 to 65,535 pulses |
| Accel/decel rate setting range | 2 to 1,023 |
| Typical operations | - Continuous operation<br>- Preset operation (positioning)<br>- Zero return operation<br>- Timer operation |
| Typical functions | - Linear and S-curve acceleration/deceleration<br>- Immediate stop and decelerating stop<br>- Speed change<br>- Settable ramping-down point<br>- External start and stop function<br>- Idling pulse output function<br>- Excitation sequencing output for 2-phase stepper motors<br>[Phase signals for unipolar and bipolar motors]<br>[2-2 phase excitation, 1-2 phase excitation phase signals] |
| Ambient operating temperature | 0 to +85℃ |
| Storage temperature | -40 to +125℃ |
| Package | PCD4511: 44-pin QFP<br>PCD4521: 64-pin QFP<br>PCD4541: 100-pin QFP |
| Chip design | C-MOS |

* This value is true when a stepper motor is used within the 24-bit preset counter range.

## 3. Table of registers

| Register No. | Details | Bit length | R/W | Setting range ( ) = HEX |
|---|---|---|---|---|
| R0 | Set the preset counter value and check the remaining pulses | 24 | R/W | 0 to 16, 777, 215 (FFFFFF) |
| R1 | Set the FL speed | 13 | W(R) | 1 to 8, 191 (1FFF) |
| R2 | Set the FH speed | 13 | W(R) | 1 to 8, 191 (1FFF) |
| R3 | Set the acceleration/deceleration rate | 10 | W(R) | 2 to 1, 023 (3FF) |
| R4 | Set the magnification rate | 10 | W(R) | 2 to 1, 023 (3FF) |
| R5 | Set the ramping-down point | 16 | W(R) | 0 to 65, 535 (FFFF) |
| R6 | Set the number of idling pulses | 3 | W(R) | 0 to 7 |
| R7 | Enter environmental data (PCD4541 only) See Note | 1 | W(R) | 0 to (1) |

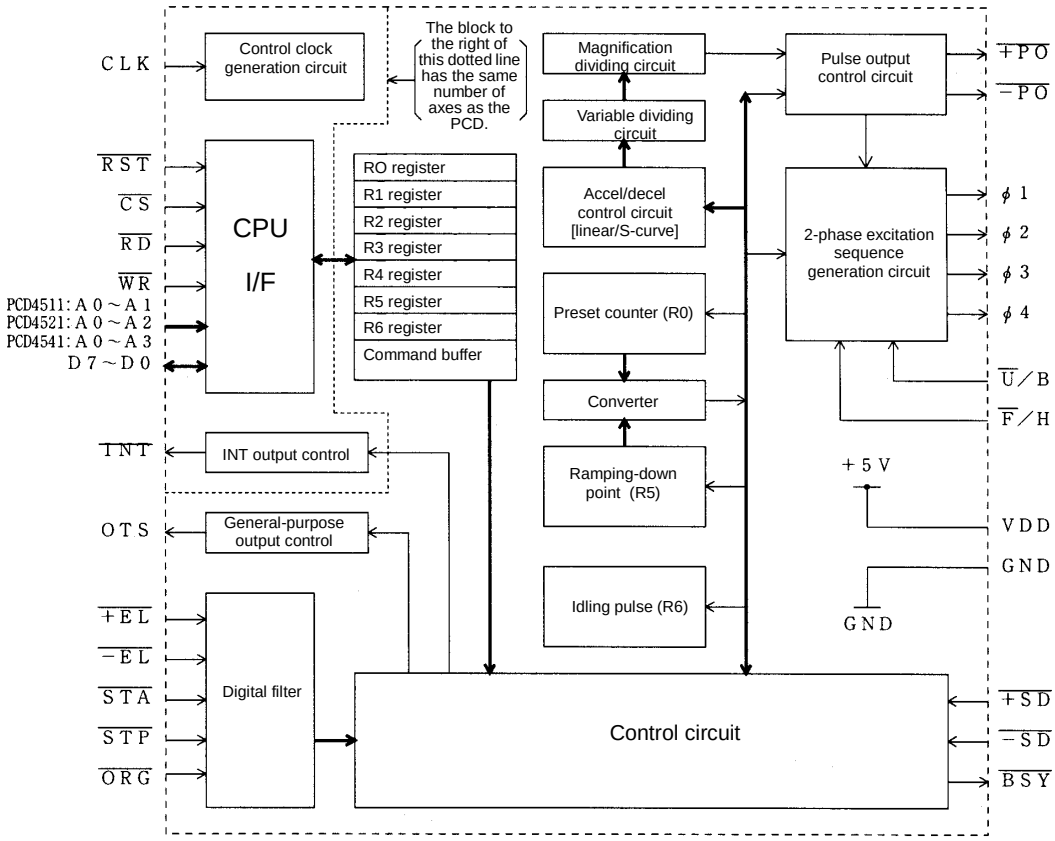
* R/W: Read/Write register

W(R): Write only register. However, reading is possible by enabling the extension monitor.

Note: Only the PCD4541 can write a "1" to R7. "0" must be written to this register on the PCD4511 and 4521.

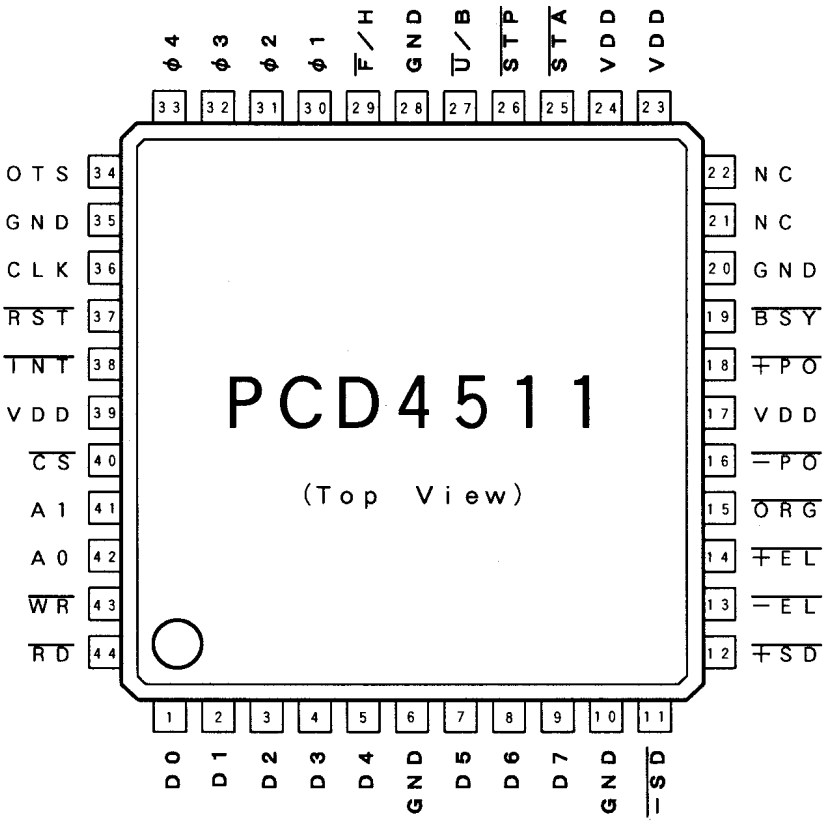
## 4. Hardware description

4-1. Circuit block diagram

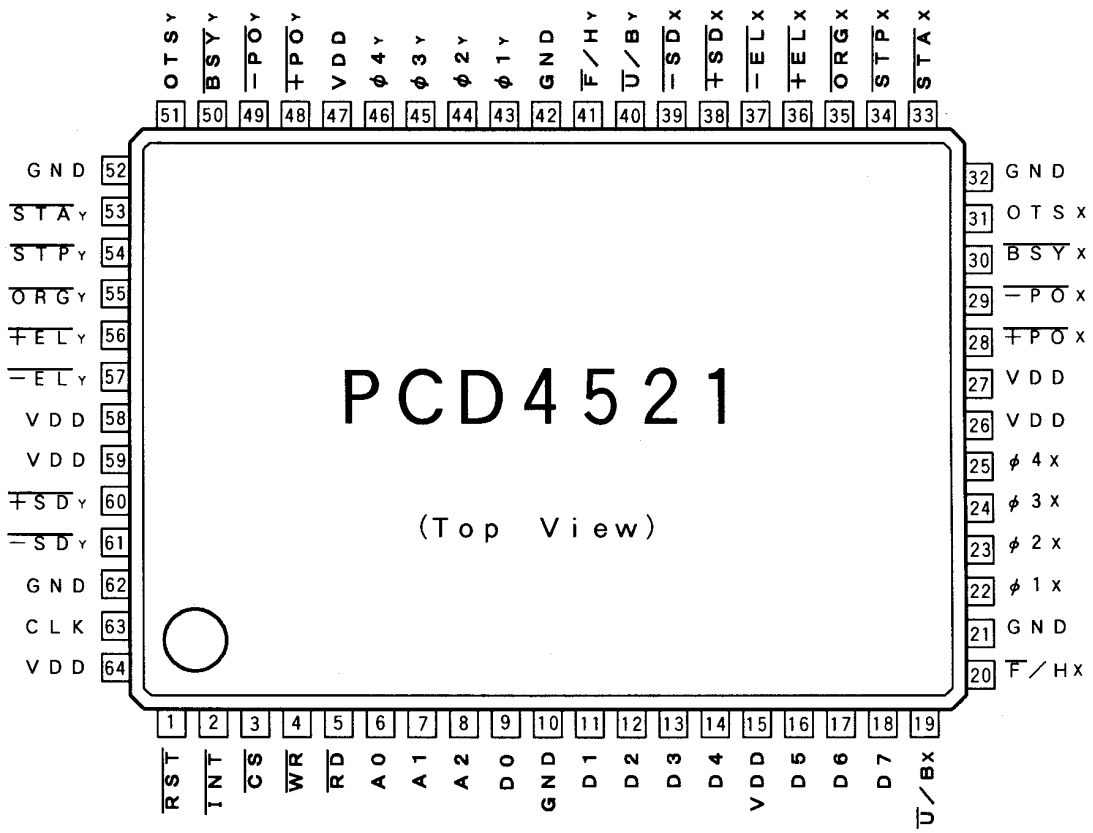


4-2. Terminal assignment diagrams

4-2-1. Terminal assignment diagram for the PCD4511



4-2-2. Terminal assignment diagram for the PCD4521



4-2-3. Terminal assignment diagram for the PCD4541

4-3. List of terminals

4-3-1. List of terminals on the PCD4511

| Terminal number | Terminal name | Input/output | Logic | General description |
|---|---|---|---|---|
| 1 to 5 | D0 to D4 | Input/output | Positive | Data bus signal |
| 6, 10, 20, 28, 35 | GND | | | 0 V |
| 7 to 9 | D5 to D7 | Input/output | Positive | Data bus signal |
| 11 | $\overline{\text{- SD}}$ | Input % | Negative | Negative deceleration switch signal |
| 12 | $\overline{\text{+ SD}}$ | Input % | Negative | Positive deceleration switch signal |
| 13 | $\overline{\text{- EL}}$ | Input % | Negative | Negative end limit switch signal |
| 14 | $\overline{\text{+ EL}}$ | Input % | Negative | Positive end limit switch signal |
| 15 | $\overline{\text{ORG}}$ | Input % | Negative | Zero position limit switch signal |
| 16 | $\overline{\text{- PO}}$ | Output | Negative # | Negative pulse |
| 17, 23, 24, 39 | VDD | | | +5V±10% |
| 18 | $\overline{\text{+ PO}}$ | Output | Negative # | Positive pulse |
| 19 | $\overline{\text{BSY}}$ | Output | Negative | Running signal |
| 21, 22 | NC | Output | | Test signal |
| 25 | $\overline{\text{STA}}$ | Input % | Negative | External start signal |
| 26 | $\overline{\text{STP}}$ | Input % | Negative | Forced stop signal |
| 27 | $\overline{\text{U}}$/B | Input % | | Select excitation method (unipolar/bipolar) |
| 29 | $\overline{\text{F}}$/H | Input % | | Select excitation sequence (2-2 phase / 1-2 phase) |
| 30 | Φ 1 | Output | Positive | 1st phase excitation signal |
| 31 | Φ 2 | Output | Positive | 2nd phase excitation signal |
| 32 | Φ 3 | Output | Positive | 3rd phase excitation signal |
| 33 | Φ 4 | Output | Positive | 4th phase excitation signal |
| 34 | OTS | Output | Positive | General-purpose output signal |
| 36 | CLK | Input | | Reference clock |
| 37 | $\overline{\text{RST}}$ | Input | Negative | Reset signal |
| 38 | $\overline{\text{INT}}$ | Output* | Negative | Interrupt signal |
| 40 | $\overline{\text{CS}}$ | Input | Negative | Chip select signal |
| 41, 42 | A1, A0 | Input | Positive | Address signal |
| 43 | $\overline{\text{WR}}$ | Input | Negative | Write signal |
| 44 | $\overline{\text{R D}}$ | Input | Negative | Read signal |

- A "*" in the input/output column means that a pull up resistor is integrated into the open drain output. (These outputs can be wire ORed).
- A "%" in the input/output column means that a pull up resistor is integrated into the input. (To avoid a high impedance state.)
- A "#" in the logic column means that the logic for this signal can be inverted. The condition given refers to the initial status.
- Make sure that all 5 GND terminals are connected and that all 4 VDD terminals are connected.
- Leave both NC terminals open.

4-3-2. List of terminals on the PCD4521

| Terminal number | Terminal name | Input/output | Logic | General description |
|---|---|---|---|---|
| 1 | $\overline{RST}$ | Input | Negative | Reset signal |
| 2 | $\overline{INT}$ | Output* | Negative | Interrupt signal |
| 3 | $\overline{CS}$ | Input | Negative | Chip select signal |
| 4 | $\overline{WR}$ | Input | Negative | Write signal |
| 5 | $\overline{R\ D}$ | Input | Negative | Read signal |
| 6, 7, 8 | A0 to A2 | Input | Positive | Address signal |
| 9 | D0 | Input/output | Positive | Data bus signal |
| 10, 21, 32, 42, 52, 62 | GND | | | 0 V |
| 11 to 14 | D1 to D4 | Input/output | Positive | Data bus signal |
| 15, 26, 27, 47, 58, 59, 64 | VDD | | | +5V ±10% |
| 16 to 18 | D5 to D7 | Input/output | Positive | Data bus signal |
| 19 (X), 40(Y) | $\overline{U}$/B | Input % | | Select excitation method (unipolar/bipolar) |
| 20 (X), 41(Y) | $\overline{F}$/H | Input % | | Select excitation sequence (2-2 phase / 1-2 phase) |
| 22 (X), 43(Y) | Φ 1 | Output | Positive | 1st phase excitation signal |
| 23 (X), 44(Y) | Φ 2 | Output | Positive | 2nd phase excitation signal |
| 24 (X), 45(Y) | Φ 3 | Output | Positive | 3rd phase excitation signal |
| 25 (X), 46(Y) | Φ 4 | Output | Positive | 4th phase excitation signal |
| 28 (X), 48(Y) | $\overline{+ PO}$ | Output | Negative # | Positive pulse |
| 29 (X), 49(Y) | $\overline{- PO}$ | Output | Negative # | Negative pulse |
| 30 (X), 50(Y) | $\overline{BSY}$ | Output | Negative | Running signal |
| 31 (X), 51(Y) | OTS | Output | Positive | General-purpose output signal |
| 33 (X), 53(Y) | $\overline{STA}$ | Input % | Negative | External start signal |
| 34 (X), 54(Y) | $\overline{STP}$ | Input % | Negative | Forced stop signal |
| 35 (X), 55(Y) | $\overline{ORG}$ | Input % | Negative | Zero position limit switch signal |
| 36 (X), 56(Y) | $\overline{+ EL}$ | Input % | Negative | Positive end limit switch signal |
| 37 (X), 57(Y) | $\overline{- EL}$ | Input % | Negative | Negative end limit switch signal |
| 38 (X), 60(Y) | $\overline{+ SD}$ | Input % | Negative | Positive deceleration switch signal |
| 39 (X), 61(Y) | $\overline{- SD}$ | Input % | Negative | Negative deceleration switch signal |
| 63 | CLK | Input | | Reference clock |

- "X" in the terminal number column is the terminal number for the X axis, "Y" is for the Y axis.
- A "*" in the input/output column means that a pull up resistor is integrated into the open drain output. (These outputs can be wire ORed.)
- A "%" in the input/output column means that a pull up resistor is integrated into the input. (To avoid a high impedance state.)
- A "#" in the logic column means that the logic for this signal can be inverted. The condition given refers to the initial status.
- Make sure that all 6 GND terminals are connected and that all 7 VDD terminals are connected.

4-3-3. List of terminals on the PCD4541

| Terminal number | Terminal name | Input/output | Logic | General description |
|---|---|---|---|---|
| 1, 2, 3, 4 | A0 to A3 | Input | Positive | Address signal |
| 5 | $\overline{\text{INT}}$ | Output* | Negative | Interrupt signal |
| 6, 16, 41, 54, 67, 68, 91, 95 | VDD | | | +5V ±10% |
| 7 to 14 | D0 to D7 | Input/output | Positive | Data bus signal |
| 15, 27, 40, 66, 90, 93 | GND | | | 0 V |
| 17(X), 35(Y), 62(Z), 82(U) | $\overline{\text{BSY}}$ | Output | Negative | Running signal |
| 18(X), 36(Y), 63(Z), 83 (U) | Φ 1 | Output | Positive | 1st phase excitation signal |
| 19(X), 37(Y), 64(Z), 84(U) | Φ 2 | Output | Positive | 2nd phase excitation signal |
| 20(X), 38(Y), 65(Z), 85(U) | Φ 3 | Output | Positive | 3rd phase excitation signal |
| 21(X), 39(Y), 69(Z), 86(U) | Φ 4 | Output | Positive | 4th phase excitation signal |
| 22(X), 42(Y), 70(Z), 87(U) | $\overline{\text{+ PO}}$ | Output | Negative # | Positive pulse |
| 23(X), 43(Y), 71(Z), 88(U) | $\overline{\text{- PO}}$ | Output | Negative # | Negative pulse |
| 24(X), 44(Y), 72(Z), 89(U) | OTS | Output | Positive | General-purpose output signal |
| 25(X), 45(Y), 73(Z), 96(U) | $\overline{\text{U}}$/B | Input % | | Select excitation method (unipolar/bipolar) |
| 26(X), 46(Y), 74(Z), 97(U) | $\overline{\text{F}}$ /H | Input % | | Select excitation sequence (2-2 phase / 1-2 phase) |
| 28(X), 47(Y), 55(Z), 75(U) | $\overline{\text{STA}}$ | Input % | Negative | External start signal |
| 29(X), 48(Y), 56(Z), 76(U) | $\overline{\text{STP}}$ | Input % | Negative | Forced stop signal |
| 30(X), 49(Y), 57(Z), 77(U) | $\overline{\text{ORG}}$ | Input % | Negative | Zero position limit switch signal |
| 31(X), 50(Y), 58(Z), 78(U) | $\overline{\text{+ EL}}$ | Input % | Negative | Positive end limit switch signal |
| 32(X), 51(Y), 59(Z), 79(U) | $\overline{\text{- EL}}$ | Input % | Negative | Negative end limit switch signal |
| 33(X), 52(Y), 60(Z), 80(U) | $\overline{\text{+ SD}}$ | Input % | Negative | Positive deceleration switch signal |
| 34(X), 53(Y), 61(Z), 81(U) | $\overline{\text{- SD}}$ | Input % | Negative | Negative deceleration switch signal |
| 92 | CLK | Input | | Reference clock |
| 94 | $\overline{\text{RST}}$ | Input | Negative | Reset signal |
| 98 | $\overline{\text{CS}}$ | Input | Negative | Chip select signal |
| 99 | $\overline{\text{RD}}$ | Input | Negative | Read signal |
| 100 | $\overline{\text{WR}}$ | Input | Negative | Write signal |

- "X" in the terminal number column is the terminal number for the X axis, "Y" is for the Y axis, "Z" is for the Z axis, and "U" refers to the U axis.
- A "*" in the input/output column means that a pull up resistor is integrated into the open drain output. (These outputs can be wire ORed.)
- A "%" in the input/output column means that a pull up resistor is integrated into the input. (To avoid a high impedance state.)
- A "#" in the logic column means that the logic for this signal can be inverted. The condition given refers to the initial status.
- Make sure that all 6 GND terminals are connected and that all 8 VDD terminals are connected.

4-4. Description of each terminal

4-4-1. $\overline{+SD}$, $\overline{-SD}$

Input terminals for deceleration speed switch signals.
When $\overline{SD}$ signal control is enabled in the control mode command, and when the $\overline{SD}$ signal with the same polarity as the current direction of rotation goes LOW while in high-speed operation, the LSI will start to decelerate.
When the $\overline{SD}$ signal goes HIGH again, the LSI will begin to accelerate again.

4-4-2. $\overline{+EL}$, $\overline{-EL}$

Input terminals for the end limit switch signals.
When the $\overline{EL}$ signal which has the same polarity as the current direction of motor rotation goes LOW, the LSI will stop the motor immediately. The LSI will not restart the motor, even when this signal goes HIGH again.
If the $\overline{EL}$ signal is already LOW and an attempt is made to start the motor rotating in that direction, the LSI will not let it start.
When pulse output control is set to "halt output (timer mode)" using the output mode command, the $\overline{EL}$ signal is disabled.

4-4-3. $\overline{ORG}$

Input terminal for the zero position switch signal.
When $\overline{ORG}$ signal control is enabled (zero position return operation) using the control mode command, and when this signal goes LOW, the motor will stop immediately. Even if this signal goes HIGH again, the LSI not start the motor.
If the $\overline{ORG}$ signal is already LOW and an attempt is made to start the motor, the LSI will not let it start.
When pulse output control is selected "halt output (timer mode)" using the output mode command, the $\overline{ORG}$ signal is disabled.

4-4-4. $\overline{STP}$

Input terminal for the forced stop signal.
When the $\overline{STP}$ signal goes LOW, regardless of the rotation direction of the motor, the motor will stop immediately. Even if this signal goes HIGH again, the LSI will not start the motor.
If the $\overline{STP}$ signal is already LOW and an attempt is made to start the motor, the LSI will not let it start.

4-4-5. $\overline{STA}$

Input terminal for external start signal.
When a start latch command is entered using the start mode command, the motor will start rotation on the leading edge of an $\overline{STA}$ signal transition from HIGH to LOW.
A signal shorter than 4 cycles of the reference clock is not accepted.

4-4-6. $\overline{+PO}$, $\overline{-PO}$

Pulse output terminals.

When the rotation direction is set to positive using the control mode command, the LSI will output pulses at a 50% duty cycle from $\overline{+PO}$ terminal. When the rotation direction is set to negative using the control mode command, the LSI will output pulses at a 50% duty cycle from $\overline{-PO}$ terminal.

The logic of the $\overline{+PO}$ and $\overline{-PO}$ terminals, and the ON/OFF control of pulse outputs, can be changed using the output mode command.

4-4-7. $\phi 1, \phi 2, \phi 3$, and $\phi 4$

Excitation signal output terminals for a stepper motor.

The switching of the excitation sequencing signals is synchronized with the output pulses.

Using the $\overline{F}$/H terminals, you can select between 1-2 phase and 2-2 phase excitation sequencing.

Using the $\overline{U}$/B terminals, you can select between unipolar and bipolar excitation sequencing.

When pulse output control is set to "halt output (timer mode)" using the output mode command, the excitation sequencing cannot be changed.

Using the output mode command, the excitation signal can be masked (to make all of the terminals $\phi 1$ to 4 LOW).

4-4-8. $\overline{U}$/B

Terminal for selecting the excitation method.

Select unipolar excitation with a LOW or bipolar excitation sequencing with a HIGH on this terminal. Connect to GND or VDD.

This terminal is latched when reset.

For details about the sequence for reading this terminal, see "6-1. Excitation sequencing for stepper motors."

4-4-9. $\overline{F}$/H

Terminal for selecting the excitation sequence.

2-2 phase and 1-2 phase are typical excitation sequences for 2-phase stepper motors. Select the sequence using this terminal.

Select 2-2 phase excitation with a LOW and 1-2 phase excitation sequencing with a HIGH. Connect to GND or VDD.

For details about the sequence for reading this terminal, see "6-1. Excitation sequencing for stepper motors."

4-4-10. OTS

General-purpose output terminal.

This terminal can be used as an excitation ON/OFF control signal for a motor driver IC. This terminal can be controlled by a CPU. When bit 4 of the control mode command is "1" this terminal is HIGH, when it is "0" the terminal is LOW.

4-4-11. $\overline{INT}$

Output terminal for sending an interrupt request signal to a CPU.
This terminal will go LOW when the LSI requests an interrupt. Set this signal HIGH using the interrupt condition setting command. This terminal can also be masked.
By setting the start mode command, the LSI can be set to output an $\overline{INT}$ request signal when stopping the motor. Using this terminal, you can call for an interrupt when the preset operation is complete, or when operation is stopped by the $\overline{ORG}$ signal, $\overline{+EL}$ or $\overline{-EL}$ signal, or the $\overline{STP}$ signal. An interrupt can also be requested by a deceleration stop or an immediate stop command.
Using the register select command, an $\overline{INT}$ request signal can be output when starting deceleration from the ramping-down point or from an external signal.
When using PCD series LSIs, the $\overline{INT}$ terminals of a number of chips can be wire ORed. Install an external pull up resistor (5 to 10 K ohms).

4-4-12. $\overline{BSY}$

Operation status monitor terminal.
When the LSI is in operation, the signal from this terminal goes LOW.
This terminal can be used to check the operation or to provide current to the motor and force it to remain stopped.

4-4-13. CLK

Input terminal for the reference clock.
Reference clock precision affects the output pulse precision.
Besides affecting the output pulses, it also affects the input sensitivity of the start timing signal, $\overline{STA}$, $\overline{ORG}$, $\overline{EL}$ and $\overline{STP}$ signals, as well as read and write timing.
Make sure that only a CMOS level input is applied to the CLK terminal.

4-4-14. $\overline{RST}$

Reset signal input terminal.
Bring this terminal LOW for 3 reference clock pulses to reset the LSI.
For details about the initial status after a reset, see "4-6. Initial status."

4-4-15. $\overline{CS}$

Chip select signal input terminal
Bring this terminal LOW to enable $\overline{RD}$ and $\overline{WR}$ signals, which will allow reading and writing to the CPU.

4-4-16. $\overline{RD}$

Read signal input terminal
Bring this terminal and the $\overline{CS}$ terminal LOW to output the contents of the specified register on data bus lines D0 to D7.

4-4-17. $\overline{WR}$

Write signal input terminal

Bring this terminal and the $\overline{CS}$ terminal LOW to write the contents of data bus lines D0 to D7 into the LSI. The lines will be read when the $\overline{WR}$ signal changes from LOW to HIGH.

4-4-18. A0, A1, A2, and A3

Address signal input terminals.

The LSI uses the A0 and A1 terminals to assign use of the data bus to the command buffer, and to the upper, middle, and lower areas of register data.

On the PCD4521 and 4541, terminals A2 and A3 are used to select the axis to control.

Normally, this terminal is connected to the lowest bit on the CPU address bus.

4-4-19. D0 to D7

Input and output terminals for the tri-state data bus.

4-4-20. VDD and GND

Power supply terminals.

Supply +5VDC ±10% to the VDD terminals. Make sure to connect all of the power supply terminals.

4-4-21. NC [PCD4511 only]

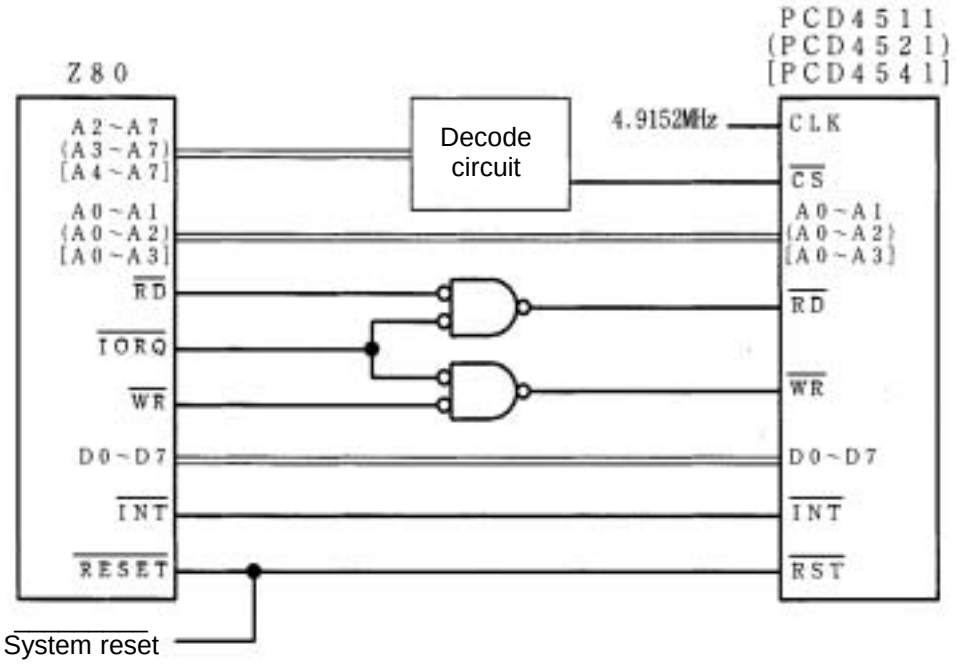
Output terminal for testing. Leave this terminal open.

4-5. Initial (reset) status

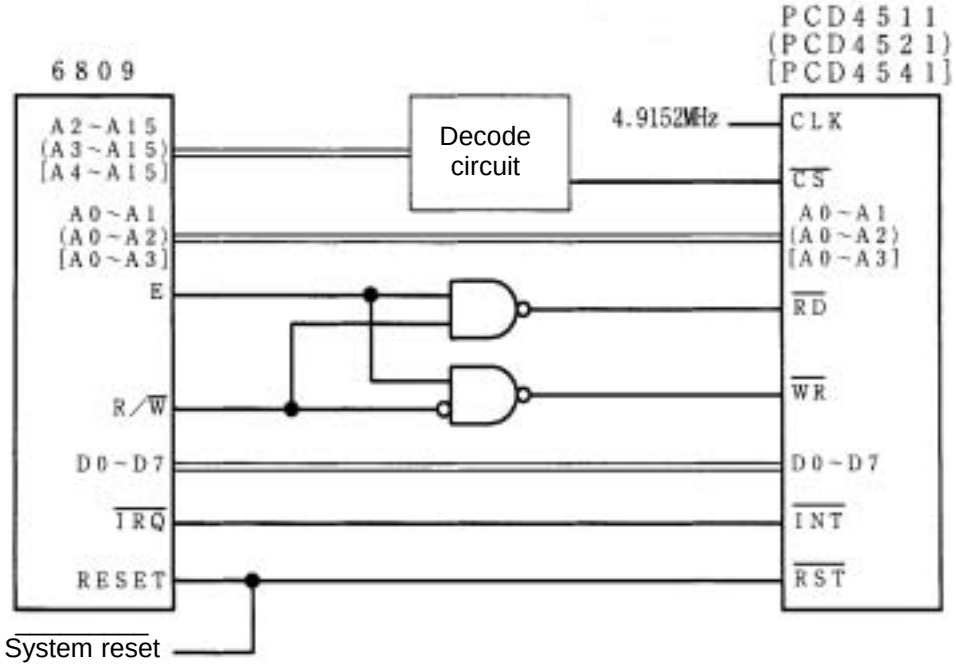
| Item | Initial (reset) status |
|---|---|
| Internal registers (R0 to R6) | All zeros |
| Start mode command | 00 HEX |
| Control mode command | 40 HEX |
| Register select command | 80 HEX |
| Output mode command | C0 HEX |
| $\overline{INT}$ terminal | H |
| Terminals D0 to D7 | High impedance |
| $\phi$1, $\phi$2, $\phi$3, and $\phi$4 [$\overline{U}$/B terminal = when L] | H, L, L, H |
| $\phi$1, $\phi$ $\phi$2, $\phi$3, and $\phi$4 [$\overline{U}$/B terminal = when H] | H, L, L, L |
| $\overline{\pm PO}$terminal | H |
| $\overline{BSY}$ terminal | H |
| OTS terminal | L |

4-6. CPU interface circuit block diagram

1) Z80 interface




2) 6809 interface



4-7. Precautions for designing hardware

4-7-1. Input terminals

Only the CLK terminal requires a CMOS level input. Be careful when connecting this terminal. (For reset operations, the internal processing may require up to three reference clock cycles. When imposing a LOW on the $\overline{RST}$ terminal make sure it lasts more than 3 reference clock cycles.)

If you want to wire-OR the $\overline{INT}$ terminal or input the switch signal terminals with open collectors, we recommend installing a pull up resistor.

(The $\overline{\pm EL}$, $\overline{\pm SD}$, $\overline{ORG}$, $\overline{STA}$, $\overline{STP}$, and $\overline{INT}$ terminals on the PCD4511 have pull-up resistors built in. However these are for preventing a high impedance condition. Since their resistance values are high [25 K to 500 K ohm], we recommend installing external pull-up resistors [5-K to 10-K ohms].)

For safe operation, we recommend using a multiple-layer PC board with a separate power layer.

4-7-2. Excitation sequencing

The description of the excitation sequence required by a particular bipolar 1-2 phase stepper motor driver IC may be different.

(This LSI's excitation sequence is designed for our NP-7024M (7026M) unipolar driver IC, and our NP-2918 bipolar driver IC. These are common excitation sequences. However, bipolar excitation sequence requirements may vary with different driver IC manufacturers. Driver ICs which can use the following excitation sequence may be used. In this case, contact the driver IC manufacturer to verify the suitability of our excitation sequence.)

Ex.1

| 1-2 phase excitation for bipolar drivers | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| STEP -> | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 |
| A | H | H | H | L | L | L | L | L | H |
| DISABLE A | L | L | L | H | L | L | L | H | L |
| B | L | L | H | H | H | L | L | L | L |
| DISABLE B | L | H | L | L | L | H | L | L | L |

Ex. 2

| 1-2 phase excitation for bipolar drivers | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| STEP -> | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 |
| A | H | H | H | H | L | L | L | H | H |
| DISABLE A | L | L | L | H | L | L | L | H | L |
| B | L | H | H | H | H | H | L | L | L |
| DISABLE B | L | H | L | L | L | H | L | L | L |

In the two examples above, the LSI can be operated by connecting terminals $\phi 1$ to A, $\phi 2$ to B, $\phi 3$ to DISABLE A, and $\phi 4$ to DISABLE B.

## 5. Programming Description

5-1. Addresses

5-1-1. PCD4511 addresses

Shown below is the relationship between address lines A1, A0 and control lines $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$.

| $\overline{CS}$ | $\overline{RD}$ | $\overline{WR}$ | A1 | A0 | Details | |
|---|---|---|---|---|---|---|
| L | H | L | L | L | Data bus -> Command buffer | Writing |
| L | H | L | L | H | Data bus -> Register (bits7 to 0: Lower) | |
| L | H | L | H | L | Data bus -> Register (bits15 to 8: Middle) | |
| L | H | L | H | H | Data bus -> Register (bits23 to 16: Upper) | |
| L | L | H | L | L | Data bus <- Status0 | Reading |
| L | L | H | L | H | Data bus <- Internal data (Lower) | |
| L | L | H | H | L | Data bus <- Internal data (Middle) | |
| L | L | H | H | H | Data bus <- Internal data (Upper) | |
| L | L | L | X | X | Prohibited | |
| H | X | X | X | X | Data bus = High impedance | |

5-1-2. PCD4521 addresses

Specify the axis using address line A2, and select the control data using address lines A1, A0 and control lines $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$. The relationship between address lines A1, A0 and control lines $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ are the same as in the PCD4511.

| A2 setting | A2 = 0 | A2 = 1 |
|---|---|---|
| Selected axis | X axis | Y axis |

| $\overline{CS}$ | $\overline{RD}$ | $\overline{WR}$ | A1 | A0 | Details |
|---|---|---|---|---|---|
| | | | | | Same as for the PCD4511. |

5-1-3. PCD4541 addresses

Specify the axis using address lines A3, A2, and select the control data using address lines A1, A0, and control lines $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$. The relationship between address lines A1, A0 and control lines $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ are the same as in the PCD4511.

| A3, A2 setting | A3 = 0, A2 = 0 | A3 = 0, A2 = 1 | A3 = 1, A2 = 0 | A3 = 1, A2 = 1 |
|---|---|---|---|---|
| Selected axis | X axis | Y axis | Z axis | U axis |

| $\overline{CS}$ | $\overline{RD}$ | $\overline{WR}$ | A1 | A0 | Details |
|---|---|---|---|---|---|
| | | | | | Same as for the PCD4511. |

5-2. Read and write the data register

5-2-1. Write procedures

To specify a register, use the register select command.
The LSI interprets the data written on address lines (A1 = 0, A0 = 0) as a command. It also interprets "10XXXXXX BIN" as a register select command.

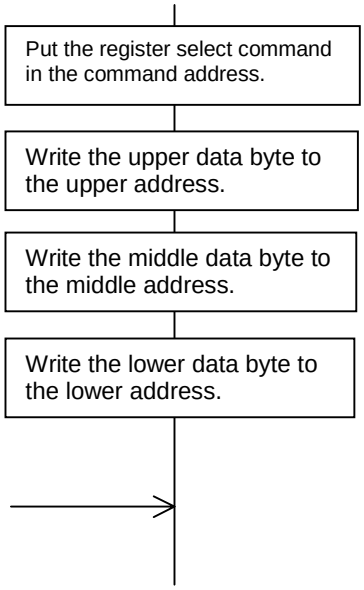
1) To write data, enter the register number using the register select command.

2) Write the upper byte (bits 23 to 16) of the data to the upper address (A1 = 1, A0 =1) of the register.

3) Write the middle byte (bits 15 to 8) of the data to the middle address (A1 = 1, A0 =0) of the register.

4) Write the lower byte (bits 7 to 0) of the data to the lower address (A1 = 0, A0 =1) of the register.

5) Since the LSI will be processing the data internally, do not write any other command or data for a period of two reference clock cycles (approx. 400 ns when CLK = 4.9152 MHz)




5-2-2. Read procedures (Example: Read the number of pulses remaining in R0 [Preset counter])

The PCD4511/4521/4541 can read the data in any register. Select a register and read the data the same way that data is written to that register.

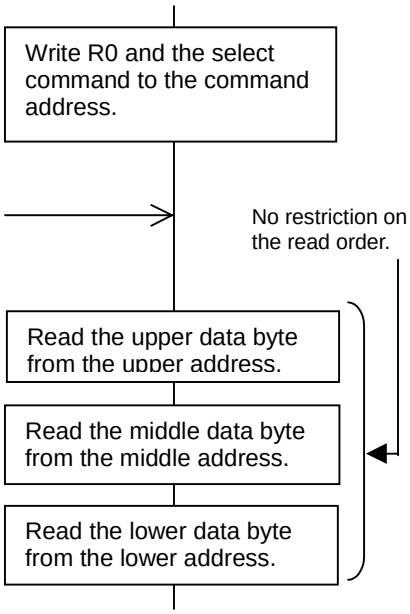
1) Enter R0 as the register you want using the register select command.

2) Since the LSI will process the command internally, wait at least 1.5 reference clock cycles (approx. 300 ns when CLK = 4.9152 MHz)

3) Read the upper data byte (bits 23 to 16) from the upper register address (A1 = 1, A0 =1).

4) Read the middle data byte (bits 15 to 8) from the middle register address (A1 = 1, A0 =0).

5) Read the lower data byte (bits 7 to 0) from the lower register address (A1 = 0, A0 =1).



Note: The Preset counter data is copied to the read buffer when the register select command is entered. When reading data, the LSI reads the contents of this buffer. Therefore, there is no restriction on the order in which the bytes are read.
Other register data can also be read by selecting the output mode. However, a buffer is not used to read that data. The LSI reads the internal data directly.
Therefore, to read data while operating or when data accuracy is required, you have to read the data twice.

5-3. Internal data monitor

With the standard monitor selected, the LSI can read status registers 0, 1, and R0 [the Preset counter]. By selecting the extension monitor, the LSI can also read Status registers 2, 3, and R1 to R6, as well as the current command. Use the output mode command to select the standard monitor or extension monitor.
By combining address and register specifications, the following data can be monitored.

When the standard monitor is selected (output mode: bit 5 = 0)

| Address / Register | A1 = 0, A0 = 0 | A1 = 0, A0 = 1 | A1 = 1, A0 = 0 | A1 = 1, A0 = 0 |
|---|---|---|---|---|
| R0 | Status0 | R0 lower data | R0 middle data | R0 upper data |
| R1 to R7 | Status0 | Status1 | 0 | 0 |

When the extension monitor is selected (output mode: bit 5 = 1)

| Address / Register | A1 = 0, A0 = 0 | A1 = 0, A0 = 1 | A1 = 1, A0 = 0 | A1 = 1, A0 = 1 |
|---|---|---|---|---|
| R0 | Status0 | R0 lower data | R0 middle data | R0 upper data |
| R1 | Status0 | R1 lower data | R1 upper data | Start mode command |
| R2 | Status0 | R2 lower data | R2 upper data | Control mode command |
| R3 | Status0 | R3 lower data | R3 upper data | Register select command |
| R4 | Status0 | R4 lower data | R4 upper data | Output mode command |
| R5 | Status0 | R5 lower data | R5 upper data | R7 data |
| R6 | Status0 | R6 data | Speed lower data | Speed upper data |
| R7 | Status0 | Status1 | Status2 | Status3 |

5-3-1. Reading Status

There are two status modes: Status0 is used for monitoring the operation status, and Status1 for monitoring the input status of signals such as $\overline{\pm EL}$, $\overline{\pm SD}$, $\overline{ORG}$, $\overline{STA}$, and $\overline{STP}$.
By selecting the extension monitor, Status2 can be read in order to monitor the output status of $\overline{\pm PO}$, $\phi$1 to 4, $\overline{INT}$, and $\overline{OTS}$ signals, and Status3 can be read in order to identify the PCD type.
There is no restriction on reading Status0. However, since Status1, 2, and 3 share the address line with a data register, there are restrictions on reading them.
To read Status1, 2, and 3, select register R7 (any register setting other than R0 when the standard monitor is selected), and Status1, Status2, and Status3 can be read from the lower data, middle data, and upper data bytes, respectively.
Since the Status' bytes are latched when reading starts, the data bus will not change while in the reading cycle.

5-3-2. Reading the register, command, and speed data

In addition to the status registers, the LSI can read register, command, and speed data. When the standard monitor is selected, only register R0 can be read. However, when the extension monitor is selected, registers R1 to R6 can also be read.

When the extension monitor is selected, the start command, control mode command, register select command, output mode command and the current speed data can all be read.

Please note that when register R3 is selected, the LSI will read the register select command from address lines A1 =1 and A0 =1, as shown in the lower part of the table in section 5-3 above. In other words, to read the register select command, you have to select register R3. Therefore, use this function only to check bits other than the register select bits.

However, the start control bit shows the internal status of the LSI, not the status of the command you write. Therefore when reading the LSI status using the start mode command, the start control bit will be "1" when running and it will change to "0" when the motor is stopped.

Since the LSI reads the internal data directly when reading the speed data, rounding up or down may occur while reading the middle and lower bytes. In this case, check the data by reading it twice.

5-4. Precautions when writing programs

5-4-1. Read/write data

[To write data to a register, write the lower data last.]

The upper and middle data bytes for a register are latched into a write buffer and transferred to the appropriate internal locations according to the write timing for the lower data byte. Therefore, write the lower data byte for the register (bits 7 to 0) last.

[To read the value in the preset counter, select R0 first.]

The value in the preset counter (number of pulses remaining) is latched into the read buffer according to the timing when the register select command is written. Therefore, you have to write the R0 register select command each time you want to read the value, even if you will be reading the value repeatedly.

There is no restriction on the read order of the upper, middle, and lower data bytes.

[To read the value in the preset counter, allow 1.5 reference clock cycles of time for internal processing. To write data to the register, allow 2 reference clock cycles of time for internal processing.]

To read the preset counter value, allow 1.5 reference clock cycles of time for internal processing after writing the register select command. Do not read any data during this period.

To write register data, allow 2 reference clock cycles of time for internal processing after writing the lower register data. Do not write any data during this period.

5-4-2. Data setting

[Even if a register is not used, set the register data within the specified range.]

When the motor is stopped instantly using an immediate stop command or the $\overline{STP}$, $\overline{\pm EL}$, or $\overline{ORG}$ signals, the motor will turn at FL speed until the last pulse is used after the stop signal is input.

For this reason, when the motor is running at FH speed and stopped instantly, the LSI will apply the FL speed until the balance of remaining pulses has been used. If the FL speed is not yet set, the motor will simply stop, leaving a number of pulses unused.

As such, if a value outside the allowable range is specified, it may cause a problem. Therefore, we recommend that you enter appropriate values for all currently unused registers. For details about the allowable range of each register, see "3. Table of registers."

[Enter data with the correct number of bits]

The last data written will remain in the write buffer until new data is written. Enter data with the correct number of bits, in order to prevent incorrect setting of the registers.

5-4-3. Preparation for starting

[Write the start mode command as the last command.]

When the start mode command is given, the LSI will trigger rotation of the motor. Therefore, only write the start mode command at the end of a setup sequence.

[Do not set bits 1, 3 and 4 to "1" at the same time in the start mode command.]

Turning ON ("1") the Start Control, Stop Control, and External Start Control bits in the start mode command at the same time will keep the operation from starting on reception of the next start command. Never set more than one of bits 1, 3, and 4 to "1" at the same time.

## 6. Description of functions

6-1. Excitation sequencing of stepper motors

This LSI can generate 1-2 phase and 2-2 phase excitation sequences for 2-phase stepper motors, in unipolar or bipolar driving modes.

Use the $\overline{U}$/B terminal to switch between unipolar and bipolar. This setting is latched during an LSI reset initiated on the $\overline{RST}$ terminal.

Use the $\overline{F}$/H terminal to switch between 1-2 phase and 2-2-phase excitation. This setting is not latched, and can be changed during operation. When the LSI is switched from 1-2 phase excitation to 2-2 phase excitation while the motor is in certain excitation phases (steps 1, 3, 5, and 7 of the 1-2 phase excitation sequence shown in the table below), the motor will change to 2-phase excitation with the next pulse output.

[Unipolar excitation sequence]

| 2-2 phase excitation | | | | | |
|---|---|---|---|---|---|
| Step -> | 0 | 1 | 2 | 3 | 0 |
| 1φ | H | H | L | L | H |
| 2φ | L | H | H | L | L |
| 3φ | L | L | H | H | L |
| 4φ | H | L | L | H | H |
| Φ - Z | H | L | L | L | H |
| Negative <- Rotation direction -> Positive | | | | | |

| 1-2 phase excitation | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Step -> | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 |
| 1φ | H | H | H | L | L | L | L | L | H |
| 2φ | L | L | H | H | H | L | L | L | L |
| 3φ | L | L | L | L | H | H | H | L | L |
| 4φ | H | L | L | L | L | L | H | H | H |
| Φ - Z | H | L | L | L | L | L | L | L | H |
| Negative <- Rotation direction -> Positive | | | | | | | | | |

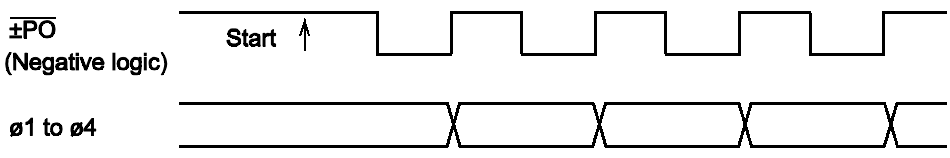
[Bipolar excitation sequence]

| 2-2 phase excitation | | | | | |
|---|---|---|---|---|---|
| Step -> | 0 | 1 | 2 | 3 | 0 |
| 1φ | H | H | L | L | H |
| 2φ | L | H | H | L | L |
| 3φ | L | L | L | L | L |
| 4φ | L | L | L | L | L |
| Φ - Z | H | L | L | L | H |
| Negative <- Rotation direction -> Positive | | | | | |

| 1-2 phase excitation | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Step -> | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 |
| 1φ | H | H | H | H | L | L | L | L | H |
| 2φ | L | L | H | H | H | H | L | L | L |
| 3φ | L | L | L | H | L | L | L | H | L |
| 4φ | L | H | L | L | L | H | L | L | L |
| Φ - Z | H | L | L | L | L | L | L | L | H |
| Negative <- Rotation direction -> Positive | | | | | | | | | |

φ — Z = Excitation zero position (This is the sequence when initialized. It can be read out from Status1.)

[Excitation sequence switching timing]



6-2. Speed pattern setting

6-2-1. Speed setting

Constant speed operation and high-speed operation (linear and S-curve acceleration /deceleration) can be specified. To specify a speed pattern, use R1, R2, R4, and R3 (when high-speed operation is used).
To change between constant speed and high speed, use bit 2 of the start mode command.
To change between linear and S-curve acceleration/deceleration, use bit 5 of the control mode command.

1) R1: FL speed setting register

This register is used to specify the speed for constant speed operation and the start speed for high-speed operation. The allowable range is 1 to 8,191 (1FFF HEX). The speed will be the product resulting from multiplying this value by the magnification rate specified in R4.

FL speed [PPS] = (Value specified in R1) x Magnification rate

2) R2: FH speed setting register

This register is used to specify the speed for constant speed operation and the operating speed for high-speed operation. For high-speed operation, specify a value that is larger than the value in R1. The allowable range is 1 to 8,191 (1FFF HEX). The speed will be the product resulting from multiplying this value by the magnification rate specified in R4.

FH speed [PPS] = (Value specified in R2) x Magnification rate

3) R3: Acceleration/deceleration rate register

This register is used to specify the acceleration/deceleration characteristics when high-speed operation is selected. The allowable range is 2 to 1,023 (3FF HEX). When the value for R3 is the same and a linear acceleration/deceleration is performed, the linear acceleration/deceleration speed will be equal to the maximum acceleration speed set for S-curve acceleration/deceleration.

[Linear accel/decel]

$$\text{Accel/decel time [Sec.]} = \frac{((\text{Value specified in R2}) - (\text{Value specified in R1})) \times (\text{Value specified in R3})}{\text{Reference clock frequency [Hz]}}$$

[S-curve accel/decel]

$$\text{Accel/decel time [Sec.]} = \frac{((\text{Value specified in R2}) - (\text{Value specified in R1})) \times (\text{Value specified in R3}) \times 2}{\text{Reference clock frequency [Hz]}}$$

4) R4: Magnification rate register

This register is used to specify the relationship between the values set in R1 and R2, in order to set the final speed. The allowable range is 2 to 1,023 (3FF HEX). The higher the magnification setting, the less accurate the speed units will be. Normally, use as small a

setting as possible. The relationship between the value selected and the magnification rate is as follows.

$$\text{Magnification} = \frac{\text{Reference clock frequency [Hz]}}{\text{(Value specified in R4)} \times 8192}$$

(When reference clock = 4.9152 MHz) (Output speed unit: PPS)

| Value in R4 | Magnification rate | Output speed range | Value in R4 | Magnification rate | Output speed range |
|---|---|---|---|---|---|
| 600 (258 HEX) | 1 | 1 to 8,191 | 60 (3C HEX) | 10 | 10 to 81,910 |
| 300 (12C HEX) | 2 | 2 to 16, 382 | 30 (1E HEX) | 20 | 20 to 163,820 |
| 120 (78 HEX) | 5 | 5 to 40,955 | 12 (0C HEX) | 50 | 50 to 409,550 |

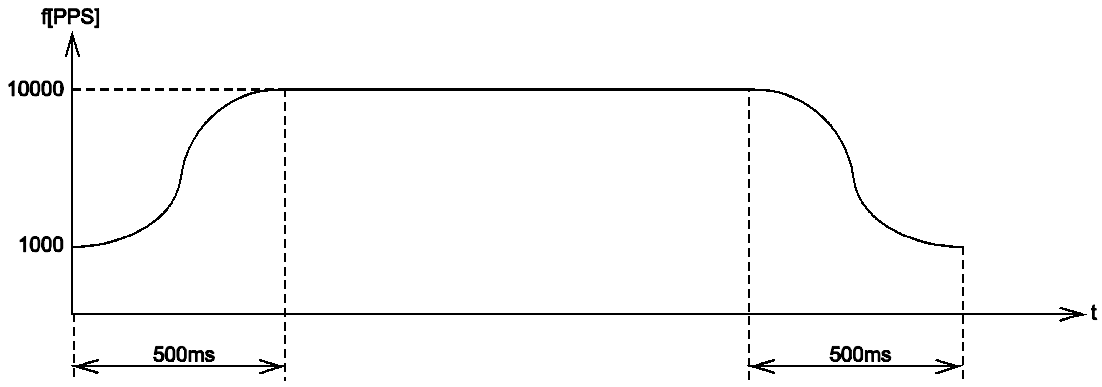
6-2-2. Example of setting the acceleration/deceleration speed pattern (S-curve accel/decel)

When the initial speed is 1,000 PPS, the operation speed is 10,000 PPS, the accel/decel time is 500 ms, and the reference clock is 4.9152 MHz, the value to use in R3 will be as follows.

1) The magnification rate used in order to output 10,000 PPS is 2x, and R4 will equal 300 (12C HEX)
2) In order to set the initial speed to 1,000 PPS in the 2x mode, R1 must equal 500 (1F4 HEX)
3) In order to set the operation speed to 10,000 PPS in the 2x mode, R2 must equal 5,000 (1388 HEX)
4) Calculate the value to use for R3 from the desired accel/decel time,
   Modify the calculation of the accel/decel time, and substitute the value,

$$\text{Value specified in R3} = \frac{\text{(Accel/decel time [Sec.]} \times \text{(Reference clock frequency [Hz])}}{\text{((Value specified in R2)} - \text{(Value specified in R1))} \times 2}$$

$$R3 = \frac{0.5 \times 4915200}{(5000 - 500) \times 2} = 273.07 \quad 273$$



6-2-3. Setting the ramping-down point

By entering a ramping-down point in the R5 register, the motor will automatically decelerate while operating in the preset or high-speed modes.
To specify this point, enter the number of remaining pulses which will trigger the deceleration. The motor will start deceleration when the contents of the Preset counter are equal to R5.
The allowable range is 0 to 65,535 (FFFF HEX). The following formula can be used to calculate the ramping-down point.

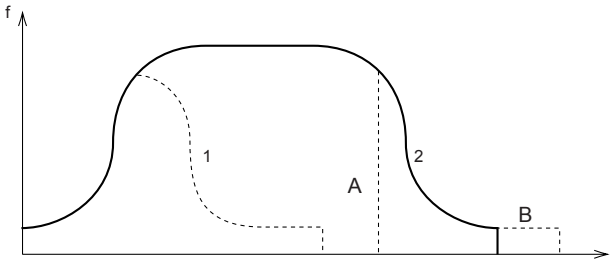
[Linear accel/decel]

$$\text{Value specified in R5 [pulses]} = \frac{((\text{Value specified in R2})^2 - (\text{Value specified in R1})^2) \times (\text{Value specified in R3})}{(\text{Value specified in R4}) \times 16384}$$

[S-curve accel/decel]

$$\text{Value specified in R5 [pulses]} = \frac{((\text{Value specified in R2})^2 - (\text{Value specified in R1})^2) \times (\text{Value specified in R3})}{(\text{Value specified in R4}) \times 8192}$$

[Speed pattern using a ramping-down point]




1) When the ramping-down point is reached while accelerating.
2) When the ramping-down point is reached after acceleration has been completed.
A) Too small a value for R5.
B) Too large a value for R5.

6-2-4. Example of setting a ramping-down point (S-curve accel/decel)

Select preset and high-speed operation with an initial speed of 1,000 PPS, an operation speed of 10,000 PPS, and an accel/decel rate in R3 of 273. Then the value of R5 will be as follows.

1) The magnification rate used in order to output 10,000 PPS is 2x, and R4 is set to 300 (12C HEX)
2) In order to make the initial speed 1,000 PPS in the 2x mode, R1 must equal 500 (1F4 HEX)
3) In order to make the operation speed 10,000 PPS in the 2x mode, R2 must equal 5,000 (1388 HEX)
4) Enter 273 for the accel/decel rate in R3 (from paragraph 6-1-2)
5) Obtain the value to use for R5 in the conditions stated above as follows.
   Enter the values in steps 1 to 4 in the ramping-down point formula,

$$R5 = \frac{(5000^2 - 500^2) \times 273}{300 \times 8192} = 2749.33 \quad 2749$$

6-3. Operating mode

In any operating mode, the motor will stop when an $\overline{EL}$ signal or $\overline{STP}$ signal of the same polarity as the direction of rotation turns ON. When high speed is selected and the $\overline{SD}$ signal is enabled, the motor will decelerate when an $\overline{SD}$ signal of the same polarity as the direction of rotation turns ON

The examples below use the following terms.

RGDT_H = Register upper byte address
RGDT_M = Register middle byte address
RGDT_L = Register lower byte address
COM_DT = Command buffer address

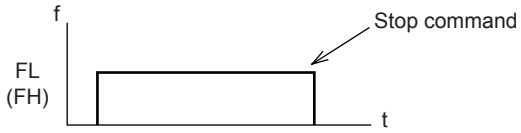
6-3-1. Continuous mode

This mode is used to keep a motor turning after it is started with a start command. The motor will keep turning until a stop command is received. Specify the direction of rotation using bit 3 in the control mode command.

To use this mode, set bit 2 (preset operation control) in the control mode command to "0". The preset counter will start counting pulses when the motor is started.

1) Constant speed continuous operation

When you want to drive a motor at FL (FH) speed using a pattern, as shown below, use the following procedure.

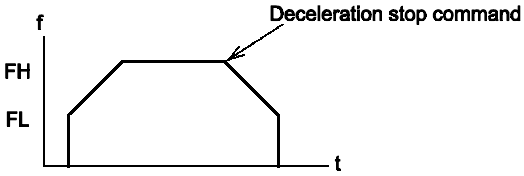



COM_DT <- 40 HEX  Control mode command (positive direction, continuous operation)
[To rotate in the opposite direction, use 48 HEX.]
COM_DT <- 10 HEX  Start command (FL constant speed start)
[Use 11 HEX when you want to start at an FH constant speed.]

To stop the motor, use an immediate stop command (08 HEX).
COM_DT <- 08 HEX  Start command (Immediate stop)

2) Continuous high speed operation

When you want to drive a motor at FH speed using a pattern, as shown below, use the following procedure.




The motor will start at FL speed and accelerate to FH speed.
It will decelerate when a deceleration stop command is received, and stop when it reaches FL speed.

COM_DT <- 40 HEX  Control mode command (positive direction, continuous operation)

[To rotate in the opposite direction, use 48 HEX.]
COM_DT <- 15 HEX  Start command (FH high speed start)

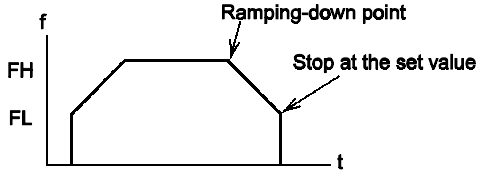
To stop the motor, use a deceleration stop command (1D HEX).
COM_DT <- 1D HEX  Start command (deceleration stop)

6-3-2. Preset mode

This mode is used to position the motor by assigning a specific number of pulses and a direction of rotation.
Specify the number of output pulses in the R0 preset counter. Then, start the motor. The motor will stop when the value in the preset counter reaches zero. Specify the direction of rotation in bit 3 in the control mode command.
The LSI will enter this mode when bit 2 in the control mode command is set to "1" (preset operation control). The preset counter decrements its contents (the number of pulses remaining). Therefore, specify a value for R0 for each positioning operation.
If R0 is set to 0, the motor will not start, even when a start command is given. However, if the $\overline{\text{INT}}$ signal is set to change state when the motor stops, an $\overline{\text{INT}}$ signal will be output even though the motor has done nothing.

1) High speed preset operation

To output a specific number of pulses at FH speed, follow the procedure below. We'll use a feed amount of 5,000 pulses (1388 HEX).




Start in FL speed and accelerate to FH speed. Decelerates at the ramping-down point and stops.

COM_DT <- 44 HEX  Control mode command (positive direction, preset operation)
[To rotate in the opposite direction, use 4C HEX.]
COM_DT <- 80 HEX  Register select command (Select R0)
RGDT_H <- 0 HEX  Preset data upper byte
RGDT_M <- 13 HEX  Preset data middle byte
RGDT_L <- 88 HEX  Preset data lower byte
* * * * * * * * * * <- Specify an R5 value, too.
COM_DT <- 15 HEX  Start command (FH high speed start)

To wait for completion of the preset operation, check bit 3 of Status0.

COM_DT -> READ  Read Status0 (check bit 3)
Bit 3 = 0: Stopped, 1: Running

6-3-3. Zero return mode

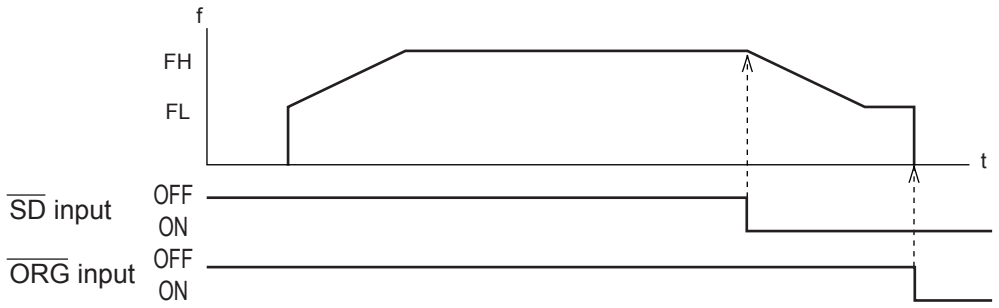
After starting the motor, when the zero position signal $\overline{ORG}$ turns ON, the motor will stop. Set the direction of rotation using bit 3 in the control mode command. This can be used together with the preset operation.

By placing a "1" in bit 0 ($\overline{ORG}$ signal control) of the control mode command, the LSI will enter this mode. The preset counter will count down from the starting value. By using the $\overline{SD}$ signal, the motor can execute a smooth zero return operation.

If the $\overline{ORG}$ terminal is LOW, the motor will not start, even if a start command is given. However, if the $\overline{INT}$ signal is set to change state when the motor stops, the $\overline{INT}$ signal will be output even though the motor has done nothing.

1) High speed zero return operation

To have the motor execute a zero return at FH speed, use the procedure below.




| | |
|---|---|
| COM_DT <- 43 HEX | Control mode command (positive direction, enable $\overline{ORG}$ and $\overline{SD}$ signal control)<br>[Use 4B HEX to rotate in the other direction.] |
| COM_DT <- 15 HEX | Start command (FH high speed) |

To wait for completion of the zero return, check bit 3 in Status0, the same as for the preset operation.

| | |
|---|---|
| COM_DT -> READ | Write Status0 (check bit 3)<br>Bit 3 = 0: Stopped1: Running |

6-3-4. Timer mode

Using the preset operation ($\overline{INT}$ signal when stopped) and pulse output control, this LSI can be used as a timer.

Stop the output of pulses and change the excitation signal using pulse output control. Specify a number of pulses in the preset counter R0. Then, start the LSI at constant speed using the preset operation. When the preset counter value reaches zero, the LSI will stop sending pulses and generate an interrupt signal.

(Specified time) = (Specified speed) x (Number of pulses specified)

Set bit 2 (preset operation control) in the control mode command to "1," and bit 1 (pulse output control) in the output mode command to "1". Then the LSI will enter this mode.

While in this mode, the LSI can be stopped by turning ON the $\overline{STP}$ signal, or by giving a stop

command. Please note that even if the $\overline{EL}$ signal or $\overline{ORG}$ signal is turned ON, the LSI will not stop outputting pulses.

1) Timer operation

To use the LSI as a 100ms timer, do the following.
Specify an FL speed of 1,000 PPS. A control time of 100ms is achieved by outputting 100 pulses at 1,000 PPS.

| | |
|---|---|
| COM_DT <- 44 HEX | Control mode command (preset operation) |
| COM_DT <- 0C2 HEX | Output mode command (pulse output stop) |
| COM_DT <- 80 HEX | R0 register select command |
| RGDT_H <- 0 HEX | Preset data upper byte (100 = 64 HEX) |
| RGDT_M <- 0 HEX | Preset data middle byte |
| RGDT_L <- 64 HEX | Preset data lower byte |
| COM_DT <- 30 HEX | Start command (FL start, output $\overline{INT}$ when stopped) |

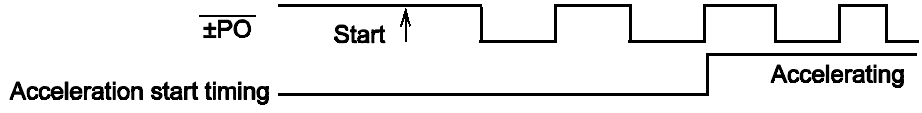
When an interrupt signal is input, the timer will time out (after 100 mS).

## 6-4. Control function

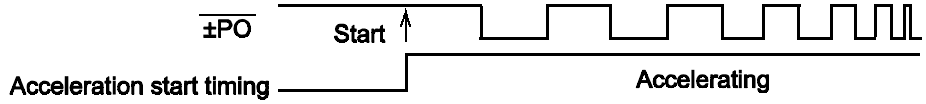
### 6-4-1. Idling pulse output

When the motor is started at FH high speed, the motor will accelerate right after starting. The idling pulse function enables the acceleration to start only after outputting some pulses at FL speed. If this function is not used, the speed calculated from the initial output pulse cycle will be higher than the FL speed, and the motor will not start automatically, even if the FL speed is set to approximately the auto start frequency.
To solve this problem, the LSI will start acceleration at the FL speed you set after 1 to 7 pulses. Then the motor will start automatically at nearly the auto start frequency. The pulses output at this FL speed are referred to as "idling pulses."
The allowable range is from 0 to 7, and this mode is available in high speed operation. When this is set to 0, the motor will start as normal.

For 2 idling pulses.




When the number of idling pulses is set to 0.

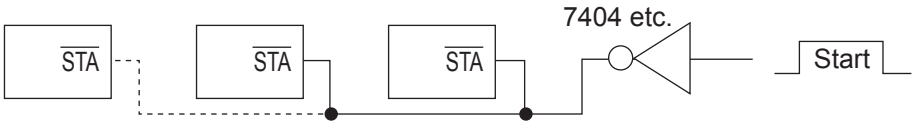



### 6-4-2. External start signal

This LSI can be started using an external signal. Using this function, multiple axes can be started simultaneously.

Delay the start command and when the LSI sees the leading edge of a LOW on the $\overline{STA}$ terminal, it will invoke the start command and the motor will start.
To delay the start command, make bit 1 of the start command "1." To end the delay, the immediate stop command can also be used.
The LSI cannot detect a $\overline{STA}$ signal shorter than 4 reference clock cycles.
While in the delayed start signal mode, if an $\overline{STP}$ or $\overline{EL}$ direction signal is input, the LSI will store the stop condition, and the LSI will not start operation, even if a $\overline{STA}$ signal is given again. By inputting these signals, the delayed start command is also cancelled and the motor will not start until the next start command is given.
By inputting an $\overline{STP}$ or $\overline{EL}$ signal while in the delayed mode, and then inputting a $\overline{STA}$ signal (or giving a start command), the start control bit in the start command in the extension monitor will change from "1" to "0."

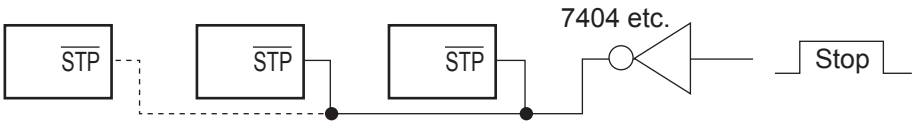
[An example of a simultaneous start using an external circuit]




6-4-3. External stop control

This LSI can be stopped instantly using an external signal. With this function, the motor can be stopped in an emergency and multiple axes can be stopped simultaneously.
Bringing the $\overline{STP}$ terminal LOW will stop the motor instantly.
While the $\overline{STP}$ terminal is LOW, the motor will not start, even if a start command is given.
However, when the $\overline{INT}$ output is enabled, the $\overline{INT}$ signal will be output after a start command is given.
The sensitivity of the $\overline{STP}$ signal input can be selected using bit 4 in the output mode command.

[Example of connections for a simultaneous stop using an external signal]




6-4-4. Excitation sequence output mask

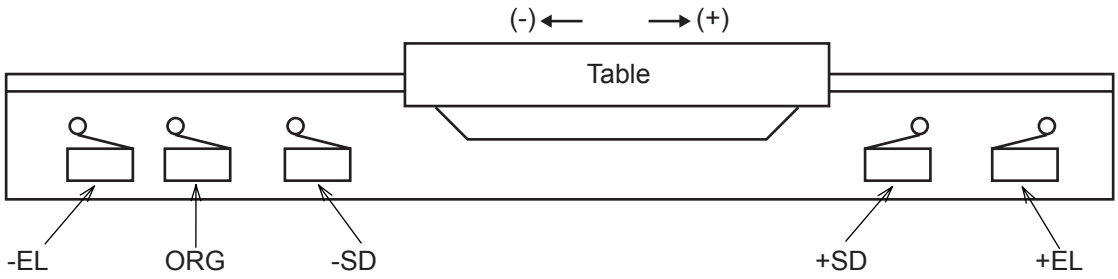
Outputs from $\phi$1 to $\phi$4 can be masked (make all of these outputs LOW).
Set bit 2 in the output mode command to "1", to enable masking.
This function is useful for turning OFF the excitation sequence when driving a unipolar system. (Some motor driving ICs cannot use a loss of excitation to control the motor. Contact the IC manufacturer.)

6-4-5. Pulse output logic

The pulse output logic of the $\pm\overline{PO}$ terminal can be selected.
Specify the logic using bit 0 in the output mode command.

6-4-6. External mechanical input control

The following five signals can be used as mechanical position detection signals.




1) $\overline{+EL}$, $\overline{-EL}$ signal

When an $\overline{EL}$ ON (LOW) signal with the same polarity as the motor direction is received, the motor will stop instantly. Even if the signal then goes back to HIGH, the motor will remain stopped. By enabling the $\overline{INT}$ signal, an $\overline{INT}$ signal will be output when the $\overline{EL}$ signal goes LOW.

When this signal is ON, the motor cannot be started in the same direction as the polarity of this signal, even if a start command is given. However, if the $\overline{INT}$ output is set to signal when stopped, an $\overline{INT}$ signal will be output.

When the output mode command pulse output control feature is used to stop the output of pulses, the $\overline{EL}$ signal is disabled. However, you can monitor the operation status using Status1.

The input sensitivity of this signal can be selected using bit 4 in the output mode command. When low sensitivity is selected, the LSI will not accept pulse signals less than 4 reference clock cycles long (approx. 800 nS with a 4.9152 MHz clock). When high sensitivity is selected, the LSI will detect pulse signals shorter than 800 nS. The input sensitivity setting is shared by the $\overline{ORG}$, $\overline{\pm EL}$, and $\overline{STP}$ signals.

2) $\overline{+SD}$, $\overline{-SD}$ signal

When $\overline{SD}$ signal control is enabled using the control mode command, and if an $\overline{SD}$ signal of the same polarity as the motor rotation is turned ON in high speed operation, the motor will start decelerating. If the $\overline{SD}$ signal goes OFF, the motor will accelerate again.

When the $\overline{SD}$ signal is enabled, giving a high speed start command while the $\overline{SD}$ signal is ON, the motor will not accelerate. It will operate at FL speed. When the $\overline{SD}$ signal changes while decelerating, the $\overline{SD}$ signal will be ignored.

Regardless of whether or not $\overline{SD}$ signal control is enabled in the control mode command, the LSI operating status can be monitored using Status1.

3) $\overline{ORG}$ signal

When $\overline{ORG}$ signal control is enabled (zero return operation) using the control mode command, and the $\overline{ORG}$ signal is turned ON the motor will stop instantly. After that, if the $\overline{ORG}$ signal goes OFF, the motor will remain stopped. By enabling the $\overline{INT}$ signal when stopped, an $\overline{INT}$ signal will be output when the $\overline{ORG}$ signal is turned ON.

If this signal is ON, the motor cannot be started even if a start command is given. However,

if the $\overline{INT}$ output is set to output when stopped, an $\overline{INT}$ signal will still be output when the signal is turned ON.
Regardless of whether or not $\overline{ORG}$ signal control is enabled in the control mode command, the LSI operating status can be monitored using Status1.
If pulse output is blocked by the pulse output control bit in the output mode command, the $\overline{ORG}$ signal is disabled. However, you can monitor the operating status using Status1.
The input sensitivity of this signal can also selected, the same as the $\overline{EL}$ signal.

6-4-7. Interrupt signal output

This LSI can output an $\overline{INT}$ signal when stopped, when the ramping-down point is reached, or when an external start signal is received.
To output an interrupt signal when stopped, use bit 5 in the start mode command.
To output an interrupt signal when the ramping-down point is reached, use bit 4 in the register select command.
To output an interrupt signal when an external start signal is received, assign bit 5 in the register select command.
By setting the interrupt control bit to "1," an $\overline{INT}$ signal will be output for each situation that is selected. To reset the $\overline{INT}$ signal, place a "0" in the respective bit. When you want to mask without using the $\overline{INT}$ signal, you should also set this bit to "0."
The $\overline{INT}$ terminal output is a logical OR of the stopped, ramping-down point, and external start conditions. To determine which condition caused the $\overline{INT}$ signal to be output, check Status0.
When using more than one LSI, each of the $\overline{INT}$ terminals can be connected in a wire OR configuration. However, in this case, connect an external pull up resistor (5K to 10K ohms).

1) How to use the $\overline{INT}$ signal with a ramping-down point

The LSI will output an $\overline{INT}$ signal when the ramping-down point is reached as follows: The preset counter (PC) value is compared to the ramping-down point value in register R5. When PC $\leqq$ R5, the LSI will output an $\overline{INT}$ signal. In addition, when the LSI is operating in preset, high speed operation, the LSI will start deceleration of the motor when PC $\leqq$ R5. Therefore, the interrupt generated when the ramping-down point is reached can be used as a comparator of the remaining pulses when the motor is in preset operation at a constant speed.
Another way to use this feature is when you want a positioning operation that will exceed the maximum value (24 bit) allowed for the PC value. Enter the remainder into R0 (after subtracting the maximum value for the PC), and set R5 to "0" to select continuous operation. Then, after the interrupt has occurred, and when PC $\neq$ 0 (Status0), change to preset operation. This makes it possible to control positions that exceed the maximum value allowed.

6-5. Command buffer

In order to operate this LSI, you must write data into the command buffer and each of the registers through an 8-bit data bus.
There are four command groups, which are invoked by setting the upper two bits of the byte. A command buffer is used to latch the command details until another command in the same group is written.
Since each command has individual functions identified by the individual bits, settings other than the examples shown to the right are also possible.
When a start command is written into the command buffer, the LSI will start its operation. Therefore, the start mode command should be the last command given. There is no other restriction on the order in which commands can be written.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C1 | C0 | | | | | | |

| C1 | C0 | Command group |
|---|---|---|
| 0 | 0 | Start mode |
| 0 | 1 | Control mode |
| 1 | 0 | Select register |
| 1 | 1 | Output mode |

6-5-1. Start mode command

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | | | | | | |

Speed selection: 0= FL speed, 1= FH speed
External start control:
0 = Does not inhibit a start
1 = Inhibit the start
Speed mode: 0 = Constant speed, 1 = High speed
Stop control: 0= OFF, 1 = ON
Start control: 0= OFF, 1 = ON
$\overline{INT}$ output when stopped
0 = Interrupt is not output ($\overline{INT}$ reset)
1 = Interrupt is output

Speed selection
[Select the operation speed by setting this bit.]
When this bit is 0, the value in register R1 (FL speed setting) is used as the operation speed.
When this bit is set to 1, the value in register R2 (FH speed setting) is used as the operation speed.

External start control
[By setting this bit, the operation start can be inhibited.]
When a start command is written to the command buffer with this bit set to 1, the LSI will

remain stopped. Then, when the $\overline{STA}$ terminal changes to LOW, the inhibit is released, and the LSI will start operation. When a start command is written to the command buffer with this bit set to 0, the LSI will start operation immediately.

Speed mode

[The speed mode is selected by setting this bit.]

Setting this bit to 0 will operate a stepper motor at a constant speed. The LSI operates at a constant speed according to the speed set with the speed selection bit (bit 0).
When the constant speed mode is selected, the $\pm\overline{SD}$ signals and the ramping-down point setting in R5 are ignored.
Setting this bit to 1 will enable accel/decel speed control (in high-speed operation).
When this mode is selected, the $\pm\overline{SD}$ signals, the idling pulse setting in R6 and the ramping-down point setting, all made using preset operations, will be enabled. This mode is used when the motor will be operated at a speed higher than the start speed.

Start/stop control

[Set these bits to control starting and stopping.]

Set the start control bit to 1 to start operation, and set the stop bit to 1 to stop the operation. By combining both bits, you can invoke a deceleration stop.
When read with a monitor, the start control bit will change to 0 when stopping.

$\overline{INT}$ output when stopped

[Setting this bit to 1 will output an $\overline{INT}$ signal when the operation is stopped.]

Setting this bit to 1 will output an $\overline{INT}$ signal when the motor is stopped in a preset operation, or when it is stopped using $\pm\overline{EL}$, $\overline{STP}$, and $\overline{ORG}$ signals or a stop command.
To reset the $\overline{INT}$ signal, set this bit to 0. To mask the $\overline{INT}$ signal, leave this bit set to 0.

The $\overline{INT}$ terminal output is the result of logically ORing this signal with the interrupt signal for the ramping-down point, and the interrupt signal when started externally, and the interrupt signal for starting from an external signal. To determine which source has caused the $\overline{INT}$ signal to be output, check Status0.

[Start command/stop command]

When using the start mode command, a command to start operation is referred to as a start command and a command to stop operation is referred to as a stop command.

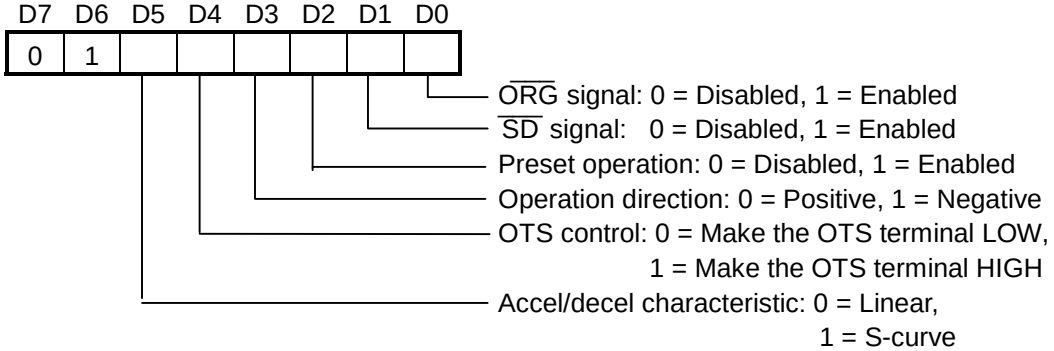
[Constant operation/high speed operation (constant speed start/high speed start)]

- Constant speed operation (constant speed start)
  Starting with the speed mode bit set to 0 is referred to as a constant speed start.
- High speed operation (high speed start)
  Starting with the speed mode bit set to 1 is referred to as a high-speed start.

Start mode command examples (X's in the table mean the value can be 0 or 1)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | Operation details |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | FL constant speed start (No $\overline{INT}$ output when stopped)<br>Operate at FL speed (speed specified in R1).<br>When starting, change to the FL speed immediately. |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30 | FL constant speed start (Output an $\overline{INT}$ when stopped) |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12 | Inhibit the FL constant speed start (no $\overline{INT}$ output when stopped) |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 32 | Inhibit the FL constant speed start (Output an $\overline{INT}$ when stopped) |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11 | FH constant speed start<br>Operate at FH speed (speed given in R2).<br>When starting, change to the FH speed immediately. |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13 | Inhibit the FL constant speed start |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 15 | FH high speed start<br>Operate from FL speed to the FH speed.<br>When operating, accelerate to the FH speed. |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 17 | Inhibit the FH high speed start. |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 14 | Decelerate during operation<br>Decelerate from the FH speed to the FL speed. |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1D | Deceleration stop (No $\overline{INT}$ output when stopped)<br>Decelerate from the FH speed to the FL speed and then stop. |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 3D | Deceleration stop (Output an $\overline{INT}$ when stopped) |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 08 | Immediate stop (No $\overline{INT}$ output when stopped) |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 28 | Immediate stop (Output an $\overline{INT}$ when stopped) |
| 0 | 0 | X | 1 | 1 | X | 1 | X | | Prohibited setting |

6-5-2. Control mode command




[Continuous operation/preset operation/zero return operation]

- Continuous operation

Operation when the preset stop control bit is set to 0.

- Preset operation
  Operation when the preset stop control bit is set to 1.

- Zero return operation
  Operation when the $\overline{ORG}$ signal control bit is set to 1.

$\overline{ORG}$ signal control

[This bit is used to enable or disable stopping with the $\overline{ORG}$ signal.]

When this bit is 1 and the $\overline{ORG}$ terminal is brought LOW while in operation, the output pulses are stopped immediately. Use this control for zero return operation.

When this bit is 0, the clock will continue to supply pulses, even if the $\overline{ORG}$ terminal is brought LOW. The setting of this bit does not affect the LSI status.

$\overline{SD}$ signal control

[This bit is used to enable or disable deceleration that can be triggered by the $\pm\overline{SD}$ signal.]

When this bit is 1 and the $\overline{SD}$ terminal with the same polarity as the rotation direction is brought LOW while in FH high speed operation, the output pulses will decelerate and then operation will continue at FL speed as long as the $\overline{SD}$ terminal remains LOW.

This is used to reduce mechanical shock when stopping in a zero return operation or when using $\pm\overline{EL}$ signals.

When this bit is 0, the LSI will continue FH high-speed operation and will not decelerate, even if $\pm\overline{SD}$ terminals go LOW.

The setting of this bit does not affect the LSI status.

Preset operation

[The setting on this bit is used to enable or disable a stop caused by the preset counter (24-bit) value (previously set in register R1) dropping to 0.]

Set this bit to 1, enter a value into the preset counter, and start operation. The preset counter will decrement by one with each pulse that is output and the LSI will stop operation when the counter reaches 0.

Set this bit to 0, and the operation will not stop even when the preset counter reaches 0.

Operation will not stop until an $\pm\overline{EL}$, $\overline{STP}$, $\overline{ORG}$ signal or a stop command is input.

Operation direction

[The setting of this bit controls the direction of the output pulses.]

When this bit is 1, the LSI will output pulses from the $+\overline{PO}$ terminal, and the excitation signal will change to positive.

When this bit is 0, the LSI will output pulses from the $-\overline{PO}$ terminal, and the excitation signal will change to negative.

The setting of this bit affects the direction of the $\pm\overline{EL}$ and $\pm\overline{SD}$ terminals.

OTS control

[This bit is used to control a general purpose OTS output.]

When this bit is 1, the OTS terminal will be HIGH. When it is 0, the OTS terminal will be LOW.

This terminal can be used to turn a motor driver excitation IC ON and OFF, and control the

current when stopped.

Accel/decel characteristic

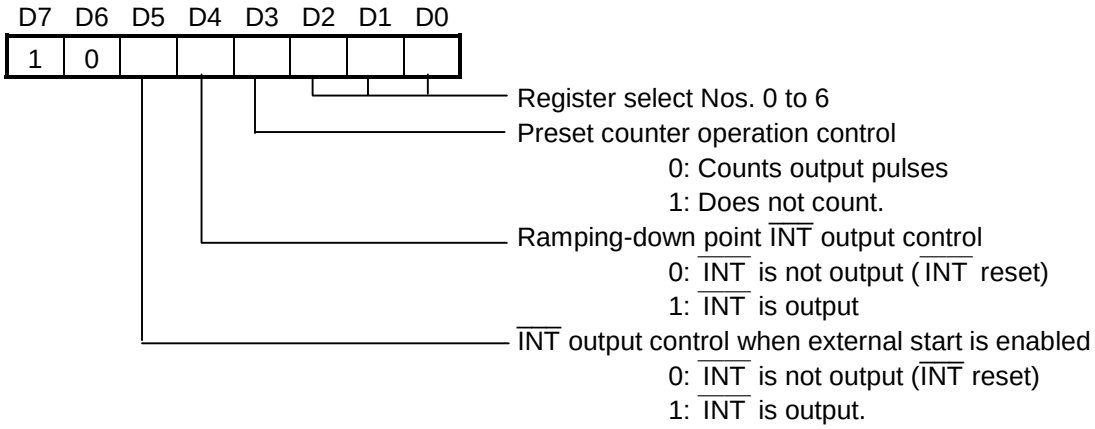
[This bit is used to select a linear or S-curve acceleration/deceleration pattern.]

Set this bit to 1 to select the S-curve accel/decel pattern (quadratic curve). Set this bit to 0 to select a linear accel/decel pattern.

Control mode command examples (X's in the table mean the value can be 0 or 1)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation details |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | X | X | X | X | X | 0 | Will not stop when the $\overline{ORG}$ terminal goes LOW. |
| 0 | 1 | X | X | X | X | X | 1 | Stops when the $\overline{ORG}$ terminal goes LOW. |
| 0 | 1 | X | X | X | X | 0 | X | Does not decelerate when the $\overline{SD}$ terminal goes LOW. |
| 0 | 1 | X | X | X | X | 1 | X | Decelerates when the $\overline{SD}$ terminal goes LOW. (In high speed operation.) |
| 0 | 1 | X | X | X | 0 | X | X | Does not stop when the preset counter reaches 0. |
| 0 | 1 | X | X | X | 1 | X | X | Stops when the preset counter reaches 0. |
| 0 | 1 | X | X | 0 | X | X | X | Runs in the positive direction. |
| 0 | 1 | X | X | 1 | X | X | X | Runs in the negative direction |
| 0 | 1 | X | 0 | X | X | X | X | OTS is LOW. |
| 0 | 1 | X | 1 | X | X | X | X | OTS is HIGH. |
| 0 | 1 | 0 | X | X | X | X | X | Linear accel/decel. |
| 0 | 1 | 1 | X | X | X | X | X | S-curve accel/decel. |
| 0 | 1 | X | X | X | 0 | 0 | 0 | Continuous operation. |
| 0 | 1 | X | X | X | 0 | X | 1 | Zero return operation. |
| 0 | 1 | X | X | X | 1 | 0 | 0 | Preset operation. |

6-5-3. Register select command




Register select No.

[Select the register to control by setting these bits.]

To write or read data in registers R0 to R6, the target register must be specified first by using the register select command.

Specify the target register using bits D2, D1, and D0.

| D2 | D1 | D0 | R No. | R/W | Detail | Bit length | Setting range |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | R0 | R/W | Preset counter data | 24 | 0 to 16,777,215 (FFFFFF) |
| 0 | 0 | 1 | R1 | W (R) | Set FL speed | 13 | 1 to 8,191 (1FFF) |
| 0 | 1 | 0 | R2 | W (R) | Set FH speed | 13 | 1 to 8, 191 (1FFF) |
| 0 | 1 | 1 | R3 | W (R) | Accel/decel rate | 10 | 2 to 1, 023 (3FF) |
| 1 | 0 | 0 | R4 | W (R) | Set magnification | 10 | 2 to 1, 023 (3FF) |
| 1 | 0 | 1 | R5 | W (R) | Set ramping-down point | 16 | 0 to 65, 535 (FFFF) |
| 1 | 1 | 0 | R6 | W (R) | Set idling pulse | 3 | 0 to 7 |
| 1 | 1 | 1 | R7 | W (R) | Set preference data (PCD4541 only) | 1 | 0 to (1) |

* R/W: Read/Write register

W(R): Write only register. However, it can be read using the extension monitor setting.

To read the preset counter value, first specify R0, and then read the data. By reading the select command, the buffer data available for reading is refreshed. To read data continuously, you have to write an R0 select command, for each read operation.

To write to R0 to R6, write the lower byte data (bits 0 to 7) last.

Preset counter operation control

[Setting this bit controls the operation of the preset counter.]

When this bit is 1, the preset counter will stop counting.

When this bit is 0, the preset counter will decrement by one for each pulse output.

Ramping-down point $\overline{INT}$ output control

[This bit controls whether or not the $\overline{INT}$ signal is output when the ramping-down point is reached.]

When this bit is 1 and the preset counter value becomes smaller than the ramping-down point setting in R5, the LSI will output an $\overline{INT}$ signal.

To reset the $\overline{INT}$ signal, set this bit to 0. If you want to mask this operation, leave this bit set to 0.

The $\overline{INT}$ terminal output is the result of logically ORing this signal with the interrupt signal when stopped, and the interrupt signal when started externally. To determine which source has caused the $\overline{INT}$ signal to be output, check Status0.

External start $\overline{INT}$ output control

[An $\overline{INT}$ signal can be output during an external start.]

When this bit is 1 and the start is inhibited, if the LSI is started using an external $\overline{STA}$ signal, the LSI will output an $\overline{INT}$ signal.

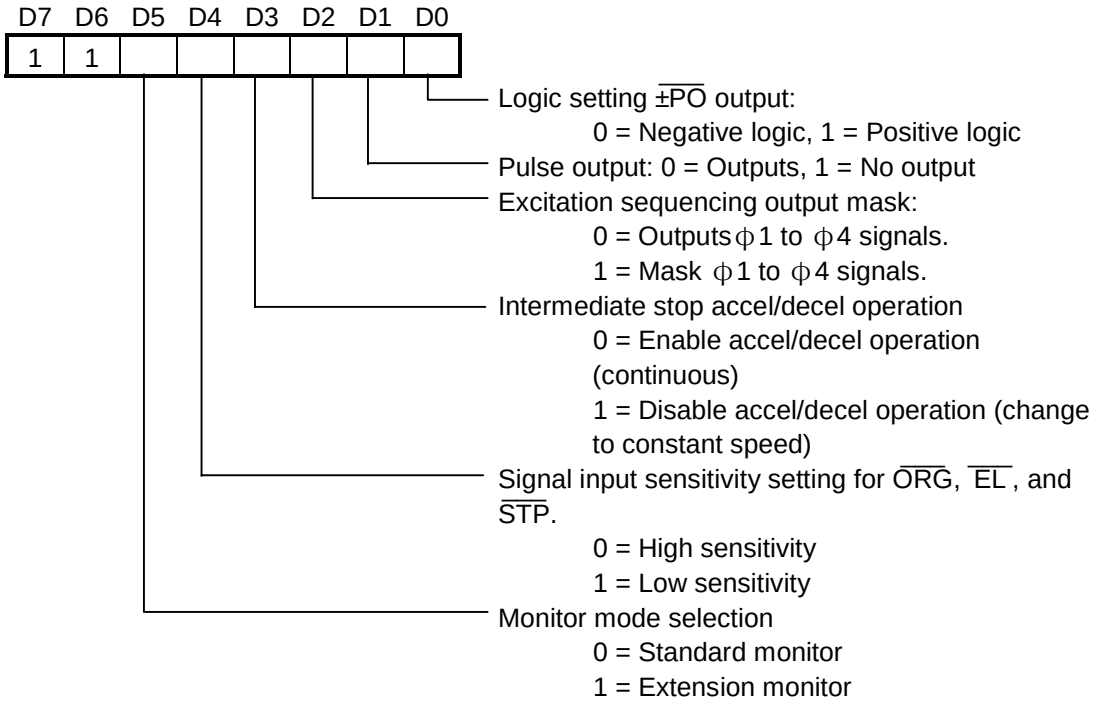
To reset the $\overline{INT}$ signal, set this bit to 0. When you do not want use this $\overline{INT}$ signal and want to mask it, leave this bit set to 0.

The $\overline{INT}$ terminal output is the result of logically ORing this signal with the interrupt signal for the ramping-down point, and the interrupt signal when stopped. To determine which source has caused the $\overline{INT}$ signal to be output, check Status0.

Register select command examples (X's in the table mean the value can be 0 or 1).

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation details |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | X | X | X | 0 | 0 | 0 | Selects R0. |
| 1 | 0 | X | X | X | 0 | 0 | 1 | Selects R1. |
| 1 | 0 | X | X | X | 0 | 1 | 0 | Selects R2. |
| 1 | 0 | X | X | X | 0 | 1 | 1 | Selects R3. |
| 1 | 0 | X | X | X | 1 | 0 | 0 | Selects R4. |
| 1 | 0 | X | X | X | 1 | 0 | 1 | Selects R5. |
| 1 | 0 | X | X | X | 1 | 1 | 0 | Selects R6. |
| 1 | 0 | X | X | X | 1 | 1 | 1 | Selects R7. |
| 1 | 0 | X | X | 0 | X | X | X | Count pulses using the preset counter. |
| 1 | 0 | X | X | 1 | X | X | X | Stop counting pulses. |
| 1 | 0 | X | 0 | X | X | X | X | Do not output an $\overline{INT}$ signal at the ramping-down point. |
| 1 | 0 | X | 1 | X | X | X | X | Output an $\overline{INT}$ signal at the ramping-down point. |
| 1 | 0 | 0 | X | X | X | X | X | Do not output an $\overline{INT}$ signal when started by an external signal. |
| 1 | 0 | 1 | X | X | X | X | X | Output an $\overline{INT}$ signal when started by an external signal. |

6-5-4. Output mode command




Logic setting for the ±PO output

[By setting this bit, you can change output logic on the ±PO terminal.]

Set this bit to 1 to select positive logic. Set this bit to 0 to select negative logic. For pulse output patterns, see the table below.

| Direction | 0: Negative logic | | 1: Positive logic | |
|---|---|---|---|---|
| | +PO | -PO | +PO | -PO |
| (+) |  | H |  | L |
| (-) | H |  | L |  |

Pulse output

[The pulse output from the ±PO terminal is enabled or disabled with this bit.]

When this bit is 1 no pulse will be output on the ±PO terminals, no changes will occur in the excitation signal, and stops triggered by the +EL and ORG signal inputs will be disabled. Other operations are not affected. Since the LSI can be configured to output an INT signal when stopped while in constant speed preset operation, and the INT signal will be output after a set time (preset number of pulses divided by the output pulse speed) has elapsed, it can be used as a timer.

When this bit is 0 the LSI is in normal operation and pulses are output on the ±PO lines.

The setting of this bit does not affect the status of the LSI.

Excitation sequencing output mask

[The excitation sequencing output can be masked with this bit.]

When this bit is 1 all the excitation sequences from $\phi$1 to $\phi$4 will be held LOW.

This function can be used to turn excitation OFF when driving a unipolar driver. (This function cannot be used with some models of motor driver ICs. Contact the manufacturer for details.)

Intermediate stop in an accel/decel operation

[The operation speed can be locked in the middle of an acceleration/deceleration using this bit.]

If this bit is set to 1 while accelerating or decelerating, the LSI will stop the acceleration/deceleration and hold the current speed. After that, if this bit is set to 0, the LSI will restart the acceleration or deceleration.

Signal input sensitivity for the $\overline{ORG}$, $\overline{EL}$, and $\overline{STP}$ signals

[The sensitivity to signals on the $\overline{ORG}$, $\pm\overline{EL}$, and $\overline{STP}$ terminals can be set using this bit.]

Set this bit to 1 to reduce the sensitivity to signals on the $\overline{ORG}$, $\pm\overline{EL}$, and $\overline{STP}$ terminals. Pulse signals shorter than 4 reference clock cycles (approx. 800 nS with a 4.9152 MHz clock) will be ignored.

Set this bit to 0 and the sensitivity is increased. Pulse signals shorter than 800 nS will be recognized.

Monitor mode selection

[The data types that can be read can be set with this bit.]

Set this bit to 1 to read data such as R0 to R7, Status0, Status1, Status2, Status3, commands, and the current speed.

Set this bit to 0 and the LSI will be compatible with the PCD4500 (previous series). As such, it can only read R0, Status0, and Status1.

Output mode command examples (X's in the table mean the value can be 0 or 1).

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation details |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | X | X | X | X | X | 0 | Makes the $\pm\overline{PO}$ lines use negative logic. |
| 1 | 1 | X | X | X | X | X | 1 | Makes the $\pm\overline{PO}$ lines use positive logic. |
| 1 | 1 | X | X | X | X | 0 | X | Outputs pulses on the $\pm\overline{PO}$ lines. |
| 1 | 1 | X | X | X | X | 1 | X | Do not output pulses on the $\pm\overline{PO}$ lines. |
| 1 | 1 | X | X | X | 0 | X | X | Output excitation signals from $\phi$1 to $\phi$4. |
| 1 | 1 | X | X | X | 1 | X | X | Mask excitation signals from $\phi$1 to $\phi$4. |
| 1 | 1 | X | X | 0 | X | X | X | Acceleration/deceleration enabled. |
| 1 | 1 | X | X | 1 | X | X | X | Stop acceleration/deceleration in mid-stream. |
| 1 | 1 | X | 0 | X | X | X | X | High sensitivity to $\overline{ORG}$, $\overline{EL}$, and $\overline{STP}$ signals. |
| 1 | 1 | X | 1 | X | X | X | X | Low sensitivity to $\overline{ORG}$, $\overline{EL}$, and $\overline{STP}$ signals. |
| 1 | 1 | 0 | X | X | X | X | X | Standard monitor setting. |
| 1 | 1 | 1 | X | X | X | X | X | Extension monitor setting. |

6-6. Registers

To write data into registers R0 to R7, first select the target register using the register select command. Write the lower byte of data last. For details about the settings for each register to achieve a certain speed, see "6-2. Speed pattern setting."

6-6-1. R0 preset pulse counter (24 bits)

This LSI has an internal preset countdown counter. By entering a number of pulses, this preset counter will begin counting down from that point.

The preset counter decrements by one for one pulse output in the continuous, zero return, and preset operations. However, if the preset counter operation mode is inhibited by the output mode command, the preset counter will not count down.

The counter value (number of remaining pulses) can be read while in operation or while stopped. To read the value, first select R0. The register select timing latches the data into a 24-bit read buffer.

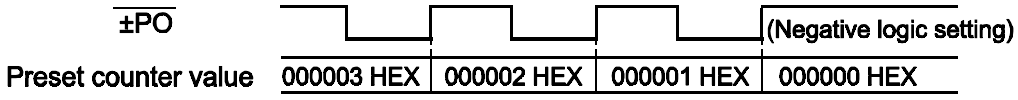
In preset operation, the LSI places a number of positioning pulses in this register, and then starts the operation. Once the LSI has started, the counter value is decremented with each pulse that is output. When the number of pulses that have been output is equal to the value originally entered in the preset counter, the value in the counter will be zero and the LSI will stop operation.

The allowable range is 0 to 16,777,215 (FFFFFF HEX).

If you enter 0 in the preset counter and write the start command, the LSI will not use the preset operation. The operation flag in Status0 and the $\overline{BSY}$ output signal would both immediately indicate that the LSI had stopped. When $\overline{INT}$ output is enabled, the LSI will output an $\overline{INT}$ signal.

If you stop the preset operation using the stop command or an external signal, the number of remaining pulses will be saved in the preset counter. By entering a new start command, the LSI will continue to output all of the remaining pulses.

After the preset number of pulses has been output, the value in the preset counter will be 0. If you want to restart the operation using the same number of pulses, you will have to put the value in R0 again.




6-6-2. R1: FL speed register (13 bits)

This register is used to set the FL speed. To operate at high speed, the LSI will start with the FL speed and then accelerate to the FH speed. When a deceleration stop command is entered while in high-speed operation, the LSI will decelerate. When the speed drops to the FL speed, the operation will stop.

If the FL speed is set to 0, the $\overline{\pm PO}$ is latched LOW when stopped and the motor may not actually stop. Make sure to set the FL speed to a number greater than 1.

The allowable range is 1 to 8,191 (1FFF HEX).

The relationship between the value entered and the output pulse speed varies with the value placed in R4 (magnification).

6-6-3. R2: FH speed register (13 bits)

This register is used to set the FH speed.
The allowable range is 1 to 8,191 (1FFF HEX).
The relationship between the value entered and the output pulse speed varies with the value placed in R4 (magnification).

6-6-4. R3: Accel/decel rate register (10 bits)

This register is used to select the acceleration and deceleration characteristics.
When the LSI executes a high-speed start, the motor starts at the FL speed entered in R1, and accelerates to the FH speed entered in R2.
Then, the motor decelerates to the FL speed when an $\overline{SD}$ signal is received, the ramping-down point is reached, or a deceleration command is received. Specify the acceleration and deceleration characteristics for these operating patterns using the accel/decel rate setting register. The acceleration rate of the linear accel/decel is equal to the maximum acceleration rate of the S-curve acceleration/deceleration pattern.
The allowable range is: 2 to 1,023 (3FF HEX)

6-6-5. R4: Magnification register (10 bits)

The speed setting registers R1 and R2 can have values from 1 to 8,191. The relationship between the values entered and the output pulse speed can be set using this magnification register.
The allowable range is 2 to 1,023 (3FF HEX).
The shorter this value, the higher the output clock speed.

6-6-6. R5: Ramping-down point register (16 bits)

While in preset, high-speed operation, the LSI compares the value in this register, R5, to the value in the preset counter. When the value in R5 is larger than the preset counter value, the LSI will start to decelerate.
If the value placed in R5 is smaller than the preset counter value and the LSI is programmed for preset, high-speed operation, the motor will operate at FL speed and not accelerate.
The FL speed, FH speed, and the accel/decel rate determine the ramping-down point.
Entering inappropriate values may stop the output of pulses during deceleration, or cause the LSI to operate longer at the FL speed after deceleration.
The allowable range is 0 to 65,535 (FFFF HEX)

6-6-7. R6: Idling pulse register (3-bit)

To operate at high speed, the motor is accelerated quickly after starting. Therefore, the speed calculated from the output pulse frequency will be higher than the FL speed that is set. If FL is set to a value lower than the self-start frequency, the motor will not start. Therefore, in order to be able to start from near the self-start frequency, the acceleration using the FL speed can be started from 1 to 7 pulses after the start command. The pulses that the start is delayed by are referred to as idling pulses.
The allowable range is 0 to 7. This is effective in high-speed operation. Setting this register to 0 will provide a normal start.

6-6-8. R7: Environmental data register (1-bit)

This register can only be set on the PCD4541.

When this register is 1, the ±$\overline{PO}$ pulse output changes from outputting ±2 pulses to the directory mode (pulse output plus direction signal output). In this mode, the LSI outputs pulses on the $\overline{+PO}$ terminal and the direction signal on the $\overline{-PO}$ terminal.

The direction signal will go HIGH while turning in the positive direction, and LOW while turning in the negative direction (when negative logic is selected).

6-7. Status

- Both Status0 (monitor current operation status) and Status1 (input status of $\overline{\pm EL}$, $\overline{\pm SD}$, $\overline{ORG}$, $\overline{STA}$, and $\overline{STP}$ signals) are available.
- When the extension monitor is selected for the monitor mode using the output mode command, Status2 (monitor output status of the $\overline{\pm PO}$, $\phi$1 to 4, $\overline{INT}$, and $\overline{OTS}$ signals) and Status3 (identify the PCD series model) are also available.
- Status0 does not have any restrictions on reading. Since Status1, Status2, and Status3 share their addresses with the lower data byte of the preset counter, there is a restriction on reading from them.

  To read Status1, Status2, or Status3, first select the R7 register (or a register other than R0 in the normal monitor mode). Then you can read Status1 from the lower data byte, Status2 from the middle data byte, and Status3 from the upper data byte.
- Status0 to 4 are latched while reading. The data bus will not change while in the read cycle.
- After operation has stopped, if the start mode command is read with the extension monitor, the start control mode bit will be 0.
- When reading using the register select command, the register selection is limited to R3 only.

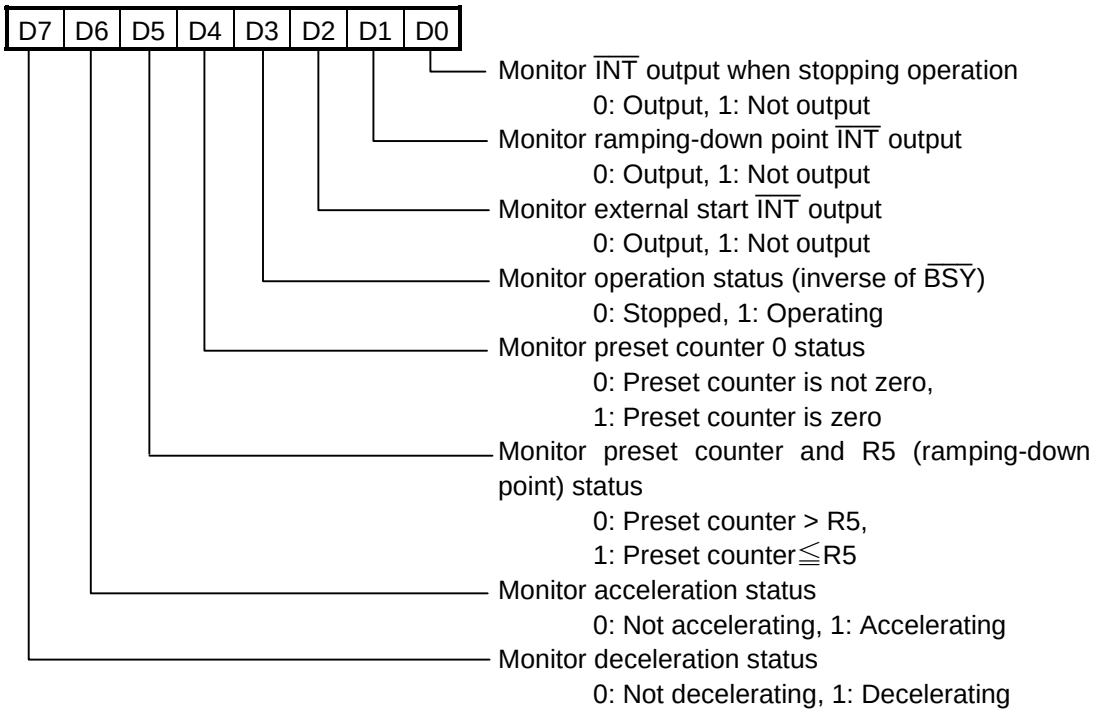
When the standard monitor is selected

| Address / Register | A1 = 0, A0 = 0 | A1 = 0, A0 = 1 | A1 = 1, A0 = 0 | A1 = 1, A0 = 1 |
|---|---|---|---|---|
| R0 | Status0 | R0 lower data | R0 middle data | R0 upper data |
| R1 to R7 | Status0 | Status1 | 0 | 0 |

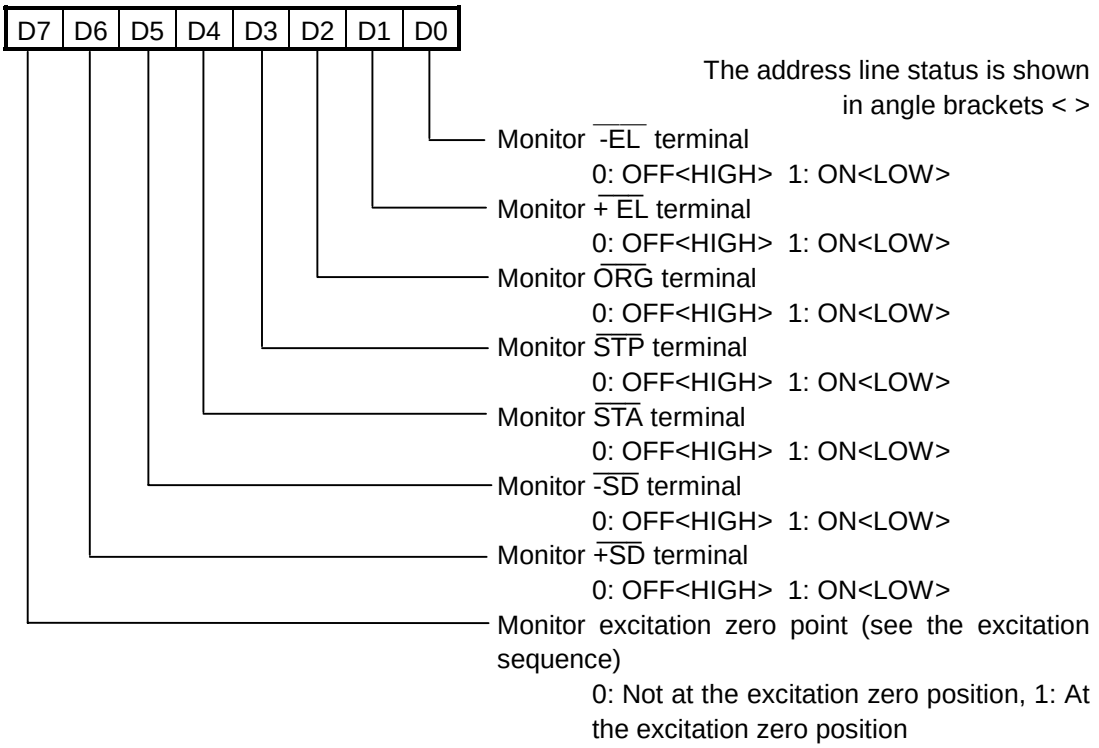
When the extension monitor is selected

| Address / Register | A1 = 0, A0 = 0 | A1 = 0, A0 = 1 | A1 = 1, A0 = 0 | A1 = 1, A0 = 1 |
|---|---|---|---|---|
| R0 | Status0 | R0 lower data | R0 middle data | R0 upper data |
| R1 | Status0 | R1 lower data | R1 upper data | Start mode command |
| R2 | Status0 | R2 lower data | R2 upper data | Control mode command |
| R3 | Status0 | R3 lower data | R3 upper data | Register select command |
| R4 | Status0 | R4 lower data | R4 upper data | Output mode command |
| R5 | Status0 | R5 lower data | R5 upper data | R7 data |
| R6 | Status0 | R6 data | Speed lower data | Speed upper data |
| R7 | Status0 | Status1 | Status2 | Status3 |

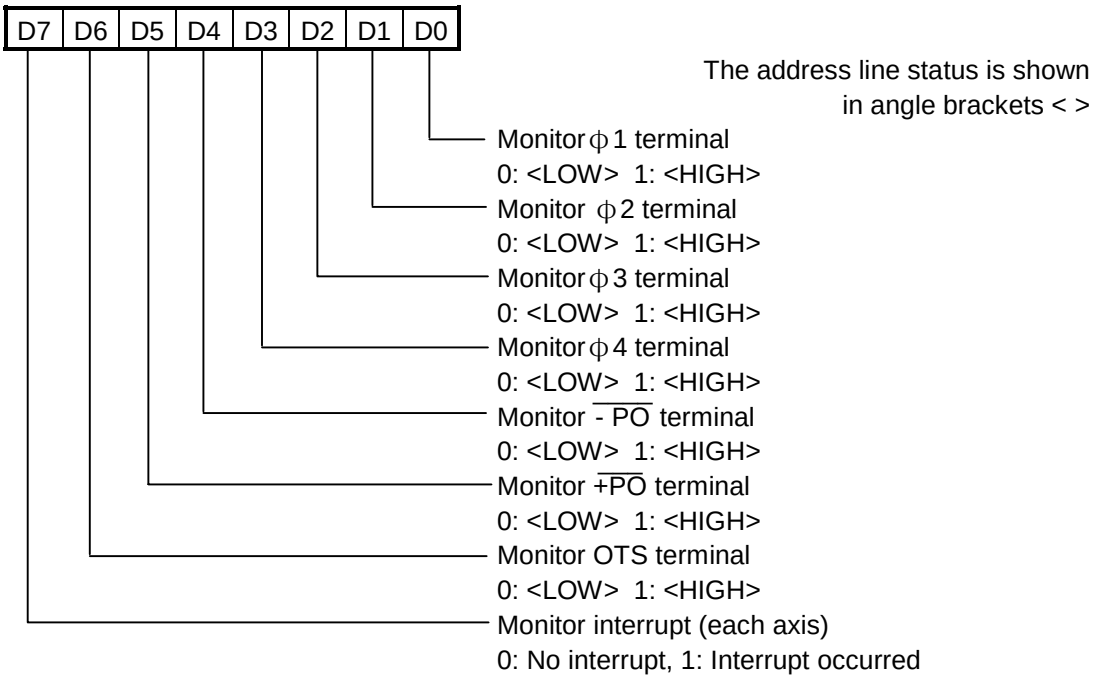
6-7-1. Status0 (address lines: A1 = 0, A0 = 0)



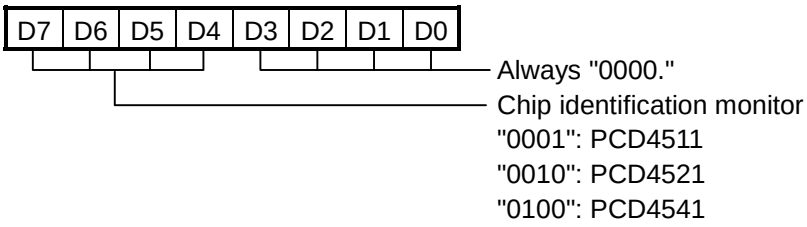
6-7-2. Status1 (Address lines: A1 = 0, A0 = 1)




6-7-3. Status2 (Terminal: A1 = 1, A0 = 0)

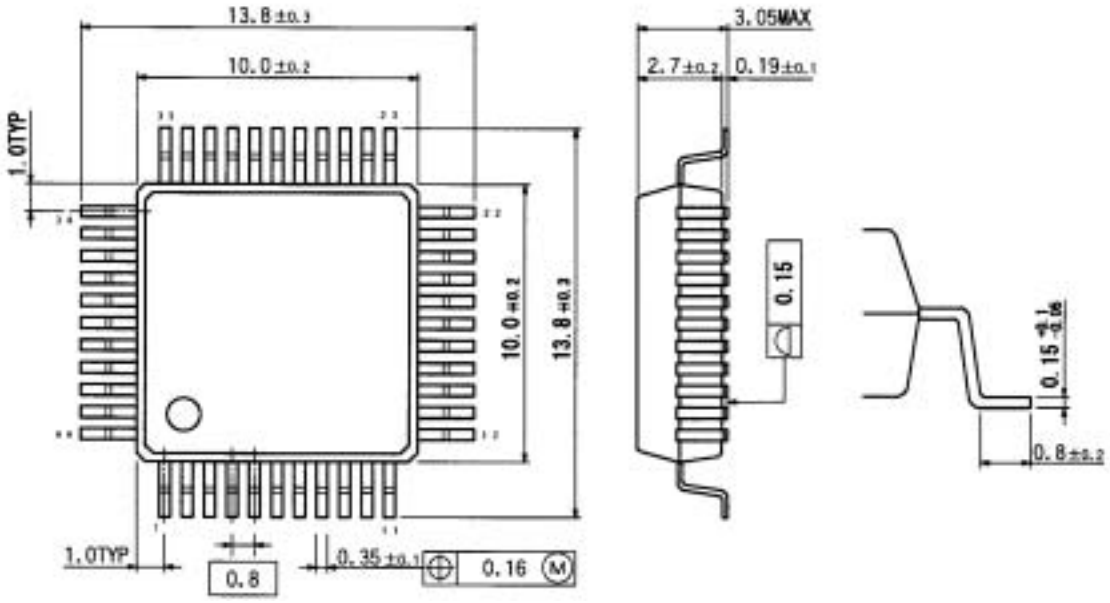


6-7-4. Status3 (Terminal: A1 = 1, A0 = 1)



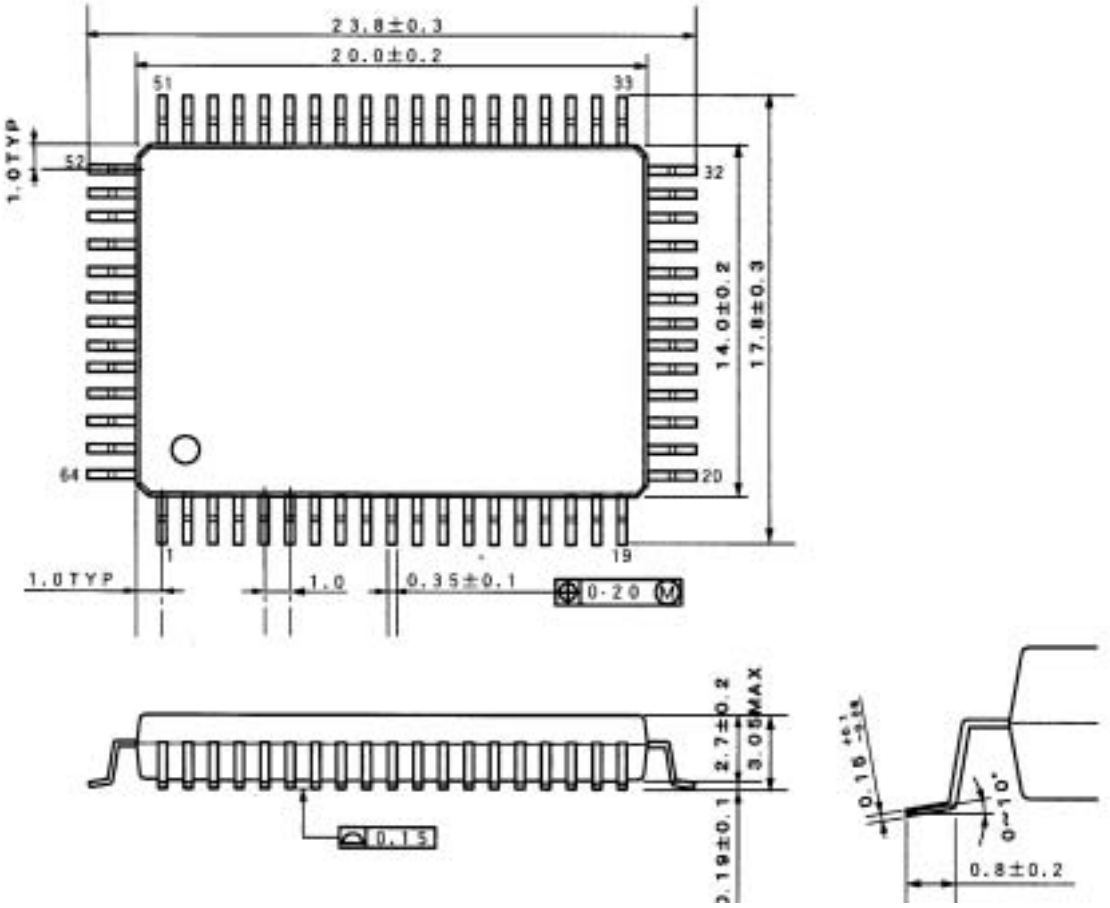
## 7. External dimensions

7-1. External dimensions of the PCD4511



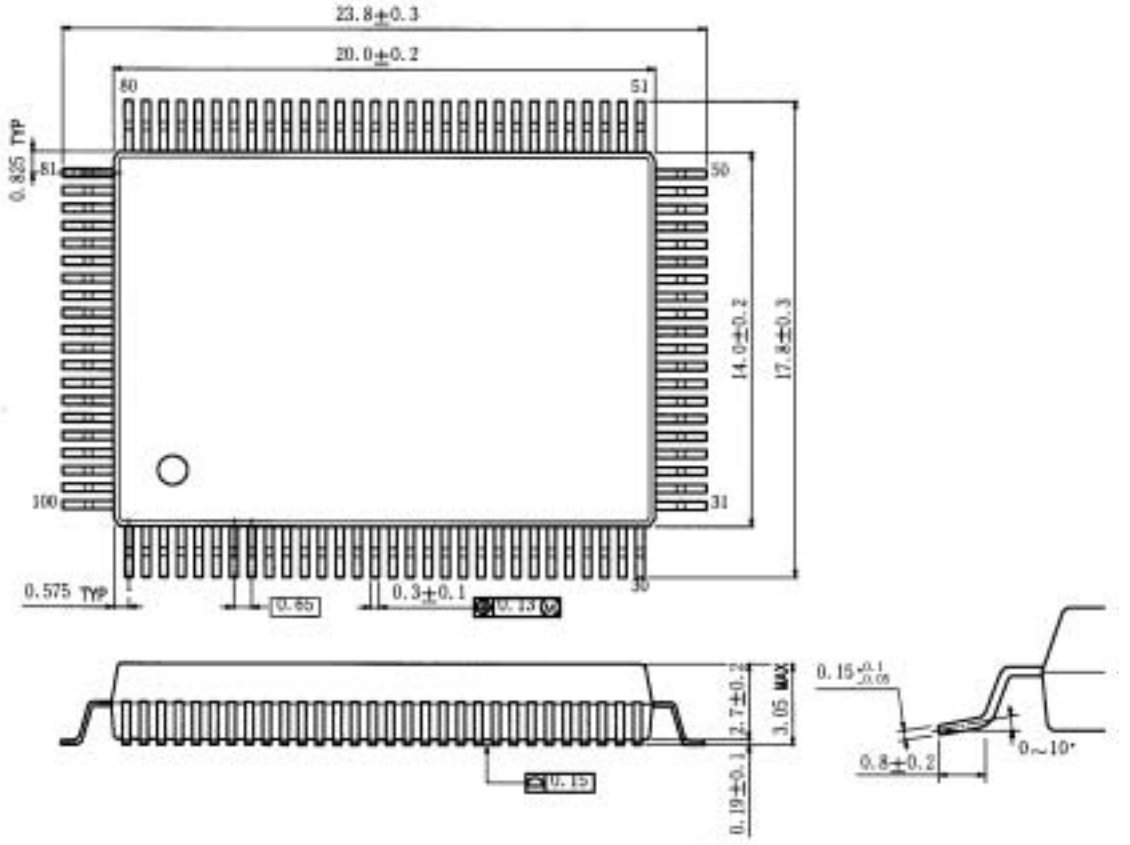

Unit: mm

7-2. External dimensions of the PCD4521




Unit: mm

7-3. External dimensions of the PCD4541




Unit: mm

## 8. Electrical characteristics

8-1. Absolute maximum rating

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Power supply voltage | $V_{DD}$ | -0.3 to +7.0 | V |
| Input voltage | $V_{IN}$ | -0.3 to $V_{DD}$ +0.3 | V |
| Current consumption | $I_{IN}$ | ±10 | mA |
| Storage temperature | $T_{stg}$ | -40 to +125 | ℃ |

8-2. Recommended operation conditions

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Power supply voltage | $V_{DD}$ | 4.5 to 5.5 | V |
| Ambient temperature | $T_j$ | 0 to +85 | ℃ |
| Logical LOW input voltage (1) (2) | $V_{IL}$ | (1) 0 to 0.8 (2) 0 to 1.0 | V |
| Logical HIGH input voltage (1) (2) | $V_{IH}$ | (1) 2.2 to $V_{DD}$ (2) 4.0 to $V_{DD}$ | V |

(1) Inputs other than CLK
(2) CLK

8-3. DC characteristics (recommended operating conditions)

| Item | Symbol | Condition | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|---|
| Current consumption (1) | $I_{DD}$ | PCD4511<br>PCD4521<br>PCD4541 | | | 17<br>34<br>65 | mA |
| Output current loss | $I_{OZ}$ | V0= $V_{DD}$ or GND | -10 | | 10 | µA |
| Input specification | $C_{IN}$ | | | 7 | | pF |
| Logical LOW input current (2) (3) | $I_{IL}$ | $V_{IN}$=GND | (2) -10<br>(3) -200 | | 10<br>-10 | µA |
| Logical HIGH input current (4) | $I_{IH}$ | $V_{IN}$= $V_{DD}$ | -10 | | 10 | µA |
| Logical LOW output current (5) (6) (7) | $I_{OL}$ | $V_{OL}$=0.4 V | (5) 8<br>(6)16<br>(7)16 | | | mA |
| Logical HIGH output current (5) (6) | $I_{OH}$ | $V_{OH}$=2.4 V | | | (5) -8<br>(6) -16 | mA |
| Logical LOW output voltage | $V_{OL}$ | $I_{OL}$=1 µA | | | 0.05 | V |
| Logical LOW output voltage | $V_{OL}$ | $I_{OL}$=MAX | | | 0.4 | V |
| Logical HIGH output voltage | $V_{OH}$ | $I_{OH}$=-1 µA | $V_{DD}$-0.05 | | | V |
| Logical HIGH output voltage | $V_{OH}$ | $I_{OH}$=MAX | 2.4 | | | V |
| Internal pull up resistance | $R_U$ | | 25 | | 500 | KΩ |

1) Reference clock: 10 MHz, at 4,999,390 pps, output load = 85 pF.
2) D0 to D7, A0, A1, A2, A3, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, CLK
3) $\overline{ORG}$, $\overline{\pm EL}$, $\overline{\pm SD}$, $\overline{STA}$, $\overline{STP}$, $\overline{U}$/B, $\overline{F}$/H, $\overline{RST}$
4) D0 to D7, A0, A1, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, $\overline{RST}$,CLK, $\overline{ORG}$, $\overline{\pm EL}$, $\overline{\pm SD}$, $\overline{STA}$, $\overline{STP}$, $\overline{U}$/B, $\overline{F}$/H
5) D0 to D7 and OTS, $\overline{BSY}$, $\overline{\pm PO}$, $\phi$1, $\phi$2, $\phi$3, and $\phi$4 on the PCD4521and PCD4541.
6) OTS, BSY, ±PO, $\phi$1, $\phi$2, $\phi$3, and $\phi$4 on the PCD4511
7) $\overline{INT}$

8-4. Timing specifications

8-4-1. Reference clock

| Item | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Clock frequency | f CLK | | | 10 | MHz |
| Clock duty cycle | t CLK | | 100 | | nS |
| Clock LOW time | t PWL | | 50 | | nS |
| Clock HIGH time | t PWH | | 50 | | nS |

8-4-2. Read cycle

| Item | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Address stabilization time | t AR | | 0 | | nS |
| Address hold time | t RA | | 0 | | nS |
| Read pulse width | t RR | | 42 | | nS |
| Data delay time | t RD | CL=85pF | | 42 | nS |
| Data float delay time | t DF | CL=85pF | | 9 | nS |

8-4-3. Write cycle

| Item | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Address stabilization time | t AW | | 0 | | nS |
| Address hold time | t WA | | 0 | | nS |
| Write pulse width | t WW | | 14 | | nS |
| Data set time | t DW | | 14 | | nS |
| Data hold time | t WD | | 0 | | nS |

8-4-4. Reset cycle

| Item | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $\overline{\text{RST}}$ pulse width | t RST | (*1) | 3 | | t CLK |
| Reset operation time | t RSTM | (*1) | | 3 | t CLK |

8-4-5. Operation timing

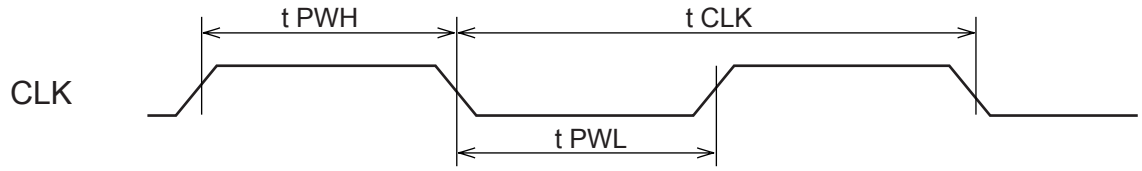
| Item | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $\overline{EL}$ pulse width ($\overline{ORG}$, $\overline{STP}$) | t EL | When high sensitivity is selected | 1 | | t CLK |
| $\overline{EL}$/$\overline{INT}$ delay time | t ELI | (*2) | | 20 | nS |
| Preset/$\overline{INT}$ delay time | t PI | | | 20 | nS |
| $\pm\overline{PO}$ delay time H to L | t PLD | | | 30 | nS |
| $\pm\overline{PO}$ delay time L to H | t PHD | | | 21 | nS |
| Phase excitation output delay time | t PΦ | | | 8 | nS |
| Bipolar $\phi$3, $\phi$4 delay time | t ΦB | | | 7 | nS |
| Preset data read interval | t DRD | (*1) | 1.5 | | t CLK |
| Register data read interval | t DWR | (*1) | 2 | | t CLK |
| $\overline{BSY}$ delay time H to L | t BSL | | | 31 | nS |
| $\overline{BSY}$ delay time (1) L to H | t BSEH | When stopped by $\overline{EL}$ | | 26 | nS |
| $\overline{BSY}$ delay time (2) L to H | t BSPH | When the preset operation is selected | | 26 | nS |

*1: "tCLK" in the unit column means one cycle of the reference clock.

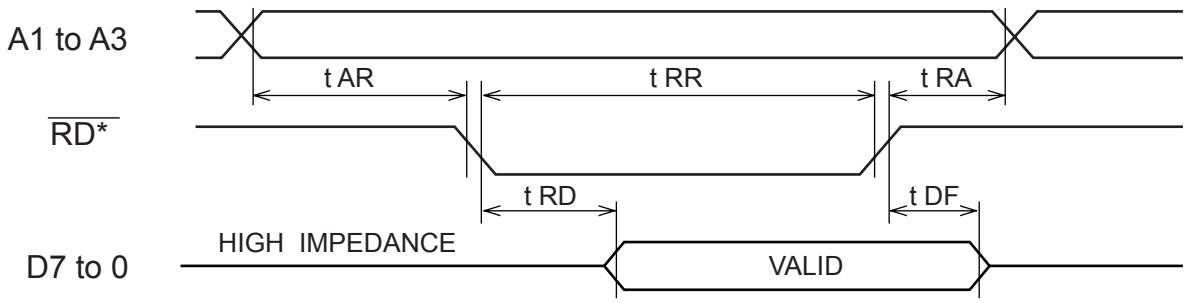
*2: When a stop signal or a stop command is supplied while outputting pulses, the operation will terminate at the end of the current cycle.

8-5. Timing chart

8-5-1. Reference clock

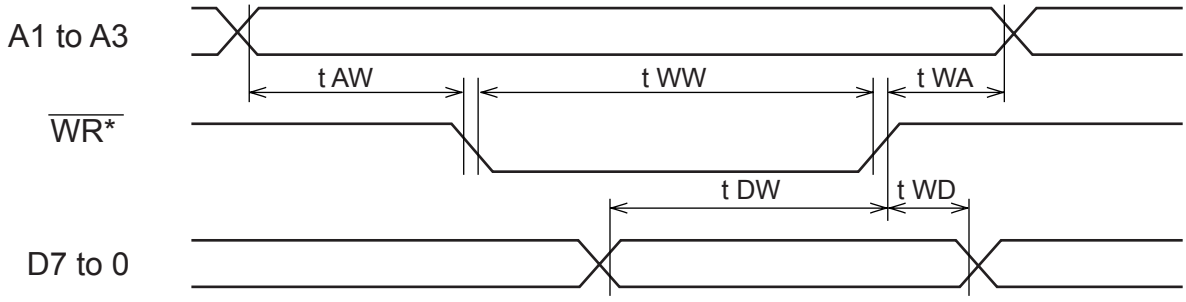



8-5-2. Read cycle



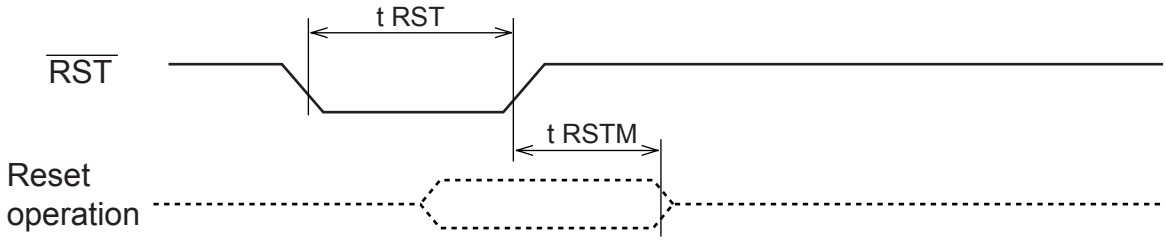

$\overline{RD}$* refers to the logical multiplication of $\overline{RD}$ and $\overline{CS}$.

8-5-3. Write cycle



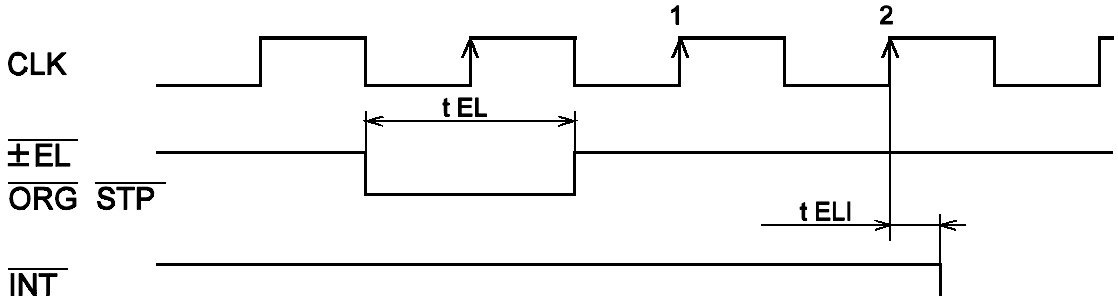

$\overline{WR}$* refers to the logical multiplication of $\overline{WR}$ and $\overline{CS}$.

8-5-4. Reset cycle

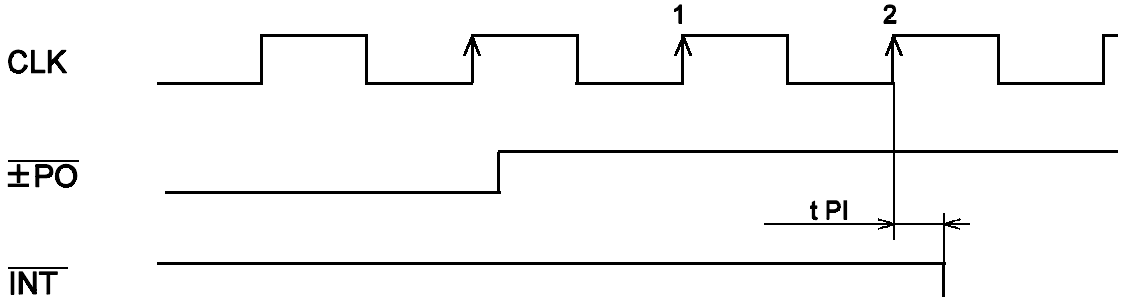


8-5-5. $\overline{INT}$ output timing (When $\overline{\pm PO}$ is set to negative logic)

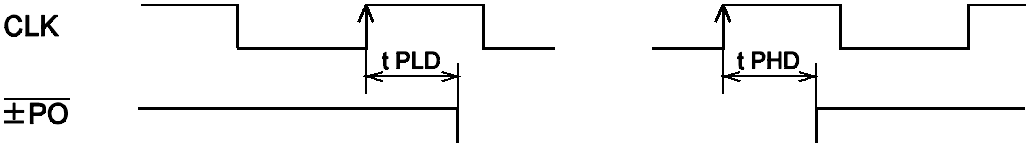
- Stop using $\overline{\pm EL}$, $\overline{ORG}$, or $\overline{STP}$



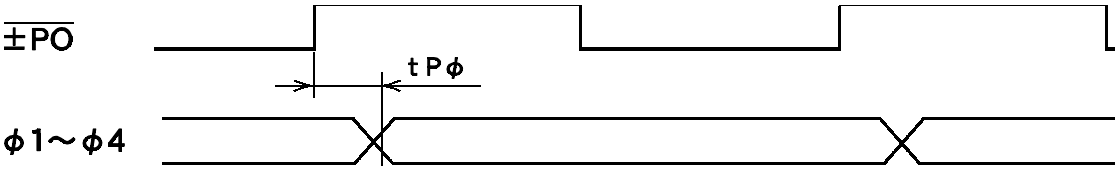

- Stop using Preset operation




8-5-6. $\overline{\pm PO}$ timing (When $\overline{\pm PO}$ is set to negative logic)

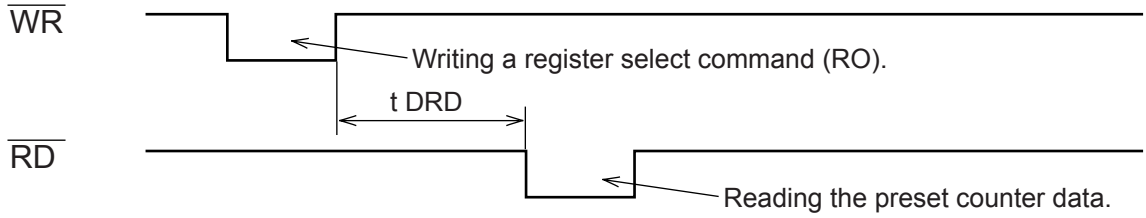



8-5-7. $\overline{\pm PO}$ excitation sequencing timing (When $\overline{\pm PO}$ is set to negative logic)

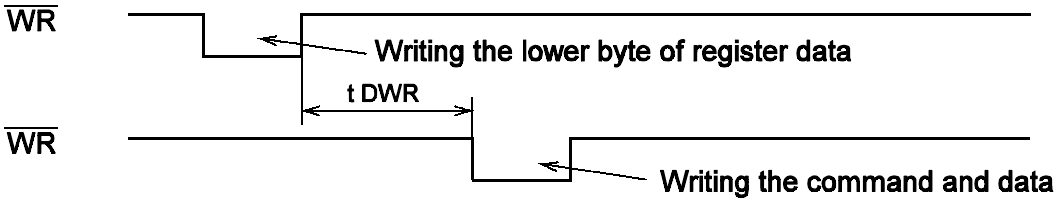



8-5-8. Bipolar 1-2 phase excitation sequence timing

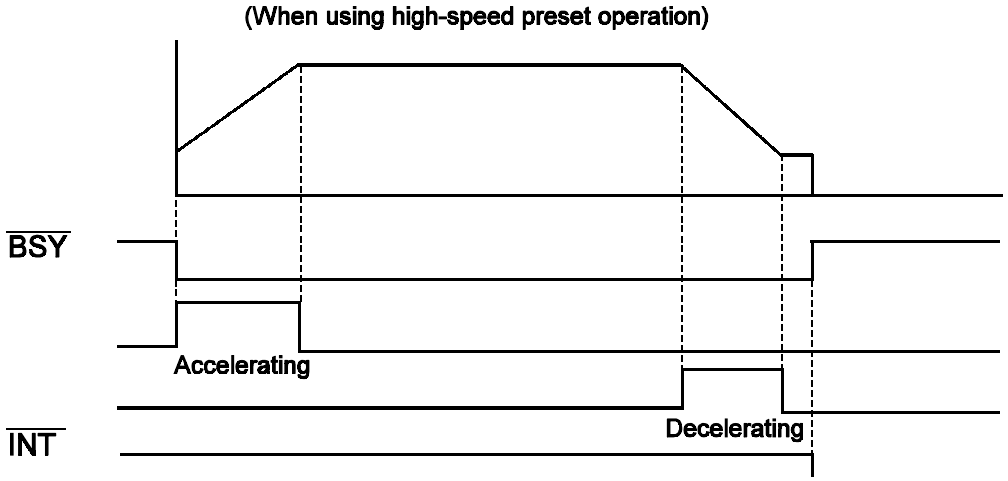
8-5-9. Preset counter data read timing



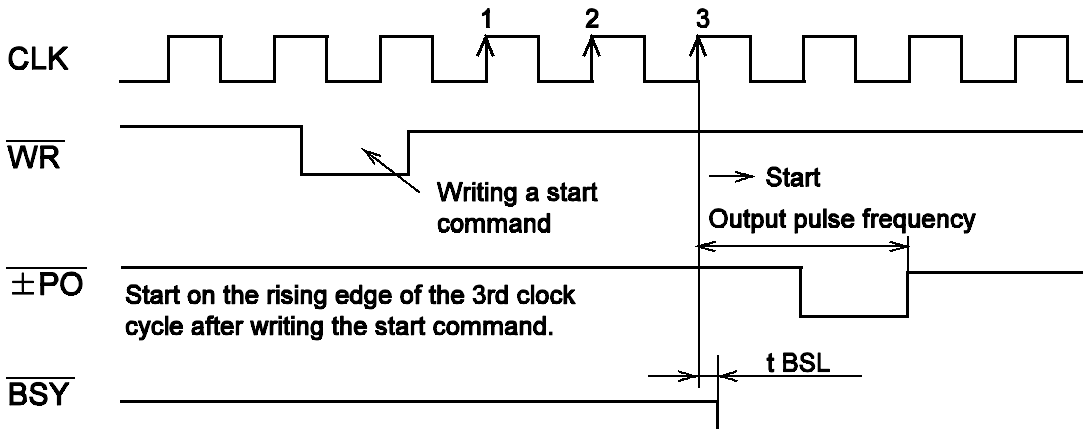

8-5-10. Register data, write timing



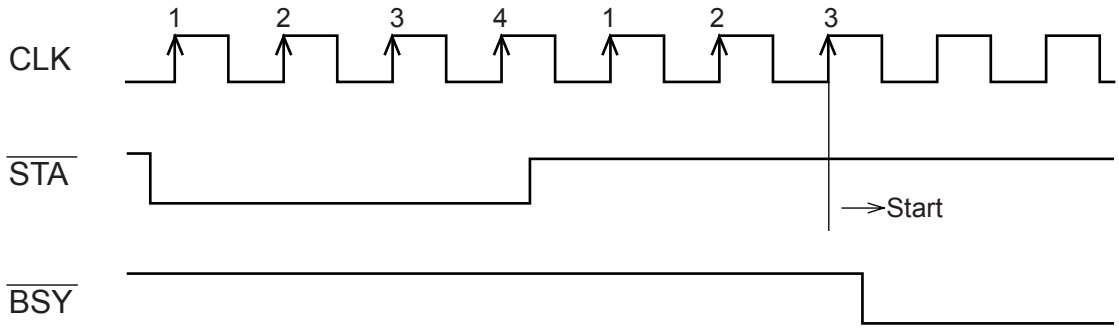

8-5-11. BSY and accel/decel timing



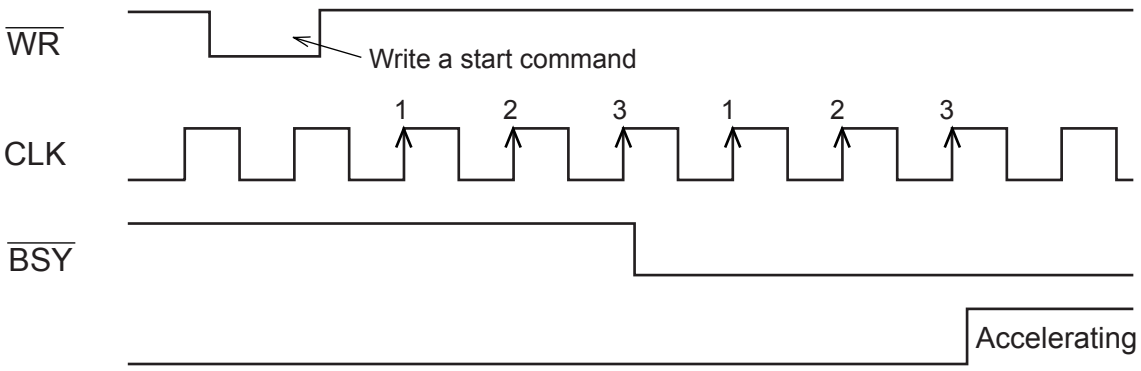
8-5-12. Start timing (When ±PO is set to negative logic)



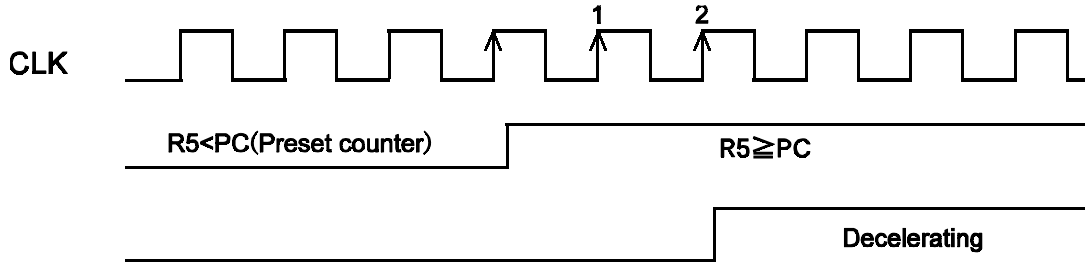

8-5-13. External start timing




8-5-14. Acceleration start timing

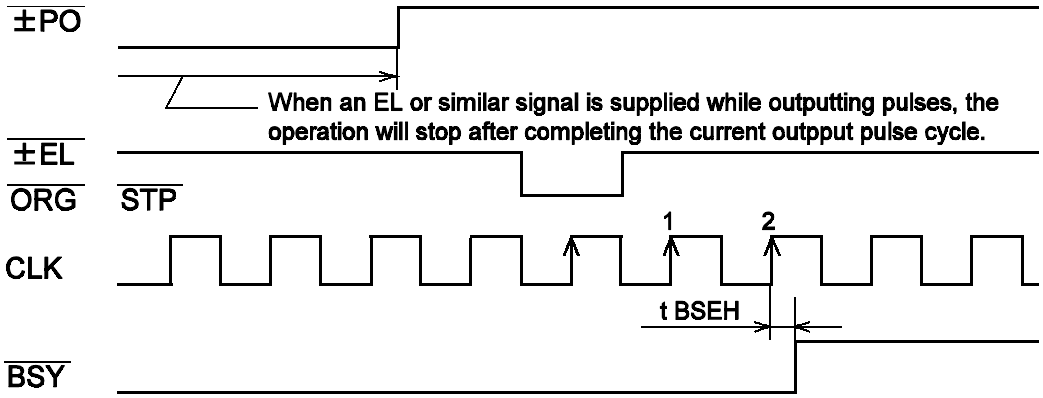


8-5-15. Ramping-down point deceleration initiation timing

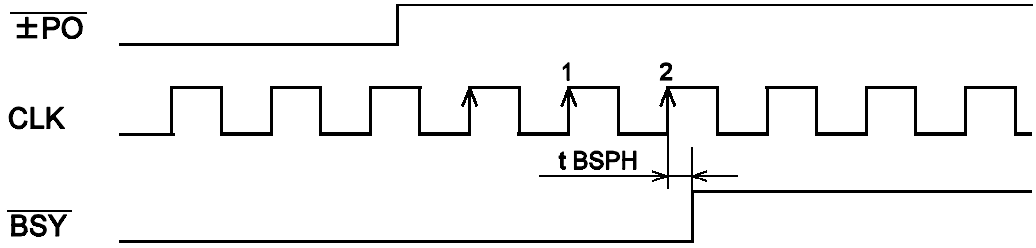



8-5-16. Stopping time (When ±PO is set to negative logic)

- Stop using ±EL, ORG, or STP.




- Stop using Preset operation



## 9. Handling precautions

9-1. Design precautions

1) Never exceed the absolute maximum ratings, even for a very short time.
2) Take precautions against the influence of heat in the environment, and keep the temperature around the LSI as cool as possible.
3) Please note that ignoring the following may result in latching up and may cause overheating and smoke.
   - Do not apply a voltage greater than VDD to the input/output terminals and do not pull them below GND. Also, make sure you consider the input timing when power is applied.
   - Be careful not to introduce external noise into the LSI.
   - Hold the unused input terminals to VDD or GND level.
   - Do not short-circuit the outputs.
   - Protect the LSI from inductive pulses caused by electrical sources that generate large voltage surges, and take appropriate precautions against static electricity.
4) Provide external circuit protection components so that overvoltages caused by noise, voltage surges, or static electricity are not fed to the LSI.

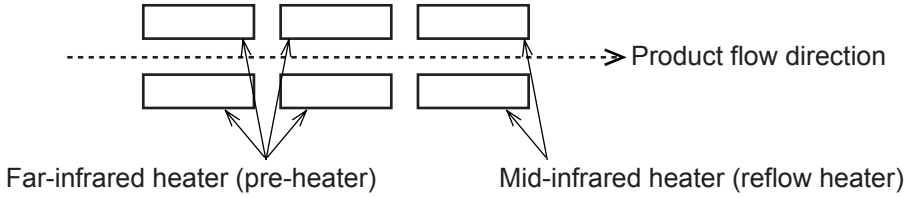
9-2. Precautions for transporting and storing LSIs

1) Always handle LSIs carefully and keep them in their packages. Throwing or dropping LSIs may damage them.
2) Do not store LSIs in a location exposed to water droplets or direct sunlight.
3) Do not store the LSI in a location where corrosive gases are present, or in excessively dusty environments.
4) Store unused LSIs in an anti-static storage container, and make sure that no physical load is placed on the LSIs.

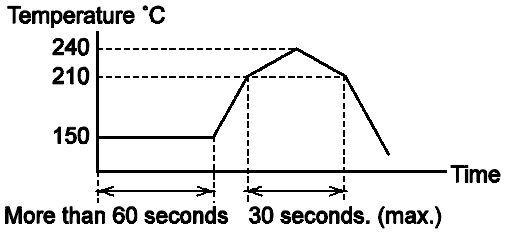
9-3. Precautions for installation

1) In order to prevent damage caused by static electricity, pay attention to the following.
   - Make sure to ground all equipment, tools, and jigs that are present at the work site.
   - Ground the work desk surface using a conductive mat or similar apparatus (with an appropriate resistance factor). However, do not allow work on a metal surface, which can cause a rapid change in the electrical charge on the LSI (if the charged LSI touches the surface directly) due to extremely low resistance.
   - When picking up an LSI using a vacuum device, provide anti-static protection using a conductive rubber pick up tip. Anything which contacts the leads should have as high a resistance as possible.
   - When using a pincer that may make contact with the LSI terminals, use an anti-static model. Do not use a metal pincer, if possible.
   - Store unused LSIs in a PC board storage box that is protected against static electricity, and make sure there is adequate clearance between the LSIs. Never directly stack them on each other, as it may cause friction that can develop an electrical charge.
2) Operators must wear wrist straps which are grounded through approximately 1M-ohm of resistance.
3) Use low voltage soldering devices and make sure the tips are grounded.
4) Do not store or use LSIs, or a container filled with LSIs, near high-voltage electrical fields, such those produced by a CRT.
5) To preheat LSIs for soldering, we recommend keeping them at a high temperature in a completely dry environment, i.e. 125℃ for 20 hours.

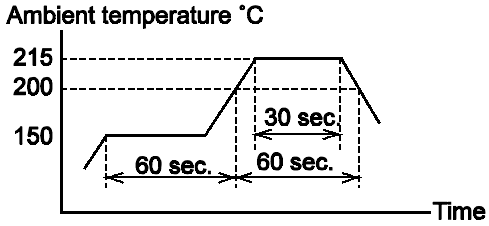
6) When using an infrared reflow system to apply solder, we recommend the use of a far-infrared pre-heater and mid-infrared reflow devices, in order to ease the thermal stress on the LSIs.




To apply heat to LSIs, make sure that the package surface and PC board surface temperatures do not exceed 240℃, and are never above 210℃ for more than 30 seconds.




7) When using hot air for solder reflow, the restrictions are the same as for infrared reflow equipment.
8) When using vapor phase solder, we recommend using Fluorinate FC-70, or its equivalent as a solvent. The ambient temperature must not exceed 215℃ for more than 30 seconds, and must not exceed 200℃ for more than 60 seconds.




9-4. Other precautions

1) When the LSI will be used in poor environments (high humidity, corrosive gases, or excessive amounts of dust), we recommend applying a moisture prevention coating.
2) The package resin is made of fire-retardant material. However, it can burn. When baked or burned, it may generate gases or fire. Do not use it near ignition sources or flammable objects.
3) This LSI is designed for use in commercial apparatus (office machines, communication equipment, measuring equipment, and household appliances). If you use it in any device that may require high quality and reliability, or where faults or malfunctions may directly affect human survival or injure humans, such as in nuclear power control devices, aviation devices or spacecraft, traffic signals, fire control, or various types of safety devices, we will not be liable for any problem that occurs, even it was directly caused by the LSI. Customers must provide their own safety measures to ensure appropriate performance in all circumstances.

**List of commands**

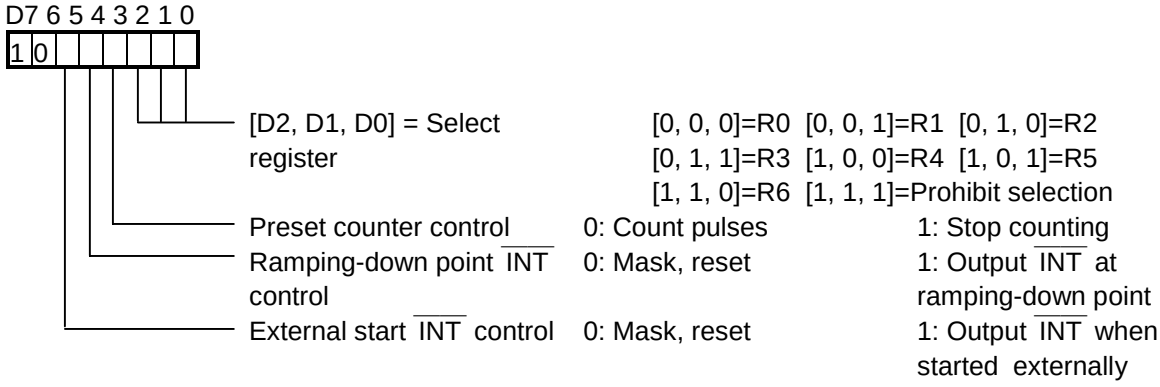
[Start mode command]


| | | |
|---|---|---|
| Select operation speed | 0: Select FL (R1) | 1: Select FH (R2) |
| Inhibited start control | 0: Immediate start | 1: Inhibited (wait for $\overline{\text{STA}}$ signal) |
| Select speed mode | 0: Constant speed (constant speed operation) | 1: High speed (accel/decel operation) |
| Stop control | 0: OFF | 1: ON |
| Start control | 0: OFF | 1: ON |
| $\overline{\text{INT}}$ control when stopped | 0: Mask, reset | 1: Output $\overline{\text{INT}}$ when stopped |

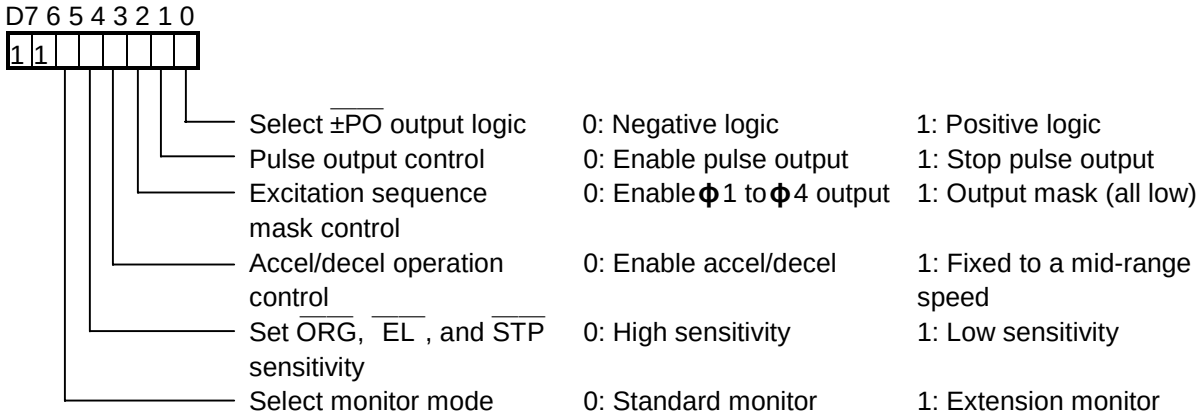
[Control mode command]


| | | |
|---|---|---|
| $\overline{\text{ORG}}$ signal control | 0: Ignores $\overline{\text{ORG}}$ signals | 1: $\overline{\text{ORG}}$ signal causes an immediate stop |
| $\overline{\text{SD}}$ signal control | 0: Ignores $\overline{\text{SD}}$ signals | 1: $\overline{\text{SD}}$ signal initiates deceleration (high speed operation) |
| Preset operation control | 0: Disabled | 1: Enabled (stop when PC reaches zero) |
| Select operating direction | 0: Positive direction | 1: Negative direction |
| OTS terminal control | 0: Make OTS terminal LOW | 1: Make OTS terminal HIGH |
| Accel/decel characteristic control | 0: Linear accel/decel | 1: S-curve accel/decel |

[Register select command]




[Output mode command]



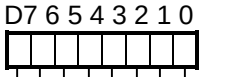

**List of registers**

| Register No. | Details | Bit length | R/W | Allowable range (HEX) |
|---|---|---|---|---|
| R0 | Set preset amount / Check remaining pulses | 24 | R/W | 0 to 16, 777, 215 (FFFFFF) |
| R1 | FL speed | 13 | W (R) | 1 to 8, 191 (1FFF) |
| R2 | FH speed | 13 | W (R) | 1 to 8, 191 (1FFF) |
| R3 | Accel/decel rate | 10 | W (R) | 2 to 1, 023 (3FF) |
| R4 | Magnification | 10 | W (R) | 2 to 1, 023 (3FF) |
| R5 | Ramping-down point | 16 | W (R) | 0 to 65, 535 (FFFF) |
| R6 | Number of idling pulse | 3 | W (R) | 0 to 7 |
| R7 | Environmental data (PCD4541 only) Note. | 1 | W (R) | 0 to (1) |

Monitor list

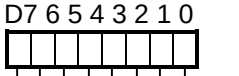
| Mode | Address / Register | A1 = 0, A0 = 0 | A1 = 0, A0 = 1 | A1 = 1, A0 = 0 | A1 = 1, A0 = 0 |
|---|---|---|---|---|---|
| Standard | R0 | Status0 | R0 lower byte | R0 middle byte | R0 upper byte |
| | R1 to R7 | Status0 | Status1 | 0 | 0 |
| Extension monitor | R0 | Status0 | R0 lower byte | R0 middle byte | R0 upper byte |
| | R1 | Status0 | R1 lower byte | R1 upper byte | Start mode command |
| | R2 | Status0 | R2 lower byte | R2 upper byte | Control mode command |
| | R3 | Status0 | R3 lower byte | R3 upper byte | Register select command |
| | R4 | Status0 | R4 lower byte | R4 upper byte | Output mode command |
| | R5 | Status0 | R5 lower byte | R5 upper byte | R7 data |
| | R6 | Status0 | R6 data | Speed lower byte | Speed upper byte |
| | R7 | Status0 | Status1 | Status2 | Status3 |

[Status0]



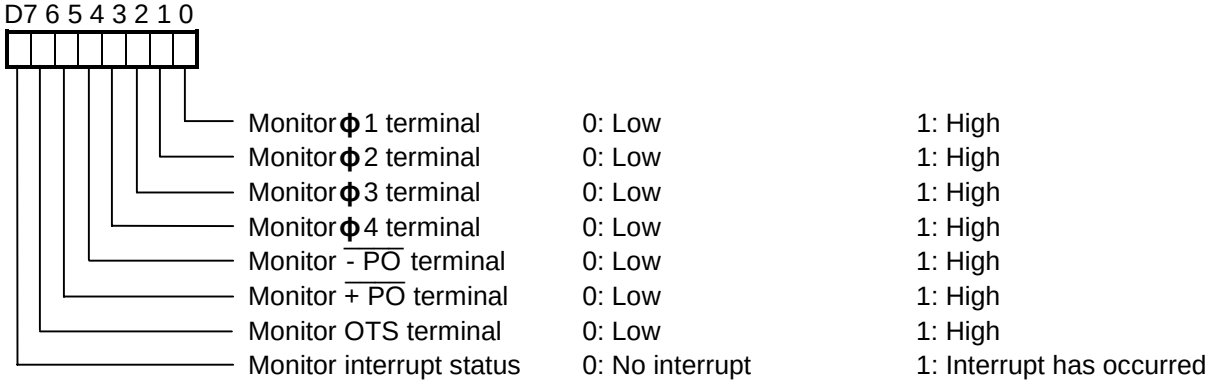

| | | |
|---|---|---|
| Monitor $\overline{\text{INT}}$ output when operation is stopped | 0: Output | 1: Not output |
| Monitor $\overline{\text{INT}}$ output at ramping-down point | 0: Output | 1: Not output |
| Monitor $\overline{\text{INT}}$ output at external start | 0: Output | 1: Not output |
| Monitor operation status | 0: Stopped | 1: Operating |
| Monitor pulse counter zero status | 0: Not zero | 1: Zero |
| Monitor pulse counter and R5 comparison | 0: Pulse counter is larger than R5 | 1: Pulse counter is smaller than R5 |
| Monitor acceleration status | 0: Not accelerating | 1: Accelerating |
| Monitor deceleration status | 0: Not decelerating | 1: Decelerating |

[Status1]

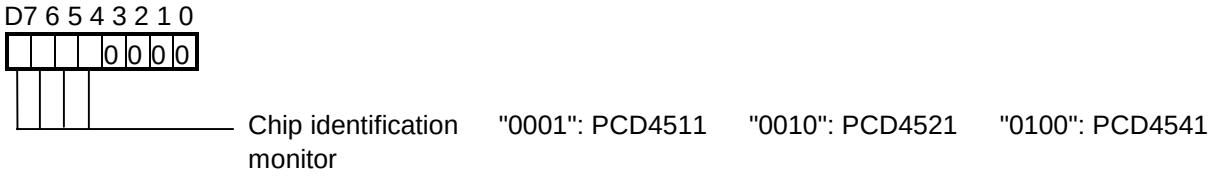



| | | |
|---|---|---|
| Monitor $\overline{\text{-EL}}$ terminal | 0: OFF | 1: ON |
| Monitor $\overline{\text{+EL}}$ terminal | 0: OFF | 1: ON |
| Monitor $\overline{\text{ORG}}$ terminal | 0: OFF | 1: ON |
| Monitor $\overline{\text{STP}}$ terminal | 0: OFF | 1: ON |
| Monitor $\overline{\text{STA}}$ terminal | 0: OFF | 1: ON |
| Monitor $\overline{\text{-SD}}$ terminal | 0: OFF | 1: ON |
| Monitor $\overline{\text{+SD}}$ terminal | 0: OFF | 1: ON |
| Monitor excitation zero position | 0: Not at excitation zero position | 1: At excitation zero position |

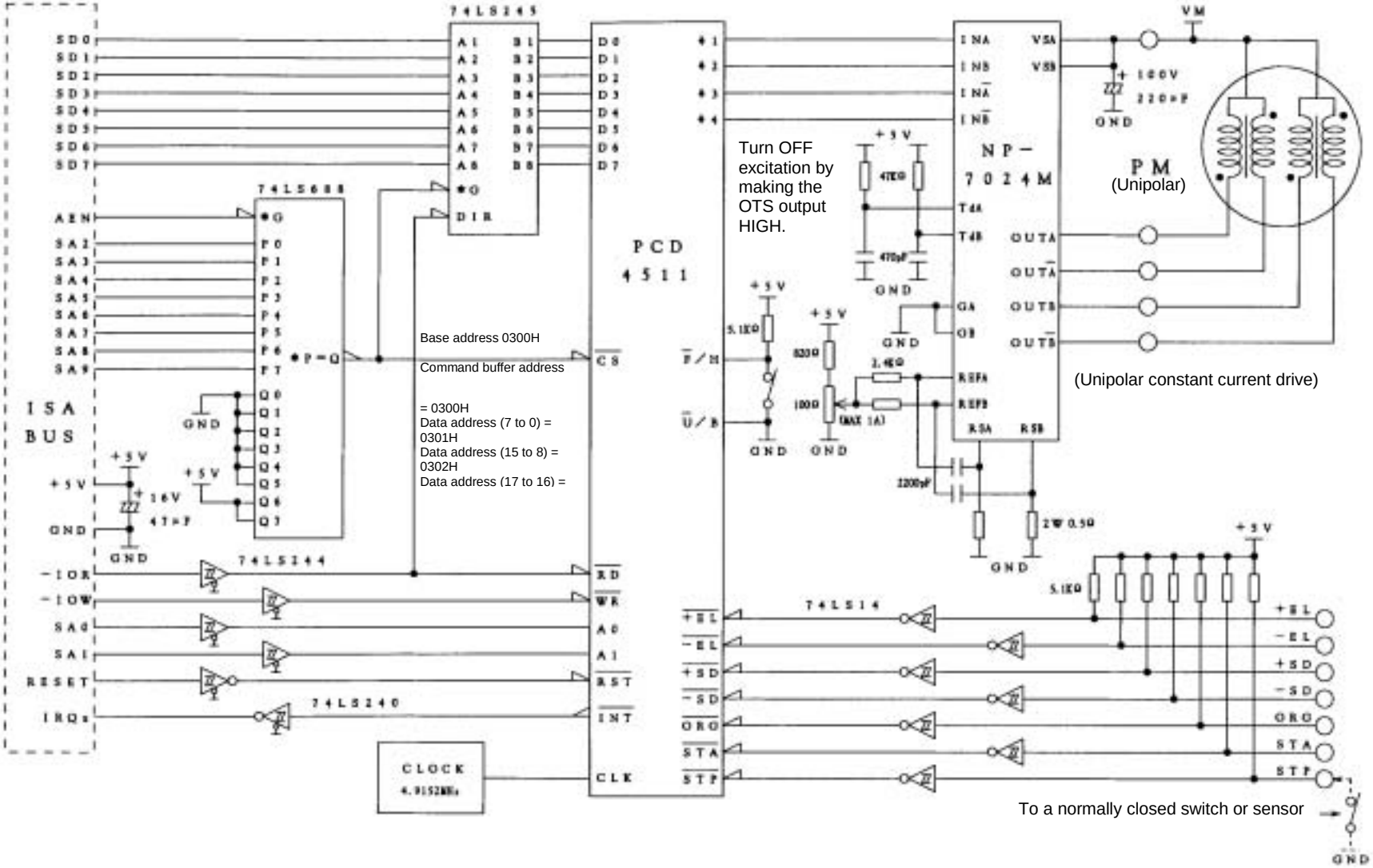
[Status2]



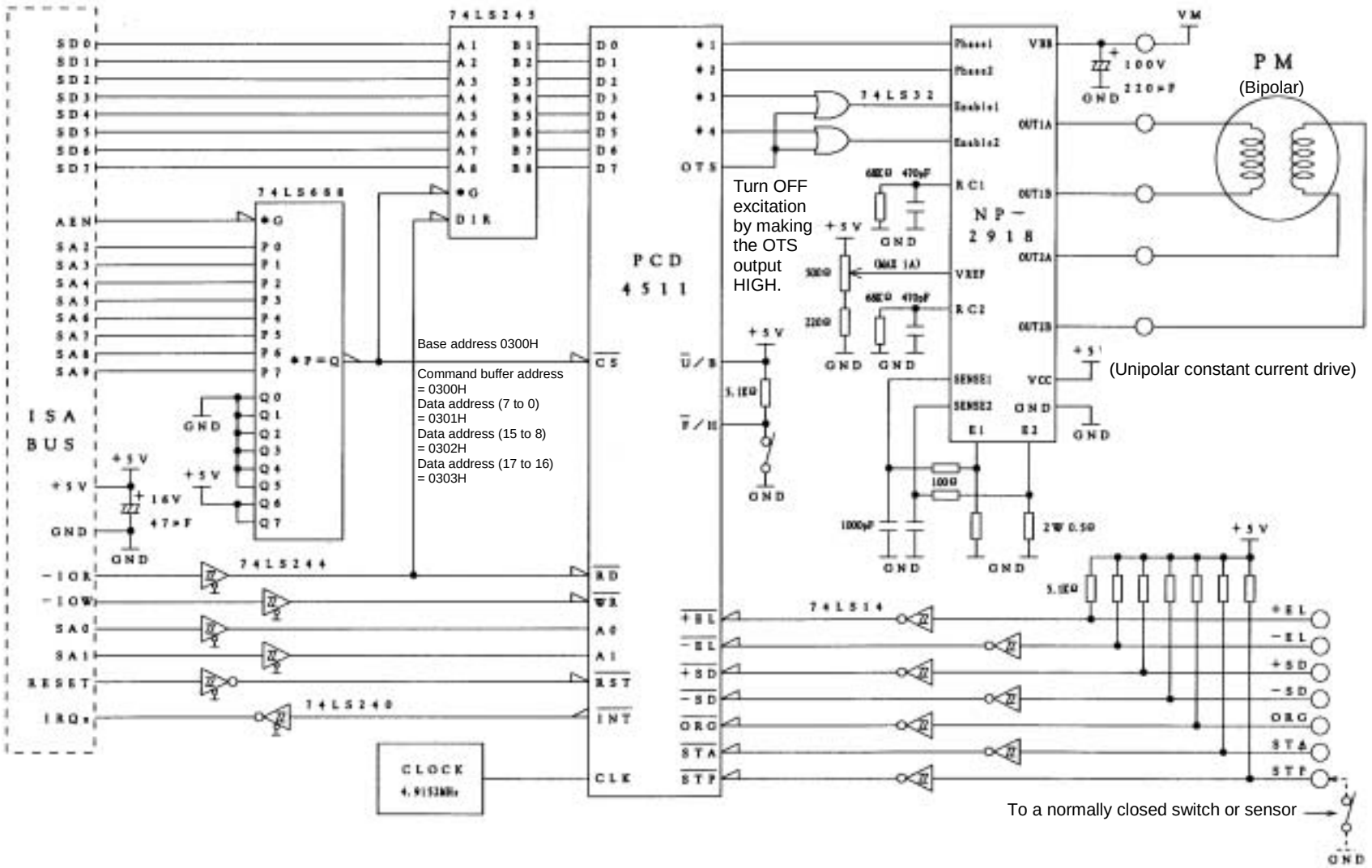

[Status3]



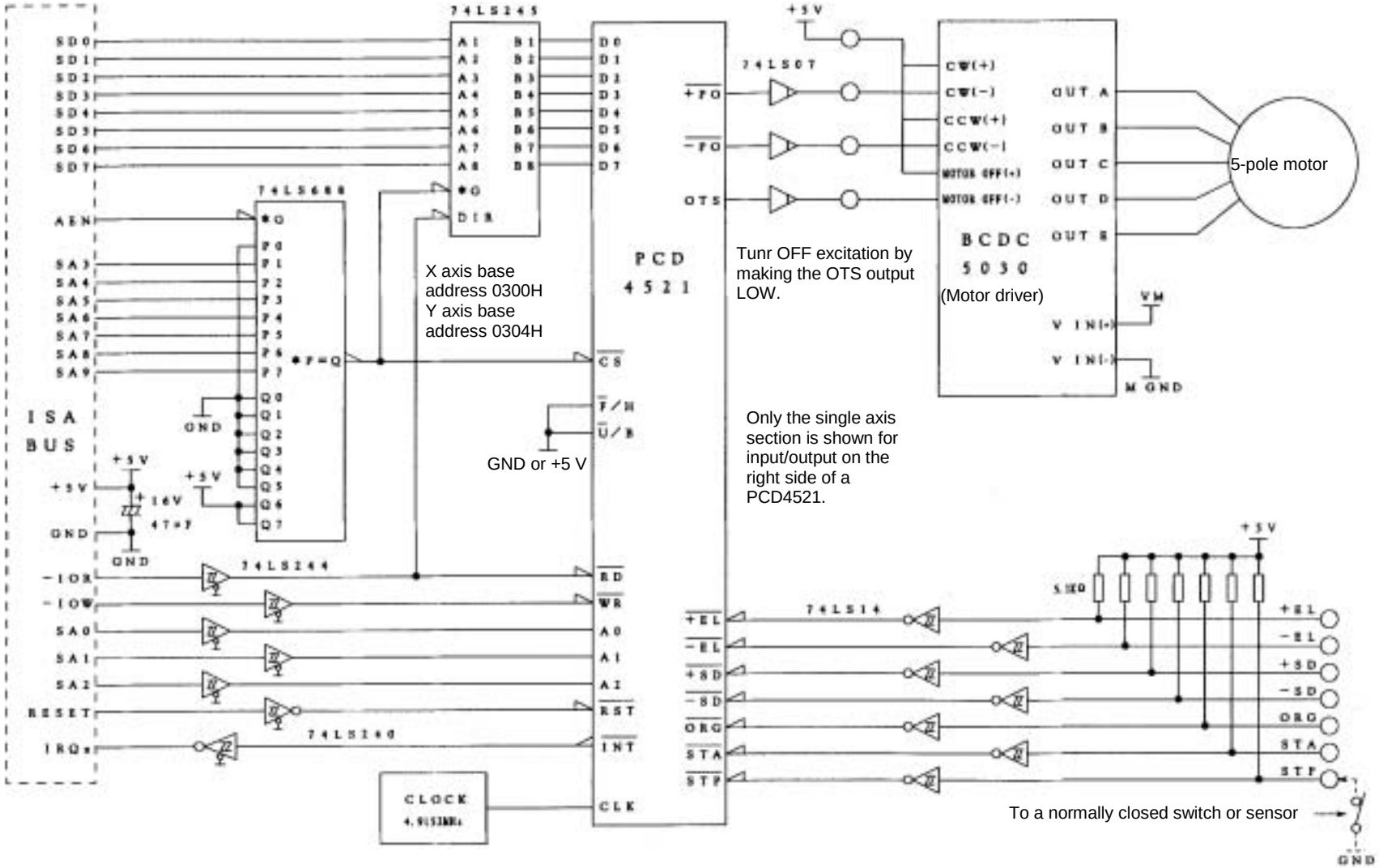
## Connection example of an ISA BUS, PCD4511, and N-7024 (6) M



Connection example of an ISA_BUS, PCD4511, and NP-2918



# Connection example of an ISA_BUS, PCD4521, and BCDC5030



Differences from the PCD4500 (first LSI in this series)

1. Added an S-curve accel/decel function.
   By setting bit 5 in the control command to 1, the S-curve accel/decel function is enabled. When this function is selected, the accel/decel time will be twice the linear accel/decel time. Therefore, the settings need to be readjusted when replacing PCD4500 LSIs.
   1) To make the maximum acceleration speed the same as with the PCD4500.
      Do not change the accel/decel rate. Double the ramping-down point. (The accel/decel time will be twice as long.)
   2) To make the accel/decel time the same as with the PCD4500
      Do not change the ramping-down point. Decrease the accel/decel rate to 1/2 the original setting. (The maximum acceleration speed will be doubled.)

2. The positioning feed counter has been changed from 18-bits to 24-bits
   The positioning preset counter has been changed from 262,143 pulses (PCD4500) to 16,777,215 pulses. Thus, the new series can be used for applications, which need a large feed number.

3. No need for an 08hex Reset command
   The PCD4500 required you to write 08h before starting. This is no longer needed in the PCD45X1 series.

4. Improved start inhibit safety using STA signal
   The PCD4500 ignores the STP and EL signals when inhibited start is used. The PCD45x1 series can accept STP and EL signals while inhibited. Therefore, even when the STA signal is input, the motor maintains stop status.

5. Additional registers and register capability
   All registers can be read. This is very useful for debugging.

6. Added an output terminal status confirmation (Status2) and an IC identification function (Status3).
   By improving the Status function, the status of the IC can be understood in greater detail.

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