NEC

MOS INTEGRATED CIRCUIT
μPD161644A

241 OUTPUT GATE DRIVER WITH POWER SUPPLY FOR TFT-LCD GATE DRIVER

DESCRIPTION

The μPD161644A is a TFT-LCD gate driver with power supply for TFT-LCD driver. Because this gate driver has a level shift circuit for logic input, it can output a high gate scanning voltage in response to a CMOS-level input. This ICs can generate the levels which TFT-LCD driver need, from 2.7 V.

FEATURES

- High breakdown voltage output (V_{DD1}–V_{SS3} = 40 V MAX.)
- 2.7 V CMOS level input
- Number of output: 241 output selectable
- To generate 4 levels from single voltage input
- To integrate regulator circuit for source driver
- Mode setting from source driver: Serial I/F or pin control
- On-chip VCOM driver
- On-chip gate output low-level selector

ORDERING INFORMATION

Part number	Package
μPD161644A	Chip

Remark Purchasing the above chip entails the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representatives.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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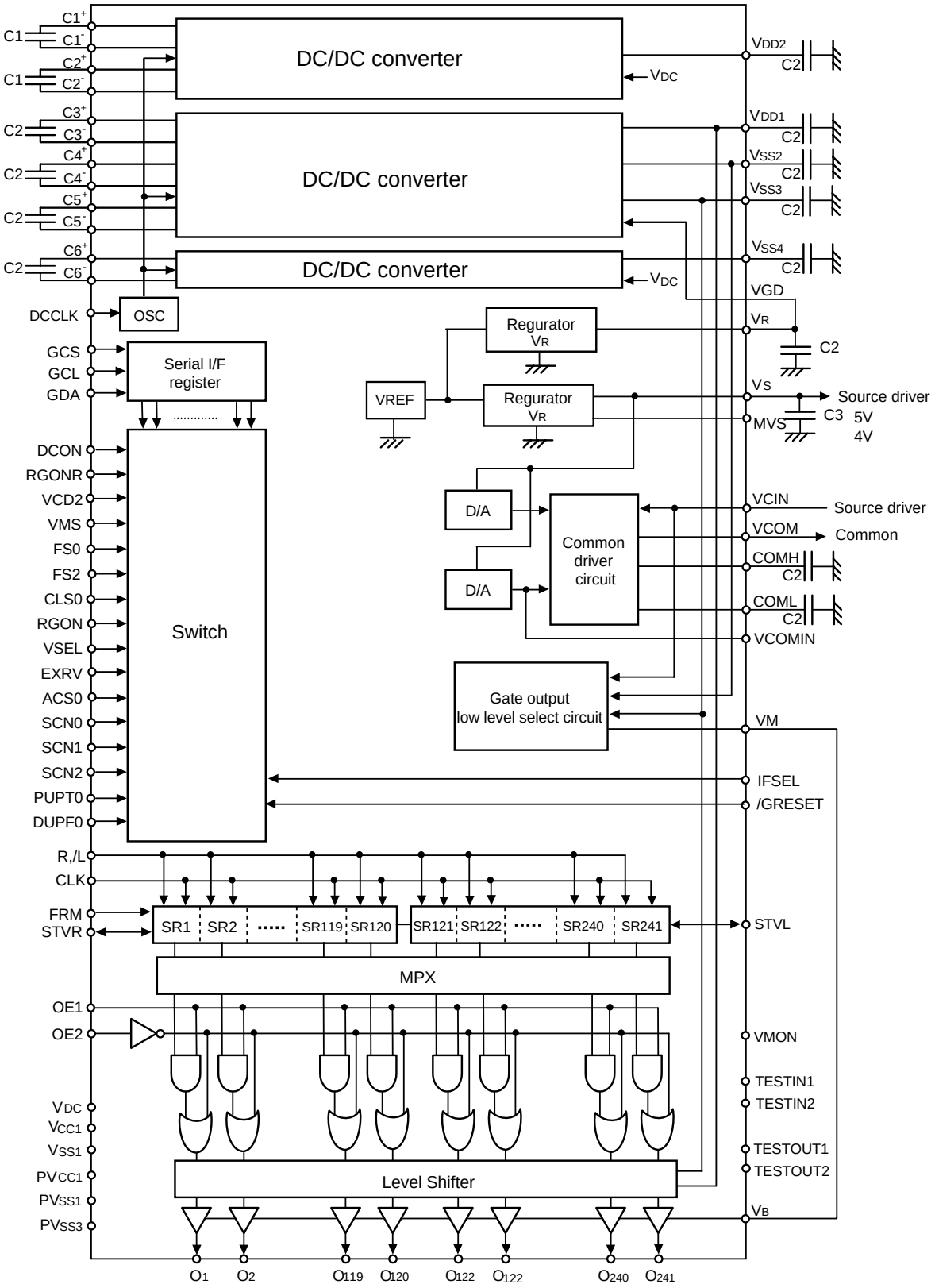
1. BLOCK DIAGRAM/SYSTEM DIAGRAM

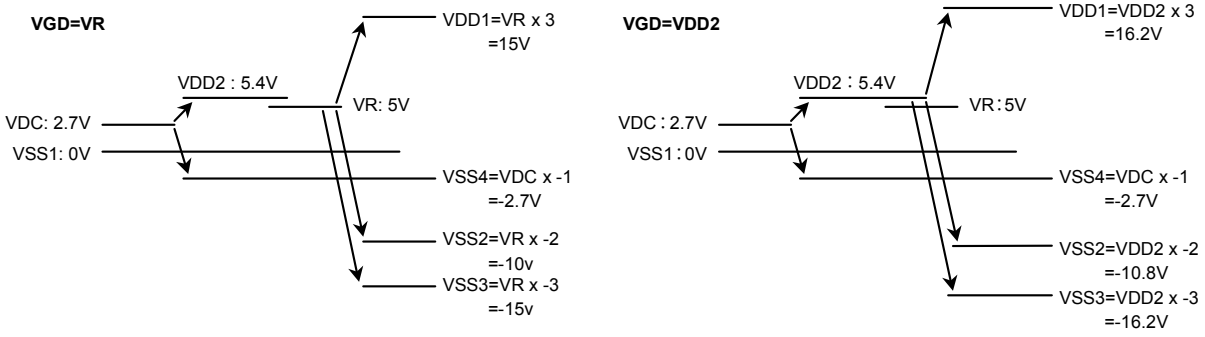


Remarks 1. /xxx indicates active low signal.

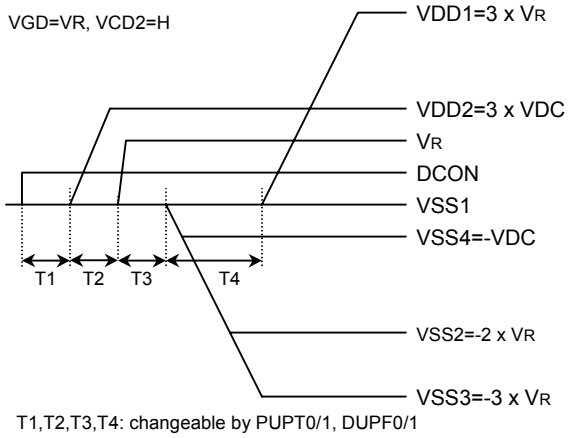
2. Level Shifter (LS): Interfaces between 2.7 V CMOS level and V_T to V_B level.

1.1 Boost Voltage Construction

The boost voltage generated in μPD161644A is shown below.



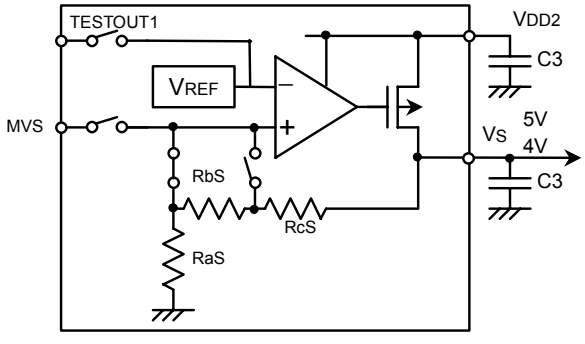
1.2 Boost Voltage Auto Start and Rising Order



T1,T2,T3,T4: changeable by PUPT0/1, DUPF0/1

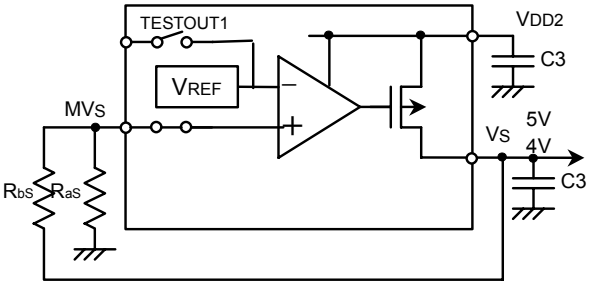
1.3 VS_AMP Circuit

Vs_AMP circuits are shown below.



Internal Resistor Mode

EXRV=L



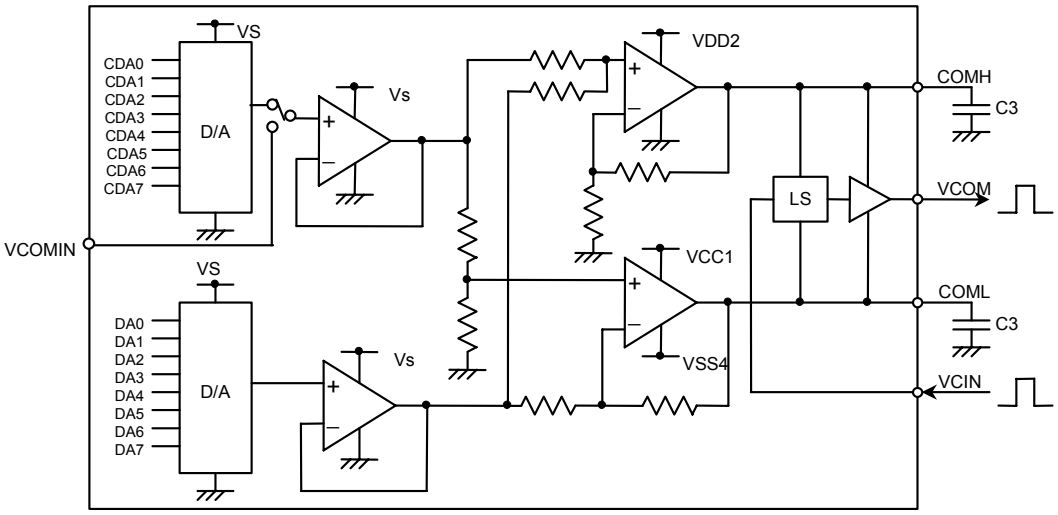
External Resistor Mode

EXRV=H

$V_S=(1+\frac{R_{bS}}{R_{aS}})V_{REF}$

1.4 Common Drive Circuit

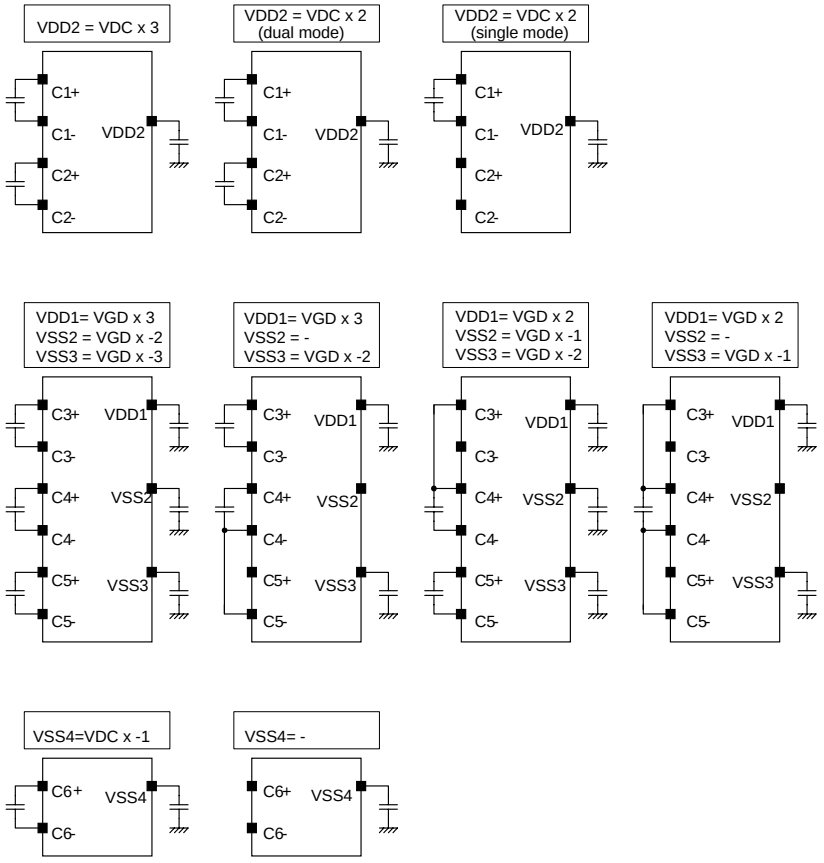
The common drive circuit is shown below.



1.5 Variable Boost Steps

The boost steps of V_{DD1}, V_{SS2}, V_{SS3} are selected according to how the external capacitor is connected.

The examples of connection are shown below. V_S is selected as a boost reference voltage in these examples (short between the V_S and VGD pins).



2. PIN CONFIGURATION (Pad Layout)

Chip size: 2.8 mm x 9.4 mm

Bump size

Input/Left/Right (includes DUMMY of input side) : 100 μm x 40 μm

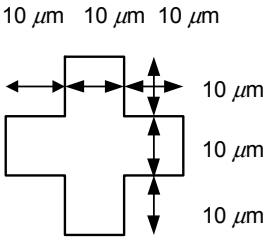
Output (includes DUMMY output side) : 86 μm x 35 μm

Alignment Mark Coordinate (mark center, unit: mm)

X	Y	Shape of Alignment Mark
−1.125	−4.5705	Type A
0.9705	4.5495	Type B
0.9705	−4.5495	Type B

Alignment Mark

Type A



Type B

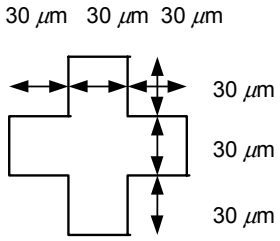


Table 2-1 Pad Layout (1/4)

長辺

PADTYPE :			
GATE INPUTS BUMP SIZE 100um x 40um			
PAD NO.	PAD NAME	X [mm]	Y [mm]
—	Alignment Mark2	−1.125	−4.5705
1	DUMMY	−1.242	−4.5500
2	TESTOUT2	−1.242	−4.4900
3	TESTIN2	−1.242	−4.4300
4	TESTIN1	−1.242	−4.3700
5	TESTOUT1	−1.242	−4.3100
6	PVCC1	−1.242	−4.2500
7	DUPF0	−1.242	−4.1900
8	PUPT0	−1.242	−4.1300
9	SCN2	−1.242	−4.0700
10	SCN1	−1.242	−4.0100
11	SCN0	−1.242	−3.9500
12	ACS0	−1.242	−3.8900
13	EXRV	−1.242	−3.8300
14	VSEL	−1.242	−3.7700
15	CLS0	−1.242	−3.7100
16	FS2	−1.242	−3.6500
17	FS0	−1.242	−3.5900
18	VMS	−1.242	−3.5300
19	RGONR	−1.242	−3.4700
20	PVSS1	−1.242	−3.4100
21	PVSS3	−1.242	−3.3500
22	VMON	−1.242	−3.2900
23	DUMMY	−1.242	−3.2300
24	PVCC1	−1.242	−3.1700
25	R/L	−1.242	−3.1100
26	IFSEL	−1.242	−3.0500
27	PVSS1	−1.242	−2.9900
28	VCOMIN	−1.242	−2.9200
29	VCOM	−1.242	−2.8500
30	VCOM	−1.242	−2.7900
31	VCOM	−1.242	−2.7300
32	COML	−1.242	−2.6600
33	COML	−1.242	−2.6000
34	COMH	−1.242	−2.5300
35	COMH	−1.242	−2.4700
36	VM	−1.242	−2.4000
37	VM	−1.242	−2.3400
38	VB	−1.242	−2.2700
39	VB	−1.242	−2.2100
40	VSS3	−1.242	−2.1400
41	VSS3	−1.242	−2.0800
42	VSS3	−1.242	−2.0200
43	VSS4	−1.242	−1.9500
44	VSS4	−1.242	−1.8900
45	VSS4	−1.242	−1.8300
46	VSS2	−1.242	−1.7600
47	VSS2	−1.242	−1.7000
48	VSS2	−1.242	−1.6400
49	C6−	−1.242	−1.5700
50	C6−	−1.242	−1.5100
51	C6+	−1.242	−1.4400
52	C6+	−1.242	−1.3800
53	C5−	−1.242	−1.3100
54	C5−	−1.242	−1.2500
55	C5+	−1.242	−1.1800
56	C5+	−1.242	−1.1200
57	C4−	−1.242	−1.0500
58	C4−	−1.242	−0.9900
59	C4+	−1.242	−0.9200
60	C4+	−1.242	−0.8600
61	C3−	−1.242	−0.7900
62	C3−	−1.242	−0.7300
63	C3+	−1.242	−0.6600
64	C3+	−1.242	−0.6000
65	VDD1	−1.242	−0.5300
66	VDD1	−1.242	−0.4700
67	VDD1	−1.242	−0.4100
68	DUMMY	−1.242	−0.3400
69	DUMMY	−1.242	−0.2800
70	DUMMY	−1.242	−0.2200
71	DUMMY	−1.242	−0.1600
72	DUMMY	−1.242	−0.0900

長辺

PADTYPE :			
GATE INPUTS BUMP SIZE 100um x 40um			
PAD NO.	PAD NAME	X [mm]	Y [mm]
73	DUMMY	−1.242	−0.0300
74	DUMMY	−1.242	0.0300
75	DUMMY	−1.242	0.0900
76	VB	−1.242	0.1600
77	VB	−1.242	0.2200
78	VSS3	−1.242	0.2900
79	VSS3	−1.242	0.3500
80	VSS3	−1.242	0.4100
81	C5−	−1.242	0.4800
82	C5−	−1.242	0.5400
83	C5+	−1.242	0.6100
84	C5+	−1.242	0.6700
85	C4−	−1.242	0.7400
86	C4−	−1.242	0.8000
87	C4+	−1.242	0.8700
88	C4+	−1.242	0.9300
89	C3−	−1.242	1.0000
90	C3−	−1.242	1.0600
91	C3+	−1.242	1.1300
92	C3+	−1.242	1.1900
93	VDD1	−1.242	1.2600
94	VDD1	−1.242	1.3200
95	VDD1	−1.242	1.3800
96	C2−	−1.242	1.4500
97	C2−	−1.242	1.5100
98	C2−	−1.242	1.5700
99	C2−	−1.242	1.6300
100	C2+	−1.242	1.7000
101	C2+	−1.242	1.7600
102	C2+	−1.242	1.8200
103	C2+	−1.242	1.8800
104	C1−	−1.242	1.9500
105	C1−	−1.242	2.0100
106	C1−	−1.242	2.0700
107	C1−	−1.242	2.1300
108	C1+	−1.242	2.2000
109	C1+	−1.242	2.2600
110	C1+	−1.242	2.3200
111	C1+	−1.242	2.3800
112	VDD2	−1.242	2.4500
113	VDD2	−1.242	2.5100
114	VDD2	−1.242	2.5700
115	VDD2	−1.242	2.6300
116	VSS1	−1.242	2.7000
117	VSS1	−1.242	2.7600
118	VSS1	−1.242	2.8200
119	VDC	−1.242	2.8900
120	VDC	−1.242	2.9500
121	VDC	−1.242	3.0100
122	VDC	−1.242	3.0700
123	VDC	−1.242	3.1300
124	VCC1	−1.242	3.2000
125	VCC1	−1.242	3.2600
126	VCC1	−1.242	3.3200
127	VSS1	−1.242	3.3900
128	VSS1	−1.242	3.4500
129	VSS1	−1.242	3.5100
130	VSS1	−1.242	3.5700
131	VSS1	−1.242	3.6300
132	VR	−1.242	3.7000
133	VR	−1.242	3.7600
134	VGD	−1.242	3.8300
135	VGD	−1.242	3.8900
136	VGD	−1.242	3.9500
137	MVS	−1.242	4.0200
138	VS	−1.242	4.0900
139	VS	−1.242	4.1500
140	VS	−1.242	4.2100
141	VS	−1.242	4.2700
142	VS	−1.242	4.3300
143	DUMMY	−1.242	4.3900

Table 2-1 Pad Layout (2/4)

短辺

PADTYPE :			
GATE INPUTS BUMP SIZE 100um x 40um			
PAD NO.	PAD NAME	X [mm]	Y [mm]
144	DUMMY	-1.0000	4.5420
145	PVCC1	-0.9300	4.5420
146	VCD2	-0.8600	4.5420
147	RGON	-0.7900	4.5420
148	DCON	-0.7200	4.5420
149	FRM	-0.6500	4.5420
150	VCIN	-0.5800	4.5420
151	PVSS1	-0.5100	4.5420
152	/GRESET	-0.4400	4.5420
153	GCS	-0.3700	4.5420
154	GCL	-0.3000	4.5420
155	GDA	-0.2300	4.5420
156	STVR	-0.1600	4.5420
157	STVL	-0.0900	4.5420
158	DCCLK	-0.0200	4.5420
159	CLK	0.0500	4.5420
160	OE1	0.1200	4.5420
161	OE2	0.1900	4.5420
162	DUMMY	0.2600	4.5420
163	DUMMY	-0.7500	-4.5720
164	DUMMY	-0.4500	-4.5720
165	DUMMY	-0.1500	-4.5720
166	DUMMY	0.1500	-4.5720
167	DUMMY	0.4500	-4.5720
168	DUMMY	0.7500	-4.5720

Table 2-1 Pad Layout (3/4)

PADTYPE : BUMP SIZE 86u x 35um			
GATE OUTPUTS 35um pitch			
PAD NO.	PAD NAME	X [mm]	Y [mm]
—	**Alignment Mark1**	0.9705	4.5495
169	DUMMY	1.249	4.3050
170	DUMMY	1.127	4.2700
171	DUMMY	1.249	4.2350
172	241	1.127	4.2000
173	240	1.249	4.1650
174	239	1.127	4.1300
175	238	1.249	4.0950
176	237	1.127	4.0600
177	236	1.249	4.0250
178	235	1.127	3.9900
179	234	1.249	3.9550
180	233	1.127	3.9200
181	232	1.249	3.8850
182	231	1.127	3.8500
183	230	1.249	3.8150
184	229	1.127	3.7800
185	228	1.249	3.7450
186	227	1.127	3.7100
187	226	1.249	3.6750
188	225	1.127	3.6400
189	224	1.249	3.6050
190	223	1.127	3.5700
191	222	1.249	3.5350
192	221	1.127	3.5000
193	220	1.249	3.4650
194	219	1.127	3.4300
195	218	1.249	3.3950
196	217	1.127	3.3600
197	216	1.249	3.3250
198	215	1.127	3.2900
199	214	1.249	3.2550
200	213	1.127	3.2200
201	212	1.249	3.1850
202	211	1.127	3.1500
203	210	1.249	3.1150
204	209	1.127	3.0800
205	208	1.249	3.0450
206	207	1.127	3.0100
207	206	1.249	2.9750
208	205	1.127	2.9400
209	204	1.249	2.9050
210	203	1.127	2.8700
211	202	1.249	2.8350
212	201	1.127	2.8000
213	200	1.249	2.7650
214	199	1.127	2.7300
215	198	1.249	2.6950
216	197	1.127	2.6600
217	196	1.249	2.6250
218	195	1.127	2.5900
219	194	1.249	2.5550
220	193	1.127	2.5200
221	192	1.249	2.4850
222	191	1.127	2.4500
223	190	1.249	2.4150
224	189	1.127	2.3800
225	188	1.249	2.3450
226	187	1.127	2.3100
227	186	1.249	2.2750
228	185	1.127	2.2400
229	184	1.249	2.2050
230	183	1.127	2.1700
231	182	1.249	2.1350
232	181	1.127	2.1000
233	180	1.249	2.0650
234	179	1.127	2.0300
235	178	1.249	1.9950
236	177	1.127	1.9600
237	176	1.249	1.9250
238	175	1.127	1.8900
239	174	1.249	1.8550
240	173	1.127	1.8200

PADTYPE : BUMP SIZE 86u x 35um			
GATE OUTPUTS 35um pitch			
PAD NO.	PAD NAME	X [mm]	Y [mm]
241	172	1.249	1.7850
242	171	1.127	1.7500
243	170	1.249	1.7150
244	169	1.127	1.6800
245	168	1.249	1.6450
246	167	1.127	1.6100
247	166	1.249	1.5750
248	165	1.127	1.5400
249	164	1.249	1.5050
250	163	1.127	1.4700
251	162	1.249	1.4350
252	161	1.127	1.4000
253	160	1.249	1.3650
254	159	1.127	1.3300
255	158	1.249	1.2950
256	157	1.127	1.2600
257	156	1.249	1.2250
258	155	1.127	1.1900
259	154	1.249	1.1550
260	153	1.127	1.1200
261	152	1.249	1.0850
262	151	1.127	1.0500
263	150	1.249	1.0150
264	149	1.127	0.9800
265	148	1.249	0.9450
266	147	1.127	0.9100
267	146	1.249	0.8750
268	145	1.127	0.8400
269	144	1.249	0.8050
270	143	1.127	0.7700
271	142	1.249	0.7350
272	141	1.127	0.7000
273	140	1.249	0.6650
274	139	1.127	0.6300
275	138	1.249	0.5950
276	137	1.127	0.5600
277	136	1.249	0.5250
278	135	1.127	0.4900
279	134	1.249	0.4550
280	133	1.127	0.4200
281	132	1.249	0.3850
282	131	1.127	0.3500
283	130	1.249	0.3150
284	129	1.127	0.2800
285	128	1.249	0.2450
286	127	1.127	0.2100
287	126	1.249	0.1750
288	125	1.127	0.1400
289	124	1.249	0.1050
290	123	1.127	0.0700
291	122	1.249	0.0350
292	121	1.127	0.0000
293	120	1.249	−0.0350
294	119	1.127	−0.0700
295	118	1.249	−0.1050
296	117	1.127	−0.1400
297	116	1.249	−0.1750
298	115	1.127	−0.2100
299	114	1.249	−0.2450
300	113	1.127	−0.2800
301	112	1.249	−0.3150
302	111	1.127	−0.3500
303	110	1.249	−0.3850
304	109	1.127	−0.4200
305	108	1.249	−0.4550
306	107	1.127	−0.4900
307	106	1.249	−0.5250
308	105	1.127	−0.5600
309	104	1.249	−0.5950
310	103	1.127	−0.6300
311	102	1.249	−0.6650
312	101	1.127	−0.7000

Table 2-1 Pad Layout (4/4)

PADTYPE : BUMP SIZE 86u x 35um			
GATE OUTPUTS 35um pitch			
PAD NO.	PAD NAME	X [mm]	Y [mm]
313	100	1.249	-0.7350
314	99	1.127	-0.7700
315	98	1.249	-0.8050
316	97	1.127	-0.8400
317	96	1.249	-0.8750
318	95	1.127	-0.9100
319	94	1.249	-0.9450
320	93	1.127	-0.9800
321	92	1.249	-1.0150
322	91	1.127	-1.0500
323	90	1.249	-1.0850
324	89	1.127	-1.1200
325	88	1.249	-1.1550
326	87	1.127	-1.1900
327	86	1.249	-1.2250
328	85	1.127	-1.2600
329	84	1.249	-1.2950
330	83	1.127	-1.3300
331	82	1.249	-1.3650
332	81	1.127	-1.4000
333	80	1.249	-1.4350
334	79	1.127	-1.4700
335	78	1.249	-1.5050
336	77	1.127	-1.5400
337	76	1.249	-1.5750
338	75	1.127	-1.6100
339	74	1.249	-1.6450
340	73	1.127	-1.6800
341	72	1.249	-1.7150
342	71	1.127	-1.7500
343	70	1.249	-1.7850
344	69	1.127	-1.8200
345	68	1.249	-1.8550
346	67	1.127	-1.8900
347	66	1.249	-1.9250
348	65	1.127	-1.9600
349	64	1.249	-1.9950
350	63	1.127	-2.0300
351	62	1.249	-2.0650
352	61	1.127	-2.1000
353	60	1.249	-2.1350
354	59	1.127	-2.1700
355	58	1.249	-2.2050
356	57	1.127	-2.2400
357	56	1.249	-2.2750
358	55	1.127	-2.3100
359	54	1.249	-2.3450
360	53	1.127	-2.3800
361	52	1.249	-2.4150
362	51	1.127	-2.4500
363	50	1.249	-2.4850
364	49	1.127	-2.5200
365	48	1.249	-2.5550
366	47	1.127	-2.5900
367	46	1.249	-2.6250
368	45	1.127	-2.6600
369	44	1.249	-2.6950
370	43	1.127	-2.7300
371	42	1.249	-2.7650
372	41	1.127	-2.8000
373	40	1.249	-2.8350
374	39	1.127	-2.8700
375	38	1.249	-2.9050
376	37	1.127	-2.9400
377	36	1.249	-2.9750
378	35	1.127	-3.0100
379	34	1.249	-3.0450
380	33	1.127	-3.0800
381	32	1.249	-3.1150
382	31	1.127	-3.1500
383	30	1.249	-3.1850
384	29	1.127	-3.2200

PADTYPE : BUMP SIZE 86u x 35um			
GATE OUTPUTS 35um pitch			
PAD NO.	PAD NAME	X [mm]	Y [mm]
385	28	1.249	-3.2550
386	27	1.127	-3.2900
387	26	1.249	-3.3250
388	25	1.127	-3.3600
389	24	1.249	-3.3950
390	23	1.127	-3.4300
391	22	1.249	-3.4650
392	21	1.127	-3.5000
393	20	1.249	-3.5350
394	19	1.127	-3.5700
395	18	1.249	-3.6050
396	17	1.127	-3.6400
397	16	1.249	-3.6750
398	15	1.127	-3.7100
399	14	1.249	-3.7450
400	13	1.127	-3.7800
401	12	1.249	-3.8150
402	11	1.127	-3.8500
403	10	1.249	-3.8850
404	9	1.127	-3.9200
405	8	1.249	-3.9550
406	7	1.127	-3.9900
407	6	1.249	-4.0250
408	5	1.127	-4.0600
409	4	1.249	-4.0950
410	3	1.127	-4.1300
411	2	1.249	-4.1650
412	1	1.127	-4.2000
413	DUMMY	1.249	-4.2350
414	DUMMY	1.127	-4.2700
415	DUMMY	1.2490	-4.3050
—	**Alignment Mark1**	0.9705	-4.5495

3. PIN FUNCTIONS

(1/5)

Symbol	Pin Name	Pad No.	I/O	Function
O_1 to O_{241}	Driver output pins	388 to 148	Output	Scan signal output pins that drive the gate electrode of a TFT-LCD. The status of each output pin changes in synchronization with the rising edge of shift clock CLK. The output voltage of the driver is V_{DD1} to V_B.
CLK	Shift clock input	139	Input	Shift clock input for the internal shift resistor. The contents of internal shift resistor are shifted at the rising edge of CLK. Connect to GCLK pin of source driver.
STVR, STVL	Start pulse input/output pin	136, 137	I/O	Input/output pin of the internal shift resistor. Start pulse signal (output from GSTB pin of source driver) is read at the rising edge of shift clock CLK and a scan signal is output from the driver output pin. The valid level of the STVR/STVL pin is determined by the setting of STVSEL. When STVSEL = L, the pulse becomes low level at the falling edge of the 240th shift clock CLK and high level at falling edge of the 241st clock.
OE_1	Enable input	140	Input	If the level selected by OE1SEL is input, the driver output is fixed to low level. (When OE1SEL = L the driver output is fixed to low level if a low level is input.) However, the shift resistor is not cleared. And, output enable actuation is asynchronous in the clock. Connect to GOE1 pin of source driver.
OE_2	Enable input	141	Input	If the level selected by OE2SEL is input, the driver output is fixed to high level. (When OE2SEL = L the driver output is fixed to low level if a high level is input.) However, the shift resistor is not cleared. And, output enable actuation is asynchronous in the clock. Connect to GOE2 pin of source driver.
R,/L	Shift direction switching input	25	Input	Shift direction switching input pin of the internal shift register. R,/L = 1 (right shift): STVR →O_1 →O_2 ··· O_{239} →O_{240} →STVL R,/L = 0 (left shift): STVL →O_{241} →O_{240} ··· O_2 →O_1 →STVR
FRM	Frame signal input	129	Input	Input frame reverse signals. Connect to GFRAME pin of source driver.
GCS	Chip select input	133	Input	<IFSEL = 0> To input chip select signals. Connect to GCS pin of source driver. <IFSEL = 1> Leave open.
GCL	Serial clock input	134	Input	<IFSEL = 0> To input serial clock signals. Connect to GCL pin of source driver. <IFSEL = 1> Leave open.

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Symbol	Pin Name	Pad No.	I/O	Function
GDA	Serial data input	135	Input	<IFSEL = 0> To input serial data signals. Connect to GDA pin of source driver. <IFSEL = 1> Leave open.
/GRESET	Reset input	132	Input	Reset input pin. Connect to /GRESET pin of source driver. If /GRESET is made low, the serial interface is initialized (the register values are not initialized). A reset operation is executed according to the level of the /GRESET signal. Be sure to execute a reset using this pin at power application.
VCIN	Common pulse input	130	Input	To input common pulse. Connect to VCOUT3 pin of source driver. Fix this pin to low when not using it.
DCCLK	Clock input for DC/DC converter	138	Input	To input the external clock for the DC/DC converter. This pin is valid only when CLS0 = 1 and CLS1 = 1. Other settings cause this pin to be pulled down to low level, so in these cases, leave open.
VGD	Power supply input for DC/DC converter	114 to 116	Input	Reference voltage input pins for V_{DD1}, V_{SS1} to V_{SS4} boost. Connect to any of V_{DD2}, V_R or V_S.
V_R	Power supply output for DC/DC converter	111 to 113	Output	Positive power supply voltage output for the DC/DC converter. The V_R output voltage can be changed by setting VRSEL0 to VRSEL2.
V_S	Positive power output supply for driver	118 to 123	Output	Positive power supply voltage output for source driver. The V_S output voltage can be changed by setting VSEL0 to VSEL2.
MVS	External resistor input	117	Input	Any output voltage can be set by connecting an external resistor. <EXRV = 0> Leave open. <EXRV = 1> Connect to external resistor.
C_1^+, C_1^- C_2^+, C_2^- C_3^+, C_3^- C_4^+, C_4^- C_5^+, C_5^- C_6^+, C_6^-	Capacitor connect pin for boost	80 to 83, 76 to 79, 72 to 75, 68 to 71, 63, 64, 61, 62, 59, 60, 57, 58, 55, 56, 53, 54, 51, 52, 49, 50	–	To connect booster for DC/DC converter. The recommended values of the capacitance and tolerance of each capacitor are shown below. Capacitance : C1, C2: 1 μF, C3 to C6: 0.47 μF Tolerance : 10 V
V_{DD1}	DC/DC converter output	65 to 67	Output	Boost voltage of DC/DC converter (V_R x2 or x3). The boost step number of V_{DD1} is selected according to how the external capacitor is connected. The boost reference voltage can be set using VGD. Refer to the function of VGD pin.
V_{DD2}	DC/DC converter output	84 to 87	Output	Boost voltage of DC/DC converter (VDC x2 or x3). The boost step number for V_{DD2} can be set using VCD2.
V_{SS2}	DC/DC converter output	46 to 48	Output	Boost voltage of DC/DC converter (V_R x-1 or x-2). The boost step number of V_{SS2} is selected according to how the external capacitor is connected. The boost reference voltage can be set using VGD. Refer to the function of VGD pin.

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Symbol	Pin Name	Pad No.	I/O	Function
V_{SS3}	DC/DC converter output	40 to 42, 143	Output	Boost voltage of DC/DC converter (V_R x-1 or x-2). The boost step number of V_{SS2} is selected according to how the external capacitor is connected. The boost reference voltage can be set using VGD. Refer to VGD pin function.
V_{SS4}	DC/DC converter output	43 to 45	Output	Boost voltage output of DC/DC converter (VDC x-1).
COMH	Common high level output	34, 35	Output	<COMON = 1> High level of common voltage is output. The voltage level changes accordance with DA0 to DA7 and CDA0 to CDA7. <COMON = 1> Leave open when not using it.
COML	Common low level output	32, 33	Output	<COMON = 1> Low level of common voltage is output. The voltage level changes accordance with DA0 to DA7 and CDA0 to CDA7. <COMON = 0> Leave open when not using it.
VCOM	Common output	29 to 31	Output	<COMON = 1> The common voltage synchronized with the VCIN input is output. Connect to common pin of panel. <COMON = 0> Leave open when not using it.
VM	Gate output low level select voltage	36, 37	Output	Gate output low level select voltage synchronized with the VCIN input is output. Connect to V_B pin.
V_B	Driver negative voltage	38, 39	Input	Negative voltage of output buffer. This is the input pin of the liquid crystal driver negative voltage. Connect to V_M pin.
IFSEL	I/F selection	26	Input	The serial I/F input switching pin. <IFSEL = 0> Serial I/F input. The DCON, RGONR, VCD2, VMS, FS0, FS2, CLS0, RGON, VSEL, EXRV, ACS0, SCN0, SCN0, SCN2, PUPT0, DUPF0 pins should be left open. <IFSEL = 1> Control pin input. The GCS, GCL, GDA pins should be left open.
DCON	DC/DC converter control	128	Input	<IFSEL = 0> Leave open. (Internal resistors are valid.) <IFSEL = 1> The DC/DC converter ON/OFF control signal is input. Connect to the DCON pin of the source driver. <DCON = 0> DC/DC converter OFF. <DCON = 1> DC/DC converter ON.
RGONR	V_R regulator control	19	Input	<IFSEL = 0> Leave open. (Internal resistors are valid.) <IFSEL = 1> The V_R regulator ON/OFF control signal is input. <RGONR = 0> V_R regulator OFF. <RGONR = 1> V_R regulator ON.
VCD2	V_{DD2} boost selection	126	Input	<IFSEL = 0> Leave open. (Internal resistors are valid.) <IFSEL = 1> The V_{DD2} boost step number select pin. <VCD2 = 0> V_{DD2} = VDC x 2. <VCD2 = 1> V_{DD2} = VDC x 3.

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Symbol	Pin Name	Pad No.	I/O	Function
VMS	V_{DD2} boost selection	18	Input	<IFSEL = 0> Leave open. (Internal resistors are valid.) <IFSEL = 1> V_{DD2} boost mode select pin. <VMS = 0> V_{DD2}: single boost mode <VMS = 1> V_{DD2}: dual boost mode
VCOMIN	VCOM center voltage input	28	Input	VCOM center voltage input pin. Leave open when COMSEL = 0. <COMSEL = 0> Internal D/A is valid. <COMSEL = 1> VCOMIN input voltage is valid.
FS0	V_{DD2} boost frequency selection in scan mode	17	Input	<IFSEL = 0> Leave open. (Internal resistors are valid.) <IFSEL = 1> V_{DD2} boost frequency select pin in scan mode <FS0 = 0 > f_{OSC}/2 <FS0 = 0 > f_{OSC}/4
FS2	V_{DD1}, V_{SS2} to V_{SS4} boost frequency selection in scan mode	16	Input	<IFSEL = 0> Leave open. (Internal resistors are valid.) <IFSEL = 1> V_{DD1}, V_{SS2} to V_{SS4} boost frequency select pin in scan mode. <FS2 = 0 > f_{OSC}/2 <FS2 = 1, > f_{OSC}/4
CLS0	DC/DC OSC frequency selection	15	Input	<IFSEL = 0> Leave open. (Internal resistors are valid.) <IFSEL = 1> Select pin of the OSC oscillation frequency for DC/DC converter. <CLS0 = 0> f_{OSC} = 20 kHz, DCCLK: Open <CLS0 = 1> External CK input mode
RGON	V_S regulator control	127	Input	<IFSEL = 0> Leave open. (Internal resistors are valid.) <IFSEL = 1> The V_S regulator ON/OFF control signal is input. Connect this pin to the RGON pin of the source driver. <RGON = 0> V_S regulator OFF. <RGON = 1> V_S regulator ON.
VSEL	V_S regulator voltage selection	14	Input	<IFSEL = 0> Leave open. (Internal resistors are valid.) <IFSEL = 1> Select pin of output voltage for V_S regulator. <VSEL = 1> V_S = 4 V <VSEL = 0> V_S = 5 V
EXRV	V_S regulating resistor selection	13	Input	<IFSEL = 0> Leave open. (Internal resistors are valid.) <IFSEL = 1> Select pin of external resistor for V_S regulator. <EXRV = 0> Internal resistor setting mode. <EXRV = 1> Any output voltage can be set by connecting MVS to an external resistor
ACS0	Amp. current selection in scan mode	12	Input	<IFSEL = 0> Leave open. (Internal resistors are valid.) <IFSEL = 1> Amp. current select pin in scan mode. <ACS0 = 0> Amp. current = 5 μA. <ACS0 = 1> Amp. current = 15 μA

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Symbol	Name	Pad No.	I/O	Function
SCN0, SCN1, SCN2	Gate scan selection	11, 10, 9	Input	<IFSEL = 0> Leave open. (Internal resistors are valid.) <IFSEL = 1> Select pin of Gate scan order. <SCN0 = 1, SCN1 = 1, SCN2 = 1> MODE1 <SCN0 = 1, SCN1 = 1, SCN2 = 0> MODE2 <SCN0 = 1, SCN1 = 0, SCN2 = 1> MODE3 <SCN0 = 1, SCN1 = 0, SCN2 = 0> MODE4 <SCN0 = 0, SCN1, SCN2 = x> MODE5
PUPT0	Setting pin of DC/DC converter power on time	8	Input	<IFSEL = 0> Leave open. (Internal resistors are valid.) <IFSEL = 1> This pin sets the rising time of V_{DD1}, V_{DD2}, V_{SS2} to V_{SS4} at DC/DC converter power on time.
DUPF0	Operating frequency setting pin at DC/DC converter power on	7	Input	<IFSEL = 0> Leave open. (Internal resistors are valid.) <IFSEL = 1> This pin sets the operating frequency at DC/DC converter power on time. <DUPT0 = 0> f_{OSC}/8 <DUPT0 = 0> f_{OSC}/16
VMON	Stand-by current reduction control pin	22	Input	The standby current reduction control pin. <VMON = PVSS3> Normal mode A quiescent current of about 0.5 μA is consumed in standby mode. When the V_{CC1} voltage drops, the driver output pins are fixed to ALL-High. <VMON = PVCC1> Standby current reduction mode Makes the quiescent current consumed in standby mode 0. When the V_{CC1} voltage drops, the driver output pins are undefined.
TESTOUT1	VREF reference voltage output	5	Output	The V_{REF} voltage measurement pin. Leave open.
V_{DC}	DC/DC converter reference voltage	93 to 100	–	Reference voltage input pin for DC/DC converter.
V_{CC1}	Logic reference voltage	101 to 104	–	2.7 V ± 5% LS: level shifter reference voltage input pins.
V_{SS1}	Ground	105 to 110	–	Connect to the system ground.
PV_{CC1}	Pull-up voltage	6, 24, 125	–	Pull-up voltage for mode setting pins.
PV_{SS1}	Pull-down voltage	20, 27, 131	–	Pull-down voltage for mode setting pins.
TESTIN1, TESTIN2	TEST input pin	4, 3	Input	Test input pins. Leave open.
TESTOUT2	TEST output pin	2	Output	Test output pin. Leave open.
PV_{SS3}	Pull-down voltage	21	–	Pull-down voltage for mode setting pin.
DUMMY	Dummy	1, 23, 92, 124, 142, 144 to 147, 389 to 391	–	Dummy data

4. COMMAND

4.1 Command List

										Data bit							
7	6	5	4	3	2	1	0	Register		7	6	5	4	3	2	1	0
0	0	0	1	1	0	0	0	R24	DC/DC operation setting		RGONR	VS4ON	VS3ON	VS2ON	VD2ON	VD1ON	DCON
0	0	0	1	1	0	0	1	R25	DC/DC step setting				VRSEL2	VRSEL1	VRSEL0	VMS	VCD2
0	0	0	1	1	0	1	0	R26	DC/DC oscillation setting		FUP	CLS1	CLS0	FS3	FS2	FS1	FS0
0	0	0	1	1	0	1	1	R27	Regulator output setting		ACS1	ACS0	EXRV	VSEL2	VSEL1	VSEL0	RGON
0	0	0	1	1	1	0	0	R28	LPM setting		LACS1	LACS0	LFS3	LFS2	LFS1	LFS0	LPM
0	0	0	1	1	1	0	1	R29	Gate scan setting			OE2SEL	OE1SEL	STVSEL	SCN2	SCN1	SCN0
0	0	0	1	1	1	1	0	R30	Gate mode setting				COMHI	COMSEL	COMON	NLINE2	NLINE1
0	0	0	1	1	1	1	1	R31	Common amplitude setting	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	0	1	0	0	0	0	0	R32	Common center setting	CDA7	CDA6	CDA5	CDA4	CDA3	CDA2	CDA1	CDA0
0	0	1	0	0	0	0	1	R33	DC/DC power on setting			PONM	PON	DUPF1	DUPF0	PUPT1	PUPT0
0	0	1	0	0	0	1	0	R34	Reset								RES

4.2 Command Description

Reset the internal data at power application by inputting a low level to the /GRESET pin.

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Resistor	Bit	Symbol	Reset	Functions	Descriptions
R24	D0	DCON	0	DC/DC converter control	Control ON/OFF of DC/DC converter <DCON = 0> DC/DC converter OFF <DCON = 1> DC/DC converter ON
	D1	VD1ON	0	V_{DD1} boost control	Control ON/OFF of V_{DD1} boost <VD1ON = 0> V_{DD1} boost OFF <VD1ON = 1> V_{DD1} boost ON
	D2	VD2ON	0	V_{DD2} boost control	Control V_{DD2} boost ON/OFF <VD2ON = 0> V_{DD2} boost OFF <VD2ON = 1> V_{DD2} boost ON
	D3	VS2ON	0	V_{SS2} boost control	Control V_{SS2} boost ON/OFF. <VS2ON = 0> V_{SS2} boost OFF <VS2ON = 1> V_{SS2} boost ON
	D4	VS3ON	0	V_{SS3} boost control	Control V_{SS3} boost ON/OFF. <VS3ON = 0> V_{SS3} boost OFF <VS3ON = 1> V_{SS3} boost ON
	D5	VS4ON	0	V_{SS4} boost control	Control V_{SS4} boost ON/OFF. <VS4ON = 0> V_{SS4} boost OFF <VS4ON = 1> V_{SS4} boost ON
	D6	RGONR	0	V_R regulator control	Control ON/OFF of V_R regulator <RGON = 0> V_R regulator OFF <RGON = 1> V_R regulator ON

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Resistor	Bit	Symbol	Reset	Functions	Descriptions
R25	D0	VCD2	0	V_{DD2} boost selection	Select the number of V_{DD2} boost step (x2/x3) <VCD2 = 0> $V_{DD2} = V_{DC}$ x 2 <VCD2 = 1> $V_{DD2} = V_{DC}$ x 3
	D1	VMS	1	V_{DD2} boost mode selection	Select V_{DD2} boost mode <VMS = 0> V_{DD2} = Single boost mode <VMS = 1> V_{DD2} = Dual boost mode
	D2 D3 D4	VRSEL0 VRSEL1 VRSEL2	1 0 1	V_R regulator output voltage selection	Select output voltage of V_R regulator. When IFSEL = 1, V_R is fixed to 5 V. <VRSEL0 = 0, VRSEL1 = 0, VRSEL2 = 0> V_R = 3 V <VRSEL0 = 1, VRSEL1 = 0, VRSEL2 = 0> V_R = 3.5 V <VRSEL0 = 0, VRSEL1 = 1, VRSEL2 = 0> V_R = 4 V <VRSEL0 = 1, VRSEL1 = 1, VRSEL2 = 0> V_R = 4.5 V <VRSEL0 = 0, VRSEL1 = 0, VRSEL2 = 1> V_R = 4.75 V <VRSEL0 = 1, VRSEL1 = 0, VRSEL2 = 1> V_R = 5 V <VRSEL0 = 0, VRSEL1 = 1, VRSEL2 = 1> V_R = 5.25 V <VRSEL0 = 1, VRSEL1 = 1, VRSEL2 = 1> V_R = 5.5 V
R26	D0 D1	FS0 FS1	1 0	V_{DD2} boost frequency selection in scan mode	Select V_{DD2} boost frequency in scan mode. When IFSEL = 1, FS1 is fixed to 0. <FS0 = 0, FS1 = 0> f_{OSC}/2 <FS0 = 1, FS1 = 0> f_{OSC}/4 <FS0 = 0, FS1 = 1> f_{OSC}/8 <FS0 = 1, FS1 = 1> f_{OSC}/16
	D2 D3	FS2 FS3	1 0	V_{DD1}, V_{SS2} to V_{SS4} boost frequency selection in scan mode	Select V_{DD1}, V_{SS2} to V_{SS4} boost frequency in scan mode. When IFSEL = 1, FS3 is fixed to 0. <FS2 = 0, FS3 = 0> f_{OSC}/2 <FS2 = 1, FS3 = 0> f_{OSC}/4 <FS2 = 0, FS3 = 1> f_{OSC}/8 <FS2 = 1, FS3 = 1> f_{OSC}/16
	D4 D5	CLS0 CLS1	1 0	DC/DC OSC frequency selection	Select oscillation frequency of OSC for DC/DC converter. When IFSEL = 1, CLS1 is fixed to 1 <CLS0 = 0, CLS1 = 0> f_{OSC} = 15 KHz, DCCLK: Open <CLS0 = 1, CLS1 = 0> f_{OSC} = 20 KHz, DCCLK: Open <CLS0 = 0, CLS1 = 1> f_{OSC} = 30 KHz, DCCLK: Open <CLS0 = 1, CLS1 = 1> External CK input mode
	D6	FUP	0	Switching of DC/DC OSC frequency	Select oscillation frequency of OSC for DC/DC converter. When IFSEL = 1, the frequency is fixed to f_{OSC}. <FUP = 0> f_{OSC} <FUP = 1> f_{OSC} x 2

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Resistor	Bit	Symbol	Reset	Functions	Descriptions
R27	D0	RGON	0	V_S regulator control	Control ON/OFF of V_S regulator <RGON = 0> V_S regulator OFF <RGON = 1> V_S regulator ON
	D1 D2 D3	VSEL0 VSEL1 VSEL2	1 0 1	V_S regulator output voltage selection	Select the output voltage of V_S regulator. VSEL0 = 0: V_S = 5 V, VSEL = 1, V_S = 4 V when IFSEL = 1. <VSEL0 = 0, VSEL1 = 0, VSEL2 = 0> V_S = 3 V <VSEL0 = 1, VSEL1 = 0, VSEL2 = 0> V_S = 3.5 V <VSEL0 = 0, VSEL1 = 1, VSEL2 = 0> V_S = 4 V <VSEL0 = 1, VSEL1 = 1, VSEL2 = 0> V_S = 4.5 V <VSEL0 = 0, VSEL1 = 0, VSEL2 = 1> V_S = 4.75 V <VSEL0 = 1, VSEL1 = 0, VSEL2 = 1> V_S = 5 V <VSEL0 = 0, VSEL1 = 1, VSEL2 = 1> V_S = 5.25 V <VSEL0 = 1, VSEL1 = 1, VSEL2 = 1> V_S = 5.5 V
	D4	EXRV	0	V_S regulator resistor selection	Select external resistor of V_S regulator. <EXRV = 0> Internal resistor mode <EXRV = 1> Connect external resistor to MVS and set any level of voltage
	D5 D6	ACS0 ACS1	0 0	Amp. current selection in scan mode	Select Amp. current of V_R and V_S regulators in scan mode. When IFSEL = 1, ACS1 is fixed to 0. <ACS0 = 0, ACS1 = 0> Amp. current = 5 μA <ACS0 = 0, ACS1 = 1> Amp. current = 10 μA <ACS0 = 1, ACS1 = 0> Amp. current = 15 μA <ACS0 = 1, ACS1 = 1> Amp. current = 30 μA
R28	D0	LPM	0	Low power mode control	Control in low power mode. When IFSEL = 1, LPM is fixed to 0. <LPM = 0> Scan mode <LPM = 1> Low power mode
	D1 D2	LFS0 LFS1	0 0	V_{DD2} boost frequency selection in low power mode	Select boost frequency of V_{DD2} in low power mode. <LFS0 = 0, LFS1 = 0> f_{OSC}/8 <LFS0 = 0, LFS1 = 1> f_{OSC}/16 <LFS0 = 1, LFS1 = 0> f_{OSC}/32 <LFS0 = 1, LFS1 = 1> f_{OSC}/64
	D3 D4	LFS0 LFS1	0 0	V_{DD1}, V_{SS2} to V_{SS4} boost frequency selection in low power mode	Select boost frequency of V_{DD1}, V_{SS2} to V_{SS4} in low power mode. <LFS0 = 0, LFS1 = 0> f_{OSC}/8 <LFS0 = 1, LFS1 = 0> f_{OSC}/16 <LFS0 = 0, LFS1 = 1> f_{OSC}/32 <LFS0 = 1, LFS1 = 1> f_{OSC}/64
	D5 D6	LACS0 LACS1	0 0	Amp. current selection in low power mode	Select Amp. current in low power mode. <LACS0 = 0, LACS1 = 0> Amp. current = 1.25 μA <LACS0 = 0, LACS1 = 1> Amp. current = 2.5 μA <LACS0 = 1, LACS1 = 0> Amp. current = 5 μA <LACS0 = 1, LACS1 = 1> Amp. current = 7.5 μA

Resistor	Bit	Symbol	Reset	Functions	Descriptions
R29	D0 D1 D2	SCN0 SCN1 SCN2	1 1 1	Gate scan selection	Select scan order of gate scan. <SCN0 = 1, SCN1 = 1, SCN2 = 1> MODE1 <SCN0 = 1, SCN1 = 1, SCN2 = 0> MODE2 <SCN0 = 1, SCN1 = 0, SCN2 = 1> MODE3 <SCN0 = 1, SCN1 = 0, SCN2 = 0> MODE4 <SCN0 = 0, SCN1, SCN2 = X> MODE5
	D3	STVSEL	0	Start pulse input/output valid level selection	Select start pulse input/output valid level to STVR/STVL. But there is no pin to select start pulse input/output valid level. When IFSEL = H (When using control pins), low-fixed is valid. Refer to **4.3 Command Setting Values When IFSEL = H (When Using Control Pins).** <STVSEL= 0> Low level is valid. <STVSEL= 1> High level is valid.
	D4	OE1SEL	0	OE1 valid level selection	Select valid level of OE1. But there is no pin to select valid level of OE1. When IFSEL = H (When using control pins), low-fixed is valid. Refer to **4.3 Command Setting Values When IFSEL = H (When Using Control Pins).** <OE1SEL = 0> OE1 = Low, gate output OFF <OE1SEL = 1> OE1 = High, gate output OFF
	D5	OE2SEL	0	OE2 valid level selection	Select valid level of OE2. There is no pin to select valid level of OE1. When IFSEL = H (When using control pins), low-fixed is valid. Refer to **4.3 Command Setting Values When IFSEL = H (When Using Control Pins).** <OE2SEL = 0> OE2 = Low, gate output OFF <OE2SEL = 1> OE2 = High, gate output OFF
R30	D0 D1	NLINE1 NLINE2	1 1	Gate mode selection	Select 1-line skip, 2-line skip or N frame inversion of a gate scan. When IFSEL = 1, this is fixed to normal mode. <NLINE1 = 1, NLINE2 = 1> Normal mode <NLINE1 = 1, NLINE2 = 0> 1-line skip mode <NLINE1 = 0, NLINE2 = 1> 2-line skip mode <NLINE1 = 0, NLINE2 = 0> N frame inversion
	D2	COMON	0	COM output control	Control ON/OFF of COM output. When IFSEL = 1, COMON is fixed to 0. <COMON = 0> COM_AMP, COM output OFF <COMON = 1> COM_AMP, COM output ON
	D3	COMSEL	0	VCOM center input selection	Select VCOM center voltage input. <COMSEL = 0> Internal D/A is valid. <COMSEL = 1> VCOMIN input voltage is valid.
	D4	COMHI	0	VCOM output selection	Select VCOM output. <COMHI = 0> VCOM = Hi-Z <COMHI = 1> VCOM = Output

Resistor	Bit	Symbol	Reset	Functions	Descriptions
R31	D0 to D7	DA0 to DA7	0	COM amplitude control	Control COM output amplitude using 8-bit D/A.
R32	D0 to D7	CDA0 to CDA7	0	COM center level control	Control COM output center level using 8-bit D/A.
R33	D0 D1	PUPT0 PUPT1	0 1	Setting of DC/DC converter power on time	This pin sets the ON time of V_{DD1} and 2, V_{SS2} to V_{SS4}, and RGON when the DC/DC converter is started up. This setting is only valid when PONM = 1. When IFSEL = 1, PUPT1 is fixed to 0.
	D2 D3	DUPF0 DUPF1	1 0	Setting of DC/DC converter power on operating frequency	This pin sets the DC/DC operating frequency when the DC/DC converter is started up. When IFSEL = 1, DUPF1 is fixed to 0. <DUPF0 = 0, DUPF1 = 0> $f_{OSC}/8$ <DUPF0 = 1, DUPF1 = 0> $f_{OSC}/16$ <DUPF0 = 0, DUPF1 = 1> $f_{OSC}/32$ <DUPF0 = 1, DUPF1 = 1> $f_{OSC}/64$
	D4	PON	0	Switching DC/DC converter startup operating frequency	This pin selects the V_{DD1}, V_{DD2}, V_{SS2} to V_{SS4} rising operating frequency when the DC/DC converter is started up. Only PONM = 0 is valid. <PON = 0> Normal operation <PON = 1> Power on operation startup operation
	D5	PONM	1	DC/DC operation startup operating selection	Select internal/external sequence of DC/DC converter power on operation. <PONM = 0> External sequence <PONM = 1> Internal sequence
R34	D0	RES	–	Command reset	This is the command reset function. A command reset must always be executed after power application. All contents of registers are initialized. This bit is automatically cleared after command reset execution (RES = 1). It is therefore not necessary to set this bit to 0 again by software (to select normal operation). Also, because this bit changes from 1 to 0 very quickly following a command reset, it is not necessary to leave any time before setting the next command after setting a command reset. <RES = 0> Normal operation <RES = 1> Command reset

4.3 Command Setting Values When IFSEL = H (When Using Control Pins)

(1/2)

Register	Bit	Symbol	Setting value	Conditions
R24	D0	DCON	–	DCON control pin is valid.
	D1	VD1ON	1	<VD1ON = 1> V_{DD1} boost ON
	D2	VD2ON	1	<VD2ON = 1> V_{DD2} boost ON
	D3	VS2ON	1	<VS2ON = 1> V_{SS2} boost ON
	D4	VS3ON	1	<VS3ON = 1> V_{SS3} boost ON
	D5	VS4ON	0	<VS4ON = 0> V_{SS4} boost OFF
	D6	RGONR	–	RGONR control pin is valid.
R25	D0	VCD2	–	VCD2 control pin is valid.
	D1	VMS	–	VMS control pin is valid.
	D2	VRSEL0	1	<VRSEL0 = 1, VRSEL1 = 0, VRSEL2 = 1 > V_R = 5 V
	D3	VRSEL1	0	
	D4	VRSEL2	1	
R26	D0	FS0	–	FS0 control pin is valid.
	D1	FS1	0	<FS0 = 0> fosc/2, <FS0 = 1> fosc/4
	D2	FS2	–	FS2 control pin is valid.
	D3	FS3	0	<FS2 = 0> fosc/2, <FS2 = 1> fosc/4
	D4	CLS0	–	CLS1 control pin is valid.
	D5	CLS1	1	<CLS0 = 0> fosc = 30 kHz, <CLS0 = 1> External
	D6	FUP	0	<FUP = 0> fosc
R27	D0	RGON	–	RGON control pin is valid.
	D1	VSEL0	–	VSEL control pin is valid.
	D2	VSEL1	–	<VSEL = 0> V_S = 5 V
	D3	VSEL2	–	<VSEL = 1> V_S = 4 V
	D4	EXRV	–	EXRV control pin is valid.
	D5	ACS0	–	ACS0 control pin is valid.
	D6	ACS1	0	<ACS0 = 0> Current = 5 μA, <ACS0 = 1> Current = 15 μA
R28	D0	LPM	0	<LPM = 0> Scan mode
	D1, D2	LFS0, LFS1	0,1	<LFS0 = 0, LFS1 = 1> fosc/32
	D3, D4	LFS0, LFS1	0,1	<LFS2 = 0, LFS3 = 1> fosc/32
	D5, D6	LACS0, LACS1	0,1	<LACS0 = 0, LACS1 = 1> Amp. current = 2.5 μA
R29	D0	SCN0	–	SCN0 control pin is valid
	D1	SCN1	–	SCN1 control pin is valid
	D2	SCN2	–	SCN2 control pin is valid
	D3	OE1SEL	0	<STVSEL = 0> low-level is valid
	D4	VMON	0	<OE1SEL = 0> OE1 = low-level, gate output OFF
	D5	COMON	0	<OE2SEL = 0> OE2 = low-level, gate output ON

Remark When IFSEL = H (when using the control pins), the GCS, GCL, and GDA pins are pulled down to low level, so be sure to leave these pins open.

When IFSEL = L (when using the serial interface), DCON, RGONR, VCD2, VMS, FS0, FS2, CLS0, RGON, VSEL, EXRV, ACS0, SCN0, SCN1, SCN2, PUPT0, DUPF0 pins should be left open.

(2/2)

Register	Bit	Symbol	Setting value	Conditions
R30	D0	NLINE1	1	<NLINE = 1, NLINE2 = 1> normal mode
	D1	NLINE2	1	
	D2	COMON	0	<COMON = 0> COM_AMP, COM output OFF
R31	D0 to D7	DA0 to DA7	0	<DA0 to DA7> 0
R32	D0 to D7	CDA0 to CDA7	0	<CDA0 to CDA7> 0
R33	D0	PUPT0	–	PUPT0 control pin is valid
	D1	PUPT1	0	<PUPT0 = 0> RGONR = 128/fosc <PUPT0 = 1> RGONR = 256/fosc
	D2	DUPF0	–	DUPF0 control pin is valid
	D3	DUPF1	0	<DUPF0 = 0> RGONR = fosc/8 <DUPF0 = 1> RGONR = fosc/16
	D4	PON	1	<PON = 1> Internal sequence
	D5	PONM	1	<PONM = 1> Internal sequence
R34	D0 to D7	RES	0	<RES = 0> Normal operation

Remark When IFSEL = H (when using the control pins), the GCS, GCL, and GDA pins are pulled down to low level, so be sure to leave these pins open.
When IFSEL = L (when using the serial interface), DCON, RGONR, VCD2, VMS, FS0, FS2, CLS0, RGON, VSEL, EXRV, ACS0, SCN0, SCN1, SCN2, PUPT0, DUPF0 pins should be left open.

5. MODE DESCRIPTION

5.1 Output Mode and Gate Scan Selection

Scan MODE	R,/L	Scan direction	Dummy output	Cascade output
MODE1	H	1→240, 241	241	240
	L	241→2,1	1	2
MODE2	H	1→121 • 241→123, 122	122	123
	L	122→241 • 121→2, 1	1	2
MODE3	H	1→161 • 241→163, 162	162	163
	L	162→241 • 161→2, 1	1	2
MODE4	H	1→201, 241→203, 202	202	203
	L	202→241 • 201→2, 1	1	2
MODE5	H	1, 241, 2, 240, 3, 239…..118, 124, 119, 123, 120, 122, 121	121	122
	L	121, 122, 120, 123, 119, 124…..4, 239, 3, 240, 2, 241, 1	1	241

2 Fields

Scan MODE	R,/L	Scan direction	Dummy output	Cascade output
MODE1	H	1, 3, 5…235, 237, 239, 241 • 2, 4, 6…236, 238, 240	241	240
	L	241, 239, 237,…7, 5, 3, 1 • 240, 238, 236…6, 4, 2	1	2
MODE2	H	1, 3, 5…117, 119, 121 • 240, 238, 236…128, 126, 124, 122, • 2, 4, 6…116, 118, 120 • 241, 239, 237…127, 125, 123	122	123
	L	122, 124, 126,…236, 238, 240 • 121, 119, 117…7, 5, 3, 1, • 123, 125, 127…237, 239, 241 • 120, 118, 116…6, 4, 2	1	2
MODE3	H	1, 3, 5…157, 159, 161 • 240, 238, 236…168, 166, 164, 162 • 2, 4, 6…156, 158, 160 • 241, 239, 237…160, 158, 156…6, 4, 2	162	163
	L	122, 124, 126,…236, 238, 240 • 121, 119, 117…7, 5, 3, 1, • 163, 165, 167…237, 239, 241 • 160, 158, 156…6, 4, 2	1	2
MODE4	H	1, 3, 5…197, 199, 201 • 240, 238, 236…208, 206, 204, 202, • 2, 4, 6…196, 198, 200 • 241, 239, 237…207, 205, 203	202	203
	L	202, 204, 206…236, 238, 240 • 201, 199, 197…7, 5, 3, 1, • 203, 205, 207…237, 239, 241 • 200, 198, 196…6, 4, 2	1	2

3 Fields

Scan MODE	R,/L	Scan direction	Dummy output	Cascade output
MODE1	H	1, 4, 7…232, 235, 238, 241 • 2, 5, 8…233, 236, 239 • 3, 6, 9…234, 237, 240	241	240
	L	241, 238, 235,…10, 7, 4, 1 • 240, 237, 234…9, 6, 3 • 239, 236, 233…8, 5, 2	1	2
MODE2	H	1, 4, 7…115, 118, 121 • 239, 236, 233…131, 128, 125, 122, • 2, 5, 8…113, 116, 119 • 241, 238, 235…130, 127, 124 • 3, 6, 9…114, 117, 120 • 240, 237, 234,…129, 126, 123	122	123
	L	122, 125, 128,…233, 236, 239 • 121, 118, 115…10, 7, 4, 1, • 123, 126, 129…234, 237, 240 • 120, 117, 114…9, 6, 3 • 124, 127, 130…235, 238, 241 • 119, 116, 113…8, 5, 2	1	2
MODE3	H	1, 4, 7…154, 157, 160, 240, 237, 234…171, 168, 165, 162, • 2, 5, 8…155, 158, 161 • 239, 236, 233…170, 167, 164 • 3, 6, 9…153, 156, 159 • 241, 238, 235…169, 166, 163	162	163
	L	162, 165, 168,…234, 237, 240 • 160, 157, 154…10, 7, 4, 1, • 163, 166, 169…235, 238, 241 • 159, 156, 153…9, 6, 3 • 164, 167, 170…233, 236, 239 • 161, 158, 155..8, 5, 2	1	2
MODE4	H	1, 4, 7…193, 196, 199 • 241, 238, 235…211, 208, 205, 202, • 2, 5, 8…194, 197, 200 • 240, 237, 234…210, 207, 204 • 3, 6, 9…195, 198, 201 • 239, 236, 233…209, 206, 203	202	203
	L	202, 205, 208…235, 238, 241 • 199, 196, 193…10, 7, 4, 1, • 203, 206, 209…2337, 236, 239 • 201, 198, 195…9, 6, 3 • 204, 207, 210…234, 240, 200 • 197, 194…8, 5, 2	1	2

N-frame reverse

Scan MODE	R,/L	FMR	Scan direction	Dummy output	Cascade output
MODE1	H	1	1→240, 241	241	240
		0	241→2, 1 (reverse operation)	241	2
	L	1	241→2, 1	1	2
		0	1→240,241(reverse operation)	1	240

5.2 DC/DC OSC Frequency Selection

CLS0	CLS1	OSC oscillation frequency for DC/DC converter	DCCLK
0	0	fosc = 15 kHz	Open
1	0	fosc = 20 kHz	Open
0	1	fosc = 30 kHz	Open
1	1	fosc = External CK	External CK input

5.3 DC/DC Converter Control

DCON	VD1ON	VD2ON	VS2ON	VS3ON	VS4ON	State of V_{DD1}, V_{DD2}, V_{SS2}, V_{SS3}, V_{SS4}
0	x	x	x	x	x	V_{DD1}, V_{DD2}, V_{SS2}, V_{SS3}, V_{SS4} : OFF
1	0	–	–	–	–	V_{DD1} : OFF
1	1	–	–	–	–	V_{DD1} : ON
1	–	0	–	–	–	V_{DD2} : OFF
1	–	1	–	–	–	V_{DD2} : ON
1	–	–	0	–	–	V_{SS2} : OFF
1	–	–	1	–	–	V_{SS2} : ON
1	–	–	–	0	–	V_{SS3} : OFF
1	–	–	–	1	–	V_{SS3} : ON
1	–	–	–	–	0	V_{SS4} : OFF
1	–	–	–	–	1	V_{SS4} : ON

5.4 V_{DD2} Boost Selection

VCD2	V_{DD2}
0	VDC x 2 boost
1	VDC x 3 boost

5.5 Division Ratio Selection of the DC/DC Converter at Power on

PONM	PON	DUPF0	DUPF1	Division ratio of the DC/DC converter OSC frequency
1	x	0	0	Internal sequence : OSC = f_{osc}/8
1	x	1	0	Internal sequence : OSC = f_{osc}/16
1	x	0	1	Internal sequence : OSC = f_{osc}/32
1	x	1	1	Internal sequence : OSC = f_{osc}/64
0	1	0	0	External sequence : OSC = f_{osc}/8
0	1	1	0	External sequence : OSC = f_{osc}/16
0	1	0	1	External sequence : OSC = f_{osc}/32
0	1	1	1	External sequence : OSC = f_{osc}/64
0	0	x	x	Normal mode

5.6 DC/DC Converter Power on Time Selection

PONM	PON	PUPT0	PUPT1	VD2ON	RGONR	VS2 to VS4 ON	VD1ON	
1	x	0	0	16/f_{osc}	128/f_{osc}	1.5 x 128/f_{osc}	2.5 x 128/f_{osc}	Internal sequence
1	x	1	0	16/f_{osc}	256/f_{osc}	1.5 x 256/f_{osc}	2.5 x 256/f_{osc}	Internal sequence
1	x	0	1	16/f_{osc}	512/f_{osc}	1.5 x 512/f_{osc}	2.5 x 512/f_{osc}	Internal sequence
1	x	1	1	16/f_{osc}	1024/f_{osc}	1.5 x 1024/f_{osc}	2.5 x 1024/f_{osc}	Internal sequence
0	1	x	x	External input	External input	External input	External input	External sequence
0	0	x	x					Normal mode

5.7 Division Ratio Selection of the DC/DC Converter OSC Frequency

LPM	FS0	FS1	FS2	FS3	LFS0	LFS1	LFS2	LFS3	Division ratio of the DC/DC converter OSC frequency
0	0	0	x	x	x	x	x	x	V_{DD2} : f_{OSC}/2
0	1	0	x	x	x	x	x	x	V_{DD2} : f_{OSC}/4
0	0	1	x	x	x	x	x	x	V_{DD2} : f_{OSC}/8
0	1	1	x	x	x	x	x	x	V_{DD2} : f_{OSC}/16
0	x	x	0	0	x	x	x	x	V_{DD1}, V_{SS2}, V_{SS3}, V_{SS4} : f_{OSC}/2
0	x	x	1	0	x	x	x	x	V_{DD1}, V_{SS2}, V_{SS3}, V_{SS4} : f_{OSC}/4
0	x	x	0	1	x	x	x	x	V_{DD1}, V_{SS2}, V_{SS3}, V_{SS4} : f_{OSC}/8
0	x	x	1	1	x	x	x	x	V_{DD1}, V_{SS2}, V_{SS3}, V_{SS4} : f_{OSC}/16
1	x	x	x	x	0	0	x	x	V_{DD2} : f_{OSC}/8
1	x	x	x	x	1	0	x	x	V_{DD2} : f_{OSC}/16
1	x	x	x	x	0	1	x	x	V_{DD2} : f_{OSC}/32
1	x	x	x	x	1	1	x	x	V_{DD2} : f_{OSC}/64
1	x	x	x	x	x	x	0	0	V_{DD1}, V_{SS2}, V_{SS3}, V_{SS4} : f_{OSC}/8
1	x	x	x	x	x	x	0	0	V_{DD1}, V_{SS2}, V_{SS3}, V_{SS4} : f_{OSC}/16
1	x	x	x	x	x	x	1	1	V_{DD1}, V_{SS2}, V_{SS3}, V_{SS4} : f_{OSC}/32
1	x	x	x	x	x	x	1	1	V_{DD1}, V_{SS2}, V_{SS3}, V_{SS4} : f_{OSC}/64

5.8 Amp. Current Selection

RGON, RGONR	LPM	ACS0	ACS1	LACS0	LACS1	V_R condition	V_S condition	State of Circuit Current
0	x	x	x	x	x	Hi-Z	Hi-Z	Amp, CS Power OFF
1	0	0	0	x	x	Output	Output	Amp. current = 5 μA
1	0	0	1	x	x	Output	Output	Amp. current = 10 μA
1	0	1	0	x	x	Output	Output	Amp. current = 15 μA
1	0	1	1	x	x	Output	Output	Amp. current = 30 μA
1	1	x	x	0	0	Output	Output	Amp. current = 1.25 μA
1	1	x	x	0	1	Output	Output	Amp. current = 2.5 μA
1	1	x	x	1	0	Output	Output	Amp. current = 5.0 μA
1	1	x	x	1	1	Output	Output	Amp. current = 7.5 μA

5.9 V_R Regulator Selection Output

Register Control

RGONR	VRSEL0	VRSEL1	VRSEL2	V_R
0	x	x	x	V_R regulator OFF (V_R = Hi-Z)
1	0	0	0	3 V : Internal resistor connection
1	1	0	0	3.5 V : Internal resistor connection
1	0	1	0	4 V : Internal resistor connection
1	1	1	0	4.5 V : Internal resistor connection
1	0	0	1	4.75 V : Internal resistor connection
1	1	0	1	5 V : Internal resistor connection
1	0	1	1	5.25 V : Internal resistor connection
1	1	1	1	5.5 V : Internal resistor connection

Pin Control

RGONR	V_R
0	V_R regulator OFF (V_R = Hi-Z)

1	5 V : Internal resistor connection

5.10 V_S Regulator Selection Output

Register Control

RGON	EXRV	VSEL0	VSEL1	VSEL2	MV$_S$ condition	V_S
0	x	x	x	x	Hi-Z	V_S regulator OFF (V_S = Hi-Z)
1	1	x	x	x	Amp.-input	External resistor connection
1	0	0	0	0	Hi-Z	3 V : Internal resistor connection
1	0	1	0	0	Hi-Z	3.5 V : Internal resistor connection
1	0	0	1	0	Hi-Z	4 V : Internal resistor connection
1	0	1	1	0	Hi-Z	4.5 V : Internal resistor connection
1	0	0	0	1	Hi-Z	4.75 V : Internal resistor connection
1	0	1	0	1	Hi-Z	5 V : Internal resistor connection
1	0	0	1	1	Hi-Z	5.25 V : Internal resistor connection
1	0	1	1	1	Hi-Z	5.5 V : Internal resistor connection

Pin Control

RGON	VSEL	V_R
0	x	V_S regulator OFF (V_S = Hi-Z)
1	0	5 V : Internal resistor connection
1	1	4 V : Internal resistor connection

5.11 Control of VM Output Control, VCOM Output

COMON	COMHI	DAC, COM_AMP	VCOM
0	x	OFF	Hi-Z
1	0	ON	Hi-Z
1	1	ON	Output

5.12 VCOM Output Frequency Adjustment

Only values in the range of 3Fh to C8h (0.9822 to 3.1372V) can be set. Do not set values in the range of 00h to 3Eh or C9h to FFh.

DA_0	DA_1	DA_2	DA_3	DA_4	DA_5	DA6	DA7	Amplitude adjustment D/A output	VCOM output amplitude
0	0	0	0	0	0	0	0	0.0000 V	0.0000 Vpp
1	0	0	0	0	0	0	0	0.0157 V	0.0314 Vpp
0	1	0	0	0	0	0	0	0.0314 V	0.0627 Vpp
1	1	0	0	0	0	0	0	0.0471 V	0.0941 Vpp
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0	0	1			1	1	1	3.9529 V	7.9058 Vpp
1	0	1			1	1	1	3.9686 V	7.9372 Vpp
0	1	1			1	1	1	3.9843 V	7.9686 Vpp
1	1	1			1	1	1	4.0000 V	8.0000 Vpp

Remark The range in which the VCOM output amplitude can be varied is restricted by the output voltage of V_{DD2} and V_{SS4}.

5.13 VCOM Output Center Adjustment

Only values in the range of 00h to 80h (0 to 2.0078 V) can be set. Do not set values in the range of 81h to FFh.

CDA_0	CDA_1	CDA_2	CDA_3	CDA_4	CDA_5	CDA6	CDA7	Center adjustment D/A output	VCOM output center
0	0	0	0	0	0	0	0	0.0000 V	0.0000 V
1	0	0	0	0	0	0	0	0.0157 V	0.0157 V
0	1	0	0	0	0	0	0	0.0314 V	0.0314 V
1	1	0	0	0	0	0	0	0.0471 V	0.0471 V
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0	0	1			1	1	1	3.9529 V	3.9529 V
1	0	1			1	1	1	3.9686 V	3.9686 V
0	1	1			1	1	1	3.9843 V	3.9843 V
1	1	1			1	1	1	4.0000 V	4.0000 V

Remark The range in which the VCOM output center can be varied is restricted by the output voltage of V_{DD2} and V_{SS4}.

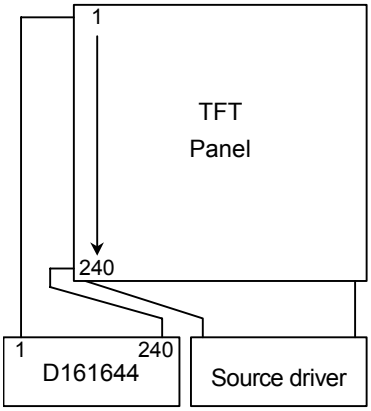
5.14 VCOM Center Adjustment Selection

COMSEL	VCOM center adjustment
0	Internal D/A is valid.
1	VCOMIN input voltage is valid.

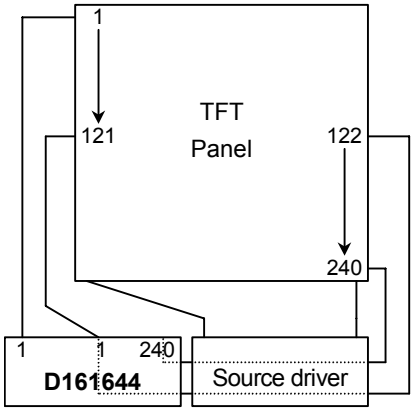
6. PANNEL CONNECTION

[MODE1]

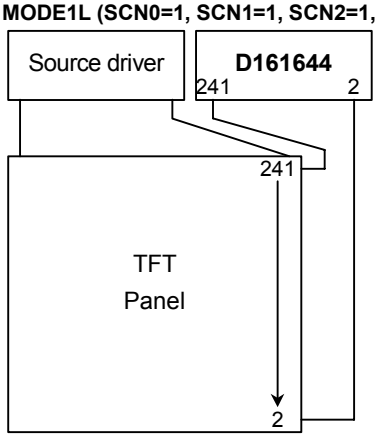
MODE1R (SCN0=1, SCN1=1, SCN2=1, R,/L=1)



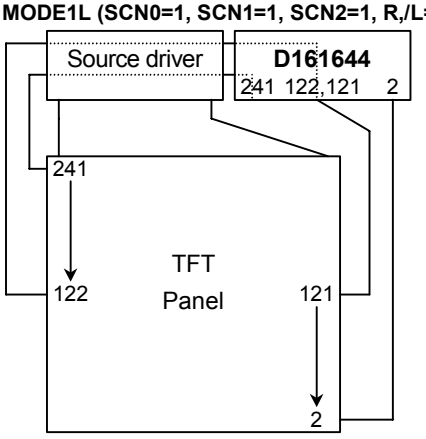
MODE1R (SCN0=1, SCN1=1, SCN2=1, R,/L=1)



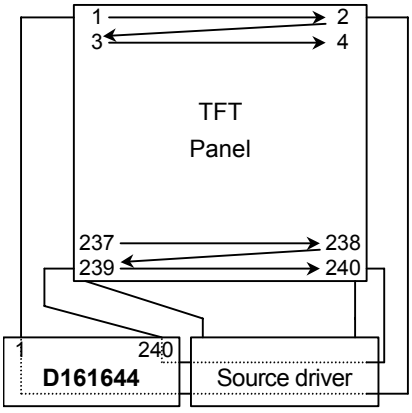
MODE1L (SCN0=1, SCN1=1, SCN2=1, R,/L=0)



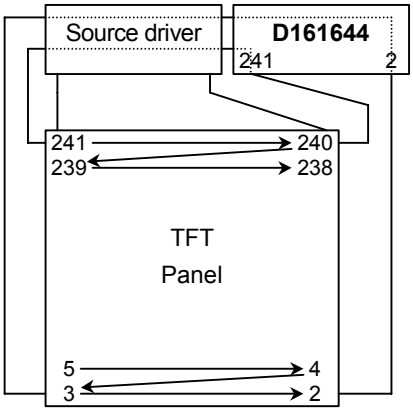
MODE1L (SCN0=1, SCN1=1, SCN2=1, R,/L=0)



MODE1R (SCN0=1, SCN1=1, SCN2=1, R,/L=1)

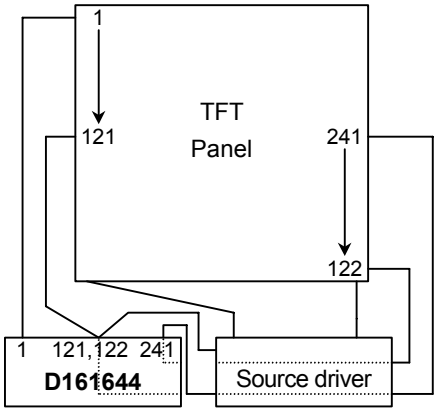


MODE1L (SCN0=1, SCN1=1, SCN2=1, R,/L=0)

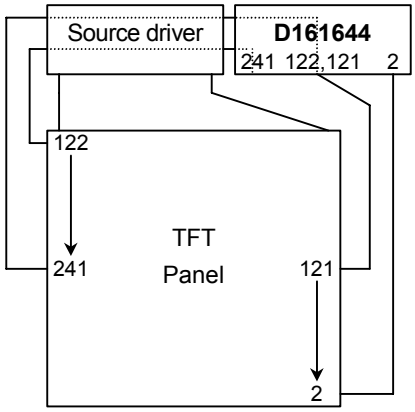


[MODE2]

MODE2R (SCN0=1, SCN1=1, SCN2=0, R,/L=1)

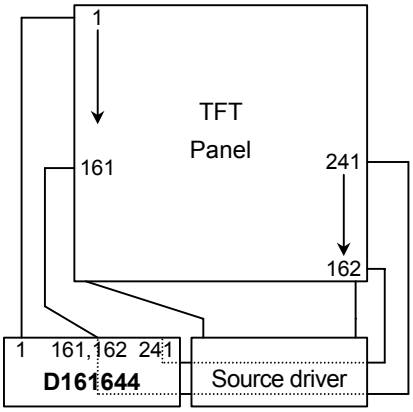


MODE2L (SCN0=1, SCN1=1, SCN2=0, R,/L=0)

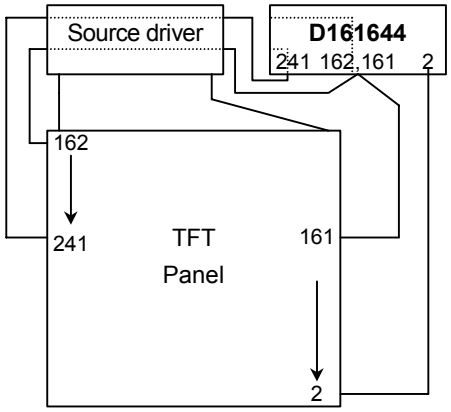


[MODE3]

MODE3R (SCN0=1, SCN1=0, SCN2=1, R,/L=1)

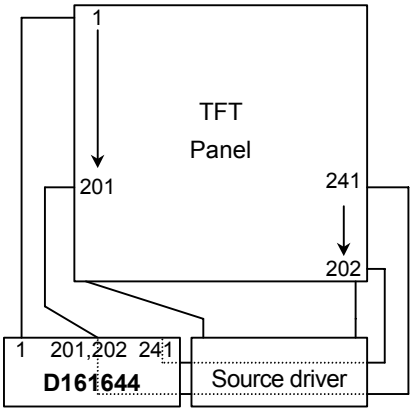


MODE3L (SCN0=1, SCN1=0, SCN2=1, R,/L=0)

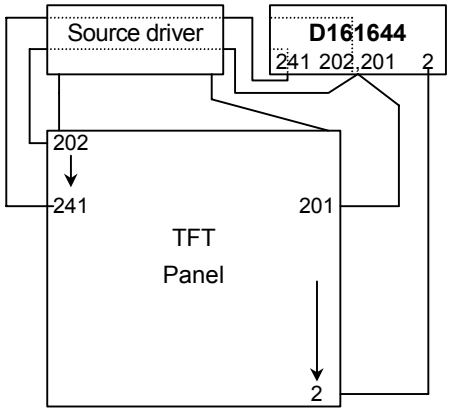


[MODE4]

MODE4R (SCN0=1, SCN1=0, SCN2=0, R,/L=1)



MODE4L (SCN0=1, SCN1=0, SCN2=0, R,/L=0)



7. CONNECT TO SOURCE DRIVER

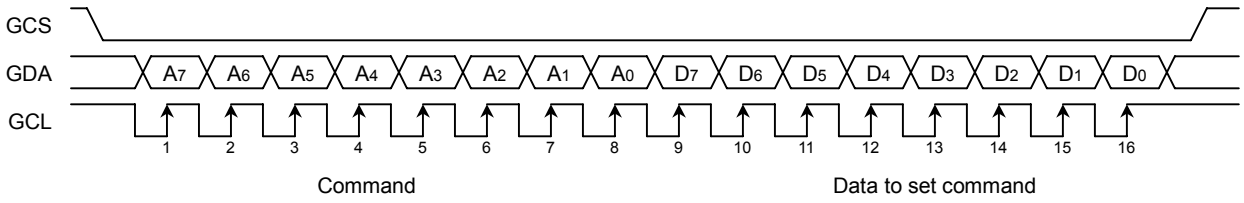
T.B.D. (To be determined.)

8. SERIAL INTERFACE

When the serial interface has been selected, if the chip is active (GCS1 = L), serial data input (GDA) and serial clock input (GCL) can be received. Serial data is read from D7 and then from D6 to D0 on the rising edge of the serial clock, via the serial input pin. This data is synchronized on the eighth serial clock's rising edge and is then converted to parallel data for processing.

The serial interface signal chart is shown below.

Figure 8-1. Serial Interface Signal Chart



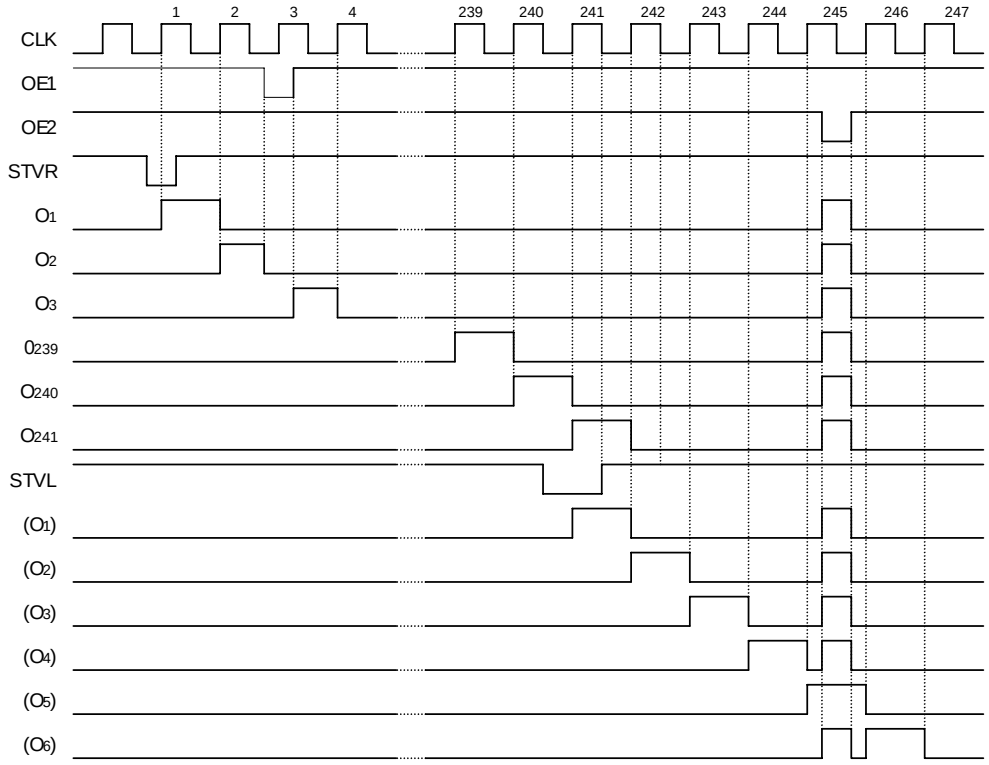
Note that odd bytes of data received after the reset command is input are recognized as commands, and even bytes of data are recognized as data values to be set to commands.

Remarks 1. The shift register and counter are reset to their initial values when the chip select signal is inactive. Do not set the chip select signal to inactive between transmission of an 8-bit command and transmission of the 8-bit data set for the command.

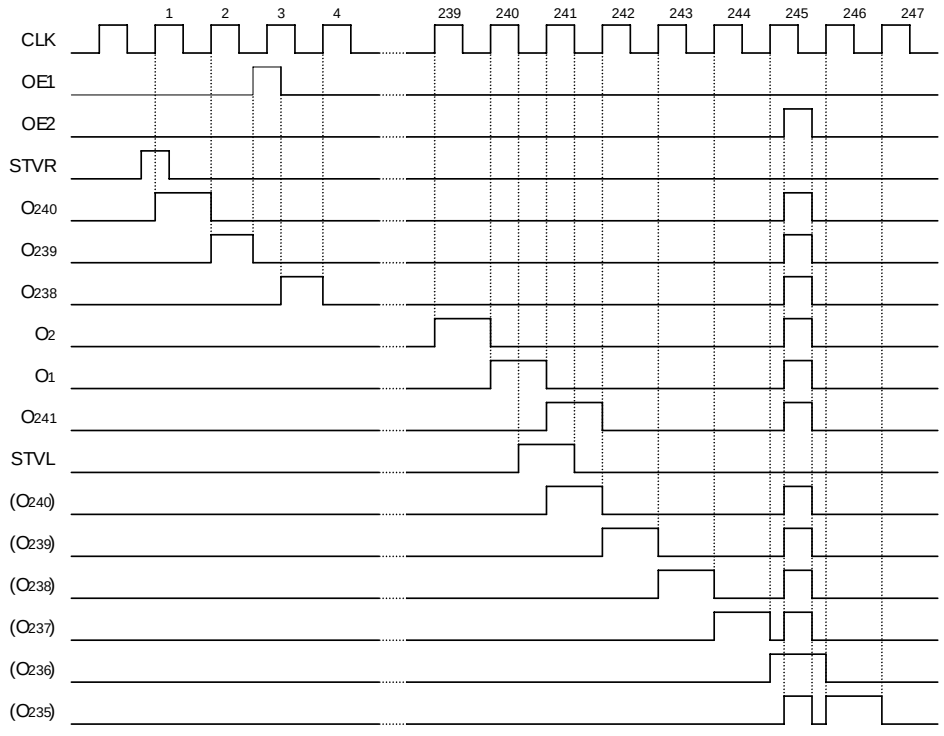
2. When using GCL wiring, take care concerning the possible effects of terminating reflection and noise from external sources. We recommend checking operation with the actual device.

9. TIMING CHARTS (MODE1 : SCN0 = H, SCN1 = H, SCN2 = H)

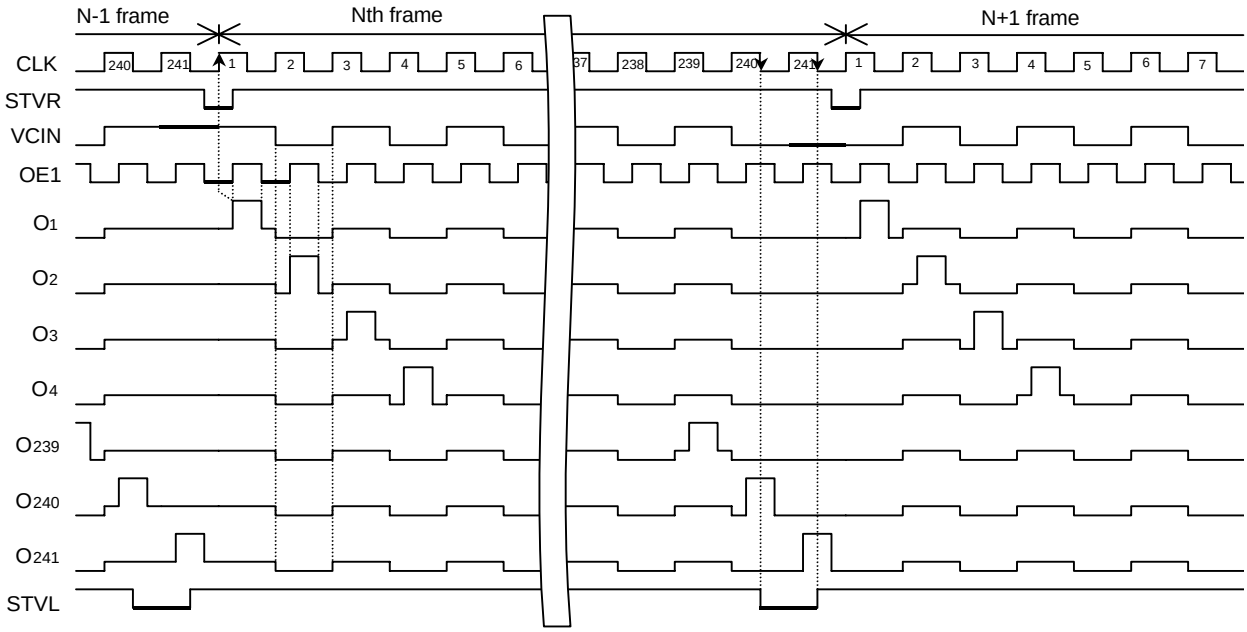
R,/L = H, STVSEL = 0, OE1SEL = 0, OE2SEL = 0



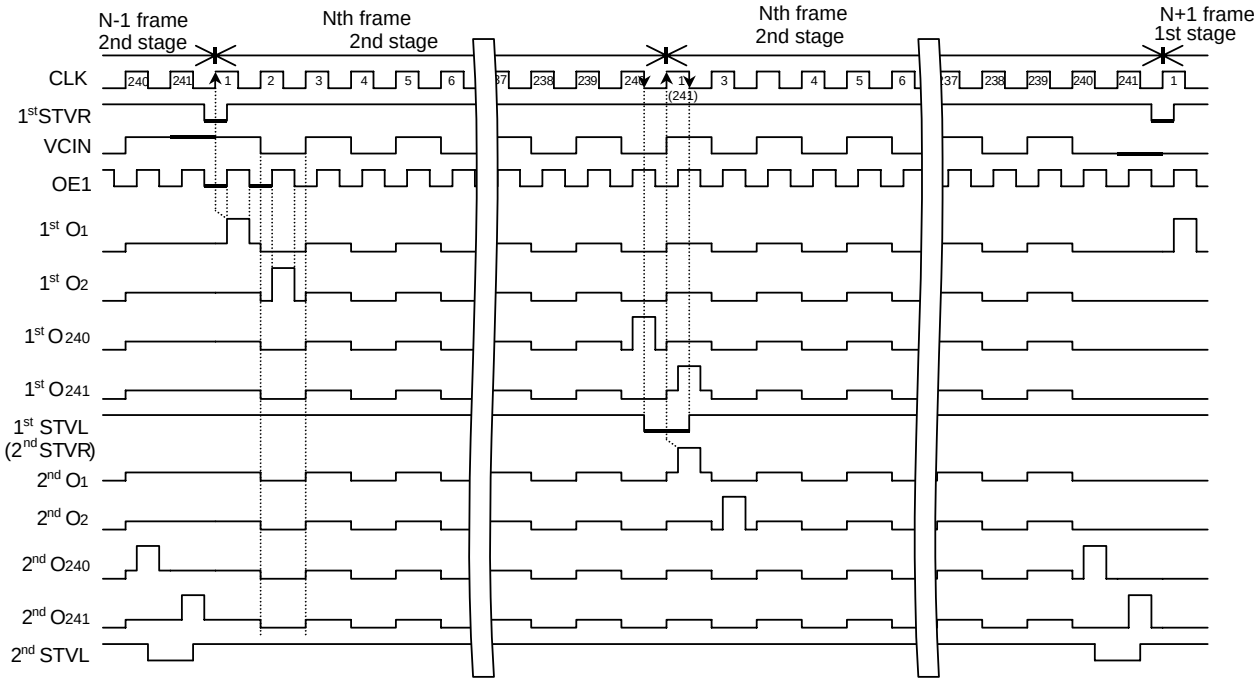
R,/L = L, STVSEL = 1, OE1SEL = 1, OE2SEL = 1



When V_B level selection signal is input (in standalone mode) R,/L = H, STVSEL = 0, OE1SEL = 0, OE2SEL = 0



When V_B level selection signal is input (in 2-stage cascade connection mode) R,/L = H, STVSEL = 0, OE1SEL = 0, OE2SEL = 0



10. POWER ON/OFF SEQUENCE

10.1 Power on sequence

There are three ways to turn on the power of the uPD161644A:

<When power supply is controlled by serial interface>

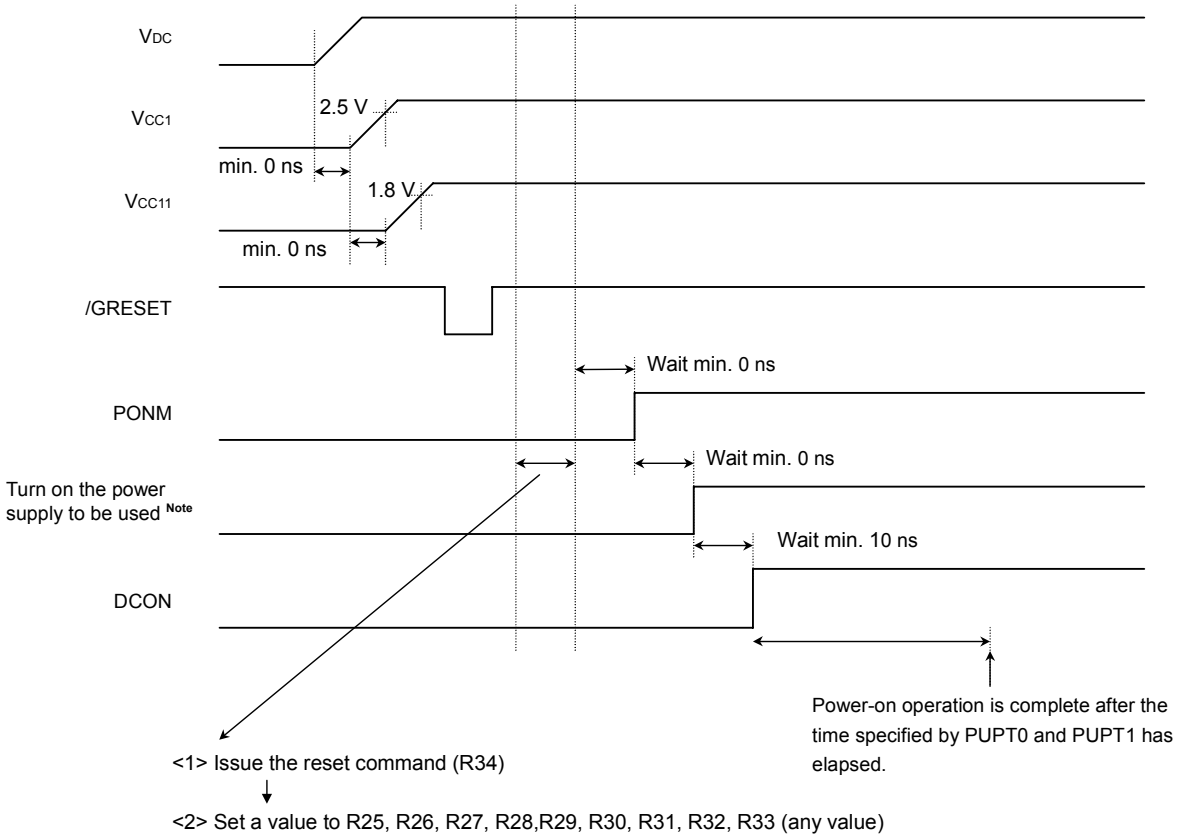
- Simple sequence
- Command control sequence

<When power supply is controlled by pin>

- Simple sequence

(1) Power supply control via serial interface (simple sequence)

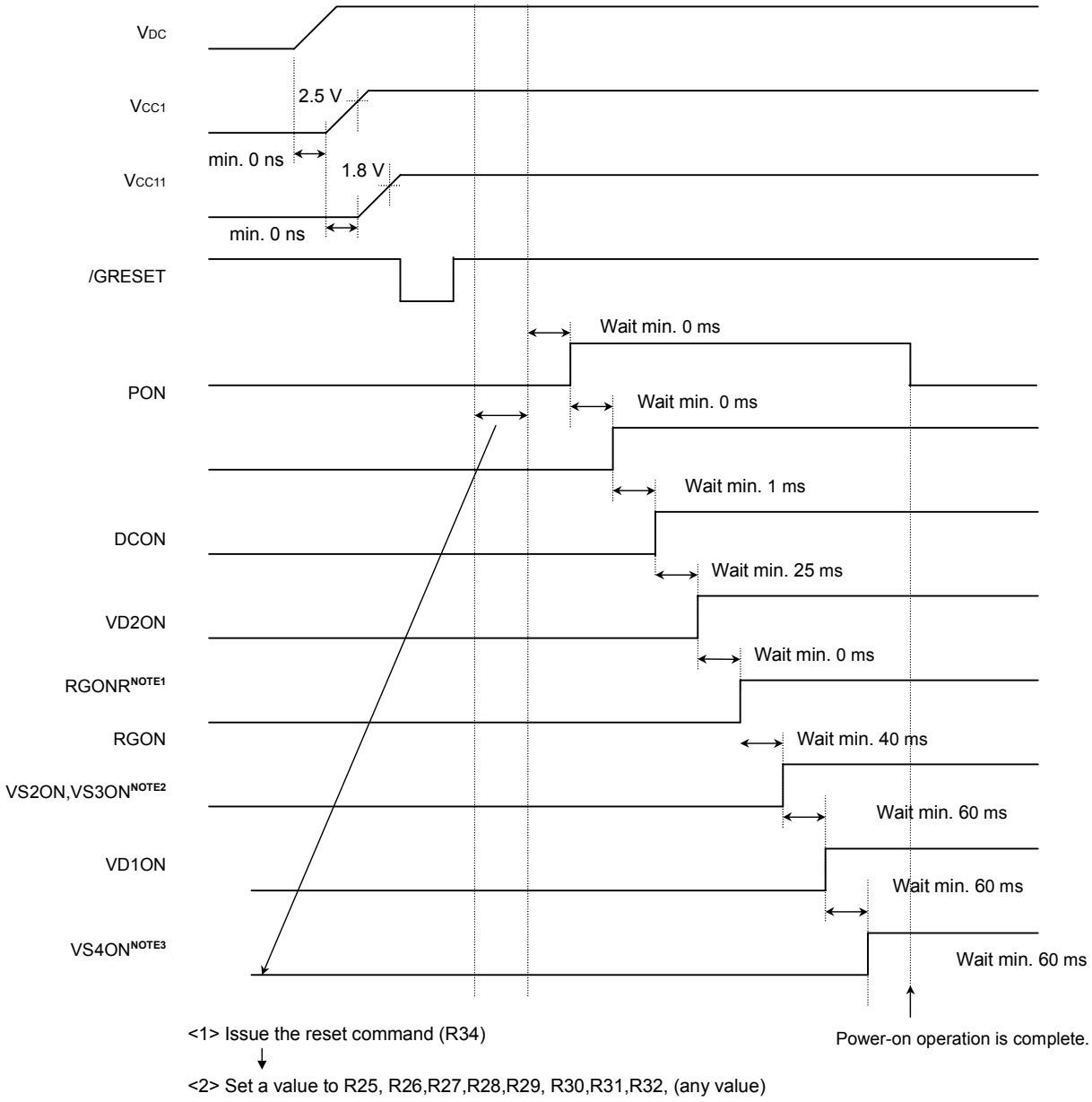
Control /GRESET pin and each command of PONM, VD2ON, RGONR, RGON, VS2ON, VS3ON, VD1ON, and DCON using the following sequence, after applying power to VDC, V_{CC1}, and V_{CC11}.



Note Turn on the power supply to be used among VD2ON, RGONR, RGON, VS2ON, VS3ON, and VD1ON.

(2) Power control by serial interface (command control sequence)

Control /GRESET pin and each command of PON, DCON, VD2ON, RGONR, RGON, VS2ON, VS3ON, VD1ON, and VS4ON after power on of VDC, V_{CC1}, V_{CC11} as shown below.



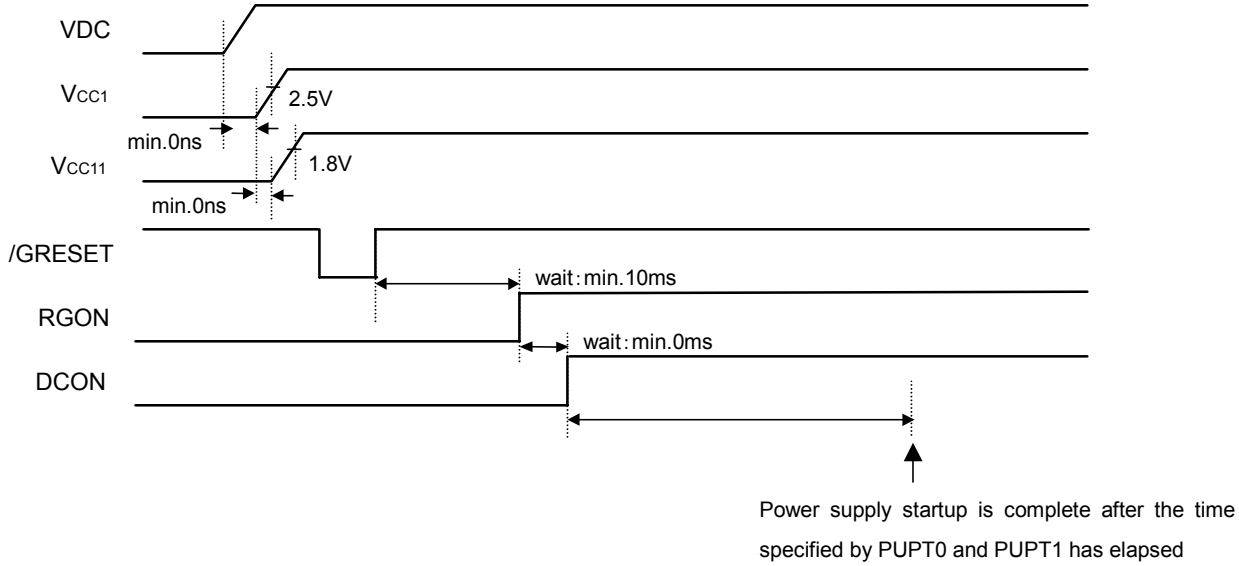
Notes 1. This pin only needs to be controlled when the VCOM is used.

2. VS2ON only needs to be controlled when V_{SS2} is used.

3. This pin only needs to be controlled when V_R amplifier is used.

(3) Power control by pins (simple sequence)

Control each pin of /GRESET, RGON, and DCON after power on of VDC, V_{CC1}, V_{CC11} as shown below.



Notes 1. When using RGON, pull it up to the high level by wiring the RGONR pin.

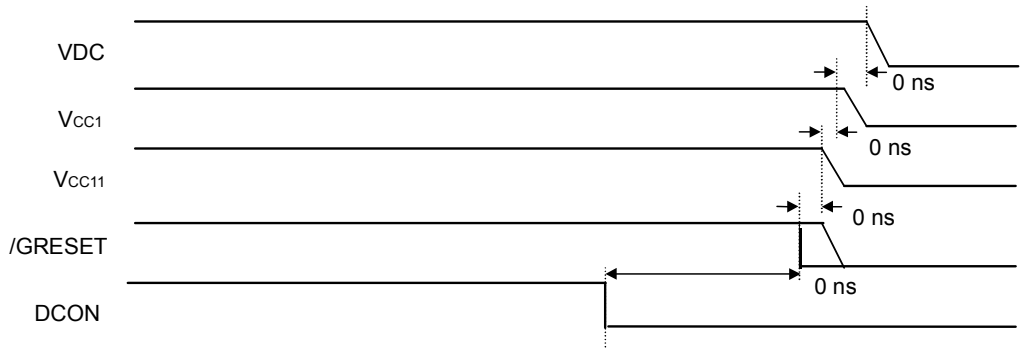
2. When using V_{SS4}, pull it up to the high level by wiring the COMON pin.

10.2 Power off sequence

When turning the power off, turn off the pins and commands used for control simultaneously, both when performing control via the serial interface and via the pins.

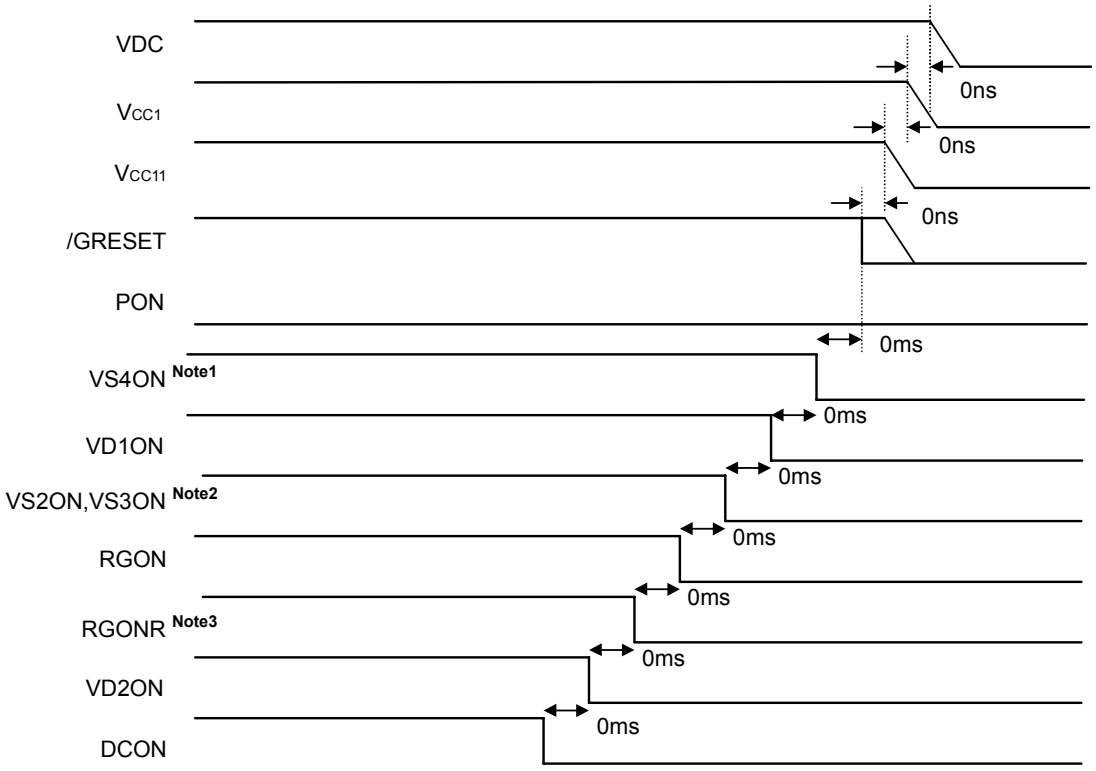
(1) Power control by serial interface (Simplified sequence)]

Control DCON pin as shown below.



(2) Power control by serial interface (Command control sequence)

Control each pin of /GRESET, RGON, and DCON as shown below.



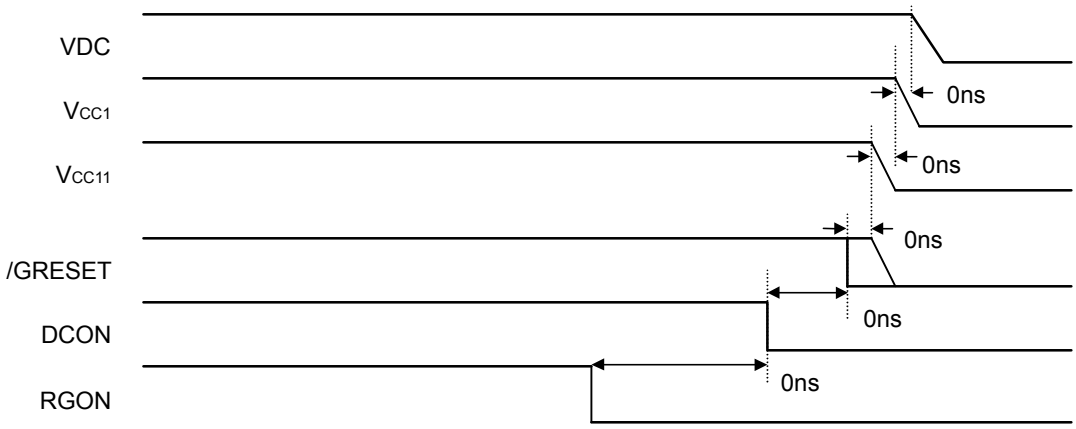
Notes 1. This pin only needs to be controlled when the VCOM is used.

2. VS2ON only needs to be controlled when V_{SS2} is used.

3. This pin only needs to be controlled when V_R amplifier is used.

(3) Power control by pins (Simplified sequence)

Control each pin of /GRESET, RGON, and DCON as shown below.



Remarks 1. When using RGON, pull it up to the high level by wiring the RGONR pin.

2. When using V_{SS4}, pull it up to the high level by wiring the COMON pin.

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC1}	−0.5 to +4.0	V
Supply Voltage	V_{DC}	−0.5 to +4.0	V
Supply Voltage	V_{SS3}	V_{DD1}−42 V to +0.5	V
Supply Voltage	V_{DD1}-V_{SS3}	−0.5 to +42	V
Input Voltage Note 1	V_I	−0.5 to V_{CC1}+0.5	V
Input Current Note 1	I_I	±1	mA
Output Current Note 2	I_{O1}	±10	mA
Output Current Note 3	I_{O2}	+10	mA
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Notes 1. CLK, STVR, STVL, R,/L, OE_1, OE_2, GCS, GCL, GDA, DCCLK, VCIN, DCON, RGON, VCD2, /GRESET, IFSEL, EXRV, SCN0, SCN1

2. STVR, STVL, VM, VCOM

3. V_S

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC1}		2.5	2.7	3.3	V
Supply Voltage	V_{DC}		2.5	2.7	3.3	V
Supply Voltage	V_{DD1}		10	15	20	V
Supply Voltage	V_{ES3}		−20	−15	−10	V
Supply Voltage	V_{DD1}–V_{SS3}		20	30	40	V
Input Voltage Note	V_I		0		V_{CC1}	V

Note CLK, STVR, STVL, R,/L, OE_1, OE_2, GCS, GCL, GDA, DCCLK, VCIN, DCON, RGON, VCD2, /GRESET, IFSEL, EXRV, SCN0, SCN1

Electrical Characteristics (T_A = –40 to +85°C, V_{CC1} = 2.5 to 3.3 V, V_{DD1} = 15 V, V_{SS3} = –15 V, V_S = 5 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	**Note 1**	0.8 V_{CC1}			V
Low-level input voltage	V_{IL1}				0.2 V_{CC1}	V
High-level input voltage	V_{IH1}	VCOM, VCIN	0.8 V_S			V
Low-level input voltage	V_{IL1}				0.2 V_S	V
High-level output voltage	V_{OH}	STVR, STVL, I_{OH} = –40 μA	V_{CC1} – 0.4		V_{CC1}	V
High-level output voltage	V_{OL}	STVR, STVL, I_{OH} = +40 μA	0		0.4	V
V_{DD1} boost voltage	V_{DD1}	I_{DD1} = 300 μA , 3x boost	2.7 V_S	–	3 V_S	V
V_{DD2} boost voltage1	V_{DD2}	V_{CD2} = L (2x boost), I_{DD2} = 1 mA	1.9 V_{DC}	–	2 V_{DC}	V
V_{DD2} boost voltage2	V_{DD2}	V_{CD2} = H (3x boost), I_{DD2} = 1 mA	2.8 V_{DC}	–	3 V_{DC}	V
V_{SS2} boost voltage	V_{SS2}	I_{SS2} = –300 μA, 2x boost	–2 V_S	–	–1.8 V_S	V
V_{SS3} boost voltage	V_{SS3}	I_{SS3} = –300 μA, 3x boost	–3 V_S	–	–2.7 V_S	V
V_{DD1} output resister	R_{VDD1}	I_{DD1} = 300 μA, 3x boost	1.5	3	5	kΩ
V_{DD2} output resistor1	R_{VDD21}	V_{CD2} = L (2x boost), I_{DD2} = 1 mA	50	100	200	Ω
V_{DD2} output resistor2	R_{VDD22}	V_{CD2} = H (3x boost), I_{DD2} = 1 mA	100	200	400	Ω
V_{SS2} output resistor	R_{VSS2}	I_{SS2} = –300 μA , 2x boost	1	2	3	kΩ
V_{SS2} output resistor	R_{VSS2}	I_{SS2} = –300 μA , 2x boost	1.5	3	5	kΩ
V_S output voltage	V_S	No load	4.5	5	5.5	V
V_R output voltage	V_S	No load	4.5	5	5.5	V
V_S output voltage	R_{VS}	V_{DD2} = 6 V, I_S = 1 mA,V_S = 5 V	–	30	60	Ω
V_R output voltage	R_{VS}	V_{DD2} = 6 V, I_R = 1mA,V_R = 5 V	–	60	120	Ω
COMH output voltage	V_{comH}	VCOM = 1/2 x V_S	4.5	5	5.5	V
COML output voltage	V_{comL}	VCOM = 1/2 x V_S	–0.5	0	0.5	V
COM output high-level voltage	V_{comH}	VCOM = 1/2 x V_S	4.5	5	5.5	V
COM output low-level voltage	V_{comL}	VCOM = 1/2 x V_S	– 0.5	0	0.5	V
COM output resistor1	R_{COM1}	COM output = High, I_{COM} = 1 mA	–	100	200	Ω
COM output resistor2	R_{COM2}	COM output = Low, I_{COM} = –1 mA	–	100	200	Ω
VM output high-level voltage	V_{M1H}		0.9 V_{SS2}	V_{SS2}	1.1 V_{SS2}	V
VM output low-level voltage	V_{M1L}		0.9 V_{SS3}	V_{SS3}	1.1 V_{SS3}	V
VM output resistance	R_{M1}		–	10	20	Ω
Output ON resistance	R_{ON1}	O_1 to O_{240}	1	2	4	kΩ
Input current	I_{I1}	**Note 1**	– 1	0	1	μA
Input current	I_{I2}	VCOM, VCIN	– 1	0	1	μA
Input leak current	I_{IL}	STVR, STVL	– 1	0	1	μA
Dynamic current	I_{CC1}	V_{CC1}, f_{CLK} = 45.5 kHz, no load, **Note 2**	–	–	200	μA
Dynamic current	I_{DC}	V_{DC}, f_{CLK} = 45.5 kHz, no load, **Note 2**	–	–	300	μA
Dynamic current	I_{EE}	V_{EE}, f_{CLK} = 45.5 kHz, no load, **Note 2**	–	–	300	μA
Static current	I_{CC1}	V_{CC1}, stand-by	–	–	5	μA
Static current	I_{DC}	V_{DC}, stand-by	–	–	5	μA
VREF voltage				1.2		V

Notes 1. CLK, STVR, STVL, R/L, OE1, OE2, GCS, GCL, GDA, VCOM, DCON, RGON, VCD2, /RESET, IFSEL, EXRV, SCN0, SCN1, VCIN

2. When AMP. current is maximum.

Switching Characteristics (T_A = –40 to +85°C, V_{CC1} = 2.5 to 3.3 V, V_{DD1} = 15 V, V_{SS3} = –15 V, V_S = 5 V, V_{SS} = 0 V)

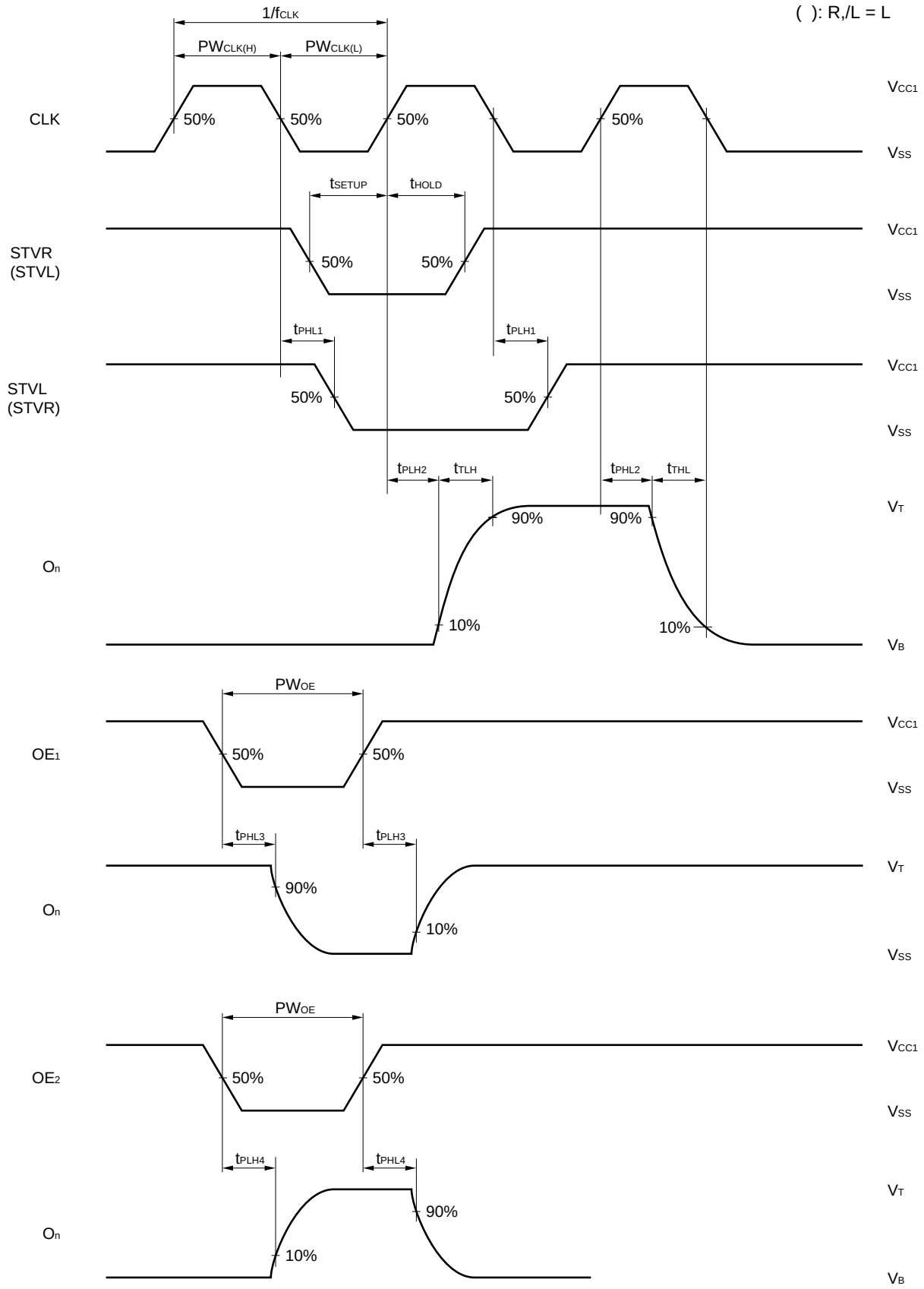
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Cascade Output Delay Time	t_{PHL1}	C_L = 50 pF			800	ns
	t_{PLH1}	CLK → STVL (STVR)			800	ns
Driver Output Delay Time 1	t_{PHL2}	C_L = 50 pF			1	us
	t_{PLH2}	CLK → O_n			1	us
Driver Output Delay Time2	t_{PHL3}	C_L = 50 pF			1	μs
	t_{PLH3}	OE_1 → O_n			1	μs
Driver Output Delay Time 3	t_{PHL4}	C_L = 50 pF			1	μs
	t_{PLH4}	OE_2 → O_n			1	μs
Output Rise Time	t_{TLH}	C_L = 50 pF			450	ns
Output Fall Time	t_{THL}				450	ns
Input Capacitance	C_I	T_A = 25°C			15	pF
DC/DC Oscillation Frequency	f_{DCDC}	FS0, FS1 = H	15	20	25	kHz
DCCLK Input Frequency	f_{DCCLK}			20	50	kHz
VCIN Input Frequency	f_{VCIN}			10	50	kHz
Clock Input Frequency	f_{CLK}	When connected in cascade		20	500	kHz

Timing Requirement (T_A = –40 to +85°C, V_{CC1} = 2.5 to 3.3 V, V_{DD1} = 15 V, V_{SS3} = –15 V, V_S = 5 V, V_{SS} = 0 V)

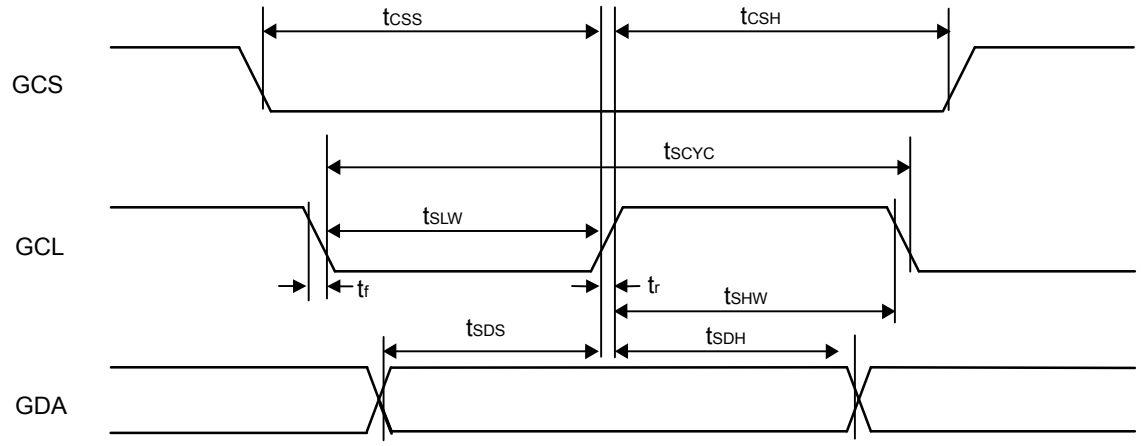
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse High Period	$PW_{CLK(H)}$		500			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		500			ns
Enable Pulse High Period	PW_{OE}	OE_1, OE_2	1.0			μs
Data Setup Time	t_{SETUP}	STVR (STVL) ↓ →CLK↑	200			ns
Data Hold Time	t_{HOLD}	CLK↑→STVR (STVL) ↑	200			ns
Serial Clock Cycle	t_{SCYC}	GCL	250			ns
GCL High-level Pulse Width	t_{SHW}	GCL	100			ns
GCL Low-level Pulse Width	t_{SLW}	GCL	100			ns
GDA Data setup time	t_{SDS}	GDA	100			ns
GDA Data Hold Time	t_{SDH}	GDA	100			ns
GCS-GCL Time	t_{CSS}	GCS	150			ns
GCL-GCS Time	t_{CSH}	GCS	150			ns

SWITCHING CHARACTERISTICS WAVEFORM (R,/L = H, STVSEL = 0, OE1SEL = 0, OE2SEL = 0)

(a) Gate interface



(b) Serial interface



[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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