

3-Input 2-Output 3-Circuit Video Switch Monolithic IC MM1238

Outline

This IC is a video switch developed for large and medium-sized high quality TVs, with 3-input and 2-output circuits. It is suitable for BS, JSB, CS or M-N (Muse NTSC conversion) comparator switching. The BS-CS decoder can be used as a W decoder.

Features

- One of the two video signal outputs is for external output, and has a 6dB amp, 75Ω, 1V_{P-P}
- Input impedance

Video circuits 1~3	15kΩ
Audio circuits 1~3	68kΩ
- Crosstalk

Video	-60dB (at 4.43MHz)
Audio	-80dB (at 1kHz)
Video : Audio	-70dB (at 100kHz)
- Frequency response

10MHz (6dB, 75Ω, amp only, 7MHz)

- Power supply voltage

8.0V~13.0V

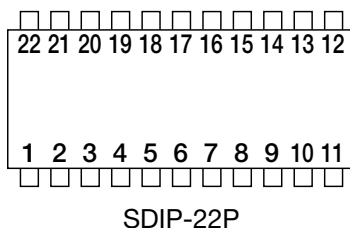
Package

SDIP-22A (MM1238XD)

Applications

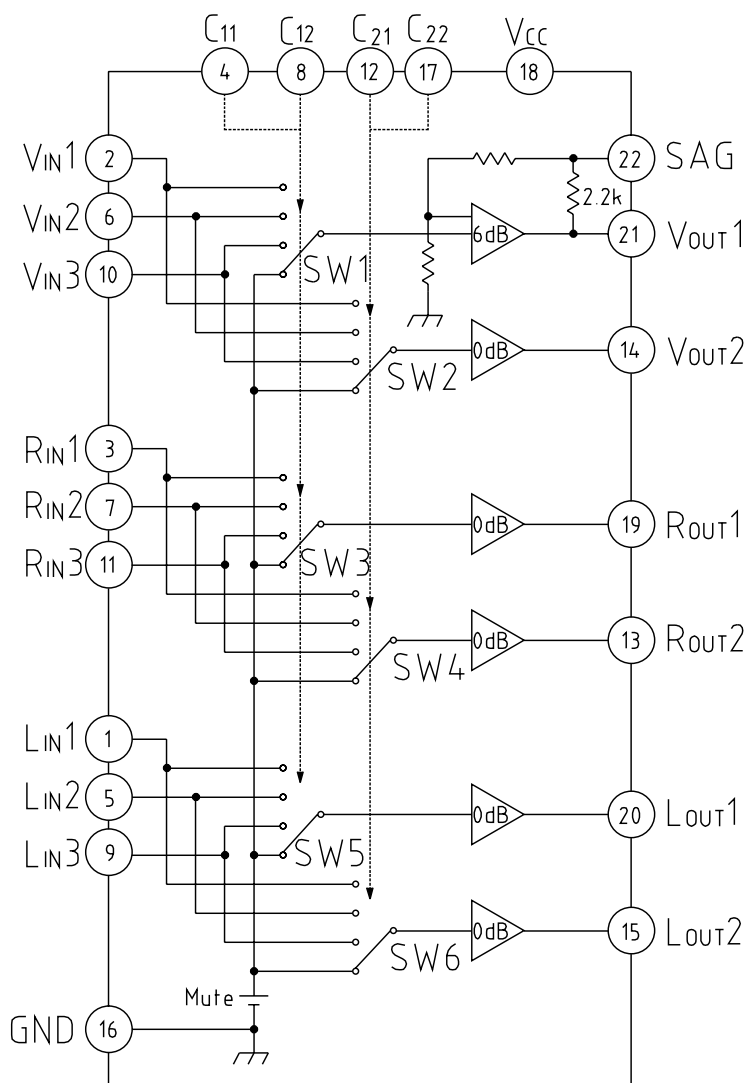
- TV
- Free-standing VCR
- Other video equipment

Pin Assignment



Pin no.	Pin name	Function	Pin no.	Pin name	Function
1	LIN1	Audio LIN1	12	C21	SW2 control
2	VIN1	Video IN1	13	Rout2	Audio Rout2
3	RIN1	Audio RIN1	14	Vout2	Video OUT2
4	C11	SW1 control	15	Lout2	Audio Lout2
5	LIN2	Audio LIN2	16	GND	GND
6	VIN2	Video IN2	17	C22	SW2 control
7	RIN2	Audio RIN2	18	Vcc	Power supply
8	C12	SW1 control	19	Rout1	Audio Rout1
9	LIN3	Audio LIN3	20	Lout1	Audio Lout1
10	VIN3	Video IN3	21	Vout1	Video OUT1
11	RIN3	Audio RIN3	22	SAG	Sag pin

Block Diagram



SW Logic

Control input		Output signal		
C11	C12	Vout1	Rout1	Lout1
L	L	Mute	Mute	Mute
L	H	VIn1	RIn1	LIn1
H	L	VIn2	RIn2	LIn2
H	H	VIn3	RIn3	LIn3

Control input		Output signal		
C21	C22	Vout2	Rout2	Lout2
L	L	Mute	Mute	Mute
L	H	VIn1	RIn1	LIn1
H	L	VIn2	RIn2	LIn2
H	H	VIn3	RIn3	LIn3

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T _{STG}	-40~+125	°C
Operating temperature	T _{OPR}	-20~+75	°C
Power supply voltage	V _{CC}	15	V
Allowable loss	P _d	800	mW

Electrical Characteristics (Except where noted otherwise, Ta=25°C, V_{CC}= 8V~13V)

Item	Symbol	Measurement circuit	Measurement conditions	Min.	Typ.	Max.	Units
Operating power supply voltage	V _{CC}	V _{CC}		8.0		13.0	V
Consumption current	I _{CC1}		V _{CC} =9V		22.0	29.0	mA
	I _{CC2}		V _{CC} =12V		25.0	33.0	mA
V_{OUT1} output							
Voltage gain	G _{V1}	TP7	SG2 : Sine wave 1V _{P-P} , 0.1MHz	5.7	6.2	6.7	dB
Frequency characteristic	F _{V1}	TP7	SG2 : Sweep signal 1V _{P-P} 7MHz/0.1MHz	-1.0	0	1.0	dB
Differential gain	DG1	TP8	SG2 : Staircase wave 1V _{P-P} APL=10, 50, 90%		0	3	%
Differential phase	DP1	TP8	SG2 : Staircase wave 1V _{P-P} APL=10, 50, 90%		0	3	deg
R_{OUT1} output							
Voltage gain	G _{R1}	TP5	SG3 : Sine wave 2.5V _{P-P} , 1kHz	-0.5	0	0.5	dB
Total harmonic distortion	THD _{R1}	TP5	SG3 : Sine wave 2.5V _{P-P} , 1kHz		0.01	0.1	%
Mute noise	V _{NM1}	TP5	15kHz band during mute select		180		μVrms
Output noise voltage	V _{NR1}	TP5	15kHz band during pin select		3	50	μVrms
L_{OUT1} output							
Voltage gain	G _{L1}	TP6	SG1 : Sine wave 2.5V _{P-P} , 1kHz	-0.5	0	0.5	dB
Total harmonic distortion	THD _{L1}	TP6	SG1 : Sine wave 2.5V _{P-P} , 1kHz		0.01	0.1	%
Mute noise	V _{NM2}	TP6	15kHz band during mute select		180		μVrms
Output noise voltage	V _{NL1}	TP6	15kHz band during pin select		3	50	μVrms
V_{OUT2} output							
Voltage gain	G _{V2}	TP2	SG2 : Sine wave 1V _{P-P} , 0.1MHz	-0.5	0	0.5	dB
Frequency characteristic	F _{V2}	TP2	SG2 : Sweep signal 1V _{P-P} 10MHz/0.1MHz	-1.0	0	1.0	dB
Differential gain	DG2	TP3	SG2 : Staircase wave 1V _{P-P} APL=10, 50, 90%		0	3	%
Differential phase	DP2	TP3	SG2 : Staircase wave 1V _{P-P} APL=10, 50, 90%		0	3	deg
R_{OUT2} output							
Voltage gain	G _{R2}	TP1	SG3 : Sine wave 2.5V _{P-P} , 1kHz	-0.5	0	0.5	dB
Total harmonic distortion	THD _{R2}	TP1	SG3 : Sine wave 2.5V _{P-P} , 1kHz		0.01	0.1	%
Mute noise	V _{NM3}	TP1	15kHz band during mute select		180		μVrms
Output noise voltage	V _{NR2}	TP1	15kHz band during pin select		3	50	μVrms
L_{OUT2} output							
Voltage gain	G _{L2}	TP4	SG1 : Sine wave 2.5V _{P-P} , 1kHz	-0.5	0	0.5	dB
Total harmonic distortion	THD _{L2}	TP4	SG1 : Sine wave 2.5V _{P-P} , 1kHz		0.01	0.1	%
Mute noise	V _{NM4}	TP4	15kHz band during mute select		180		μVrms
Output noise voltage	V _{NR2}	TP4	15kHz band during pin select		3	50	μVrms
Output offset voltage							
V _{OUT1}	V _{OFF1}	TP7	V _{OUT1} pin DC level difference during switching		0	±30	mV
V _{OUT2}	V _{OFF2}	TP2	V _{OUT2} pin DC level difference during switching		0	±15	mV
R _{OUT1}	V _{OFF3}	TP5	R _{OUT1} pin DC level difference during switching		0	±15	mV
R _{OUT2}	V _{OFF4}	TP1	R _{OUT2} pin DC level difference during switching		0	±15	mV
L _{OUT1}	V _{OFF5}	TP6	L _{OUT1} pin DC level difference during switching		0	±15	mV
L _{OUT2}	V _{OFF6}	TP4	L _{OUT2} pin DC level difference during switching		0	±15	mV

Input impedance							
V_{IN}	R_{IV}		$V_{IN1} \sim V_{IN3}$		15		k Ω
R_{IN}	R_{IR}		$R_{IN1} \sim R_{IN3}$		68		k Ω
L_{IN}	R_{IL}		$L_{IN1} \sim L_{IN3}$		68		k Ω
Output impedance							
V_{OUT}	V_{OV}		V_{OUT2}		50		Ω
R_{OUT}	V_{OR}		R_{OUT1} and R_{OUT2}		50		Ω
L_{OUT}	V_{OL}		L_{OUT1} and L_{OUT2}		50		Ω
Crosstalk							
$V_{IN} \rightarrow V_{OUT}$	CT_{VV}		SG2 : 1V _{P-P} , 4.43MHz *1		-60	-50	dB
$R_{IN} \rightarrow R_{OUT}$	CT_{RR}		SG3 : 2.5V _{P-P} , 1kHz *2		-80	-70	dB
$L_{IN} \rightarrow L_{OUT}$	CT_{LL}		SG1 : 2.5V _{P-P} , 1kHz *3		-80	-70	dB
$V_{IN} \rightarrow R_{OUT}$	CT_{RV}		SG2 : 1V _{P-P} , 100kHz *4		-70	-60	dB
$V_{IN} \rightarrow L_{OUT}$	CT_{LV}		SG2 : 1V _{P-P} , 100kHz *5		-70	-60	dB
Switch input voltage							
SW input voltage H	V_{IH}		Switching H level for each IC SW	2.1			V
SW input voltage L	V_{IL}		Switching L level for each IC SW			0.7	V
Input dynamic range							
$V_{IN} \rightarrow V_{OUT}$	D1		$V_{CC}=12V$, SG1 : sine wave, 1kHz	2.6			V_{P-P}
$R_{IN} \rightarrow R_{OUT}$	D2		$V_{CC}=12V$, SG2 : sine wave, 1kHz Total higher harmonic distortion=0.5%	2.0			V _{rms}
$L_{IN} \rightarrow L_{OUT}$	D3		$V_{CC}=12V$, SG3 : sine wave, 1kHz Total higher harmonic distortion=0.5%	2.0			V _{rms}

*1 Crosstalk ($V_{IN} \rightarrow V_{OUT}$)

Input a 1V_{P-P}, 4.43MHz sine wave to SG2.

Obtain CT_{VV} using the following formula given output amplitude for combinations other than those below for SW control pin as V_{O1} , and for the combinations below as V_{O2} .

$$CT_{VV} = 20 \times \log (V_{O2}/V_{O1}) \text{ dB}$$

1. CT_{VV1}

2. CT_{VV2}

Measuring pin	Switch status				
	S2	V1	V2	V3	V4
TP8	A	L	L	L	H
	A	H	L	L	H
	A	H	H	L	H
	B	L	L	H	L
	B	L	H	H	L
	B	H	H	H	L
	C	L	L	H	H
	C	L	H	H	H
	C	H	L	H	H

Measuring pin	Switch status				
	S2	V1	V2	V3	V4
TP3	A	L	H	L	L
	A	L	H	H	L
	A	L	H	H	H
	B	H	L	L	L
	B	H	L	L	H
	B	H	L	H	H
	C	H	H	L	L
	C	H	H	L	H
	C	H	H	H	L

***2 Crosstalk ($R_{IN} \rightarrow R_{OUT}$)**

Input a $2.5V_{P-P}$, 1kHz sine wave to SG3.

Obtain C_{TRR} using the following formula given output amplitude for combinations other than those below for SW control pin as V_{o3} , and for the combinations below as V_{o4} .

$$C_{TRR} = 20 \times \log (V_{o4}/V_{o3}) \text{ dB}$$

1. C_{TRR1}

Measuring pin	Switch status				
	S3	V1	V2	V3	V4
TP5	A	L	L	L	H
	A	H	L	L	H
	A	H	H	L	H
	B	L	L	H	L
	B	L	H	H	L
	B	H	H	H	L
	C	L	L	H	H
	C	L	H	H	H
	C	H	L	H	H

2. C_{TRR2}

Measuring pin	Switch status				
	S3	V1	V2	V3	V4
TP1	A	L	H	L	L
	A	L	H	H	L
	A	L	H	H	H
	B	H	L	L	L
	B	H	L	L	H
	B	H	L	H	H
	C	H	H	L	L
	C	H	H	L	H
	C	H	H	H	L

***3 Crosstalk ($L_{IN} \rightarrow L_{OUT}$)**

Input a $2.5V_{P-P}$, 1kHz sine wave to SG3.

Obtain C_{TLL} using the following formula given output amplitude for combinations other than those below for SW control pin as V_{o5} , and for the combinations below as V_{o6} .

$$C_{TLL} = 20 \times \log (V_{o6}/V_{o5}) \text{ dB}$$

1. C_{TLL1}

Measuring pin	Switch status				
	S1	V1	V2	V3	V4
TP6	A	L	L	L	H
	A	H	L	L	H
	A	H	H	L	H
	B	L	L	H	L
	B	L	H	H	L
	B	H	H	H	L
	C	L	L	H	H
	C	L	H	H	H
	C	H	L	H	H

2. C_{TLL2}

Measuring pin	Switch status				
	S1	V1	V2	V3	V4
TP4	A	L	H	L	L
	A	L	H	H	L
	A	L	H	H	H
	B	H	L	L	L
	B	H	L	L	H
	B	H	L	H	H
	C	H	H	L	L
	C	H	H	L	H
	C	H	H	H	L

Obtain C_{TRV} (C_{TLV}) using the following formula given output amplitude for combinations other than those below for SW control pin as V_{O7} , and for the combinations below as V_{O8} .

$$C_{TRV} (C_{TLV}) = 20 \times \log (V_{o8}/V_{o7}) \text{ dB}$$

2. C_{TLV}

Measuring pin	Switch status				
	S2	V1	V2	V3	V4
TP5	A	L	H	L	H
	B	H	L	H	L
	C	H	H	H	H
TP1	A	L	H	L	H
	B	H	L	H	L
	C	H	H	H	H

Measuring pin	Switch status				
	S2	V1	V2	V3	V4
TP6	A	L	H	L	H
	B	H	L	H	L
	C	H	H	H	H
TP4	A	L	H	L	H
	B	H	L	H	L
	C	H	H	H	H

Measuring Circuit

