EM78815

8-BIT MICRO-CONTROLLER

Version 2.4

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Specification Revision History		
Version	**Content**	
EM78813 ICE		
1.0	Initial version	
1.1	Change FSK,DTMF and CW power control	2003/3/4
2.0	1. Remove 256K byte data ROM 2. Remove expand program/data memory interface 3. Embedded 1.2%, 2.0% and 5.5% CAS frequency range deviation	
2.1	1. Add 256K byte data ROM 2. Add expand program/data memory interface 3. Remove 1.2% CAS frequency range deviation 4. Remove UART function	
2.2	1. Modify Current DA resolution from 7 bit to 10 bit	2003/8/19
2.3	1. Add UART function	2003/10/8
2.4	1. Remove Idle mode 2. Add application note item 7	2004/8/1

Application Note

1. For targeting interrupt and program run to address 0x0008, ACC, R3(STATUS), R5(Program page) and R4(6,7) will be automatically saved and R3(6,7) R register page will set to PAGE0, and reload after the instruction “RETI”.
2. 2.0V reference voltage will power down when both RD PAGE2 bit7(DAREF) and RA PAGE2 bit7(CMPEN) are clear to 0.
3. Before using Key tone function, please set Port 76 as output type.
4. For accessing data ROM, EM78P815 (OTP) can work at 10.74MHz, but please note that ROM type EM78815 only can work at 5.3MHz
5. While switching main clock (regardless of high freq to low freq or on the other hand), adding 6 instructions delay (NOP) is required.
6. Please do not switch MCU operation mode from normal mode to sleep mode directly. Before into sleep mode, please switch MCU to green mode.
7. ***Please always keep RA page0 bit7 = 0 or un-expect error will happen!!***

I. General Description

The EM78815 is an 8-bit CID (Call Identification) RISC type microprocessor with low power, high speed CMOS technology. Integrated onto a single chip are on chip watchdog (WDT), programmable real time clock/counter, external/internal interrupt, power down mode, EMC65132 LCD controller, FSK decoder, Call waiting decoder, Energy Detector (DED) , DTMF receiver, Programming Tone generator, build-in KEY TONE clock generation, Comparator and tri-state I/O. The EM78815 provides a single chip solution to design a CID of calling message display.

II. Feature

➢ ***CPU***

- Operating voltage range: 2.2V~3.6V(Normal mode), 2.0V~3.6V(Green mode)
- 64K x 13 on-chip Program ROM, support MAX 128K word program.
- 256K x 8 on chip data ROM support MAX 2M byte data
- 4K x 8 data RAM
- 128 x 8 common register
- Up to 56 bi-directional tri-state I/O ports
- IO with internal Pull high, wake-up and interrupt functions
- STACK: 24 level stack for subroutine nesting
- TCC: 8-bit real time clock/counter (TCC) with 8-bit prescaler
- COUNTER1: 16 bit counter with 8-bit prescaler can be an interrupt source
- COUNTER2: 8-bit counter with 8-bit prescaler can be an interrupt source
- Watch Dog: Programmable free running on chip watchdog timer
- CPU modes:

Mode	CPU status	Main clock	32.768kHz clock status
Sleep mode	Turn off	Turn off	Turn off
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on

- 15 interrupt source, 8 external, 7 internal
- Key Scan: Port key scan function up to 16x4 keys
- Sub-Clock: 32.768KHz crystal
- Main-clock: 3.5862MHz multiplied by 0.5, 1, 1.5 or 3 generated by internal PLL
- Key tone output: 4KHz, 2KHz, 1KHz (shared with IO)
- Comparator: 3-channel comparators: internal (16 level) or external reference voltage. (Shared with IO)

➢ ***Serial transmitter/receiver interface***

- Serial Peripheral Interface (SPI): Interrupt flag available for the read buffer full, Programmable baud rates of communication, Three-wire synchronous communication. (Shared with IO)
- Universal asynchronous receiver transmitter interface. User can select (7/8/9 bits) with/without parity bit, Baud rate setting and error detection function. Interrupt available for RX buffer full or TX buffer empty. Two wire asynchronous communication. (Share with IO)

➢ ***Current D/A***

- Operation Voltage: 2.5V~3.6V
- 10-bit resolution and 3-bit output level control
- Current DA output can drive speaker through a transistor for sound playing. (shared with IO)

➢ ***Programmable Tone Generators***

- Operation Voltage 2.2V~3.6V
- Programmable Tone1 and Tone2 generators

- Independent single tone generation for Tone1 and Tone2
- Mixed dual tone generation by Tone1 and Tone2 with 2dB difference
- Can be programmed for DTMF tone generation
- Can be programmed for FSK signal (Bell202 or V.23) generation

➢ ***CID***

- Operation Voltage 2.4V~3.6V for FSK
- Operation Voltage 2.4V~3.6V for DTMF receiver
- Compatible with Bellcore GR-30-CORE (formerly as TR-NWT-000030)
- Compatible with British Telecom (BT) SIN227 & SIN242
- FSK demodulator for Bell 202 and ITU-T V.23 (formerly as CCITT V.23)
- Differential Energy Detector (DED) for line energy detection

➢ ***CALL WAITING***

- Operation Voltage 2.4V~3.6V
- Compatible with Bellcore special report SR-TSV-002476
- Call-Waiting (2130Hz plus 2750Hz) Alert Signal Detector
- Good talkdown and talkoff performance
- Sensitivity compensated by adjusting input OP gain

➢ ***External LCD controller (64 x 256 dot MAX for a pair of Master and Slave LCD Driver)***

- Multi-chip operation (Master, Slave) available for external LCD device.

➢ ***Package type***

- 105 pin Chip: EM78815H
- 128 pin QFP: (EM78815AQ, POVD disable) (EM78815BQ, POVD enable)

III. Application

- SMS phone
- feature phones

IV. Pin Configuration

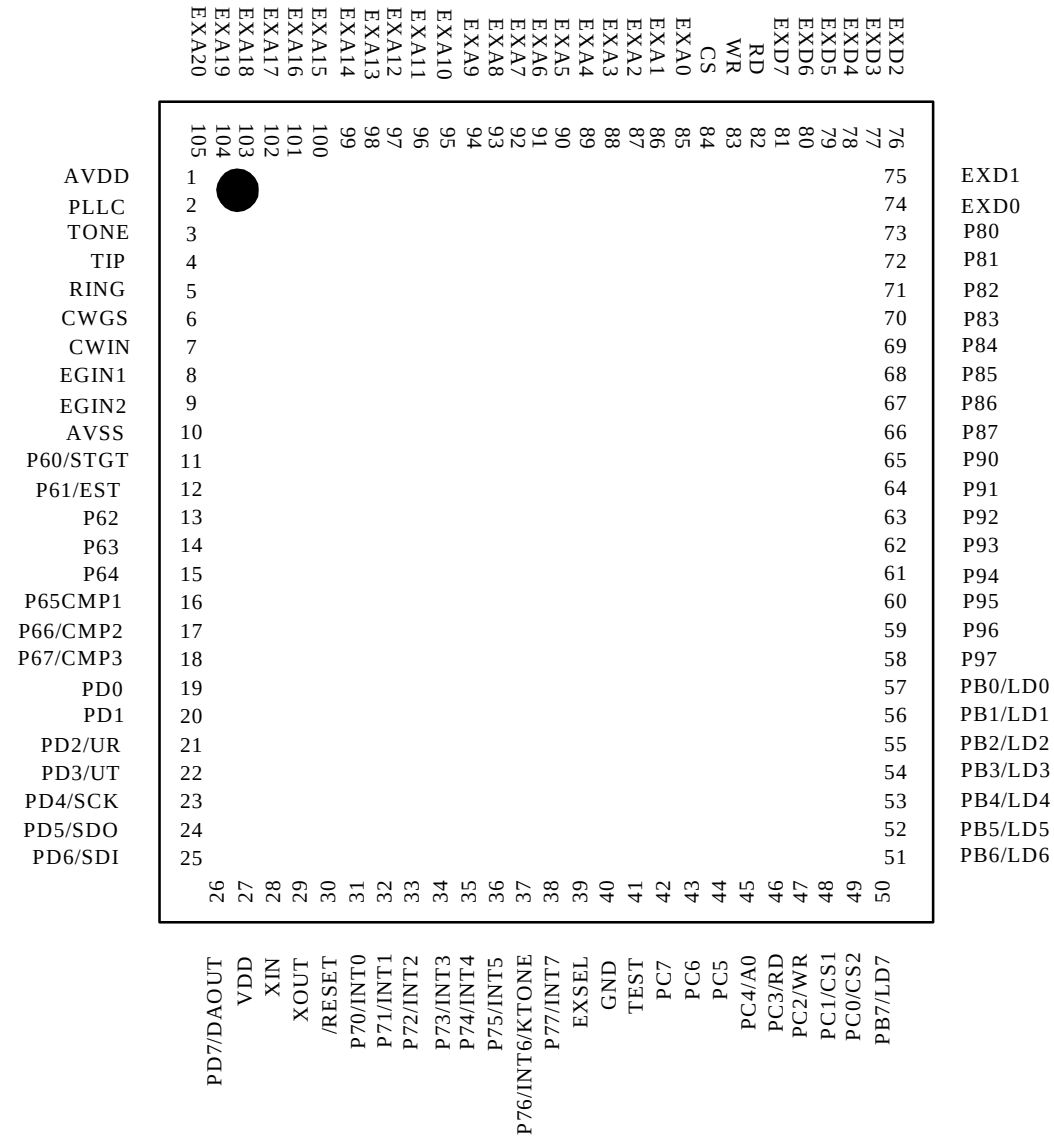


Fig.1a: 105 pin chip assignment

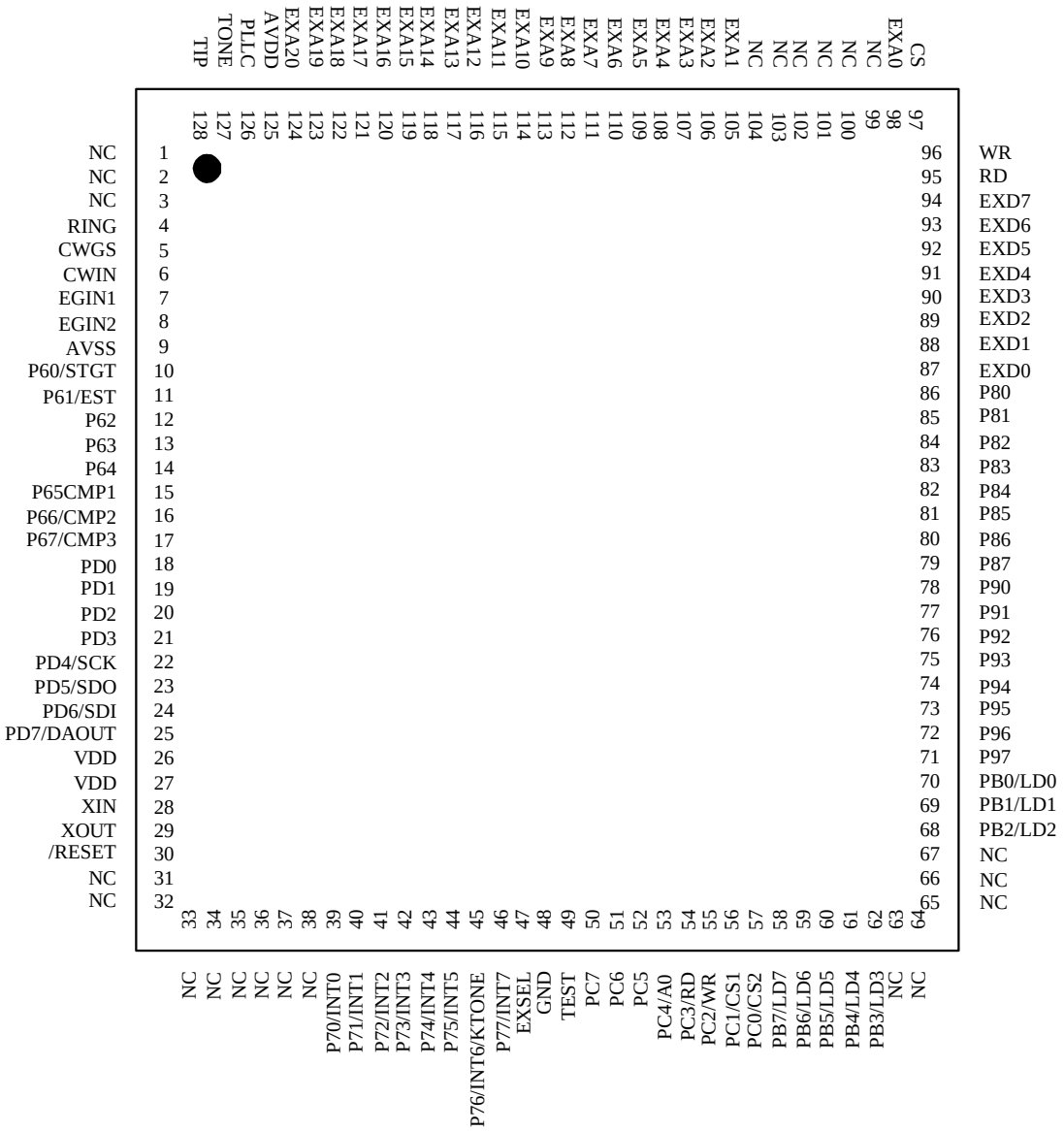


Fig.1b: 128 pin QFP assignment

V. Functional Block Diagram

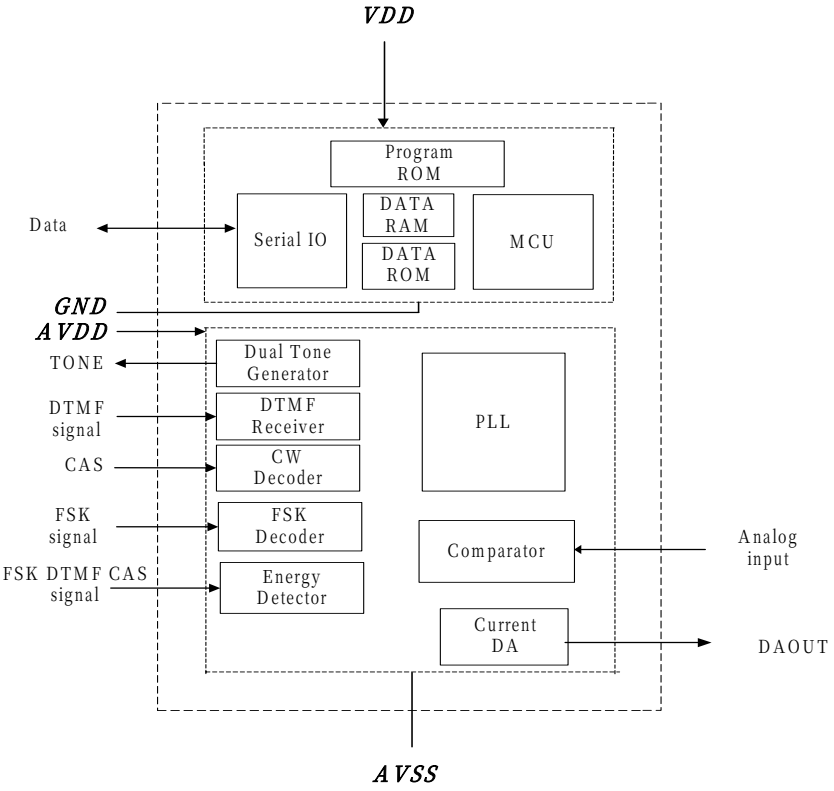


Fig.2 Block diagram1

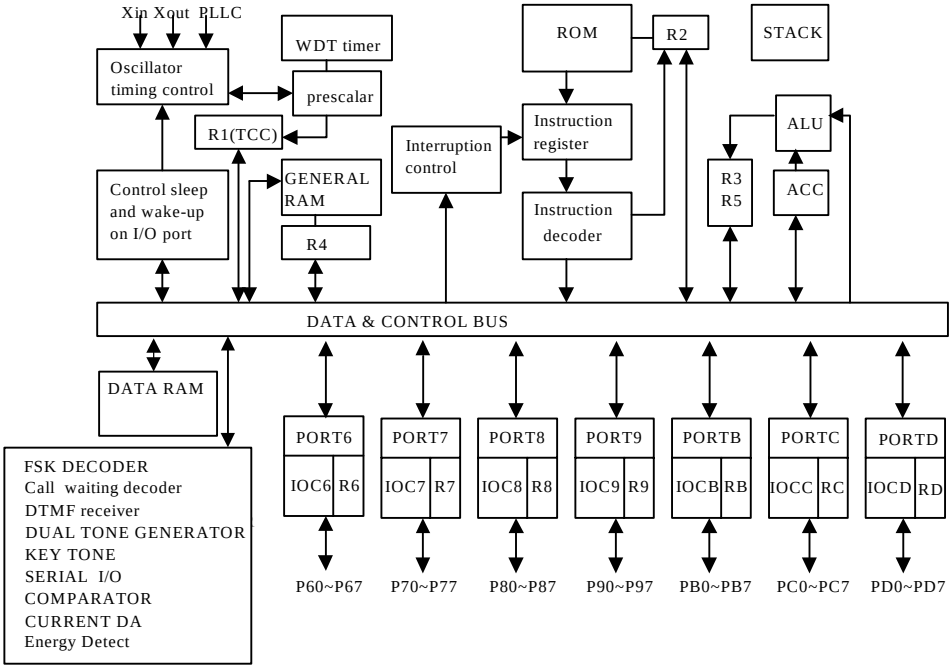


Fig.3 Block diagram2

VI. Pin Descriptions

I. POWER pin

Pin	*I/O*	*Description*
VDD	POWER	Digital Power
AVDD	POWER	Analog Power
GND	POWER	Digital Ground
AVSS	POWER	Analog Ground

II. CLOCK pin

Pin	*I/O*	*Description*
XIN	I	Input pin for 32.768 kHz oscillator
XOUT	O	Output pin for 32.768 kHz oscillator
PLLC	I	Phase loop lock capacitor, connect a capacitor 0.01u to 0.047u with GND

III. External LCD device control pin

Pin	*I/O*	*Description*
LCDD0..LCDD7	I/O	External LCD driver data bus. Shared with PORTB0..PORTB7.
/WR	O	Write enable output (active low signal). Shared with PORTC2.
/RD	O	Read enable output (active low signal). Shared with PORTC3.
A0	O	Used as register selection. When A0 equal to 1, data bus transmit LCD DATA. When A0 equal to 0,data bus transmit LCD Address. The pin shared with PORTC4.
/CS1../CS2	O	Chip Selection signal output. Shared with PORTC1..PORTC0

IV. FSK,CW

Pin	*I/O*	*Description*
TIP	I	Should be connected with TIP side of twisted pair lines for FSK.
RING	I	Should be connected with RING side of twisted pair lines for FSK.
CWGS	O	Gain adjustment of single-ended input OP Amp
CWIN	I	Single-ended input OP Amp for call waiting decoder

V. DTMF receiver , OP

Pin	*I/O*	*Description*
EST	O	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone-pair (signal condition). Any momentary loss of signal condition will cause EST to return to a logic low. This pin shared with PORT61.
STGT	I/O	Steering input/guard time output (bi-directional). A voltage greater than Vtst detected at ST causes the device to register the detected tone-pair and update the output latch. A voltage less than Vtst frees the device to accept a new tone-pair. The GT output acts to reset the external steering time-constant; its state is a function of EST and the voltage on ST . This pin shared with PORT60.

VI. Serial IO, Comparator, Current DA , Tone

Pin	*I/O*	*Description*
SCK	I/O	Master: output pin , Slave: input pin. This pin shared with PORTD4
SDO	O	Output pin for serial data transferring. This pin shared with PORTD5.
SDI	I	Input pin for receiving data. This pin shared with PORTD6.

UR	I	Data receiver pin for UART. This pin shared with PORTD2
UT	O	Data transmitter pin for UART. This pin shared with PORTD3
CMP1	I	Comparator input pins. Shared with PORT65.
CMP2	I	Comparator input pins. Shared with PORT66
CMP3	I	Comparator input pins. Shared with PORT67.
DAOUT	O	Current DA output pin. It can be a control signal for sound generating. Shared with PORTD7.
KTONE	O	Key tone output. Shared with PORT76.
TONE	O	Dual tone output pin

VII. IO

Pin	*I/O*	*Description*
P60 ~P67	I/O	PORT 6 can be INPUT or OUTPUT port each bit. Internal pull high.
P70 ~ P77	I/O	PORT 7 can be INPUT or OUTPUT port each bit. Internal Pull high function. Auto key scan function. Interrupt function.
P80 ~ P87	I/O	PORT 8 can be INPUT or OUTPUT port each bit.
P90 ~ P97	I/O	PORT 9 can be INPUT or OUTPUT port each bit.
PB0 ~ PB7	I/O	PORT B can be INPUT or OUTPUT port each bit.
PC0 ~ PC7	I/O	PORT C can be INPUT or OUTPUT port each bit.
PD0 ~ PD7	I/O	PORT D can be INPUT or OUTPUT port each bit. Shared with SPI pin Share with CMP input pin.
P70 ~ P76	I	Interrupt sources. Any pin from PORT70 to PORT76 has a falling edge signal, it will generate a corresponding interruption..
P77	I	Interrupt source. Once PORT77 has a falling edge or rising edge signal (controlled by CONT register), it will generate a interruption.
/RESET	I	Low reset

VIII Expand Program/Data ROM interface

Pin	*I/O*	*Description*
EXD0 ~ EXD7	I/O	Expand Program/Data memory Data Bus
/RD	O	Expand Program/Data memory Read request output
/WR	O	Expand Program/Data memory Write request output
/CS	O	Expand Program/Data memory CS request output
EX0~EXA20	O	Expand Program/Data memory Address Bus
EXSEL	I	0/1 →Internal 64K Program ROM used/unused

EXSEL pin : 0/1 → On-Chip program ROM used/unused switch.

EM78815 support MAX 128K Program . User can port program to both 64K EM78815 on_chip ROM and 64K expand ROM . User also can ignore 64K EM78815 on_chip ROM and porting all programs to a external 128K ROM. Using this function, user can upgrade program or download new function easily.

EM78815 provide Data ROM expand function. When user access data which address is over 256K, external ROM will be load. User must set expand start address of Data ROM to RF PAGE1, PAGE2 and IOCB PAGE1. A diagram of expand function is as below.

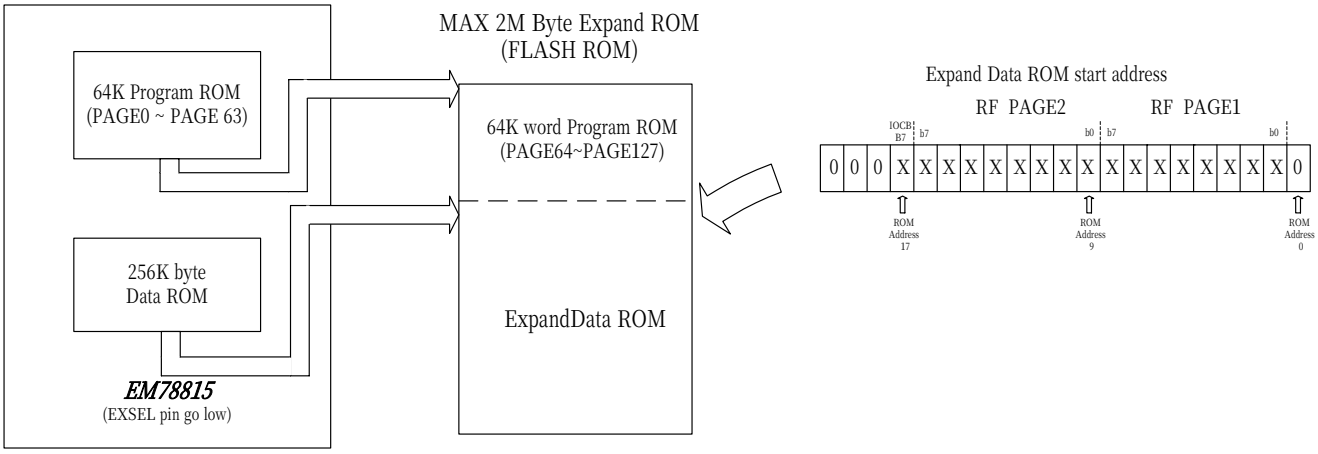


Fig_4a : EXSEL = 0,both internal and external program are used.

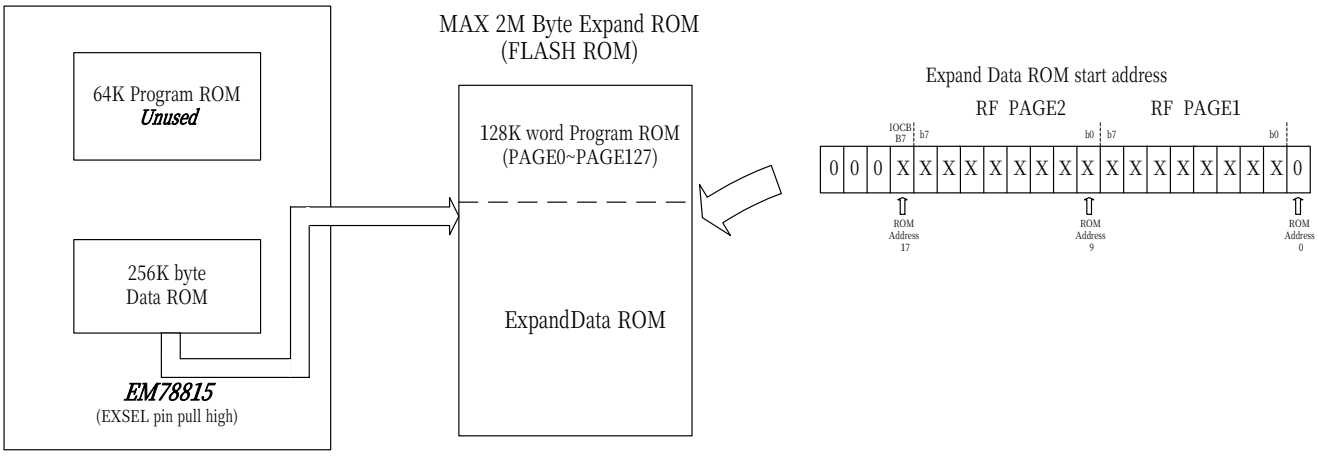


Fig_4b : EXSEL = 1, only external program are used.

How to set expanding Data ROM's starting address?

EM78815 support maximum 2M Byte expanding data memory, but user must fix the start address of external program at 0x00000 and set start address of expanding Data ROM because program ROM size is adjustable. By this way, MCU will get data from external memory if the data ROM is over 256K.

The width of an instruction is 13 bit and the data bus for external memory is 8bit, so an instruction will captured two address size and the LSB address of start address at external ROM will be 0. Besides, EM78815 only support MAX 128K program, so the start address of Data ROM will smaller than 256K+2 andA20, A19 and A18 will be 0 also. ***User only has to according to write Data ROM address A17~A1 to IOCB PAGE2 bi7,RF PAGE3 and RF PAGE2.***

VII. Function Descriptions

VII.1 Operational Register

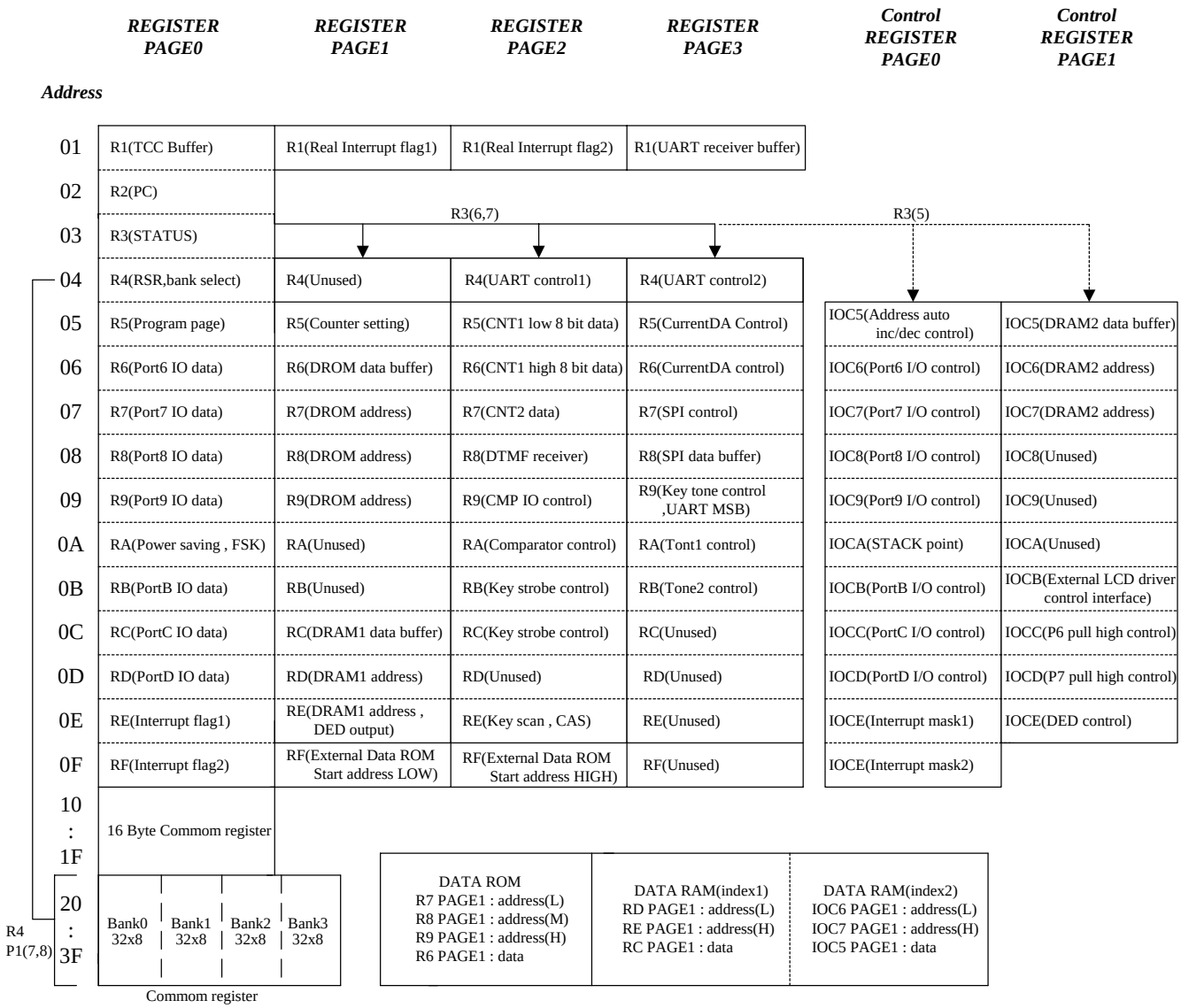


Fig 5: Control register configuration

VII.2 Operational Register Detail Description

R0 Indirect Addressing Register

R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

Example:

```
Mov   A   ,   @0x20    ;store a address at R4 for indirect addressing
Mov   0x04 ,   A
Mov   A   ,   @0xAA   ;write data 0xAA to R20 at bank0 through R0
Mov   0x00 ,   A
```

R1 PAGE0 TCC data buffer

TCC data buffer. Increased by 16.38KHz or by the instruction cycle clock (controlled by CONT register).Written and read by the program as any other register.

R1 PAGE1 Interrupt Flag1 real value

7	6	5	4	3	2	1	0
INTR7	INTR6	INTR5	INTR4	INTR3	INTR2	INTR1	INTR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7(INTR0~INTR7) : Interrupt flag1 real value. User can clear this page from 1 to 0 but can not set 1 to this register. The relation of R1 Page1, RE PAGE0 and IOCE PAGE0 is shown in fig. When user disable interrupt mask, whether interrupt occur or not , interrupt flag(RE PAGE0) will appear "0". Opposite of RE PAGE0, R1 PAGE1 will show real interrupt occur status regardless this interrupt mask enable or disable. ***User can clear corresponding external interrupt flag in RE PAGE0 or R1 PAGE1***.

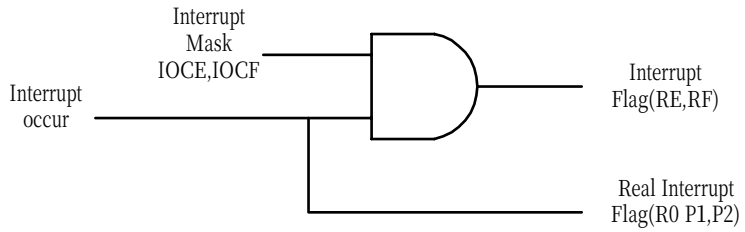


Fig 6: Relation with interrupt mask ,flag and real flag

R1 PAGE2 Interrupt Flag2 real value

7	6	5	4	3	2	1	0
RBF/STD	FSK/CW	-	UART	DED	CNT2	CNT1	TCC
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7(Internal interrupt flag real value) : Interrupt flag1 real value. User can clear this page from 1 to 0 but can not set 1 to this register. The relation of R1 Page2, RF PAGE0 and IOCF PAGE0 is shown in fig6. When user disable interrupt mask, whether interrupt occur or not , interrupt flag(RF PAGE0) will appear "0". Opposite of RF PAGE0, R1 PAGE1 will show real interrupt occur status regardless this interrupt mask enable or disable. ***User can clear corresponding interrupt flag in RF PAGE0 or R1 PAGE2***.

R1 PAGE3 UART receiver data buffer

7	6	5	4	3	2	1	0
URR7	URR6	URR5	URR4	URR3	URR2	URR1	URR0
R	R	R	R	R	R	R	R

Bit 0~Bit 7(URR0~URR7) : UART receiver low 8 bit data buffer. UART receiver data buffer is *read-only* register

R2 Program Counter

External 128K × 13 PROGRAM ROM addresses to the relative programming instruction codes. The structure is depicted on Fig.5

"JMP" instruction allows the direct loading of the low 10 program counter bits.

"CALL" instruction loads the low 10 bits of the PC, PC+1, and then push into the stack.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.

"MOV R2,A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".
"ADD R2,A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".
"TBL" allows a relative address be added to the current PC, and contents of the ninth and tenth bits don't change. The most significant bit (A10~A14) will be loaded with the content of bit PS0~PS3 in the status register (R5) upon the execution of a "JMP", "CALL", "ADD R2, A", or "MOV R2, A" instruction.
If a interrupt trigger, PROGRAM ROM will jump to address 8 at page0. The CPU will store ACC,R3 status and R5 PAGE automatically, it will restore after instruction RETI.

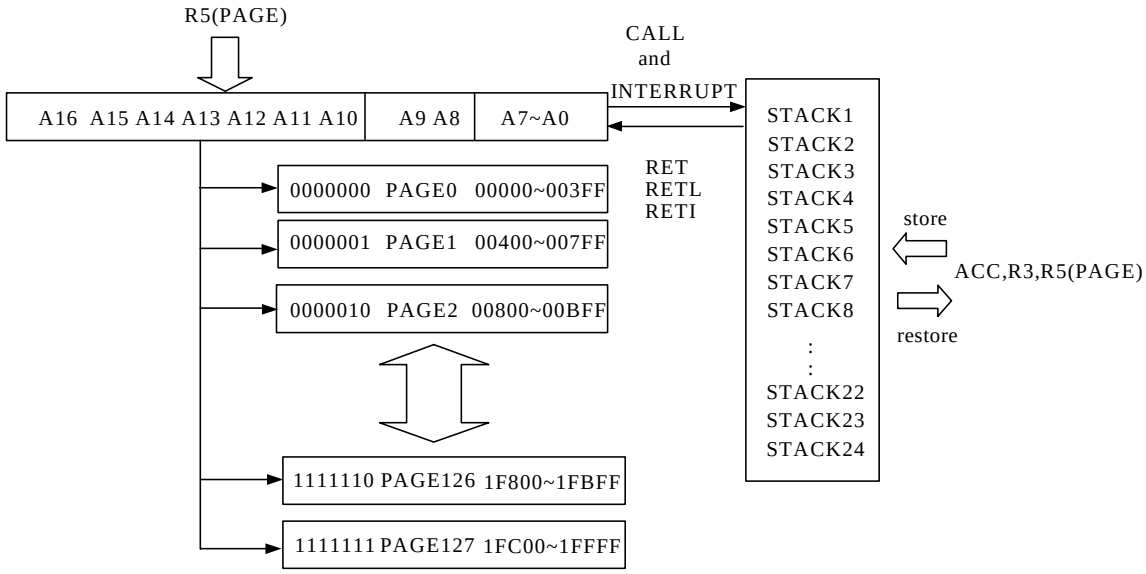


Fig.7: Program counter organization

R3 Status Register

7	6	5	4	3	2	1	0
RS1	RS0	IOCS	T	P	Z	DC	C
R/W-0	R/W-0	R/W-0	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 (C) : Carry
Bit 1 (DC) : Auxiliary carry flag
Bit 2 (Z) : Zero flag
Bit 3 (P) : Power down bit.
Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.
Bit 4 (T) : Time-out bit.
Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

EVENT	T	P	REMARK
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode)	0	1	
/RESET wake up from sleep	1	0	
Power up	1	1	
Low pulse on /RESET	X	X	x : don't care

Bit 5 (IOCS) : IOC register select bit. Change IOC5 ~ IOCE to another PAGE
Bit 6~Bir 7 (RS0 ~ RS1) : R register select bits. Change R1,R2,R4 ~ RE to another PAGE.

RS1	RS0	R PAGE
0	0	PAGE 0
0	1	PAGE 1
1	0	PAGE 2
1	1	PAGE 3

R4 RAM select for common Registers R20~R3F , UART control register

PAGE0

7	6	5	4	3	2	1	0
RBS1	RBS0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W-0	R/W-0	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 5 (RSR0 ~ RSR5) : Indirect addressing for common registers R20 ~ R3F

RSR bits are used to select up to 32 registers (R20 to R3F) in the indirect addressing mode.

Bit 6 ~ Bit 7 (RB0 ~ RB1) : Bank selection bits for common registers R20 ~ R3F

These selection bits are used to determine which bank is activated among the 4 banks for 32 register (R20 to R3F)..

Please refer to Fig.4 control register configuration for details.

PAGE1 Undefined Register

This register is not allowed to used.

PAGE2 UART control register1

7	6	5	4	3	2	1	0
TRS2	TRS1	TRS0	URM1	URM0	ERE	TXE	RXE

Bit 0(RXE) : Enable UART receiving function & UART interrupt mask.

1 ➔ Enable.

0 ➔ Disable.

Bit 1(TXE) : Enable UART transmission function & UART interrupt mask.

1 ➔ Enable

0 ➔ Disable.

Bit 2(ERE) : Enable UART receiver error interrupt mask.

ERR	TXE	REX	RF bit4(UART) interrupt trigger event	IO status
X	0	0	UART interrupt disable	PD2→IO PD3→IO
0	0	1	UART read buffer full	PD2→UART receiver pin PD3→IO
1	0	1	UART read buffer full Or receiver data error	PD2→UART receiver pin PD3→IO
X	1	0	UART transmitter buffer empty	PD2→IO PD3→UART transmitter pin
0	1	1	UART read buffer full Or UART transmitter buffer empty	PD2→UART receiver pin PD3→UART transmitter pin
1	1	1	UART read buffer full Or UART transmitter buffer empty Or receiver data error	PD2→UART receiver pin PD3→UART transmitter pin

Bit 4~Bit 3(URM1~URM0) : UART mode select

URM1	URM0	Mode STATUS
0	0	7 bit data
0	1	8 bit data
1	0	9 bit data
1	1	X

Bit 7~Bit 5(TRS2~TRS0) : Baud rate select

TRS2	TRS1	TRS0	Baud rate
0	0	0	600 baud
0	0	1	1200 baud
0	1	0	2400 baud
0	1	1	9600 baud
1	0	0	19200 baud
1	0	1	38400 baud
1	1	0	57600 baud
1	1	1	115200 baud

**** 600 and 1200 baud rate can be run in green mode.**

PAGE 3 UART control register2

7	6	5	4	3	2	1	0
-	EVEN	PRE	PRERR	OVERR	FMERR	UTBE	URBF
X	R/W-X	R/W-0	R/W-0	R/W-0	R/W-0	R	R

Bit 0(URBF) : UART read buffer full flag . Set to 1 when receiver one character is received.
Reset to 0 automatically when read from UART data buffer.

Bit 1(UTBE) : UART transfer buffer empty flag. Set to 1 when transfer buffer empty. Reset to 0 automatically when write into UART data buffer

Bit 2(FMERR) : receiver error flag . Set to 1 when frame error occur. Clear this bit to 0 by software.

Bit 3(OVERR) : receiver error flag . Set to 1 when over running error occur. Clear this bit to 0 by software.

Bit 4(PRERR) : receiver error flag . Set to 1 when parity error occur. Clear this bit to 0 by software.

Bit 5(PRE) : Enable parity addition.
1 ➔ Enable
0 ➔ Disable

Bit 6(EVEN) : EVEN/ODD parity check select
1➔ EVEN parity
0➔ ODD parity

In Universal Asynchronous Receiver Transmitter(UART) , each transmitted or received character is individually synchronized by framing it with a start bit and stop bit.

The figure below shows the general format of one character sent or received. The communication channel is normally held in the mark state(high). Character transmission or reception starts with a transition to the space state(low).

The first bit transmitted or received is the start bit(low). It is followed by the data bits, in which the least significant bit (LSB) comes first. The data bits are followed by the parity bit. If present, then the stop bit or bits (high) confirming the end of the frame.

In receiving, the UART synchronizes on the falling edge of the start bit. When two or more “0” are detected during 3 samples, it is recognized as normal start bit and the receiving operation is started.

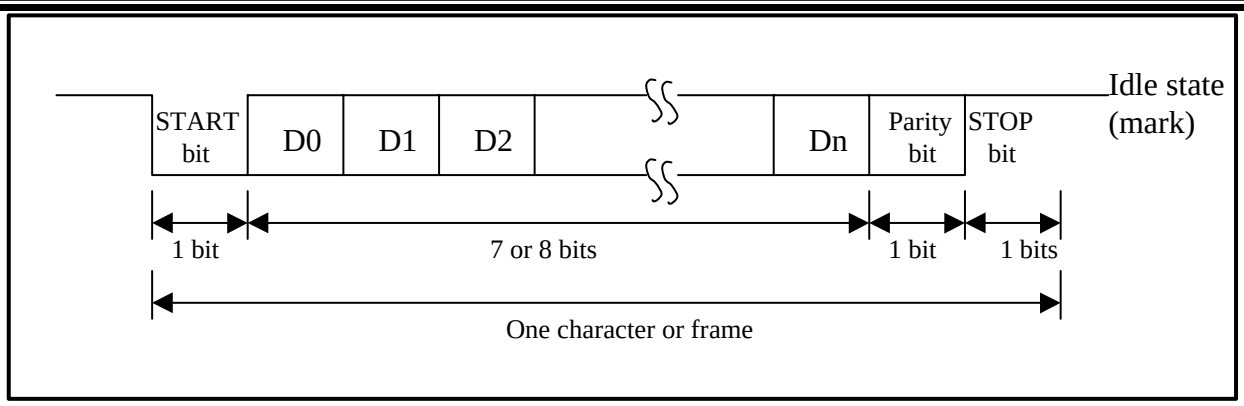


Fig 8: UART data frame

There are 3 mode in UART. Mode 1 (7 bits data) and Mode 2 (8 bits data) allow the addition of a parity bit. The parity bit addition is not available in Mode 3. Figure below shows the data format in each mode.

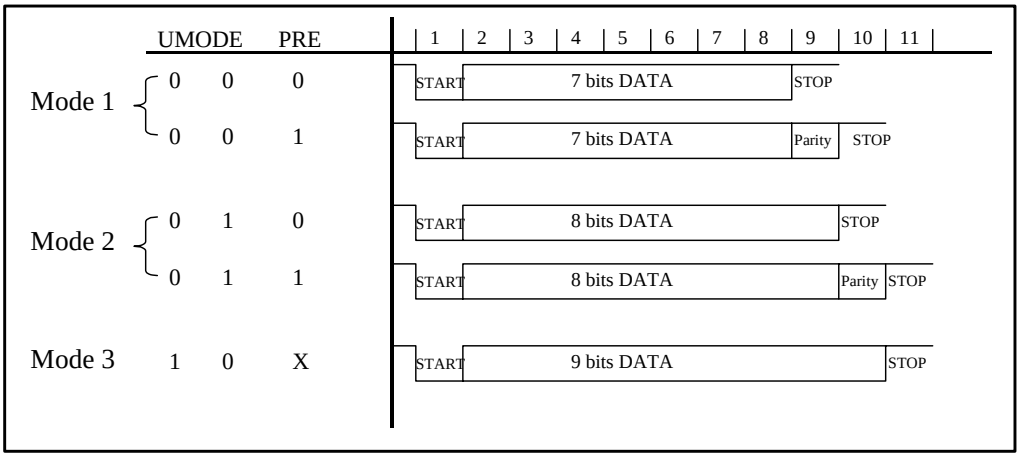


Fig 9: UART mode

In transmitting serial data, the UART operates as follows.

1. Set **TXE** bit of UARTCON register to enable UART transmission function.
2. Write data into UART data buffer . Then start transmitting .
3. Serial transmit data are transmitted in the following order from UT(PortC7) pin.

(a) Start bit: one "0" bit is output.
(b) Transmit data: 7, 8 or 9 bits data are output from LSB to MSB.
(c) Parity bit: one parity bit (odd or even selectable) is output.
(d) Stop bit: one "1" bit (stop bit) is output.
(e) Mark state: output "1" continues until the start bit of the next transmit data.

4. After transmitting the stop bit, the UART generates a **UART** interrupt (if enable) and **UTBE**
5. bit will set to 1.

In receiving, the UART operates as follows.

1. Set **RXE** bit of UARTCON register to enable UART receiving function.
   The UART monitors the UR(PortC6) pin and synchronizes internally when it detects a start bit.
2. Receive data is shifted into UARTRx register in order from LSB to MSB.
3. The parity bit and the stop bit are received.
   After one character received, the UART generates a **UART** interrupt (if enable). And **URBF** bit will be set to 1.
4. The UART makes the following checks:

(a) Parity check: The number of 1 in receive data must match the even or odd parity setting of the **EVEN** bit in UARTSTA register.

(b)Frame check: The start bit must be 0 and the stop bit must be 1.
(c)Overrun check: **URBF** bit of UARTCON register must be cleared(means UARTRx register should be read out) before next received data load into UARTRx register.
If any checks failed, the UART interrupt will be generated(if enable).. The error flag should be cleared by software else the UART interrupt will occur when next byte received.
5.Read received data from UART register. And **URBF** bit will be clear by hardware.

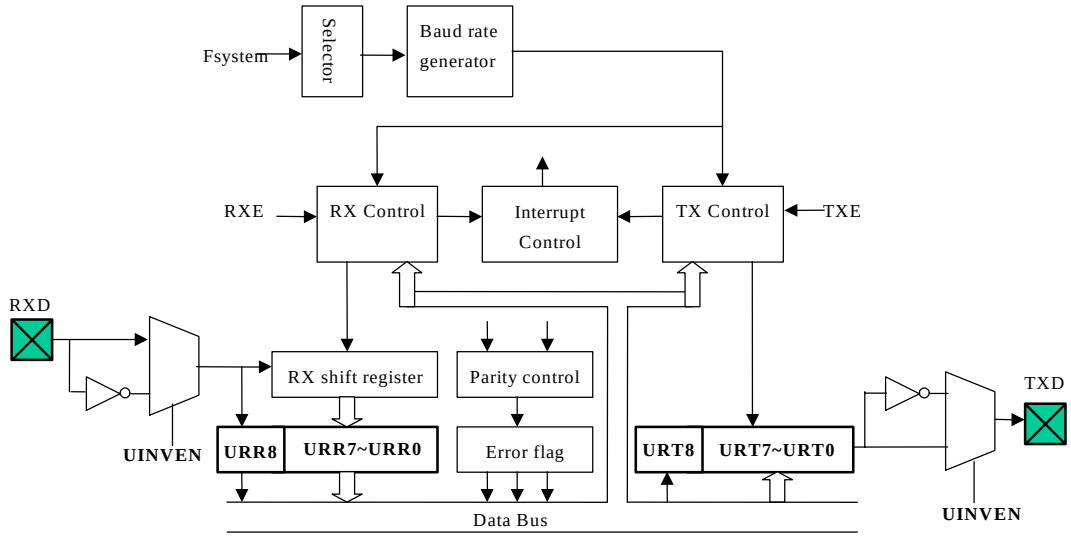


Fig 10: UART function block

Bit 7 : Unused

R5 Program page selection , CNT CLK & scale setting , CNT1 data(L)

PAGE0 Program page

7	6	5	4	3	2	1	0
	PS6	PS5	PS4	PS3	PS2	PS1	PS0
X	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 6 (PS0 ~ PS6) : Program page selection bits

PS6	PS5	PS4	PS3	PS2	PS1	PS0	Program memory page (Address)
0	0	0	0	0	0	0	Page 0
0	0	0	0	0	0	1	Page 1
0	0	0	0	0	1	0	Page 2
0	0	0	0	0	1	1	Page 3
		:	:	:	:	:	:
		:	:	:	:	:	:
1	1	1	1	1	1	0	Page 126
1	1	1	1	1	1	1	Page 127

User can use PAGE instruction to change page to maintain program page by user.

Bit 7 : .This bit is undefined and not allowed to use.

PAGE1 Counter1 Counter2 CLK and scale setting

7	6	5	4	3	2	1	0
CNT2S	C2P2	C2P1	C2P0	CNT1S	C1P2	C1P1	C1P0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 2(C1P0~C1P2) : Counter1 scaling

C1P2	C1P1	C1P0	COUNTER1
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (CNT1S) : Counter1 clock source
0/1 ➔ 16.384kHz/instruction clock

Bit 4~Bit 6(C2P0~C2P2) : Counter2 scaling. Prescaler is as different as Bit 0~Bit 2.

C2P2	C2P1	C2P0	COUNTER2
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 7 (CNT2S) : Counter2 clock source
0/1 ➔ 16.384kHz/instruction clock

PAGE2 Counter 1 Low 8bit Data buffer

7	6	5	4	3	2	1	0
CN17	CN16	CN15	CN14	CN13	CN12	CN11	CN10
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7(CN10~CN17) : Counter1's data buffer

Counter1 is a 16 bits up-counter with 8-bit prescaler and user can read or write the counter through R5 page2 and R6 page2. After a interruption, it will reload the preset value.

```
Example: write:   MOV   0x05,A   ; write the data at accumulator to counter1 (preset)
Example: read:    MOV   A,0x05   ; read R5 data and write to accumulator
Example: write:   MOV   0x06,A   ; write the data(high 8 bits) at accumulator to counter1
Example: read:    MOV   A,0x06   ; read R6 data(high 8 bits) and write to accumulator
```

PAGE3 DA Control

7	6	5	4	3	2	1	0
				CDAS	CDAL2	CDAL1	CDAL0
				R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 2 (CDAL0 ~ CDAL2) : change output level of current DA

CDAL2	CDAL1	CDAL0	Output level
0	0	0	L0 (ratio = 1/8)
0	0	1	L1 (ratio = 2/8)
0	1	0	L2 (ratio = 3/8)
0	1	1	L3 (ratio = 4/8)
1	0	0	L4 (ratio = 5/8)
1	0	1	L5 (ratio = 6/8)
1	1	0	L6 (ratio = 7/8)
1	1	1	L7 (ratio =1)

Bit 3 (CDAS) : Current DA switch
0 ➔ normal PORTD7
1 ➔ Current DA output

Bit 4 ~ Bit 7 : Undefined Register. These bits are undefined and not allowed to use.

R6 Port 6 I/O Data , Data ROM data buffer,CNT1 Data(H),DA control

PAGE0 Port 6 I/O Data

7	6	5	4	3	2	1	0
P67	P66	P65	P64	P63	P62	P61	P60
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (P60 ~ P67) : 8-bit PORT6 (0~7) I/O data register
User can use IOC register to define input or output each bit..

PAGE1 Data ROM Data buffer

7	6	5	4	3	2	1	0
DRD7	DRD6	DRD5	DRD4	DRD3	DRD2	DRD1	DRD0
R	R	R	R	R	R	R	R

Bit 0 ~ Bit 7 (DRD0 ~ DRD7) : Data ROM data buffer for ROM reading.
Example.

```
MOV   A,@1
MOV   R7_PAGE1,A
MOV   A,@0
MOV   R8_PAGE1,A
MOV   A,@0
MOV   R9_PAGE1,A
MOV   A,R6_PAGE1        ;read the data at Data ROM which address is "00001".
```

PAGE2 Counter1 high 8bit Data buffer

7	6	5	4	3	2	1	0
CN1F	CN1E	CN1D	CN1C	CN1B	CN1A	CN19	CN18
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7(CN18~CN1F) : Counter1's high 8 bits data buffer. Please refer to R5 page2 counter1 low 8 bit data buffer for detail.

PAGE3 DA Control

7	6	5	4	3	2	1	0
DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (DA2 ~ DA9) : Current DA most significant 8 bits of Current DA output buffer
Combine these 8 bits and R9 page3 bit4~bit5 2 bits as complete 10 bits Current DA output

data. Control register bit3 is Current DA power control .

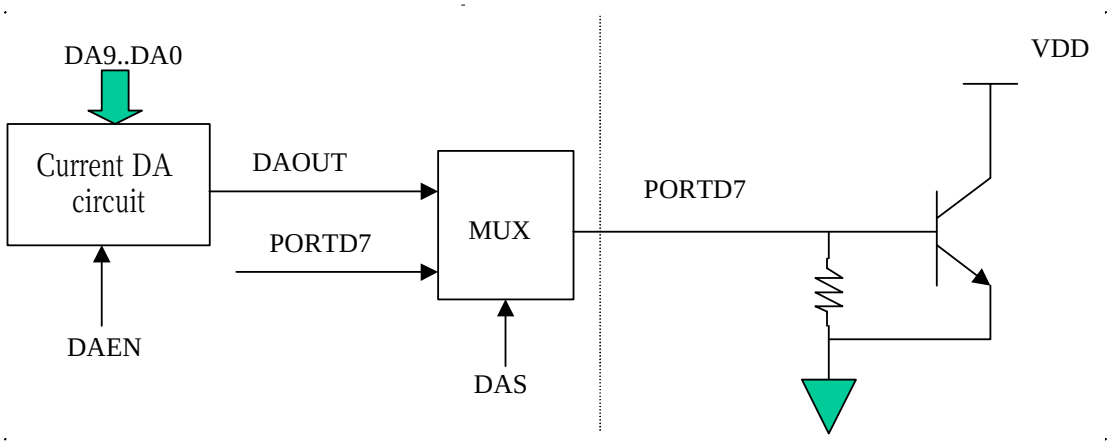


Fig 11: Current DA structure

R7 Port 7 I/O Data , Data ROM address , CNT2 Data , SPI control

PAGE0 Port 7 I/O Data

7	6	5	4	3	2	1	0
P77	P76	P75	P74	P73	P72	P71	P70
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (P70 ~ P77) : 8-bit PORT7(0~7) I/O data register
User can use IOC register to define input or output each bit.

PAGE1 Data ROM address

7	6	5	4	3	2	1	0
DRA7	DRA6	DRA5	DRA4	DRA3	DRA2	DRA1	DRA0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (DRA0 ~ DRA7) : Data ROM address (0~7) for ROM reading

PAGE2 Counter2 Data buffer

7	6	5	4	3	2	1	0
CN27	CN26	CN25	CN24	CN23	CN22	CN21	CN20
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7(CN20~CN27) : Counter2's data buffer
User can read and write this buffer. Counter2 is a eight bit up-counter with 8-bit prescaler that user can use R7 page2 to preset and read the counter. (write = preset) After a interruption, it will reload the preset value.
Example: write: MOV 0x07 , A ; write the data at accumulator to counter1 (preset)
Example: read: MOV A , 0x07 ; read R7 data and write to accumulator

PAGE3 SPI Control Register

7	6	5	4	3	2	1	0
RBF	SPIE	SRO	SE	SCES	SBR2	SBR1	SBR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Fig.12 shows how SPI to communicate with other device by SPI module. If SPI is a master controller, it

sends clock through the SCK pin. An 8-bit data is transmitted and received at the same time. If SPI, however, is defined as a slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted on a basis of both the clock rate and the selected edge.

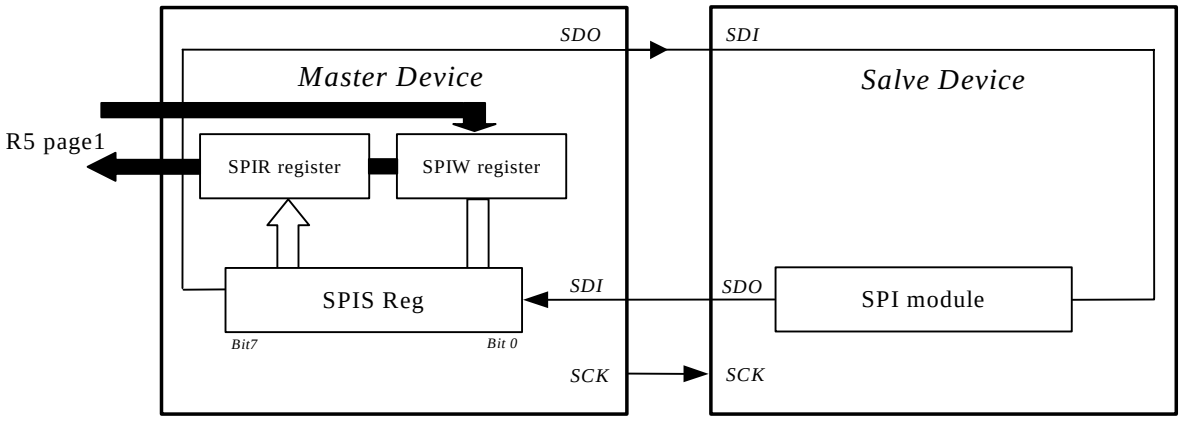


Fig 12: Single SPI Master / Salve Communication

Bit 0 ~ Bit 2 (SBR0 ~ SBR2) : SPI baud rate selection bits

SBR2	SBR1	SBR0	Mode	Baud rate
0	0	0	Master	Fsco
0	0	1	Master	Fsco/2
0	1	0	Master	Fsco/4
0	1	1	Master	Fsco/8
1	0	0	Master	Fsco/16
1	0	1	Master	Fsco/32
1	1	0	Slave	
1	1	1	X	

<Note> Fsco = CPU instruction clock

For example:

If PLL enable and RA PAGE0 (Bit5,Bit4)=(1,1), instruction clock is 3.58MHz/2 ➔ Fsco=3.5862MHz/2

If PLL enable and RA PAGE0 (Bit5, Bit4)=(0,0), instruction clock is 0.895MHz/2 ➔ Fsco=0.895MHz/2

If PLL disable, instruction clock is 32.768kHz/2 ➔ Fsco=32.768kHz/2.

Bit 3 (SCES) : SPI clock edge selection bit

1 ➔ Data shifts out on falling edge, and shifts in on rising edge. Data is hold during the high level.

0 ➔ Data shifts out on rising edge, and shifts in on falling edge. Data is hold during the low level.

Bit 4 (SE) : SPI shift enable bit

1 ➔ Start to shift, and keep on 1 while the current byte is still being transmitted.

0 ➔ Reset as soon as the shifting is complete, and the next byte is ready to shift.

<Note> This bit has to be reset in software.

Bit 5 (SRO) : SPI read overflow bit

1 ➔ A new data is received while the previous data is still being hold in the SPIB register. In this situation, the data in SPIS register will be destroyed. To avoid setting this bit, users had better to read SPIB register even if the transmission is implemented only.

0 ➔ No overflow

<Note> This can only occur in slave mode.

Bit 6 (SPIE) : SPI enable bit

1 ➔ Enable SPI mode

0 ➔ Disable SPI mode

Bit 7 (RBF) : SPI read buffer full flag

1 ➔ Receive is finished, SPIB is full.

0 ➔ Receive is not finish yet, SPIB is empty.

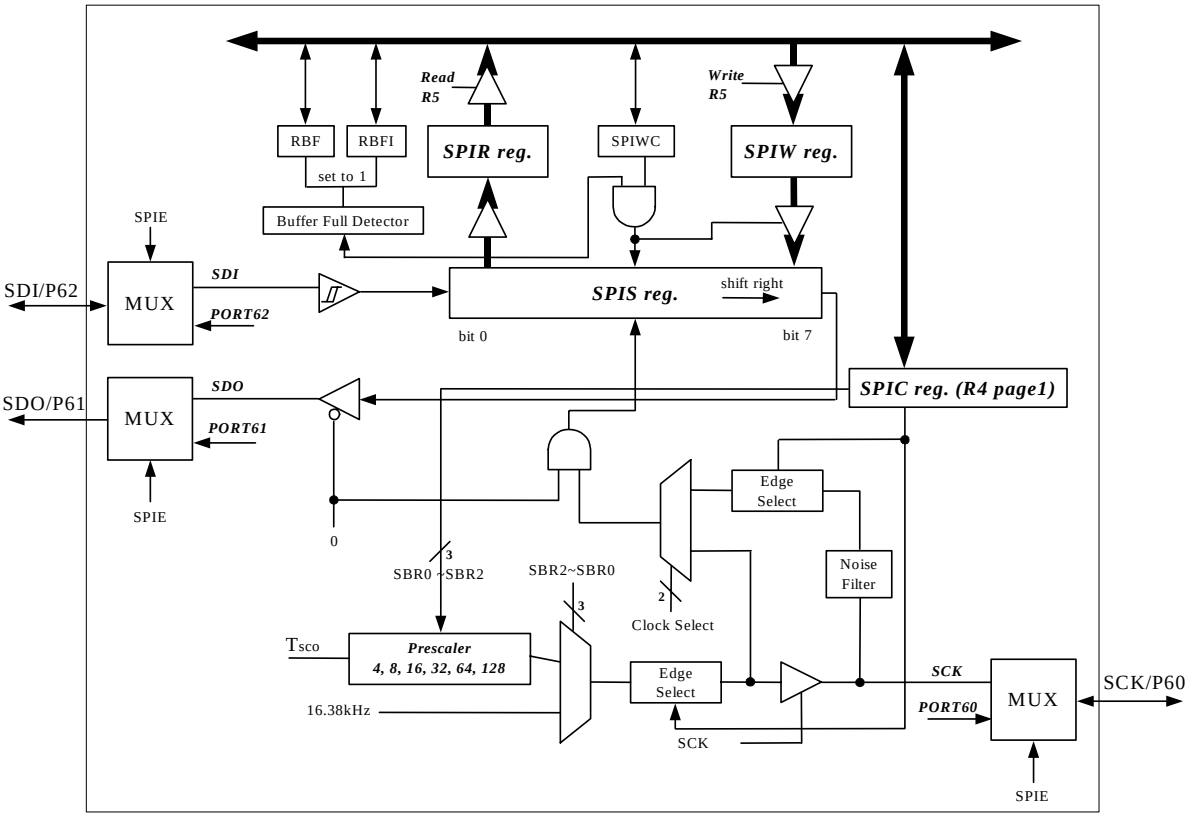


Fig.13 SPI Structure

SPIC reg. : SPI control register

SDO/P61 : Serial data out

SDI/P62 : Serial data in

SCK/P60 : Serial clock

RBF : Set by buffer full detector, and reset in software.

RBFI : Interrupt flag. Set by buffer full detector, and reset in software.

Buffer Full Detector : Sets to 1, while an 8-bit shifting is complete.

SE : Loads the data in SPIW register, and begin to shift

SPIE : SPI control register

SPIS reg. : Shifting byte out and in. The MSB will be shifted first. Both the SPIS register and the SPIW register are loaded at the same time. Once data being written to, SPIS starts transmission / reception. The received data will be moved to the SPIR register, as the shifting of the 8-bit data is complete. The RBF (Read Buffer Full) flag and the RBFI(Read Buffer Full Interrupt) flag are set.

SPIR reg. : Read buffer. The buffer will be updated as the 8-bit shifting is complete. The data must be read before the next reception is finished. The RBF flag is cleared as the SPIR register read.

SPIW reg. : Write buffer. The buffer will deny any write until the 8-bit shifting is complete. The SE bit will be kept in 1 if the communication is still under going. This flag must be cleared as the shifting is finished. Users can determine if the next write attempt is available.

SBR2 ~ SBR0: Programming the clock frequency/rates and sources.

Clock select : Selecting either the internal instruction clock or the external 16.338KHz clock as the shifting clock.

Edge Select : Selecting the appropriate clock edges by programming the SCES bit

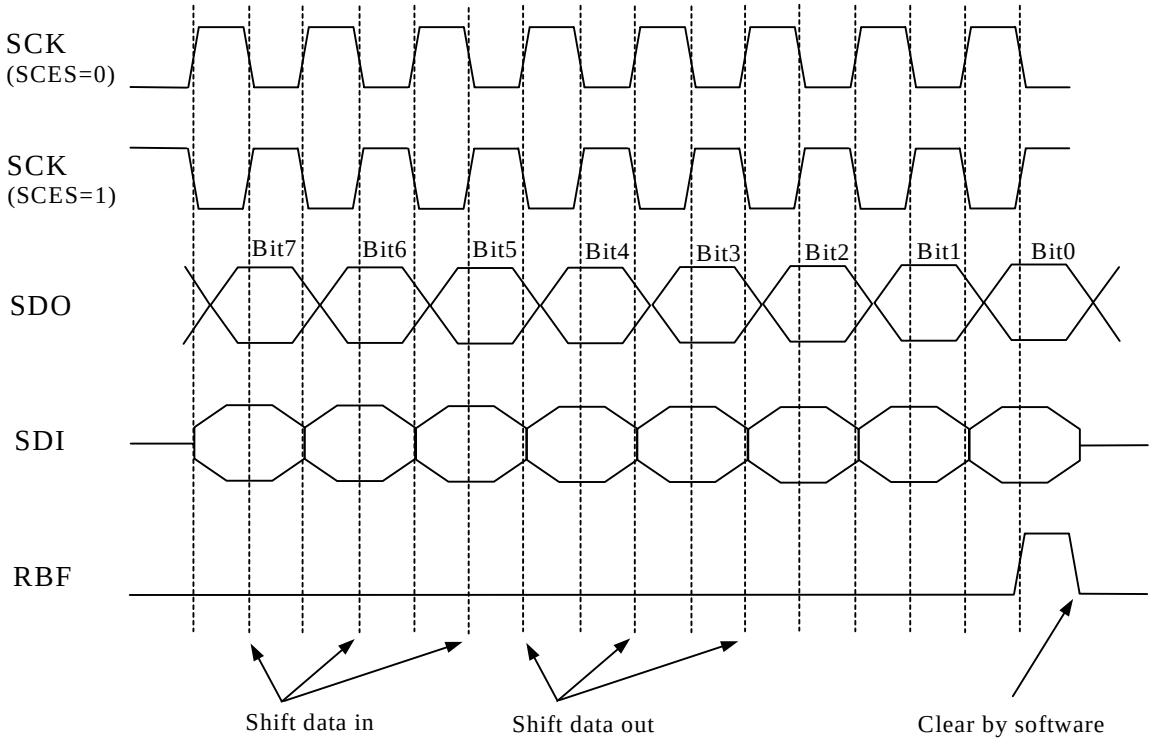


Fig.14: SPI timing

R8 Port 8 I/O Data , Data ROM address , DTMF receiver , SPI Data

PAGE0 Port 8 I/O Data

7	6	5	4	3	2	1	0
P87	P86	P85	P84	P83	P82	P81	P80
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (P80 ~ P87) : 8-bit PORT8 (0~7) I/O data register
User can use IOC register to define input or output each bit.

PAGE1 Data ROM address

7	6	5	4	3	2	1	0
DRA15	DRA14	DRA13	DRA12	DRA11	DRA10	DRA9	DRA8
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (DRA8 ~ DRA15) : Data ROM address (8~15) for ROM reading

PAGE2 DTMF Receive

7	6	5	4	3	2	1	0
CMPFLAG	STD	-	-	Q4	Q2	Q1	Q0
R	R/W-0	X	X	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 3 (Q1 ~ Q4) : DTMF receiver decoding data

To provide the code corresponding to the last valid tone-pair received (see code table). STD signal which steering output presents a logic high when a received tone-pair has been registered and the Q4 ~ Q1 output latch updated and generate a interruption (IOCF has enabled); returns to logic low when the voltage on ST/GT falls below Vtst.

F low	F high	Key	DREN	Q4~Q1
697	1209	1	1	0001
697	1336	2	1	0010
697	1477	3	1	0011
770	1209	4	1	0100
770	1336	5	1	0101
770	1477	6	1	0110
852	1209	7	1	0111
852	1336	8	1	1000
852	1477	9	1	1001
941	1209	0	1	1010
941	1336	*	1	1011
941	1477	#	1	1100
697	1633	A	1	1101
770	1633	B	1	1110
852	1633	C	1	1111
941	1633	D	1	0000
Any	Any	Any	0	xxxx (x:unknown)

Bit 4~Bit 5: Undefined Register.

Bit 6 (STD) : Delayed steering output.

Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V tst.

0/1 ➔ Data invalid/data valid

Be sure open main clock before using DTMF receiver circuit . A logic"0,0" applied to R5 page3 b4 and b3 will shut down power of the device to minimize the power consumption in a standby mode. It stops functions of the filters.

In many situations not requiring independent selection of receive and pause, the simple steering circuit of is applicable. Component values are chosen according to the following formulae:

t REC = t DP + t GTP t ID = t DA + t GTA

The value of t DP is a parameter of the device and t REC is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 uF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t REC of 30mS would be 300k.

Different steering arrangements may be used to select independently the guard-times for tone-present (t GTP) and tone-absent (t GTA). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and inter digital pause.

Guard-time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t REC improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t REC with a long t DO would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be required.

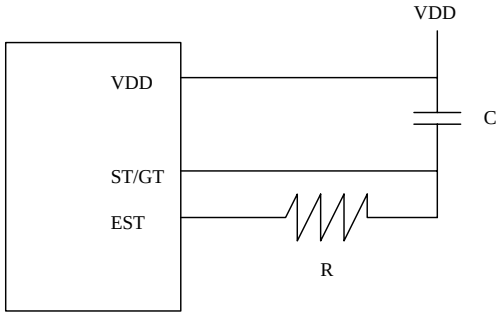


Fig.15 : DTMF receiver delay time control

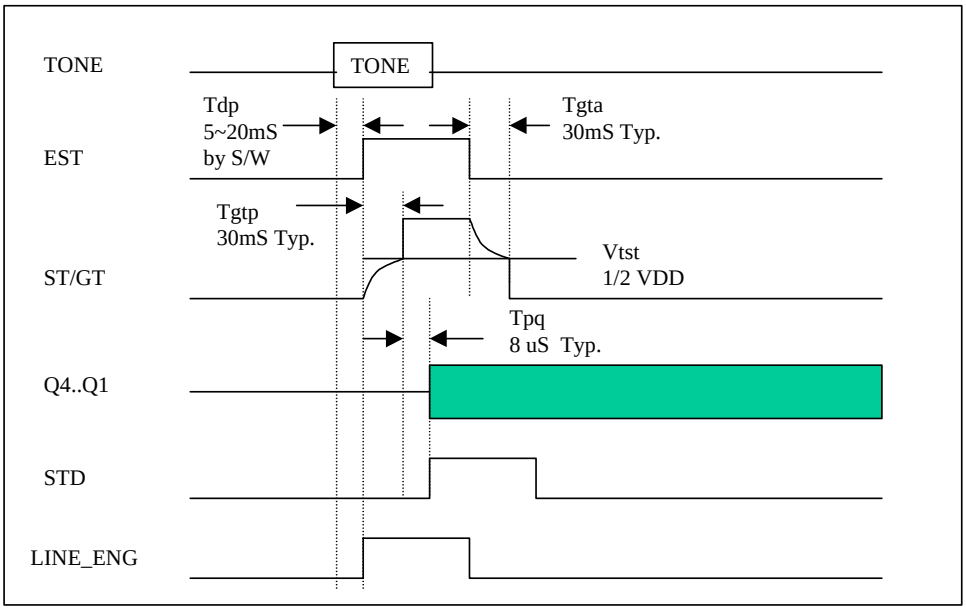


Fig.16 DTMF receiver timing.

Bit 7 (CMPFLAG) : Comparator output flag

0 ➔ Input voltage < reference voltage

1 ➔ Input voltage > reference voltage

<Note>Please refer to RA page 2 comparator control register .

PAGE3 SPI Data buffer

7	6	5	4	3	2	1	0
SPIB7	SPIB6	SPIB5	SPIB4	SPIB3	SPIB2	SPIB1	SPIB0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (SPIB0 ~ SPIB7) : SPI data buffer

If you write data to this register, the data will write to SPIW register. If you read this data, it will read the data from SPIR register. Please refer to Fig.9

R9 Port 9 I/O Data , Data ROM address , Key tone control

PAGE0 Port 9 I/O Data

7	6	5	4	3	2	1	0
P97	P96	P95	P94	P93	P92	P91	P90
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (P90 ~ P97) : 8-bit PORT9 (0~7) I/O data register
User can use IOC register to define input or output each bit.

PAGE1 Data ROM address

7	6	5	4	3	2	1	0
			DRA20	DRA19	DRA18	DRA17	DRA16
			R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 4 (DRA16 ~ DRA20) : Data ROM address(16~20) for ROM reading..
Bit 5~Bit 7 : Unused

PAGE2 FSK/CW/DTMF Power select ,

7	6	5	4	3	2	1	0
PCTRL1	PCTRL0	ADCS3	ADCS2	ADCS1			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			

Bit 0 ~ Bit 1 : Unused
Bit 3 ~ Bit 5(ADCS1 ~ ADCS3) : PORT65 ~ PORT67 normal IO / CMP input control bit.
ADCSX = 1 ➔Comparator input
ADCSX = 0 ➔normal IO

Bit 6~Bit 7 (PCTRL0~PCTRL1) : FSK and DTMF power control bits

PCTRL1	PCTRL0	Select	Relation Register
0	0	FSK and DTMFr power off	-
0	1	FSK power on	RA PAGE0
1	0	DTMF receiver power on	R8 PAGE2
1	1	***Can not used***	

*Please do not set 1 to both the bits, or FSK and DTMFr function will fail..
*When User turn on DTMF receiver power, PORT60 and PORT61 will switch to /STGT and EST pin.

PAGE3 KEY Tone Control

7	6	5	4	3	2	1	0
URT8	URR8	DA1	DA0	URINV	KT1	KT0	KTS
R/W-X	R	R/W-X	R/W-X	R/W-X	R/W-0	R/W-0	R/W-0

Bit 0 (KTS) : Key tone output switch
0 ➔ normal PORT76
1 ➔ key tone output .
Bit 1 ~ Bit 2 (KT0 ~ KT1) : Key tone output frequency and its power control

KT1	KT0	Key tone frequency and power
0	0	32.768KHz/32 = 1.024kHz clock and enable
0	1	32.768KHz/16 = 2.048kHz clock and enable
1	0	32.768KHz/8 = 4.096kHz clock and enable
1	1	Power off key tone

Bit 3(URINV) : Enable UART TXD, RXD port inverse output
0➔ Disable UART TXD, RXD port inverse output
1➔ Enable UART TXD, RXD port inverse output

Bit 4 ~ Bit 5(DA0~DA1) : These two bits are the least significant 2 bits of Current DA. Combine R6 PAGE3 and these 2 bits as complete 10 bits Current DA output data.
Bit 6(URR8) : MSB of UART receiver data buffer.

Bit 7(URT8) : MSB of UART transmitter data buffer.

RA CPU Power saving , main CLK select , FSK , WDT timer Comparator control , Tone1 generator

PAGE0 Power saving , main CLK select , FSK , WDT timer

7	6	5	4	3	2	1	0
0	PLLEN	CLK1	CLK0	**ROMRI**	FSKDATA	/CD	WDTEN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R	R	R/W-0

Bit 0 (WDTEN) : Watch dog control register

User can use WDTC instruction to clear watch dog counter. The counter 's clock source is 32768/2 Hz. If the prescaler assigns to TCC. Watch dog will time out by (1/32768)*2 * 256 = 15.616ms. If the prescaler assigns to WDT, the time of time out will be more times depending on the ratio of prescaler.

0/1 ➔ disable/enable

Bit 1 (/CD) : FSK carrier detect indication

0/1 ➔ Carrier Valid/Carrier Invalid

It's a read only signal. If FSK decoder detect the energy of mark or space signal. The Carrier signal will go to low level. Otherwise it will go to high.. Note!! Should be at normal mode.

Bit 2 (FSKDATA) : FSK decoding data output

It's a read only signal. If FSK decode the mark or space signal , it will output high level signal or low level signal at this register. It's a raw data type. That means the decoder just decode the signal and has no process on FSK signal. Note!! Should be at normal mode.

User can use FSK data falling edge interrupt function to help data decoding.

Example:

```
MOV   A,@01000000
IOW   IOCF                ;enable FSK interrupt function
CLR   RF
ENI                       ;wait for FSK data's falling edge
:
```

0 = Space data (2200Hz)

1 = Mark data (1200Hz)

FSK block power is controlled by R5 page3 bit3,4. When PCTRI1=0 and PCTRL0=1 , FSK power on.

The relation between R5 bit3 to bit4 and RA bit1 to bit 2 are show in Fig.17. You have to power FSK decoder up first, then wait a setup time (Tsup) and check carrier signal (/CD). If the carrier is low, program can process the FSK data.

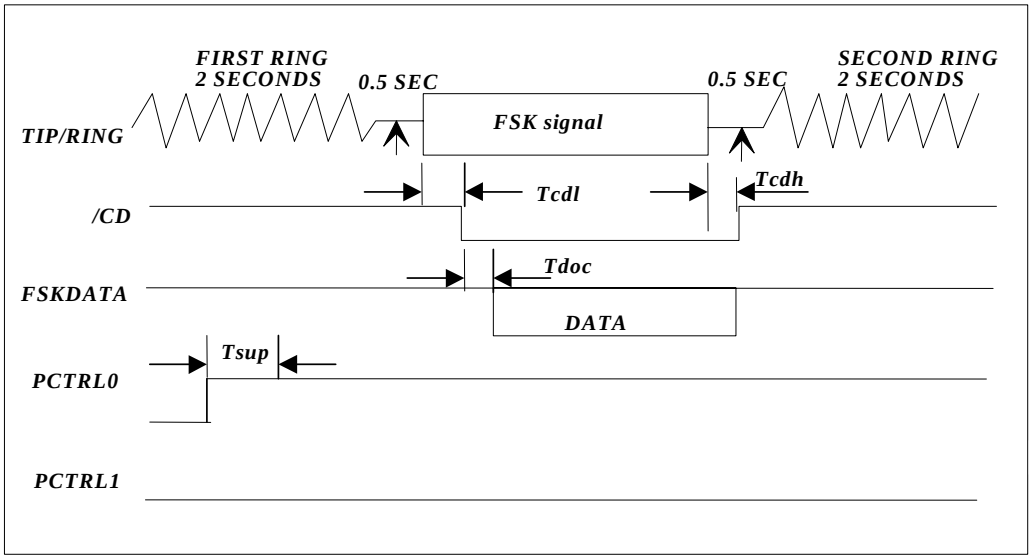


Fig.17: The relation between R5 bit3 to bit4 and RA bit1 to bit 2

The controller is a CMOS device designed to support the Caller Number Deliver feature which is offered by the Regional Bell Operating Companies. The FSK block comprises one path: the signal path. The signal path consist of an input differential buffer, a band pass filter, an FSK demodulator and a data valid with carrier detect circuit.

In a typical application, user can use his own external ring detect output as a triggering input to IO port. User can use this signal to wake up whole chip by external ring detect signal. By setting “0,1” to R5 b4 and b3 (PCTRL1 & PCTRL0) of register RA to activate the block of FSK decoder. If b4 and b3 of register R5 is set to “0,1”, the block of FSK decoder will be powered down.

The input buffer accepts a differential AC coupled input signal through the TIP and RING input and feeds this signal to a band pass filter. Once the signal is filtered, the FSK demodulator decodes the information and sends it to a post filter. The output data is then made available at bit 2 (FSKDATA) of register RA. This data, as sent by the central office, includes the header information (alternate "1" and "0") and 150 ms of marking which precedes the date, time and calling number. If no data is present, the bit 2 (DATA) of register RA is held on “1” state. This is accomplished by an carrier detect circuit which determines if the in-band energy is high enough. If the incoming signal is valid, bit 1 (/CD) of register RA will be “0” otherwise it will be held on “1”. And thus the demodulated data is transferred to bit 2 (DATA) of register RA. If it is not, then the FSK demodulator is blocked.

Bit 3 (ROMRI) : External Data ROM read data address auto_increase enable.

RO_IDEN	ROMRI	Result
0	**X**	**Regardless Read/Write external Data ROM, Address flag cannot increase or decrease.**
1	**0**	**Address flag will auto_increase or decrease after Read/Write external Data ROM**
1	**1**	**Address flag will auto_increase or decrease after Write external Data ROM, but address flag is constant after read external Data ROM.**

Bit 4 ~ Bit 5 (CLK0 ~ CLK1) : Main clock selection bits

User can choose different frequency of main clock by CLK1 and CLK2. All the clock selection is list below.

PLLEN	CLK1	CLK0	Sub clock	MAIN clock	CPU clock
1	**0**	**0**	**32.768kHz**	**5.374MHz**	**5.374MHz (Normal mode)**
1	0	1	32.768kHz	1.7913MHz	1.7913MHz (Normal mode)
1	1	0	32.768kHz	10.7479MHz	10.7479MHz (Normal mode)
1	1	1	32.768kHz	3.5826MHz	3.5826MHz (Normal mode)
0	Don't care	don't care	32.768kHz	Don't care	32.768kHz (Green mode)
0	Don't care	don't care	32.768kHz	Don't care	32.768kHz (Green mode)
0	Don't care	don't care	32.768kHz	Don't care	32.768kHz (Green mode)
0	Don't care	don't care	32.768kHz	Don't care	32.768kHz (Green mode)

Bit 6 (PLLEN) : PLL enable control bit

It is CPU mode control register. If PLL is enabled, CPU will operate at normal mode (high frequency , main clock); otherwise, it will run at green mode (low frequency, 32768 Hz).

0/1 ➔ disable/enable

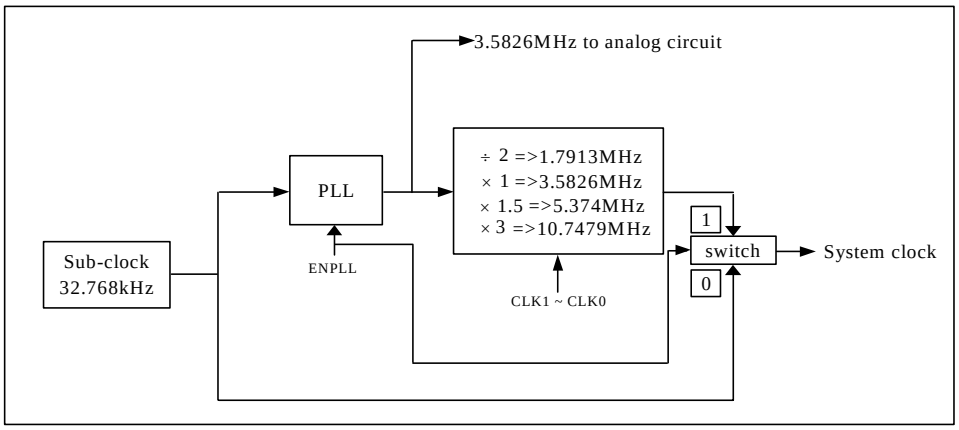


Fig.18 The relation between 32.768kHz and PLL

Bit 7: Unused register. Always keep this bit to 0 or some un-expect error will happen!

Wakeup signal	SLEEP mode	GREEN mode	NORMAL mode
	RA(7,6)=(0,0) + SLEP	RA(7,6)=(x,0) no SLEP	RA(7,6)=(x,1) no SLEP
TCC time out IOCF bit 0=1 And "ENI"	No function	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
COUNTER1 time out IOCF bit 1=1 And "ENI"	No function	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
COUNTER2 time out IOCF bit 2=1 And "ENI"	No function	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
WDT time out	RESET and	RESET and Jump	RESET and

	Jump to address 0	to address 0	Jump to address 0
PORT7 Any one bit in IOCE page0 = 1 And "ENI"	RESET and Jump to address 0	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
DED interrupt IOCE page1 bit 6 = 1 And RF bit3 logic level variation (switch by EDGE bit) And “ENI”	No function	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)

<Note> PORT70 ~ PORT76 's wakeup function is controlled by IOCE PAGE0 bit 0~bit 6 and ENI instruction. They are falling edge trigger.
PORT77 's wakeup function is controlled by IOCE PAGE0 bit 7. It can be trigger in falling edge or rising edge (controlled by CONT register).

PAGE1 Undefined Register

This Register is not allowed to use.

PAGE2 Comparator control Register

7	6	5	4	3	2	1	0
CMPEN	CMPREF	CMPS1	CMPS0	CMPB3	CMPB2	CMPB1	CMPB0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

If user define PORT63 , PORT64 or PORT65 (by ADCS1, ADCS2, ADCS3 at R9 page2) as a comparator input or PORT6. User can use this register to control comparator's function.

Bit 0~Bit 3(CMPB0 ~ CMPB3) : Reference voltage selection of internal bias circuit for comparator.
Reference voltage for comparator = VDD x (N + 0.5)/ 16 , N = 0 to 15

Bit 4~Bit 5(CMPS0~CMPS1) : Channel selection from CMP1 to CMP3 for comparator

CMPS1	CMPS0	Input
0	0	CMP1
0	1	CMP2
1	0	CMP3
1	1	Reserved

Bit 6(CMPREF) : Switch for comparator reference voltage type
0 ➔ internal reference voltage
1 ➔ external reference voltage

Bit 7(CMPEN) : Enable control bit of comparator.
0/1 ➔ disable/enable, When CMPEN bit set to “0” , 2.0V ref circuit will powered off.
The relation between these registers shown in Fig.19.

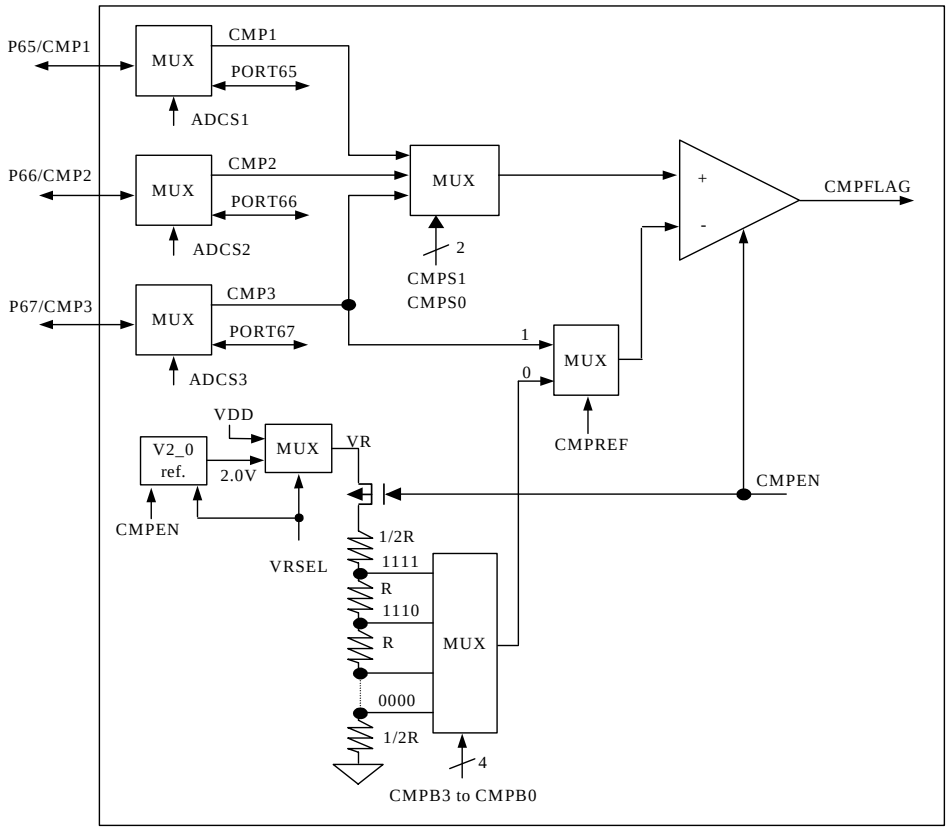


Fig.19: Comparator circuit

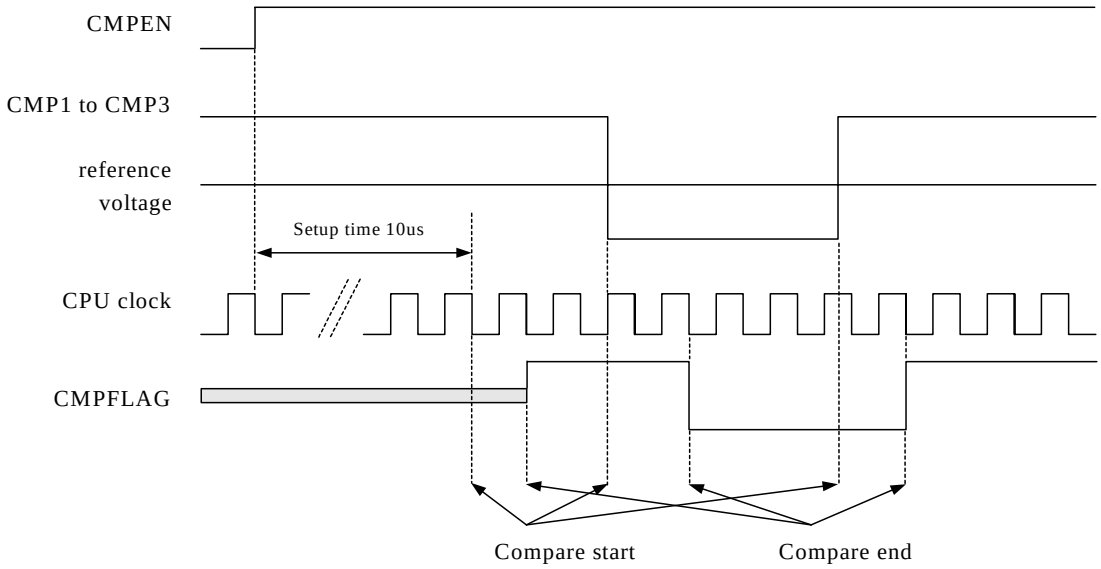


Fig.20: Comparator timing

PAGE3 Tone 1 Control Register

7	6	5	4	3	2	1	0
T17	T16	T15	T14	T13	T12	T11	T10
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7(T10~T17) : Tone generator1 frequency divider and power control

Please Run in Normal mode .

Clock source = 85300Hz

T17~T10 = '11111111' ➔Tone generator1 will has 334(85300/255) Hz SIN wave output.

:

:

T17~T10 = '00000010' ➔Tone generator1 will has 41150(85300/2) Hz SIN wave output.

T17~T10 = '00000001' ➔DC bias voltage output

T17~T10 = '00000000' ➔Power off

Built-in tone generator can generate dialing tone signals for telephone of dialing tone type or just a single tone. In DTMF application, there are two kinds of tone. One is the group of row frequency (TONE1), the other is the group of column frequency (TONE2), each group has 4 kinds of frequency, user can get 16 kinds of DTMF frequency totally. Tone generator contains a row frequency sine wave generator for generating the DTMF signal which selected by RA page3 and a column frequency sine wave generator for generating the DTMF signal which selected by RB page3. This block can generate single tone by filling one of these two register.

If all the values are low, the power of tone generators will turn off .

		TONE2 (RB page3) High group freq.			
		1201.4Hz (0X47)	1332.8Hz (0X40)	1470.7Hz (0X3A)	1640.4Hz (0X34)
TONE1(RA page3)	699.2Hz(0x07A)	1	2	3	A
	768.5Hz(0x06F)	4	5	6	B
Low group freq.	853.0Hz(0x064)	7	8	9	C
	937.4Hz(0x05B)	*	0	#	D

Also TONE1 and TONE2 are an asynchronous tone generator so the both can be used to generate Caller ID FSK signal. In FSK generator application, TONE1 or TONE2 can generate 1200Hz Mark bit and 2200Hz Space bit for Bell202 or 1300Hz Mark bit and 2100Hz Space bit for V.23. See the following table.

TONE1(IOCC PAGE1) or TONE2(IOCD PAGE1)	Freq. (Hz)	meaning
0x47	1201.4	Bell202 FSK Mark bit
0x27	2187.2	Bell202 FSK Space bit
0x42	1292.4	V.23 FSK Mark bit
0x29	2080.5	V.23 FSK Space bit

Tone generator can also generate CW or SMS signal. See the following table.

TONE1(IOCC PAGE1) or TONE2(IOCD PAGE1)	Freq. (Hz)	meaning
0x28	2132.5	CAS freq
0x1F	2751.6	CAS freq

RB Port B I/O Data, Key strobe , Tone 2 generator

PAGE0 Port B I/O Data

7	6	5	4	3	2	1	0
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (PB0 ~ PB7) : 8-bit PORTB (0~7) I/O data register
User can use IOC register to define input or output each bit.

PAGE1 Undefined Register

This Register is not allowed to use.

PAGE2 KEY Strobe Control Register

7	6	5	4	3	2	1	0
STRB7	STRB6	STRB5	STRB4	STRB3	STRB2	STRB1	STRB0
R	R	R	R	R	R	R	R

Bit 0 ~ Bit 7 (STRB0 ~ STRB7) : Key strobe control bits
These key strobe control registers correspond to Port80 ~ Port87 . Please refer to KEYSTOBE explanation (RE page3).

PAGE3 Tone 2 Control Register

7	6	5	4	3	2	1	0
T27	T26	T25	T24	T23	T22	T21	T20
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7(T20~T27) : Tone generator1's frequency divider and power control. Please refer to RA Page3 Tone1 control register for detail.

RC Port C I/O Data , Data RAM data buffer , Tone 2 generator

PAGE0 Port C I/O Data

7	6	5	4	3	2	1	0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (PC0 ~ PC7) : 8-bit PORTC (0~7) I/O data register
User can use IOC register to define input or output each bit.

PAGE1 Data RAM data buffer1

7	6	5	4	3	2	1	0
RAM1D7	RAM1D6	RAM1D5	RAM1D4	RAM1D3	RAM1D2	RAM1D1	RAM1D0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (RAM1D0 ~ RAM1D7) : Data RAM data buffer1 for RAM reading or writing.
Example.

```
MOV    A,@1
MOV    RD_PAGE1,A
MOV    A,@0
MOV    RE_PAGE1,A
MOV    A,@0x55
MOV    RC_PAGE1,A      ;write data 0x55 to DATA RAM which address is "0001".
MOV    A,RC_PAGE1      ;read data
  :
```

PAGE2 KEY Strobe Control Register

7	6	5	4	3	2	1	0
STRB15	STRB14	STRB13	STRB12	STRB11	STRB10	STRB9	STRB8
R	R	R	R	R	R	R	R

Bit 0 ~ Bit 7 (STRB8 ~ STRB15) : Key strobe control bits
These key strobe control registers correspond to Port90 ~ Port97 . Please refer to KEYSTOBE explanation (RE page3).

PAGE3 Undefined Register

This Register is not allowed to use.

RD PORT D I/O Data , Data RAM address

PAGE0 PORT D I/O Data , Data RAM address

7	6	5	4	3	2	1	0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (PD0 ~ PD7) : 7-bit PORTD (0~6) I/O data register
User can use IOC register to define input or output each bit.

PAGE1 Data RAM Address1(Low 8 bits)

7	6	5	4	3	2	1	0
RAM1A7	RAM1A6	RAM1A5	RAM1A4	RAM1A3	RAM1A2	RAM1A1	RAM1A0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0~Bit 7 (RAM1A0 ~ RAM1A7) : Data RAM address1 (address0 to address7) for RAM reading or writing

PAGE2 Undefined Register

PAGE3 Undefined Register

These 2 Registers are not allowed to use.

RE Interrupt flag1 , Data RAM address1(H) CAS , Key Scan,

PAGE0 Interrupt flag1

7	6	5	4	3	2	1	0
INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Interrupt flag registers. User can only clear these bits from 1 to 0 but not set them from 0 to 1.

Bit 0 (INT0) : External INT0 pin interrupt flag
If PORT70 has a falling edge trigger signal. CPU will set this bit.

Bit 1 (INT1) : External INT1 pin interrupt flag
If PORT71 has a falling edge trigger signal. CPU will set this bit.

Bit 2 (INT2) : External INT2 pin interrupt flag
If PORT72 has a falling edge trigger signal. CPU will set this bit.

Bit 3 (INT3) : External INT3 pin interrupt flag
If PORT73 has a falling edge trigger signal. CPU will set this bit.

Bit 4 (INT4) : External INT4 pin interrupt flag
If PORT74 has a falling edge trigger signal. CPU will set this bit.

Bit 5 (INT5) : External INT5 pin interrupt flag
If PORT75 has a falling edge trigger signal. CPU will set this bit.

Bit 6 (INT6) : External INT6 pin interrupt flag
If PORT76 has a falling edge trigger signal. CPU will set this bit.

Bit 7 (INT7) : External INT7 pin interrupt flag

If PORT77 has a falling (or rising and falling) edge trigger signal. CPU will set this bit.

Signal	Trigger	<Note>
INT0 : INT6	Falling edge	
INT7	Falling/Falling & rising edge	Controlled by CONT register

PAGE1 Data RAM Address1(H)

7	6	5	4	3	2	1	0
				RAM1A11	RAM1A10	RAM1A9	RAM1A8
X	X	X	X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0~Bit 3(RAM1A8 ~ RAM1A11) : Data RAM address (address8 to address11) for RAM reading.

Bit 4~Bit 7 Undefined Register. ***These registers are not sure to be 0 or 1. Please don't use them.***

PAGE2 CAS detected flag , Key Scan

7	6	5	4	3	2	1	0
CAS		KEYSTROB	KEYSCAN	LCD1	LCD0		
R	X	R/W-0	R/W-0	R/W-0	R/W-0	X	X

Bit 0~Bit 1 : ***Undefined register. These bits are not allowed to use.***

Bit 2~Bit 3 (LCD0~LCD1) : These two bits used to enable/disable key scan and LCD controller.

LCD1	LCD0	Sates
0	0	Key scan disable (ignore KEYSCAN bit) External LCD controller disable
0	1	Key scan disable (ignore KEYSCAN bit) External LCD controller disable
1	0	Key scan disable (ignore KEYSCAN bit) External LCD controller disable
1	1	Key scan enable (KEYSCAN bit must = 1) External LCD controller enable

Bit 4 (KEYSCAN) : Key scan function enable control bit.

0/1 ➔ disable/enable

If you enable key scan function (LCD0, LCD1 and KEYSCAN =1), PORT8 and PORT9 will pull high automatically and become key strobe pins . The key scan waveform is as follow below.

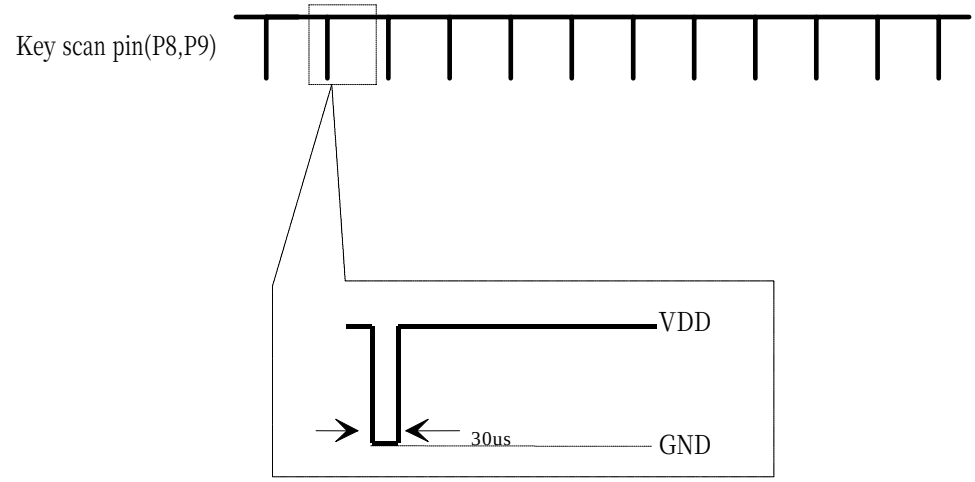


Fig.21 key scan waveform

Bit 5 (KEYSTRB) : Key strobe enable control bit

0/1 ➔ disable/enable

key strobe signal , if you set this bit , segment will switch to strobe signal temporally and output zero signal (one instruction long) one by one from PORT80 to PORT87 and PORT90 to PORT97. During one strobe time, CPU will check port7(0:3) equal to "1111" or not. If not, CPU will latch a zero at RB PAGE1 and RC PAGE1 one by one depends on which segment strobe. After strobe, this bit will be cleared . Fig.22 is key strobe signal.

One instruction

REGISTER

STROBE	RB(0)	RB(1)	RB(2)	RB(3)	RB(4)	RB(5)	RB(6)	RB(7)	RC(0)	RC(1)	RC(2)	RC(3)	RC(4)	RC(5)	RC(6)	RC(7)
PORT80	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
PORT81	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
PORT82	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
PORT83	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
PORT84	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
PORT85	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
PORT86	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
PORT87	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
PORT90	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
PORT91	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
PORT92	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
PORT93	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
PORT94	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
PORT95	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
PORT96	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
PORT97	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Fig.22 key strobe signal

Bit 6 Unused

Next figure is the relationship between KEYSCAN, KEYSTROBE .And fig.24 is key scan flow by interrupt trigger.

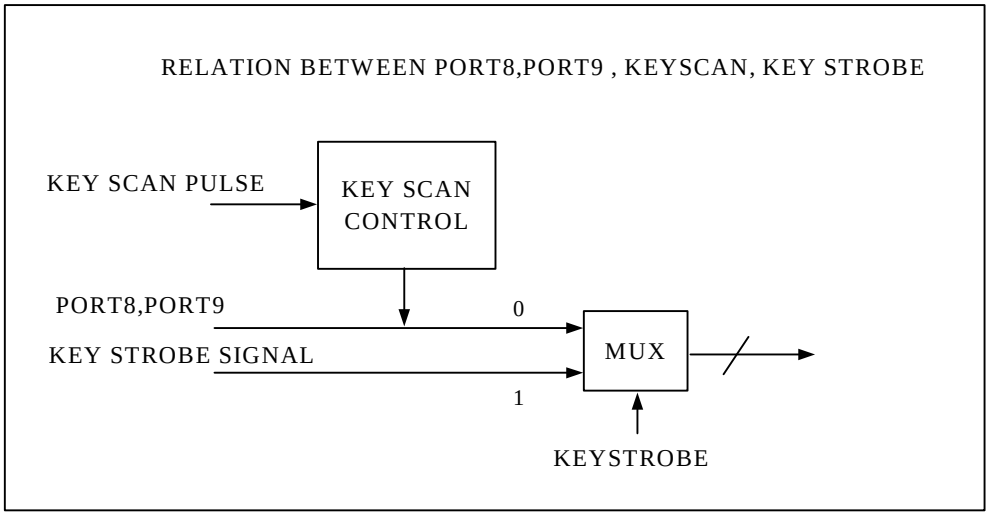


Fig.23 KEYSCAN, KEYSTROBE and segments.

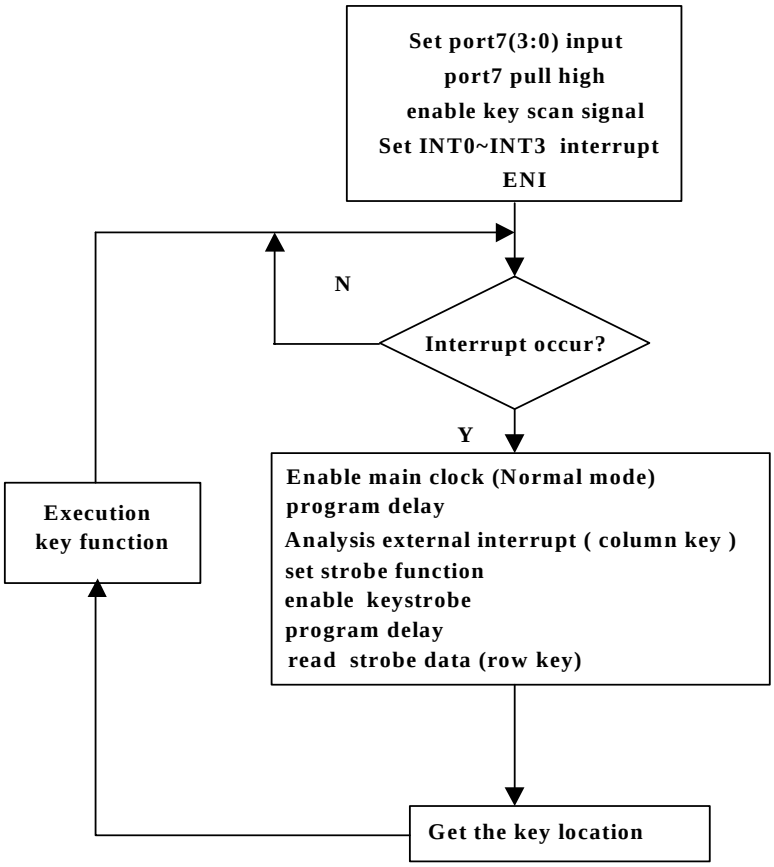


Fig.24 key scan flow by interrupt trigger

Bit 7 (CAS) : CALL WAITING decoding output
0/1 ➔ CW data valid / No data

PAGE3 UART transmitter data buffer

7	6	5	4	3	2	1	0
URT7	URT6	URT5	URT4	URT3	URT2	URT1	URT0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0~Bit 7(URT0~URT7) : Low 8 bit UART transmitter data buffer

RF Interrupt flag

7	6	5	4	3	2	1	0
RBF/STD	FSK/CW		UART	DED	CNT2	CNT1	TCC
R/W-0	R/W-0	X	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

"1" means interrupt request, "0" means non-interrupt

Bit 0 (TCC) : TCC timer overflow interrupt flag
Set when TCC timer overflows .

Bit 1 (CNT1) : Counter1 timer overflow interrupt flag
Set when counter1 timer overflows.

Bit 2 (CNT2) : Counter2 timer overflow interrupt flag
Set when counter2 timer overflows .

Bit 3 (DED) : Interrupt flag of Differential Energy Detector (DED) output data. If DEDD(RE page2 bit7) has a falling edge signal (or falling & rising edge signal , switch by IOCE page1 bit5), CPU will set this bit.

Bit 4 (UART) : Universal Asynchronous Receiver Transmitter interrupt flag. When transmitter buffer empty , receiver buffer full or receiver data error, this bit will be set.

Bit 5: Undefined register. These bits are not allowed to use.

Bit 6 (FSK/CW) : FSK data or Call waiting data interrupt flag.
If FSKDATA or CAS has a falling edge trigger signal, CPU will set this bit.

Bit 7 (RBF/STD) : SPI data transfer complete or DTMF receiver signal valid interrupt
If serial IO 's RBF signal has a rising edge signal (RBF set to "1" when transfer data completely), CPU will set this bit. Or DTMF receiver's STD signal has a rising edge signal (DTMF decode a DTMF signal).

IOCF is the interrupt mask register. User can read and clear.

Trigger edge as the table

Signal	Trigger	<Note>
TCC	Time out	
COUNTER1	Time out	8/16 bits select by CONT register
COUNTER2	Time out	
DED	Signal detect	
UART	Receiver full, Transmitter empty or error(if enable)	
FSK	Falling edge	
RBF/STD	Rising edge	

EM78815 MCU will store ACC,R3 status and R5 PAGE automatically after an interrupt is triggered. And it will be restored after instruction “RETI”.

PAGE1 External Data ROM

7	6	5	4	3	2	1	0
EXA8	EXA7	EXA6	EXA5	EXA4	EXA3	EXA2	EXA1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7(EXA1~EXA8) : Expanding Data ROM start address A1~A8

PAGE2 External Data ROM

7	6	5	4	3	2	1	0

EXA16	EXA15	EXA14	EXA13	EXA12	EXA11	EXA10	EXA9
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7(EXA9~EXA16) : Expanding Data ROM start address A9~A16,,IOCB PAGE1 bit7 is the MSB(EXA17) for Expanding Data ROM start address.

PAGE3 Unused

R10~R3F (General Purpose Register)

R10~R3F (Banks 0 ~ 3) : All of them are general purpose registers

VII.3 Special Purpose Registers

A (Accumulator)

Internal data transfer, or instruction operand holding
It's not an addressable register.

CONT (Control Register)

7	6	5	4	3	2	1	0
INT/EDGE	INT	TS	DAEN	PAB	RSR2	RSR1	RSR0

Bit 0 ~ Bit 2 (PSR0 ~ PSR2) : TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC rate	WDT rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3(PAB) : Prescaler assignment bit
0/1 ➔ TCC/WDT

Bit 4 (DAEN) : Current DA enable control
0/1 (disable/enable

Bit 5 (TS) : TCC signal source
0/1 ➔ Instruction clock / 16.384K Hz
Instruction clock = MCU clock/2, Refer to RA Bit 4 ~ Bit 6 for PLL and Main clock selection. See Fig.15.

Bit 6 (INT) : INT enable flag
0 ➔ interrupt masked by DISI or hardware interrupt
1 ➔ interrupt enabled by ENI/RETI instructions

Bit 7(INT_EDGE) : interrupt edge type of P77
0 ➔ P77 's interruption source is a rising edge signal and falling edge signal.
1 ➔ P77 's interruption source is a falling edge signal.

CONT register is readable (CONTR) and writable (CONTW).There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time.

An 8 bit counter is available for TCC or WDT determined by the status of the bit 3 (PAB) of the CONT register. See the prescaler ratio in CONT register.Fig.25 depicts the circuit diagram of TCC/WDT. Both TCC and prescaler will be cleared by instructions which write to TCC each time. The prescaler will be cleared by the WDTC and SLEP instructions, when assigned to WDT mode.
The prescaler will not be cleared by SLEP instructions, when assigned to TCC mode.

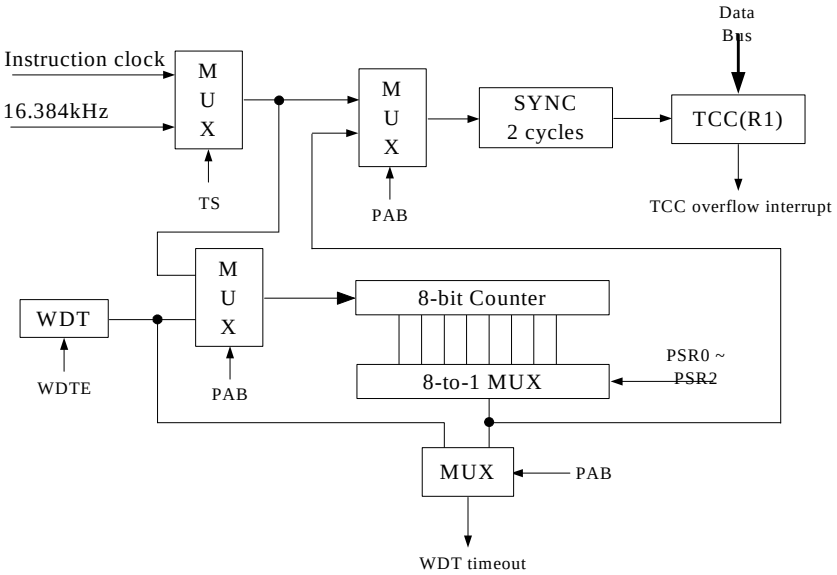


Fig.25 Block diagram of TCC and WDT

IOC5 Address Automatic Increase/Decrease control , Data RAM data buffer2

PAGE0 Address Automatic Increase/Decrease control register

7	6	5	4	3	2	1	0
DA2_ID	DA1_ID	DO_ID		DA2_IDEN	DA1_IDEN	DO_IDEN	
R/W-1	R/W-1	R/W-1	X	R/W-0	R/W-0	R/W-0	X

Bit 0 : Undefined register., not allowed to use

Bit 1 (DO_IDEN) : Enable DATA ROM address flag Increase/Decrease Enable Function.

If set this bit, DATA ROM address will increase or decrease after access (read or write) DATA ROM data.

When Expanding Data ROM is used, user can read or write external memory. By controlling RA PAGE0 bit3, address auto increase/decrease function can be change. Please refer to RA PAGE0 for detailed description.

1/0 ➔ Enable / Disable

Bit 2(DA1_IDEN) : Enable DATA RAM address flag1(RD and RE register) Increase/Decrease Enable Function.

If set this bit, DATA RAM address will increase or decrease after access (read or write) DATA RAM data (RC register).

1/0 ➔ Enable / Disable

Bit 3 (DA2_IDEN) : Enable DATA RAM address flag2(IOC6 and IOC7) Increase/Decrease Enable Function.

If set this bit, DATA RAM address will increase or decrease after access (read or write) DATA RAM data (IOC5 register).

1/0 ➔ Enable / Disable

Bit 4 : Undefined register., not allowed to use.

Bit 5 (DO_ID) : DATA ROM address automatic increase/decrease switch. Set to 1 means auto_increase, clear to 0 means auto_decrease.

1/0 ➔ auto increase / auto decrease

Bit 6 (DA1_ID) : DATA RAM address(RD and RE register) automatic increase/decrease switch. Set to 1 means auto_increase, clear to 0 means auto_decrease.

1/0 ➔ auto increase / auto decrease

Bit 7 (DA2_ID) : DATA RAM address(IOC6 and IOC7 register) automatic increase/decrease switch. Set to 1 means

auto_increase, clear to 0 means auto_decrease.

1/0 ➔ auto increase / auto decrease

PAGE1 Data RAM data buffer2

7	6	5	4	3	2	1	0
RAM2D7	RAM2D6	RAM2D5	RAM2D4	RAM2D3	RAM2D2	RAM2D1	RAM2D0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (RAM1D0 ~ RAM1D7) : Data RAM data buffer for RAM reading or writing.
Collocation RC~RE PAGE2 , user can move a large number continue data from an address to another in data RAM.

Example(move data from 0x0000 to 0x1000):

```
BC      R3,@5
MOV     A , @0xF0       ;Enable Rata RAM flag1 and flag2 auto_increase function
IOW     0x05
BS      R3 , @5         :Set correspond PAGE
BS      R3 , @6
BC      R3 , @7
MOV     A , @0x00       ;Assign DATA RAM index1 start address"0x0000"
MOV     0x0D , A
MOV     0x0E , A
IOW     0x06            ; Assign DATA RAM index2 start address"0x1000"
MOV     A , @0x10
IOW     0x07
MOV     A , 0x0C        ;Read data from index1(address:0x0000)
IOW     0x05            ;Write data to index2(address:0x1000)
MOV     A , 0x0C        ;Read data from index1(address:0x0001)
IOW     0x05            ;Write data to index2(address:0x1001)
    :
    :
```

IOC6 PORT 6 I/O Control , Data RAM address(L)
PAGE0 PORT 6 I/O Control

7	6	5	4	3	2	1	0
IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0~Bit 7 (IOC60 ~ IOC67) : PORT6(0~7) I/O direction control register
0 ➔ put the relative I/O pin as output
1 ➔ put the relative I/O pin into high impedance

PAGE1 Data RAM Address2(L)

7	6	5	4	3	2	1	0
RAM2A7	RAM2A6	RAM2A5	RAM2A4	RAM2A3	RAM2A2	RAM2A1	RAM2A0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0~Bit 7 (RAM2A0 ~ RAM2A7) : Data RAM address (address0 to address7) for RAM reading or writing

IOC7 PORT 7 I/O Control , Data RAM Address2(H)
PAGE0 PORT 7 I/O Control

7	6	5	4	3	2	1	0
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0~Bit 7 (IOC70 ~ IOC77) : PORT7(0~7) I/O direction control register
0 ➔ put the relative I/O pin as output
1 ➔ put the relative I/O pin into high impedance

PAGE1 Data RAM address2(H)

7	6	5	4	3	2	1	0
				RAM2A11	RAM2A10	RAM2A9	RAM2A8
X	X	X	X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0~Bit 3 (RAM2A8 ~ RAM2A11) : Data RAM address (address8 to address11) for RAM reading or writing
Bit 4~Bit 7 : Undefined register, not allowed to use.

IOC8 PORT 8 I/O Control
PAGE0 PORT 8 I/O Control

7	6	5	4	3	2	1	0
IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC80 ~ IOC87) : PORT8(0~7) I/O direction control register
0 ➔ put the relative I/O pin as output
1 ➔ put the relative I/O pin into high impedance

PAGE1 Undefined register
This register is not allowed to use.

IOC9 PORT9 I/O Control
PAGE0 PORT 9 I/O Control

7	6	5	4	3	2	1	0
IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC90 ~ IOC97) : PORT9(0~7) I/O direction control register
0 ➔ put the relative I/O pin as output
1 ➔ put the relative I/O pin into high impedance

PAGE1 Undefined register
This register is not allowed to use.

IOCA Undefined register
IOCA page0 and page1 are not allowed to use.

IOCB PORT B I/O Control ,External LCD driver interface (for EMC 65x132)
PAGE0 PORT B I/O Control

7	6	5	4	3	2	1	0
IOCB7	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0~Bit 7 (IOCB0~IOCB7) : PORTB(0~7) I/O direction control register
0 ➔ put the relative I/O pin as output
1 ➔ put the relative I/O pin into high impedance

PAGE1 External LCD Driver controller

7	6	5	4	3	2	1	0
EXA17	CWPWR			CSS	CSSON	DIS	EXLCD
R/W-0	R/W-0	X	X	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0(EXLCD) : External LCD driver enable/disable.

0/1 ➔ PORTB,PORTC normal IO/External LCD driver control (RE page2 LCD0,LCD1 must = 1)

If EXLCD equal to 0, PortB and PortC output are normal IO. When EXLCD equal to 1, PortB and PortC are switch to external LCD driver control pin. At this time, when user execute read or write PORTB instruction, PORTC timing characteristic plot is follow below.

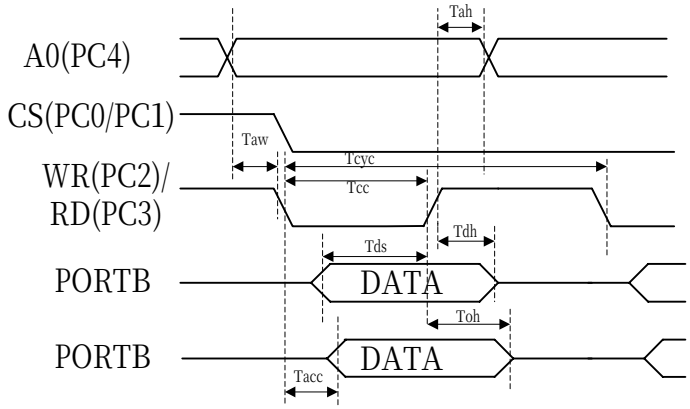


Fig.26 timing characteristic of external LCD driver data read/write

Symbol	Applicable pins	Rated value		Unit
		Min	Max	
Tah	A0	0		ns
Taw	A0	0		
Tcyc	A0	150		
Tcc	WR/RD	60		
Tds	D0 ~D7	20		
Tdh	D0 ~D7	10		
Tacc	D0 ~D7	-	60	
Toh	D0 ~D7	10	40	

Tah : Address hold time
Taw : Address setup time
Tcyc : System cycle time
Tcc : Pulse width
Tds : Data setup time
Tdh : Data hold time
Tacc : Read access time
Toh : Output disable time

User can operate in coordination on chip Data ROM address automatic increase function to write a large number of data from internal Data ROM to external LCD RAM.

Example(To collocate EM9L8580 LCD driver):

```
START:
    MOV    A , @0x0C;
```

```
        IOW   IOC5_PAGE0     ;Set Data ROM address automatic increase after read/write data
        MOV   A , @0x09
        IOW   IOCB_PAGE1    ;External LCD driver chip 1 INSTRUCTION mode select .
        MOV   A , @0xB0;
        MOV   RB_PAGE0 , A   ;Set external LCD driver start address PAGE 0
        MOV   A , @0x10
        MOV   RB_PAGE0 , A
        MOV   A , @0x00
        MOV   RB_PAGE0 , A   ; Set external LCD driver start address Column 0
        MOV   A , @0x00;
        MOV   R7_PAGE1 , A;
        MOV   R8_PAGE1 , A;
        MOV   R9_PAGE1 , A   ;Start address : 0x00000
        MOV   A , @0x0B
        IOW   IOCB_PAGE1     ;select data mode
CN1:
        MOV   A , R6_PAGE1   ;read data from Data ROM and address flag increase
        MOV   RB_RAGE0 , A   ;write data to external LCD driver.
        JMP     LOOP
```

Bit 1(DIS) : External LCD driver DATA/INSTRUCTION switch.

0/1 ➔ INSTRACTION/DATA

When EXLCD equal to 1 and DIS bit equal to 0 , MUC will transmit/receive INSTRUCTION. A0(PortC7) will output 0. If DIS bit set to 1, MUC will transmit/receive DATA. A0(PortC4) will output 1

Bit 2(CSSON) : External LCD driver select enable

CSSON	CSS0	CS1..CS2	
		LOW	HIGH
0	X	-	CS1,CS2
1	0	CS1	CS2
1	1	CS2	CS1

Example(for EMC 65x132 LCD driver):

```
MOV   A, @0x01
IOW    IOCB_PAGE1        ;Select external LCD driver & INSTRUCTURE mode
MOV   A,@0xB0
MOV   RB,A               ;Select external LCD driver COM0
MOV   A,@0x10
MOV   RB,A               ;Select external LCD driver SEG Upper 4-bit = 0
MOV   A,@0x00
MOV   RB,A               ;Select external LCD driver SEG Lower 4-bit = 0
MOV   A,@0x03
IOW   IOCB_PAGE1         ;switch to DATA mode
MOV   A,@0xFF
MOV   RB,A               ;write 0xFF to COM0 &SEG0
   :
```

User must assign external LCD address at first time. After writing or reading the display data, The SEGMENT address is automatically incremented. So that the MUC can continuously write or read data to the address.

Bit 3(CSS) : External LCD driver chip select bit.

0/1 ➔ chip1 / chip2

Bit 4..Bit 5 : Unused.

Bit 6(CWPWR) : CAS decoder power control.

0/1 → Power off / Power on.

Bit 7 (EXA17) : Expanding Data ROM start address MSB. This bit can be set only at connected pin "EXSAL " to VDD.

IOCC PORT C I/O Control , Port 6 Pull high register

PAGE0 PORT C I/O Control

7	6	5	4	3	2	1	0
IOCC7	IOCC6	IOCC5	IOCC4	IOCC3	IOCC2	IOCC1	IOCC0
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0~Bit 7 (IOCC0~IOCC7) : PORTC(0~7) I/O direction control register

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

PAGE1 Port 6 Pull High Register

7	6	5	4	3	2	1	0
PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7(PH60~PH67) : PORT6(0~7) pull high control register

0 → disable pull high function.

1 → enable pull high function

IOCD PORT D I/O Control , Port 7 Pull high register

PAGE0 PORT D I/O Control

7	6	5	4	3	2	1	0
IOCD7	IOCD6	IOCD5	IOCD4	IOCD3	IOCD2	IOCD1	IOCD0
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0~Bit 6 (IOCD0~IOCD6) : PORTD(0~6) I/O direction control register

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

PAGE1 Port 7 Pull High Register

7	6	5	4	3	2	1	0
PH77	PH76	PH75	PH74	PH73	PH72	PH71	PH70
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7(PH70~PH77) : PORT7(0~7) pull high control register

0 → disable pull high function.

1 → enable pull high function

IOCE Interrupt mask , Differential Energy Detect

PAGE0 Interrupt Mask Register1

7	6	5	4	3	2	1	0
INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7 : Interrupt enable bits.

0/1 → disable interrupt/enable interrupt

PAGE1 Differential Energy Detect

7	6	5	4	3	2	1	0
VRSEL	DEDD	EDGE	WUEDD	CW_SMB	DEDCLK	DEDPWR	DEDTHD

R/W-0	R	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0(DEDTHD) : The minimum detection threshold of Differential Energy Detector (DED)
0/1 ➔ -45dBm/-30dBm

Bit 1 (DEDPWR) : Power control of Differential Energy Detector (DED)
0/1 ➔ Power off / Power on

Bit 2 (DEDCLK) : Operating clock for Differential Energy Detector (DED)
0/1 ➔ 32.768kHz/3.5826MHz
This bit is used to select operating clock for Differential Energy Detector (DED). When this bit is set to "1", the PLL is also enabled regardless of RA bit 6 (ENPLL) . At this time, the Energy detector works at high frequency mode. When this bit is set to "0", the Energy Detector works at low frequency mode. The difference between high frequency and low frequency is as follows.

DEDPWR	DEDCLK	ENPLL	Energy detector clock	Main CLK
0	X	X	X	Decision by ENPLL
1	0	0	32.768 KHz	Disable
1	0	1	32.768 KHz	Enable
1	1	0	3.5826 MHz	Enable
1	1	1	3.5826 MHz	Enable

PS. "X" means don't care

Bit 3(CW_SMB) : Call Waiting / short message receiver switch
0 ➔ Short message mode select. ± 5.5% CAS tone accepted frequency range deviation.(Protocol : ± 5%)
1 ➔ Call Waiting mode select. ± 2.0% CAS tone accepted frequency range deviation.

Bit 4 (WUEDD) : Wake-up control of Energy Detector (DED) output data
1/0 ➔ enable/disable

Bit 5 (EDGE) : Wake-up and interrupt trigging edge control of Energy Detector (DED) output
1/0 ➔ Rising edge and Falling edge trig /Falling edge trig.

Bit 6(DEDD) : Output data of Differential Energy Detector (DED) If input signal from TIP/EGIN1 and RING/EGIN2 pin to Differential Energy Detector is over the threshold level setting at IOCE PAGE 2 bit 0 (DEDTHD), the DED will extract the zero-crossing pulse waveform corresponding to input signal.

Bit 7 (VRSEL) : Reference voltage VR selection bit for Comparator
0 ➔ VR = VDD
1 ➔ VR = 2.0V
When this bit is set to "0", V2_0 ref. circuit will be powered off. 2.0V ref. circuit is only powered on when this bit and RA page2 bit 7(CMPEN) are all set to "1".

IOCF Interrupt Mask Register2

7	6	5	4	3	2	1	0
RBF/STD	FSK/CW	-	UART	DED	CNT2	CNT1	TCC
R/W-0	R/W-0	X	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7 : Interrupt enable bits.
0/1 ➔ disable interrupt/enable interrupt

VII.4 I/O PORT

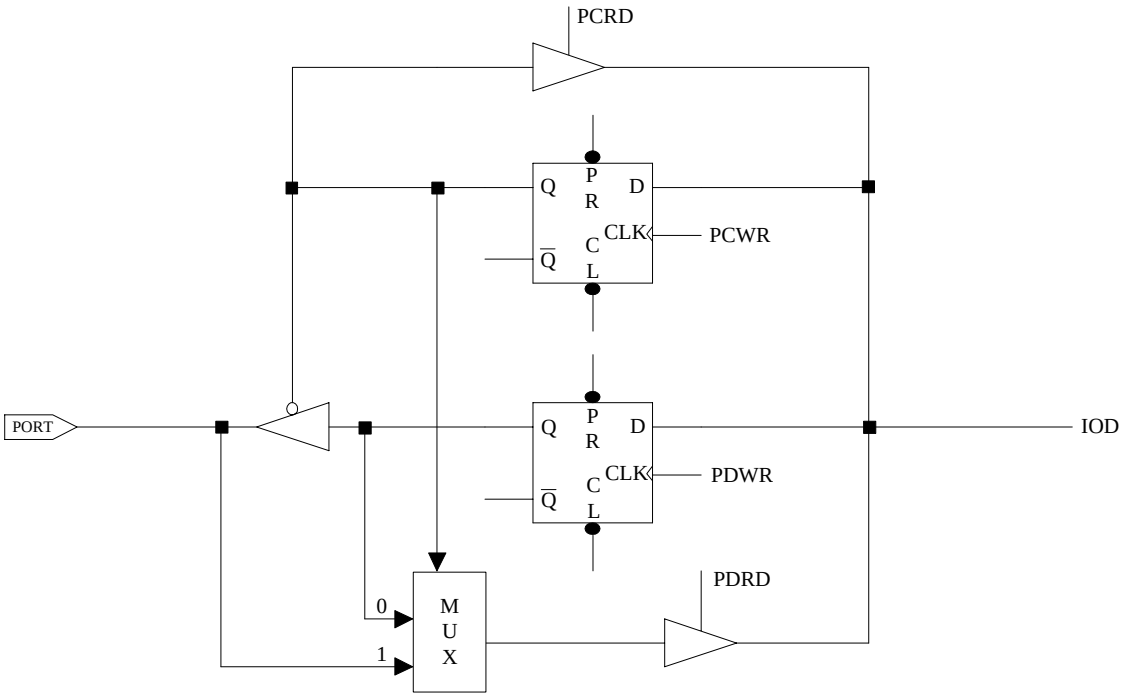


Fig.27 The circuit of I/O port and I/O control register

The I/O registers are bi-directional tri-state I/O ports. The I/O ports can be defined as "input" or "output" pins by the I/O control registers under program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig.27.

MCU will consumption large current when IO is set to input and at floating status. Be careful to set unused IO at output or connect them to VDD or GND when they are setting to input status.

VII.5 RESET

The RESET can be caused by
(1) Power on voltage detector reset (POVD) and power on reset
(2) WDT timeout. (if enabled and in GREEN or NORMAL mode)
(3) /RESET pin pull low
<Note> At case (1), POVD is controlled by CODE OPTION. If you enable POVD, CPU will reset at 2V under. And CPU will consume more current about 3uA . And the power on reset is a circuit always enable. It will reset CPU at about 1.4V and consume about 0.5uA.
Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- When power on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler counter are cleared.
- The Watchdog timer is disabled.
- The CONT register is set to all "1"
- The other register (bit7..bit0)

address	R register page0	R register page1	R register page2	R register page3	IOC register page0	IOC register page1
1	xxxxxxxx	00000000	00000000	xxxxxxxx		
4	00xxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx		
5	x0000000	00000000	00000000	xxxx0000	11110000	xxxxxxxx
6	xxxxxxxx	xxxxxxxx	00000000	00000000	11111111	xxxxxxxx
7	xxxxxxxx	xxxxxxxx	00000000	00000000	11111111	xxxxxxxx
8	xxxxxxxx	xxxxxxxx	xxxx0000	Xxxxxxxx	11111111	00000000
9	xxxxxxxx	xxxxxxxx	00000xxx	xxxxx000	11111111	00000000
A	00000xx0	xxxxxxxx	00000000	00000000	xxxxxxxx	xxxxxxxx
B	xxxxxxxx	xxxxxxxx	11111111	00000000	11111111	00xx0000
C	xxxxxxxx	xxxxxxxx	11111111	xxxxxxxx	11111111	00000000
D	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	11111111	00000000
E	00000000	xxxxxxxx	xx00xxxx	xxxxxxxx	00000000	0x000000
F	00xx0000	00000000	00000000	xxxxxxxx	00000000	--

VII.6 wake-up

The controller provided power saving mode:

(1) SLEEP mode, RA (7)=0 + "SLEP" instruction .

The controller will turn off all the CPU and crystal. Other circuit with power control like key tone control or PLL control (which has enable register), user has to turn it off by software.

Wake-up from SLEEP mode:

(1) WDT time out

(2) External interrupt

(3) /RESET pull low.

All these cases will reset controller , and run the program at address zero. The status just like the power on reset.

VII.7 Interrupt

RE and RF is the interrupt status register which records the interrupt request in flag bits. IOCE and IOCF is the interrupt mask register. TCC timer, Counter1 and Counter2 are internal interrupt source. P70 ~ P77(INT0 ~ INT7) are external interrupt input which interrupt sources are come from the external. If the interrupts are happened by these interrupt sources, then RE or RF register will generate '1' flag to corresponding register if you enable IOCE or IOCF register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) generated, will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine the source of the interrupt can be determined by polling the flag bits in the RE and RF register. The interrupt flag bit must be cleared in software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

VII.8 Instruction Set

Instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operates on I/O register.

The symbol "R" represents a register designator which specifies which one of the 64 registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4

determine the selected register bank. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED	Instruction cycle
0 0000 0000 0000	0000	NOP	No Operation	None	1
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C	1
0 0000 0000 0010	0002	CONTW	A → CONT	None	1
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P	1
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P	1
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None	1
0 0000 0001 0000	0010	ENI	Enable Interrupt	None	1
0 0000 0001 0001	0011	DISI	Disable Interrupt	None	1
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None	2
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None	2
0 0000 0001 0100	0014	CONTR	CONT → A	None	1
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None	1
0 0000 0010 0000	0020	TBL	R2+A → R2 bits 9,10 do not clear	Z,C,DC	2
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None	1
0 0000 1000 0000	0080	CLRA	0 → A	Z	1
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z	1
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC	1
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC	1
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z	1
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z	1
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z	1
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z	1
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z	1
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z	1
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z	1
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z	1
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC	1
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC	1
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z	1
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z	1
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z	1
0 0100 11rr rrrr	04rr	COM R	/R → R	Z	1
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z	1
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z	1
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None	2 if skip
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None	2 if skip
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C	1
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C	1
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C	1
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C	1

0	0111	00rr	rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None	1
0	0111	01rr	rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None	1
0	0111	10rr	rrrr	07rr	JZA R	R+1 → A, skip if zero	None	2 if skip
0	0111	11rr	rrrr	07rr	JZ R	R+1 → R, skip if zero	None	2 if skip
0	100b	bbrr	rrrr	0xxx	BC R,b	0 → R(b)	None	1
0	101b	bbrr	rrrr	0xxx	BS R,b	1 → R(b)	None	1
0	110b	bbrr	rrrr	0xxx	JBC R,b	if R(b)=0, skip	None	2 if skip
0	111b	bbrr	rrrr	0xxx	JBS R,b	if R(b)=1, skip	None	2 if skip
1	00kk	kkkk	kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None	2
1	01kk	kkkk	kkkk	1kkk	JMP k	(Page, k) → PC	None	2
1	1000	kkkk	kkkk	18kk	MOV A,k	k → A	None	1
1	1001	kkkk	kkkk	19kk	OR A,k	A ∨ k → A	Z	1
1	1010	kkkk	kkkk	1Akk	AND A,k	A & k → A	Z	1
1	1011	kkkk	kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z	1
1	1100	kkkk	kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None	2
1	1101	kkkk	kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC	1
1	1110	0000	0001	1E01	INT	PC+1 → [SP] 001H → PC	None	1
1	1110	1kkk	kkkk	1E8k	PAGE k	K->R5(4:0)	None	1
1	1111	kkkk	kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC	1

**** One instruction cycle = 2 main clk.***

VII.9 CODE Option Register

The controller has one CODE option register which is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

CODE Option Register1 (Program ROM)

7	6	5	4	3	2	1	0
-						/DED	/POVD

Bit 0 (/POVD) : Power on voltage detector, 0/1 ➔ enable/disable

/POVD	2.2V /POVD reset voltage	2.2V Power on reset voltage	Sleep mode current (VDD=5V)
1	No	Yes (2.2V)	1uA
0	Yes (2.2V)	No	15uA

Bit 1(/DED) : Differential Energy Detect function enable bit
0/1 ➔ enable / disable DED function

VII.10 CALL WAITING Function Description

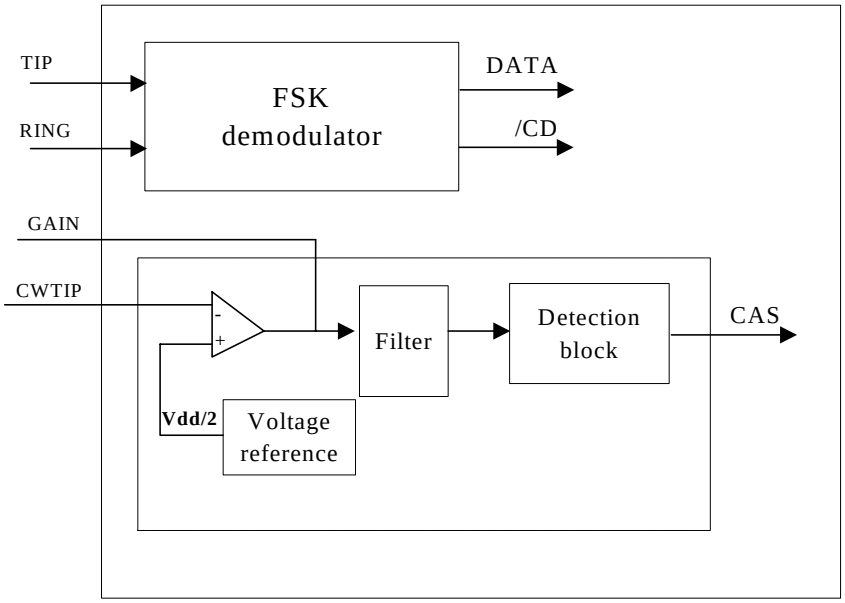


Fig.28 Call Waiting Block Diagram

Call Waiting service works by alerting a customer engaged in a telephone call to a new incoming call. This way the customer can still receive important calls while engaged in a current call. The CALL WAITING DECODER can detect CAS(Call-Waiting Alerting Signal 2130Hz plus 2750Hz) and generate a valid signal on the data pins.

The call waiting decoder is designed to support the Caller Number Deliver feature, which is offered by regional Bell Operating Companies.

In a typical application, after enabling CW circuit (by R5 page3 bit3 & bit4) this IC receives Tip and Ring signals from twisted pairs. The signals as inputs of pre-amplifier, and the amplifier sends input signal to a band pass filter. Once the signal is filtered, the Detection block decodes the information and sends it to RE page2 bit7 . The output data made available at RE CAS bit.

The data is CAS signals. The CAS is normal high. When this IC detects 2130Hz and 2750Hz frequency, then CAS pin goes to low.

VII.11 Differential Energy Detector (DED)

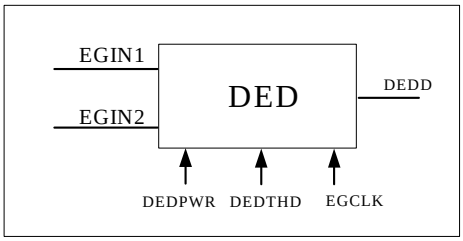


Fig.29 DED Block diagram

The Differential Energy Detector is differential input level and zero crossing detector named as DED. It can detect any incoming AC signal above its threshold level and output corresponding zero-crossing frequency pulse. For this energy detector, the user can set it's minimum detection threshold level at –35dBm or –45dBm by DEDTHD bit. All the minimum detection value can be achieved under input capacitor more than 4700pF and input resistor around 100k ohms. The energy detector has power control by IOCE PAGE1 bit 1 (DEDPWR).

Register bits of Energy Detector :

Register bits	Descriptions
RF PAGE0 bit 3 (DED)	DED : Interrupt flag of DED output data
IOCE PAGE1 bit 7 (DEDD)	DEDD : Output data of DED
IOCE PAGE1 Bit 5 (EDGE)	EDGE : edge control of DED output data 1/0 => Falling edge trig. / Rising edge and Falling edge trig.
IOCE PAGE1 Bit 4 (WUEDD)	WUEDD : Wake-up control of DED output data 1/0 => enable/disable
IOCE PAGE1 Bit 6 (DED)	DED : Interrupt mask of DED output data 1/0 ➔ enable/disable interrupt of DED output data
IOCE PAGE1 Bit 0 (DEDTHD)	DEDTHD : Minimum detection threshold of DED 0/1 ➔ -45dBm/-30dBm
IOCE PAGE1 Bit 1 (DEDPWR)	DEDPWR : Power control of DED 0/1 ➔ power off/power on
IOCE PAGE1 Bit 2 (DEDCLK)	DEDCLK : operating clock of DED 0 : low frequency clock 1 : high frequency clock

VIII. Absolute Operation Maximum Ratings

RATING	SYMBOL	Min	Typ	Max	Unit
DC SUPPLY VOLTAGE	VDD	-0.3		6	V
INPUT VOLTAGE	Vin	VDD-0.5	VDD	VDD+0.5	V
OPERATING TEMPERATURE RANGE	Ta	0	25	70	℃

IX. DC Electrical Characteristic

(Operation current consumption for Analog circuit)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operation current for FSK	I_FSK	VDD=3V, CID power on		1.5	2.5	mA
Operation current for CW	I_CW	VDD=5V, CID power on		1.5	2.5	mA
Operation current for DTMF Receiver	I_DR	VDD=3V, DTMFr power on		1.5	2.5	mA
Operation current for TONE generator	I_DTMF	VDD=3V, DTMF power on		0.5	0.8	mA
Operation current for Current DA	I_DA	VDD=3V, CDA power on		1.5	4	mA
Operation current for Comparator	I_CMP	VDD=5V, PT power on		0.1		mA

(Ta=0°C ~ 70°C, VDD=3V±5%, VSS=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Leakage Current for input pins	IIL1	VIN = VDD, VSS			±1	μA
Input Leakage Current for bi-directional pins	IIL2	VIN = VDD, VSS			±1	μA
Input High Voltage	VIH		2.0			V
Input Low Voltage	VIL				0.8	V
Input high threshold Voltage	VIHT	/RESET, TCC, RDET1	2.0			V
Input low threshold Voltage	VILT	/RESET, TCC,RDET1			0.8	V
Clock Input High Voltage	VIHX	OSCI	1.8			V
Clock Input Low Voltage	VILX	OSCI			1.2	V
Output High Voltage (port 8,9,B,C,D)	VOH1	IOH = -6mA	2.0	2.4		V
Output High Voltage (port6,7)		IOH = -10.0mA	2.0	2.4		V
Output Low Voltage (port 8,9,B,C,D)	VOL1	IOL = 6mA			0.4	V
Output Low Voltage (port6,7)		IOL = 10.0mA			0.4	V
Pull-high current	IPH	Pull-high active input pin at VSS		-10	-15	μA
Power down current (SLEEP mode)	ISB1	All input and I/O pin at VDD, output pin floating, WDT disabled		1	4	μA
Low clock current (GREEN mode)	ISB2	CLK=32.768KHz,All analog circuit disable , All input and I/O pin at VDD, output pin floating, WDT disabled,		30	40	μA
Operating supply current (NORMAL mode)	ICC	/RESET=High, PLL enable CLK=3.579MHz, output pin floating, all analog circuit disable		2	3	mA
Tone generator reference voltage	Vref2		0.5		0.7	VDD

Differential Energy Detector (DED) (Ta=25°C, VDD=3.0V±5%, VSS=0V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EGIN1	Operating current for SED	SEDCLK bit = 0		20	25	μA
EGIN2	Operating current for SED	SEDCLK bit = 0		20	25	μA

X. AC Electrical Characteristic

CPU instruction timing (Ta=25°C, VDD=3V, VSS=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input CLK duty cycle	Dclk		45	50	55	%
Instruction cycle time	Tins	32.768kHz 3.579MHz		60 550		us ns
Device delay hold time	Tdrh			16		ms
TCC input period	Ttcc	Note 1	(Tins+20)/N			ns
Watchdog timer period	Twdt	Ta = 25°C		16		ms

Note 1: N= selected prescaler ratio.

FSK AC Characteristic (Vdd=3V,Ta=+25°C)

CHARACTERISTIC	Min	Typ	Max	Unit
FSK sensitivity				
Low Level Sensitivity Tip & Ring @SNR 20dB	-40	-48		dBm
High Level Sensitivity Tip & Ring @SNR 20dB		0		dBm
Signal Reject		-51		dBm
FSK twist				
Positive Twist (High Level)	+10			dB
Positive Twist (Low Level)	+10			dB
Negative Twist (High Level)	-6			dB
Negative Twist (Low Level)	-6			dB

CW AC Characteristic (Vdd=3V,Ta=+25°C)

CHARACTERISTIC	Min	Typ	Max	Unit
CW sensitivity				
Sensitivity @SNR 20dB		-38		dBm
USA & Europe mode				
Low Tone Frequency 2130Hz		±1.2		%
High Tone Frequency 2750Hz		±1.2		%
Chinese Call waiting mode				
Low Tone Frequency 2130Hz		±2.0		%
High Tone Frequency 2750Hz		±2.0		%
Chinese SMS mode				
Low Tone Frequency 2130Hz		±5.5		%
High Tone Frequency 2750Hz		±5.5		%
CW twist				
Twist	±7			dB

DTMF (DTMF receiver) AC Characteristic (Vdd=3V,Ta=+25°C)

CHARACTERISTIC	Min	Typ	Max	Unit
DTMF receiver				
Low Level Signal Sensitivity		-36		dBm
High Level Signal Sensitivity		0		dBm
Low Tone Frequency		±2		%
High Tone Frequency		±2		%
DTMF receiver noise endurance				
Signal to noise ratio	15			dB

TONE generators for AC Characteristic (Vdd=3V,Ta=+25°C)

CHARACTERISTIC	Min	Typ	Max	Unit
Tone1/Tone2 signal strength (root mean square voltage)				
Tone1 signal strength V1rms (ps1)	130	155	180	mV
Tone2 signal strength V2rms (ps1)	1.259V1rms			mV
Tone twist				
(Tone1 – Tone2) twist		-2		dB
Tone frequency deviation				
Frequency deviation			±1	%

(ps1) : V1rms and V2rms has 2dB difference. It means 20log(V2rms/V1rms) = 20log1.259 = 2 (dB)

DED AC Characteristic (Vdd=+3.0V,Ta=+25℃)

CHARACTERISTIC	MIN	TYP	MAX	UNIT
Input sensitivity TIP and RING for DED, DEDTHD bit=0		-45	--	dBm
Input sensitivity TIP and RING for DED, DEDTHD bit=1		-35	--	dBm

Timing characteristic (Vdd=3V,Ta=+25°C)

Description		Symbol	Min	Typ	Max	Unit
Oscillator timing characteristic						
OSC start up	32.768kHz	Tosc			1500	ms
	3.579MHz PLL				10	us
Timing characteristic of reset						
The minimum width of reset low pulse		Trst	3			uS
The delay between reset and program start		Tdrs		18		mS
FSK timing characteristic						
Carrier detect low		Tcdl	--	10	14	ms
Carrier detect low to data valid		Tcdv	--	10	20	ns
Power up to FSK(setup time)		Tsup	--	15	20	ms
End of FSK to Carrier Detect high		Tcdh		--	4	ms
CW timing characteristic						
CAS input signal length (2130 ,2750 Hz @ -20dBm)		Tcasi		80		ms
Call waiting data detect delay time		Tcwd		42		ms
Call waiting data release time		Tcwr		26		ms
DTMF receiver timing characteristic						
Tone Present Detection Time		Tdp		(ps1)		
The guard-times for tone-present (C=0.1uF, R=300K)		Tgtp		30		ms

The guard-times for tone-absent (C=0.1uF, R=300K)	Tgta		30		mS
Propagation Delay (St to Q)	Tpq		8		us
Tone Absent Detection Time	Tda		(ps2)		ms
SPI timing characteristic (CPU clock 3.58MHz and Fsco = 3.58Mhz /2)					
/SS set-up time	Tcss	560			ns
/SS hold time	Tcsh	250			
SCLK high time	Thi	250			ns
SCLK low time	Tlo	250			ns
SCLK rising time	Tr		15	30	ns
SCLK falling time	Tf		15	30	ns
SDI set-up time to the reading edge of SCLK	Tisu	25			ns
SDI hold time to the reading edge of SCLK	Tihd	25			ns
SDO disable time	Tdis			560	ns

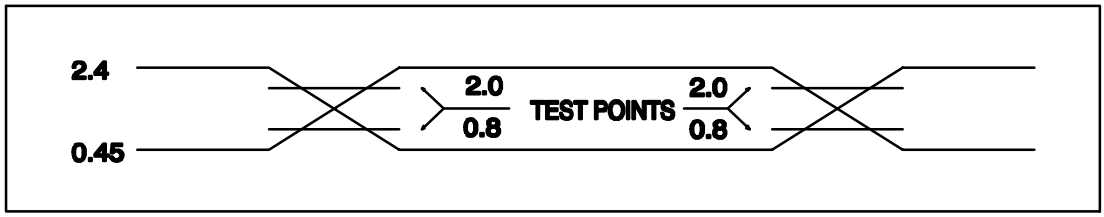
(ps1) : Controlled by software
(ps2) : Controlled by RC circuit.

Data ROM access timing characteristic

Symbol	Description	Condition	Min	Typ	Max	Unit
Tdiea	Delay from Phase 3 end to INSEND active	Cl=100pF			30	ns
Tdiei	Delay from Phase 4 end to INSEND inactive	Cl=100pF			30	ns
Tiew	INSEND pulse width		30			ns
Tdca	Delay from Phase 4 end to CA Bus valid	C1=100pF			30	ns
Tacc	ROM data access time		100			ns
Tcds	ROM data setup time		20			ns
Tcdh	ROM data hold time		20			ns
Tdca-1	Delay time of CA-1	C1=100pF			30	ns

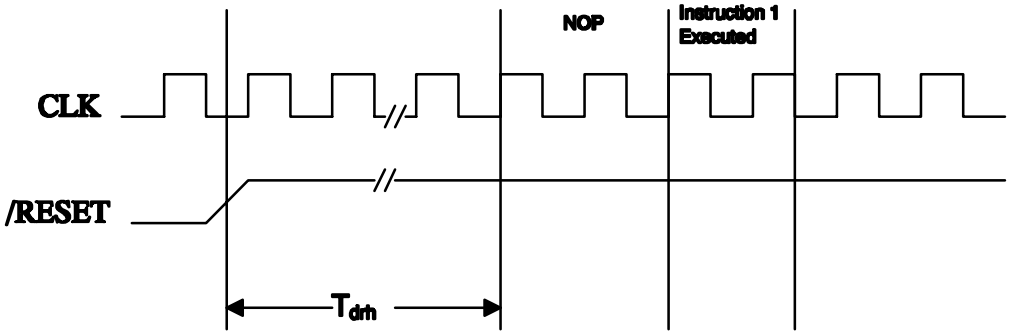
XI. Timing Diagrams

AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing



TCC Input Timing

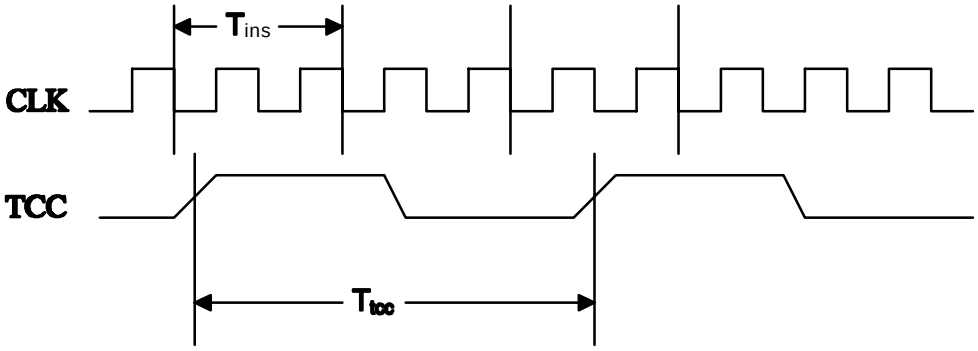


Fig.30 AC timing

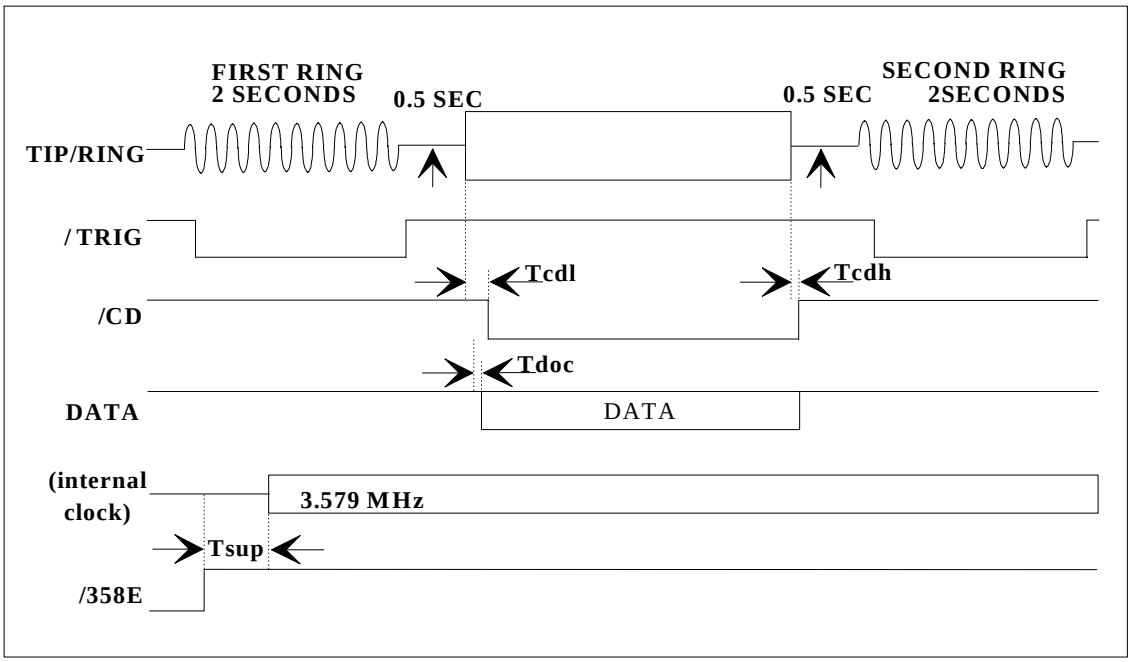


Fig.31 FSK timing diagram

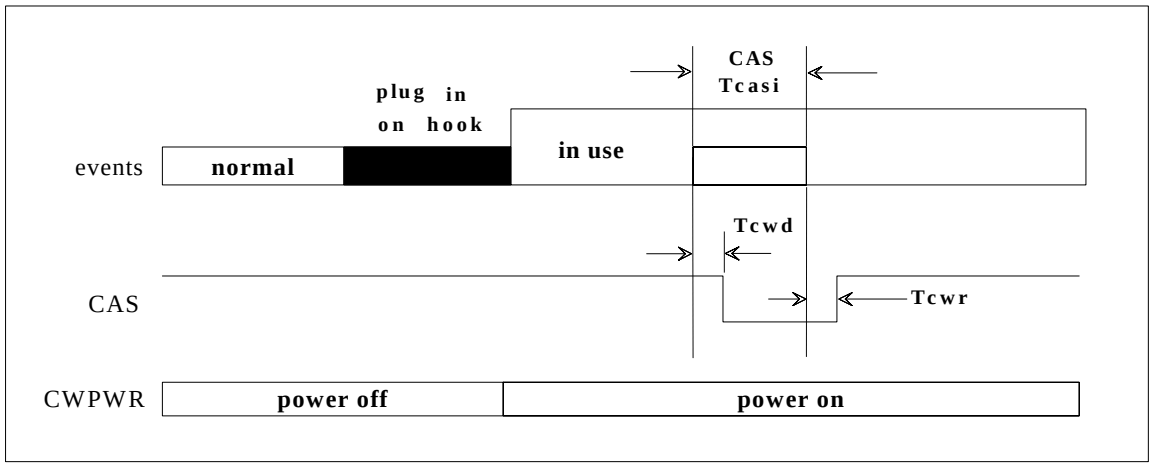


Fig.32 Call waiting timing diagram

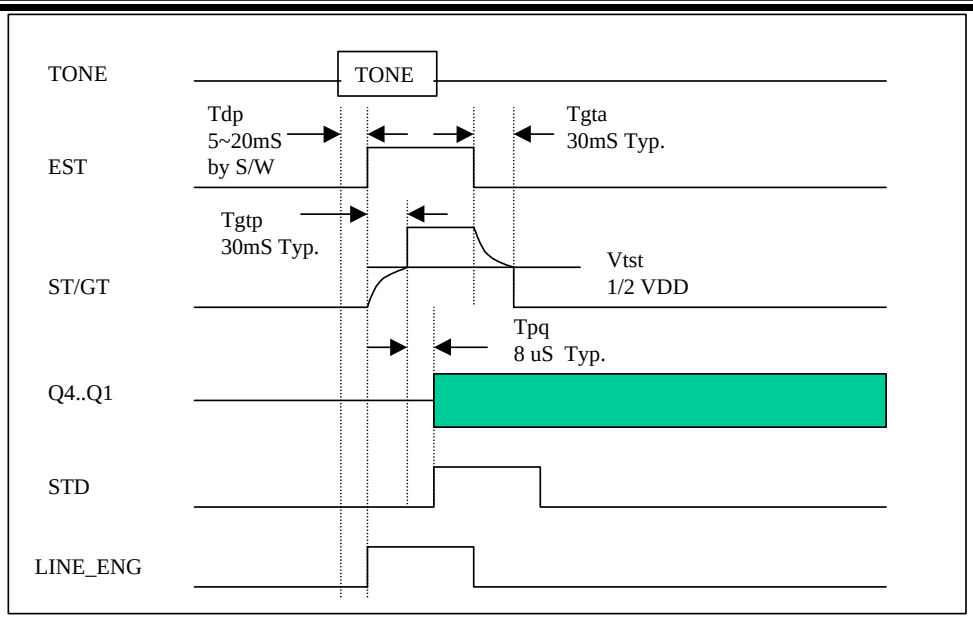


Fig.33 DTMF receiver timing diagram

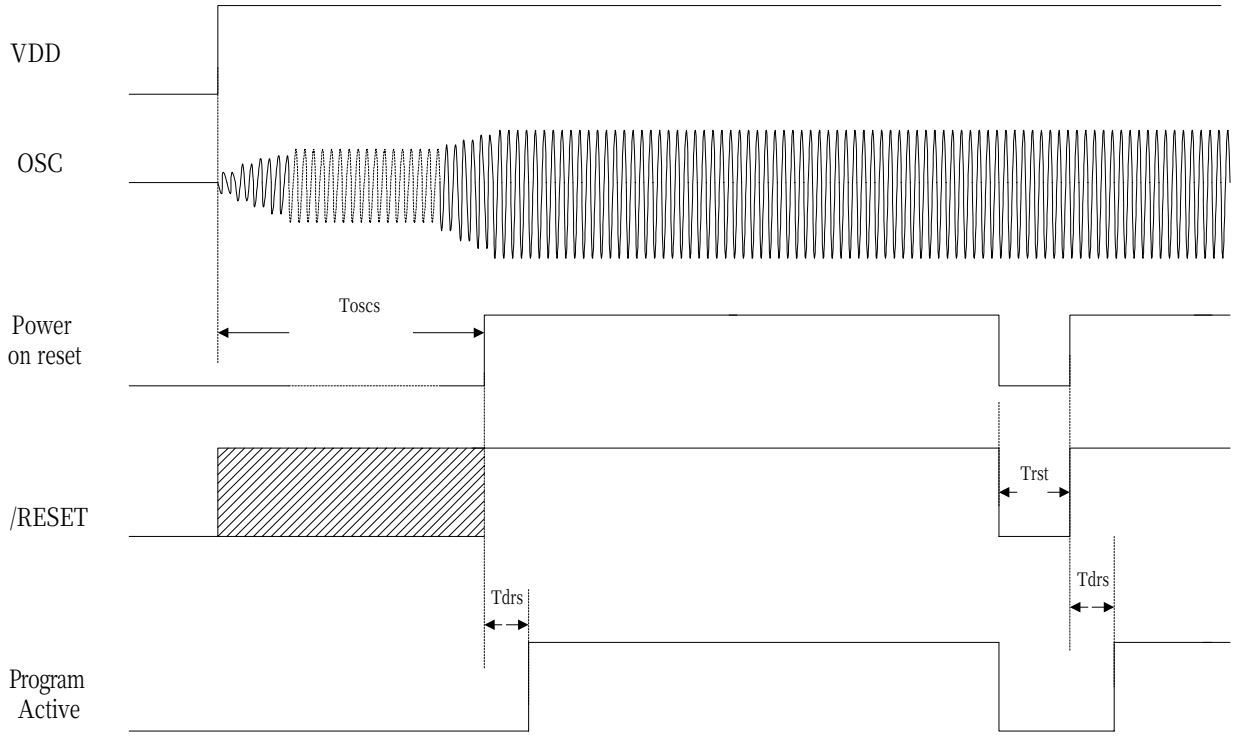


Fig.34: The relative between OSC stable and reset time.

XII Application Circuit

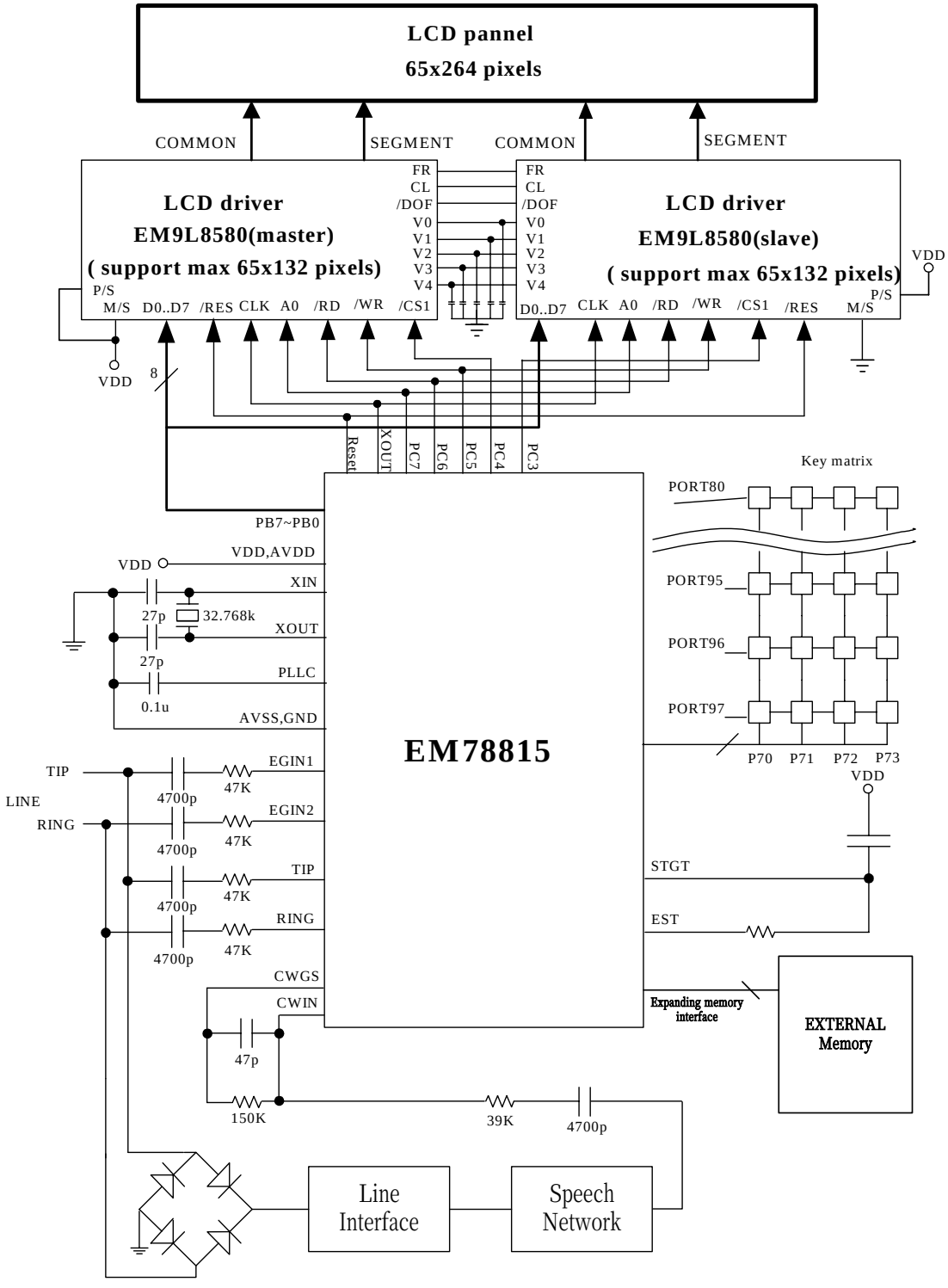


Fig 35: External multi-chip LCD driver application circuit