ANALOG DEVICES

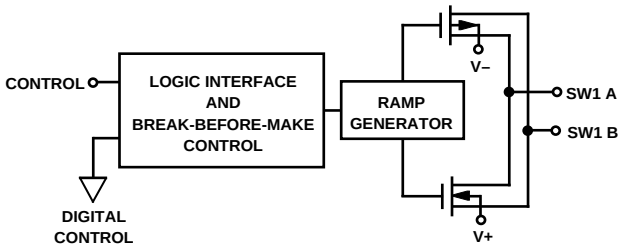
Quad Audio Switch

SSM2404

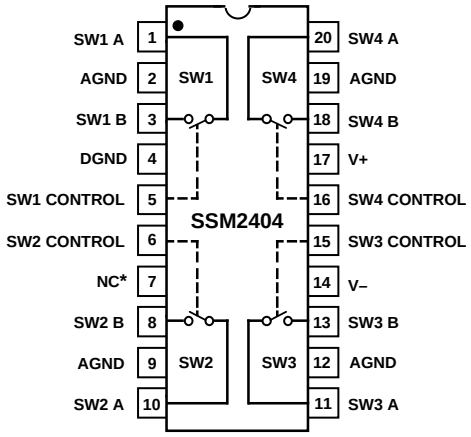
FEATURES

"Clickless" Bilateral Audio Switching
Four SPST Switches in a 20-Pin Package
Ultralow THD+N: 0.0008% @ 1 kHz (2 V rms, R_L = 100 kΩ)
Low Charge Injection: 35 pC typ
High OFF Isolation: –100 dB typ (R_L = 10 kΩ @ 1 kHz)
Low Crosstalk: –94 dB typ (R_L = 10 kΩ @ 1 kHz)
Low ON Resistance: 28 Ω typ
Low Supply Current: 900 μA typ
Single or Dual Supply Operation: +11 V to +24 V or ±5.5 V to ±12 V
Guaranteed Break-Before-Make
TTL and CMOS Compatible Logic Inputs
Low Cost-Per-Switch

BLOCK DIAGRAM OF ONE SWITCH CHANNEL



PIN CONNECTIONS
Epoxy Mini-DIP (P Suffix) and SOIC (S Suffix)



NC = NO CONNECT

*CONNECT TO ANALOG GROUND FOR BEST NOISE ISOLATION

GENERAL DESCRIPTION

The SSM2404 integrates four SPST analog switches in a single 20-pin package. Developed specifically for high performance audio applications, distortion and noise are negligible over the full operating range of 20 Hz to 20 kHz. With very low charge injection of 35 pC, "clickless" audio switching is possible, even under the most demanding conditions.

Switch control is realized by conventional TTL or CMOS logic. Guaranteed "break-before-make" operation assures that all switches in a large system will open before any switch reaches the ON state.

Single or dual supply operation is possible. Additional features include –100 dB OFF isolation, –94 dB crosstalk and 28 Ω ON resistance. Optional current-mode switching permits an extended signal-handling range. Although optimized for large load impedances, the SSM2404 maintains good audio performance even under low load impedance conditions.

REV. B

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SSM2404–SPECIFICATIONS

(V_S = ±12 V, T_A = +25°C, unless otherwise noted. Typical specifications apply at T_A = +25°C.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD+N	@ 1 kHz, with 80 kHz Filter, R_L = 100 kΩ, V_{IN} = 2 V rms		0.0008		%
Spectral Noise Density	e_n	20 Hz to 20 kHz		0.8		nV/√Hz
Wideband Noise Density	e_n p-p	20 Hz to 20 kHz		0.6		µV p-p
ANALOG SIGNAL SECTION						
Analog Voltage Range	V_A	V_{INH} = 2.4 V, I_A = ±2 mA		±12		V
Analog Current Range	I_A	V_{INH} = 2.4 V, V_A = 0 V		±10		mA
ON Resistance	R_{ON}	I_A = ±10 mA, V_A = ±10 V dc		28	45	Ω
R_{ON} Matching	R_{ON} Match	I_A = ±10 mA, V_A = 0 V		1		%
ON Leakage Current	$I_{S(ON)}$	V_A = ±10 V	–20	0.1	+20	nA
OFF Leakage Current	$I_{S(OFF)}$	V_A = ±10 V	–20	0.1	+20	nA
Charge Injection	Q			35		pC
ON-State Input Capacitance	C_{ON}	V_A = 5 V rms		31		pF
OFF-State Input Capacitance	C_{OFF}	V_A = 5 V rms		17		pF
OFF Isolation	$I_{SO(OFF)}$	V_A = 50 mV rms, f = 1 kHz, R_L = 10 kΩ		–100		dB
Channel-to-Channel Crosstalk	C_T	V_A = 50 mV rms, f = 1 kHz, R_L = 10 kΩ		–94		dB
CONTROL SECTION						
Digital Input High	V_{INH}	DGND = 0 V	2.4		V_S	V
Digital Input Low	V_{INL}	DGND = 0 V	0		0.8	V
Turn-On Time[1]	t_{ON}	See Test Circuit		8	50	ms
Turn-Off Time[2]	t_{OFF}	See Test Circuit		5	30	ms
Break-Before-Make Time Delay	t_{ON}-t_{OFF}			3	20	ms
Logic Input Current						
Logic HI		V_{INH} = 2.4 V	–1000	1.3	+1000	nA
Logic LO		V_{INL} = 0.8 V	–1000	1.0	+1000	nA
POWER SUPPLY						
Supply Voltage Range	V_S	Single Supply	+11		+24	V
		Dual Supply	±5.5		±12	V
Positive Supply Current	I_{SY+}	All Channels On		0.9	5	mA
Negative Supply Current	$I_{SY–}$	All Channels On	–1.5	–0.6		mA
Ground Current		All Channels On	–2.0	–0.3		mA

NOTES

[1]Turn-on time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the final value.

[2]Turn-off time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the initial value.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- Single Supply . . . . . +27 V
- Dual Supply . . . . . ±13.5 V

Analog Input Voltage (V_A) . . . . . V_S

Logic Input Voltage ($V_{INL/INH}$) . . . . . V_S

Maximum Current Through Any Switch . . . . . 20 mA

Operating Temperature Range . . . . . –40°C to +85°C

Storage Temperature Range . . . . . –65°C to +150°C

Junction Temperature (T_J) . . . . . +150°C

Lead Temperature (Soldering, 60 sec) . . . . . +300°C

Thermal Resistance[1]
- 20-Pin Plastic DIP (P): θ_{JA} = 74, θ_{JC} = 32 . . . . . °C/W
- 20-Pin SOIC (S): θ_{JA} = 90, θ_{JC} = 27 . . . . . °C/W

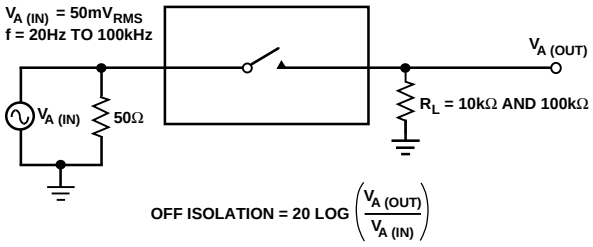
NOTE

[1]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for P-DIP package.

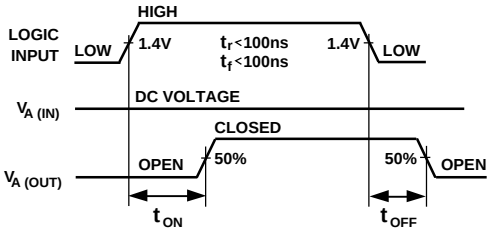
ORDERING GUIDE

Model	Operating Temperature Range	Package	Package Option*
SSM2404P	–40°C to +85°C	20-Pin Plastic DIP	N-20
SSM2404S	–40°C to +85°C	20-Pin SOIC	R-20

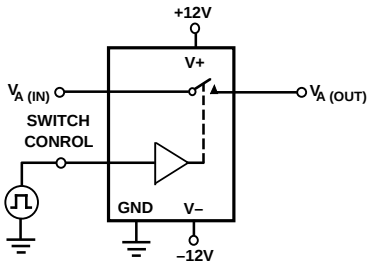
*N = Plastic DIP, R = SOIC.



OFF Isolation Test Circuit



t_{ON}/t_{OFF} Timing Diagram



Test Circuit for t_{ON}/t_{OFF} Timing Specification, t_{ON}/t_{OFF} Switching Response, and ON/OFF Transition Photos

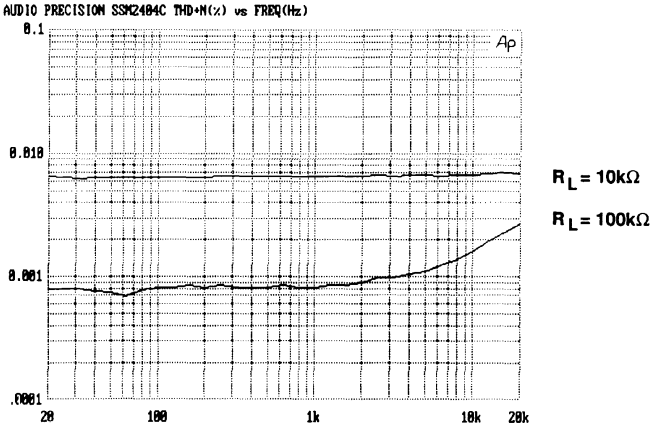


Figure 1. THD+N vs. Frequency (V_S = ±12 V, V_A = 2 V rms, with 80 kHz Filter)

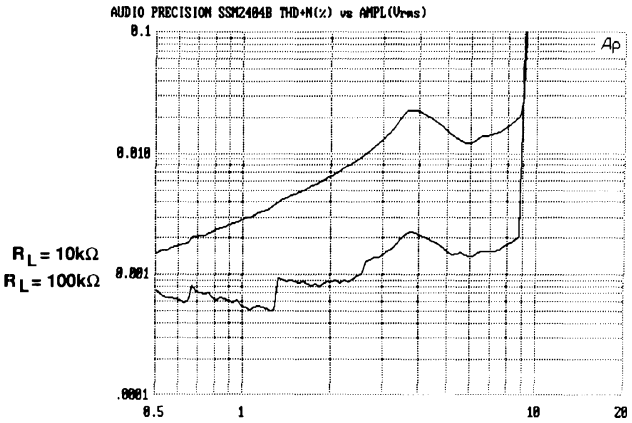


Figure 2. Headroom (V_S = ±12 V, f = 1 kHz, with 80 kHz Filter)

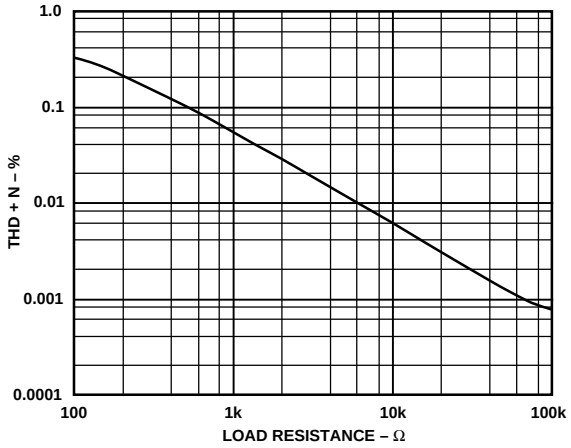


Figure 3. THD+N vs. Load (V_S = ±12 V, V_A = 2 V rms, f = 1 kHz, with 80 kHz Filter)

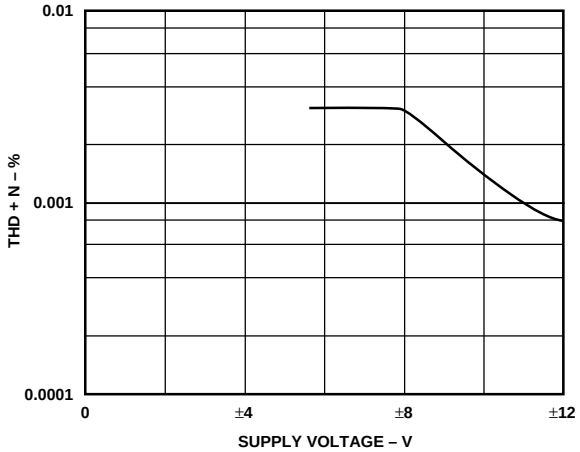


Figure 4. THD+N vs. Supply Voltage (V_A = 2 V rms, f = 1 kHz, R_L = 100 kΩ, with 80 kHz Filter)

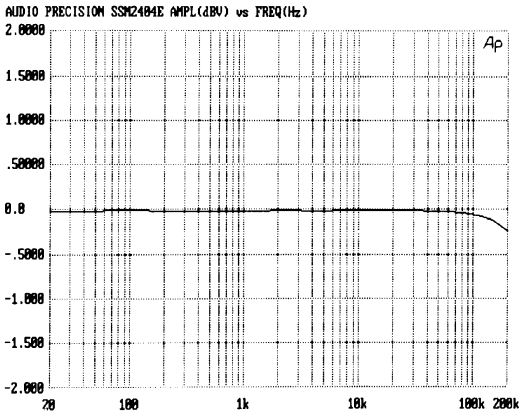


Figure 5. Frequency Response (V_S = ±12 V, V_A = 1 V rms, R_L = 100 kΩ)

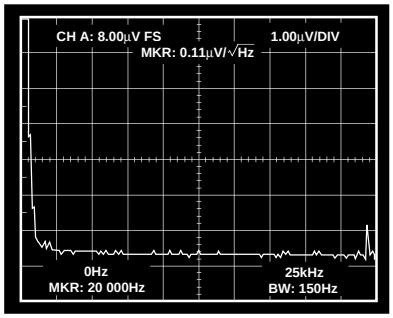


Figure 6. SSM2404 Spectral Noise Density e_n [5 Devices (20 Switches) Chained Together]

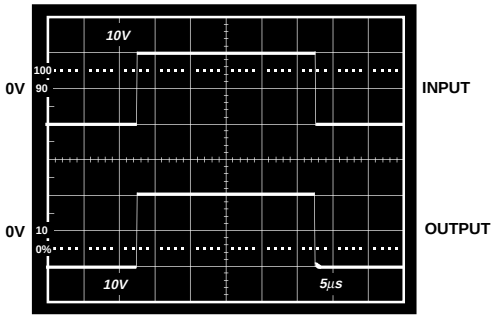


Figure 7. Square Wave Response (T_A = +25°C, V_S = ±12 V, R_L = 100 kΩ, f = 20 kHz)

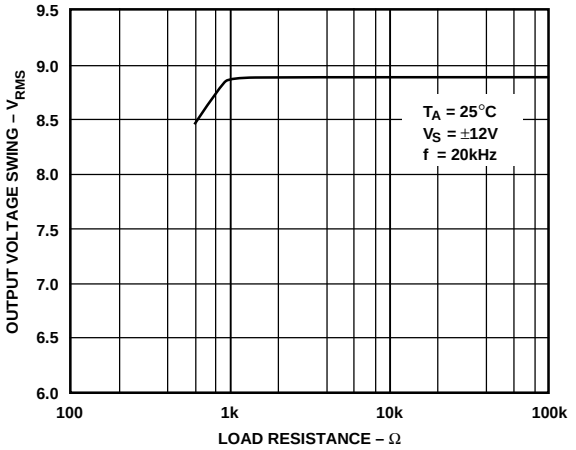


Figure 8. Output Voltage Swing vs. Load Resistance

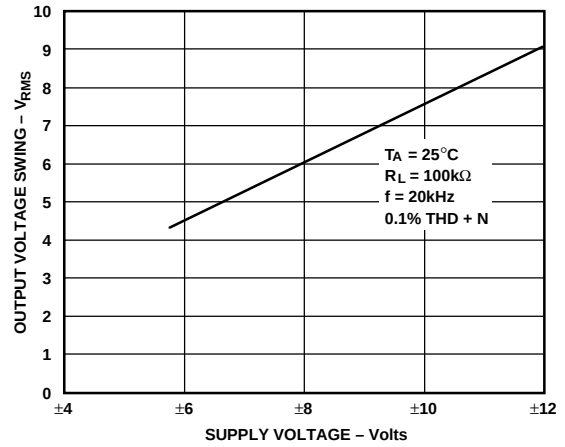


Figure 9. Output Voltage Swing vs. Supply Voltage

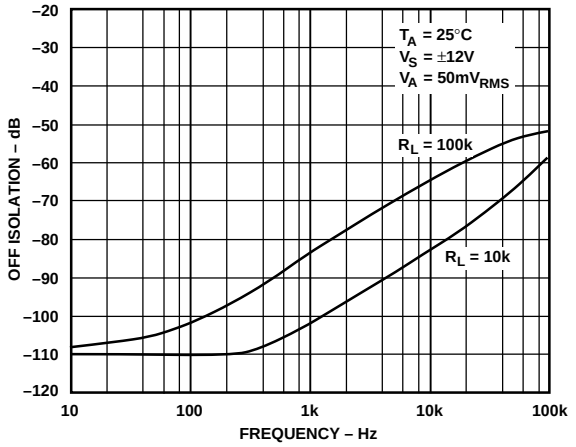


Figure 10. OFF-Isolation vs. Frequency

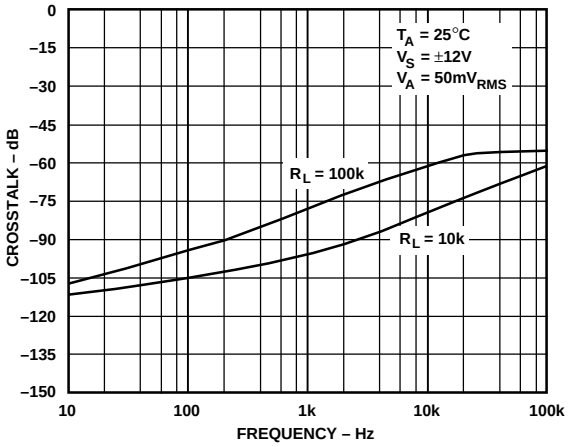


Figure 11. Channel-to-Channel Crosstalk vs. Frequency (Worst Case Conditions, as Measured Between Switches 1 and 4, or 2 and 3)

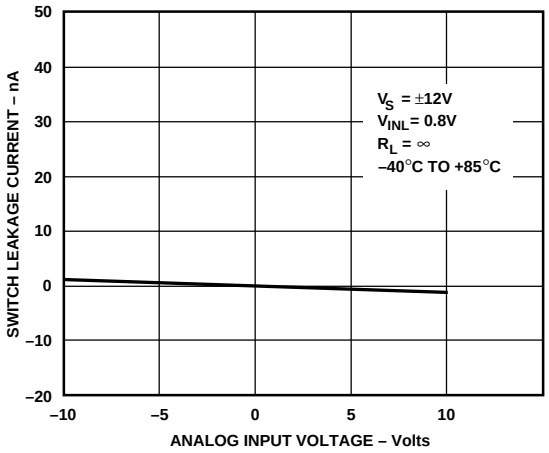


Figure 14. Leakage Current vs. Analog Voltage

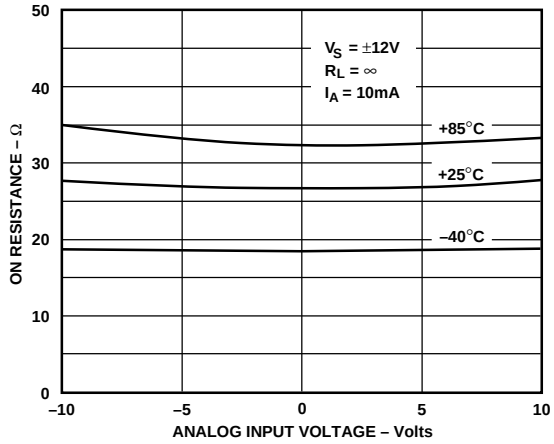


Figure 12. ON Resistance vs. Analog Voltage

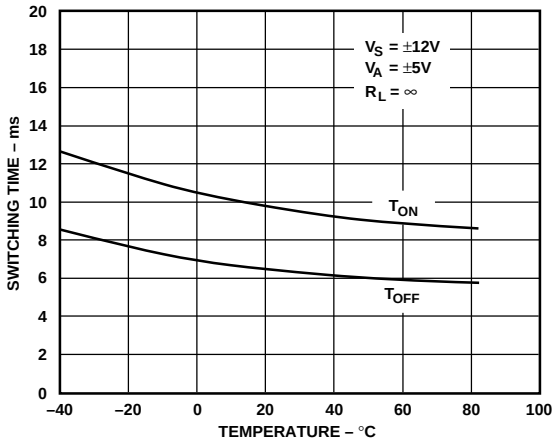


Figure 15. Switching Time vs. Temperature

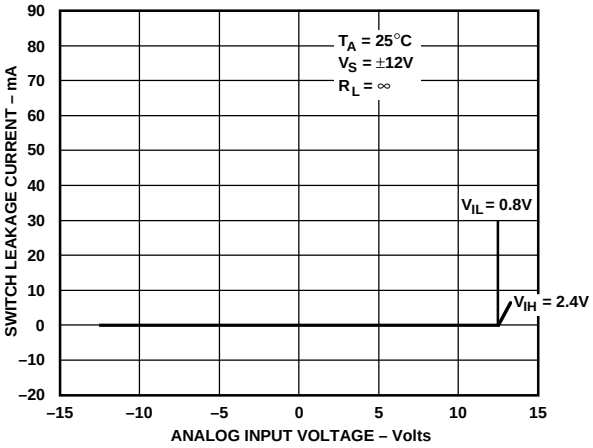


Figure 13. Overvoltage Characteristics

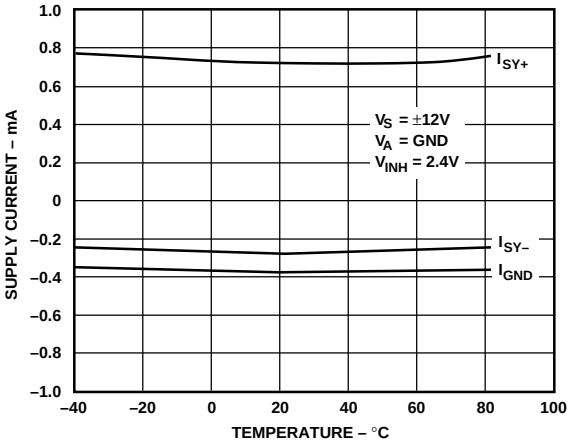


Figure 16. Supply Current vs. Temperature

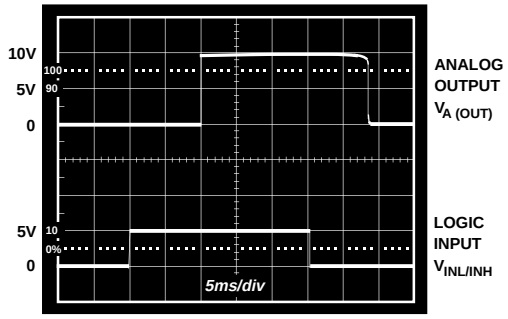


Figure 17. t_{ON}/t_{OFF} Switching Response

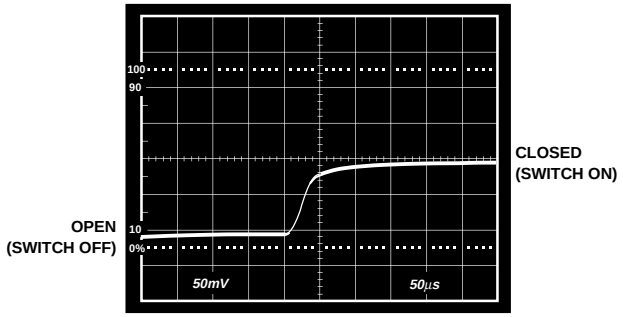


Figure 18. Switch OFF-to-ON Transition (R_L = 5 kΩ)

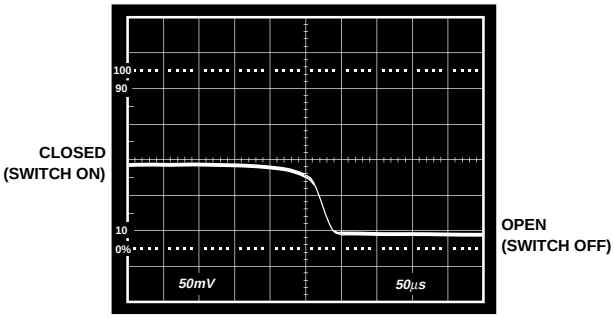


Figure 19. Switch ON-to-OFF Transition (R_L = 5 kΩ)

APPLICATIONS INFORMATION

The SSM2404 integrates four analog CMOS switches with guaranteed "break-before-make" operation to provide high quality audio switching. Each switch has complementary N-channel and P-channel MOSFETs to allow the analog input voltage range to include the positive and negative rails and improve linearity. In addition, the topology permits fully bilateral switching. When using the SSM2404 there is full flexibility in configuring the switches. For example, they can be used individually as shown in Figure 20, or as a double-pole, double-throw (DPDT) switch, which is explained later. The SSM2404 can also be configured as a 4:1 multiplexer, or by using additional packages, as 8:1 or 16:1 and up. The break-before-make feature is guaranteed from part to part allowing such multiple-package applications.

As Figure 20 shows, the SSM2404 is easy to use, and no additional devices are needed. The load resistors are recommended for improved OFF-isolation and charge injection. The ON resistance of the switch is only 28 Ω typically, which causes very little signal attenuation even with a load resistor.

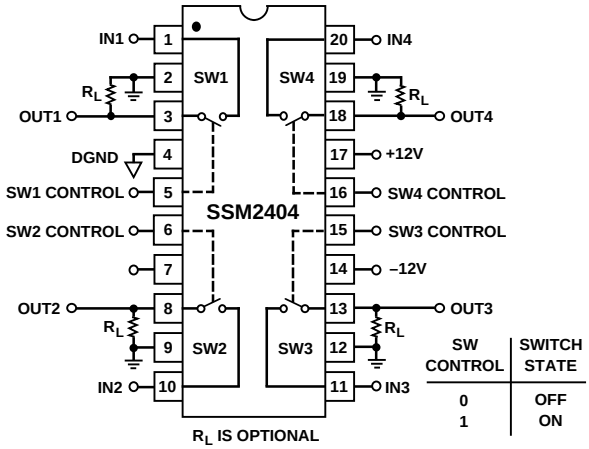


Figure 20. Basic Circuit Configuration

OPTIMIZING PERFORMANCE

As the performance curves show, the switch is optimized for high impedance loads. The distortion performance is at its best when the switch has a load impedance of 100 kΩ or greater as shown in Figure 1. However, even at lower values of load resistances, the 1 kHz distortion performance is still excellent, 0.006% for a 10 kΩ load. The main trade-off with THD is OFF-isolation and crosstalk. This is shown in Figures 10 and 11, again with two different load conditions. As these graphs show, the 10 kΩ load yields approximately a 16 dB improvement in both characteristics.

Thus, the optimum operating point depends on the most critical parameters. When THD is critical then high load impedances should be used; however, when crosstalk and OFF-isolation are critical, lower impedances on the order of 10 kΩ should be used. An additional benefit of using the smaller load resistor is that any charge injected onto the output will be shunted to ground through the resistor. If improved OFF-isolation is needed, the SSM2404 dual audio switch should be considered with its excellent 120 dB OFF-isolation at 20 kHz.

It is important that all of the AGND pins be connected to the system analog ground. These pins isolate the input and output of each switch. Without connecting these pins, the OFF-isolation will degrade significantly.

DETAILED SWITCH OPERATION

A simplified circuit schematic with the functional sections is shown in Figure 21. The TTL interface has an internally regulated 5 V to ensure TTL logic levels regardless of the supply voltage. The logic threshold is with respect to the DGND pin, which can be offset. For example, if DGND is connected to the negative supply, then the SSM2404 will operate with negative rail logic. The interface shifts the control logic down to the negative supply and inverts it to drive N1.

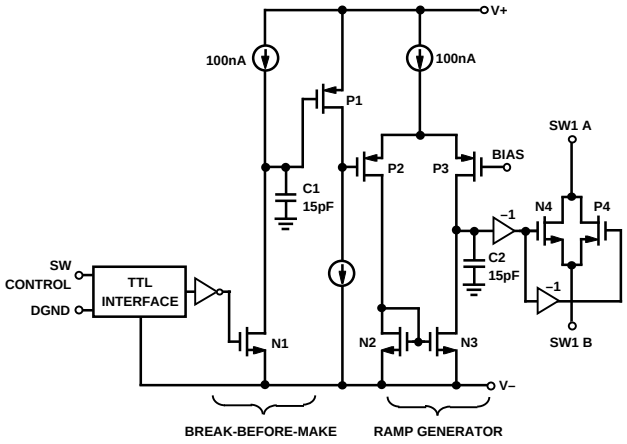


Figure 21. Simplified Schematic

N1 in combination with C1 and the 100 nA current source provides the break-before-make operation of the switch. When the switch is on, N1 is off and C1 is charged up to the positive rail. However, when the SW CONTROL is turned off, then the gate of N1 is pulled high. This turns N1 on, providing a low impedance path to quickly discharge C1 to the negative rail, which quickly "breaks" the switch. On the other hand, when the SW CONTROL goes high again, the gate of N1 is pulled low, turning it off. This leaves C1 to be slowly charged up to the positive rail by the 100 nA current source. The difference in the discharge and charging times ensures break-before-make operation, even from device to device.

The voltage on C1 is inverted by P1 to drive the ramp generator differential pair, consisting of P2, P3 and N2, N3. This differential pair steers the 100 nA of tail current to either charge or discharge C2. As discussed above, when the switch is on, C1 is charged up to the positive rail. P1 inverts this, putting a low voltage equivalent to the negative supply on the gate of P2. The BIAS voltage is approximately equal to the midpoint of the two supply voltages. Thus, when P2 is pulled down, it is turned on and P3 is off. All of the 100 nA flows through N2 and is mirrored by N3. Thus, the 100 nA discharges C2 through N3. When C2 is pulled low, the inverter turns N4 on by pulling its gate high, and the second inverter turns P4 on. To turn the switch off the gate of P2 is pulled above the BIAS so that all 100 nA charges C2 through P3. This is then inverted to turn off N4 and P4.

The internal ramp has rise and fall times on the order of a few milliseconds which is sped up by the inverters. As the gate voltages of N4 and P4 are changing, the ON resistance of each switch is ramping from its OFF state to 28 Ω and vice versa. The actual rise and fall times are shown in Figures 18 and 19 for a 5 kΩ load. These times are significantly slower than typical switches, minimizing the SSM2404's charge injection and giving it "clickless" performance.

DOUBLE-POLE DOUBLE-THROW SWITCH

The SSM2404 is ideal as a one-chip solution for a stereo switch. The schematic in Figure 22 shows the typical configuration. This circuit will select one of two stereo sources, channel A or B. The switch controls for the left and right input of each channel are tied together so that both will be turned on or off simultaneously. An inverter is inserted between the channel A and B controls so that only one logic signal is needed. The outputs can be configured many different ways, such as an inverting or noninverting amplifier stage, and the 10 kΩ load resistors are added to improve the OFF-isolation. The performance of this stereo switch is equivalent to each individual switch, yielding a high quality audio switch that is virtually transparent to the signal.

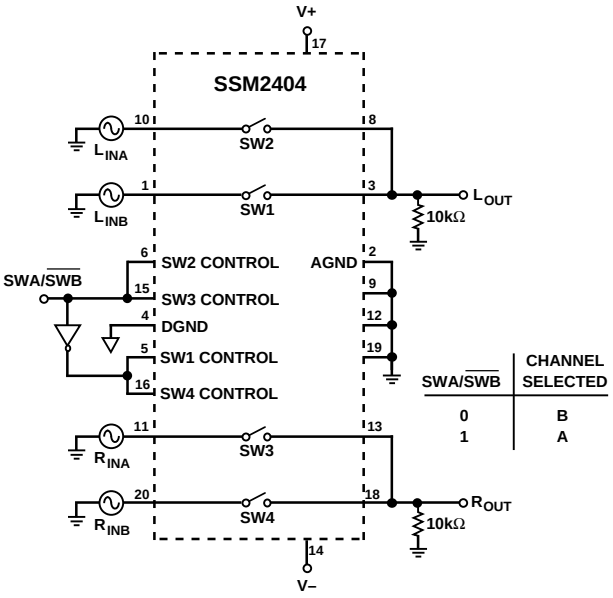


Figure 22. Double-Pole, Double-Throw Stereo Switch

VIRTUAL GROUND SWITCHING

The SSM2404 was built on a CMOS process with a 24 V operating limit for the total supply voltage across the part. This leads to a corresponding limit on the analog voltage range. However, to achieve larger signal swings, the SSM2404 should be configured in the virtual ground mode. As shown in Figure 23, the output of the SSM2404 is connected to the inverting input of an amplifier. Since the noninverting input is grounded, the SSM2404 will also be biased at ground, and large voltage swings on the circuit's input will not significantly change the voltage on the switch. The only limitation is that the current through the switch needs to be less than ±10 mA, and the voltage range is limited only by the op amp and its supply voltages.

The circuit was tested with an SSM2131 high slew rate audio amplifier and the results are shown in Figures 24 and 25. This configuration yields excellent THD performance that is primarily determined by the amplifier. Also, the headroom is now +24 dBu (0 dBu = 0.775 V rms), which is due to the amplifier's output voltage swing. Thus, even though the SSM2404 has a ±12 V limitation on its supplies, it can be used in systems with much higher voltage ranges. For example, the double-pole double-throw switch from Figure 22 can be reconfigured in the virtual ground mode to allow higher voltage swings, as shown in Figure 26. This application realizes the excellent performance of Figures 24 and 25 while providing a low cost switching solution.

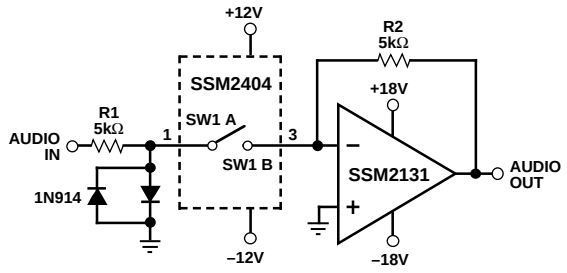


Figure 23. Virtual Ground Switching

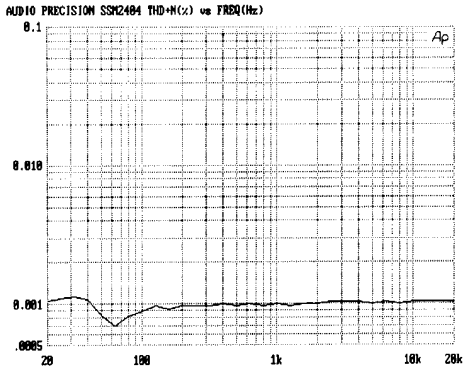


Figure 24. Virtual Ground Switch THD+N vs. Frequency (V_S = ±12 V, V_A = 2 V rms, with 80 kHz Filter)

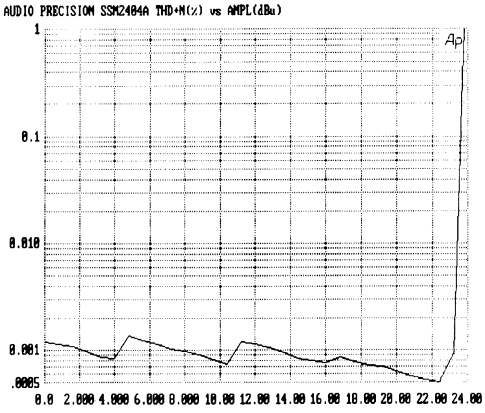


Figure 25. Virtual Ground Switch Headroom (V_S = ±12 V for SSM2404; V_S = ±18 V for Op Amp, f = 1 kHz, with 80 kHz Filter)

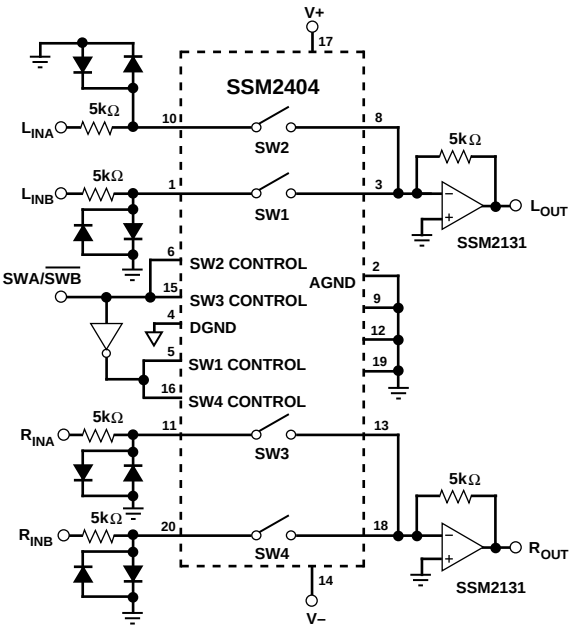


Figure 26. Double-Pole, Double-Throw Stereo Switch Using Virtual Ground Operation

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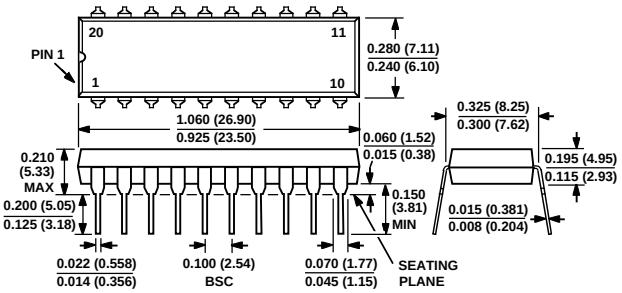
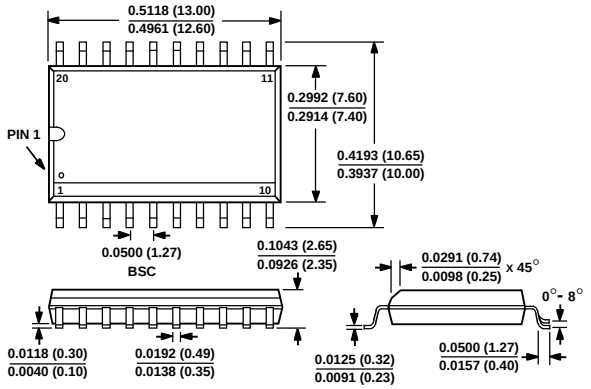
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Mini-DIP (P Suffix)



SOIC (S Suffix)



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