ANALOG DEVICES

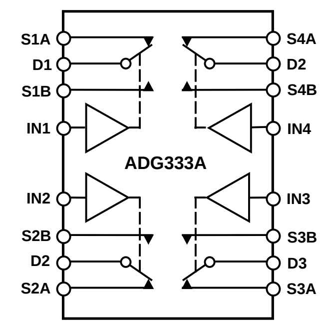
Quad SPDT Switch

ADG333A

FEATURES
44 V Supply Maximum Ratings
V_{SS} to V_{DD} Analog Signal Range
Low On Resistance (45 Ω max)
Low ΔR_{ON} (5 Ω max)
Low R_{ON} Match (4 Ω max)
Low Power Dissipation
Fast Switching Times
t_{ON} < 175 ns
t_{OFF} < 145 ns
Low Leakage Currents (5 nA max)
Low Charge Injection (10 pC max)
Break-Before-Make Switching Action

APPLICATIONS
Audio and Video Switching
Battery Powered Systems
Test Equipment
Communication Systems

FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG333A is a monolithic CMOS device comprising four independently selectable SPDT switches. It is designed on an LC^2MOS process which provides low power dissipation yet achieves a high switching speed and a low on resistance.

The on resistance profile is very flat over the full analog input range ensuring good linearity and low distortion when switching audio signals. High switching speed also makes the part suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the part ideally suited for portable, battery powered instruments.

When they are ON, each switch conducts equally well in both directions and has an input signal range which extends to the power supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG333A is fabricated on an enhanced LC^2MOS process, giving an increased signal range which extends to the supply rails.
2. Low Power Dissipation
3. Low R_{ON}
4. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG333A can be operated from a single rail power supply. The part is fully specified with a single +12 V supply.

REV. 0

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ADG333A–SPECIFICATIONS[1]

DUAL SUPPLY (V_{DD} = +15 V, V_{SS} = –15 V, GND = 0 V, unless otherwise noted)

Parameter	+25°C	–40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
R_{ON}	20		Ω typ	V_D = ±10 V, I_S = –1 mA
	45	45	Ω max	
ΔR_{ON}		5	Ω max	V_D = ±5 V, I_S = –10 mA
R_{ON} Match		4	Ω max	V_D = ±10 V, I_S = –10 mA
LEAKAGE CURRENTS				V_{DD} = +16.5 V, V_{SS} = –16.5 V
Source OFF Leakage I_S (OFF)	±0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V
	±0.25	±3	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.1		nA typ	V_S = V_D = ±15.5 V
	±0.4	±5	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}		±0.005	μA typ	V_{IN} = 0 V or V_{DD}
		±0.5	μA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	90		ns typ	R_L = 300 Ω, C_L = 35 pF;
		175	ns max	V_S = ±10 V; Test Circuit 4
t_{OFF}	80		ns typ	R_L = 300 Ω, C_L = 35 pF;
		145	ns max	V_S = ±10 V; Test Circuit 4
Break-Before-Make Delay, t_{OPEN}	10		ns min	R_L = 300 Ω, C_L = 35 pF;
				V_S = +5 V; Test Circuit 5
Charge Injection	2		pC typ	V_D = 0 V, R_D = 0 Ω, C_L = 10 nF;
	10		pC max	V_{DD} = +15 V, V_{SS} = –15 V; Test Circuit 6
OFF Isolation	72		dB typ	R_L = 75 Ω, C_L = 5 pF, f = 1 MHz;
				V_S = 2.3 V rms, Test Circuit 7
Channel-to-Channel Crosstalk	85		dB typ	R_L = 75 Ω, C_L = 5 pF, f = 1 MHz;
				V_S = 2.3 V rms, Test Circuit 8
C_S (OFF)	5		pF typ	
C_D, C_S (ON)	20		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.05		mA typ	Digital Inputs = 0 V or 5 V
	0.25	0.35	mA max	
I_{SS}	0.01		μA typ	
	1	5	μA max	
V_{DD}/V_{SS}		±3/±20	V min/V max	$\lvert V_{DD}\rvert = \lvert V_{SS}\rvert$

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

SINGLE SUPPLY (V_{DD} = +12 V, V_{SS} = 0 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	+25°C	–40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
R_{ON}	35		Ω typ	V_D = +1 V, +10 V, I_S = –1 mA
		75	Ω max	
LEAKAGE CURRENTS				V_{DD} = +13.2 V
Source OFF Leakage I_S (OFF)	±0.1		nA typ	V_D = 12.2 V/1 V, V_S = 1 V/12.2 V
	±0.25	±3	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.1		nA typ	V_S = V_D = 12.2 V/1 V
	±0.4	±5	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}		±0.005	µA typ	V_{IN} = 0 V or V_{DD}
		±0.5	µA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	110		ns typ	R_L = 300 Ω, C_L = 35 pF;
		200	ns max	V_S = +8 V; Test Circuit 4
t_{OFF}	100		ns typ	R_L = 300 Ω, C_L = 35 pF;
		180	ns max	V_S = +8 V; Test Circuit 4
Break-Before-Make Delay, t_{OPEN}	10		ns min	R_L = 300 Ω , C_L = 35 pF;
			ns min	V_S = +5 V; Test Circuit 5
Charge Injection	5		pC typ	V_D = 6 V, R_D = 0 Ω, C_L = 10 nF;
				V_{DD} = +12 V, V_{SS} = –0 V; Test Circuit 6
OFF Isolation	72		dB typ	R_L = 75 Ω, C_L = 5 pF, f = 1 MHz;
				V_S = 1.15 V rms, Test Circuit 7
Channel-to-Channel Crosstalk	85		dB typ	R_L = 75 Ω, C_L = 5 pF, f = 1 MHz;
				V_S = 1.15 V rms, Test Circuit 8
C_S (OFF)	5		pF typ	
C_D, C_S (ON)	20		pF typ	
POWER REQUIREMENTS				V_{DD} = +13.5 V
I_{DD}	0.05		mA typ	Digital Inputs = 0 V or 5 V
	0.25	0.35	mA max	
V_{DD}		+3/+30	V min/V max	

NOTES

[1]Temperature range is as follows: B Version: –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} . . . . +44 V
V_{DD} to GND . . . . –0.3 V to +30 V
V_{SS} to GND . . . . +0.3 V to –30 V
Analog, Digital Inputs[2] . . . . V_{SS} – 2 V to V_{DD} + 2 V
or 20 mA, Whichever Occurs First
Continuous Current, S or D . . . . 20 mA
Peak Current, S or D . . . . 40 mA
(Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range
Industrial (B Version) . . . . –40°C to +85°C
Storage Temperature Range . . . . –65°C to +125°C
Junction Temperature . . . . +150°C
Plastic Package
θ_{JA}, Thermal Impedance . . . . 103°C/W
Lead Temperature, Soldering (10 sec) . . . . +260°C
SOIC Package
θ_{JA}, Thermal Impedance . . . . 74°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . +215°C
Infrared (15 sec) . . . . +220°C
SSOP Package
θ_{JA}, Thermal Impedance . . . . 130°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . +215°C
Infrared (15 sec) . . . . +220°C

NOTES
[1]Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.
[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG333A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG333ABN	–40°C to +85°C	N-20
ADG333ABR	–40°C to +85°C	R-20
ADG333ABRS	–40°C to +85°C	RS-20

*N = Plastic DIP, R = Small Outline IC (SOIC). RS = Shrink Small Outline Package (SSOP).

Table I. Truth Table

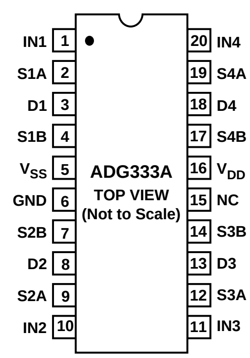
Logic	Switch A	Switch B
0	OFF	ON
1	ON	OFF

TERMINOLOGY

S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input.
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	R_{ON} variation due to a change in the analog input voltage with a constant load current.
R_{ON} Match	Difference between the R_{ON} of any two channels.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	"OFF" Switch Source Capacitance.
C_D (OFF)	"OFF" Switch Drain Capacitance.
C_D, C_S (ON)	"ON" Switch Capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on.
t_{OFF}	Delay between applying the digital control input and the output switching off.
t_{OPEN}	Break Before Make delay when switches are configured as a multiplexer.
V_{INL}	Maximum input voltage for logic "0."
V_{INH}	Minimum input voltage for logic "1."
I_{INL} (I_{INH})	Input current of the digital input.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.

PIN CONFIGURATION

DIP/SOIC/SSOP



NC = NO CONNECT

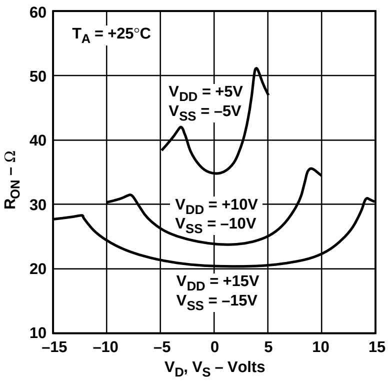


Figure 1. R_{ON} as a Function of V_D (V_S): Dual Supply

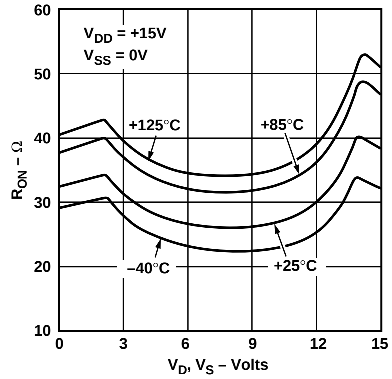


Figure 4. R_{ON} as a Function of V_D (V_S) for Different Temperatures: Single Supply

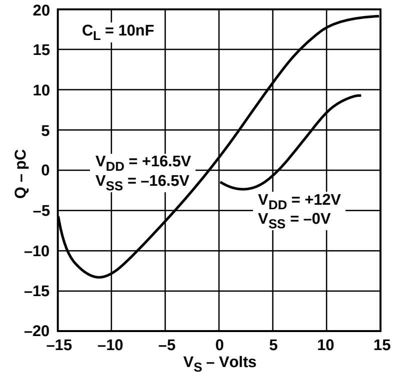


Figure 7. Charge Injection as a Function of V_S

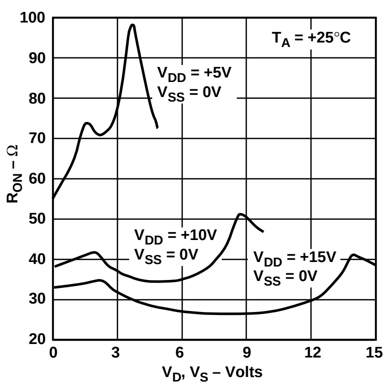


Figure 2. R_{ON} as a Function of V_D (V_S): Single Power Supply

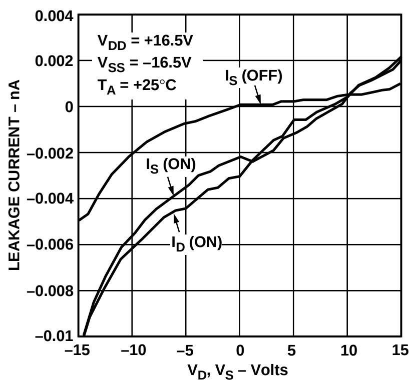


Figure 5. Leakage Currents as a Function of V_D (V_S): Dual Supply

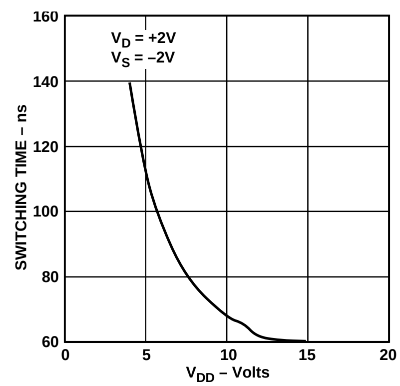


Figure 8. Switching Time as a Function of V_{DD}

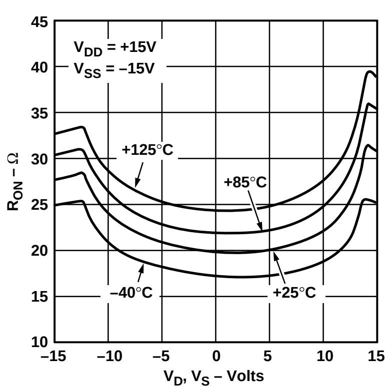


Figure 3. R_{ON} as a Function of V_D (V_S) for Different Temperatures: Dual Supply

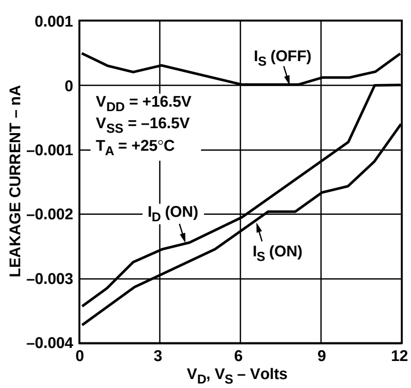


Figure 6. Leakage Currents as a Function of V_D (V_S): Single Supply

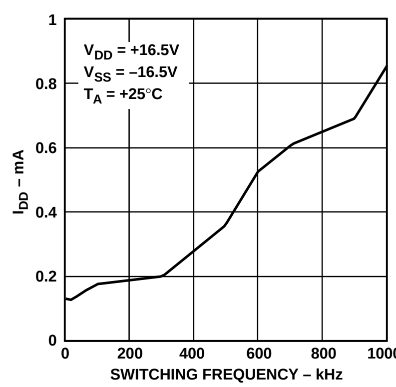
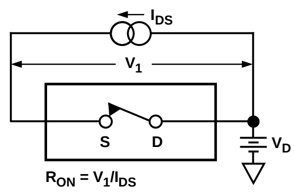
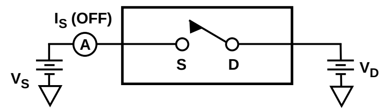


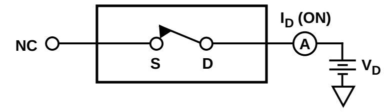
Figure 9. I_{DD} as a Function of Switching Frequency



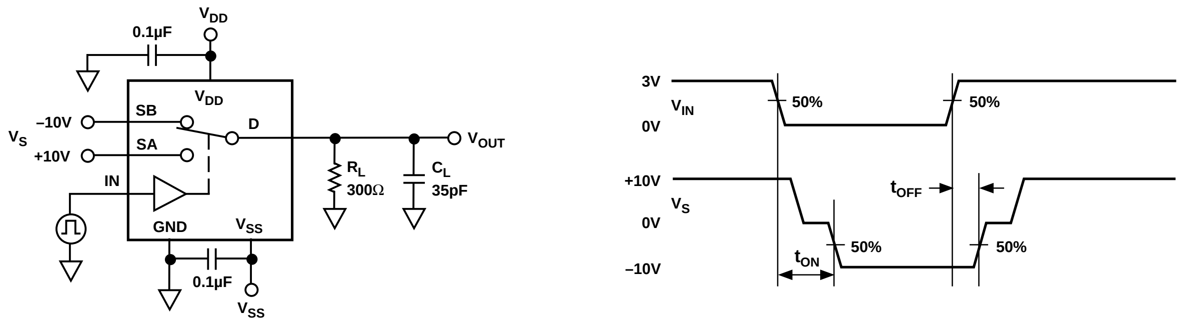
Test Circuit 1. On Resistance



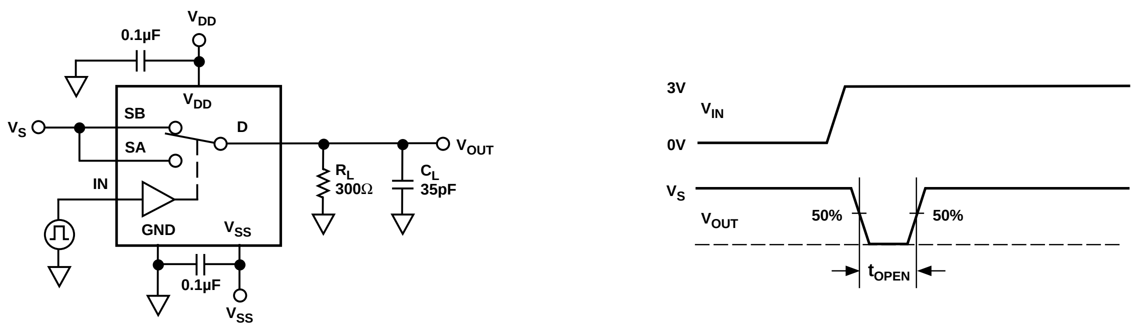
Test Circuit 2. Off Leakage



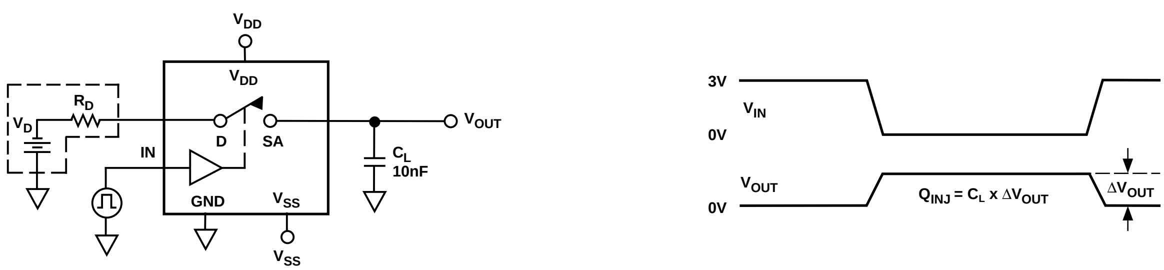
Test Circuit 3. On Leakage



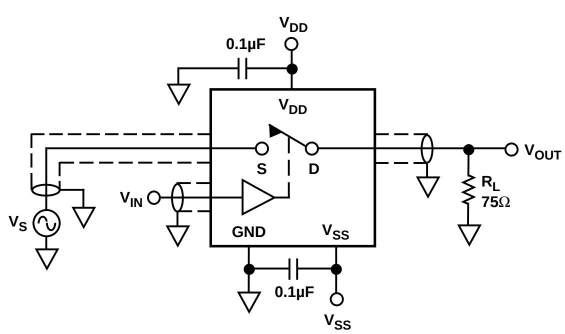
Test Circuit 4. Switching Times



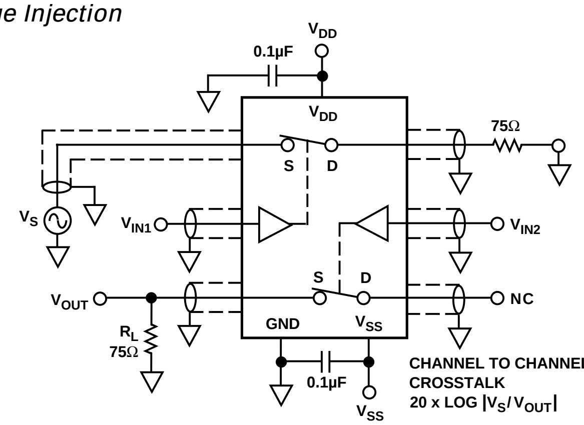
Test Circuit 5. Break-Before-Make Delay, t_{OPEN}



Test Circuit 6. Charge Injection



Test Circuit 7. Off Isolation



Test Circuit 8. Channel-to-Channel Crosstalk

APPLICATIONS INFORMATION

ADG333A Supply Voltages

The ADG333A can operate off a dual or signal supply. V_{SS} should be connected to GND when operating with a single supply. When using a dual supply the ADG333A can also operate with unbalanced supplies, for example V_{DD} = 20 V and V_{SS} = –5 V. The only restrictions are that V_{DD} to GND must not exceed 30 V, V_{SS} to GND must not drop below –30 V and V_{DD} to V_{SS} must not exceed +44 V. It is important to remember that the ADG333A supply voltage directly affects the input signal range, the switch ON resistance and the switching times of the part. The effects of the power supplies on these characteristics can be clearly seen from the characteristic curves in this data sheet.

Power Supply Sequencing

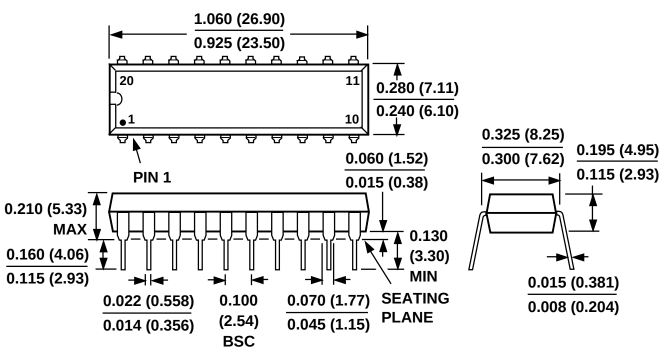
When using CMOS devices care must be taken to ensure correct power-supply sequencing. Incorrect power-supply sequencing can result in the device being subjected to stresses beyond those maximum ratings listed in the data sheet. This is also true for the ADG333A. Always sequence V_{DD} on first followed by V_{SS} and the logic signals. An external signal within the maximum specified ratings can then be safely presented to the source or drain of the switch

C2076–18–10/95

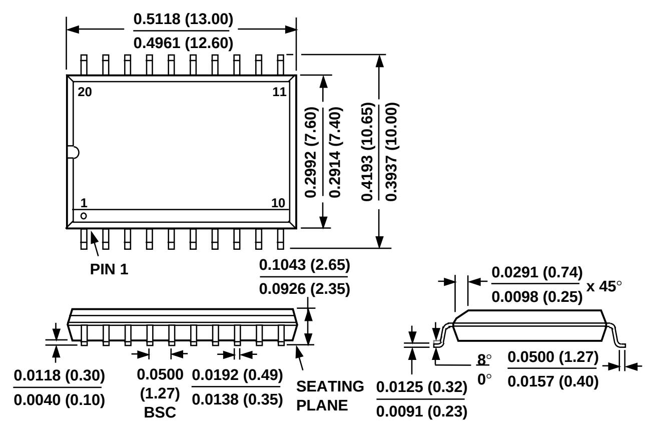
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

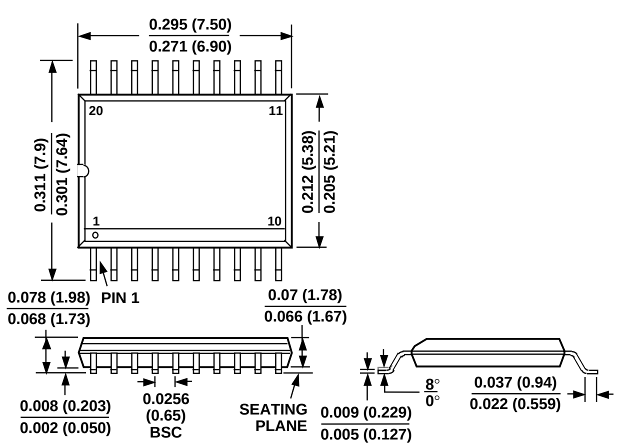
20-Pin Plastic DIP (N-20)



20-Pin SOIC (R-20)



20-Pin SSOP (RS-20)



LEADS WILL BE EITHER TIN PLATED OR SOLDIER DIPPED
IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS

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