Quad 10-bit, 40/65 MSPS Serial LVDS 1.8 V A/D Converter

Preliminary Technical Data

AD9219

FEATURES

Four ADCs in one package
Serial LVDS (ANSI-644 ,IEEE 1596.3 reduced range link)
Data and frame clock outputs
SNR = 61 dB (to Nyquist)
Excellent linearity
- **DNL = ±0.3 LSB (typical)**
- **INL = ±0.5 LSB (typical)**

400 MHz full power analog bandwidth
112 mW ADC power per channel at 65 MSPS
2 Vp-p input voltage range
1.8 V supply operation
Serial port control
- **Full-chip and individual-channel power-down modes**
- **Flexible bit orientation**
- **Built-in and custom digital test pattern generation**
- **Programmable clock and data alignment**
- **Programmable output resolution**
- **Standby mode**
- **Programmable input bandwidth**

APPLICATIONS

Tape drives
Medical imaging / Ultrasound
Quadrature Radio Recievers

FUNCTIONAL BLOCK DIAGRAM

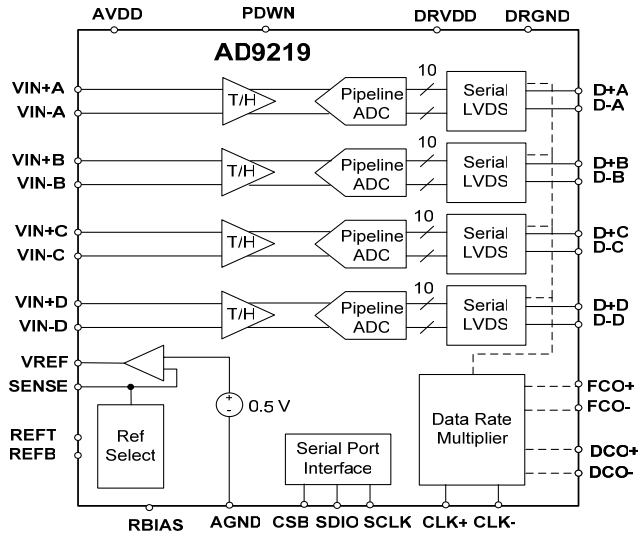

Figure 1. Functional Block Diagram

PRODUCT DESCRIPTION

The AD9219 is a quad 10-bit, 65 MSPS analog-to-digital converter (ADC) with an on-chip track-and-hold circuit that is designed for low cost, low power, small size, and ease of use. The product operates up to a 65 MSPS conversion rate and is optimized for outstanding dynamic performance and low power where a small package size is critical.

The ADC requires a single 1.8 V power supply and a LVPECL/CMOS/LVDS compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock (DCO) for capturing data on the output and a frame clock (FCO) trigger for signaling a new output byte are provided. Individual channel power down is supported and typically consumes less than 3 mW when all channels are enabled.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudo-random patterns, along with custom, user-defined test patterns entered via the serial port interface (SPI).

The AD9219 is available in a Pb Free, 48-LFCSP. It is specified over the industrial temperature range of –40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Four ADCs are contained in a small, space-saving package and low power of 112mW/channel at 65MSPS.
2. A data clock out (DCO) is provided, which operates up to 325 MHz and supports double-data rate operation (DDR).
3. The outputs of each ADC are serialized LVDS with data rates up to 650 Mbps (10 bits × 65 MSPS).
4. Serial port interface (SPI) control offers wide range of flexible features to meet specific system requirements

Rev. PrB

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5. The AD9219 operates from a single 1.8 V power supply.
6. Pin compatible family including the AD9287 (8bit), AD9228 (12bit), AD9259 (14bit).

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REVISION HISTORY

11/04—Initial Version: Rev. A

1/17/05 – Rev B, Updated Power Supply Specs, Rid of CML references

6/20/05 – Updated Full Power Bandwidth Spec

7/8/05 – Updated Power Supplies and Power Specs

8/2/05 – Deleted Test Levels

8/29/05 – Updated Pinout, performance plots and timing diagram

9/8/05 – Updated FFT Plots, power & SNR specs

9/15/05 – Added Theory of Op, SPI Table, and Eval Brd info.

SPECIFICATIONS

AVDD = 1.8V, DRVDD = 1.8V conversion rate = 65 MSPS, 2Vp-p differential input, 1.0V internal reference, AIN = –0.5 dBFS, unless otherwise noted.

Table 1.Specifications[1]

Parameter	AD9219-40			AD9219-65			
	Min	Typ	Max	Min	Typ	Max	Unit
RESOLUTION	12			12			Bits
ACCURACY							
No Missing Codes		Guaranteed			Guaranteed		
Offset Error		±0.5			±0.5		mV
Offset Matching		±25			±25		mV
Gain Error		±0.5			±0.5		% FS
Gain Matching		±2			±2		% FS
Differential Nonlinearity (DNL)		±0.3			±0.3		LSB
		±0.3			±0.3		LSB
Integral Nonlinearity (INL)		±0.5			±0.5		LSB
		±0.5			±0.5		LSB
TEMPERATURE DRIFT							
Offset Error		TBD			TBD		ppm/°C
Gain Error		TBD			TBD		ppm/°C
Reference Voltage (1 V Mode)		TBD			TBD		ppm/°C
REFERENCE							
Output Voltage Error (VREF = 1 V)		TBD			TBD		mV
Load Regulation @ 1.0 mA (VREF = 1 V)		TBD			TBD		mV
Input Resistance		TBD			TBD		kΩ
COMMON-MODE Level Output							
Voltage		AVDD/2			AVDD/2		V
Load Regulation		TBD			TBD		
ANALOG INPUTS							
Differential Input Voltage Range (VREF = 1 V)		2			2		Vp-p
Common Mode Voltage		AVDD/2			AVDD/2		V
Input Capacitance		7			7		pF
Analog Bandwidth, Full Power		400			400		MHz
POWER SUPPLY							
AVDD	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	1.7	1.8	1.9	1.7	1.8	1.9	V
IAVDD		222.2	TBD		222.2	TBD	mA
IDRVDD		27	TBD		27	TBD	mA
Total Power Dissipation (including output drivers)		450			450		mW
Power-Down Dissipation		<3	TBD		<3	TBD	mW
Power Supply Rejection Ratio (PSRR)		TBD			TBD		mV/V
CROSSTALK		-90			-90		dB

AC SPECIFICATIONS

AVDD = 1.8V, DRVDD = 1.8V, conversion rate = 65 MSPS, 2Vp-p differential input, 1.0V internal reference, AIN = –0.5 dBFS, unless otherwise noted.

Table 2.

Parameter		AD9219-40 Min	AD9219-40 Typ	AD9219-40 Max	AD9219-65 Min	AD9219-65 Typ	AD9219-65 Max	Unit
SIGNAL TO NOISE RATIO (SNR)	f_{IN} = 2.3 MHz		61			61		dB
	f_{IN} = 10.3 MHz	TBD			TBD			dB
	f_{IN} = 19.7 MHz		61					dBc
	f_{IN} = 35 MHz					61		dB
	f_{IN} = 70MHz	TBD			TBD			dB
SIGNAL TO NOISE AND DISTORTION RATIO (SINAD)	f_{IN} = 2.3 MHz		60.5			60.5		dB
	f_{IN} = 10.3 MHz	TBD			TBD			dB
	f_{IN} = 19.7 MHz		60.5					dB
	f_{IN} = 35 MHz					60.5		dB
	f_{IN} = 70MHz	TBD			TBD			dB
EFFECTIVE NUMBER OF BITS (ENOB)	f_{IN} = 2.3 MHz		9.7			9.7		Bits
	f_{IN} = 10.3 MHz	TBD			TBD			Bits
	f_{IN} = 19.7 MHz		9.7					Bits
	f_{IN} = 35 MHz					9.7		Bits
	f_{IN} = 70MHz	TBD			TBD			Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)	f_{IN} = 2.3 MHz		80			80		dB
	f_{IN} = 10.3 MHz	TBD			TBD			dB
	f_{IN} = 19.7 MHz		80					dB
	f_{IN} = 35 MHz		80			80		dB
	f_{IN} = 70MHz	TBD			TBD			dB
WORST HARMONIC (Second or Third)	f_{IN} = 2.3 MHz		-80			-80		dBc
	f_{IN} = 10.3 MHz			TBD			TBD	dBc
	f_{IN} = 19.7 MHz		-80					dBc
	f_{IN} = 35 MHz					-80		dBc
	f_{IN} = 70MHz	TBD			TBD			dBc
WORST OTHER (Excluding Second or Third)	f_{IN} = 2.3 MHz		-80			-80		dBc
	f_{IN} = 10.3 MHz			TBD			TBD	dBc
	f_{IN} = 19.7 MHz		-80					dBc
	f_{IN} = 35 MHz					-80		dBc
	f_{IN} = 70MHz	TBD			TBD			dBc
TWO TONE INTERMOD DISTORTION (IMD) AIN1 and AIN2 = -7.0dBFS	f_{IN1} = 15 MHz, f_{IN2} = 16 MHz		TBD			TBD		dBc
	f_{IN1} = 70 MHz, f_{IN2} = 71 MHz		TBD			TBD		dBc

DIGITAL SPECIFICATIONS

AVDD = 1.8V, DRVDD = 1.8V, conversion rate = 65 MSPS, 2Vp-p differential input, 1.0V internal reference, AIN = –0.5 dBFS, unless otherwise noted.

Table 3.

Parameter	AD9219-40 Min	AD9219-40 Typ	AD9219-40 Max	AD9219-65 Min	AD9219-65 Typ	Max	Unit

Parameter	AD9219-40 Min	Typ	Max	AD9219-65 Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK–)							
Logic Compliance		CMOS/LVDS/LVPECL			CMOS/LVDS/LVPECL		
Differential Input Voltage	TBD			TBD			mVp-p
High Level Input Current		TBD			TBD		uA
Low Level Input Current		TBD			TBD		uA
Input Common-Mode Voltage		TBD			TBD		V
Input Resistance		TBD			TBD		kΩ
Input Capacitance		TBD			TBD		pF
LOGIC INPUTS (PDWN,CSB,SCLK/DTP,SDIO/ODM)							
Logic 1 Voltage	TBD			TBD			V
Logic 0 Voltage			TBD			TBD	V
Input Resistance		TBD			TBD		kΩ
Input Capacitance		TBD			TBD		pF
LOGIC OUTPUTS (SDIO)							
Logic 1 Voltage	TBD			TBD			V
Logic 0 Voltage			TBD			TBD	V
Input Resistance		TBD			TBD		kΩ
Input Capacitance		TBD			TBD		pF
DIGITAL OUTPUTS (D+, D-), (ANSI-644)							
Logic Compliance	LVDS			LVDS			
Differential Output Voltage (V_{OD})	247		454	247		454	mV
Output Offset Voltage (V_{OS})	1.125		1.375	1.125		1.375	V
Output Coding		Offset Binary			Offset Binary		
DIGITAL OUTPUTS (D+, D-), (IEEE 1596.3)							
Logic Compliance	LVDS			LVDS			
Differential Output Voltage (V_{OD})	150		250	150		250	mV
Output Offset Voltage (V_{OS})	1.150		1.250	1.150		1.250	V
Output Coding		Offset Binary			Offset Binary		

[1] With a 1.0 V internal reference.

SWITCHING SPECIFICATIONS

AVDD = 1.8V, DRVDD = 1.8V, conversion rate = 65 MSPS, 2Vp-p differential input, 1.0V internal reference, AIN = –0.5 dBFS, unless otherwise noted.

Table 4.

Parameter	AD9219-40 Min	Typ	Max	AD9219-65 Min	Typ	Max	Unit
CLOCK							
Maximum Clock Rate	40			65			MSPS
Minimum Clock Rate			10			10	MSPS
Clock Pulse Width High (t_{EH})							ns
Clock Pulse Width Low (t_{EL})							ns

OUTPUT PARAMETERS							
Valid Time (t_V)[1]		TBD			TBD		CLK cycles
Propagation Delay (t_{PD})		TBD			TBD		ns
Rise Time (t_R) (20% to 80%)		TBD			TBD		ps
Fall Time (t_F) (20% to 80%)		TBD			TBD		ps
FCO Propagation Delay (t_{FCO})		TBD			TBD		ns
DCO Propagation Delay (t_{CPD})		TBD			TBD		ns
DCO to Data Delay (t_{DATA})							ps
DCO to FCO Delay (t_{FRAME})							ps
Data to DCO Skew ($t_{PD} – t_{CPD}$)							ps
Data to Data Skew ($t_{DATA-MAX} - t_{DATA-MIN}$)							ps
Wake-Up Time		TBD			TBD		ms
Pipeline Latency		TBD			TBD		CLK cycles
APERTURE							
Aperture Delay (t_A)		TBD			TBD		ps
Aperture Uncertainty (Jitter)		TBD			TBD		ps rms
Out-of-Range Recovery Time		TBD			TBD		CLK cycles

[1] Clock inputs are LVDS-compatible. They require external dc bias and cannot be ac-coupled.

TIMING DIAGRAMS

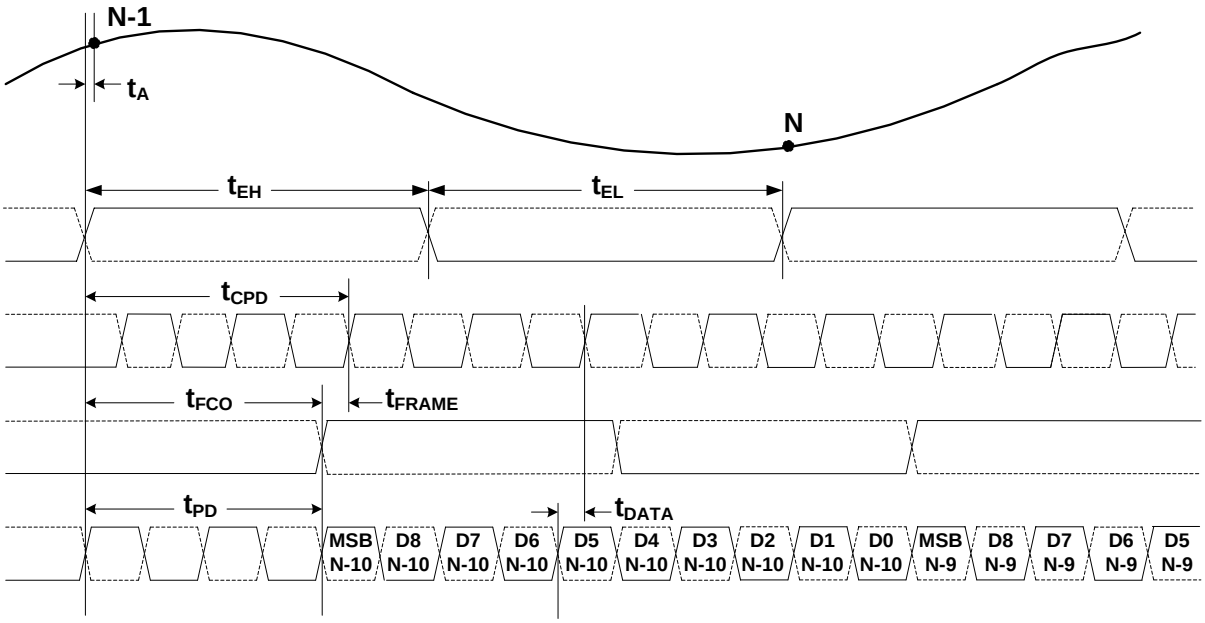


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect To	Min	Max	Unit
ELECTRICAL				
AVDD	AGND	–0.3	+ TBD	V
DRVDD	DRGND	–0.3	+ TBD	V
AGND	DRGND	–0.3	-0.3	V
DRGND	DRVDD	-0.3	+ TBD	V
Digital Outputs (D+, D–, DCO+, DCO–,FCO+, FCO–)	DRGND	–0.3	DRVDD + 0.3	V
CLK+, CLK–	AGND	–0.3	AVDD + 0.3	V
VIN+, VIN–	AGND	–0.3	AVDD + 0.3	V
PDWN, CSB, SCLK/DTP, SDIO/ODM	AGND	–0.3	AVDD + 0.3	V
REFT, REFB, RBIAS	AGND	–0.3	AVDD + 0.3	V
VREF, SENSE	AGND	–0.3	AVDD + 0.3	V
ENVIRONMENTAL				
Operating Temperature Range (Ambient)		–40	+85	°C
Maximum Junction Temperature		150		°C
Lead Temperature (Soldering, 10 sec)		TBD		°C
Maximum Case Temperature		TBD		°C
Storage Temperature Range (Ambient)		TBD	TBD	°C
Thermal Impedance[1]			TBD	°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1] θ_{JA} for a 4-layer PCB with solid ground plane in still air.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

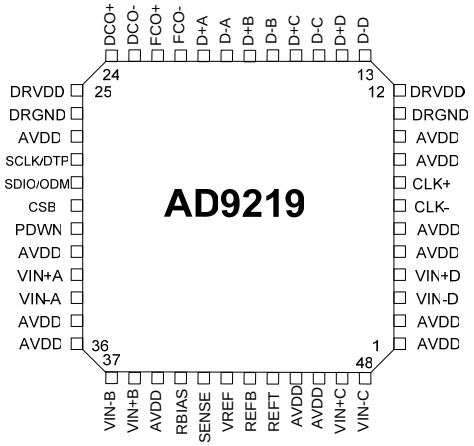


Figure 3. 48LFCSP 7x7 Top View

Table 6. Pin Function Descriptions

Pin Number	Name	Description
0	AGND	Analog Ground (exposed paddle)
1,2,5,6,9,10 ,27,32,35,3 6,39,45,46	AVDD	1.8 V Analog Supply
11,26	DRGND	Digital Output Driver Ground
12,25	DRVDD	1.8 V Digital Output Driver Supply
28	SCLK/DTP	SCLK / Digital Test Pattern
29	SDIO/ODM	SDIO / Output Driver Mode
30	CSB	CSB
31	PDWN	Power Down
33	VIN+A	ADC A Analog Input – True
34	VIN-A	ADC A Analog Input – Complement
37	VIN-B	ADC B Analog Input – Complement
38	VIN+B	ADC B Analog Input – True
40	RBIAS	External resistor sets the Internal ADC Core Bias Current
41	SENSE	Reference Mode Selection
42	VREF	Voltage Reference Input/Output
43	REFB	Differential Reference (Negative)
44	REFT	Differential Reference (Positive)
47	VIN+C	ADC C Analog Input – True
48	VIN-C	ADC C Analog Input – Complement
3	VIN-D	ADC D Analog Input – Complement
4	VIN+D	ADC D Analog Input – True
7	CLK-	Input Clock – Complement
8	CLK+	Input Clock – True
13	D-D	ADC D Complement Digital Output
14	D+D	ADC D True Digital Output
15	D-C	ADC C Complement Digital Output
16	D+C	ADC C True Digital Output
17	D-B	ADC B Complement Digital Output
18	D+B	ADC B True Digital Output
19	D-A	ADC A Complement Digital Output
20	D+A	ADC A True Digital Output
21	FCO-	Frame Clock Output - Complement
22	FCO+	Frame Clock Output- True
23	DCO-	Data Clock Output – Complement
24	DCO+	Data Clock Output – True

EQUIVALENT CIRCUITS

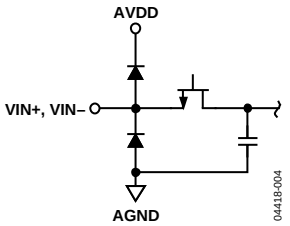


Figure 3. Equivalent Analog Input Circuit

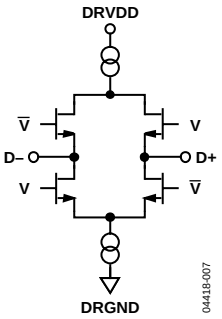


Figure 6. Equivalent Digital Output Circuit

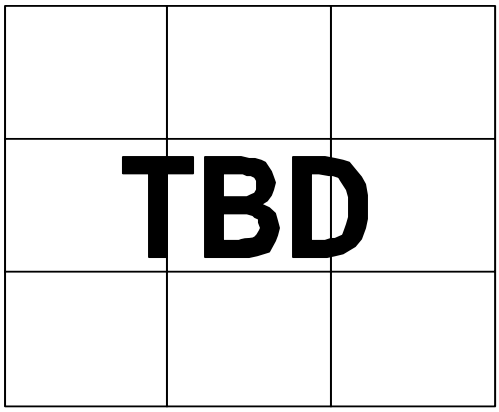


Figure 4. Equivalent Clock Input Circuit

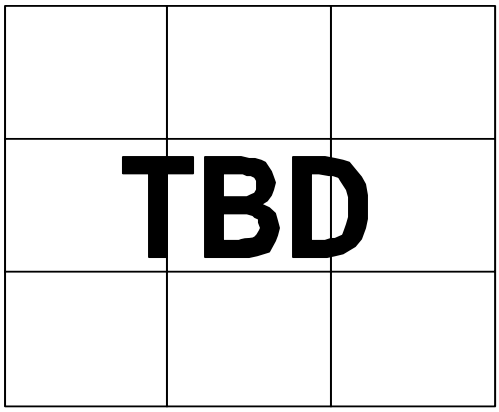


Figure 7. Equivalent PDWN Input Circuit

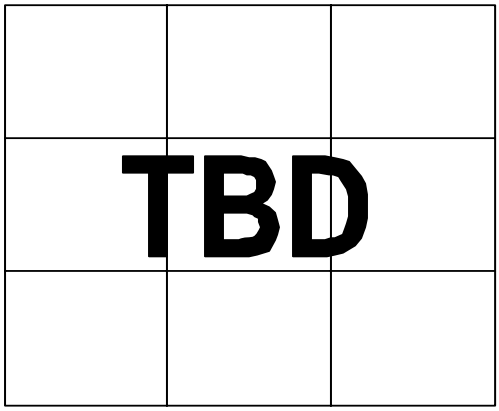


Figure 5. Equivalent Digital Input Circuit (CSB,SCLK/DTP,SDIO/ODM)

TYPICAL PERFORMANCE CHARACTERISTICS

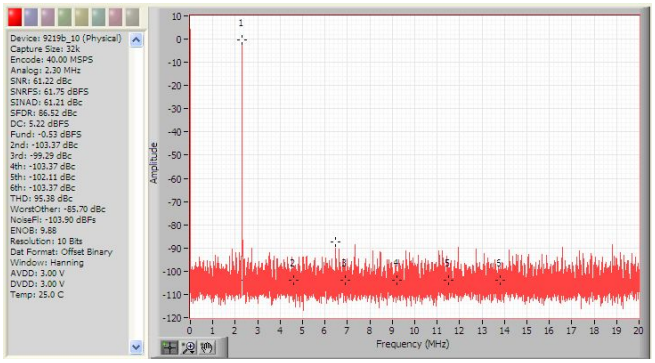


Figure 8. Single-Tone 32k FFT with f_{IN} = 2.3 MHz, f_{SAMPLE} = 40 MSPS

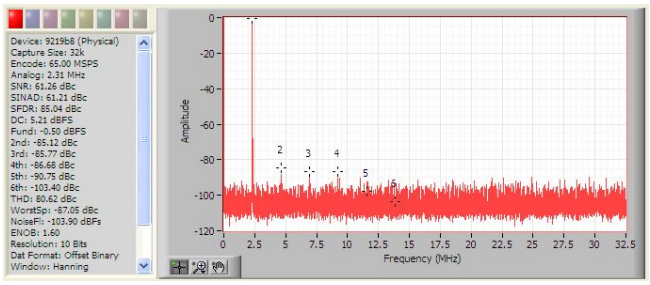


Figure 9. Single-Tone 32k FFT with f_{IN} = 2.3 MHz, f_{SAMPLE} = 65 MSPS

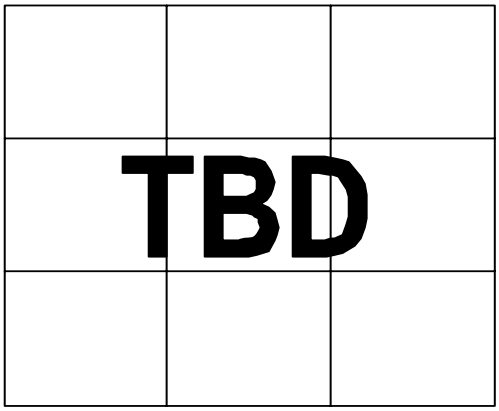


Figure 10. Single-Tone 32k FFT with f_{IN} = 70 MHz, f_{SAMPLE} = 65 MSPS

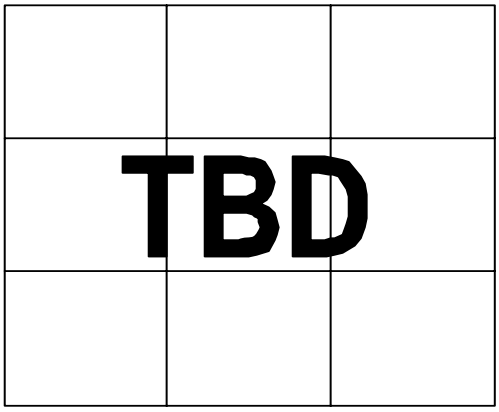


Figure 11. Single-Tone 32k FFT with f_{IN} = 120 MHz, f_{SAMPLE} = 65 MSPS

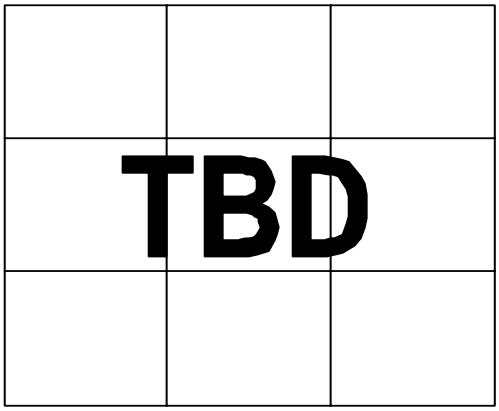


Figure 12. AD9219-40 SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 10.3 MHz

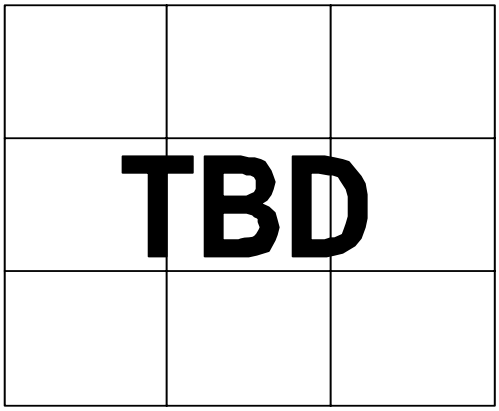


Figure 13. AD9219-40, SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 25 MHz

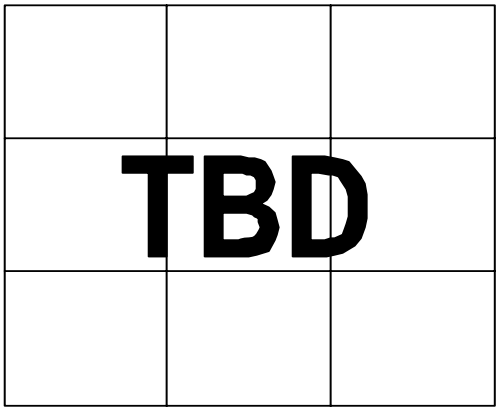


Figure 14. AD9219-65, SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 10.3 MHz

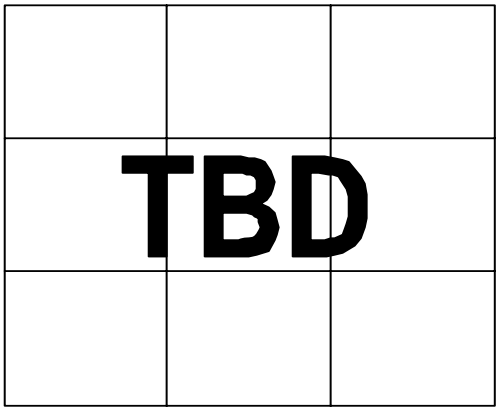


Figure 17. AD9219-40, SNR/SFDR vs. Analog Input Level, f_{IN} =25 MHz

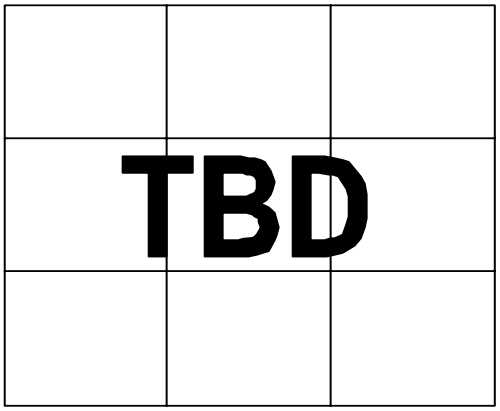


Figure 15. AD9219-65, SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 30 MHz

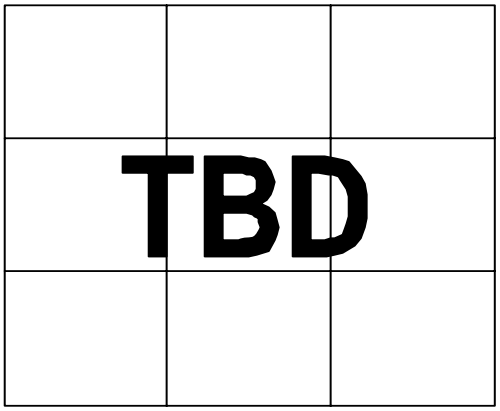


Figure 18. AD9219-65, SNR/SFDR vs. Analog Input Level, f_{IN} = 10.3 MHz

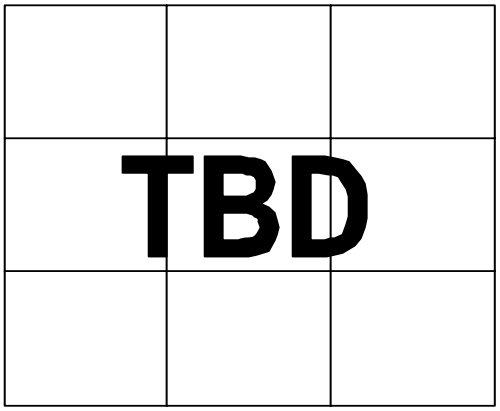


Figure 16. AD9219-40, SNR/SFDR vs. Analog Input Level, f_{IN} = 10.3 MHz

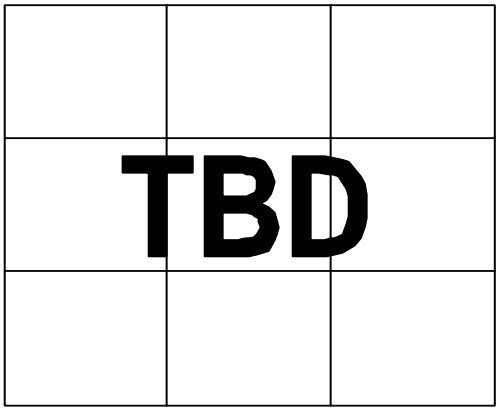


Figure 19. AD9219-65, SNR/SFDR vs. Analog Input Level, f_{IN} = 30 MHz

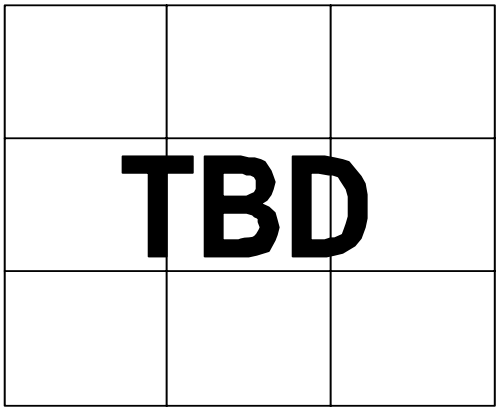


Figure 20. SNR/SFDR vs. f_{IN}, f_{SAMPLE} = 65 MHz

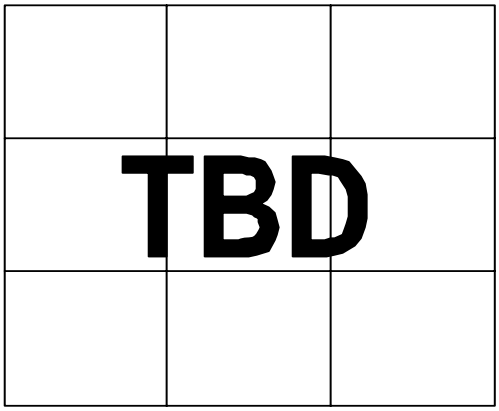


Figure 23. Two-Tone SFDR vs. Analog Input Level, f_{IN1} = 15 MHz and f_{IN2} = 16 MHz, f_{SAMPLE} = 65 MSPS

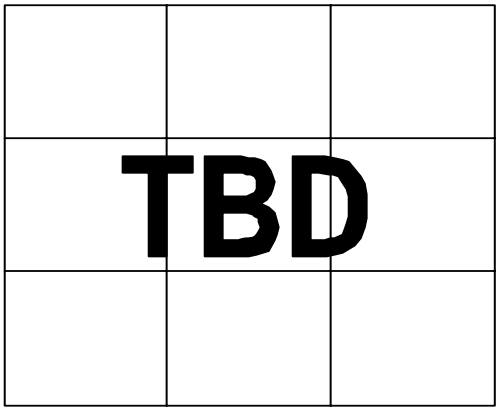


Figure 21. Two-Tone 32k FFT with f_{IN1} = 15 MHz and f_{IN2} = 16 MHz, f_{SAMPLE} = 65 MSPS

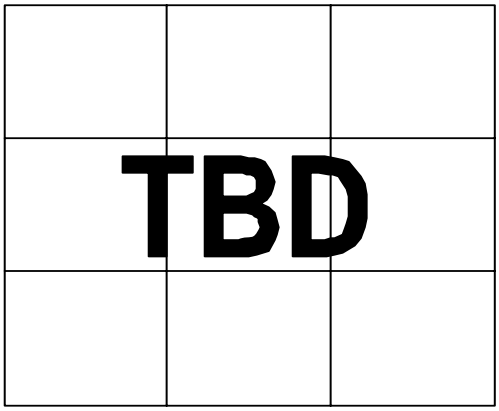


Figure 24. Two-Tone SFDR vs. Analog Input Level, f_{IN1} = 69 MHz and f_{IN2} = 70 MHz, f_{SAMPLE} = 65 MSPS

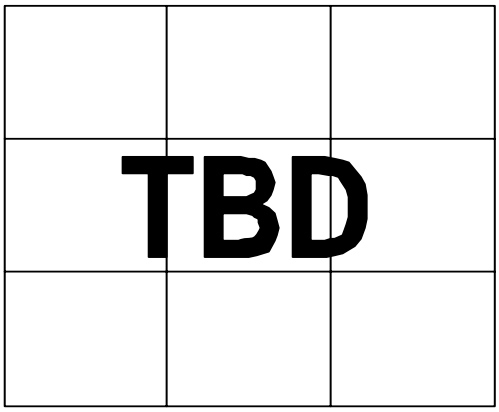


Figure 22. Two-Tone 32k FFT with f_{IN1} = 69 MHz and f_{IN2} = 70 MHz, f_{SAMPLE} = 65 MSPS

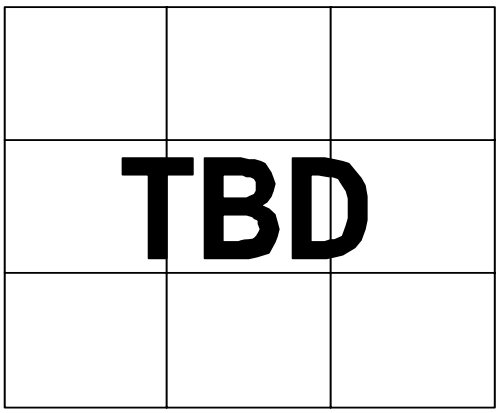


Figure 25. SINAD/SFDR vs. Temperature, f_{IN} 10.3 MHz, f_{SAMPLE} = 65 MSPS

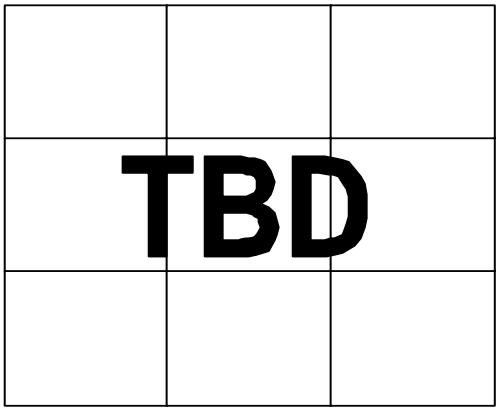


Figure 26. Gain Error vs. Temperature

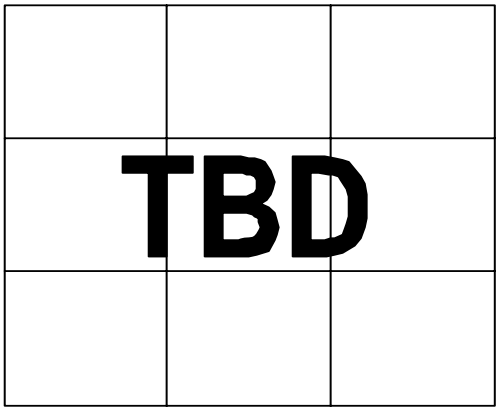


Figure 29. CMRR vs. Frequency, f_{SAMPLE} = 65 MSPS

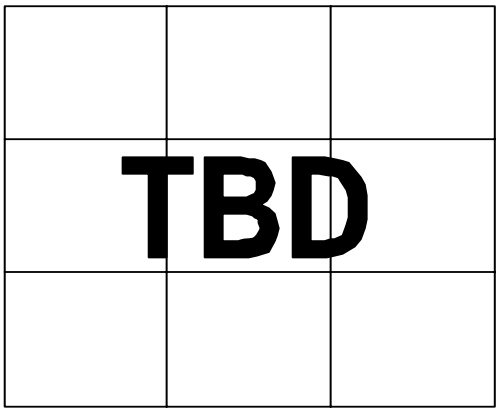


Figure 27. Typical INL, f_{IN} = 2.4 MHz, f_{SAMPLE} = 65 MSPS

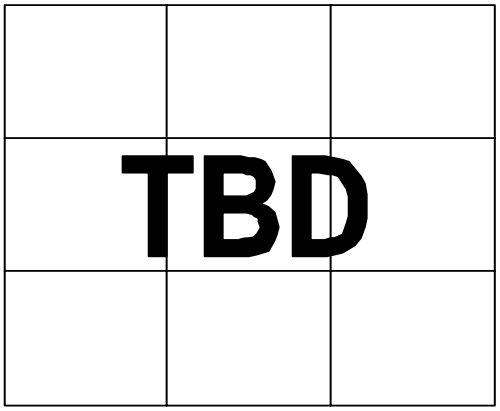


Figure 30. Input Referred Noise Histogram, f_{SAMPLE} = 65 MSPS

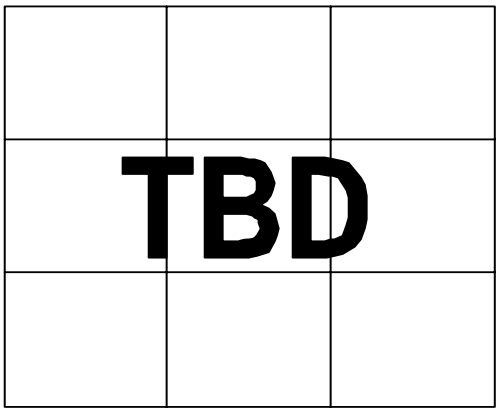


Figure 28. Typical DNL, f_{IN} = 2.4 MHz, f_{SAMPLE} = 65 MSPS

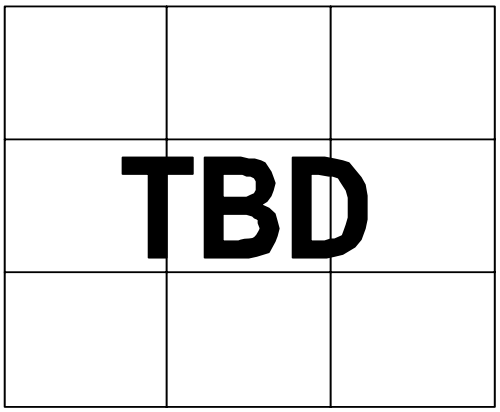


Figure 31. Noise Power Ratio (NPR), f_{SAMPLE} = 65 MSPS

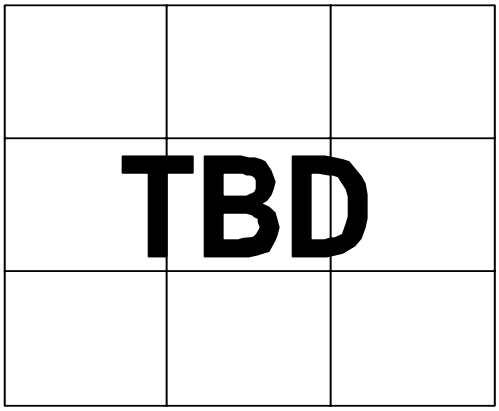


Figure 32. Full Power Bandwidth vs. Frequency, f_{SAMPLE} = 65 MSPS

TERMINOLOGY

Analog Bandwidth
Analog bandwidth is the analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB from full scale.

Aperture Delay
Aperture delay is a measure of the sample-and-hold input circuit performance and is measured from the 50% point rising edge of the clock input to the time at which the input signal is held for conversion.

Aperture Uncertainty (Jitter)
Aperture jitter is the variation in aperture delay for successive samples and can be manifested as frequency-dependent noise on the ADC input.

Clock Pulse Width and Duty Cycle
Pulse width high is the minimum amount of time that the clock pulse should be left in the Logic 1 state to achieve rated performance. Pulse width low is the minimum time the clock pulse should be left in the low state. At a given clock rate, these specifications define an acceptable clock duty cycle.

Common Mode Rejection Ratio (CMRR)
CMRR is defined as the amount of rejection on the differential analog inputs when a common signal is applied. Typically expressed as 20 log (differential gain/common-mode gain).

Crosstalk
Crosstalk is defined as the measure of any feedthrough coupling onto the quiet channel when all other channels are driven by a full-scale signal.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a pin and subtracting the voltage from a second pin that is 180° out of phase.

Differential Nonlinearity (DNL, No Missing Codes)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to an n-bit resolution indicates that all 2^n codes, respectively, must be present over all operating ranges.

Effective Number of Bits (ENOB)
For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula, it is possible to obtain a measure of performance expressed as *N*, the effective number of bits:

$$N = (\text{SINAD} - 1.76)/6.02$$

Full Power Bandwidth
Full power bandwidth is the measured –3 dB point at the analog front end input relative to the frequency measured.

Gain Error
The largest gain error is specified and is considered the difference between the measured and ideal full-scale input voltage range.

Gain Matching
Expressed in %FSR and computed using the following equation:

$$Gain\ Matching = \frac{FSR_{\max} - FSR_{\min}}{\left(\frac{FSR_{\max} + FSR_{\min}}{2}\right)} \times 100\%$$

where FSR_{MAX} is the most positive gain error of the ADCs, and FSR_{MIN} is the most negative gain error of the ADCs.

Input-Referred Noise
Input-referred noise is a measure of the wideband noise generated by the ADC core. Histograms of the output codes are created while a dc signal is applied to the ADC input. Input-referred noise is calculated using the standard deviation of the histograms and presented in terms of LSB rms.

Integral Nonlinearity (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a level 1.5 LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Noise Power Ratio (NPR)
NPR is the full-scale rms noise power injected into the ADC vs. the rejected band of interest (notch depth measured).

Offset Error
The largest offset error is specified and is considered the difference between the measured and ideal voltage at the analog input that produces the midscale code at the outputs.

Offset Matching
Expressed in millivolts and computed using the following equation:

$$Offset\ Matching = OFF_{MAX} - OFF_{MIN}$$

where OFF_{MAX} is the most positive offset error, and OFF_{MIN} is the most negative offset error.

Out-of-Range Recovery Time
Out-of-range recovery time is the time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

Output Propagation Delay
The delay between the clock logic threshold and the time when all bits are within valid logic levels.

Second and Third Harmonic Distortion
The ratio of the rms signal amplitude to the rms value of the second or third harmonic component, reported in decibels relative to the carrier.

Signal-to Noise and Distortion (SINAD) Ratio
SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference in decibels between the rms amplitude of the input signal and the peak spurious signal.

Temperature Drift
The temperature drift for offset error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. It may be reported in decibels relative to the carrier (that is, degrades as signal levels are lowered) or in decibels relative to full scale (always related back to converter full scale).

THEORY OF OPERATION

The AD9219 architecture consists of a pipelined ADC that is divided into three sections: a 4-bit first stage followed by eight 1.5-bit stages and a final 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stages. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The data is then serialized and aligned to the frame and output clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9219 is a differential-switched capacitor circuit that has been designed for optimum performance while processing a differential input signal. The input can support a wide common-mode range and maintain excellent performance. An input common-mode voltage of midsupply minimizes signal-dependent errors and provides optimum performance.

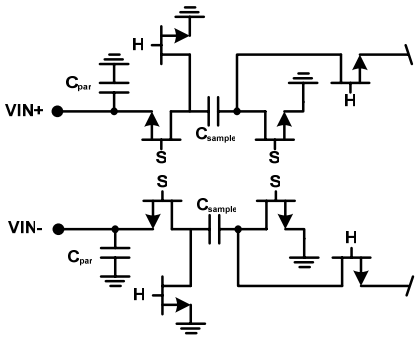


Figure 33. Switched-Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 33). When the input circuit is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. Also, a small shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC's input; therefore, the precise values are dependent on the application.

The analog inputs of the AD9219 are not internally dc-biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that $V_{CM} = AVDD/2$ is recommended for optimum performance, but the device functions over a wider range with reasonable performance (see Figure 34 and Figure 35).

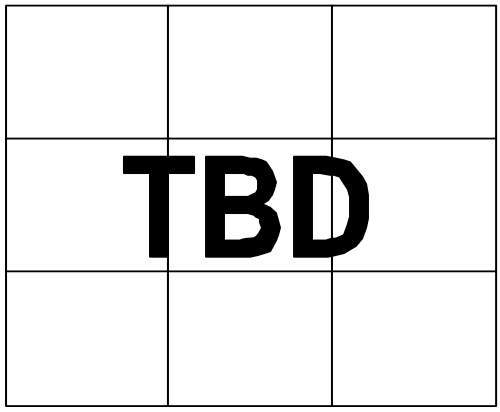


Figure 34. SNR/SFDR vs. Common-Mode Voltage, f_{IN} = 2.4 MHz, f_{SAMPLE} = 65 MSPS

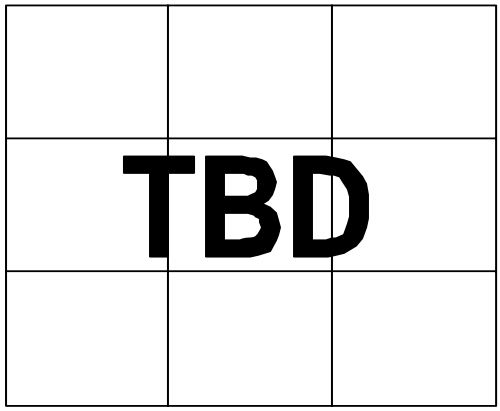


Figure 35. SNR/SFDR vs. Common-Mode Voltage, f_{IN} = 30 MHz, f_{SAMPLE} = 65 MSPS

For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC.

An internal reference buffer creates the positive and negative reference voltages, REFT and REFB, respectively, that defines the span of the ADC core. The output common-mode of the reference buffer is set to midsupply, and the REFT and REFB voltages and span are defined as

$$REFT = 1/2\ (AVDD + VREF)$$
$$REFB = 1/2\ (AVDD - VREF)$$
$$Span = 2 \times (REFT - REFB) = 2 \times VREF$$

It can be seen from the equations above that the REFT and REFB voltages are symmetrical about the midsupply voltage and, by definition, the input span is twice the value of the VREF voltage.

The internal voltage reference is pin-strapped to a fixed value of 1.0 V or adjusted within the same range, as discussed in the Internal Reference Connection section. Maximum SNR performance is achieved by setting the AD9219 to the largest input span of 2 V p-p.

The input circuit should be driven from a source that keeps the signal peaks within the allowable range for the selected reference voltage. The minimum and maximum common-mode input levels are defined in Figure 34 and Figure 35.

Differential Input Configurations

Optimum performance is achieved by driving the AD9219 in a differential input configuration. For ultrasound applications, the AD8332 differential driver provides excellent performance and a flexible interface to the ADC (see Figure 36).

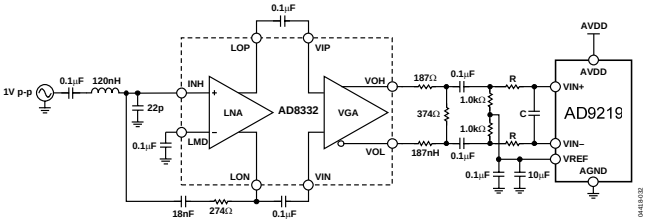


Figure 36. Differential Input Configuration Using the AD8332

However, the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9219. For applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example of this is shown in Figure 37.

In any configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

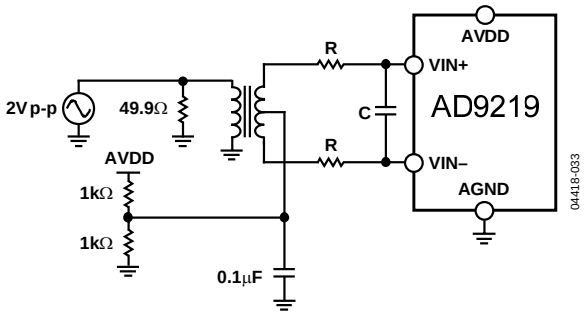


Figure 37. Differential Transformer—Coupled Configuration

Single-Ended Input Configuration

A single-ended input can provide adequate performance in cost-sensitive applications. In this configuration, SFDR and distortion performance degrade due to the large input common-mode swing. However, if the source impedances on each input are matched, there should be little effect on SNR performance. Figure 38 details a typical single-ended input configuration.

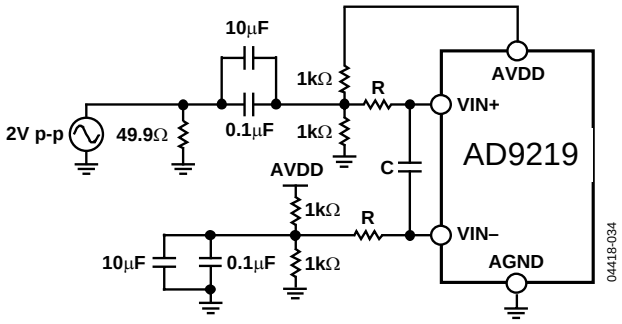


Figure 38. Single-Ended Input Configuration

CLOCK INPUT CONSIDERATIONS

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Typically, a 10% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9219 has a self-contained clock duty cycle stabilizer that retimes the nonsampling edge, providing an inter-nal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9219.

An on-board phase-locked loop (PLL) multiplies the input clock rate for the purpose of shifting the serial data out. The stability criteria for the PLL limits the minimum sample clock rate of the ADC to 10 MSPS. Assuming steady state operation of the input clock, any sudden change in the sampling rate could create an out-of-lock condition leading to invalid outputs at the DCO, FCO, and data out pins.

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_A) due only to aperture jitter (t_A) can be calculated with the following equation:

$$SNR\ degradation = 20 \times \log 10\ [1/2 \times \pi \times f_A \times t_A]$$

In the equation, the rms aperture jitter, t_A, represents the root sum square of all jitter sources, which include the clock input, analog input signal, and ADC aperture jitter specification. Applications that require undersampling are particularly sensitive to jitter.

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9219. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other

methods), it should be retimed by the original clock at the last step.

Power Dissipation and Power-Down Mode

As shown in Figure 39 and Figure 40, the power dissipated by the AD9219 is proportional to its sample rate. The digital power dissipation does not vary much because it is determined primarily by the DRVDD supply and bias current of the LVDS output drivers.

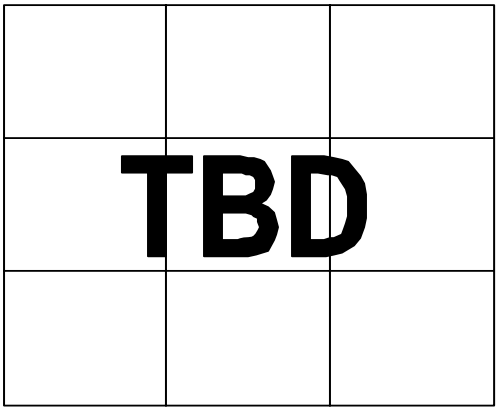


Figure 39. AD9219-50, Supply Current vs. f_{SAMPLE} for f_{IN} = 10.3 MHz

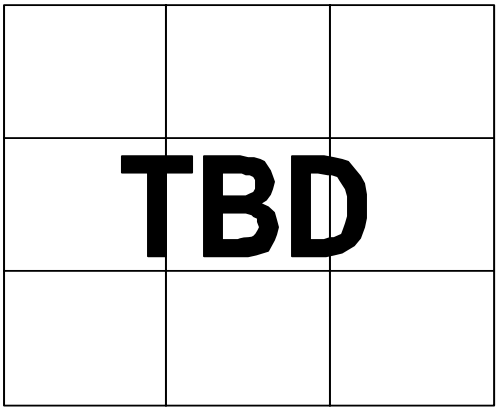


Figure 40. AD9219-65, Supply Current vs. f_{SAMPLE} for f_{IN} = 10.3 MHz

By asserting the PDWN pin high, the AD9219 is placed in power-down mode. In this state, the ADC typically dissipates 3 mW. During power-down, the LVDS output drivers are placed in a high impedance state. Reasserting the PDWN pin low returns the AD9219 to normal operating mode.

In power-down mode, low power dissipation is achieved by shutting down the reference, reference buffer, PLL, and biasing networks. The decoupling capacitors on REFT and REFB are discharged when entering standby mode and then must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in the power-down mode; shorter cycles result in proportionally shorter wake-up times. With the recommended 0.1 µF and 2.2 µF decoupling capacitors on REFT and REFB, it takes approximately 1 sec to fully discharge the reference buffer decoupling capacitors and 1 ms to restore full operation.

Digital Outputs

The AD9219's differential outputs conform to the ANSI-644 LVDS standard on default power up. The LVDS driver current is derived on-chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing at the receiver.

The AD9219's LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs that have LVDS capability for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as close to the receiver as possible. It is recommended to keep the trace length no longer than 12 inches and to keep differential output traces close together and at equal lengths.

The format of the output data is offset binary. An example of the output coding format can be found in Table 7.

Table 7. Digital Output Coding

Code	(VIN+) – (VIN–), Input Span = 2 V p-p (V)	Digital Output Offset Binary (D11 ... D0)
1023	1.000	11 1111 1111
512	0	10 0000 0000
517	–0.001953	01 1111 1111
0	–1.00	00 0000 0000

SDIO/ODM Pin

For applications that do not require SPI mode operation. The serial data input-output/output driver mode (SDIO/ODM) pin can enable a lower power IEEE reduced-range link output standard if this pin is tied to AVDD during device power up. This should only be used when the digital output trace lengths are less than 1inch in length to the LVDS receiver. The FCO, DCO, and outputs still work as usual while all channels LVDS signal swing is reduced from 350mVpp to 200mVpp. This output mode allows the user to further lower the power on the DRVDD supply. For normal operation this pin should be tied to AGND through a 10k resistor.

Table 8. Output Driver Mode Pin Settings

Selected ODM	ODM Voltage	Resulting Output Standard	Resulting FCO and DCO
Normal operation	10kohm to AGND	ANSI-644 (Defualt)	ANSI-644 (Defualt)
ODM	AVDD	IEEE 1596.3	IEEE 1596.3

Timing

Data from each ADC is serialized and provided on a separate channel. The data rate for each serial stream is equal to 12 bits times the sample clock rate, with a maximum of 780 bps (12 bits × 65 MSPS = 780 bps). The lowest typical conversion rate is 10 MSPS.

Two output clocks are provided to assist in capturing data from the AD9219. The DCO is used to clock the output data and is equal to six times the sampling clock (CLK) rate. Data is clocked out of the AD9219 and can be captured on the rising and falling edges of the DCO that supports double-data rate (DDR) capturing. The frame clock out (FCO) is used to signal the start of a new output byte and is equal to the sampling clock rate. See the timing diagram shown in Figure 2 for more information.

SCLK/DTP Pin

For applications that do not require SPI mode operation. The serial clock/digital test pattern (SCLK/DTP) pin can enable a single digital test pattern if this pin is held high during device power up. When the DTP is tied to AVDD, all the ADC channel outputs shift out the following pattern: 10 0000 0000. The FCO and DCO outputs still work as usual while all channels shift out the repeatable test pattern. This pattern allows the user to perform timing alignment adjustments between the FCO, DCO, and the output data. For normal operation this pin should be tied to AGND through a 10k resistor.

Table 7. Digital Test Pattern Pin Settings

Selected DTP	DTP Voltage	Resulting D+ and D–	Resulting FCO and DCO
Normal operation	10kohm to AGND	Normal operation	Normal operation
DTP	AVDD	10 0000 0000	Normal operation

RBIAS

To set the internal core bias current of the ADC, place a resistor (nominally equal to 10.0 kΩ) to ground at the RBIAS pin. The resistor current is derived on-chip and sets the ADC core current (excluding the LVDS driver supply) to a nominal 418mW. If SFDR performance is not as critical as power simply adjust the ADC core current to achieve a lower power. Table 10 shows a couple of different values that could be used in exchange for less dynamic range.

Table 10. RBIAS Pin Configuration

RBIAS	Internal Core Power (65/40MSPS)
TBD	xxx mW
10.0 kΩ (Default)	450 mW/450 mW
TBD	xxx mW

Voltage Reference

A stable and accurate 0.5 V voltage reference is built into the AD9219. The input range can be adjusted by varying the reference voltage applied to the AD9219, using either the internal reference or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly.

When applying the decoupling capacitors to the VREF, REFT, and REFB pins, use ceramic, low ESR capacitors. These capacitors should be close to the ADC pins and on the same layer of the PCB as the AD9219. The recommended capacitor values and configurations for the AD9219 reference pin can be found in Figure 41 and Figure 42.

Table 11. Reference Settings

Selected Mode	SENSE Voltage	Resulting VREF (V)	Resulting Differential Span (V p-p)
External Reference	AVDD	N/A	2 × external reference
Programmable	0.2 V to VREF	0.5 × (1 + R2/R1)	2 × VREF
Internal, 2 V p-p FSR	AGND to 0.2 V	1.0	2.0

Internal Reference Connection

A comparator within the AD9219 detects the potential at the SENSE pin and configures the reference into four possible states (summarized in Table 1). If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 41), setting VREF to 1 V. If an external resistor divider is connected as shown in Figure 42, the switch is again set to the SENSE pin. This puts the reference amplifier in a noninverting mode and defines the VREF output as

$$VREF = 0.5 \times \left(1 + \frac{R2}{R1}\right)$$

In all reference configurations, REFT and REFB establish their input span of the ADC core. The analog input full-scale range of the ADC equals twice the voltage at the reference pin for either an internal or an external reference configuration.

If the internal reference of the AD9219 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 43 depicts how the internal reference voltage is affected by loading.

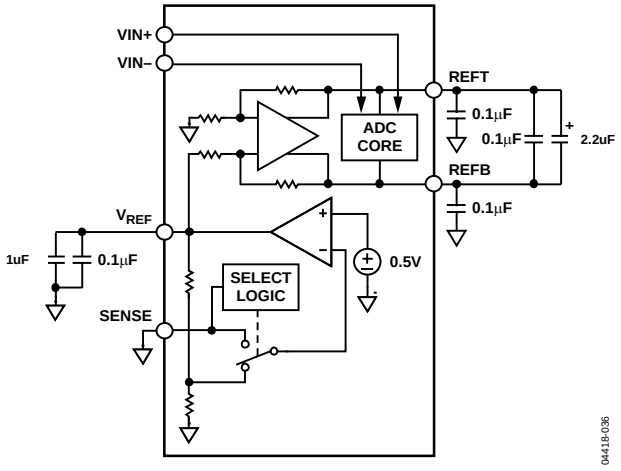


Figure 41. Internal Reference Configuration

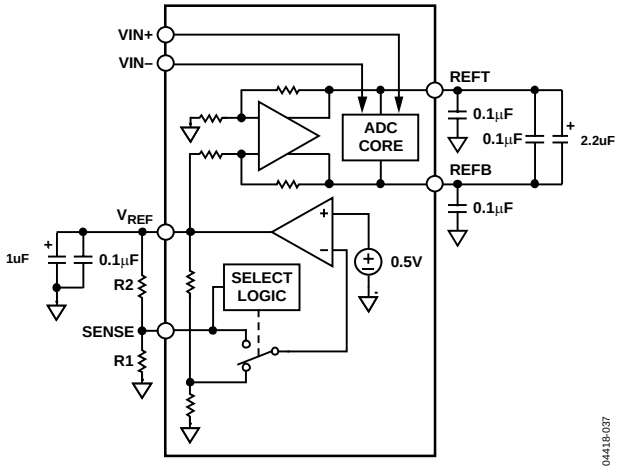


Figure 42. Programmable Reference Configuration

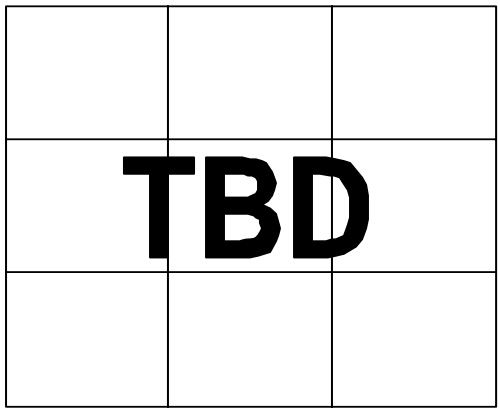


Figure 43. VREF Accuracy vs. Load

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 44 shows the typical drift characteristics of the internal reference.

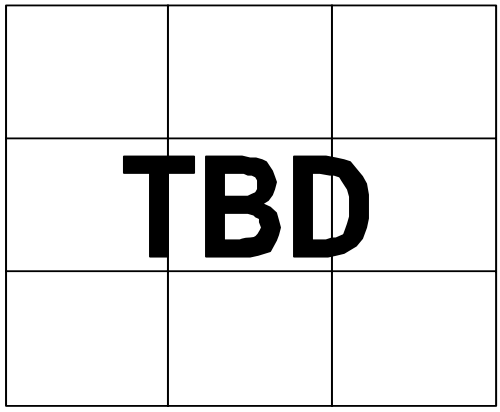


Figure 44. Typical VREF Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. The external reference is loaded with an equivalent 7 kΩ load. An internal reference buffer generates the positive and negative full-scale references, REFT, and REFB for the ADC core. Therefore, the external reference must be limited to a maximum of 1 V.

SERIAL PORT INTERFACE (SPI)

The AD9219 serial port interface allows the user to configure the converter for specific functions or operations througha structured register space is provided inside the ADC. This gives the user added flexibility and customization depending on the application. Addresses are accessed (programmed or readback) serially in one-byte words. Each byte may be further divided down into fields which are documented in the Memory Map Section.

There are three pins that define the serial port interface or SPI to this particular ADC. They are the SCLK, SDIO, and CSB pins. The SCLK (serial clock) is used to synchronize the read and write data presented the ADC. The SDIO (serial data input/output) is a dual purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB or chip select bar is an active low control that enables or disables the read and write cycles. See Table 12.

Table 12. Serial Port Pins

Pin	Function
SCLK	SCLK (Serial Clock) is the serial shift clock in. SCLK is used to synchronize serial interface reads and writes.
SDIO	SDIO (Serial Data Input/Output) is a dual purpose pin. The typical role for this pin is an input and output depending on the instruction being sent and the relative position in the timing frame.
CSB	CSB (Chip Select Bar) is active low controls that gates the read and write cycles.

The falling edge of the CSB in conjunction with the rising edge of the SCLK determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 46 and Table 13 .

During an instruction phase a 16bit instruction is transmitted followed by one or more data bytes which are determined by the bit fields W0 and W1.

In addition to word length, the instruction phase also determines if the serial frame is a read or write operation, allowing the serial port to be used both to program the chip as well as read the contents of on chip memory. If the instruction is a Readback operation, performing a Readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

Data may be sent in MSB or in LSB first mode. MSB first is default on power up and may be changed by changing the configuration register. For more information about this feature and others see SPI Doc at www.analog.com.

HARDWARE INTERFACE

The pins described in Table 12 comprise the physical interface between the user's programming device and the serial port of the AD9228. The SCLK and CSB pins function as inputs when using the SPI interface. The SDIO pin is bidirectional functioning as an input during write phases and as an output during Readback

This interface is flexible enough to be controlled by either PROMS or PIC mirocontrollers as well. This provides the user an alternate alternate method to program the ADC other than a full SPI controller.

If the user chooses not to use the SPI interface these pins serve a dual function and are associated with secondary functions when the CSB is strapped to AVDD during device power up. See Theory of operation section to see what pin strappable functions are supported on the SPI pins.

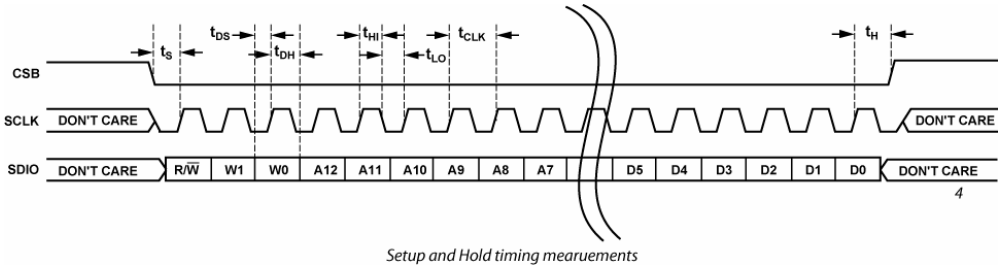


Figure 4645. Serial Timing Details

Table 13. Serial Timing Definitions

Spec Name	Meaning
t_{DS}	Setup time between data and rising edge of SCLK
t_{DH}	Hold time between data and rising edge of SCLK
t_{CLK}	Period of the clock
t_S	Setup time between CSB and SCLK
t_H	Hold time between CSB and SCLK
t_{HI}	Minimum period that SCLK should be in a logic high state
t_{LO}	Minimum period that SCLK should be in a logic low state

MEMORY MAP

READING THE MEMORY MAP TABLE

Each row in the memory map table has eight address locations. The memory map is roughly divided into four sections: chip configuration register map (Address 0x00 to Address 0x02), device index and transfer register map (Address 0x04 to Address 0x05, and Address 0xFF), global ADC function register map (Address 0x08 to Address 0x09), and flexible ADC functions register map (Address 0x0B to Address 0x25). The flexible ADC functions register map is product specific.

Starting from the right hand column the memory map register in

14 the default hex value for the giving hex address is shown. The column with the heading Byte 7 (MSB) is the start of the default hex value giving. For example, hex address 0x14, flex_output_phase has a hex default value of 00h. This means Bit 3 = 0, Bit 2 = 0, Bit 1 = 1, and Bit 0 = 1 or 0011 in binary. This setting is the default output clock or DCO phase adjust option. The default value adjusts the DCO phase 90deg relative to the Nominal DCO edge and 180deg relative to the data edge. For more information on this function and others consult the SPI Doc at www.analog.com.

OPEN LOCATIONS

Undefined memory locations should not be written to unless the value written corresponds to the default power up values. Addresses which have values marked as "open" should be written with zeros in the fields marked as open.

DEFAULT VALUES

Coming out of reset, critical registers are pre-loaded with default values. These values are indicated in Table 14 below. Other registers do not have default values and retain the previous value when exiting reset.

LOGIC LEVELS

An explanation of various registers, "bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit." Similarly "clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Table 14. Memory Map Register

Addr (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Def. Value (Hex)	Default Notes and comments
Chip Configuration Registers											
00	chip_port_config	OPEN	LSB First	Soft Reset	Bit set	Bit set	Soft Reset	LSB First	OPEN	18h	The nibbles should be mirrored by the user so that LSB or MSB first mode will register correctly regardless of shift mode.
01	chip_id	8-bit Chip ID bits 7:0 AD9219 = 0x02								Read only	Default is unique chip ID, different for each device. This is a read only register. See data sheet for more details.
02	chip_grade	OPEN	Child ID 6:4 (identify device variants of Chip ID) 000 = 65MSPS 001 = 40MSPS			OPEN				Read only	Read only. Child ID used to differentiate graded devices. See data sheet for more details
Device Index and Transfer Registers											
05	device_index_A	OPEN	OPEN	Clock Channel DCO	Clock Channel FCO	Data Channel D	Data Channel C	Data Channel B	Data Channel A	0Fh	Bits are set to determine which device on chip receives the next write command. The default will be all devices on chip.
FF	device_update	OPEN							SW Transfer	00h	Synchronously transfers data from the master shift register to the slave
Global ADC Functions											
08	global_modes	OPEN	OPEN		OPEN	OPEN	Internal Power Down Mode 0 – chip run 1 – full power down 2 – standby 3 – reset			00h	Determines various generic modes of chip operation.

Addr (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Def. Value (Hex)	Default Notes and comments
09	global_clock	OPEN	OPEN	OPEN	OPEN				Duty Cycle Stabilize	01h	
Flexible ADC Functions (may or may not be specified by device_index – product specific)											
0D	flex_test_io	User Test Mode 00h single 01h alternate 10h single once 11h alternate once		Reset PN Long Gen	Reset PN Short Gen	Flex Output test mode 0 – off 1 – midscale short 2 - +FS short 3 - -FS short 4 – checker board output 5 – PN 23 sequence 6 – PN 9 7 – one/zero word toggle 8 – user input 9 – one/zero bit toggle 10 – 1x Sync 11 – one bit high 12 – Mixed bit frequency (format determined by flex_output_mode)				00h	When set, the test data is placed on the output pins in place of normal data
0F	flex_adc_input	0 – BW A 1 – BW B 2 – BW C 3 – BW D (default)					OPEN	OPEN	OPEN	60h	
14	flex_output_mode	OPEN	0 – LVDS ANSI 1 – LVDS IEEE	OPEN	OPEN	OPEN	Output Invert	0 – offset binary 1 - 2's complement		00h	Configures the outputs and the format of the data.
15	flex_output_adjust	OPEN		Output Driver Termination 5:4 00 = None 1 = 200ohm 2 = 100ohm 3 = 100ohm		OPEN				00h	Determines LVDS or other output properties. Primarily functions to set the LVDS span and common mode levels in place of an external resistor.
16	flex_output_phase	OPEN	OPEN	OPEN	OPEN	Output Clock phase adjust 3:0 (0000 through 1010)				03h	On devices that utilize global clock divide, determines which phase of the divider output is used to supply the output clock. Internal latching is unaffected.

Addr (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Def. Value (Hex)	Default Notes and comments
19	flex_user_patt1_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h	User Defined Pattern 1 LSB
1A	flex_user_patt1_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h	User Defined Pattern 1 MSB
1B	flex_user_patt2_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h	User Defined Pattern 2 LSB
1C	flex_user_patt2_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h	User Defined Pattern 2 MSB
21	flex_serial_control	LSB first				OPEN	000 – normal bit stream 010 – 10 bits 011 – 12 bits			00h	Serial stream control. Default causes MSB first and the native bit stream. (global)
22	flex_serial_ch_stat							ch output reset	ch power down	00h	Used to power down individual sections of a converter. (local)

Power and Ground Recommendations

When connecting power to the AD9219, it is recommended that two separate 3.0 V supplies be used: one for analog (AVDD) and one for digital (DRVDD). If only one supply is available, then it should be routed to the AVDD first and tapped off and isolated with a ferrite bead or filter choke with decoupling capacitors proceeding. The user can employ several different decoupling capacitors to cover both high and low frequencies. These should be located close to the point of entry at the PC board level and close to the parts with minimal trace length.

A single PC board ground plane should be sufficient when using the AD9219. With proper decoupling and smart partitioning of the PC board's analog, digital, and clock sections, optimum performance is easily achieved.

Exposed Paddle Thermal Heat Slug Recommendations

It is mandatory that the exposed paddle on the underside of the ADC is connected to analog ground (AGND) to achieve the best electrical and thermal performance of the AD9219. A continuous exposed (no solder mask) copper plane on the PCB should mate to the AD9219 exposed paddle, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be filled or plugged with nonconductive epoxy.

To maximize the coverage and adhesion between the ADC and PCB, overlay a silkscreen to partition the continuous plane on the PCB into several uniform sections. This provides several tie points between the two during the reflow process. Using one continuous plane with no partitions only guarantees one tie point between the ADC and PCB. See Figure 47 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, go to www.analog.com.

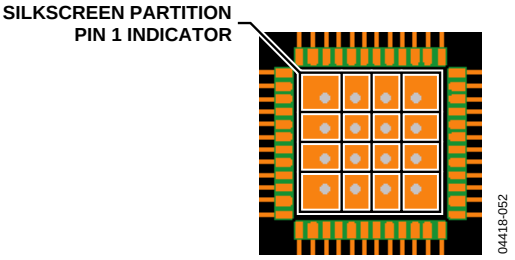


Figure 47. Typical PCB Layout

EVALUATION BOARD

The AD9219 evaluation board provides all of the support circuitry required to operate the ADC in its various modes and configurations. The converter can be driven differentially through a transformer (default) or through the AD8332 driver. The ADC can also be driven single-ended. Separate power pins are provided to isolate the DUT from the AD8332 drive circuitry. Each input configuration can be selected by proper connection of various jumpers (see Figure 479 to Figure 503). Figure 48468 shows the typical bench characterization setup used to evaluate the ac performance of the AD9219. It is critical that the signal sources used for the analog input and clock have very low phase noise (<1 ps rms jitter) to realize the ultimate performance of the converter. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is also necessary to achieve the specified noise performance.

See Figure 48469 to Figure 543 for complete schematics and layout plots that demonstrate the routing and grounding techniques that should be applied at the system level.

POWER SUPPLIES

This evaluation board comes with a wall mount switching power supply that provides a 6 V, 2 A maximum output. Simply connect the supply to the rated 100 to 240 ac wall outlet at 47 Hz to 63 Hz. The other end is a 2.1 mm inner diameter jack that connects to the PCB at P503. Once on the PC board, the 6 V supply is fused and conditioned before connecting to three low dropout linear regulators that supply the proper bias to each of the various sections on the board.

When operating the evaluation board in a nondefault condition, L504 to L507 can be removed to disconnect the switching power supply. This enables the user to individually bias each section of the board. Use P501 to connect a different supply for each section. At least one 1.8 V supply is needed with a 1 A current capability for AVDD_DUT and DRVDD_DUT; however, it is recommended that separate supplies be used for both analog and digital. To operate the evaluation board using the VGA option, a separate 5.0 V analog supply is needed. The 5.0 V supply, or AVDD_5V, should have a 1 A current capability. To operate the evaluation board using the SPI options, a separate 3.3 V analog supply is needed in addition to the other supplies. The 3.3 V supply, or AVDD_3.3V, should have a 1 A current capability as well.

INPUT SIGNALS

When connecting the clock and analog source, use clean signal generators with low phase noise, such as Rohde & Schwarz SMHU or HP8644 signal generators or the equivalent. Use 1 m long, shielded, RG-58, 50 Ω coaxial cable for making connections to the evaluation board. Dial in the desired frequency and amplitude within the ADC's specifications tables. Typically, most ADI evaluation boards can accept a ~2.8 V p-p or 13 dBm sine wave input for the clock. When connecting the analog input source, it is recommended to use a multipole, narrow-band band-pass filter with 50 Ω terminations. ADI uses TTE, Allen Avionics, and K&L type band-pass filters. The filter should be connected directly to the evaluation board if possible.

OUTPUT SIGNALS

The default setup uses the HSC-ADC-FPGA high speed deserialization board, which deserializes the digital output data and converts it to parallel CMOS. These two channels interface directly with ADI's standard dual channel FIFO data capture board (HSC-ADC-EVALA-DC). Two of the four channels can then be evaluated at the same time. For more information on channel settings on these boards and their optional settings, visit www.analog.com/FIFO.

NOTE: Evaluation boards are only intended for device evaluation and not for production purposes. Evaluation boards as supplied "as is" and without warranties of any kind, express, implied, or statutory including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose. No license is granted by implication or otherwise under any patents or other intellectual property by application or use of evaluation boards. Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Analog Devices reserves the right to change devices or specifications at any time without notice. Trademarks and registered trademarks are the property of their respective owners. Evaluation boards are not authorized to be used in life support devices or systems.

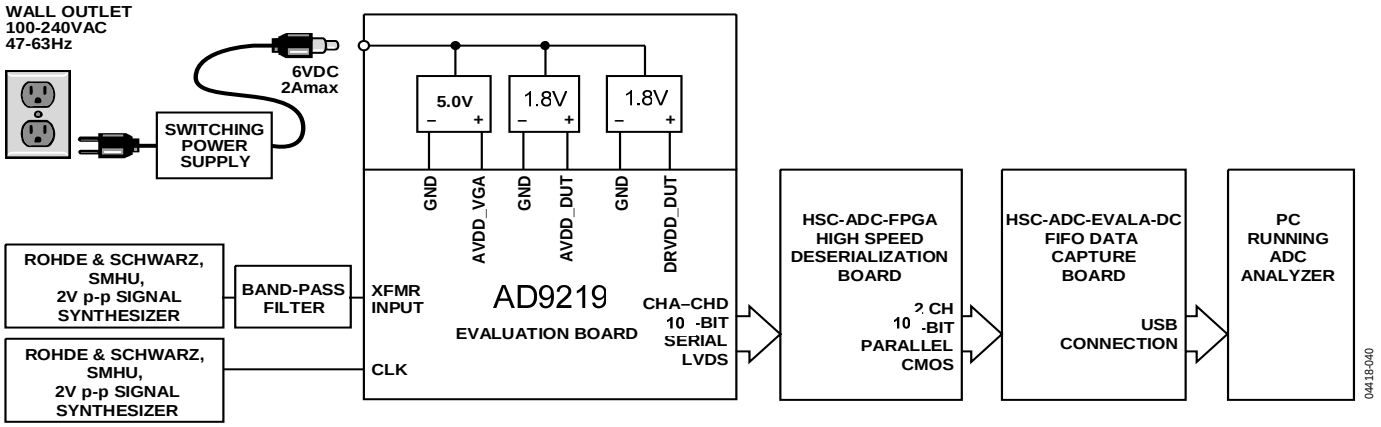


Figure 4846. Evaluation Board Connection

DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

The following is a list of the default and optional settings or modes allowed on the AD9219 Rev A evaluation board.

- POWER: Connect the switching power supply that is supplied in the evaluation kit between a rated 100-240AC wall outlet at 47 Hz to 63 Hz and P503.
- AIN: The evaluation board is set up for a transformer coupled analog input with optimum 50 Ω impedance matching out to 400 MHz. For more bandwidth response, the differential capacitor across the analog inputs could be changed or removed. The common mode of the analog inputs is developed from the center tap of the transformer or AVDD_DUT/2.
- VREF: VREF is set to 1.0 V by tying the SENSE pin to ground, R237. This causes the ADC to operate in 2.0 V p-p full-scale range. A number of other VREF options are available on the evaluation board, including a variable range which the user can set by choosing R232 and R233 as well as a separate external reference option using the ADR510 or ADR520. Simply populate R231 and R235 and remove C214. To use these optional VREF modes, switch the jumper setting on R234 to R237. Proper use of the VREF options is noted in the Voltage Reference section.
- RBIAS: RBIAS is has a default setting of 10kohm to ground to set the ADC core bias current. To further lower the core power (excluding the LVDS driver supply) simply change the resistor setting. However, performance of the ADC will degrade depending on the resistor chosen. See RBIAS section for more information.
- CLOCK: The default clock input circuitry is derived from a simple transformer coupled circuit using a high bandwidth 1:1 impedance ratio transformer that adds a very low amount of jitter to the clock path. The clock input is 50 Ω terminated and ac-coupled to handle a single-ended sine wave type inputs. The transformer converts the singled-ended input to a differential signal that is clipped before entering the ADC clock inputs.

  A differential LVPECL clock can also be used to clock the ADC input using the AD9515. Simply populate R225 and R227 with 0ohm resistors and remove R217 and R218 to disconnect the default clock path inputs. C207 and C208 will also need to be populated with a 0.1uF capacitor and remove C210 and C211 to disconnect the default cloth path outputs. The AD9515 has many pin strappable options that are set to a default working condition. Consult the AD9515 datasheet at www.analog.com for more information about these options and more.

  If using an oscillator, two oscillator footprint options are also available (OSC201) to check the ADC's performance. J205 give the user flexibility in using the enable pin, which is common on most oscillators.
- PDWN: To enable the power-down feature, simply short J201 to AVDD on the PDWN pin.
- DTP: To enable one of the two digital test patterns on digital outputs of the ADC, use J204. If J204 is tied to AVDD during device power up this enables test pattern 10 0000 0000. See the SCLK/DTP Pin section for more details.
- ODM: To enable the IEEE reduced range link LVDS output standard, use J203. If J203 is tied to AVDD during device power up this enables the IEEE LVDS output standard from the default ANSI standard. This option will change the signal swing from 350mVpp to 200mVpp which will reduce the power of the DRVDD supply. See the SCLK/DTP Pin section for more details.
- CSB: To enable the SPI information on the SDIO and SCLK pins to be processed simply tie J202 low in the always enable mode. To ignore the SDIO and SCLK information tie J202 to AVDD.
- RBIAS: To change core current the level of the all ADC channels, simply change the value of R201. Other recommended values can be found in the RBIAS section.
- D+, D–: If an alternate data capture method to the setup described in Figure 48468 is used, optional receiver terminations, R205 to R210, can be installed next to the high speed backplane connector.

ALTERNATE ANALOG INPUT DRIVE CONFIGURATION

The following is a brief description of the alternate analog input drive configuration using the AD8332 dual VGA. This particular drive option may need to be populated, in which case all the necessary components are listed in Table 5. This table lists the necessary settings to properly configure the evaluation board for this option. For more details on the AD8332 dual VGA, how it works, and its optional pin settings, consult the AD8332 data sheet.

To configure the analog input to drive the VGA instead of the default transformer option, the following components need to be removed and/or changed.

1. Remove R102, R115, R128, R141, T101, T102, T103, and T104 in the default analog input path.
2. Populate R101, R114, R127, and R140 with 0 Ω resistors in the analog input path.

3. Populate R106, R107, R119, R120, R132, R133, R144, and R145 with 10 kΩ resistors to provide an input common-mode level to the analog input.
4. Populate R105, R113, R118, R124, R131, R137, R151, and R160 with 0 Ω resistors in the analog input path.
5. Currently L301 to L308 and L401 to L408 are populated with 0 Ω resistors to allow signal connection. This area allows the user to design a filter if additional requirements are necessary.

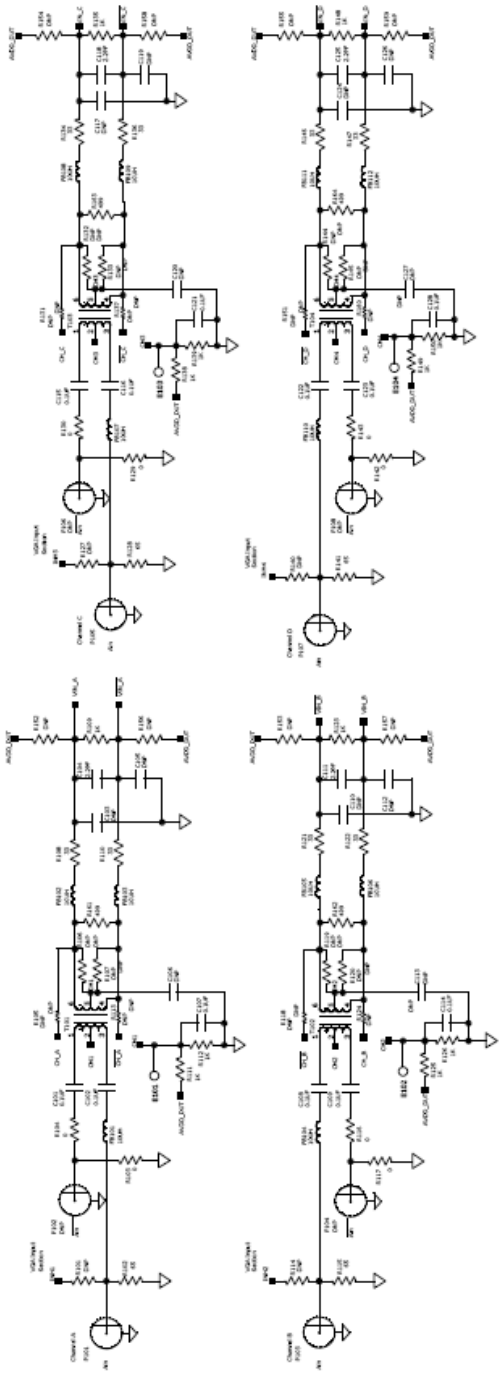


Figure 479. Evaluation Board Schematic, DUT Analog Inputs

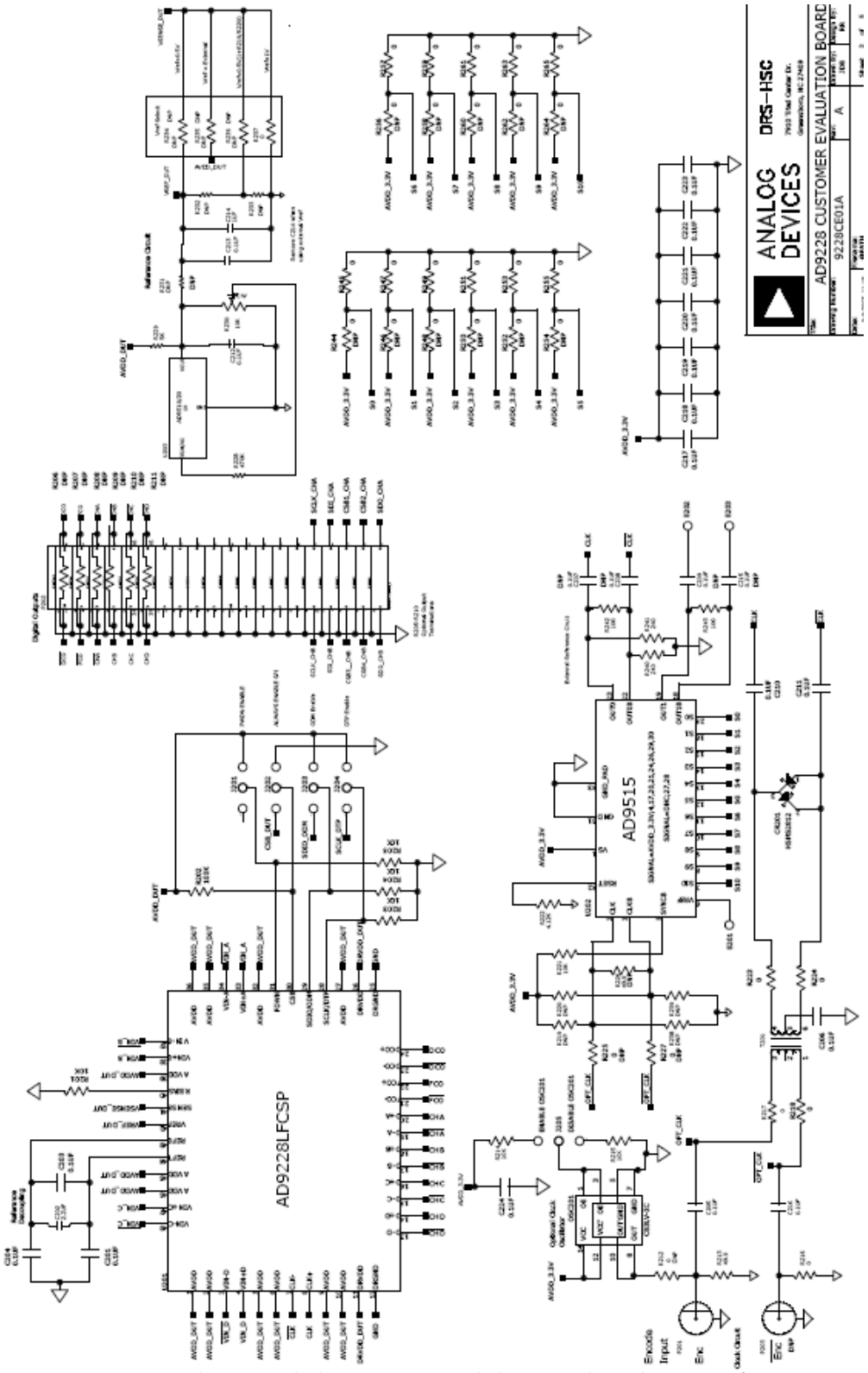


Figure 50. Evaluation Board Schematic, DUT, VREF, Clock Inputs, and Digital Output Interface

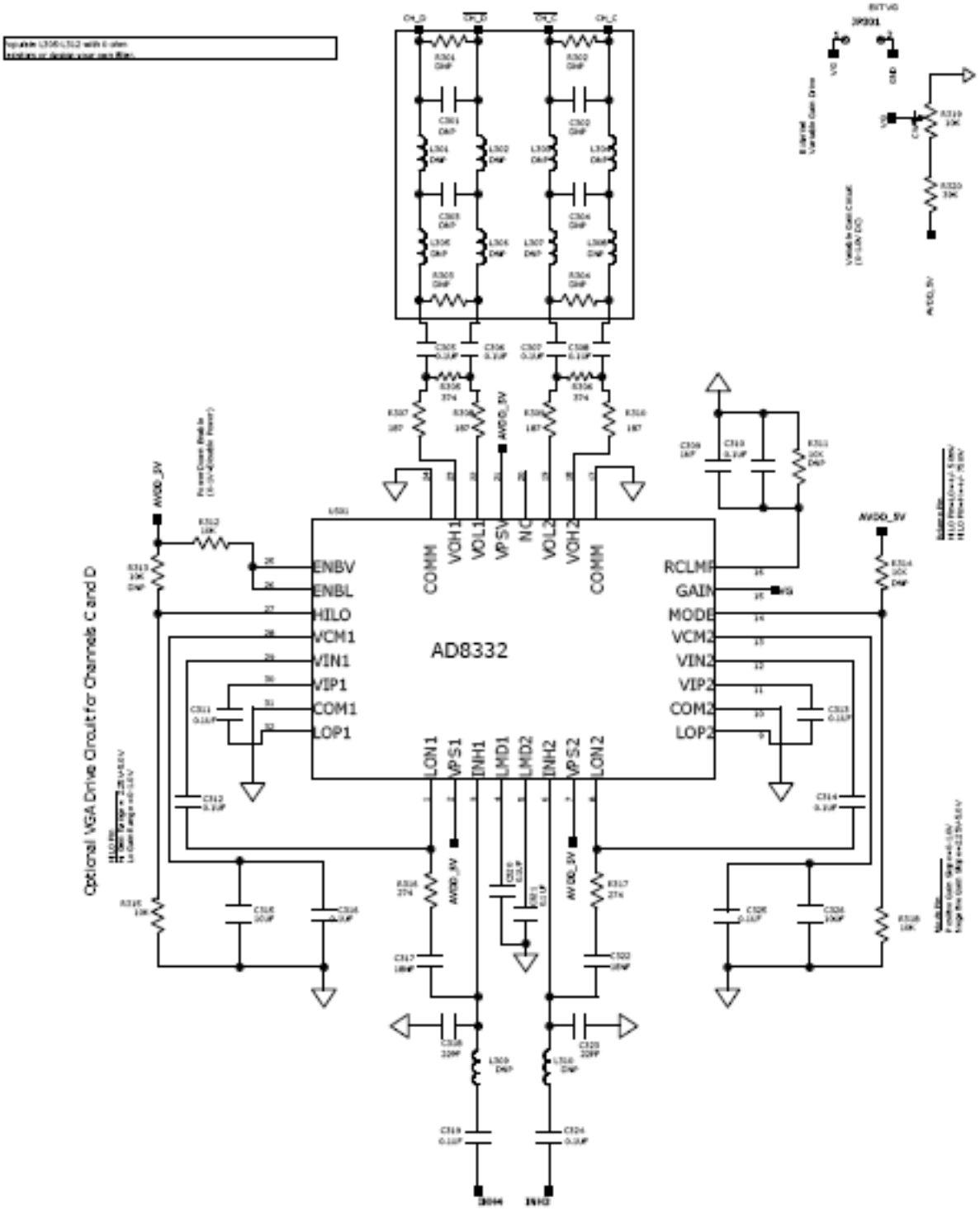


Figure 481. Evaluation Board Schematic, Optional DUT Analog Input Drive

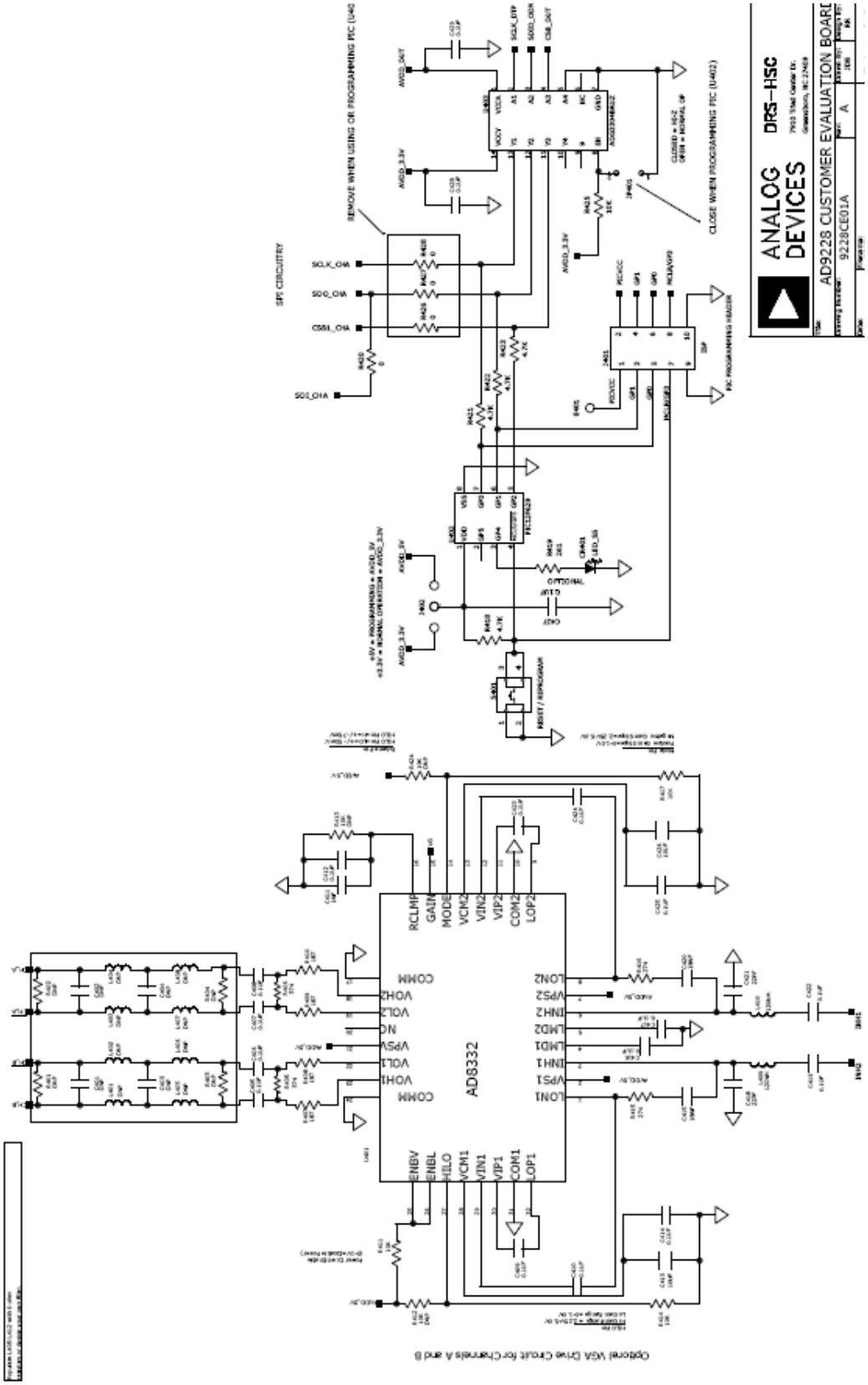


Figure 5249. Evaluation Board Schematic, Optional DUT Analog Input Drive Continued

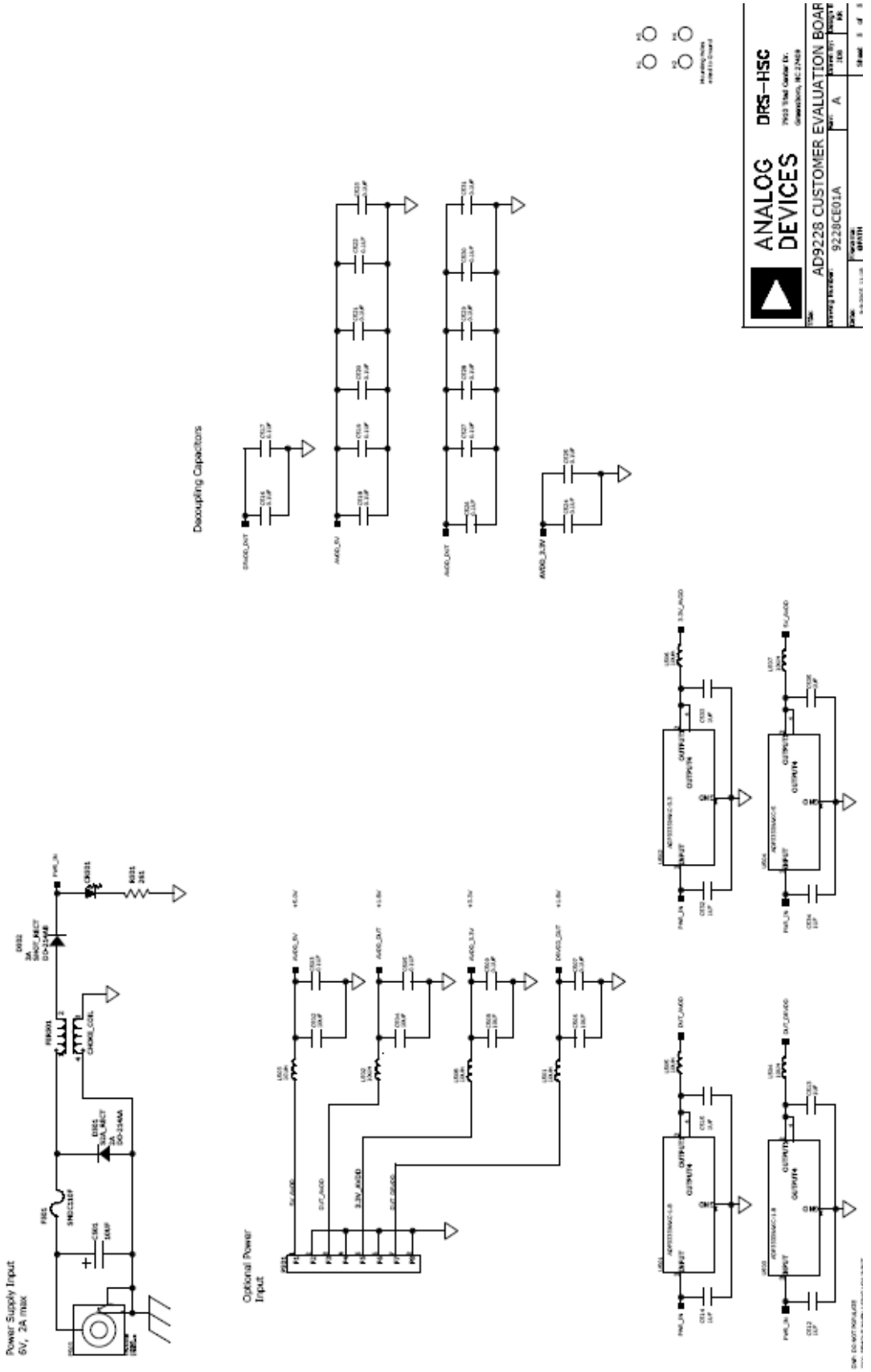


Figure 503. Evaluation Board Schematic, Power Supply Inputs

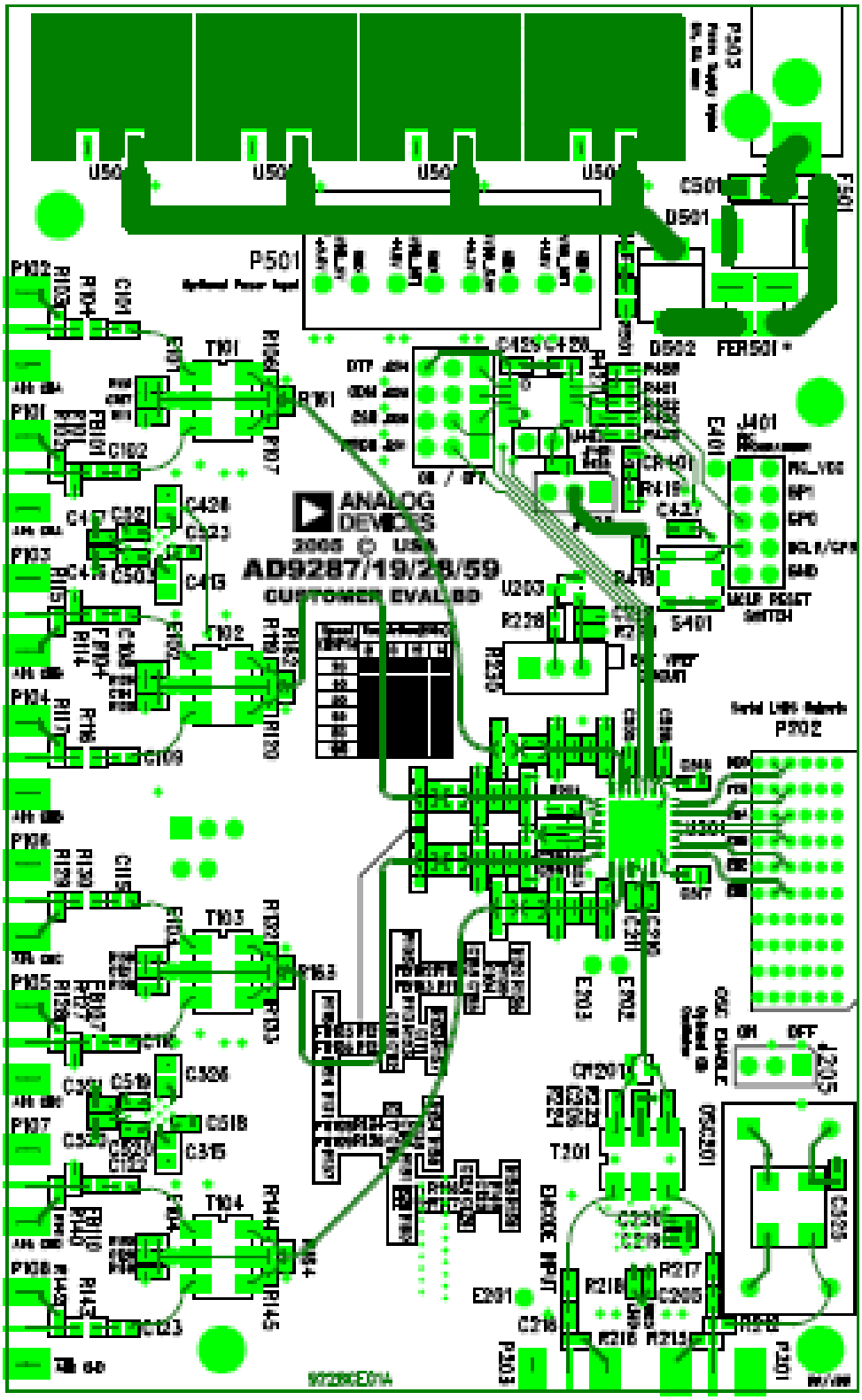


Figure 51. Evaluation Board Layout, Primary Side

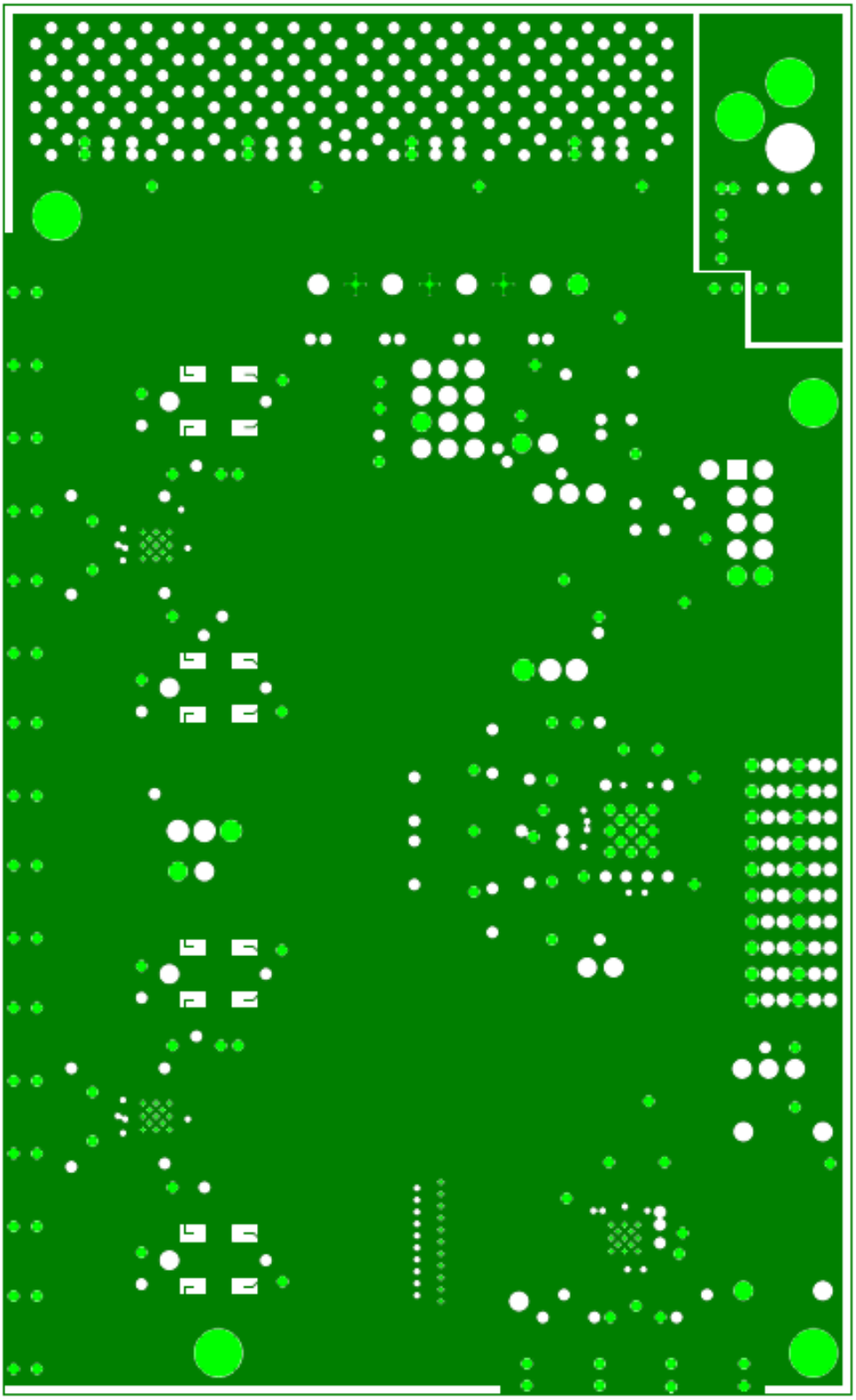


Figure 52. Evaluation Board Layout, Ground Plane

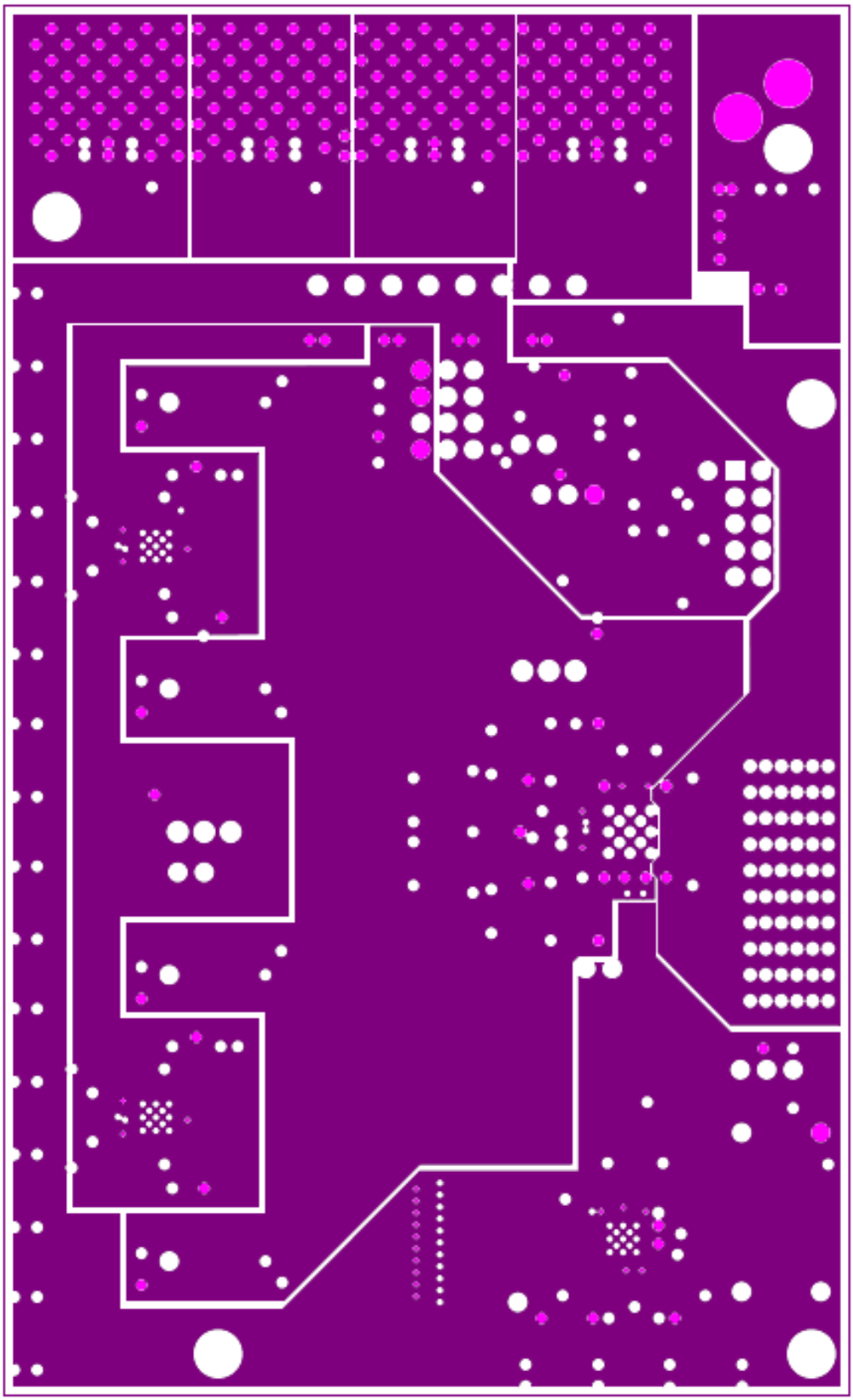


Figure 53. Evaluation Board Layout, Power Plane

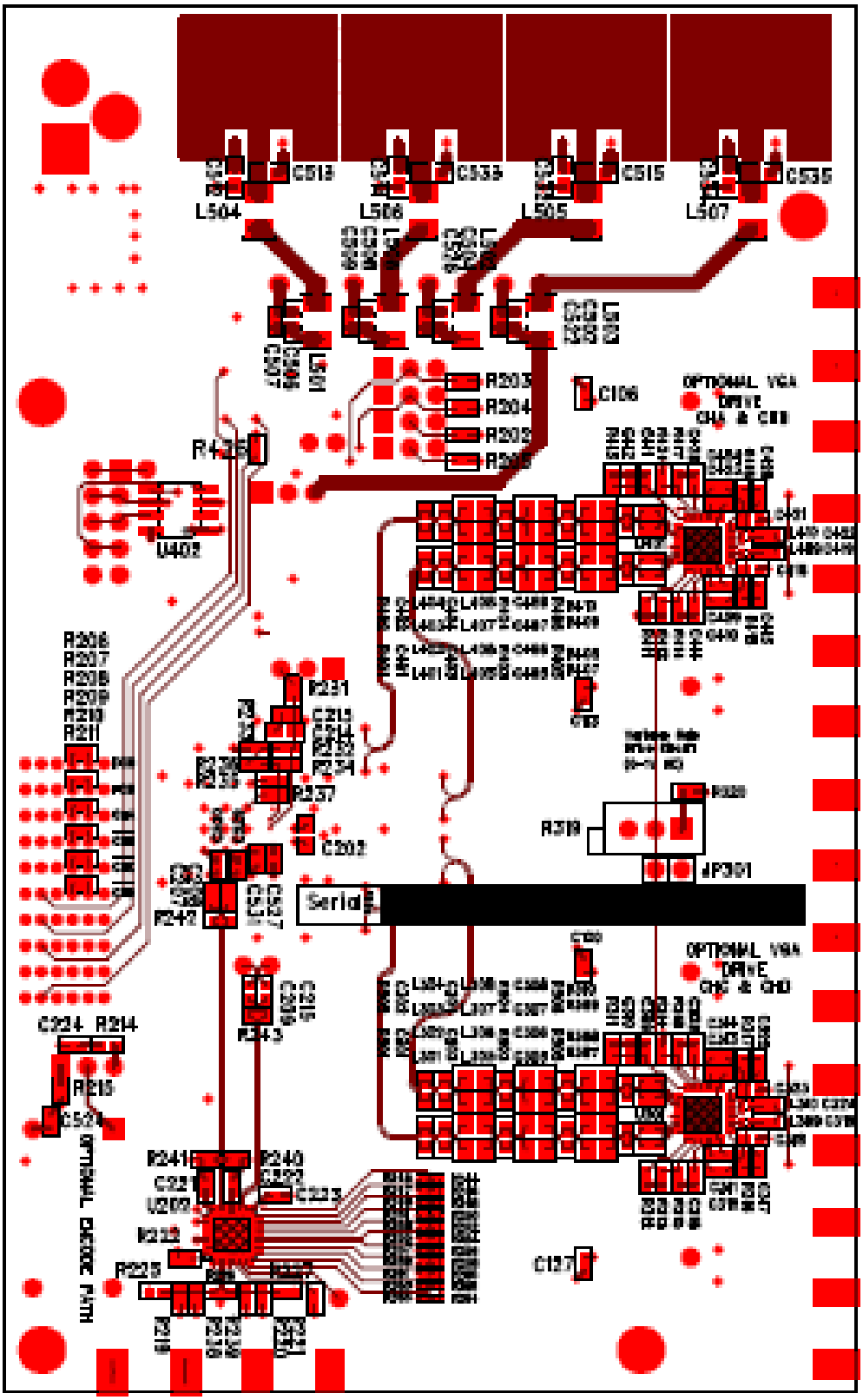


Figure 54. Evaluation Board Layout, Secondary Side (Mirrored Image)

Table 15. Evaluation Board Bill of Materials (BOM)

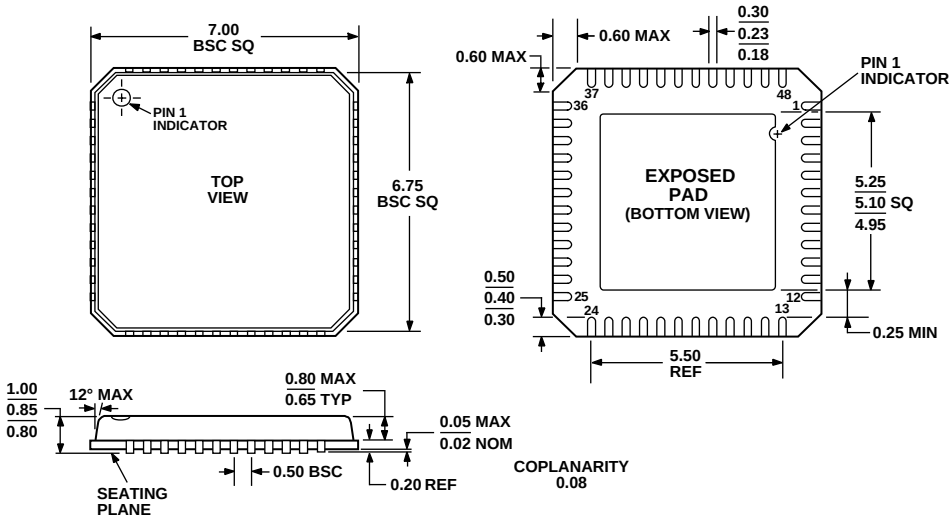
Item	Qnty. per Board	REFDES	Device	Pkg.	Value	Mfg.	Mfg. Part Number
1	1	AD9219LFCSP_REVA	PCB	PCB	PCB		
2	67	C101,C102,C107,C108,C109,C114,C115,C116,C121,C122,C123,C128,C201,C203,C204,C205,C206,C210,C211,C212,C213,C216,C310,C311,C312,C313,C314,C316,C319,C320,C321,C324,C325,C409,C410,C412,C414,C416,C417,C419,C422,C423,C424,C425,C427,C428,C429,C503,C505,C507,C509,C516,C517,C518,C519,C520,C521,C522,C523,C524,C525,C526,C527,C528,C529,C530,C531	Capacitor	402	0.1 µF, ceramic, X5R, 10 V, 10% tol	Panasonic	ECJ-0EB1A104K
3	4	C104, C111, C118, C125	Capacitor	402	2.2 pF, ceramic, COG, 0.25 pF tol, 50 V	Murata	GRM1555C1H2R2GZ01B
4	4	C315,C326,C413,C426	Capacitor	805	10 µF, 6.3 V ±10% ceramic X5R	AVX	08056D106KAT2A
5	1	C202	Capacitor	603	2.2 µF, ceramic, X7R, 16 V, 10% tol	Kemet	
6	2	C309, C411	Capacitor	402	1000 pF, ceramic, X7R, 25 V, 10% tol	Kemet	C0402C102K3RACTU
7	4	C317,C322,C415,C420	Capacitor	402	0.018 µF, ceramic, X7R, 16 V, 10% tol	AVX	0402YC183KAT2A
8	4	C318,C323,C418,C421	Capacitor	402	22 pF, ceramic, NPO, 5% tol, 50 V	Kemet	C0402C220J5GACTU
9	1	C501	Capacitor	1206	10 µF, tantalum, 16 V, 10% tol	Kemet	T491B106K016AS
10	9	C214,C512,C513,C514,C515,C532,C533,C534,C535	Capacitor	603	1 µF, ceramic, X5R, 6.3 V, 10% tol	Panasonic	ECJ-1VB0J105K
11	8	C305,C306,C307,C308,C405,C406,C407,C408	Capacitor	805	0.1 µF, ceramic, X5R, 6.3 V, 10% tol		
12	4	C502,C504,C506,C508	Capacitor	603	10 µF, ceramic, X5R, 6.3 V, 10% tol		
13	1	CR201	Diode	SOT23	30V, 20mA, Dual Schottky		HSMS2812
14	2	CR401,CR500	LED	603	Green, 4 V, 5 m candela	Panasonic	LNJ306G8TRA
15	1	D502	Diode	DO-214AB	3 A, 30 V, SMC	Micro Commercial Co.	SK33MSCT
16	1	D501	Diode	DO-214AA	2 A, 50 V, SMC	Micro Commercial Co.	S2A
17	1	F501	Fuse	1210	6.0 V, 2.2 A trip current resettable fuse	Tyco/Raychem	NANOSMDC110F-2
18	1	FER501	Ferrite bead	2020	10 µH, 5 A, 50 V, 190 Ω @ 100 MHz	Murata	DLW5BSN191SQ2L
19	12	FB101, FB102, FB103,	Ferrite	603	10 Ω, test freq	Murata	BLM18BA100SN1

Item	Qnty. per Board	REFDES	Device	Pkg.	Value	Mfg.	Mfg. Part Number
		FB104, FB105, FB106, FB107, FB108, FB109, FB110, FB111, FB112	bead		100 MHz, 25% tol, 500 mA		
20	2	JP301, JP401	Connector	2-pin	100 mil header jumper, 2-pin	Samtec	TSW-102-07-G-S
21	2	J205,J402	Connector	3-pin	100 mil header jumper, 3-pin	Samtec	TSW-103-07-G-S
22	1	J201-J204	Connector	12-pin	100 mil header male, 4x3 triple row straight	Samtec	
23	1	J401	Connector	10-pin	100 mil header, male, 2x5 double row straight	Samtec	
24	8	L501, L502, L503, L504, L505, L506,L507,L508	Ferrite bead	1210	10 µH, bead core 3.2 × 2.5 × 1.6 SMD, 2 A	Panasonic - ECG	EXC-CL3225U1
25	4	L309, L310, L409, L410	Inductor	402	120 nH, test freq 100 MHz, 5% tol, 150 mA	Murata	LQG15HNR12J02B
26	16	L301, L302, L303, L304, L305,L306,,L307,L308,L401, L402, L403, L404, L405, L406, L407, L408	Resistor	805	0 Ω, 1/8 W, 5% tol	Panasonic	ERJ-6GEY0R00V
27	1	OSC200	Oscillator	SMT	Clock oscillator, 66.66 MHz, 3.3 V	CTS REEVES	CB3LV-3C-66M6666-T
28	5	P101, P103, P105, P107,P201	Connector	SMA	Sidemount SMA for 0.063" board thickness	Johnson Components	142-0711-821
29	1	P202	Connector	HEADER	1469169-1, right angle 2-pair, 25 mm, header assembly	Tyco	1469169-1
30	1	P503	Connector	0.1", PCMT	RAPC722, power supply connector	Switchcraft	SC1153
31	14	R201, R203,R204,R205, R214, R215, R221, R312, R315, R318, R411, R414,R417,R425	Resistor	402	10 kΩ, 1/16 W, 5% tol	Yageo America	9C04021A1002JLHF3
32	14	R103,R117,R129,R142,R216,R217,R218,R223,R224,R237,R420,R426,R427,R428	Resistor	402	0 Ω, 1/16 W, 5% tol	Yageo America	9C04021A0R00JLHF3
33	4	R102, R115, R128, R141	Resistor	402	64.9 Ω, 1/16 W, 1% tol	Panasonic	ERJ-2RKF64R9X
34	4	R104, R116, R130, R143	Resistor	603	0 Ω, 1/10 W, 5% tol	Panasonic	ERJ-3GEY0R00V
35	12	R109, R111,R112, R123, R125, R126, R135, R138, R139, R148, R149, R150	Resistor	402	1 kΩ, 1/16 W, 1% tol	Panasonic	ERJ-2RKF1001X
36	8	R108, R110, R121, R122, R134, R136, R146, R147	Resistor	402	33 Ω, 1/16 W, 5% tol	Yageo America	9C04021A33R0JLHF3
37	4	R161, R162, R163, R164	Resistor	402	499 Ω, 1/16 W, 1% tol	Panasonic	ERJ-2RKF4990X
38	1	R202	Resistor	402	100kΩ, 1/16 W, 5% tol	Yageo America	
39	1	R222	Resistor	402	4.02 kΩ, 1/16 W, 1% tol	Panasonic	ERJ-2RKF4021X

Item	Qnty. per Board	REFDES	Device	Pkg.	Value	Mfg.	Mfg. Part Number
40	1	R213	Resistor	402	49.9 Ω, 1/16 W, 0.5% tol	Susumu	RR0510R-49R9-D
41	1	R229	Resistor	402	5k Ω, 1/16 W, 5% tol	Yageo America	
42	2	R230,R319	Potentiometer	3-lead	10 kΩ, Cermet trimmer potentiometer, 18 turn top adjust, 10%, ½ W	BC Components	CT-94W-103
43	1	R228	Resistor	402	470 kΩ, 1/16 W, 5% tol	Yageo America	9C04021A4703JLHF3
44	1	R320	Resistor	402	39 kΩ, 1/16 W, 5% tol	Susumu	RR0510P-393-D
45	8	R307, R308, R309, R310, R407, R408, R409, R410,	Resistor	402	187 Ω, 1/16 W, 1% tol	Panasonic	ERJ-2RKF1870X
46	4	R305, R306, R405, R406, R500	Resistor	402	374 Ω, 1/16 W, 1% tol	Panasonic	ERJ-2RKF3740X
47	4	R316, R317, R415, R416	Resistor	402	274 Ω, 1/16 W, 1% tol	Panasonic	ERJ-2RKF2740X
48	11	R245,R247,R249,R251,R253,R255,R257,R259,R261,R263,R265	Resistor	201	0Ω, 1/16 W, 5% tol	Susumu	
49	4	R418,R421,R422,R423,	Resistor	402	4.7k Ω, 1/16 W, 1% tol	Panasonic	
50	1	R419	Resistor	402	261 Ω, 1/16 W, 1% tol	Panasonic	
51	1	R501	Resistor	603	261 Ω, 1/16 W, 1% tol	Panasonic	
52	2	R240,R241	Resistor	402	240 Ω, 1/16 W, 1% tol	Panasonic	
53	2	R242,R243	Resistor	402	100 Ω, 1/16 W, 1% tol	Panasonic	
54	1	S401	Switch	SMD	LIGHT TOUCH, 100GE, 5MM	Panasonic	EVQ-PLDA15
55	5	T101, T102, T103, T104,T201	Transformer	CD542	ADT1-1WT, 1:1 impedance ratio transformer	Mini-Circuits	ADT1-1WT
56	2	U501, U503	IC	SOT-223	ADP33339AKC-1.8, 1.5 A, 1.8 V LDO regulator	ADI	ADP33339AKC-1.8
57	2	U301, U401	IC	LFCSP, CP-32	AD8332ACP, ultralow noise precision dual VGA	ADI	AD8332ACP
58	1	U504	IC	SOT-223	ADP33339AKC-5	ADI	ADP33339AKC-5
59	1	U502	IC	SOT-223	ADP33339AKC-3.3	ADI	ADP33339AKC-3.3
60	1	U201	IC	LFCSP, CP-48-1	AD9219-65, quad 12-bit, 65 MSPS serial LVDS 3 V ADC	ADI	AD9219BCPZ-65
61	1	U203	IC	SOT-23	ADR510AR, 1.0 V, precision low noise shunt voltage reference	ADI	ADR510AR
62	1	U202	IC	LFCSP, CP-32-2	AD9515	ADI	AD9515BCPZ
63	1	U403	IC	TSSOP,	ADG3304	ADI	ADG3304BRUZ

Item	Qnty. per Board	REFDES	Device	Pkg.	Value	Mfg.	Mfg. Part Number
				RU-14			
64	1	U402	IC		PIC12F629	Microchip	PIC12F629
65	4	MP101-104	Part of assembly		CBSB-14-01A-RT, 7/8" height, standoffs for circuit board support	Richco	CBSB-14-01A-RT
66	4	MP105-108	Part of assembly		SNT-100-BK-G-H, 100 mil jumpers	Samtec	SNT-100-BK-G-H
67	4	MP109-112	Part of assembly		5-330808-3, pin sockets, closed end for OSC200	AMP	5-330808-3

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2

Figure 55. 48-Lead Frame Chip Scale Package [LFCSP]
(CP-48-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9219BCPZ-40	–40°C to +85°C	48 pin LF-CSP (Pb-Free) 7.0x7.0	CP-48
AD9219BCPZ-65	–40°C to +85°C	48 pin LF-CSP (Pb-Free) 7.0x7.0	CP-48
AD9219-65EB		Evaluation Board	