Isolated Half-Bridge Driver, 0.1 A Amp Output

Preliminary Technical Data

ADuM1230

FEATURES

- Isolated high-side and low-side outputs
  - High-side or low-side relative to input: ±700 V_{PEAK}
  - High-side/low-side differential: 700 V_{PEAK}
- 0.1 A peak output current
- High frequency operation: 5 MHz max
- High common-mode transient immunity: >50 kV/µs
- High temperature operation: 105°C
- Wide body, 16-lead SOIC
- UL1577 2500 V rms input-to-output withstand voltage

APPLICATIONS

- Isolated IGBT/MOSFET gate drives
- Plasma displays
- Industrial inverters
- Switching power supplies

GENERAL DESCRIPTION

The ADuM1230[1] is an isolated half-bridge gate driver that employs Analog Devices' *i*Coupler® technology to provide independent and isolated high-side and low-side outputs. Combining high speed CMOS and monolithic transformer technology, this isolation component provides outstanding performance characteristics superior to optocoupler-based solutions.

By avoiding the use of LEDs and photodiodes, this *i*Coupler gate drive device is able to provide precision timing characteristics not possible with optocouplers. Furthermore, the reliability and performance stability problems associated with optocoupler LEDs are avoided.

In comparison to gate drivers employing high voltage level translation methodologies, the ADuM1230 offers the benefit of true, galvanic isolation between the input and each output. Each output may be operated up to ±700 V_P relative to the input, thereby supporting low-side switching to negative voltages. The differential voltage between the high-side and low-side can be as high as 700 V_P.

As a result, the ADuM1230 provides reliable control over the switching characteristics of IGBT/MOSFET configurations over a wide range of positive or negative switching voltages.

[1] Protected by U.S. Patents 5,952,849 and 6,291,907.

FUNCTIONAL BLOCK DIAGRAM

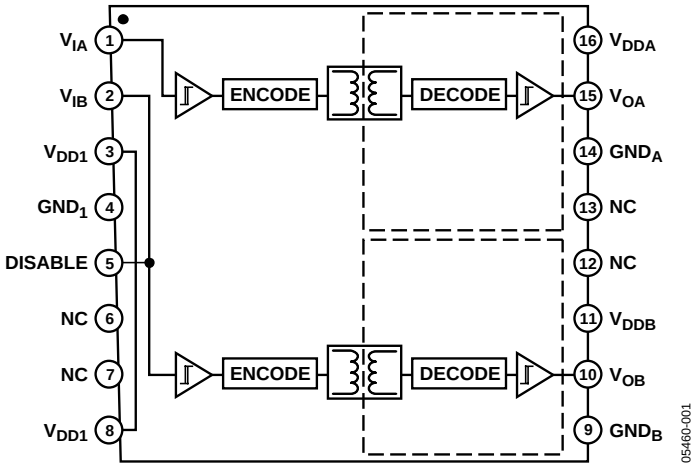

Figure 1.

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REVISION HISTORY

11/05—Rev. Sp0 to Rev. A

5/05—Revision Sp0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

All voltages are relative to their respective ground. 4.5 V ≤ V_{DD1} ≤ 5.5 V, 12 V ≤ V_{DDA} ≤ 18 V, 12 V ≤ V_{DDB} ≤ 18 V. All min/max specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = 5 V, V_{DDA} = 15 V, V_{DDB} = 15 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, Quiescent	$I_{DDI (Q)}$			4.0	mA	
Output Supply Current, A or B, Quiescent	$I_{DDA (Q)}$, $I_{DDB (Q)}$			1.2	mA	
Input Supply Current, 10 Mbps	$I_{DDI (10)}$			8.0	mA	
Output Supply Current, A or B, 10 Mbps	$I_{DDA (10)}$, $I_{DDB (10)}$			22	mA	C_L = 200 pF
Input Currents	I_{IA}, I_{IB}, $I_{DISABLE}$	−10	+0.01	+10	µA	0 ≤ V_{IA}, V_{IB}, $V_{DISABLE}$ ≤ V_{DD1}
Logic High Input Threshold	V_{IH}	2.0			V	
Logic Low Input Threshold	V_{IL}			0.8	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	V_{DDA} − 0.1, V_{DDB} − 0.1	V_{DDA}, V_{DDB}		V	I_{OA}, I_{OB} = −1 mA
Logic Low Output Voltages	V_{OAL}, V_{OBL}			0.1	V	I_{OA}, I_{OB} = 1 mA
Output Short-Circuit Pulsed Current[1]	$I_{OA (SC)}$, $I_{OB (SC)}$	100			mA	
SWITCHING SPECIFICATIONS						
Minimum Pulse Width[2]	PW			100	ns	C_L = 200 pF
Maximum Switching Frequency[3]		10			Mbps	C_L = 200 pF
Propagation Delay[4]	t_{PHL}, t_{PLH}	97	124	160	ns	C_L = 200 pF
Change vs. Temperature			100		ps/°C	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			8	ns	C_L = 200 pF
Channel-to-Channel Matching, Rising or Falling Edges[5]				5	ns	C_L = 200 pF
Channel-to-Channel Matching, Rising vs. Falling Edges[6]				13	ns	C_L = 200 pF
Part-to-Part Matching, Rising or Falling Edges[7]				55	ns	C_L = 200 pF
Part-to-Part Matching, Rising vs. Falling Edges[8]				63	ns	C_L = 200 pF
Output Rise/Fall Time (10% to 90%)	t_R/t_F			20	ns	C_L = 200 pF

[1] Short-circuit duration less than 1 second. Average power must conform to the limit shown under the Absolute Maximum Ratings.
[2] The minimum pulse width is the shortest pulse width at which the specified timing parameters are guaranteed.
[3] The maximum switching frequency is the maximum signal frequency at which the specified timing parameters are guaranteed.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] Channel-to-channel matching, rising vs. falling edges is the magnitude of the propagation delay difference between two channels of the same part when the inputs are either both rising edges or falling edges. The supply voltages and the loads on each channel are equal.
[6] Channel-to-channel matching, rising or falling edges is the magnitude of the propagation delay difference between two channels of the same part when one input is a rising edge and the other input is a falling edge. The supply voltages and loads on each channel are equal.
[7] Part-to-part matching, rising or falling edges is the magnitude of the propagation delay difference between the same channels of two different parts when the inputs are either both rising or falling edges. The supply voltages, temperatures, and loads of each part are equal.
[8] Part-to-part matching, rising vs. falling edges is the magnitude of the propagation delay difference between the same channels of two different parts when one input is a rising edge and the other input is a falling edge. The supply voltages, temperatures, and loads of each part are equal.

PACKAGE CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		2.0		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	θ_{JCa}		76		°C/W	

[1] The device is considered a 2-terminal device: Pins 1 through 8 are shorted together, and Pins 9 through 16 are shorted together.

REGULATORY INFORMATION

The ADuM1230 is approved, as shown in Table 3.

Table 3.

UL[1]
Recognized under 1577 component recognition program

[1] In accordance with UL1577, each ADuM1230 is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 5 µA).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.7 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.1 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

RECOMMENDED OPERATING CONDITIONS

Table 5.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+105	°C
Input Supply Voltage[1]	V_{DD1}	4.5	5.5	V
Output Supply Voltages[1]	V_{DDA}, V_{DDB}	12	18	V
Input Signal Rise and Fall Times			1	ms
Common-Mode Transient Immunity, Input-to-Output[2]		−50	+50	kV/µs
Common-Mode Transient Immunity, Between Outputs[2]		−50	+50	kV/µs
Transient Immunity, Supply Voltages[2]		−50	+50	kV/µs

[1] All voltages are relative to their respective ground.
[2] See the Common-Mode Transient Immunity section for transient diagrams and additional information.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{ST}	−55	+150	°C
Ambient Operating Temperature	T_A	−40	+105	°C
Input Supply Voltage[1]	V_{DD1}	−0.5	+7.0	V
Output Supply Voltage[1]	V_{DDA}, V_{DDB}	−0.5	+27	V
Input Voltage[1]	V_{IA}, V_{IB}	−0.5	V_{DDI} + 0.5	V
Output Voltage[1]	V_{OA}, V_{OB}	−0.5	V_{DDA} + 0.5, V_{DDB} + 0.5	V
Input-Output Voltage[2]		−700	+700	V_{PEAK}
Output Differential Voltage[3]			700	V_{PEAK}
Output DC Current	I_{OA}, I_{OB}	−20	+20	mA
Common-Mode Transients[4]		−100	+100	kV/µs

[1] All voltages are relative to their respective ground.
[2] Input-to-output voltage is defined as GND_A − GND_1 or GND_B − GND_1.
[3] Output differential voltage is defined as GND_A − GND_B.
[4] Refers to common-mode transients across any insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings can cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Ambient temperature = 25°C, unless otherwise noted.

Table 7. ADuM1230 Truth Table (Positive Logic)

V_{IA}/V_{IB} Input	V_{DD1} State	DISABLE	V_{OA}/V_{OB} Output	Notes
H	Powered	L	H	
L	Powered	L	L	
X	Unpowered	X	L	Output returns to input state within 1 µs of V_{DDI} power restoration.
X	Powered	H	L	

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on