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Analog Devices JTAG Emulation Technical Reference

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Introduction

This document provides technical information to properly design a JTAG emulator interface for Analog Devices, Inc. (ADI) processor targets, that in this document are all referred to as *Digital Signal Processors (DSPs).*

ADI designs, manufactures, and sells several different types of JTAG emulators for use with ADI DSP targets supporting an embedded JTAG emulator port. This document has been revised to only support the current line of ADI emulators. This product line includes the HPPCI, HPUSB and USB emulators.

Table 4 explains in detail important information referenced by a "Note n" reference in figures and tables throughout this document. You should first review this table before continuing with this document. Most questions addressed by users regarding differences with our JTAG emulator products and previous versions of this document are answered in this table.

Older versions of this document supported ADI JTAG emulator legacy products. They included the *Mountain-ICE, Summit-ICE, Trek-ICE, Apex-ICE, and EZ-ICE.* If you require information for any ADI JTAG emulators not supported in this document, you should contact ADI's DSP development tools technical support for an older revision of this document which contains legacy JTAG emulator information.

Do not use older versions of EE-68 for new target designs. Periodically check ADI's web site at

http://www.analog.com/ee-notes/

for newer revisions of this document. Targets which were designed using an older revision of EE-68 should only be updated if there are problems performing JTAG emulation.

JTAG Emulator Interface Design

All ADI JTAG emulators interface with the DSP using a 14-pin JTAG emulator header. The header provides a connection interface for the JTAG emulator pod. The header can also be used to route an optional local boundary scan controller to the DSP when the JTAG emulator is not attached.

All ADI JTAG emulators use a superset of the IEEE 1149.1 standard to send and receive data from the DSP JTAG emulation port. The JTAG emulators use an additional signal called EMU~ as a JTAG emulation status flag from the DSP. This signal is a vendor specific signal, which is not part of the IEEE 1149.1 specification.

The following pages will define in detail the design requirements for supporting ADI JTAG emulators. This information includes functional, electrical, and mechanical requirements for interfacing a target design with a JTAG emulator.

JTAG Emulator Target Header

Referring to Figure 1, the JTAG emulator header has 14 pins. You must supply this header on your target to communicate with the JTAG emulator. The JTAG emulator target header interface is a standard dual-row 0.025” male square-post header, set on 0.1” x 0.1” spacing, with a minimum post length of 0.235”. Pin 3 on the JTAG emulator cable header is keyed to prevent accidental insertion of the pod to the target backwards. Clip pin 3 on your target board header allow insertion of the JTAG emulator cable female header.

(See Table 4 for notes)

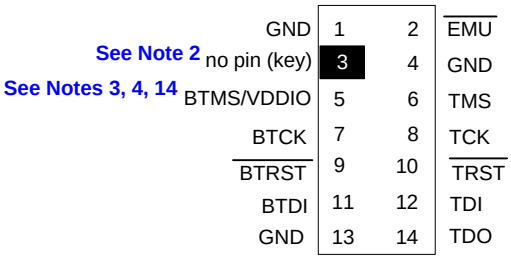

Figure 1. JTAG Emulator Target Header Interface

JTAG Emulator Pod Mechanical Requirements

This section explains the mechanical specifications for the JTAG emulator pod.

JTAG Emulator Header clearance requirements

Provide a clearance of at least 0.30” and 0.10” around the length and width of the header. Refer to Figure 2 for information about the pod connector keep out area.

Make sure you allow for height clearance above the header for attaching and detaching the JTAG emulator cable from your target.

Refer to Figure 3 for any height clearance restriction information regarding the HPPCI JTAG emulator cable. Refer to Figure 4 for any height clearance restriction information for the HPUSB and USB JTAG emulators.

(See Table 4 for notes)

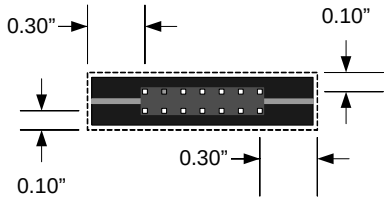

Figure 2. JTAG Emulator Header Keep Out Area

(See Table 4 for notes)

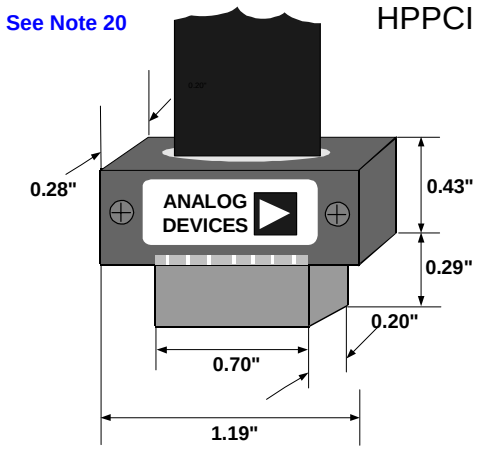

Figure 3. HPPCI JTAG Emulator Pod Dimensions

(See Table 4 for notes)

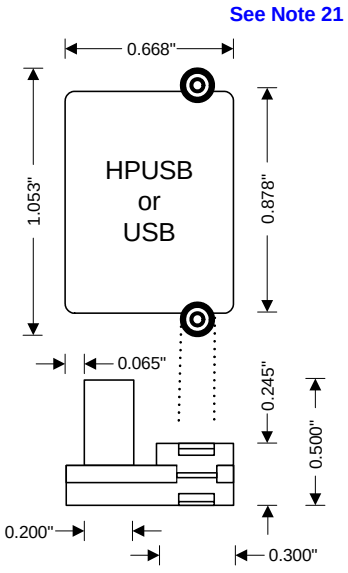

Figure 4. HPUSB JTAG Emulator Pod Dimensions

Local Boundary Scan Controller

Referring to Figure 1, the set of signals on the odd-numbered side of the connector can be used by targets which have an optional local boundary scan controller. These signals include the boundary-scan controller JTAG signals BTMS/VDDIO, BTCK, BTDI, and BTRST~. Each of these signals is described in Table 1.

Pin	Signal	Description	Emulator	Target
1	GND	Digital Ground	Passive	Passive
2	EMU~	JTAG Emulation Flag	Input *{active low}*	Output *{open drain} {active low}*
3	KEY	Header Alignment position -- pin must be clipped on target header See note 2	No Connect	No Connect
4	GND	Digital Ground	Passive	Passive
5	VDDIO or BTMS	Automatic Voltage Sense (VDDIO) See note 3 or Target Local Boundary Scan Controller JTAG TAP Test Mode Select	Input	Passive or Output
6	TMS	JTAG TAP Test Mode Select	Output	Input
7	BTCK	Target Local Boundary Scan Controller JTAG TAP Test Clock	No Connect	Output
8	TCK	JTAG TAP Test Clock	Output	Input
9	BTRST~	Target Local Boundary Scan Controller JTAG TAP Test Reset	No Connect	Output *{active low}*
10	TRST~	JTAG TAP Test Reset	Output	Input *{active low}*
11	BTDI	Target Local Boundary Scan Controller JTAG TAP Test Data In	No Connect	Output
12	TDI	JTAG TAP Test Data In	Output	Input
13	GND	Digital Ground	Passive	Passive
14	TDO	JTAG TAP Test Data Out	Input	Output

Table 1. JTAG Emulator Header Signal Descriptions

Only the HPPCI JTAG emulator supports automatic voltage sensing with pin 5. The USB and HPUSB JTAG emulators pin 5 only supports the BTMS functionality. See note 3 and note 4 in Table 4 regarding special instructions for pin 5.

Pin 5 (BTMS/VDDIO) is a dual purpose pin. First, it is used by the JTAG emulator to sense the DSP IO voltage (VDDIO). Second, it can be used to route a local boundary scan controller BTMS signal to the DSP TMS pin when the JTAG emulator is not connected.

The ***HPPCI*** JTAG emulator can automatically sense a DSP IO voltage (VDDIO) up to 5 V. The ***HPPCI*** JTAG emulator uses the VDDIO voltage it senses from the BTMS/VDDIO pin to adjust the JTAG emulator interface input signal thresholds and output signal drive levels to those shown in Table 2. You must pull pin 5 (BTMS/VDDIO) up to

the DSP IO voltage (VDDIO) with a 4.7 KΩ resistor when using the ***HPPCI*** JTAG emulator. See note 3 and note 4 in Table 4 regarding special instructions for pin 5.

Targets with Local Boundary Scan Logic

Targets which use optional local boundary scan controller logic should connect the local boundary-scan signal pins to the JTAG emulator header pins shown in Figure 5.

If your target has a optional local boundary scan controller, and you attach the ***HPPCI*** JTAG emulator, you will need to isolate BTMS signal from the BTMS/VDDIO voltage before starting the emulator software. Referring to Figure 5 and Figure 7, during JTAG emulation you can isolate pin 5 on the ***HPPCI*** JTAG emulator header from the local boundary scan controller logic using a jumper or tri-state buffer. You must provide a method to isolate the BTMS signal on your target from the BTMS/VDDIO pin on the JTAG emulator header when the ***HPPCI*** JTAG emulator is connected. Isolation must be effective before the ***HPPCI*** JTAG emulator software is invoked. This isolation will prevent the local boundary scan controller BTMS signal from confusing the automatic voltage sensing logic in the ***HPPCI*** JTAG emulator pod.

Connections are made between the local boundary scan controller and the DSP by installing or removing jumpers between the local boundary scan controller JTAG signals and the DSP JTAG emulation signals. The local boundary scan signals include BTMS, BTCK, BTDI, and BTRST~. DSP JTAG emulation signals TMS, TCK, TDI, and TRST~ connect to local boundary scan signals using jumpers on the JTAG emulator header shown in Figure 5.

TRST~ must be pulsed low at power up when using a local boundary scan controller, and should be kept low when the local boundary scan controller and the JTAG emulator are not being used. Figure 5 shows how TRST~ should be controlled when the target uses a local boundary scan controller.

If your target has a local boundary scan controller and your target *does not* control the BTRST~ signal, you will need to control the BTRST~ signal with additional logic. This additional logic needs to guarantee the BTRST~ signal is only pulsed low during power on reset. It should be driven high all other times during local boundary scan. This will prevent holding the BTRST~ signal low continuously during local boundary scans. Keeping the DSP TAP constantly in reset with the BTRST~ signal forced to ground with a jumper or pull-down resistor will prevent the DSP from executing a local boundary scan.

Jumpers can be substituted with zero ohm resistors on production boards. If you plan to use the same board revision for debugging and production, you should design your target with a dual footprint. The dual footprint should accommodate the header described in Figure 1 for debug version boards, and surface mount resistors for production version boards.

With the exception of pin 5 (BTMS/VDDIO) on the ***HPPCI*** JTAG emulator, all target local boundary scan controller pins (BTCK, BTRST~, BTDI) are not connected inside the JTAG emulator pod. They are used only to provide a method for inserting or removing the DSP from the local boundary-scan controller logic using jumpers across the JTAG emulation header.

Targets without Local Boundary Scan Logic

As shown in Figure 6 and Figure 8, targets which do not use a local boundary scan controller, or do not include the DSP in the local boundary scan controller chain, should tie all boundary scan pins to ground except for pin 5 on the ***HPPCI*** JTAG emulator. Pin 5 the BTMS/VDDIO signal, is required by the ***HPPCI*** JTAG emulator pod to automatically sense the DSP IO voltage (VDDIO).

Jumpers can be substituted with zero ohm resistors on production boards. If you plan to use the same board revision for debugging and

production, you should design your target with a dual footprint. The dual footprint should accommodate the header described in Figure 1 for debug boards, and surface mount resistors for production boards.

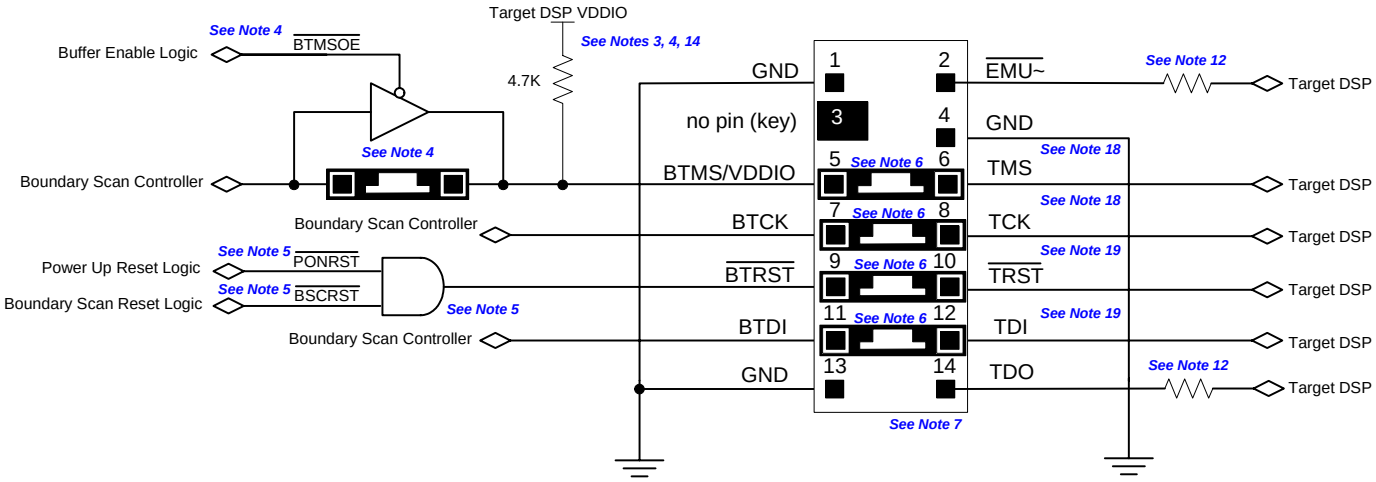

Figure 5. Single DSP Target with a Local Boundary Scan Controller

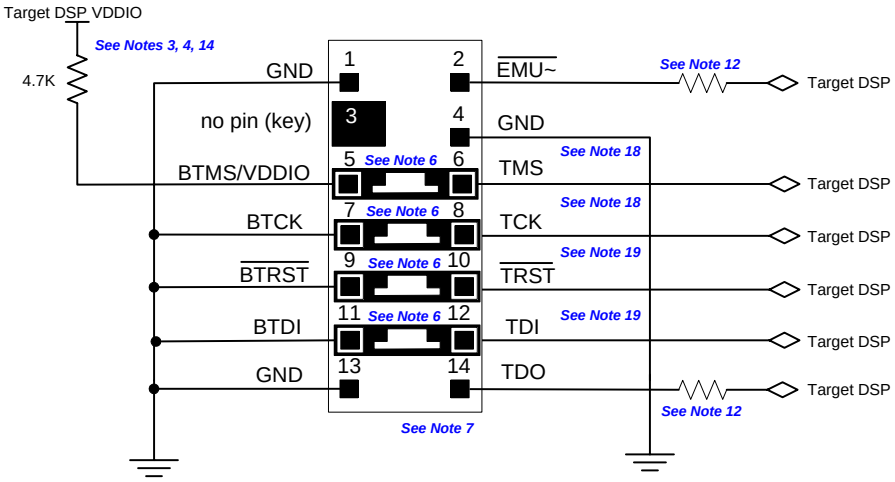

Figure 6. Single DSP Target without a Local Boundary Scan Controller

Single DSP Target Connections

Single DSP targets with route distances between the JTAG emulator header and DSP less than six (6) inches do not require buffering. Your target requires buffering if the worst case route distance between the JTAG emulator header and the DSP is greater than six (6) inches regardless of the number of DSPs in the scan chain path.

Figure 6 shows the connections between the JTAG emulator header and the DSP for a single DSP target *without* a local boundary scan controller. Figure 5 shows the connections between the JTAG emulator header and the DSP for a single DSP target *with* a local boundary scan controller.

Figure 5 and Figure 6 show series terminating resistors for the TDO and EMU~ signals going to the JTAG emulator. These resistors are optional.

You should design them into your target if you have routes longer than 6 inches in length between the TDO or EMU~ outputs from the DSP back to the JTAG emulator header. The resistor value is generally equal to the impedance of the printed circuit (Z_{PCB}) board minus the output impedance of the TDO or EMU~ signal I/O driver (Z_{Driver}). Initially set these resistors to zero ohms. Change the value of the termination resistance $Z_{Terminator,}$ to $Z_{PCB} - Z_{Driver}$ if signal integrity problems are observed when using the JTAG emulator. Tuning the termination resistor value to something slightly less than or greater than ($Z_{Terminator}$) may be required depending on the condition of the signals. Place the termination resistors as close as possible to the DSP.

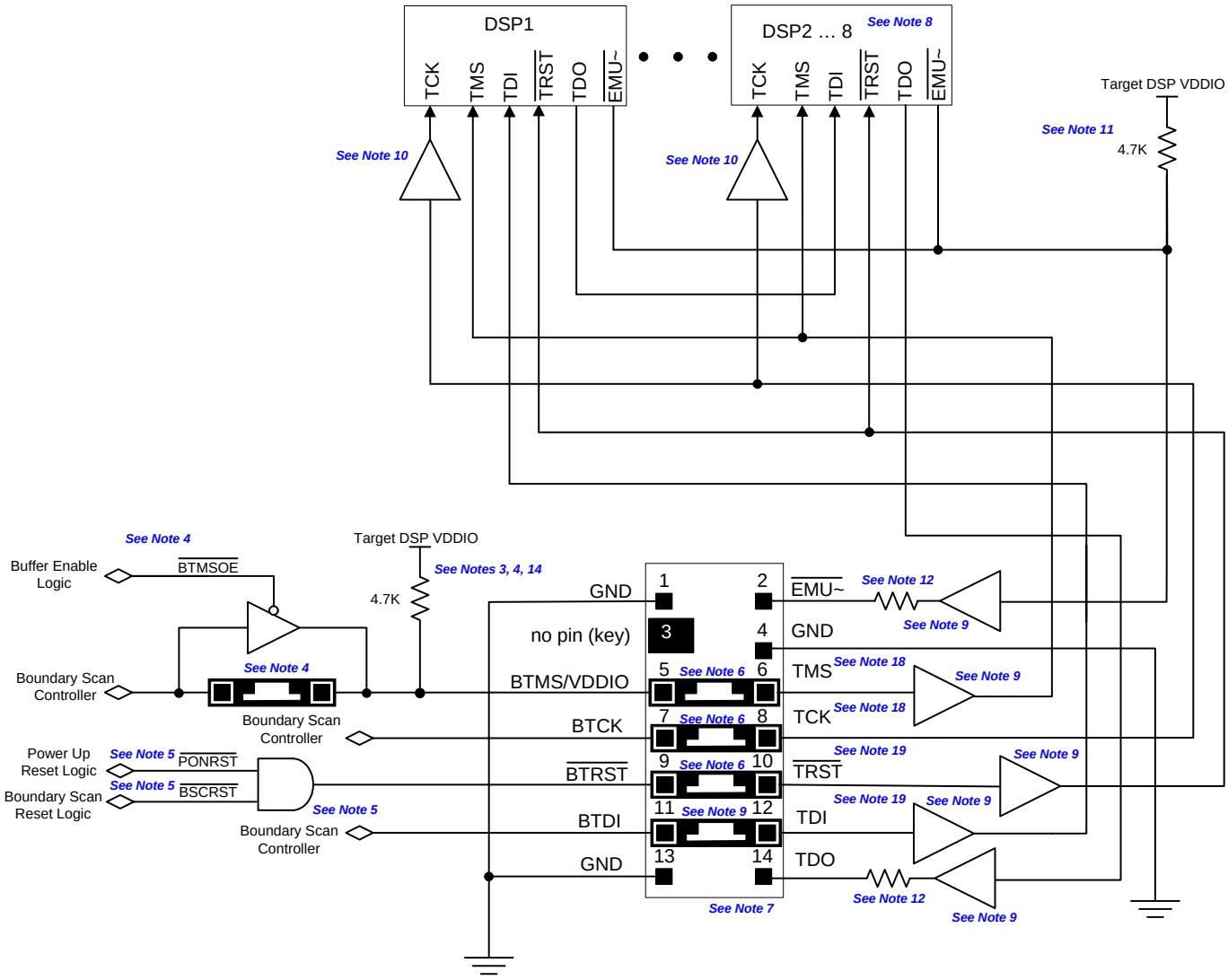

Figure 7. Multiple DSP Target with a Local Boundary Scan Controller

Printed circuit board traces between the JTAG emulator header and the DSP on a single DSP target without JTAG signal buffers must be shorter than six (6) inches. Route all traces between the JTAG emulator header and the DSP as a group, using equal lengths (if possible). Provide good crosstalk isolation from other signal nets especially clocks.

Multiple DSP Target Connections

Targets with more than one DSP in the scan path require buffering as shown in Figure 7 and Figure 8. Figure 7 shows the connections between the JTAG emulator header and the buffers for a multiple DSP target *with* a local boundary scan controller. Figure 8 shows the connections between the JTAG emulator header and the buffers for a multiple DSP target *without* a local boundary scan controller.

Figure 7 and Figure 8 show series terminating resistors for the TDO and EMU~ signals going to the JTAG emulator. These resistors are optional. You should design them into your target if you have routes longer than 6 inches in length between the TDO or EMU~ buffers and the JTAG emulator header. The resistor value is generally equal to the impedance of the printed circuit (Z_{PCB}) board minus the output impedance of the TDO or EMU~ signal I/O driver (Z_{Driver}). Initially set these resistors to zero ohms. Change the value of the termination resistance $Z_{Terminator,}$ to $Z_{PCB} - Z_{Driver}$ if signal integrity problems are observed when using the JTAG emulator. Tuning the termination resistor value to something slightly less than or greater than ($Z_{Terminator}$) may be required depending on the condition of the signals. Place the termination resistors as close to the DSP as possible.

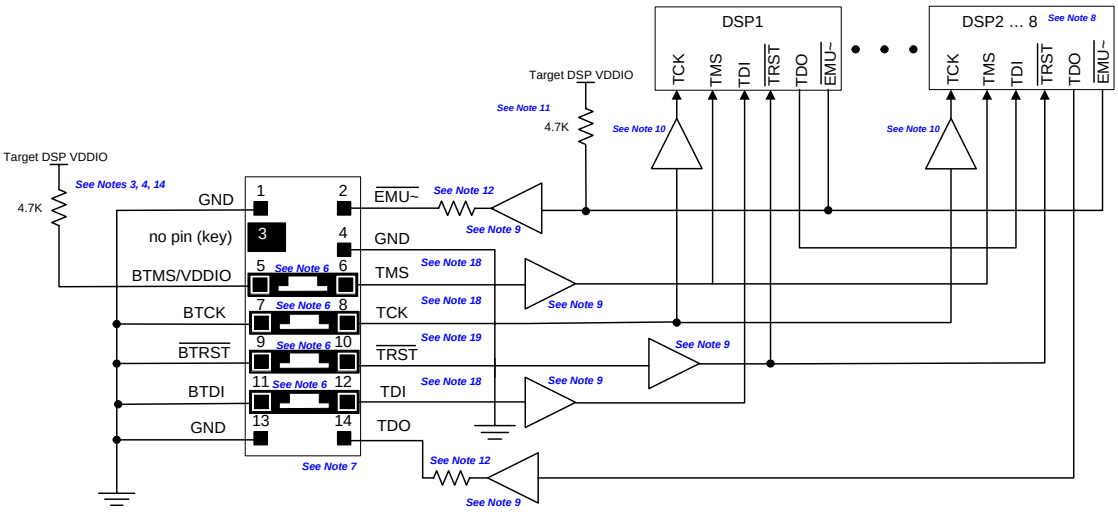

Figure 8. Multiple DSP Target without a Local Boundary Scan Controller

Route all traces between the JTAG emulator header and the DSP as a group, using equal lengths when possible. Provide good crosstalk isolation from other signal nets especially clocks.

To minimize signal skew, ensure buffers for the TMS, TDI, TRST~ TDO, and EMU~ signals come from a single package. For TCK signals, use a driver with a high fan out. The drivers should come from a single dedicated package that *is not* used by other TMS, TDI, TRST~, TDO, and EMU~ signals.

Limit the number of loads (DSPs) for the TMS, TRST~, and EMU~ buffered signals to eight (8). Limit the number of loads for the TCK buffered signals to one (1). Additional loads (DSPs) should use another buffer to support up to eight (8) more devices.

Using more than sixteen (16) physical devices in one scan chain is not recommended. The best approach for large numbers (>16) of physical devices is to break the chain into smaller independent chains, each with its own JTAG header and buffers. If this is not possible, try adding jumpers to reduce the number of devices in one chain at a time for debug purposes. Pay special attention to PCB routing to minimize transmission line effects.

JTAG Emulator Interface PCB Layout

Treat all JTAG emulator signals (TCK, TMS, TDI, TDO, EMU~, and TRST~) as critical route signals. Pay special attention when routing these signals on your target. Specify a controlled impedance requirement between 50 Ω and 75 Ω. Minimize cross-talk and inductance on these signal lines by using a solid ground plane and routing the JTAG emulator signals away from high frequency nets, especially clock lines. Keep these routes as short as possible, and equal in length when possible.

These lines must be clean. You may need to provide series terminations for very long TDO and EMU~ routes. See note 12 in Table 4 regarding series terminations.

JTAG Emulator Power Sequence

Your JTAG emulator should be powered on, and connected to a host PC, prior to attaching it to a target JTAG emulator header. All ADI High Performance JTAG emulator products can be attached or removed from a powered "hot" target without any power restrictions.

Avoid emulation errors by making sure the emulation software is not started or executing when power is not applied to the target, or when attaching the JTAG emulator to a target with or without power.

A jumper should be installed for the TRST~, signal across the JTAG emulator header TRST~ and BTRST~ pins before applying power to the target. You should also have this jumper installed whenever the JTAG emulator is not attached to the JTAG emulator header after power has been applied to the target. This jumper will prevent the JTAG TAP in the DSP from getting "lost" in an un-recoverable state. All though not required, as an extra added precaution you should also jumper the TMS, TCK, and TDI signals at the JTAG emulation header.

JTAG Emulator Pod Electrical Requirements

This section explains the electrical specifications for the JTAG emulator pod.

HPPCI JTAG Emulator Automatic Voltage Sense Pod Logic

The ***HPPCI*** JTAG emulator pod uses pin 5 (BTMS/VDDIO) of the JTAG emulator header to automatically sense the target I/O voltage. The voltage sensing logic controls which voltage threshold values the JTAG emulator uses for JTAG signals received from the target. The voltage sensing logic also sets the drive levels for JTAG signals sent to the target.

Your target DSP IO voltage (VDDIO) may or may not be the same voltage used by the DSP core. Make sure you are using correct DSP supply voltage for VDDIO when configuring your target for the HPPCI JTAG emulator automatic voltage sense. You must pull the signal up to the correct voltage plane with a 4.7 KΩ resistor. *Do not* connect the BTMS/VDDIO pin directly to the VDDIO voltage plane. See note 3 and note 4 in Table 4 for more information regarding the BTMS/VDDIO pin.

JTAG Emulator Pod I/O Characteristics

The JTAG emulator pod is tolerant up to 5VDC. It will work with all Analog Devices JTAG family DSPs with JTAG I/O voltages of 5 V, 3.3 V, 2.5 V, and 1.8 V. The pod will drive 5 V targets with 3.3 V logic levels, which are well within the 5 V logic threshold requirements. Table 2 includes all the I/O characteristics for the JTAG emulator pod.

Pin	JTAG Emulator Signal	VDDIO (VDC)	Cin (pF)	Cout (pF)	VIH (VDC)	VIL (VDC)	VOH (VDC)	VOL (VDC)	IOL (mA)	IOH (mA)
2	EMU~	5 / 3.3	6		2.0	0.8	-	-	-	-
6	TMS	5 / 3.3		6.5	-	-	2.3	0.7	12	12
8	TCK	5 / 3.3		6.5	-	-	2.3	0.7	12	12
10	TRST~	5 / 3.3		6.5	-	-	2.3	0.7	12	12
12	TDI	5 / 3.3		6.5	-	-	2.3	0.7	12	12
14	TDO	5 / 3.3	6		2.0	0.8	-	-	-	-
2	EMU~	2.5	6		1.7	0.7	-	-	-	-
6	TMS	2.5		6.5	-	-	1.8	0.6	8	8
8	TCK	2.5		6.5	-	-	1.8	0.6	8	8
10	TRST~	2.5		6.5	-	-	1.8	0.6	8	8
12	TDI	2.5		6.5	-	-	1.8	0.6	8	8
14	TDO	2.5	6		1.7	0.7	-	-	-	-
2	EMU~	1.8	6		1.2	0.6	-	-	-	-
6	TMS	1.8		6.5	-	-	1.3	0.5	4	4
8	TCK	1.8		6.5	-	-	1.3	0.5	4	4
10	TRST~	1.8		6.5	-	-	1.3	0.5	4	4
12	TDI	1.8		6.5	-	-	1.3	0.5	4	4
14	TDO	1.8	6		1.2	0.6	-	-	-	-

Table 2. JTAG Emulator Pod I/O Characteristics

JTAG Emulator Pod Timing

This section details important timing information regarding JTAG signals at the target JTAG emulator header. Figure 9 diagrams switching and timing relationships for JTAG signals at the target JTAG emulator header.

Table 3 defines switching parameters for the JTAG emulator output signals (`TCK`, `TMS`, `TDI`, and `TRST~`), and setup and hold requirements for JTAG emulator input signals (`TDO`, and `EMU~`). Table 3 also defines the frequency of operation range for high performance JTAG emulator products. The table parameter reference numbers maps to the timing diagram reference numbers shown in Figure 9.

You should use this information to determine your target's maximum routing lengths, net loading, and load capacitance which can be tolerated for JTAG emulation signal routes.

#	Parameter	Product	Frequency	Description	Min	Max	Unit
1	t_{c}TCK	HPPCI	10↔50 MHz	TCK period	*19.9*	*100.1*	ns
1	t_{c}TCK	HPUSB	5↔50 MHz	TCK period	*19.9*	*200.1*	ns
1	t_{c}TCK	USB	10 MHz	TCK period	*99.1*	*100.1*	ns
2	t_{w}TCKH	HPPCI	10↔50 MHz	TCK high pulse width	*9.95*	*50.05*	ns
2	t_{w}TCKH	HPUSB	5↔50 MHz	TCK high pulse width	*9.95*	*100.05*	ns
2	t_{w}TCKH	USB	10 MHz	TCK high pulse width	*49.95*	*50.05*	ns
3	t_{w}TCKL	HPPCI	10↔50 MHz	TCK low pulse width	*9.95*	*50.05*	ns
3	t_{w}TCKL	HPUSB	5↔50 MHz	TCK low pulse width	*9.95*	*100.05*	ns
3	t_{w}TCKL	USB	10 MHz	TCK low pulse width	*49.95*	*50.05*	ns
4	tdTMS	HPPCI	10↔50 MHz	Delay TMS/TDI/TRST~ from TCK ↓		3	ns
4	tdTMS	HPUSB	5↔50 MHz	Delay TMS/TDI/TRST~ from TCK ↓		3	ns
4	tdTMS	USB	10 MHz	Delay TMS/TDI/TRST~ from TCK ↓		3	ns
5	tsuTDO	HPPCI	10 MHz	Setup time TDO/EMU~ to TCK ↑	14.1		ns
5	tsuTDO	HPPCI	25 MHz	Setup time TDO/EMU~ to TCK ↑	1		ns
5	tsuTDO	HPPCI	33 MHz	Setup time TDO/EMU~ to TCK ↑	8.4		ns
5	tsuTDO	HPPCI	50 MHz	Setup time TDO/EMU~ to TCK ↑	9.9		ns
5	tsuTDO	HPUSB	5-50 MHz	Setup time TDO/EMU~ to TCK ↑	2		ns
5	tsuTDO	USB	10 MHz	Setup time TDO/EMU~ to TCK ↑	2		ns
6	thTDO	HPPCI	10-50 MHz	Hold time TDO/EMU~ from TCK ↑	0		ns
6	thTDO	HPUSB	5-50 MHz	Hold time TDO/EMU~ from TCK ↑	0		ns
6	thTDO	USB	10 MHz	Hold time TDO/EMU~ from TCK ↑	0		ns

Table 3. JTAG Emulator Pod Timing Information

The maximum frequency numbers shown in Table 3 are only guaranteed when your target meets the setup and hold requirements defined in Table 3. When calculating your setup and hold

margins, remember to include the TDO and EMU~ delay parameters from the target DSP datasheet. If your target does not meet the setup and hold requirements defined in Table 3, you will have to operate the JTAG emulator at a lower frequency for reliable performance.

If you can not operate the JTAG emulator using the lowest available frequency, you should check your target for a miss wiring or redesign your target to reduce delays. You should look at reducing trace lengths, reducing electrical loads, and using faster buffers.

The setup and hold time requirements are based on the worst case maximum delay of the JTAG emulator hardware. Typically, the setup and hold time requirements will be considerably smaller than the values in the table. If you have a complex JTAG emulation path with long propagation delays, you should perform a timing analysis on your targets JTAG paths. This analysis should determine if your target JTAG emulation paths have sufficient timing margin to operate at the desired JTAG TCK frequency.

When performing a timing analysis, the timing margin must be a positive number. As a general rule, the margin desired should be at least 10 % of a full TCK clock period. However, be aware when you are doing your analysis, the delay numbers given are based on worst case delay. Typically, logic will tend to run somewhere in the middle between minimum and maximum delay, although this cannot be guaranteed. If your margin is negative, but very close (< 1 ns), you may want to try using typical numbers in your analysis to see you still have a negative margin.

If you still calculate a negative margin using typical values, you must try selecting a slower TCK frequency if available, or make changes to your target to reduce the JTAG emulator path delays.

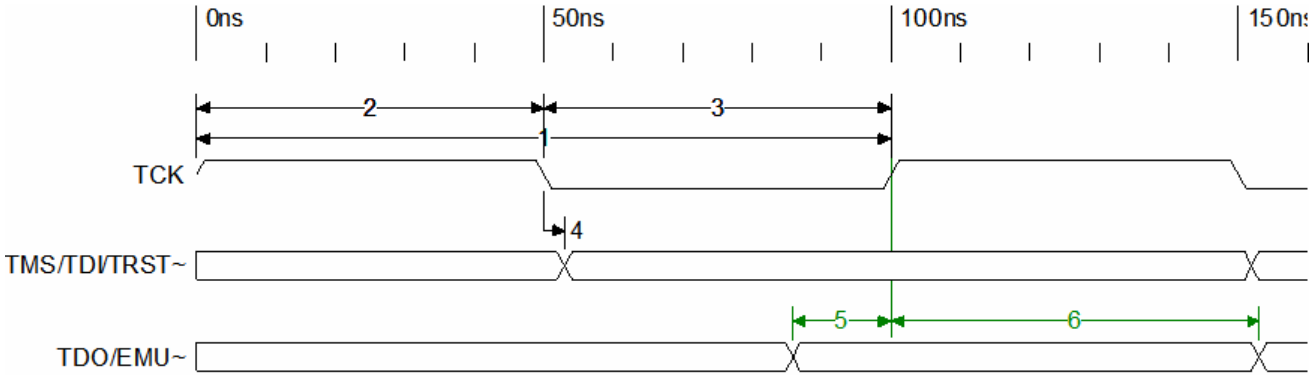

Figure 9. JTAG Emulator Pod Timing Waveform

Conclusion

Using the recommendations described in this document, should make designing the JTAG emulation interface for your target straight forward. Having a well designed JTAG emulator interface on your target will allow you to rapidly begin development and testing your application, instead of spending valuable time debugging the JTAG emulation port.

You should check the ADI DSP Tools Web site periodically for updates to this document

Reference

The IEEE 1149.1 JTAG standard is sponsored by the Test Technology Standards Committee of the IEEE Computer Society, and published by the IEEE.

To order a copy, call IEEE at 1-800-678-4333 in the US and Canada, 1-908-981-1393 outside of the US and Canada. You can also visit the IEEE standards web site at

http://standards.ieee.org/

Appendix

#	Note Description
1	Deleted –
2	The JTAG emulator 14-pin female header has position 3 plugged to prevent improper connection, and is used as a orientation key. The JTAG emulator 14-pin female header position 3 *does* connect to a wire in the JTAG cable which is connected to ground at the JTAG emulator.
3	Pin 5 BTMS/VDDIO is a dual purpose pin on the HPPCI JTAG emulator. First, it allows you to route an optional local boundary scan controller TMS signal to the target DSP TMS signal when the JTAG ICE is not attached to the JTAG header and a jumper is installed between pins 5 and 6 of the JTAG header. Second, this pin is used by the JTAG ICE to auto detect the targets DSP I/O voltage (VDDIO) up to 5 V. The JTAG ICE uses the sensed voltage to establish input and output voltage levels for the DSP JTAG signals. You should pull this pin up to the VDDIO level using a 4.7 KΩ resistor. Do not connect it directly to the VDDIO plane. The HPUSB and USB emulators do not support VDDIO auto sensing on pin 5. Pin 5 is a single function pin used to route an optional local boundary scan controller TMS signal to the target DSP TMS signal when the JTAG ICE is not attached to the JTAG header and a jumper is installed between pins 5 and 6 of the JTAG header. You may connect a HPUSB or USB JTAG emulator to a target designed for the HPPCI JTAG emulator, with the VDDIO auto sensing logic. The HPUSB or USB JTAG emulator does not connect pin 5 back at the emulator, so no harm will be done to the target or the emulator. The voltage thresholds for your target when using the HPUSB or USB JTAG emulators are set manually by the user in the VisualDSP Debugger session configurator.
4	When using the HPPCI JTAG emulator, you need to control the BTMS signal at pin 5 so that it is not being driven by the local boundary scan controller when the JTAG ICE is attached to the header. Failure to isolate the BTMS signal when the JTAG ICE is connected could result in unpredictable behavior by the JTAG ICE due to possible incorrect voltage sensing on pin 5. As shown above, you can isolate the BTMS signal using a jumper, or a buffer. When using a buffer, its output must be disabled when the JTAG ICE is connected. When using the HPUSB and USB JTAG emulators which do not support VDDIO auto sensing, you

#	Note Description
	can connect pin 5 directly to the target local boundary scan controller BTMS signal without any pull-up resistor required.
5	When using local boundary scan, you must control the TRST~ signal on the DSP so that it is pulsed low when power is first applied to the target. Failure to properly reset the DSP JTAG TAP can result in unpredictable DSP behavior during boundary scans. The circuit shown above (AND gate) is one possible way to control the TRST~ signal correctly. If your target has a local boundary scan controller but your target does not control the BTRST~ signal, you will need to control the BTRST~ signal with additional logic. The additional logic needs to guarantee the BTRST~ signal is only pulsed low during power on reset, and is then driven high all other times during local boundary scan. This will prevent holding the BTRST~ signal low continuously during local boundary scans. Keeping the DSP TAP constantly in reset with the BTRST~ signal will prevent the DSP from executing a local boundary scan.
6	You may substitute jumpers with zero ohm resistors on production boards.
7	See figure 1 for description of the JTAG emulator header pins.
8	Each buffer should support a maximum of 8 DSPs, except for TCK buffers, which should support only one DSP per buffer.
9	For 5 V targets, buffer the TMS, TDI, TRST~, TDO, and EMU~ signals with a type 74AC11244 buffer (or equivalent). For 3.3 V / 2.5 V / 1.8 V low-voltage targets, buffer the TMS, TDI, TRST~, TDO, and EMU~ signals with a type 74AVC16244 buffer (or equivalent).
10	For 5 V targets, buffer the TCK signal with a low skew, high fan out, minimal input-to-output delay dual 1-to-5 clock driver type IDT49FCT3805E (or equivalent). For 3.3 V low voltage targets, buffer the TCK signal with a low skew, high fan out, minimal input-to-output delay dual 1-to-5 clock driver type IDT49FCT805 (or equivalent). For 2.5 V / 1.8 V very low voltage targets, buffer the TCK signal with a low skew, high fan out, minimal input-to-output delay single 1-to-5 clock driver type IDT5T9050 (or equivalent).
11	The DSP EMU~ signal is an open drain signal which must be pulled up with a 4.7 KΩ resistor on multiprocessor targets at the buffer input. On single processor targets without a buffer, the JTAG ICE internal logic will pull up the open drain signal with a internal 4.7 KΩ resistor.
12	These resistors are optional. We recommended you design them into your target if you have TDO or EMU~ routes between the DSP and JTAG emulation header greater than 6 inches in length. The resistor value ($Z_{Termination}$) is generally equal to the impedance of the printed circuit (Z_{PCB}) board minus the output impedance of the TDO or EMU~ signal I/O driver (Z_{Driver}).
13	BSC -- Local Boundary Scan Controller if implemented on target.
14	VDDIO is the Target DSP I/O voltage supply *not* the DSP core voltage supply, make sure you connect VDDIO to the correct voltage plane when using the HPPCI VDDIO auto sense function.

#	Note Description
15	Currently, the High Performance product line includes ADI's *HPPCI ICE*, *HPUSB ICE*, and the *USB ICE*.
16	JTAG emulator signals EMU~ and TDO are type input.
17	JTAG emulator signals TCK, TMS, TDI, and TRST~ are type output.
18	Previous versions of EE-68 have called for 4.7 KΩ pull-up resistors for TMS, TCK, and TDI to increase the noise immunity for these signals. High speed rail to rail CMOS buffers with strong output drive current now used in our High Performance JTAG emulator product line makes this requirement unnecessary .
19	Previous versions of EE-68 have called out for a 4.7 KΩ pull-down resistor for TRST~. This resistor has been removed. This is to prevent the DSP JTAG TAP from being constantly in reset on targets which use a local boundary scan controller but do not drive TRST~.
20	This figure shows dimensions for the HPPCI JTAG emulator pod only.
21	This figure shows dimensions for the HPUSB and USB JTAG emulator pods only.

Table 4. Document Notations

Document History

Revision	Description
Rev 9 – October 18, 2004 by David M. Doyle	Major update. • Incremented revision code to Rev 9 due to revision system change • Removed all obsolete Legacy information. • Simplified and combined drawings and tables when possible • Re-wrote most sections in more concise format
Rev 2.6 – July 9, 2003 by David M. Doyle	Updated all document discussions for the TRST~ signal and JTAG Emulation header jumper requirements. Most sections of the document were affected. Change keep out clearance requirements for larger HPPCI pod.
Rev 2.5 – March 20, 2003 by David M. Doyle	Divided document into discussion of Legacy ICE products and our new HPPCI ICE product. Added HPPCI information.
Rev 2.4 – December 3, 2002 by David M. Doyle	Updated all sections and added timing information
Rev 2.3 – August 2001 by David M. Doyle	Update to power up sections
Rev 2.2 – March 2001 by David M. Doyle	Update to target connections

Rev 2.1 – August 2000 *by David M. Doyle*	Update to 2.5 logic
Rev 2.0 – February 2000 *by David M. Doyle*	General update
Rev 1.0 – December 1999 *by David M. Doyle*	Initial Release