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ADSP-2146x Board Design Guidelines for DDR2 Memory

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Introduction

Designing DSP-based systems with DDR2 (Double Data Rate 2) SDRAM memory devices is simpler than designing GP-based systems because the memory devices are expected to be board-mounted and are not assumed to be DIMM module interfaces.

The ADSP-2146x SHARC® processors family supports a 16-bit DDR2 interface operating at a maximum frequency of half the core clock. Thus, the ADSP-2146x maximum core speed of 450 MHz translates into 225 MHz (clock) and 450 MHz (data) for the DDR2 controller.

Given the above information, the following sections provide the guidelines for termination, layout, placement, and routing of DDR2 signals for ADSP-2146x based designs. Two separate and operational hardware platforms have been developed:

- The ADSP-2146x bring-up board (BUB), which is an Analog Devices-internal platform designed and developed for early silicon testing and debugging.
- The ADSP-21469 EZ-Board™ evaluation board, which is a general reference design for developers.

The majority of the guidelines provided in this document apply to all DDR2 customer designs. Some guidelines, however, refer specifically to the platform on which those guidelines were implemented.

Signal Grouping and Naming Conventions

The ADSP-2146x SHARC processors have been designed to interface with DDR2 memories operating at a maximum speed of 533 Mbits/sec. This document provides suggestions for PCB designers to consider while laying out high-speed DDR2 signals.

Table 1 shows the signal names and group descriptions for all associated DDR2 signals. It also shows board-level layout guidelines for signals within a particular group, as well as signals between different signal groups.

Spacing is listed as center-to-center distance in units of trace width W . In other words, $3W$ spacing is $2W$ trace separation.

Skew or trace length matching should be done within each group. Match all group A signals, match all group B signals, and match all group C signals.

Group	Skew Match Group	Signals	To each other if differential	To others in this group	To other DDR2 groups
Clock	A	DDR2_CLK0, /DDR2_CLK0, DDR2_CLK1, /DDR2_CLK1	100Ω differential impedance	4W	4W
Address and Control	A	DDR2_ADDR [15:0], DDR2_BA[2:0], DDR2CKE, /DDR2WE, /DDR2CAS, /DDR2RAS /DDR2_MS[3:0], ODT	N/A	3W	4W
Data	B	DQS0, /DQS0	Constant	4W	4W
Data	B	DDR2_DATA [7:0]	N/A	3W	4W
Data	B	DM0	N/A	4W	4W
Data	C	DQS1, /DQS1	Constant	4W	4W
Data	C	DDR2_DATA [15:8]	N/A	3W	4W
Data	C	DM1	N/A	4W	4W

Table 1. DDR2 signals and signal groups

General PCB Guidelines for DDR2 Signals

Several industry-standard PCB guidelines for DDR2 interfacing are enumerated below:

1. The ADSP-21469 processor's BGA package assists in laying out the DDR2 components on top and bottom of the board. So it's preferable to arrange this way to have a clean and efficient configuration with respect to the uniform routing trace length across the byte lanes.
2. Provide logic analyzer connectors for the DDR2 signals in the PCB for debugging, if possible.
3. If used, place series termination resistors close to the source driver (the processor in this case) for address and control signals. For data signals, place them close to the receivers (i.e., the DDR2 memory).
4. If used, place parallel termination resistors close to the receivers (DDR2 memory in this case) for address and control signals. For data

signals, place them close to the source driver (processor) because on-die termination (ODT) is not enabled by default.

5. Ensure that the distance from the series termination resistor to the source output driver is shorter in length than the distance from the series termination resistor to the load (DDR2 memory).

6. DDR2 clocks (DDR2_CLK0 and /DDR2_CLK0) and data strobes (DQS0, /DQS0, DQS1, and /DQS1) signals are differential. The two signals (true and complement) must be routed together with a resistor in series with a jumper between them placed close to the DDR2 memory.

7. The PCB trace characteristic impedance must be approximately 50 ohms.

8. While routing the DDR2 signals, try to maintain perpendicularity between adjacent layers. For example, horizontal and vertical adjacent layers are standard design practice to reduce crosstalk. Do not route signals on the top or bottom layers. Internal layers are necessary to

achieve 50 ohms characteristic impedance, and also in order to reduce crosstalk.

9. It is critical that all DDR2 signal routing layers have a ground reference plane, meaning that there is a full, contiguous ground plane next to every DDR2 routing layer. Two routing layers can share a ground plane (one signal layer above, and one signal layer below the ground plane). Ground plane cuts are not allowed in the DDR2 region (ground plane cuts are generally a bad idea, and should only be done very carefully, if absolutely necessary on other areas of the PCB). The ground plane provides a path for return currents to minimize crosstalk and EMI. Power planes cannot be used as signal returns for the DDR2 interface.

10. Ensure that the DDR2 memory device has been placed as close as possible to the DSP on the board.

11. The DDR2 keep-out region (area in the PCB solely for DDR2, its signals, and its interface circuitry) should encompass all DDR2 circuitry and will vary depending on placement. Non-DDR2 signals must not be routed on the DDR signal layers within the DDR2 keep-out region. Non-DDR2 signals may be routed in this region, provided they are routed on layers separated from DDR2 signal layers by a ground layer. No breaks shall be allowed in the reference ground layers in this region. In addition, the 1.8 V power plane should cover the entire keep-out region.

The following guidelines must be followed for laying out each net group on the board:

1. CLK (clock) and ADD_CTL (address and control) net group signals must be matched in length within 100 mils.
2. The signals in the CLK net group must be laid out as a differential pair. The trace separation between the differential pair of net group CLK should be such to maintain the desired differential impedance (100 ohms). Other traces should be kept away from the CLK signal group traces by at

least 4 W center to spacing (The PCB route trace width is defined as W for the purpose of defining minimum trace separation for the various signal groups. Therefore, if the PCB is designed with the widest possible traces, the trace width is $W = 4$ mils. If the PCB is designed with 3 mil traces/spaces, W would be 3 mils). Traces within the ADD_CTL net group should be spaced at least 3 W center-to-center from each other.

Traces of other net groups should be kept 4W away from the ADD_CTL net group as shown below.

3. The net groups that make up the two DQS and two DQ bytes must have the same routing rules. Note that the individual byte net groups do not have to be skew matched to each other. Skew matching is only required between the /DQn net group and its associated /DQSn net group.

/DQSn and /DQn nets are sourced by the processor during writes and are sourced by the DDR2 devices during reads. The DQS acts as the data strobe at it is always sourced with the DQ. For write cycles, the DQS transitions in the middle of the bits cells on DQ. For read cycles, the DQS transitions at the same time as the DQ. The interface is more sensitive to DQS <-> DQ crosstalk during reads. The data mask bits (DMn) are static during reads, thus they can be used as shields between the DQ and DQS to improve read crosstalk performance.

ADSP-21469 EZ-Board Design Specific Layout Rules

For detailed information on the DDR2 signals described below, refer to the ADSP-21469 EZ-Board schematic and layout files available for download from:

http://download.analog.com/tools/ezkit/ADSP-21469_EZ-Board_Design_Reference_Info.zip

In addition to the general layout guidelines previously enumerated, the following list of specific guidelines was used to lay out the ADSP-21469 EZ-Board evaluation board. While

customers are encouraged to follow the recommendations below, it may be that all recommendations are difficult to adhere to:

- All traces must be less than 1.1 inches.
- Length match the following signals to each other:
 - Lower data group (must be 10-15ps of each other):
 - DDR2_DATA[7:0], DDR2_DQS0 and /DDR2_DQS0 (they should also run parallel), DDR2_DM0
 - Upper data group (must be 10-15ps of each other):
 - DDR2_DATA[15:8], DDR2_DQS1 and /DDR2_DQS1 (they should also run parallel), DDR2_DM1
 - Address/Control group:
 - DDR2_DM1, DDR2_ADDR[15:0], DDR2_BA[2:0], /DDR2_RAS, /DDR2_CAS, /DDR2_WE, /DDR2_CS0, DDR2_ODT, DDR2_CKE
- Ensure that R193 is as close as possible to U13.J8 and U13.K8.
- DDR2_CLK0 and /DDR2_CLK0 should be laid out parallel to one another.
- Between two data groups there can be up to 50 ps difference, but it is recommended to keep them as minimal as possible.
- Try to keep all groups running on the same layers, if possible.
- Place R194, R195, C26, and C27 as close to U12.J2 as possible.

Board-Level Termination Recommendations

By default, the ability to turn on on-die termination (ODT) at the memory device is not enabled on the ADSP-2146x DDR2 memory controller. Also, memory manufacturer guidelines state that board-level net lengths of 2.5 inches or less do not require DDR2 end-of-line termination resistors, nor are Vtt tracking circuits required.

Customers are encouraged to perform thorough board-level simulations of their systems, in order to arrive at an optimal termination scheme. Analog Devices uses Mentor Graphics' HyperLynx® LineSim™ and BoardSim™ simulation tools to validate board designs. IBIS models for the various processors are provided on our web site for simulation purposes:

<http://www.analog.com/en/embedded-processing-dsp/SHARC/processors/mod-ibis-models/resources/index.html>

ADSP-21469 EZ-Board Termination Scheme

Due to strict layout guidelines followed on the ADSP-21469 EZ-Board evaluation board per the recommendations mentioned above, DDR2 signals on this board contain a 33 ohms series termination resistor on all DDR2 data, address, strobe, as well as control signals. The resistors are placed close to the source driver (processor).

The differential DDR2 clock signal pair (DDR2_CLK0 and /DDR2_CLK0) have been terminated with a 100 ohms parallel termination resistor between them, placed close to the receiver (DDR2 memory device).

Resistor-packs may also be used for termination options. In this case, it is recommended that the following combination of signals be grouped together as shown in Figure 1. Further, within address and data signals, it is advisable to group adjacent address lanes together to the same resistor pack, and group adjacent data lanes together on the same resistor-pack.

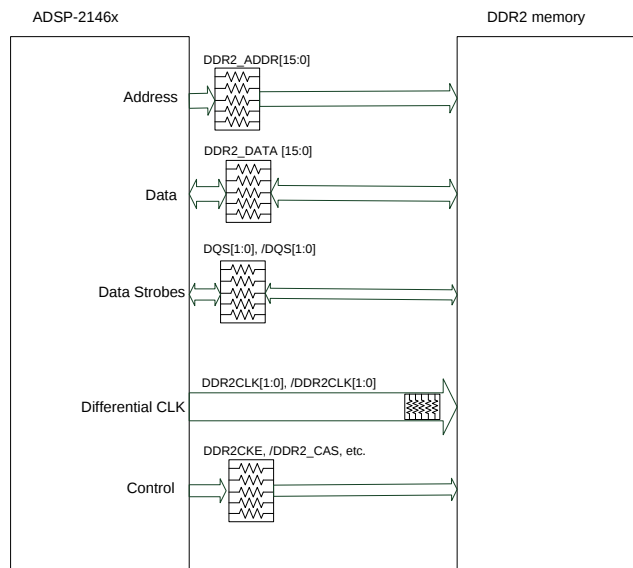


Figure 1. Using resistor-packs for termination

ADSP-21469 BUB Termination Scheme

The BUB design has more conservative termination options than the EZ-Board evaluation board. The termination scheme followed for BUB design includes 15 ohms series termination resistors placed close to the driver on all address, control, and clock signals, 33 ohms series termination resistors placed close to the driver on all data and strobe signals, and pull-up termination resistors to V_{tt} on all address and control signals. For more details, refer to the BUB DDR2 memory design schematics provided in the associated .ZIP file.

Bypass and Decoupling Capacitors for DDR2 Signals

Each bypass capacitor requires two vias: one for each pin. Via sharing for bypass capacitors is not permitted. This is due to the inductance of the vias. Via sharing compromises the performance of the bypass capacitor due to this inductance.

For the same reason, sharing of vias by power and ground pins of the processor or DDR2

devices is also not permitted. Vias used for bypass capacitor and device power connections are referred to as *power vias*. To minimize inductance, power vias should be as large as possible. Ensure that power vias are not so large as to inadvertently cut planes. Power vias should be connected to the device pads with the shortest possible traces that are as wide as possible.

Ideally, the trace length from the power via to the device pad should not exceed 30 mils. Maximum trace length from power via to bypass capacitor is 60 mils. Maximum trace length from power via to power ball pad is 35 mils. Placement of the mid-bulk bypass capacitors (10 uF) is not that critical, and they can be placed to accommodate other circuitry with more constrained placement and routing requirements.

Designers should ensure that trace length specifications are kept in mind when placing the bypass capacitors.

Bypass Capacitors by the Numbers for Power Supplies

Recommended bypass capacitor requirements are given in Table 2 for different supplies. This can be taken as a starting point and can be altered, depending on the performance.

The large 10uF capacitors serve to filter out low frequency noise and must be located close to the corresponding power pins. As for the smaller capacitors, which filter out high frequency noise, place as many of them as possible close to the processor.

Bypass Capacitor Recommended Quantities			
Power Supply	Quantity 10 uF	Quantity 0.1 uF	Quantity 0.01 uF
VDD_INT	2	24	16
VDD_EXT	2	24	16
VDD_DDR2	2	12	8
VDD_DDR2 (memory)	1	4	4

Table 2. Bypass capacitors

VREF Signal Considerations

Ensure that the VREF signal is routed with a wide trace (minimum of 20–25 mils recommended, and that VREF is isolated from noisy signals in its proximity. In addition, maintain at least a 20–25 mils clearance from VREF to other traces. If possible, isolate VREF from adjacent ground traces.

VREF signals must be properly decoupled. Each source and each destination pin must be decoupled with a 0.1 μ F capacitor. If a resistor divider network is used to generate VREF, ensure that both resistors have the same value and 1% tolerance.

Vtt Tracking Circuitry

Vtt tracking circuits have been omitted from the ADSP-21469 EZ-Board reference design due to memory manufacturer guidelines.

The ADSP-21469 BUB design uses National Semiconductor's LP2997 device to provide DDR2 voltage regulation, as per JEDEC DDR2 and SSTL-18 specifications. For detailed information, please refer to the DDR2 circuit schematics provided in the associated .ZIP file.

Power Supply Requirements

The board must provide different power supplies starting with core (VDD_INT: 1.10 V $\pm$ 10%), post-drivers of the LVCMOS interface (VDD_EXT: 3.3 V $\pm$ 10%), post-drivers of the DDR2 memory I/O interface (VDD_DDR2: 1.8 V $\pm$ 5%), reference supply for the DDR2 memory I/O receivers (VREF: 0.5 x VDD_EXT with a minimum of 0.49 x VDD_EXT and a maximum of 0.51 x VDD_EXT).

The reference supply can be drawn (through a resistor divider from two 1K ohms, 1% tolerance resistors) from the 1.8 V supply with a requirement of peak-to-peak AC noise on VREF

not exceeding $\pm$ 2% of VREF. It is not a high-current supply, but it is important to keep it as clean as possible, with minimal inductance. The minimal nominal trace width for VREF is 20 mils. Necking down VREF to accommodate BGA escapes and localized via congestion is acceptable, but keep it 20 mils wide as much as possible. It is a DC net and as such, trace delay is not critical; however, keep overall trace length to a minimum. The four or five bypass capacitors on the VREF net are intended to reduce AC noise.

Preliminary Results of Board-Level Simulations

As part of the initial design process, pad and layout files of the ADSP-2146x BUB and EZ-Board platforms were fed into the Mentor Graphics' HyperLynx LineSim™/BoardSim simulation package. The overshoot/undershoot as well as timing diagrams were calculated with different drive-strength as well as series termination resistor values. The results were determined to be within the bounds of design recommendations and JEDEC requirements.

The following figures show an example of one particular signal (/DDR2_CAS). [Figure 2](#) shows one layer of the board as observed by BoardSim. [Figure 3](#) shows just the signal of interest, /DDR2_CAS. The corresponding net for this signal can be extracted and exported to LineSim in the form of a free-form schematic model. [Figure 4](#) shows the HyperLynx LineSim model for this particular signal. Using this model, not only can the individual signal be simulated and observed (as shown in [Figure 5](#)) but also parameters such as termination resistor values, as well as where they are placed, can easily be modified and simulations re-run, to compare results.

ADSP-21469 IBIS models required to run these simulations, as well as DDR2 memory devices (such as the Micron MT47H64M16 used in these simulations) can be readily obtained on the web.

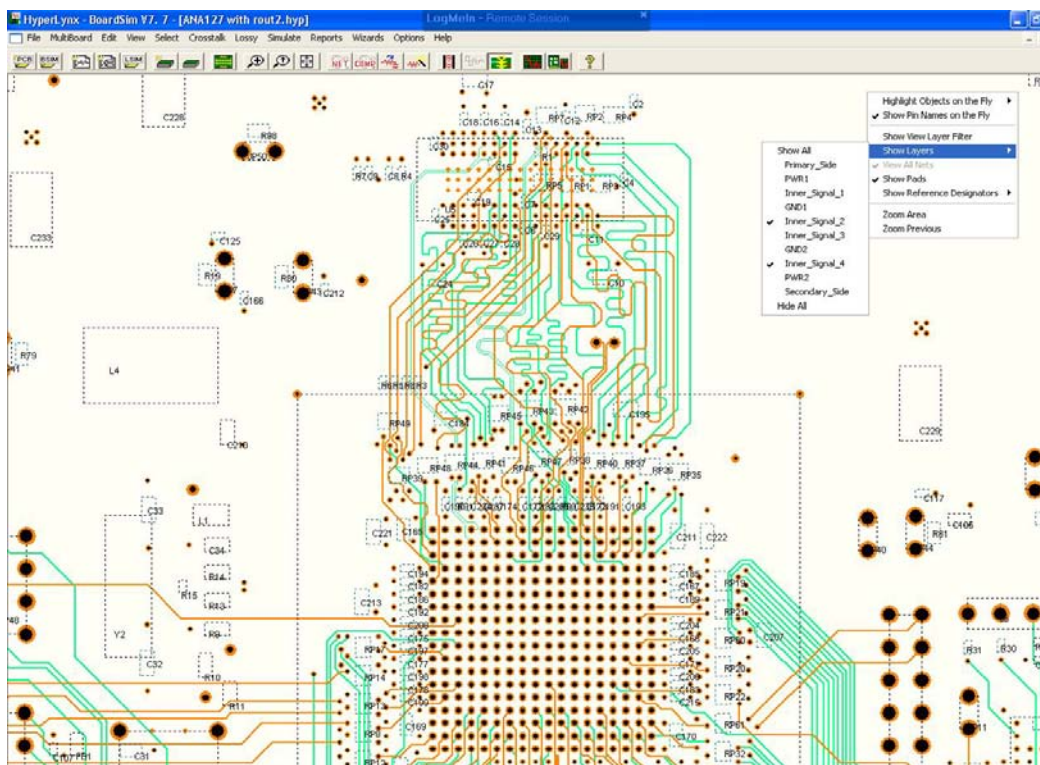


Figure 2. BoardSim slice of ADSP-21469 BUB layer showing layout of DDR2 signals

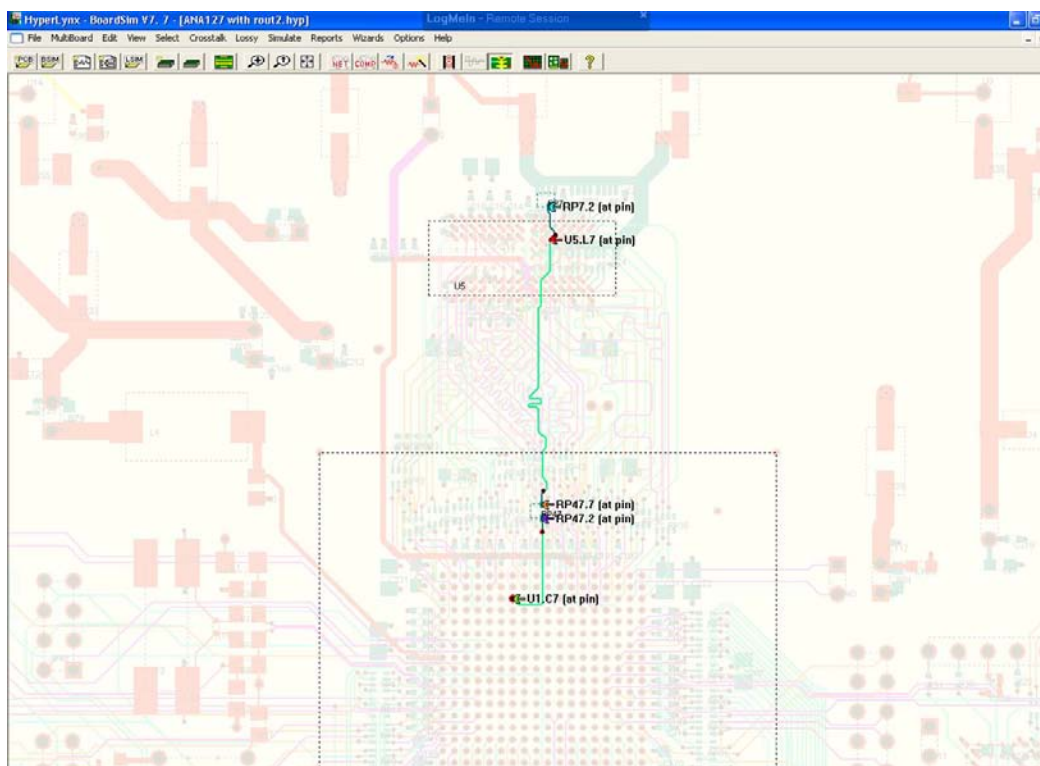


Figure 3. BoardSim view of /DDR2_CAS signal

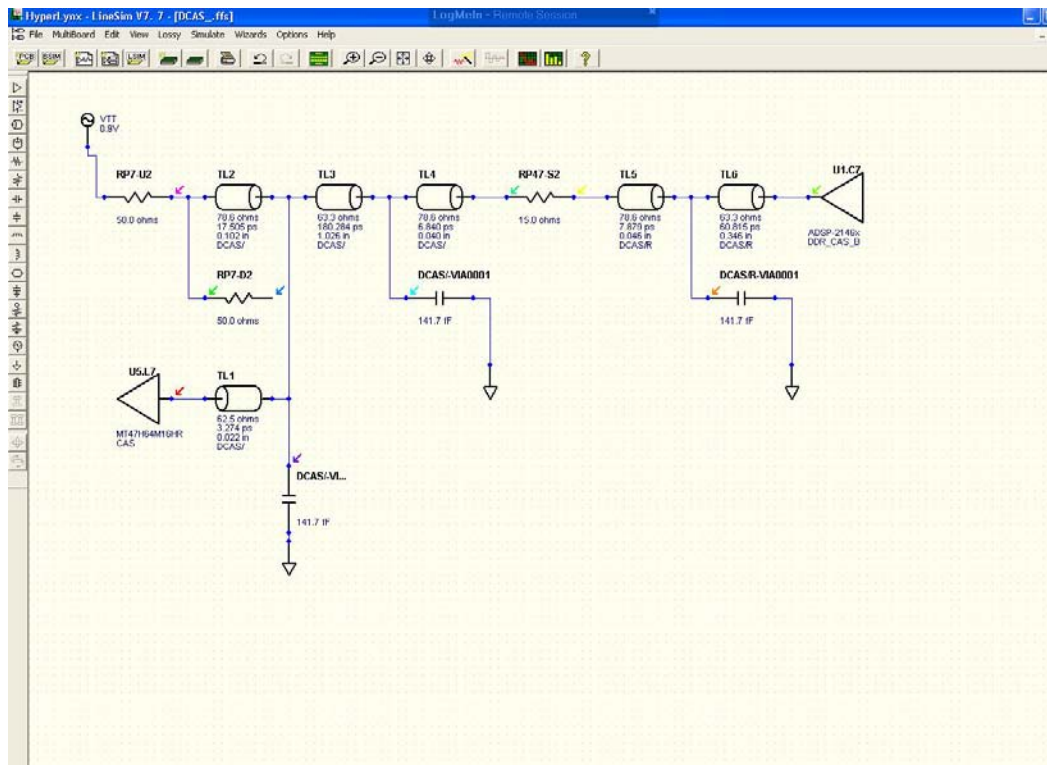


Figure 4. HyperLynx LineSim model of /DDR2_CAS

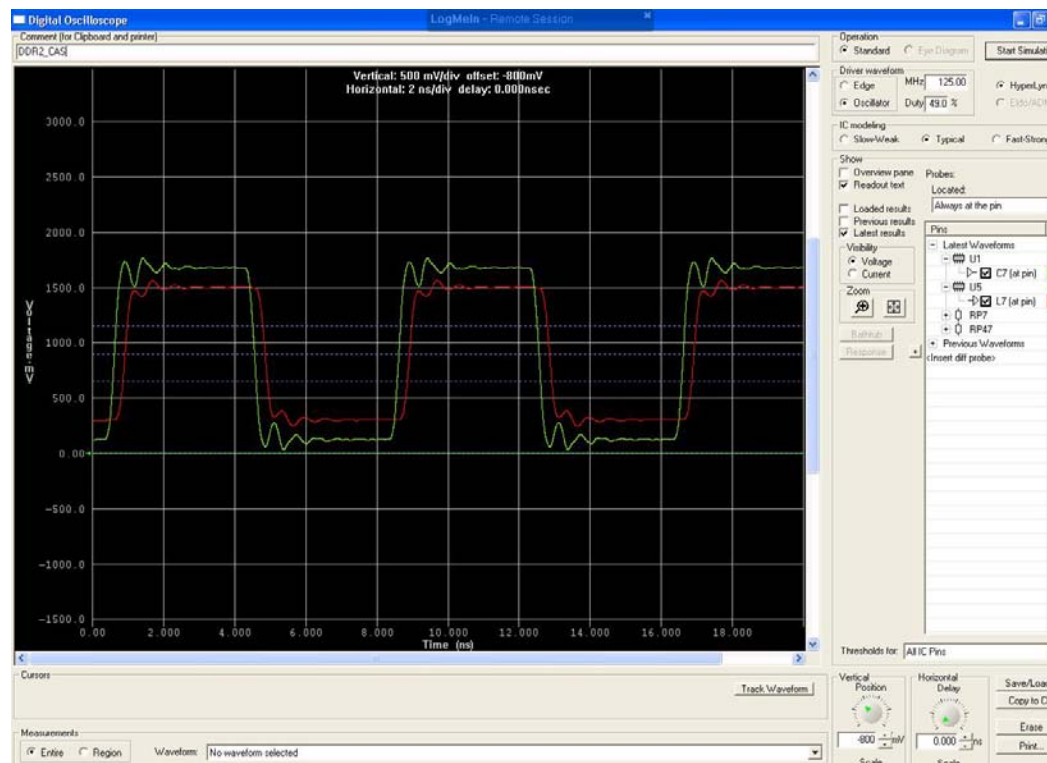


Figure 5. LineSim simulations of DDR2_CAS signal

Figure 6 and Figure 7 compare signals observed using HyperLynx simulations versus actual board-level measurements taken on an Agilent Technology oscilloscope. This exercise was performed to determine how accurately the signals were modeled by HyperLynx. As can be seen, the models appear to be quite close in shape to the actual measured signal. We estimate that some of the high-frequency components are not observed on the simulations owing to frequency limitations in the tools versions that were used.

Note that all measurements were taken at the memory (Micron DDR2 part number MT47H64M16) of the ADSP-21469 BUB design, using Agilent Technology Infinium® 9000 series oscilloscopes connected via W2639A flex wing scope adapter board connectors and W2631A DDR2 BGA probes.

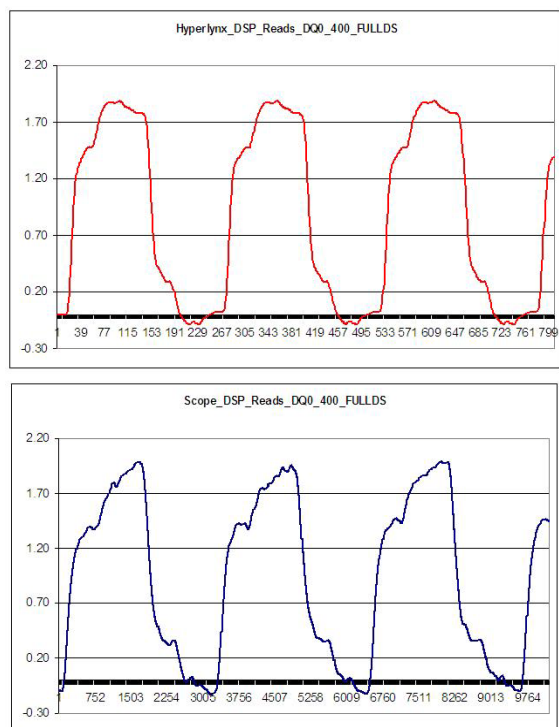


Figure 6. Simulated (top) and measured (bottom) waveform of DDR2_DQ0 signal under maximum drive strength

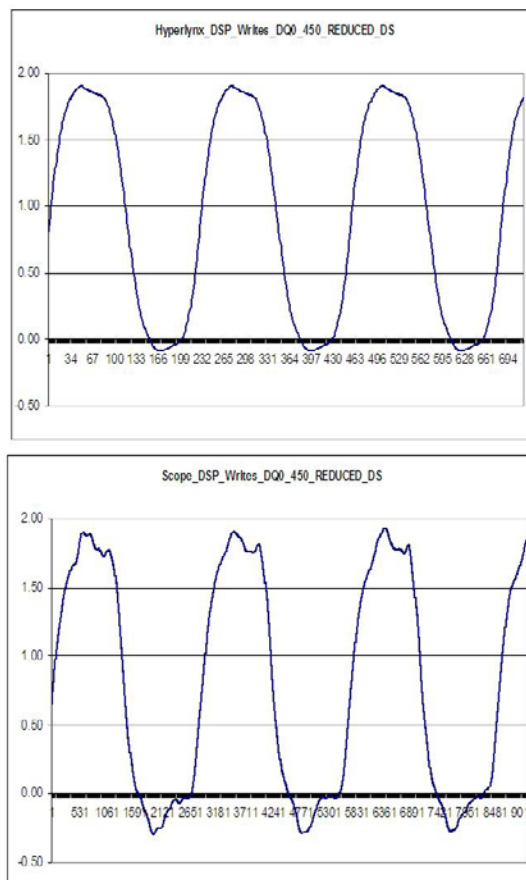


Figure 7. Simulated (top) and measured (bottom) waveform of DDR2_DQ0 signal under reduced drive strength

Eye Diagrams

The following section contains scope snapshots of data eye diagrams taken with maximum-strength (default setting) as well as reduced-strength drive settings on the DDR2 controller, as well as with ODT (on-die-termination) set to different values (disabled/default setting, 50, 75, and 150 ohms). For each set of measurements taken at a particular drive strength setting and ODT status, the vertical and horizontal scales were kept unchanged.

Note that the measurements were taken on a board at room temperature, and are representative of a typical device. Results may vary from part to part.

Also, the board-level termination settings were not modified for each measurement. The measurements are provided strictly for illustration purposes, and board designers are strongly encouraged to model their specific systems and select the best possible drive strength settings and corresponding termination schemes to suit their particular needs.

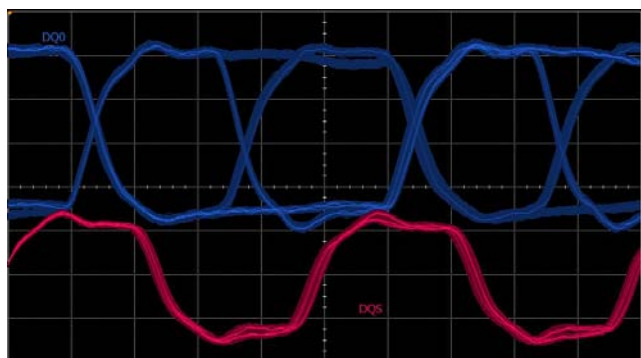


Figure 8. Data_Eye_WR_ODTDIS_redDS

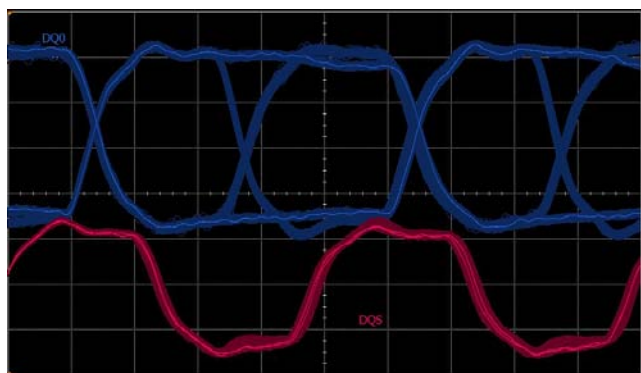


Figure 9. Data_Eye_WR_ODTDIS_maxDS

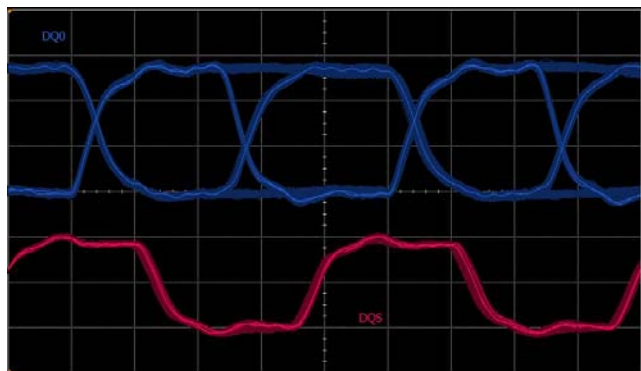


Figure 10. Data_Eye_WR_ODT150_redDS

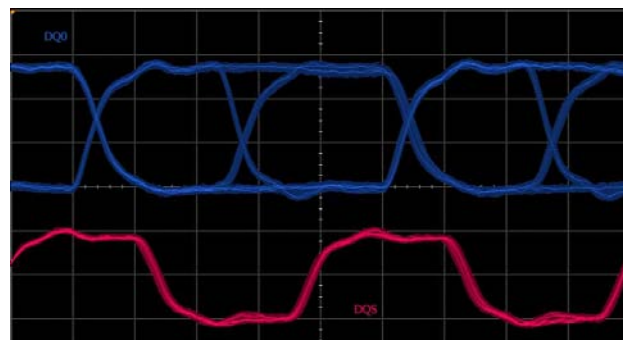


Figure 11. Data_Eye_WR_ODT_150_maxDS

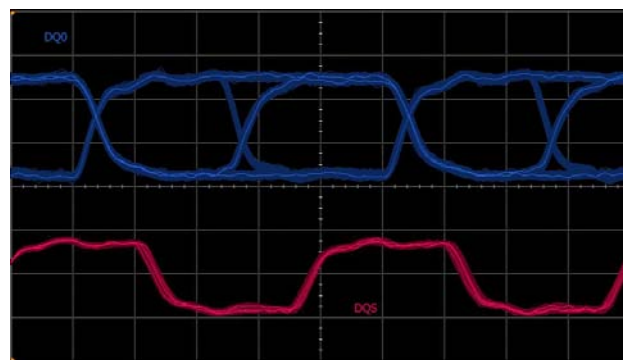


Figure 12. Data_Eye_WR_ODT75_redDS

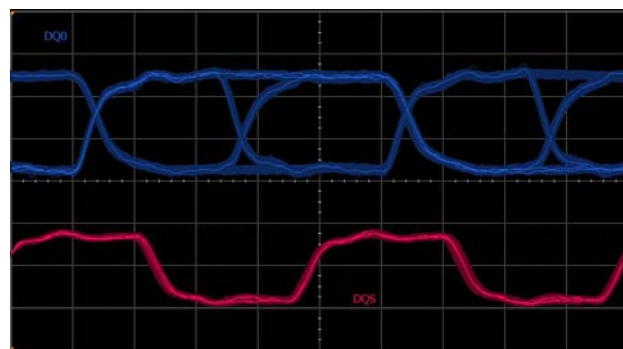


Figure 13. Data_Eye_WR_ODT75_maxDS

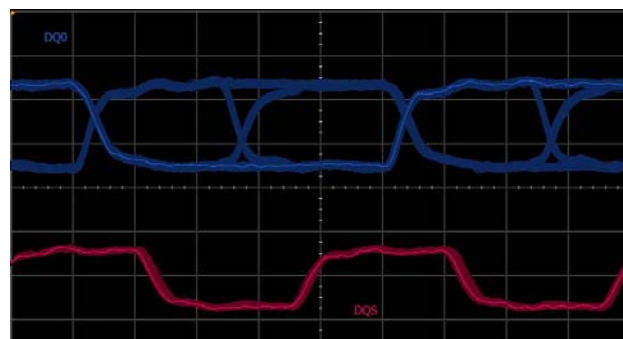


Figure 14. Data_Eye_WR_ODT50_redDS

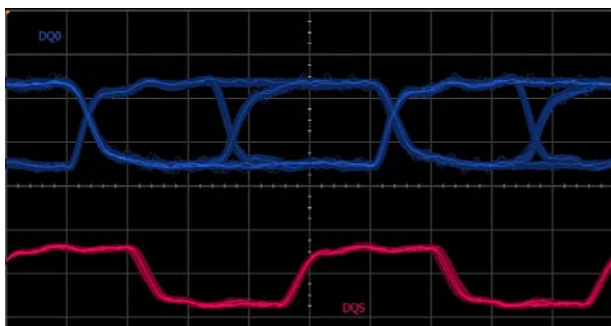


Figure 15. Data_Eye_WR_ODT50_maxDS

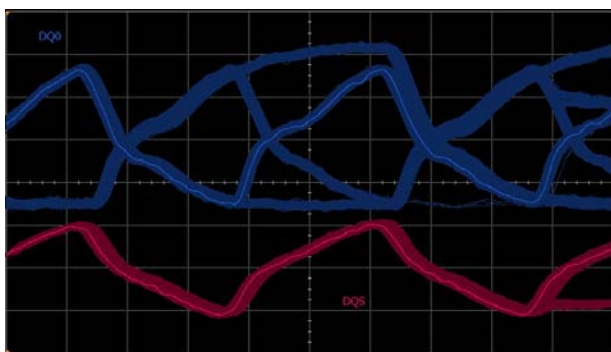


Figure 16. Data_Eye_RD_ODTDIS_redDS

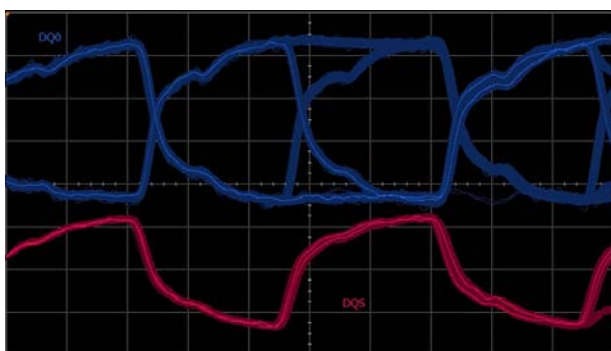


Figure 17. Data_Eye_RD_ODTDIS_maxDS

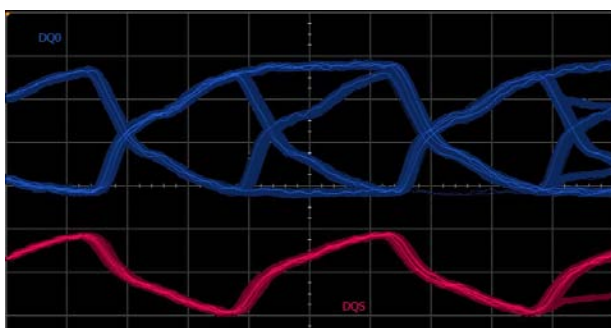


Figure 18. Data_Eye_RD_ODT150_redDS

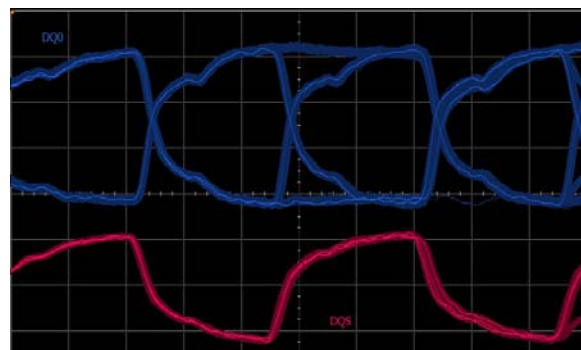


Figure 19. Data_Eye_RD_ODT150_maxDS

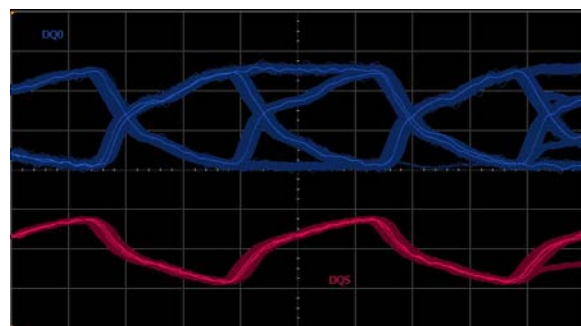


Figure 20. Data_Eye_RD_ODT75_redDS

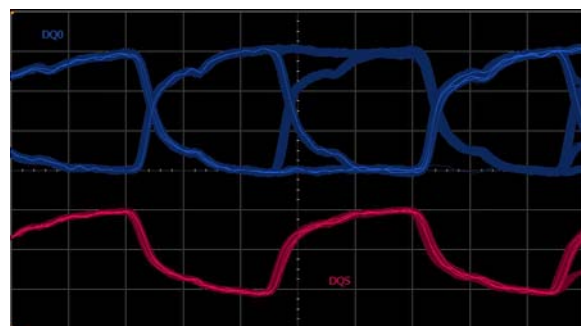


Figure 21. Data_Eye_RD_ODT75_maxDS

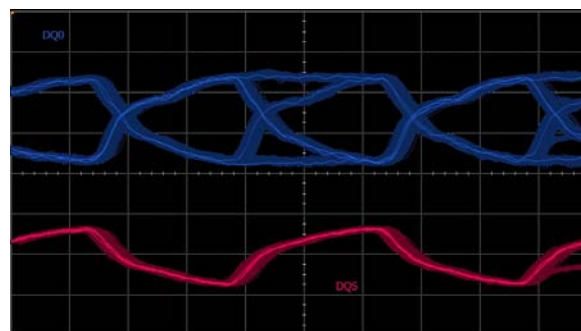


Figure 22. Data_Eye_RD_ODT50_redDS

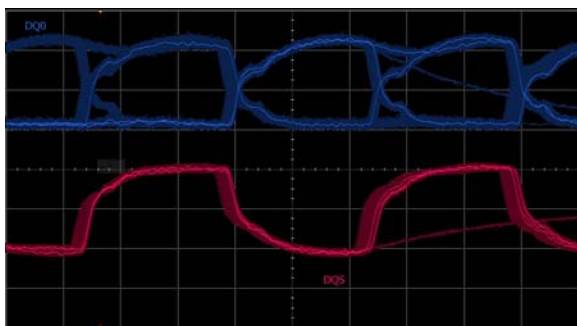


Figure 23. Data_Eye_RD_ODT50_maxDS

Full and Reduced Drive Strength Settings for DDR2 Signals

When a user sets (or clears) the OPDS bit in the DDR2CTL3 register, the drive strengths of DDR2 data and strobe pins will be driven at reduced

(or full) strength, respectively. By default, the bit is cleared (i.e., full drive strength).

However, drive strengths of address, control, and differential clock signals, which are outputs from the controller are not affected.

DDR2 JEDEC Compliance Testing

In addition to visual measurements and inspections of DDR2 signals, such as AC and DC parameters, as well as overshoot and undershoot measurement and extensive simulations, controller timing was proven to be within JEDEC specified limits by use of Agilent Technology's N5413A Automated DDR2 Compliance Test Application running on the scope.

Summary of Results

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✓	0	1	Input signal minimum rising slew rate, SLEW _r	2.658160V/ns	165.8 %	VALUE >= 1.000000V/ns
✓	0	1	Input signal minimum falling slew rate, SLEW _f	3.150996V/ns	215.1 %	VALUE >= 1.000000V/ns
✓	0	1	Maximum AC Input Logic High, V _{IH} (ac)	1.772000V	45.9 %	1.150000V <= VALUE <= 2.300000V
✓	0	1	Minimum DC Input Logic High, V _{IH} (dc)	1.782000V	29.6 %	1.025000V <= VALUE <= 2.100000V
✓	0	1	Minimum AC Input Logic Low, V _{IL} (ac)	-107.0000mV	34.2 %	-500.0000mV <= VALUE <= 650.0000mV
✓	0	1	Maximum DC Input Logic Low, V _{IL} (dc)	-4.000000mV	27.5 %	-300.0000mV <= VALUE <= 775.0000mV
✓	0	1	Overshoot amplitude (Address, Control)	104.0000mV	79.2 %	VALUE <= 500.0000mV
✓	0	1	Overshoot area (Address, Control)	48pV-ns	100.0 %	VALUE <= 1.330000V-ns
✓	0	1	Undershoot amplitude (Address, Control)	-75.0000mV	85.0 %	VALUE >= -500.0000mV
✓	0	1	Undershoot area (Address, Control)	0.000000V-ns	100.0 %	VALUE <= 1.330000V-ns
✓	0	1	Overshoot amplitude (Clock, Data, Strobe, Mask)	100.0000mV	80.0 %	VALUE <= 500.0000mV
✓	0	1	Overshoot area (Clock, Data, Strobe, Mask)	18pV-ns	100.0 %	VALUE <= 380.0000mV-ns
✓	0	1	Undershoot amplitude (Clock, Data, Strobe, Mask)	-219.0000mV	56.2 %	VALUE >= -500.0000mV
✓	0	1	Undershoot area (Clock, Data, Strobe, Mask)	0.000000V-ns	100.0 %	VALUE <= 380.0000mV-ns

DDR2 Test Report

Overall Results: 0 of 14 Tests Failed

Test Configuration Details	
Device Description	
Speed Grade	DDR2-400
Test Mode	Compliance
Test Session Details	
Infimium SW Version	02.01.0000
Infimium Model Number	DSO91304A
Infimium Serial Number	MY47481362
Application SW Version	2.39.9054
Compliance Limits (official)	DDR2-400 Test Limit
Last Test Date	11/30/2009 5:06:20 PM

Figure 24. Snapshot of automated report generated by Agilent Technology N5413A application

Conclusion

The recommendations and results presented in this EE-Note have been tested and shown to work. Board designers are encouraged to follow these guidelines while laying out and designing their PCB. Although other techniques may work equally well, a thorough analysis including signal and board-level simulations are required to ensure that the design is robust.

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Document History

Revision	Description
<i>Rev 2 – September 29, 2010 by Ramdas Chary</i>	Corrected multiple instances of “millimeters” to “mils”.
<i>Rev 1 – May 27, 2010 by Ramdas Chary</i>	Initial release.