



AD9887 Versus AD9887A Design Considerations

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REGISTER DIFFERENCES

Registers 00h to 1Ch are identical in the AD9887 and the AD9887A. Additional bit definitions for the AD9887A are as follows:

Register	Bit	Bit Name	Bit Description
1D	6	HDCP Key Detect (read only)	0 = Key Not Detect, 1 = Key Detect
20	7	HDCP Address	Sets Bit 0 of HDCP Slave Port Address
20	6	Pin 49 Function Select	0 = Pin 49 is CTL3 for DVI (not yet defined), 1 = Pin 49 is MCL for HDCP
20	4	MDA/MCL Three-State	0 = MDA, MCL Three-States, 1 = MDA, MCL Normal

SOFTWARE CHANGES

In addition to the register definitions above, there are some register changes that should be made to optimize the performance of both the analog and DVI interfaces. These are described in the following table:

Register	Bit	Description	AD9887 Value	AD9887A Value
0x03	6:2	VCO Range, CP Current	See Table VII in Data Sheet (or use the PLL Settings Calculator Spreadsheet)	See Table VII in Data Sheet (or use the PLL Settings Calculator Spreadsheet)
0x1C	7:3	Test Bits	01101	00000
0x1E	7:0	Test Bits		0xFF
0x1F	7:0	Test Bits		0x84
0x21	7:0	Test Bits		0x00
0x22	7:0	Test Bits		0x00
0x23	7:0	Test Bits		0x00
0x24	7:0	Test Bits		0x00
0x25	7:0	Test Bits		0xF0
0x26	7:0	Test Bits		0xFF

PCB CONSIDERATIONS FOR COMPATIBILITY

The definitions for Pins 49, 71, 72, and 73 have changed from the AD9887 to the AD9887A. However, since these pins are not used on the AD9887, with proper layout there should be no problem converting to the AD9887A without making changes to the PCB. These pins should be left as no connects for the AD9887 (CTL3, Pin 49, is currently undefined by the DVI specification). If HDCP is to be implemented for the AD9887A design, these pins must be connected as described in the AD9887A Data Sheet. This will not affect the operation of the AD9887.

PERFORMANCE DIFFERENCES

The AD9887A's analog interface is designed to operate up to 170 MHz (140 MHz for the AD9887). The AD9887A's DVI interface is designed for 165 MHz operation (112 MHz for the AD9887). The AD9887A's input bandwidth is 500 MHz (330 MHz for the AD9887). Some specifications (such as power dissipation and PLL jitter) of the AD9887A have changed somewhat from the AD9887. Refer to the latest AD9887A Data Sheet for details.