ANALOG DEVICES

AN-117
APPLICATION NOTE

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OP-42 Advanced SPICE Macro-Model

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INTRODUCTION

This application note describes the SPICE macro-model for the OP-42 high-speed, fast-settling precision operational amplifier. This model was tested with, and is compatible with PSpice* and HSPICE**. The schematic and net-list are included here so that the model can easily be used. This model can accommodate multiple frequency poles and multiple zeroes, which is an advanced concept that results in more accurate AC and transient responses necessary for simulating the behavior of today's high-speed op amps. For example, 8 poles and 2 zeroes are required to sufficiently simulate the OP-42, which this advanced model can easily accommodate.

Throughout the OP-42 macro-model, RC networks produce the multiple poles and zeroes which simulate the OP-42's AC behavior. Each stage contains a pole or a pole-zero pair. The stages are separated from each other by voltage-controlled current sources so that the pole and zero locations do not interact. The only nonlinear elements in the entire model are two p-channel JFETs which comprise the input stage. Limiting the model to almost entirely linear circuit elements significantly reduces simulation time and simplifies model development.

MODEL DESCRIPTION

The schematic (Figure 1) and net-list (Figure 2) describe the complete OP-42 model. This model breaks up the OP-42 into many distinct stages as described below:

INPUT STAGE

To correctly model the behavior of the OP-42, the model uses a differential pair of p-channel JFETs biased with a 1mA current source (Figure 1a). To keep this stage as simple as possible only those parameters necessary to the JFET model are specified, that is the threshold voltage VTO, the transconductance coefficient BETA, and the gate p-n saturation current IS, which is scaled to give the proper input bias current. All other JFET parameters are left at the model default values, most of which are zero.

As for non-ideal behaviors of the input stage, such as V_{OS}, I_{OS}, and C_{IN}, these are modelled with external circuit elements. For example, no gate capacitance is specified for the JFET model, therefore a capacitor, C_{IN}, is added across the inputs. Furthermore, since in this model the input JFETs are perfectly matched, V_{OS} and I_{OS} error sources are added using an external voltage source and current source, respectively. Lastly, the drain resistors R_3 and R_4 are chosen to be 1/gm of the JFETs to give a gain of unity in the input stage. C_2 is added to create one of the secondary poles in the model.

GAIN STAGE

The open-loop gain of the OP-42 is achieved entirely in the gain stage (Figure 1b), and all other stages have unity gain. The two voltage-controlled current sources, G_1 and G_2, have scaled transconductances that, when combined with R_5 and R_6, yield an open-loop gain of 250,000. This stage also uses C_3 and C_4 to create the dominant pole at 45Hz and to model the amplifier slew rate. Lastly, the diodes, D_1 and D_2, and voltage sources V_2 and V_3, are necessary to clamp the voltage of node 9 below the power supplies. Because the next stage (Figure 1c) has unity gain and its voltage-controlled current sources are controlled by node 9, it too is clamped, at node 11, below the power supplies. The same is true for the subsequent stages, including the output at node 32, such that their voltages are clamped below the power supplies.

POLE-ZERO STAGES

All of the pole-zero stages (Figures 1c-g, i) have unity gain, which is a result of the gm of the voltage-controlled current sources being the reciprocal of the resistors. The RC networks are used to model the secondary poles and zeroes of the OP-42.

COMMON-MODE STAGE

The common-mode voltage that is used to create the CM error is created by the two input resistors, R_1 and R_2. This voltage is referenced by G_{13} and G_{14} in the common-mode stage (Figure 1h). The transconductances of these two sources are scaled such that, in combination with R_{21} and R_{22}, the V_{CM} is attenuated by the CMRR of 96dB. This error voltage is then inserted as an offset voltage in the input stage by E_{OS}. The inductors, L_1 and L_2, mimic the pole in the CMR vs. frequency response of the OP-42.

OUTPUT STAGE

The output stage (Figure 1j) is modelled as an ideal output with an output resistance, R_{28} in parallel with R_{29}. An inductor, L_3, is added to model the rising output impedance of the emitter-follower output stage with frequency. The voltage sources V_6 and V_7, and diodes D_5 and D_6, combine to limit the voltage across the resistors, thus limiting the output current, I_{OUT} to 30mA.

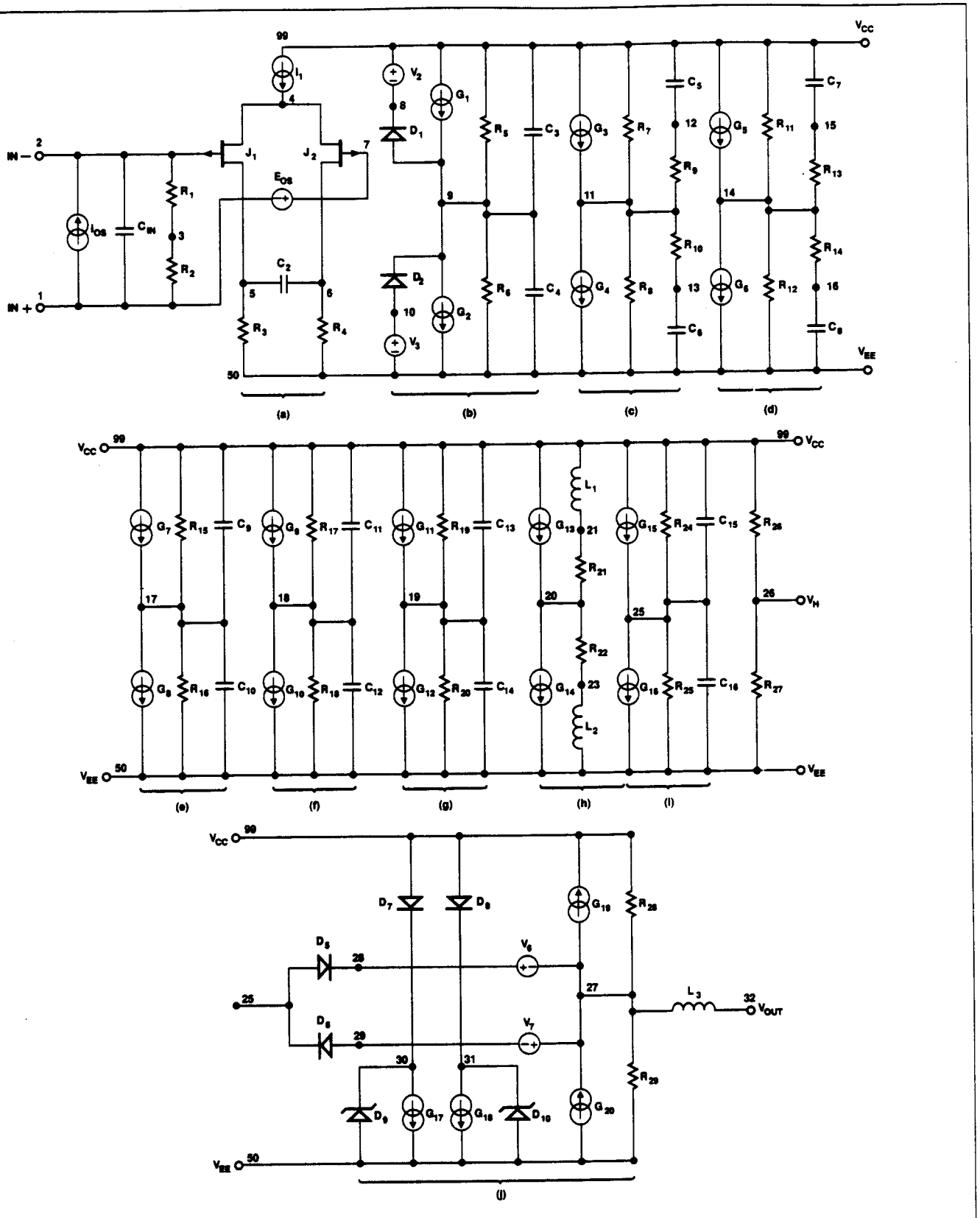

FIGURE 1: *OP-42 SPICE Macro-Model Schematic and Node List*

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OP-42 MACRO-MODEL © PMI 1989
*
* SUBCKT OP-42 1  2 99 50 32
*
* INPUT STAGE & POLE AT 15.9 MHZ
*
R1    2   3        5E11
R2    1   3        5E11
R3    5   50       707.36
R4    6   50       707.36
CIN   1   2        5E-12
C2    5   6        7.08E-12
I1    99  4        1E-3
IOS   1   2        2E-12
EOS   7   1        POLY(1) 20 26 0.3E-3 1
J1    5   2   4    JX
J2    6   7   4    JX
*
* SECOND STAGE & POLE AT 45 HZ
*
R5    9   99       176.84E6
R6    9   50       176.84E6
C3    9   99       20E-12
C4    9   50       20E-12
G1    99  9        POLY(1) 5 6 3.96E-3 1.4137E-3
G2    9   50       POLY(1) 6 5 3.96E-3 1.4137E-3
V2    99  8        2.5
V3    10  50       3.1
D1    9   8        DX
D2    10  9        DX
*
* POLE-ZERO PAIR AT 1.80 MHZ/2.20 MHZ
*
R7    11  99       1E6
R8    11  50       1E6
R9    11  12       4.5E6
R10   11  13       4.5E6
C5    12  99       16.1E-15
C6    13  50       16.1E-15
G3    99  11       9  26  1E-6
G4    11  50       26  9  1E-6
*
* POLE-ZERO PAIR AT 1.80 MHZ/2.20 MHZ
*
R11   14  99       1E6
R12   14  50       1E6
R13   14  15       4.5E6
R14   14  16       4.5E6
C7    15  99       16.1E-15
C8    16  50       16.1E-15
G5    99  14       11 26 1E-6
G6    14  50       26 11 1E-6
*
* POLE AT 53 MHZ
*
R15   17  99       1E6
R16   17  50       1E6
C9    17  99       3E-15
C10   17  50       3E-15
G7    99  17       14 26 1E-6
G8    17  50       26 14 1E-6
*
* POLE  AT 53 MHZ
*
R17   18  99       1E6
R18   18  50       1E6
C11   18  99       3E-15
C12   18  50       3E-15
G9    99  18       17 26 1E-6
G10   18  50       26 17 1E-6
*
* POLE AT 53 MHZ
*
R19   19  99       1E6
R20   19  50       1E6
C13   19  99       3E-15
C14   19  50       3E-15
G11   99  19       18 26 1E-6
G12   19  50       26 18 1E-6
*
*COMMON-MODE GAIN NETWORK WITH ZERO AT 100 KHZ
*
R21   20  21       1E6
R22   20  23       1E6
L1    21  99       1.5915
L2    23  50       1.5915
G13   99  20       3  26 1.58E-11
G14   20  50       26  3 1.58E-11
*
*POLE AT 79.6 MHZ
*
R24   25  99       1E6
R25   25  50       1E6
C15   25  99       2E-15
C16   25  50       2E-15
G15   99  25       19 26 1E-6
G16   25  50       26 19 1E-6
*
*OUTPUT STAGE
*
R26   26  99       111.1E3
R27   26  50       111.1E3
R28   27  99       90
R29   27  50       90
L3    27  32       2.5E-7
G17   30  50       25 27 11.1111E-3
G18   31  50       27 25 11.1111E-3
G19   27  99       99 25 11.1111E-3
G20   50  27       25 50 11.1111E-3
V6    28  27       0.7
V7    27  29       0.7
D5    25  28       DX
D6    29  25       DX
D7    99  30       DX
D8    99  31       DX
D9    50  30       DY
D10   50  31       DY
*
* MODELS USED
*
.MODEL JX PJF(BETA=999.3E-6 VTO=-2.000 IS=8E-11)
.MODEL DX   D(IS=1E-15)
.MODEL DY   D(IS=1E-15 BV=50)
.ENDS OP-42
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FIGURE 2: *OP-42 SPICE Net-List*

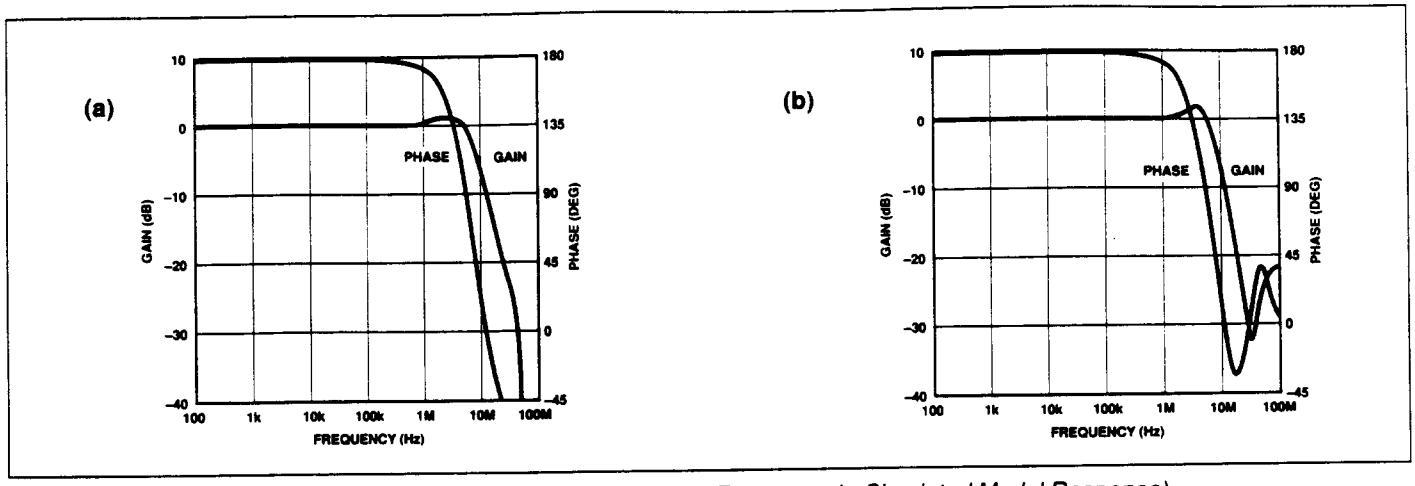

FIGURE 4: *Gain-Phase Plots, Closed-Loop Gain of –1 (a. Actual Response, b. Simulated Model Response)*

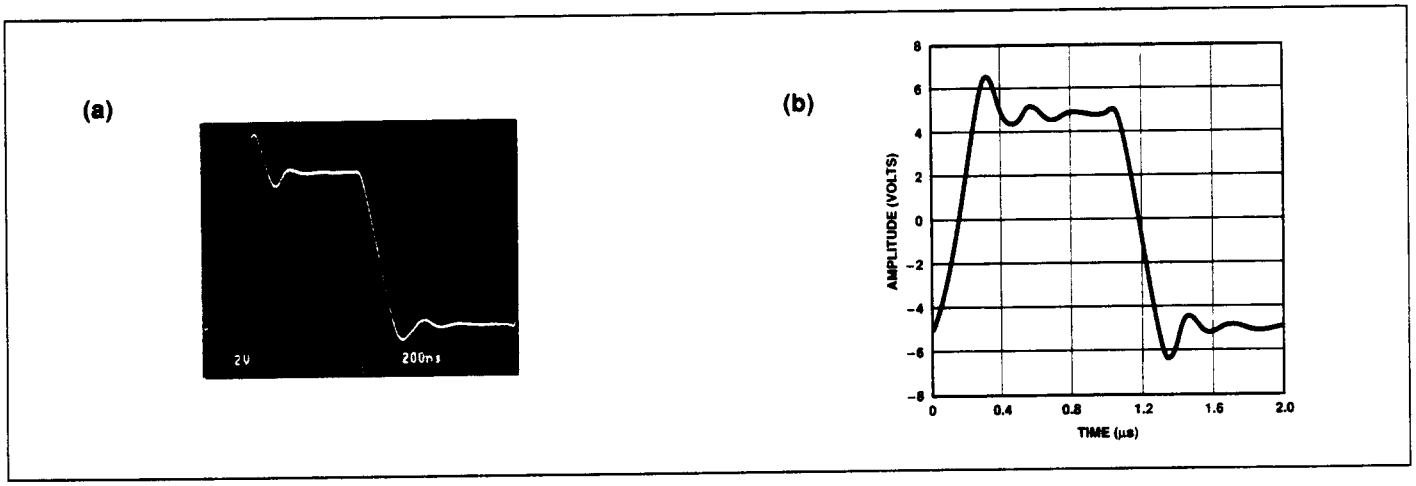

FIGURE 5: *Large-Signal Transient Response (a. Actual, b. Model)*

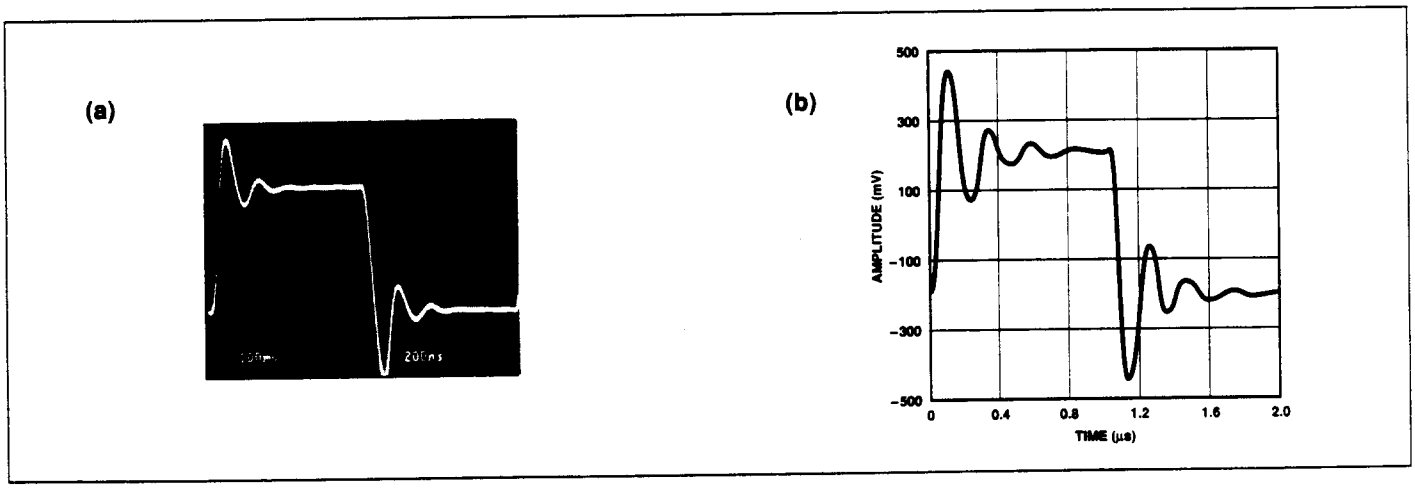

FIGURE 6: *Small-Signal Transient Response (a. Actual, b. Model)*