



# 3-Channel Digital Potentiometer with Nonvolatile Memory

## Preliminary Technical Data

## ADN2860

### FEATURES

**3 Channels: Dual 512-Position Single 128-Position**  
**25K $\Omega$  or 150K $\Omega$  Full-Scale Resistance**  
**Low Temperature Coefficient: 35ppm/ $^{\circ}$ C**  
**Nonvolatile Memory Retains Wiper Settings**  
**Permanent Memory Write-Protection**  
**Linear Increment/Decrement**  
**Log taper Increment/Decrement**  
**I $^2$ C Compatible Serial Interface**  
**3V to 5V Single Supply Operation**  
 **$\pm$ 2.5V Dual Supply Operation**  
**256 Bytes General Purpose User EEPROM**  
**11 Bytes RDAC user EEPROM**  
**GBIC and SFP Compliant EEPROM**  
**100-year Typical Data Retention at TA=55 $^{\circ}$ C**

### APPLICATIONS

**Laser Diode Drivers**  
**Optical Amplifiers**  
**TIA Gain Setting**  
**TEC Controller Temperature Set Points**

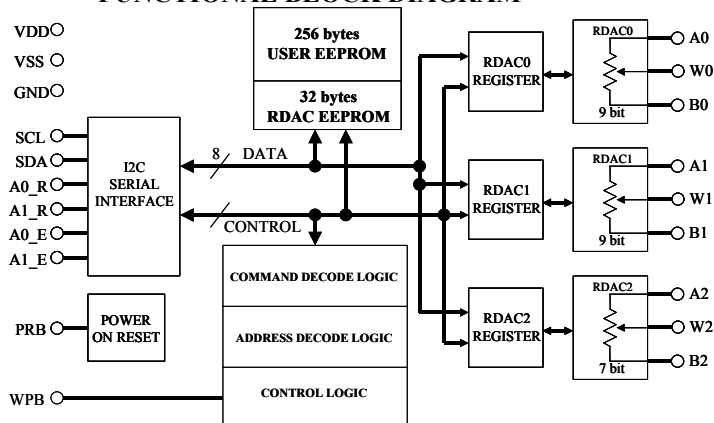
### GENERAL DESCRIPTION

The ADN2860 provides dual 512-position and a single 128-position digitally controlled variable resistor<sup>1</sup> (VR) in a single 4x4mm LFCSP package. This device performs the same electronic adjustment function as a potentiometer, trimmer, or variable resistor. Each VR offers a completely programmable value of resistance between the A terminal and the Wiper or the B terminal and the Wiper. The fixed A-to-B terminal resistance of 25k $\Omega$  or 250k $\Omega$  has a 1% channel-to-channel matching tolerance and a nominal temperature coefficient of 35ppm/ $^{\circ}$ C.

Wiper position programming, EEPROM reading, and EEPROM writing is conducted via the standard 2-wire I $^2$ C interface. Previous/Default wiper position settings can be stored in memory, and refreshed upon system power-up.

Additional features of the ADN2860 include preprogrammed linear and logarithmic increment/decrement wiper changing, and actual resistor tolerances are stored in EEPROM so that the

### FUNCTIONAL BLOCK DIAGRAM



actual end-to-end resistance is known, which is valuable for calibration in precision applications.

The ADN2860 EEPROM, channel resolution, and package size conforms to GBIC and SFP specifications. The ADN2860 is available in a 4x4mm 24-lead LFCSP package. All parts are guaranteed to operate over the extended industrial temperature range of -40 $^{\circ}$ C to 85 $^{\circ}$ C.

1. The term nonvolatile memory, EEMEM, and EEPROM are used interchangeably.
2. The term programmable resistor, variable resistor, RDAC, and digital potentiometer are used interchangeably.

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## ADN2860 ELECTRICAL CHARACTERISTICS 25k, 250k VERSIONS

( $V_{DD} = 3V$  to  $5.5V$  and  $-40^{\circ}C < T_A < +85^{\circ}C$ , unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE (Specifications apply to all RDACs)						
Resistor Differential Nonlinearity <sup>2</sup>	R-DNL	$R_{WB}$	-2		+2	LSB
Resistor Integral Nonlinearity <sup>2</sup>	R-INL	$R_{WB}$	-4		+4	LSB
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$			35		ppm/ $^{\circ}C$
Wiper Resistance	$R_W$	$V_{DD} = +5V$ , $I_W = 1V/R_{WB}$		70	100	$\Omega$
		$V_{DD} = +3V$ , $I_W = 1V/R_{WB}$		200		$\Omega$
Channel Resistance Matching	$\Delta R_{WB}/R_{WB}$	Ch 1 and 2 $R_{WB}$ , $Dx = 3FF_H$		0.1		%
Nominal Resistor tolerance	$\Delta R_{WB}$	$Dx = 3FF_H$	-30		30	%
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE Specifications apply to all VRs						
Differential Nonlinearity <sup>3</sup>	DNL		-2		+2	LSB
Integral Nonlinearity <sup>3</sup>	INL		-4		+4	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = Half-scale		15		ppm/ $^{\circ}C$
Full-Scale Error	$V_{WFSE}$	Code = Full-scale	-1.5		0	LSB
Zero-Scale Error	$V_{WZSE}$	Code = Zero-scale	0		+1.5	LSB
RESISTOR TERMINALS						
Terminal Voltage Range <sup>4</sup>	$V_{A, B, W}$		$V_{SS}$		$V_{DD}$	V
Capacitance <sup>5</sup> Ax, Bx	$C_{A, B}$	$f = 1\text{ MHz}$ , measured to GND, Code = Half-scale		11		pF
Capacitance <sup>5</sup> Wx	$C_W$	$f = 1\text{ MHz}$ , measured to GND, Code = Half-scale		80		pF
Common-mode Leakage Current <sup>5,6</sup>	$I_{CM}$	$V_W = V_{DD}/2$		0.01	1	$\mu A$
DIGITAL INPUTS & OUTPUTS						
Input Logic High	$V_{IH}$	with respect to GND, $V_{DD} = 5V$	2.4			V
Input Logic Low	$V_{IL}$	with respect to GND, $V_{DD} = 5V$			0.8	V
Input Logic High	$V_{IH}$	with respect to GND, $V_{DD} = 3V$	2.1			V
Input Logic Low	$V_{IL}$	with respect to GND, $V_{DD} = 3V$			0.6	V
Input Logic High	$V_{IH}$	with respect to GND, $V_{DD} = +2.5V$ , $V_{SS} = -2.5V$	2.0			V
Input Logic Low	$V_{IL}$	with respect to GND, $V_{DD} = +2.5V$ , $V_{SS} = -2.5V$			0.5	V
Output Logic High (SDO, RDY)	$V_{OH}$	$R_{PULL-UP} = 2.2K\Omega$ to +5V	4.9			V
Output Logic Low	$V_{OL}$	$I_{OL} = 1.6mA$ , $V_{LOGIC} = +5V$			0.4	V
Input Current	$I_{IL}$	$V_{IN} = 0V$ or $V_{DD}$			$\pm 5$	$\mu A$
Input Capacitance <sup>5</sup>	$C_{IL}$			5		pF
POWER SUPPLIES						
Single-Supply Power Range	$V_{DD}$	$V_{SS} = 0V$	3.0		5.5	V
Dual-Supply Power Range	$V_{DD}/V_{SS}$		$\pm 2.25$		$\pm 2.75$	V
Positive Supply Current	$I_{DD}$	$V_{IH} = V_{DD}$ or $V_{IL} = GND$ , $T_A = 25^{\circ}C$		2	4.5	$\mu A$
Positive Supply Current	$I_{DD}$	$V_{IH} = V_{DD}$ or $V_{IL} = GND$		3.5	10	$\mu A$
Programming Mode Current	$I_{DD(PG)}$	$V_{IH} = V_{DD}$ or $V_{IL} = GND$		35		mA
Negative Supply Current	$I_{SS}$	$V_{IH} = V_{DD}$ or $V_{IL} = GND$ , $V_{DD} = 2.5V$ , $V_{SS} = -2.5V$		3.5	10	$\mu A$
Power Dissipation <sup>8</sup>	$P_{DISS}$	$V_{IH} = V_{DD}$ or $V_{IL} = GND$		18	50	$\mu W$
Power Supply Sensitivity <sup>5</sup>	$P_{SS}$	$\Delta V_{DD} = +5V \pm 10\%$		0.002	0.01	%/%

NOTES: See bottom of table next page.

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## ADN2860 ELECTRICAL CHARACTERISTICS 25k, 250k VERSIONS

( $V_{DD} = 3V$  to  $5.5V$  and  $-40^{\circ}C < T_A < +85^{\circ}C$ , unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Units
DYNAMIC CHARACTERISTICS <sup>5, 9</sup>						
Bandwidth –3dB	BW	$V_{DD}/V_{SS} = \pm 2.5V$ , $R_{AB} = 25k\Omega / 250k\Omega$		125/12		kHz
Total Harmonic Distortion	THD <sub>W</sub>	$V_A = 1V_{rms}$ , $V_B = 0V$ , $f = 1kHz$		0.05		%
$V_W$ Settling Time	$t_S$	$V_A = V_{DD}$ , $V_B = 0V$ , $V_W = 0.50\%$ error band, code 000 <sub>H</sub> to 200 <sub>H</sub> . $R_{AB} = 25k/250k\Omega$		4 / 36		$\mu s$
Resistor Noise Spectral Density	$e_{N\_WB}$	$R_{AB} = 25k\Omega / 250k\Omega$ , $T_A = 25^{\circ}C$		20 / 64		nV $\sqrt{Hz}$
Crosstalk ( $C_{W1}/C_{W2}$ )	$C_T$	$V_A = V_{DD}$ , $V_B = 0V$ , Measured $V_{W1}$ with $V_{W2}$ making full scale change, $R_{AB} = 25k/250k\Omega$		90/21		nV-s
Analog Crosstalk	$C_{TA}$	$V_{DD} = V_{A1} = +2.5V$ , $V_{SS} = V_{B1} = -2.5V$ , Measure $V_{W1}$ with $V_{W2} = 5V$ p-p @ $f = 1kHz$ , Code1 = 200 <sub>H</sub> , Code 2 = 3FF <sub>H</sub> , $R_{AB} = 25k\Omega / 250k\Omega$		-81/-62		dB
INTERFACE TIMING CHARACTERISTICS applies to all parts(Notes 6,12)						
SCL Clock Frequency	$f_{SCL}$		0		400	KHz
$t_{BUF}$ Bus free time between STOP & START	$t_1$		1.3			$\mu s$
$t_{HD;STA}$ Hold Time (repeated START)	$t_2$	After this period the first clock pulse is generated	600			ns
$t_{LOW}$ Low Period of SCL Clock	$t_3$		1.3			$\mu s$
$t_{HIGH}$ High Period of SCL Clock	$t_4$		0.6		50	$\mu s$
$t_{SU;STA}$ Setup Time For START Condition	$t_5$		600			ns
$t_{HD;DAT}$ Data Hold Time	$t_6$				900	ns
$t_{SU;DAT}$ Data Setup Time	$t_7$		100			ns
$t_R$ Rise Time of both SDA & SCL signals	$t_8$				300	ns
$t_F$ Fall Time of both SDA & SCL signals	$t_9$				300	ns
$t_{SU;STO}$ Setup time for STOP Condition	$t_{10}$		600			ns

### NOTES:

- Typical represent average readings at  $+25^{\circ}C$ ,  $V_{DD} = +5V$ .
- Resistor position non-linearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. See figure 20 test circuit.
- INL and DNL are measured at  $V_W$  with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter.  $V_A = V_{DD}$  and  $V_B = 0V$ . DNL specification limits of  $\pm 1LSB$  maximum are Guaranteed Monotonic operating conditions. See Figure 19 test circuit.
- Resistor terminals A, B, W have no limitations on polarity with respect to each other.
- Guaranteed by design and not subject to production test.
- Bandwidth, noise and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.
- $P_{DISS}$  is calculated from  $(I_{DD} \times V_{DD})$ . CMOS logic level inputs result in minimum power dissipation.
- All dynamic characteristics use  $V_{DD} = +5V$ .
- See timing diagram for location of measured values.
- Endurance is qualified to 100,000 cycles as per JEDEC Std. 22 method A117 and measured at  $-40^{\circ}C$ ,  $+25^{\circ}C$  and  $+85^{\circ}C$ , typical endurance at  $25^{\circ}C$  is 700,000 cycles.
- Retention lifetime equivalent at junction temperature ( $T_J$ ) =  $55^{\circ}C$  as per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6eV will derate with junction temperature.

The ADN2860 contains 21,035 transistors. Die size: 88.2 mil x 87.0 mil, 7673 sq. mil.  
Specifications Subject to Change without Notice

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**Absolute Maximum Rating**<sup>1</sup> ( $T_A = +25^{\circ}\text{C}$ , unless otherwise noted)

$V_{DD}$ to GND.....	-0.3 V, +7 V
$V_{SS}$ to GND .....	+0.3 V, -7 V
$V_{DD}$ to $V_{SS}$ .....	+7 V
$V_A$ , $V_B$ , $V_W$ to GND.....	$V_{SS}-0.3$ V, $V_{DD}+0.3$ V
$I_A$ , $I_B$ , $I_W$	
Intermittent <sup>2</sup> .....	$\pm 20$ mA
Continuous .....	$\pm 2$ mA
Digital Inputs & Output Voltage to GND....	-0.3 V, $V_{DD}+0.3$ V
Operating Temperature Range <sup>3</sup> .....	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
Maximum Junction Temperature ( $T_J \text{ MAX}$ ).....	$+150^{\circ}\text{C}$
Storage Temperature.....	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Lead Temperature, Soldering <sup>4</sup>	
Vapor Phase (60 sec) .....	$+215^{\circ}\text{C}$
Infrared (15 sec).....	$+220^{\circ}\text{C}$

Thermal Resistance Junction-to-Ambient  $\theta_{JA}$ ,

    LFCSP-24..... TBD  $^{\circ}\text{C/W}$

Thermal Resistance Junction-to-Case  $\theta_{JC}$ ,

    LFCSP-24..... TBD  $^{\circ}\text{C/W}$

Package Power Dissipation =  $(T_J \text{ MAX} - T_A) / \theta_{JA}$

## NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the B, and W terminals at a given resistance.
3. Includes programming of Nonvolatile memory

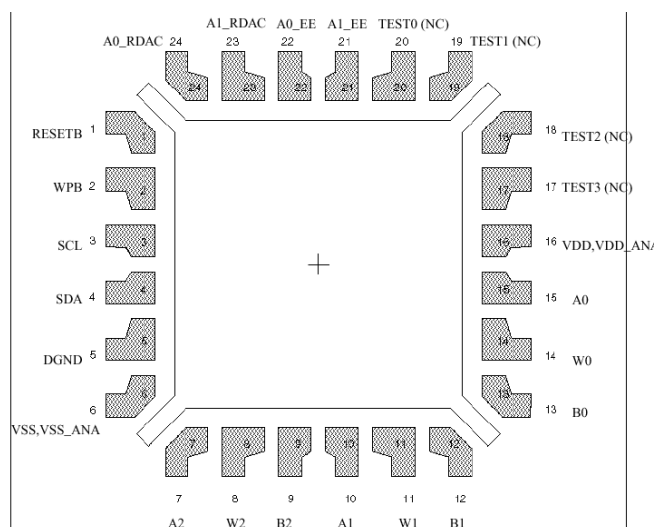
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADN2860 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# Preliminary Technical Data

ADN2860ACP PIN CONFIGURATION

# ADN2860



## PIN DESCRIPTIONS

#	Name	Description
1	RESET	Reset the scratch pad register with current contents of the EEMEM register. Factory defaults midscale before any programming
2	WP	Write Protect Pin. When active low, $\overline{WP}$ prevents any changes to the present register contents, except $\overline{PR}$ and cmd 1 and 8 will refresh the RDAC register from EEMEM. Execute a NOP instruction before returning to $\overline{WP}$ high.
3	SCL	Serial Input Register clock pin. Shifts in one bit at a time on positive clock edges.
4	SDA	Serial Data Input Pin. Shifts in one bit at a time on positive clock CLK edges. MSB loaded first.
5	DGND	Ground pin, logic ground reference
6	V <sub>SS</sub>	Negative Supply. Connect to zero volts for single supply applications.
7	A2	A terminal of RDAC2.
8	W2	Wiper terminal of RDAC2
9	B2	B terminal of RDAC2.
10	A1	A terminal of RDAC1.
11	W1	Wiper terminal of RDAC1
12	B1	B terminal of RDAC1
13	A0	A terminal of RDAC0.
14	W0	Wiper terminal of RDAC0.
15	B0	B terminal of RDAC0
16	V <sub>DD</sub>	Positive Power Supply Pin.
17	TEST3	Test pin 3 (Do Not Connect)
18	TEST2	Test pin 2 (Do Not Connect)
19	TEST1	Test pin 1 (Do Not Connect)
20	TEST0	Test pin 0 (Do Not Connect)
21	A1_EE	I2C Device Address 1 for EEMEM
22	A0_EE	I2C Device Address 0 for EEMEM
23	AD1	I2C Device Address 1 for RDAC
24	AD0	I2C Device Address 0 for RDAC

# Preliminary Technical Data

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## I<sup>2</sup>C Interface Timing Diagram

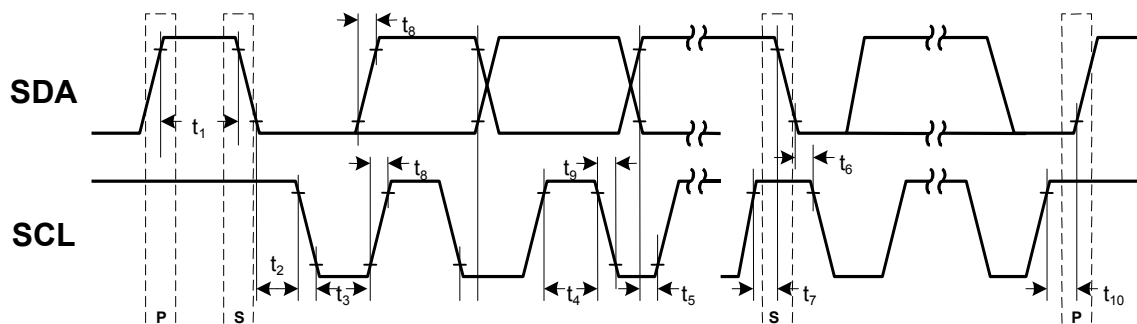


Figure 1. I2C Timing Diagram

## I<sup>2</sup>C Interface General Description

From Master to Slave

From Slave to Master

S = Start Condition

P = Stop Condition

A = Acknowledge (SDA Low)

$\bar{A}$  = Not Acknowledge (SDA High)

R/ $\bar{W}$  = Read Enable at High and Write Enable at Low

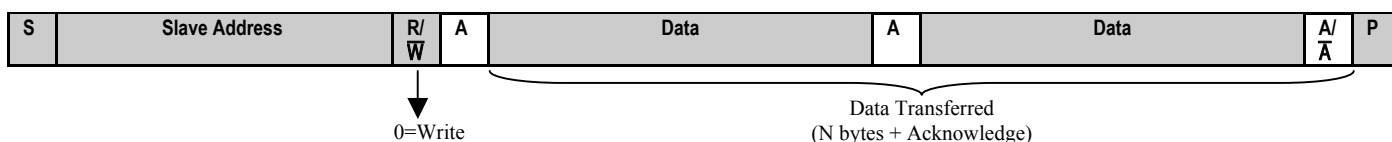


Figure 2. I<sup>2</sup>C - Master Transmitting Data to Slave

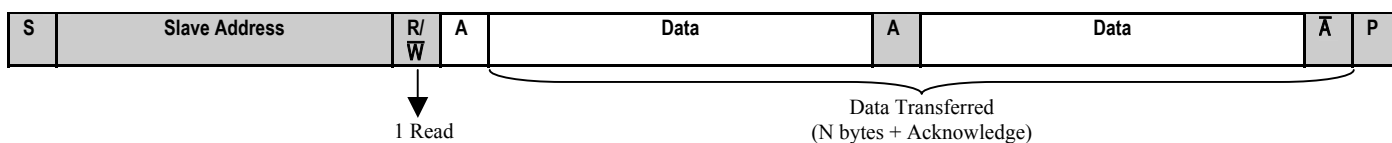


Figure 3. I<sup>2</sup>C - Master Reading Data From Slave

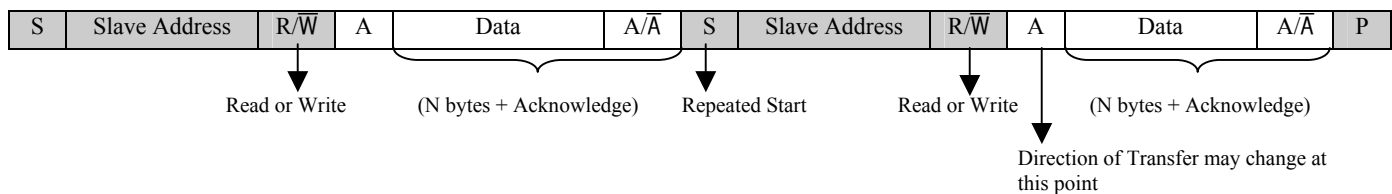


Figure 4. I<sup>2</sup>C - Combined Transmit/Read

# Preliminary Technical Data

## EEPROM I<sup>2</sup>C Interface Description

# ADN2860

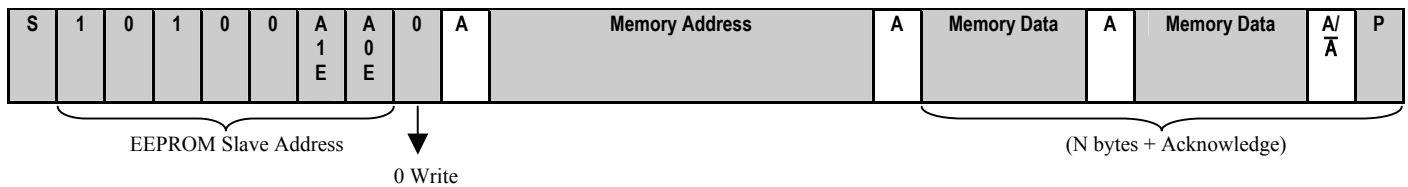


Figure 5. EEPROM Write

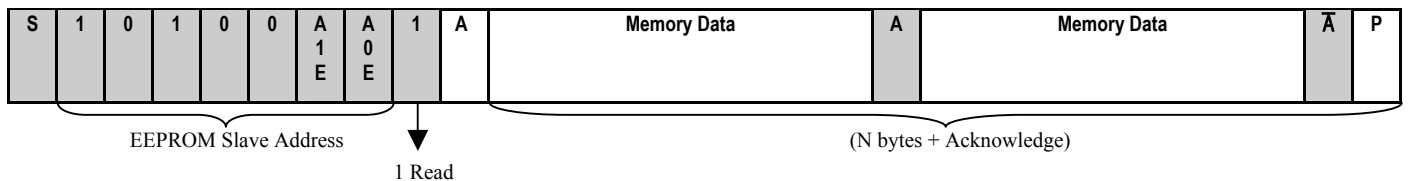


Figure 6. EEPROM Current Read

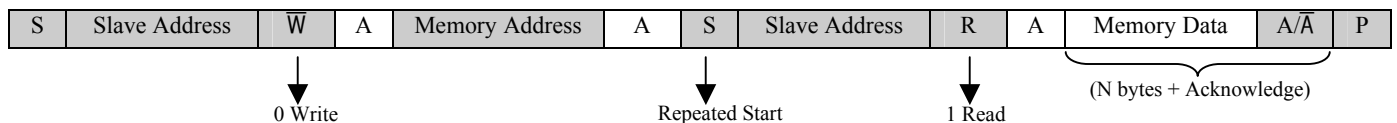


Figure 7. EEPROM Random Read

### EEPROM Interface Operation

The 256 bytes of EEPROM memory provided in the ADN2860 are organized into 16 pages of 16 bytes each. The word size of each memory location is one byte wide.

The I<sup>2</sup>C slave address of the EEPROM is 10100(A1E)(A0E), where A1E and A0E are external pin programmable address bits. The two pin programmable address bits allow a total of four ADN2860 devices to be controlled by a single I<sup>2</sup>C master bus, each having its own EEPROM.

An internal 8-bit address counter for the EEPROM is automatically incremented following each read or write operation. For read operations, the address counter is incremented after each byte is read, and the counter will rollover from address location 255 to 0.

For write operations, the address counter will be incremented after each byte written. The counter rolls-over from the upper most address of the current page to the lower most address of the current page. For example, writing two bytes beginning at address location 31 will cause the counter to roll back to address location 16 after the first byte is written, and then the address will increment to 17 after the second byte is written.

### EEPROM Write

Each write operation issued to the EEPROM can program 1 byte to 16 bytes (1 page) of memory. Figure 5 shows the EEPROM write interface, the number of bytes of data, N, the user wishes to send to the EEPROM is unrestricted. If more than 16 bytes of data are sent in a single write operation, the address counter will rollback to the beginning address, and the previously sent data will be overwritten.

### EEPROM Write-Acknowledge Polling

After each write operation, an internal EEPROM write cycle begins. During the EEPROM internal write cycle, the I<sup>2</sup>C interface of the device will be disabled. In order to determine if the internal write cycle is complete and whether the I<sup>2</sup>C interface is enabled, interface polling must be executed. I<sup>2</sup>C interface polling can be conducted by sending a start condition followed by the EEPROM slave address + desired R/W bit. If the ADN2860 I<sup>2</sup>C interface responds with an ACK, then the write cycle is complete and the interface is ready to proceed with further operations. Otherwise, the I<sup>2</sup>C interface needs to be polled again to determine whether the write cycle has been completed.

### EEPROM Read

The ADN2860 EEPROM provides two different read operations, shown in figures 6 and 7. The number of bytes, N, read from the EEPROM in a single operation is unrestricted. If more than 256 bytes are read, the address counter will rollback to the start address, and data previously read will be read again.

Figure 6 shows the EEPROM Current Read operation. This operation does not allow an address location to be specified and reads data beginning at the current address location stored in the internal address counter.

A random read operation is shown in figure 7. This operation changes the address counter to the specified memory address by performing a “dummy write” and then performing a read operation beginning at the new address counter location.

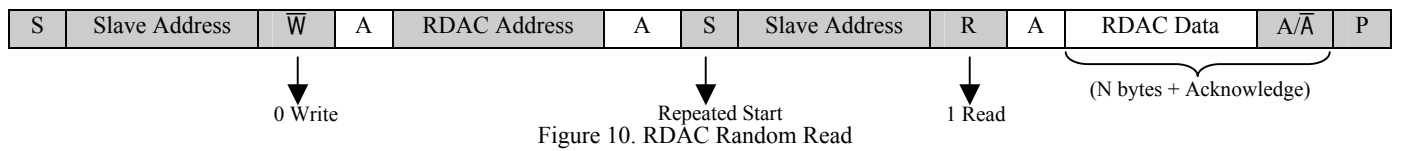
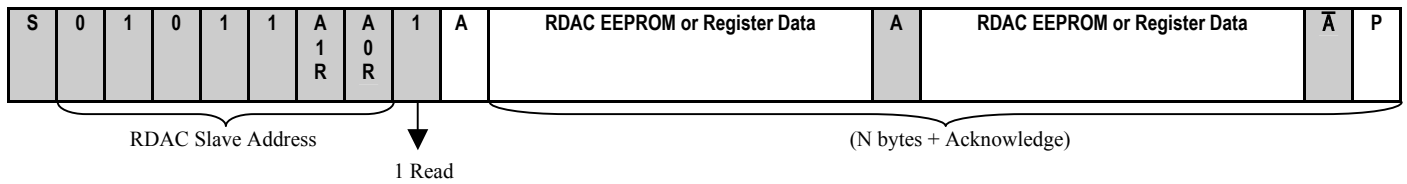
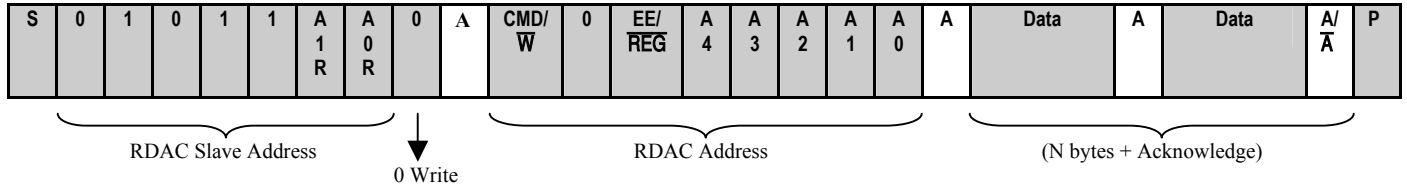
### EEPROM Write Protection

# Preliminary Technical Data

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Setting the  $\overline{WP}$  pin to a logic LOW protects the EEPROM memory from future write operations. In this mode, EEPROM read operations and RDAC register loading can still operate normally.

## RDAC I<sup>2</sup>C Interface Description



**RDAC Register Addresses (CMD/ $\overline{W}$ =0, EE/ $\overline{REG}$ =0)**

A4	A3	A2	A1	A0	RDAC	Byte Description
0	0	0	0	0	RDAC0	(D7)(D6)(D5)(D4)(D3)(D2)(D1)(D0) – RDAC0 8 LSBs
0	0	0	0	1	RDAC0	(X)(X)(X)(X)(X)(X)(X)(D8) – RDAC0 MSB
0	0	0	1	0	RDAC1	(D7)(D6)(D5)(D4)(D3)(D2)(D1)(D0) – RDAC1 8 LSBs
0	0	0	1	1	RDAC1	(X)(X)(X)(X)(X)(X)(X)(D8) – RDAC1 MSB
0	0	1	0	0	RDAC2	(X)(D6)(D5)(D4)(D3)(D2)(D1)(D0) – RDAC2 7 bits
0	0	1	0	1 to 1		reserved

Table 1. RDAC Register Address Table

**RDAC R/W EEPROM Address Table (CMD/ $\overline{W}$ =0, EE/ $\overline{REG}$ =1)**

A4	A3	A2	A1	A0	Byte Description
0	0	0	0	0	RDAC0 8 LSBs
0	0	0	0	1	RDAC0 MSB
0	0	0	1	0	RDAC1 8 LSBs
0	0	0	1	1	RDAC1 MSB
0	0	1	0	0	RDAC2 7 bits
0	0	1	0	1 to 1	11 bytes RDAC USER EEPROM

Table 2. RDAC R/W EEPROM Address Table

**RDAC Read-Only EEPROM Address Table (CMD/ $\overline{W}$ =0, EE/ $\overline{REG}$ =1)**

A4	A3	A2	A1	A0	Byte Description
1	0	0	0	0	% Tolerance
1	0	0	0	1	% Tolerance
1	0	0	1	0	% Tolerance
1	0	0	1	1	% Tolerance
1	0	1	0	0	% Tolerance
1	0	1	0	1 to 1	reserved



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# ADN2860

## RDAC I<sup>2</sup>C Interface Description (cont'd)

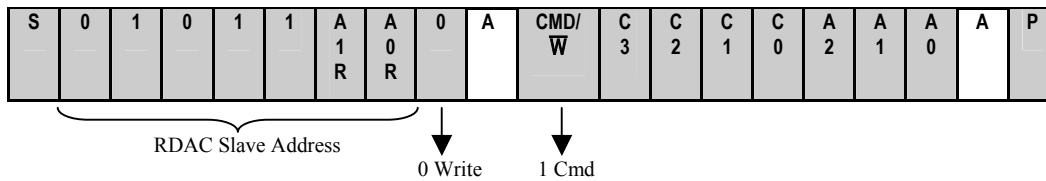


Figure 11. RDAC Command Write (Dummy Write)

RDAC Command Table (CMD/W=1)

C3	C2	C1	C0	Command Description
0	0	0	0	NOP
0	0	0	1	Load EEPROM to RDAC*
0	0	1	0	Store RDAC to EEPROM
0	0	1	1	Decrement RDAC 6dB
0	1	0	0	Decrement All RDACs 6dB
0	1	0	1	Decrement RDAC One Step
0	1	1	0	Decrement All RDACs One Step
0	1	1	1	Reset: Load EEPROM to all RDACs
1	0	0	0	Increment RDAC 6dB
1	0	0	1	Increment All RDAC 6dB
1	0	1	0	Increment RDAC One Step
1	0	1	1	Increment All RDAC One Step
1	1	0	0 to 1	reserved

Table 3. RDAC Commands

\* This command leaves the device in the EEPROM Read power state. Issue the NOP command to return the device to the idle state.

### RDAC Interface Operation

Each programmable resistor wiper setting is controlled by specific RDAC registers, as shown in the RDAC Register Address Table (table 1). Each RDAC register corresponds to an EEPROM memory location, which provides non-volatile wiper storage functionality.

RDAC registers and their corresponding EEPROM memory locations can be programmed and read independently from each other. The RDAC register can be refreshed by the EEPROM locations either with a hardware reset via pin 1, or by issuing one of the various RDAC register load commands shown in the RDAC command table (table 3).

### RDAC Write

Setting the wiper position requires an RDAC write operation, shown in figure 8. RDAC write operations follow a format similar to the EEPROM write interface. The only difference between an RDAC write and an EEPROM write operation is the use of an RDAC address byte in place of the memory address used in the EEPROM write operation. The RDAC address byte is described in detail in the tables 1 and 2.

As with the EEPROM write operation, the RDAC write operation disables the I<sup>2</sup>C interface during the internal write cycle. Acknowledge polling, as described in the EEPROM I<sup>2</sup>C

interface section, is required to determine whether the write cycle has been completed.

### RDAC Read

The ADN2860 provides two RDAC read operations. The first, shown in figure 9 reads the contents of the current RDAC address counter. Figure 10 illustrates the second read operation. This operation allows users to specify which RDAC register to read by first issuing a “dummy write” command to change the RDAC address pointer, and then proceeding with the RDAC read operation at the new address location.

The read-only RDAC EEPROM memory locations can also be read by using the address and bits specified in the RDAC Read-Only EEPROM Address Table (table 2).

### RDAC Quick Commands

Eleven shortcut “quick” commands are provided for easy manipulation of RDAC registers and their corresponding EEPROM memory locations. These commands are shown in table 3.

The interface for issuing an RDAC quick command is shown in figure 11. All quick commands require Acknowledge polling to determine whether the command has finished executing.

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A more detailed discussion about the RDAC quick commands can be found in the Operational Overview section of this document.

## OPERATIONAL OVERVIEW

The ADN2860 digital potentiometer is designed to operate as a true variable resistor. The resistor wiper position is determined by the RDAC register contents. The RDAC register acts like a scratch-pad register, allowing unlimited changes of resistance settings. RDAC register contents can be changed using the ADN2860's serial I<sup>2</sup>C interface. The format of the datawords and commands to program the RDAC registers are discussed in the RDAC I<sup>2</sup>C Interface section of this document.

RDAC registers also have a corresponding EEPROM memory location, which provide non-volatile storage of resistor wiper position settings. The ADN2860 provides commands to store the RDAC register contents to their respective EEPROM memory locations. During subsequent power on sequences, the RDAC registers will automatically be loaded with the stored value.

Saving data from an RDAC register to EEPROM memory takes approximately 25ms and consumes 20mA of current.

In addition to the movement of data between RDAC registers and EEPROM memory, the ADN2860 provides other shortcut commands that facilitate the users' programming needs.

- |     |   |
|-----|---|
| 1.  | Restore EEPROM setting to RDAC                      |
| 2.  | Save RDAC register contents to EEPROM               |
| 3.  | Decrement RDAC 6dB (Shift Data Bits Right)          |
| 4.  | Decrement all RDACs 6dB (Shift All Data Bits Right) |
| 5.  | Decrement RDAC one step                             |
| 6.  | Decrement all RDACs one step                        |
| 7.  | Reset EEPROM setting to RDAC                        |
| 8.  | Increment RDAC 6dB (Shift Data Bits Left)           |
| 9.  | Increment all RDACs 6dB (Shift All Data Bits Left)  |
| 10. | Increment RDAC one step                             |
| 11. | Increment all RDACs one step                        |

Table 4. ADN2860 Shortcut Commands

### Linear Increment and Decrement Commands

The increment and decrement commands (#10, #11, #5, #6) are useful for linear step adjustment applications. These commands simplify microcontroller software coding by allowing the controller to just send an increment or decrement command to the ADN2860. The adjustment can be directed to an individual RDAC or all three RDACs.

### Logarithmic Taper Mode Adjustment ( $\pm 6\text{dB}/\text{step}$ )

The ADN2860 accommodates logarithmic taper adjustment of the RDAC wiper position(s) by shifting the register contents left/right for increment/decrement operations. Commands 8, 9, 3, and 4 can be used to logarithmically increment or decrement the wiper positions individually or change all three channel settings at the same time.

Incrementing the wiper position by +6dB is essentially doubling the RDAC register value, while decrementing by -6dB is halving the register content. Internally, the ADN2860 uses a shift register to shift the bits left and right to achieve a logarithmic increment or decrement.

Non-ideal  $\pm 6\text{dB}$  step adjustment occurs under certain conditions. Table 5 illustrates the shifting function on an individual RDAC register data bits. Each line going down the table represents a successive shift operation. Note that the left shift (#10 & #11) commands were modified such that if the data in the RDAC register is equal to zero, and the data is shifted the RDAC register is then set to code 1. Similarly, if the data in the RDAC register is greater than or equal to mid-scale, and the data is left shifted, the data in the RDAC register is automatically set to full-scale. This makes the left shift function as close to a logarithmic adjustment as possible.

The right shift commands (#3 & #4) will be ideal only if the LSB is a 0 (ideal logarithmic = no error). If the LSB is a 1 then the right shift function generates a linear half LSB error, which translates to a number of error bits.

	Left Shift	Right Shift	
	0 0000 0000	1 1111 1111	
	0 0000 0001	0 1111 1111	
	0 0000 0010	0 0111 1111	
	0 0000 0100	0 0011 1111	
	0 0000 1000	0 0001 1111	
Left	0 0001 0000	0 0000 1111	Right
Shift	0 0010 0000	0 0000 0111	Shift
(+6dB/step)	0 0100 0000	0 0000 0011	(-6dB/step)
	0 1000 0000	0 0000 0001	
	1 0000 0000	0 0000 0000	
	1 1111 1111	0 0000 0000	
	1 1111 1111	0 0000 0000	

Table 5. RDAC Register Contents After  $\pm 6\text{dB}$  Step Adjustments

Actual conformance to a logarithmic curve between the data contents in the RDAC register and the wiper position for each right shift (#3 & #4) command execution contains an error only for odd numbers of bits. Even numbers of bits are ideal. The graph in figure 12 shows a plot of Log\_Error [i.e.  $20 \cdot \log_{10}(\text{error}/\text{code})$ ] for the ADN2860.

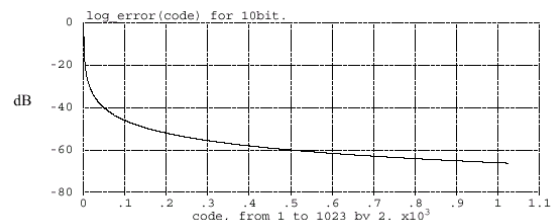


Figure 12. Plot of Log\_Error Conformance for Odd Numbers of Bits Only (Even Numbers of Bits are ideal)

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## Using Additional Internal Nonvolatile EEPROM

The ADN2860 contains additional internal user EEPROM for saving constants and other data. The user EEPROM I<sup>2</sup>C dataword follows the same format as the general purpose EEPROM memory shown in figures 5 and 6. User EEPROM memory addresses are shown at the bottom of table 2.

To support the use of multiple EEPROM modules on a single I<sup>2</sup>C bus, the ADN2860 features two external addressing pins, pins 21 and 22 (A1\_EE and A0\_EE) to manually set the address of the EEPROM included with the ADN2860. This feature ensures that the correct EEPROM memory is accessed when using multiple memory modules on a single I<sup>2</sup>C bus.

## Digital Input/Output Configuration

All digital inputs are ESD protected. Digital inputs are high impedance and can be driven directly from most digital sources. Active at logic low, **RESET** and **WP** should be biased to  $V_{DD}$  if they are not used. There are no internal pull-up resistors present on any of the digital input pins of the ADN2860. As a result, pull-up resistors are needed if these functions are not used.

ESD protection of the digital inputs is shown in figure 13.

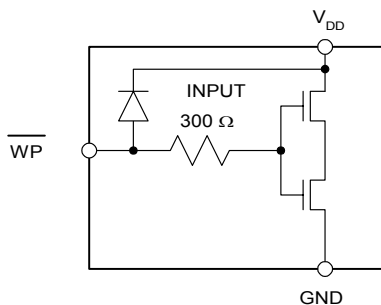


Figure 13. Equivalent WP Input Protection

## Multiple Devices On One Bus

Figure 14 shows four ADN2860 devices on the same serial bus. Each has a different slave address since the state of their AD0 and AD1 pins are different. This allows each RDAC within each device to be written to or read from independently.

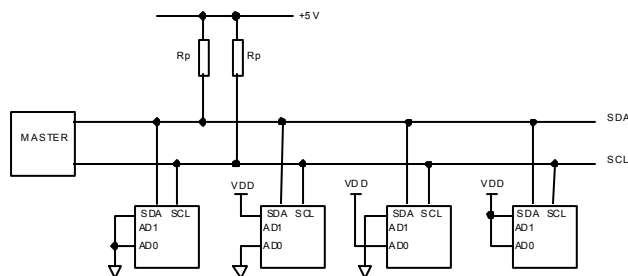


Figure 14. Multiple ADN2860 Devices on a Single Bus

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## Level Shift for Bi-Directional Communication

While most old systems may be operating at one voltage, a new component may be optimized at another. When two systems transmit the same signal at two different voltages, proper level shifting is required.

In some instances, for example, a 3.3V EEPROM memory module may be used along with a 5V digital potentiometer. A level shifting scheme is required in order to enable bi-directional communication between the two devices.

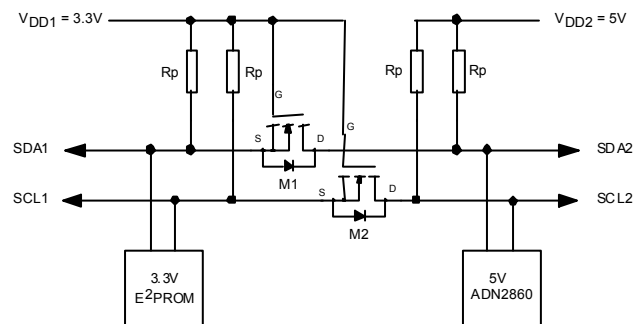


Figure 15. Level Shifting for different voltage devices on an I2C bus

Figure 15 shows one of many possible techniques to properly level shift signals between two devices. M1 and M2 can be N-channel FETs (2N7002). If  $V_{DD}$  falls below 2.5V, M1 and M2 should be low threshold N-channel FETs (FDV301N).

## Terminal Voltage Operation Range

The ADN2860 positive  $V_{DD}$  and negative  $V_{SS}$  power supply inputs define the boundary conditions for proper 2-terminal programmable resistance operation. Supply signals on terminals W and B that exceed  $V_{DD}$  or  $V_{SS}$  will be clamped by the internal forward biased diodes of the ADN2860.

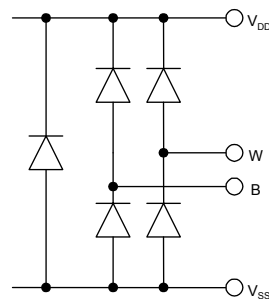


Figure 16. Maximum Terminal Voltages Set by  $V_{DD}$  &  $V_{SS}$

The ground pin of the ADN2860 device is primarily used as a digital ground reference, which needs to be tied to the common ground of the PCB. The digital input control signals to the ADN2860 must be referenced to the device ground pin, and satisfy the logic levels defined in the specification table of this datasheet.

An internal level shift circuit insures that the common mode voltage range of the 2-terminals extends from  $V_{SS}$  to  $V_{DD}$

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irrespective of the digital input level. In addition, there is no polarity constraint on the voltage across terminals W and B. The magnitude of  $|V_{WB}|$  is bounded by  $V_{DD} - V_{SS}$ .

## Power-Up Sequence

Since there are ESD protection diodes that limit the voltage compliance at terminals A, B, and W (see figure 16), it is important to power  $V_{DD} / V_{SS}$  before applying any voltage to terminals A, B, and W. Otherwise, the diode will be forward biased such that  $V_{DD} / V_{SS}$  will be powered unintentionally and may affect the rest of the users' circuit. The ideal power-up sequence is in the following order: GND,  $V_{DD}$ ,  $V_{SS}$ , digital inputs, and  $V_{A/B/W}$ . The order of powering  $V_A$ ,  $V_B$ ,  $V_W$ , and digital inputs is not important as long as they are powered after  $V_{DD} / V_{SS}$ .

## Layout and Power Supply Biasing

It is always a good practice to employ compact, minimum lead length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors. Low ESR (Equivalent Series Resistance)  $1\mu\text{F}$  to  $10\mu\text{F}$  tantalum or electrolytic capacitors should be applied at the supplies to minimize any transient disturbance and filter low frequency ripple. Figure 17 illustrates the basic supply bypassing configuration for the ADN2860.

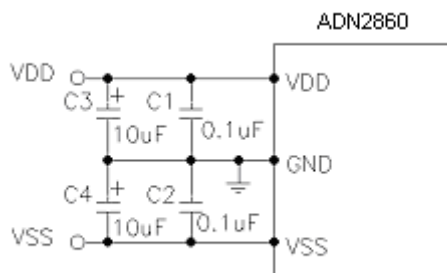


Figure 17. Power Supply Bypassing

## RDAC Structure

The patent pending RDAC contains a string of equal resistor segments, with an array of analog switches. The switches act as the wiper connection.

The ADN2860 has two RDACs with 512 connection points allowing it to provide better than 0.2% set-ability resolution. The ADN2860 also contains a third RDAC with 128 step resolution.

Figure 18 shows an equivalent structure of the connections between the two terminals that make up one channel of an RDAC. The SWB switch will always be ON, while one of the switches SW(0) to SW(2N-1) will be ON at any given time depending on the resistance position decoded from the databits in the RDAC register.

Since the switches are non-ideal, there is a  $50\Omega$  wiper resistance,  $R_W$ . Wiper resistance is a function of supply voltage and temperature, lower supply voltages and higher temperatures result in higher wiper resistances. Consideration of wiper resistance dynamics is important in applications where accurate prediction of output resistance is required.

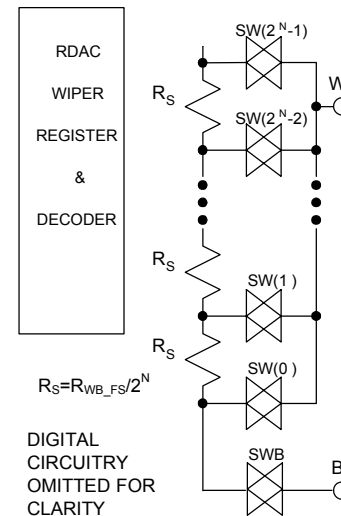


Figure 18.. Equivalent RDAC structure

## Calculating the Programmable Resistance

The nominal resistance of the RDAC between terminals A and B is available in  $25k\Omega$  or  $250k\Omega$ . The final two or three digits of the part number determine the nominal resistance value, e.g.  $25k\Omega = 25$  and  $250k\Omega = 250$ .

The following discussion describes the calculation of resistance  $R_{WB}(D)$  at different codes of a  $25k\Omega$  part for RDAC 0. The 9-bit data word in the RDAC latch is decoded to select one of the 512 possible settings.

The wiper first connection starts at the B terminal for data  $000_H$ .  $R_{WB}(0)$  is  $50\Omega$  because of the wiper resistance and it is independent to the full-scale resistance. The second connection is the first tap point where  $R_{WB}(1)$  becomes  $48.8\Omega + 50 = 98.8\Omega$  for data  $001_H$ . The third connection is the next tap point representing  $R_{WB}(2) = 97.6 + 50 = 147.6\Omega$  for data  $002_H$  and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at  $R_{WB}(512) = 25001\Omega$ . See Figure 18 for a simplified diagram of the equivalent RDAC circuit.

The general equations that determine the programmed output resistance between W and B are:

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$$R_{WB}(D) = \frac{D}{512} \cdot R_{AB} + R_W \quad (\text{RDAC 0 and 1}) \quad (1)$$

$$R_{WB}(D) = \frac{D}{128} \cdot R_{AB} + R_W \quad (\text{RDAC 2 only}) \quad (2)$$

Where D is the decimal equivalent of the data contained in the RDAC register and  $R_W$  is the wiper resistance.

The output resistance values in table 6 will be set for the following RDAC latch codes with  $V_{DD} = 5\text{ V}$  (applies to  $R_{AB} = 25\text{ k}\Omega$  Digital Potentiometers):

D (DEC)	$R_{WB}^{(D)}$ ( $\Omega$ )	Output State
511	25001	Full-Scale
256	12550	Mid-Scale
1	98.8	1 LSB
0	50	Zero-Scale (Wiper contact resistance)

Table 6.  $R_{WB}$  at Selected Codes for  $R_{WB\_FS} = 25\text{ k}\Omega$

Note that in the zero-scale condition a finite wiper resistance of  $50\Omega$  is present. Care should be taken to limit the current flow between W and B in this state to no more than 20mA to avoid degradation or possible destruction of the internal switches.

Channel-to-channel  $R_{WB}$  matching is better than 1%. The change in  $R_{WB}$  with temperature has a 35ppm/ $^{\circ}\text{C}$  temperature coefficient.

Like the mechanical potentiometer the RDAC replaces, the ADN2860 parts are totally symmetrical. The resistance between the wiper W and terminal A also produces a digitally controlled complementary resistance  $R_{WA}$ . When  $R_{WA}$  is used, the B terminal can be let floating or tied to the wiper. Setting the resistance value for  $R_{WA}$  starts at a maximum value of resistance and decreases as the data loaded in the latch is increased in value. The general transfer equation for this operation is:

$$R_{WA}(D) = \frac{512 - D}{512} \cdot R_{AB} + R_W \quad (\text{RDAC 0 and 1}) \quad (3)$$

$$R_{WA}(D) = \frac{128 - D}{128} \cdot R_{AB} + R_W \quad (\text{RDAC 2 only}) \quad (4)$$

For example, the following output resistance values will be set for the following RDAC latch codes (applies to  $R_{AB} = 25\text{ k}\Omega$  Digital Potentiometers):

D (DEC)	$R_{WA}(D)$ ( $\Omega$ )	Output State
511	98.8	full-scale
128	12550	Mid-scale
1	25001	1 LSB
0	25050	Zero-scale

Table 7. ADN2860.  $R_{WA}(D)$  at selected codes for  $R_{AB} = 25\text{ k}\Omega$ .

The typical distribution of  $R_{AB}$  from channel-to-channel matches to  $\pm 0.2\%$  within the same package. Device to device matching is process lot dependent, with a worst case of  $\pm 30\%$  variation. Changes in  $R_{AB}$  with temperature has a 35ppm/ $^{\circ}\text{C}$  temperature coefficient.

## PROGRAMMING THE POTENTIOMETER DIVIDER

### Voltage Output Operation

The digital potentiometer can be configured to generate an output voltage at the wiper terminal, which is proportional to the input voltages applied to terminals A and B. Connecting terminal A to +5V and terminal B to ground produces an output voltage at the wiper which can be any value starting at zero volts up to +5V. Each LSB of voltage is equal to the voltage applied across terminals A and B divided by the  $2^N$  position resolution of the potentiometer divider.

Since ADN2860 can also be supplied by dual supplies, the general equations defining the output voltage at  $V_W$  with respect to ground for any given input voltages applied to terminals A and B are:

$$V_W(D) = \frac{D}{512} \cdot V_{AB} + V_B \quad (\text{RDAC 0 and 1}) \quad (5)$$

$$V_W(D) = \frac{D}{128} \cdot V_{AB} + V_B \quad (\text{RDAC 2}) \quad (6)$$

Equation 5 assumes  $V_W$  is buffered so that the effect of wiper resistance is nulled. Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. In this mode, the output voltage is dependent on the ratio of the internal resistors not the absolute value, therefore, the drift improves to 15ppm/ $^{\circ}\text{C}$ . There is no voltage polarity restriction between terminals A, B, and W as long as the terminal voltage ( $V_{\text{TERM}}$ ) stays within  $V_{SS} < V_{\text{TERM}} < V_{DD}$ .

## APPLICATIONS

### Laser Diode Driver (LDD) calibration

The ADN2860 can be used with any laser diode driver. Its high resolution, compact footprint, and superior temperature drift characteristics make it ideal for optical parameter setting.

The ADN2841 is a 2.7 Gbps laser diode driver that utilizes a unique control algorithm to manage both the laser average power and extinction ratio after initial factory calibration. It stabilizes the laser data transmission by continuously monitoring its optical power, and correcting the variations caused by temperature and the laser degradation over time. In ADN2841, the  $I_{MPD}$  monitors the laser diode current. Through its dual loop Power and Extinction Ratio control, calibrated by ADN2860, the internal driver controls the bias current  $I_{BIAS}$  and consequently the average power. It also regulates the modulation current,  $I_{MODP}$  by changing the modulation current linearly with slope efficiency. Any changes in the laser threshold current or slope efficiency are therefore compensated. As a result, this optical supervisory system minimizes the laser characterization efforts and therefore

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enables designers to apply comparable lasers from multiple sources.

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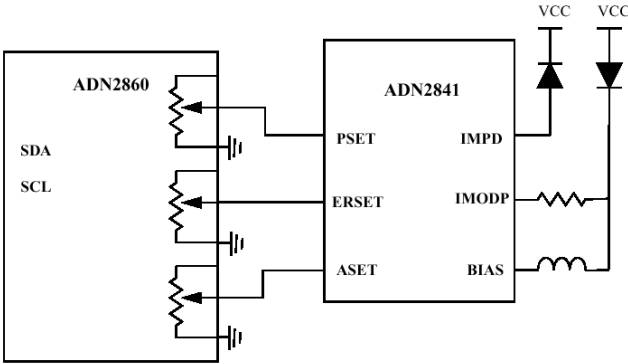


Figure 19. Optical Supervisory System

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## Outline Dimensions

Dimensions shown in inches and (mm).

[4x4mm 24-Lead LFCSP package diagrams To Be Provided]