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# Multi-Rate to 2.7Gbps Clock and Data Recovery IC with Limiting Amplifier

# Preliminary Technical Data ADN2809

**FEATURES**

**Meets SONET Requirements for Jitter Transfer / Generation / Tolerance**
**Quantizer Sensitivity: 6 mV typical**
- **Adjustable Slice Level: +/- 100 mV**
- **1.9GHz minimum Bandwidth**

**Loss of Signal Detect Range: 4mV to 17mV**
**Single Reference Clock Frequency for all rates Including 15/14 (7%) Wrapper Rate**
- **Choice of 19.44, 38.88, 77.76 or 155.52MHz**

**LVPECL / LVDS / LVCMOS / LVTTL compatible inputs (LVPECL / LVDS only at 155.52 MHz)**
**19.44MHz Crystal Oscillator for Module apps**
**Loss of Lock indicator**
**Loopback mode for High Speed Test Data**
**Output Squelch & Clock Recovery Functions**
**Single Supply Operation: 3.3 Volts (±10%)**
**Low Power: 780 mW Typical**
**Patented Clock Recovery Architecture**
**7 x 7 mm 48 pin LFCSP**

**APPLICATIONS**

**SONET OC-3/12/48, SDH STM-1/4/16, and all associated FEC rates**
**WDM transponders**
**SONET/SDH regenerators and test equipment**
**Backplane applications**

**PRODUCT DESCRIPTION**

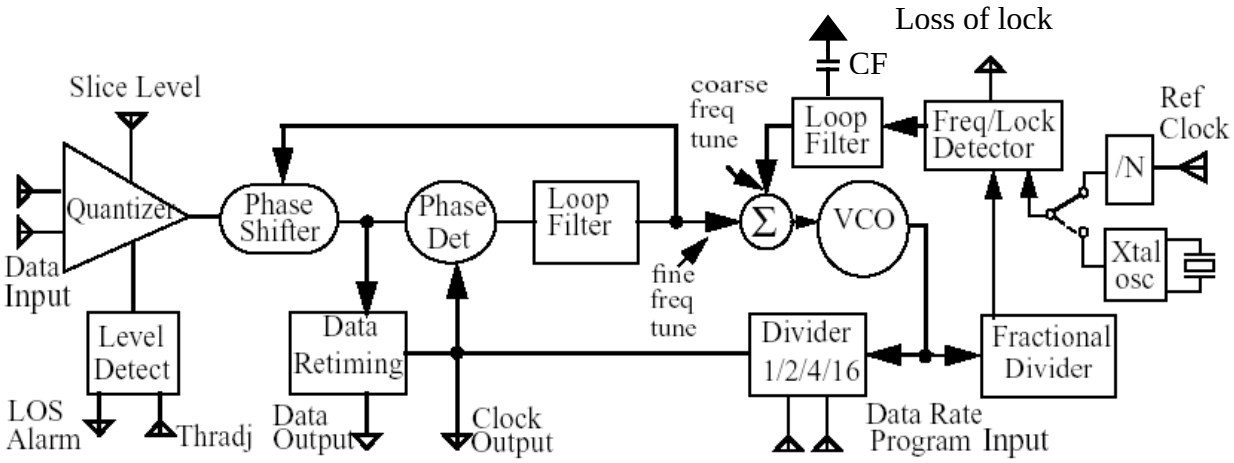
The ADN2809 provides the receiver functions of Quantization, Signal Level Detect and Clock and Data Recovery at rates of OC-3, OC-12, Gigabit Ethernet, OC-48 and all FEC rates. All SONET jitter requirements are met, including: Jitter Transfer; Jitter Generation; and Jitter Tolerance. All specifications are quoted for -40 to 85C ambient temperature unless otherwise noted.

The device is intended for WDM system applications and can be used with either an external reference clock or an on-chip oscillator crystal. Both native rates and 15/14 rate digital 'wrappers' rates are supported by the ADN2809, without any change of reference clock required.

This device together with a PIN diode and a TIA preamplifier can implement a highly integrated, low cost, low power fiber optic receiver.

The receiver front end Signal Detect circuit indicates when the input signal level has fallen below a user adjustable threshold.

The ADN2809 is available in a compact 48 pin chip scale package.




**Functional Block Diagram**

REV. PrB Sept 2001



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## ADN2809 ELECTRICAL CHARACTERISTICS at $T_A=T_{MIN}$ to $T_{MAX}$, $V_{CC}=V_{MIN}$ to $V_{MAX}$, $V_{EE}$=0V, $C_F$=4.7µF, 20 ohm ESR for xo unless otherwise noted

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **QUANTIZER–DC CHARACTERISTICS** | | | | | |
| Input Voltage Range | Single Ended, DC Coupled @ $P_{IN}$ or $N_{IN}$ | 0 | | 1.2 | V |
| Input Common Mode Voltage | " | 0.4 | | 1.2 | V |
| Input Peak-to-Peak Differential Voltage | @ $P_{IN}$ or $N_{IN}$ AC Coupled I/P[1] | | 2.4 | | V |
| Input Sensitivity, $V_{SENSE}$ (Peak-to-Peak Differential) | $P_{IN}$- $N_{IN}$, Figure 2, BER= $\leq$1 x $10^{-10}$ | 10 | 6 | | mV |
| Input Overdrive, $V_{OD}$ | Figure 3, BER = $\leq$1 X $10^{-10}$ | 5 | 3 | | mV |
| Input Maximum Offset Voltage | SliceP, SliceN = VCC | | 0.5 | | mV |
| Input Current | | | 10 | | µA |
| Input RMS Noise | BER = $\leq$1 X $10^{-10}$ | | 244 | | µVrms |
| **QUANTIZER-AC CHARACTERISTICS** | | | | | |
| Upper –3 dB Bandwidth | | | 1.9 | | GHz |
| Small Signal Gain | Differential | | 54 | | dB |
| S11 Maximum @ 2.5GHz, Figure 7 | | | -15 | | dB |
| Input Resistance | Single-Ended | | 50 | | Ω |
| Input Capacitance | | | 0.65 | | pF |
| Pulse Width Distortion | | | 10 | | ps |
| **QUANTIZER SLICE ADJUSTMENT** | | | | | |
| Gain (Threshold/Vin) | Vin = SliceP-SliceN | 0.131 | | 0.134 | V/V |
| Control Voltage Range | SliceP-SliceN | -0.8 | | 0.8 | V |
| Control Voltage Range | SliceP or SliceN | 1.3 | | VCC | V |
| Slice Threshold Offset | Full input range | -1.0 | | 1.0 | mV |
| **LEVEL DETECT** | | | | | |
| Level Detect Range (See Figure 4) | $R_{THRESH}$ = 0Ω | 2 | 3 | 4 | mV |
| | $R_{THRESH}$ = 10kΩ | 6 | 8.8 | 12 | mV |
| | $R_{THRESH}$ = 200kΩ | 15 | 17 | 21 | mV |
| Response Time | DC Coupled | 0.1 | 3 | 5 | µs |
| Hysterises (Electrical), AC Coupled Signal | $R_{THRESH}$ = 0Ω | | 5 | 7 | dB |
| | $R_{THRESH}$ = 10kΩ | | 5 | 7 | dB |
| | $R_{THRESH}$ = 200kΩ | | 5 | 7 | dB |
| SDOUT output Logic High | Load = +2mA (ADN2812 Sources I) | 2.7 | 3 | | V |
| SDOUT output Logic Low | Load = -2mA (ADN2812 Sinks I) | | 0.2 | 0.4 | V |
| Level Detect Output is a logic "1" LVCMOS Compatible with no signal present. | | | | | |
| **POWER SUPPLY VOLTAGE** | $V_{MIN}$ to $V_{MAX}$ | 3.0 | | 3.6 | V |
| **POWER SUPPLY CURRENT** | $V_{MIN}$ to $V_{MAX}$ | 140 | 236 | 380 | mA |
| **PHASE-LOCKED LOOP CHARACTERISTICS** | **NOTE: SONET SPECS APPEAR IN BOLD** | | | | |
| JITTER TRANSFER BANDWIDTH | OC-48 | | 370 | **2000** | KHz |
| (See Figure 5 and Table 1) | Gigabit Ethernet | | 185 | 1000 | KHz |
| | OC-12 | | 93 | **500** | KHz |
| | OC-3 | | 23 | **130** | KHz |
| JITTER TOLERANCE TRACKING BANDWIDTH | OC-48 | **1.0** | 4.8 | | MHz |
| (See Figure 5 and Table 1) | Gigabit Ethernet | 0.5 | 4.8 | | MHz |
| | OC-12 | **0.25** | 4.8 | | MHz |
| | OC-3 | **0.065** | 4.8 | | MHz |
| JITTER TOLERANCE (OC-48) | 600 Hz | | 80 | | UIp-p |
| | 6 KHz | | >20[2] | | UIp-p |
| | 100 MHz | | 5.5 | | UIp-p |
| | 1 MHz | | **>0.6**[2] | | UIp-p |
| JITTER GENERATION | | | | | |
| (12kHz to 20MHz) | OC-48 | | 0.003 | **0.01** | UI rms |
| | | | 0.03 | **0.1** | UIp-p |
| (12kHz to 10MHz) | Gigabit Ethernet | | 0.003 | 0.01 | UI rms |
| | | | 0.03 | 0.1 | UIp-p |
| (12kHz to 5MHz) | OC-12 | | 0.003 | **0.01** | UI rms |
| | | | 0.03 | **0.1** | UIp-p |
| (12kHz to 1.3MHz) | OC-3 | | 0.003 | **0.01** | UI rms |
| | | | 0.03 | **0.1** | UIp-p |

## ADN2809 ELECTRICAL CHARACTERISTICS at $T_A=T_{MIN}$ to $T_{MAX}$, $V_{CC}=V_{MIN}$ to $V_{MAX}$, $V_{EE}=0V$, $C_F=4.7\mu F$, 20 ohm ESR for xo unless otherwise noted

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| JITTER PEAKING MAXIMUM | OC-48 | | **0.1** | | dB |
| | Gigabit Ethernet | | 0.1 | | dB |
| | OC-12 | | **0.1** | | dB |
| | OC-3 | | **0.1** | | dB |
| **CML OUTPUT FORMAT** | | | | | |
| Single-Ended Output Voltage Swing $V_{SE}$ | See Figure 2 and Figure 6 | 300 | 430 | 550 | mV |
| Differential Output Voltage Swing $V_{DIFF}$ | See Figure 2 and Figure 6 | 600 | 860 | 1100 | mV |
| Rise Time ($t_R$) | 20% - 80% | | | 150 | pS |
| Fall Time ($t_F$) | 80% - 20% | | | 150 | pS |
| Output High Voltage $V_{OH}$ | Figure 6 | | VCC | | V |
| Output Low Voltage $V_{OL}$ | Figure 6 | VCC-0.55 | | VCC-0.32 | V |
| Data Setup Time $T_S$ (Figure 1) | OC48 | 150 | | | pS |
| | Gigabit Ethernet | 350 | | | pS |
| | OC12 | 750 | | | pS |
| | OC3 | 3150 | | | pS |
| Data Hold Time $T_H$ (Figure 1) | OC48 | 150 | | | pS |
| | Gigabit Ethernet | 350 | | | pS |
| | OC12 | 750 | | | pS |
| | OC3 | 3150 | | | pS |
| **TEST DATA DC CHARACTERISTICS** | | | | | |
| Input Voltage Swing $V_{SE}$ (Figure 2) | Single-Ended | 0.06 | | 0.8 | V |
| Input Voltage Range | Single-Ended | 2.3 | | VCC+0.4 | V |
| **LVTTL DC CHARACTERISTICS** | | | | | |
| $V_{OH}$ Output High Voltage | $I_{OH}$ = -100uA (ADN2809 Sources I) | 2.4 | | | V |
| $V_{OL}$ Output Low Voltage | $I_{OL}$ = 1.0mA (ADN2809 Sinks I) | | | 0.5 | V |
| $V_{IH}$ Input High Voltage | | 2.0 | | | V |
| $V_{IL}$ Input Low Voltage | | | | 0.8 | V |
| $I_{IH}$ Input High Current | Vin = +2.4 V @ +25C | | | 50 | µA |
| $I_{IL}$ Input Low Current | Vin = +0.5 V @ +25C | -500 | | | µA |
| **REFCLK DC CHARACTERISTICS** | | | | | |
| Input Voltage Swing $V_{SE}$ (Figure 2) | Single-Ended | 0.032 | | VCC | V |
| Input Voltage Range | Single-Ended | 0 | | VCC | V |

Note: (1) Recommended for Optimum Sensitivity.
Note: (2) Equipment Limitation.

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage..... ...+8 V
Input Voltage (pin x or pin xto Vcc).... ..... .TBD
Maximum Junction Temperature.....165 deg C
Storage Temperature Range..... ..... -65 deg C to +150 deg C
Lead Temperature (Soldering 10 sec).. ..... ....300 deg C
ESD Rating (human body model)..... ..... ..TBD

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ORDERING GUIDE

| MODEL | TEMP RANGE | Package Descript-ion | Option |
|---|---|---|---|
| ADN2809XCP | -40/+85°C | LFCSP-16 | CP-16 |
| ADN2809XCP-RL | -40/+85°C | LFCSP-16 2500 Pieces | CP-16 |

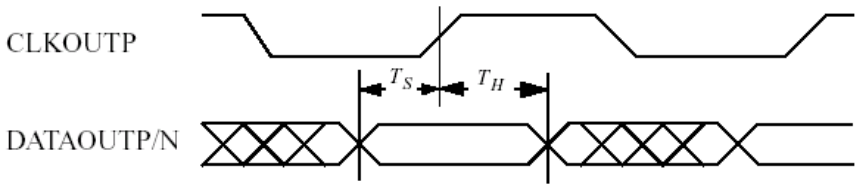



*Figure 1. Output Timing definitions*

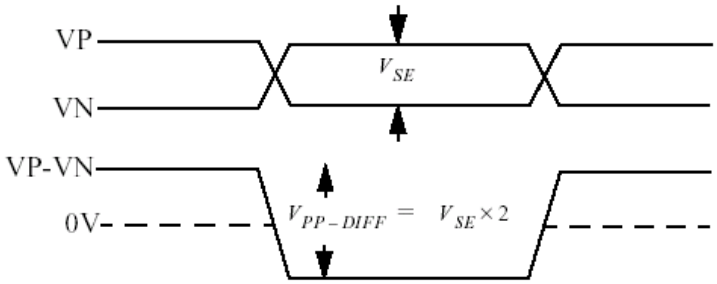



*Figure 2. Signal Level Definition*

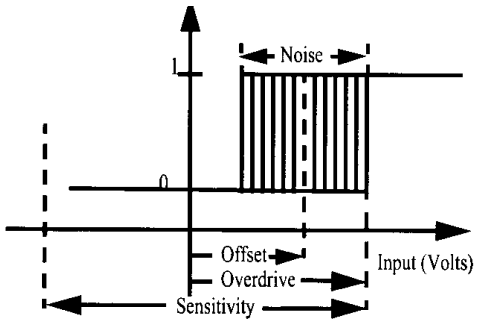



*Figure 3. Quantizer Signal Definitions*

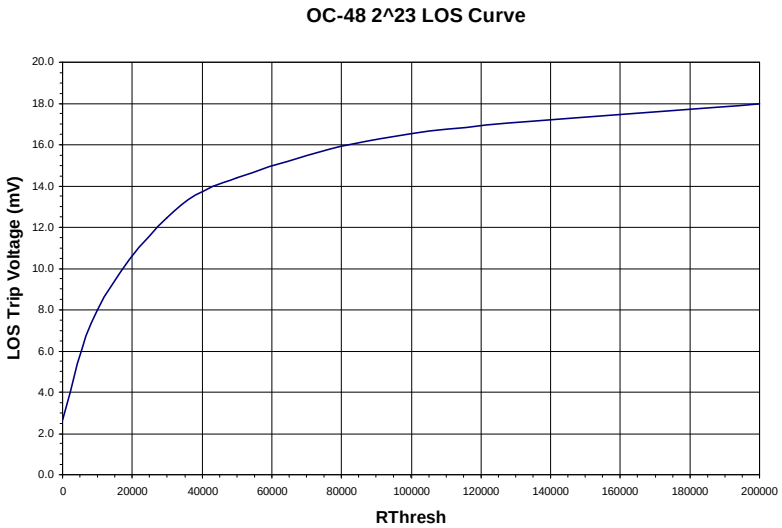



*Figure 4. LOS Comparator Trip Point Programming*

| Rate | Jitter Transfer | | | Jitter Tolerance | | |
|---|---|---|---|---|---|---|
| | SONET Spec | ADN2809 | Margin | SONET spec | ADN2809 | Margin |
| OC48 | 2MHz | 370kHz | 5.4 | 1MHz | 4.77MHz | 4.8 |
| GbE | 1MHz | 185kHz | 5.4 | 500kHz | 4.77MHz | 9.6 |
| OC12 | 500kHz | 93kHz | 5.4 | 250kHz | 4.77MHz | 19.2 |
| OC3 | 130kHz | 23kHz | 5.6 | 65kHz | 4.77MHz | 73.4 |

*Table I. Typical Jitter Transfer and Jitter Tolerance Performance*

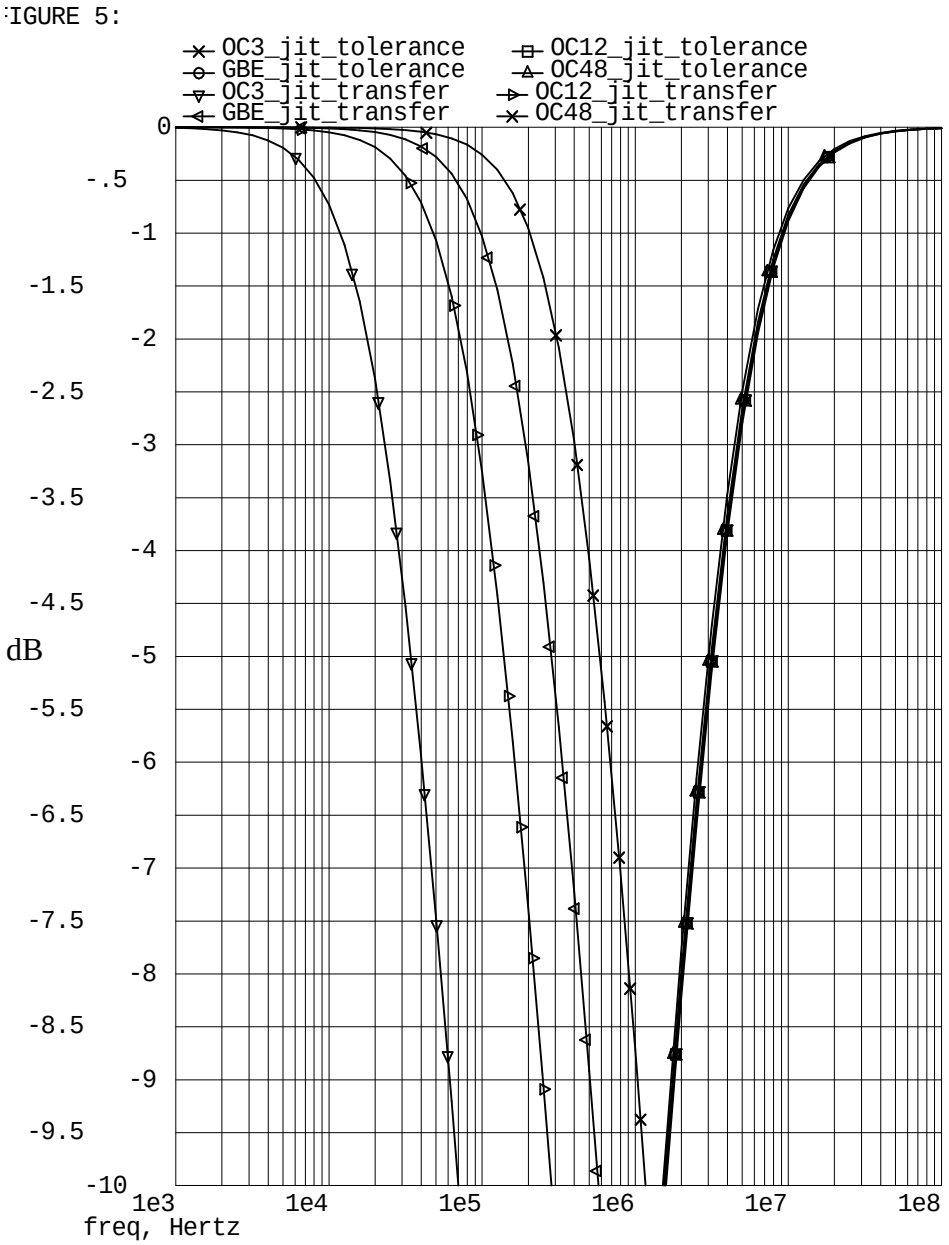



*Figure 5. Tracking Bandwidth and Jitter Filtering*

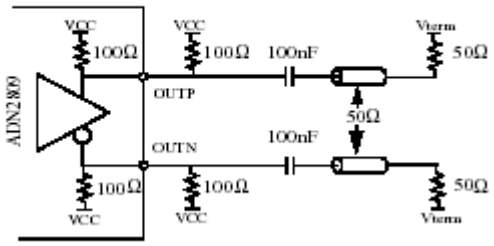



*Figure 6. Recommended AC Output Termination*

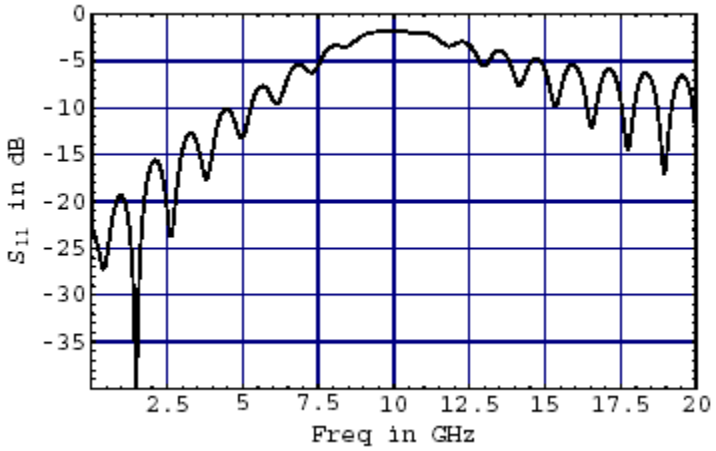



*Figure 7. ADN2809 S11 vs. Frequency*

**THEORY OF OPERATION**

The ADN2809 is a delay- and phase-locked loop circuit for clock recovery and data retiming from an NRZ encoded data stream. The phase of the input data signal is tracked by two separate feedback loops which share a common control voltage. A high speed delay- locked loop path uses a voltage controlled phase shifter to track the high frequency components of input jitter. A separate phase control loop, comprised of the vco, tracks the low frequency components of input jitter. The initial frequency of the vco is set by yet a third loop which compares the vco frequency with the reference frequency and sets the coarse tuning voltage. The jitter tracking phase-locked loop controls the vco by the fine tuning control.

The delay- and phase- loops together track the phase of the input data signal. For example, when the clock lags input data, the phase detector drives the vco to higher frequency, and also, increases the delay through the phase shifter: these actions both serve to reduce the phase error between the clock and data. The faster clock picks up phase while the delayed data loses phase. Since the loop filter is an integrator, the static phase error will be driven to zero.

Another view of the circuit is that the phase shifter implements the zero required for frequency compensation of a second order phase-locked loop, and this zero is placed in the feedback path and thus, does not appear in the closed-loop transfer function. Jitter peaking in a conventional second order phase-locked loop is caused by the presence of this zero in the closed-loop transfer function. Since this circuit has no zero in the closed-loop transfer, jitter peaking is minimized.

The delay- and phase- loops together simultaneously provide wide-band jitter accommodation and narrow-band jitter filtering. The linearized block diagram in Figure 8 shows the jitter transfer function , Z(s)/X(s), is a second order low pass providing excellent filtering. Note the jitter transfer has no zero, unlike an ordinary second order phase-locked loop. This means that the main PLL loop has low jitter peaking, see Figure 9. This makes this circuit ideal for signal regenerator applications where jitter peaking in a cascade of regenerators can contribute to hazardous jitter accumulation.

The error transfer, e(s)/X(s), has the same high pass form as an ordinary phase-locked loop. This transfer function is free to be optimized to give excellent wide-band jitter accommodation since the jitter transfer function, Z(s)/X(s), provides the narrow-band jitter filtering. See Figure 5 for a table of error transfer bandwidths and jitter transfer bandwidths at the various data rates.

The delay- and phase- loops contribute to overall jitter accommodation. At low frequencies of input jitter on the data signal, the integrator in the loop filter provides high gain to track large jitter amplitudes with small phase error. In this case the vco is frequency modulated and jitter is tracked as in an ordinary phase-locked loop. The amount of low frequency jitter that can be tracked is a function of the vco tuning range. A wider tuning range gives larger accommodation of low frequency jitter. The internal loop control voltage remains small for small phase errors, so the phase shifter remains close to the center of its range and thus contributes little to the low frequency jitter accommodation.

At medium jitter frequencies, the gain and tuning range of the vco are not large enough to track input jitter. In this case the vco control voltage becomes large and saturates and the vco frequency dwells at one or the other extreme of its tuning range. The size of the vco tuning range, therefore has only a small effect on the jitter accommodation. The delay-locked loop control voltage is now larger, and so the phase shifter takes on the burden of tracking the input jitter. The phase shifter range, in UI, can be seen as a broad plateau on the jitter tolerance curve . The phase shifter has a minimum range of 2UI at all data rates.

The gain of the loop integrator is small for high jitter frequencies, so that larger phase differences are needed to make the loop control voltage big enough to tune the range of the phase shifter. Large phase errors at high jitter frequencies cannot be tolerated. In this region the gain of the integrator determines the jitter accommodation. Since the gain of the loop integrator declines linearly with frequency, jitter accommodation is lower with higher jitter frequency. At the highest frequencies, the loop gain is very small, and little tuning of the phase shifter can be expected. In this case, jitter accommodation is determined by the eye opening of the input data, the static phase error, and the residual loop jitter generation. The jitter accommodation is roughly 0.5UI in this region. The corner frequency between the declining slope and the flat region is the closed loop bandwidth of the delay-locked loop, which is roughly 3MHz for all data rates.

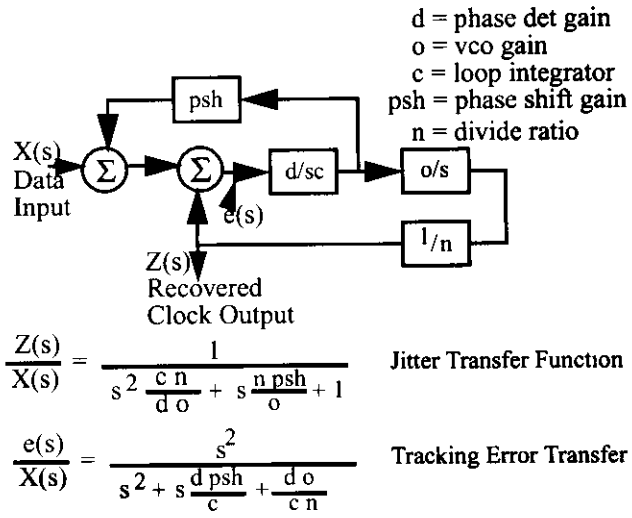



*Figure 8. ADN2809 Architecture*

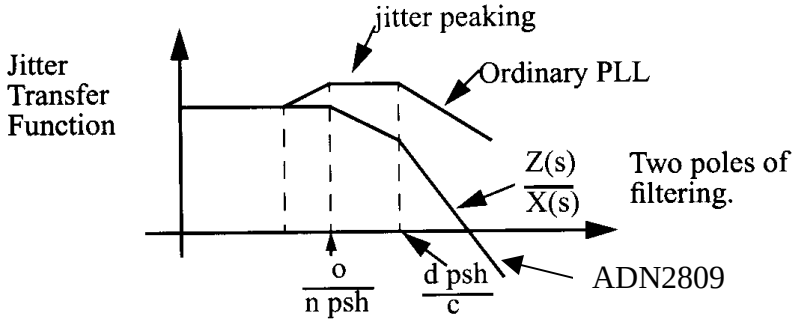



*Figure 9. ADN2809 Jitter Response vs. Conventional PLL*

## FUNCTIONAL DESCRIPTION

### Limiting Amplifier / Bypass & Loopback

The limiting amplifier has differential inputs (PIN/NIN), which are normally AC coupled to the internal 50 ohm termination (although DC coupling is possible). Input offset is factory trimmed to achieve better than 6mV typical sensitivity with minimal drift. The Quantizer Slicing level can be offset by +/-100mV to mitigate the effect of ASE (amplified spontaneous emission) noise by a differential voltage input of +/-0.8V applied to 'SLICEP/N' inputs. If no adjustment of the slice level is needed, SLICEP/N should be tied to VCC.

When the 'Bypass' input is driven to a TTL high state, the Quantizer output is connected directly to the buffers driving the Data Out pins, thus bypassing the clock recovery circuit (Figure 10). This feature can help the system to deal with non standard bit rates. The loopback mode can be invoked by driving the 'LOOPEN' pin to a TTL high state, which facilitates system diagnostic testing. This will connect the Test inputs (TDINP/N) to the clock and data recovery circuit (per Figure 10). The Test inputs can be left floating, when not in use. They accept AC or DC coupled signal levels, or AC coupled LVDS.

### Loss of Signal (LOS) Detector

The receiver front end Signal Detect circuit indicates when the input signal level has fallen below a user adjustable threshold. The threshold is set with a single external resistor, as illustrated in figure 4, which assumes that the slice inputs are inactive.

If the LOS detector is used the Quantizer Slice Adjust pins must both be tied to VCC, to avoid interaction with the LOS threshold level. Note that it is not expected to use both LOS and Slice Adjust at the same time: systems with optical amplifiers need the slice adjust to evade ASE, but a loss of signal causes the optical amplifier output to be full scale noise, thus the LOS would not detect the failure. In this case the Loss of Lock signal will indicate the failure.

### Reference Clock

The ADN2809 can accept any of the following reference clock frequencies: 19.44 MHz, 38.88MHz, 77.76MHz at LVTTL/LVCMOS/LVPECL/LVDS levels or 155.52MHz at LVPECL/LVDS levels via the REFCLKN/P inputs, independent of data rate (including gigabit ethernet). The input buffer accepts any differential signal with a peak to peak differential amplitude of greater than 64mV (e.g. LVPECL or LVDS) or a standard single ended low voltage TTL input, providing maximum system flexibility. The appropriate division ratio can be selected using the REFSEL0/1 pins, according to Table 3. Phase noise and duty cycle of the Reference Clock are not critical and 100ppm accuracy is sufficient.

A crystal oscillator is also provided, as an alternative to using the REFCLKN/P input. Details of the recommended crystal are given in Table 3.

REFSEL must be tied to VCC when the REFCLKN/P inputs are active, or tied to VEE when the oscillator is used. No connection between the XO pin and REFCLK input is necessary (see figure 11). Please note that the crystal should operate in series resonant mode, which renders it insensitive to external parasitics. No trimming capacitors are required.

### Lock Detector Operation

The lock detector monitors the frequency difference between the VCO and the reference clock, and de-asserts the 'Loss of Lock' signal when the VCO is within 500ppm of center frequency. This enables the phase loop which then maintains phase lock, unless the frequency error exceeds 0.1%. Should this occur, the 'Loss of Lock' signal is re-asserted and control returns to the frequency loop which will re-acquire, and maintain a stable clock signal at the output. The frequency loop requires a single external capacitor between CF1 and CF2. The capacitor specification is given in Table 5.

### Squelch Mode

When the 'Squelch' input is driven to a TTL high state, both the clock and data outputs are set to the zero state, to suppress downstream processing. If desired, this pin can be directly driven by the LOS (Loss-Of-Signal) or LOL (Loss-Of-Lock) detector outputs. If the Squelch function is not required, the pin should be tied to VEE.

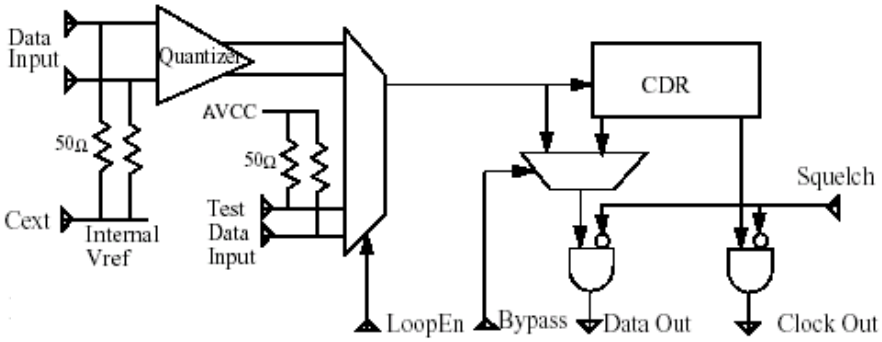



*Figure 10. Test Modes*

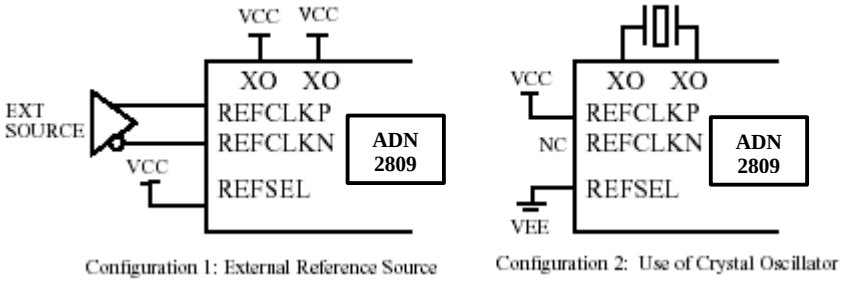
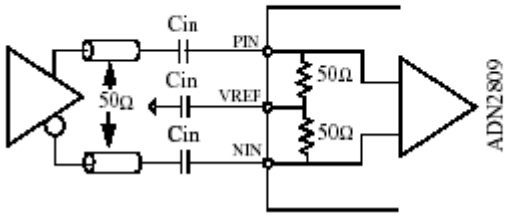



*Figure 11. Reference Sources*




Note:

The value of Cin required depends on the data rate, # Consecutive Identical Digits (CID) and amount of Patter Dependent Jitter (PDJ) which can be tolerated. e.g. for 1000 CID and <0.01UI pk-pk PDJ, 100nF is needed at OC48 and 1.6uF at OC3.

*Figure 12. Data Input Terminations*

**TABLE 2. Data Rate Selection**

| SEL2 | SEL0 | SEL1 | Rate | Frequency |
|---|---|---|---|---|
| 0 | 0 | 0 | OC48 | 2.48832 GHz |
| 0 | 0 | 1 | Gigabit Ethernet | 1.25 GHz |
| 0 | 1 | 0 | OC12 | 622.08 MHz |
| 0 | 1 | 1 | OC3 | 155.52 MHz |
| 1 | 0 | 0 | OC48 * 15/14 | 2.666 GHz |
| 1 | 0 | 1 | Gigabit Ethernet * 15/14 | 1.339 GHz |
| 1 | 1 | 0 | OC12 * 15/14 | 666.51 MHz |
| 1 | 1 | 1 | OC3 * 15/14 | 166.63 MHz |

**TABLE 3. Reference Frequency Selection**

| REFSEL1 | REFSEL0 | Applied Reference Frequency |
|---|---|---|
| 0 | 0 | 19.44 MHz |
| 0 | 1 | 38.88 MHz |
| 1 | 0 | 77.76 MHz |
| 1 | 1 | 155.52 MHz |

**TABLE 4. Crystal Specification - see note (3)**

| Parameter | Value |
|---|---|
| Mode | Series Resonant |
| Frequency / Overall Stability | 19.44 MHz / +/- 50 ppm |
| Frequency Accuracy | +/- 50 ppm / total Temp. Stability |
| Temp. Stability | |
| Ageing | |
| ESR | 20 ohms max |

(3) No additional external components are required

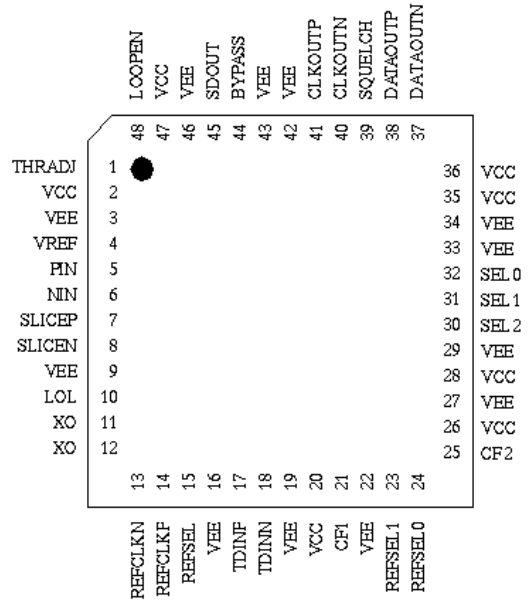
**TABLE 5. Recommended Capacitor Specification**

| Parameter | Value |
|---|---|
| Capacitance | (-40C to 85C) >3.0uF |
| Leakage | (-40C to 85C) <80nA |
| Rating | >6.3V |

**ADN2809 PIN DESCRIPTION**

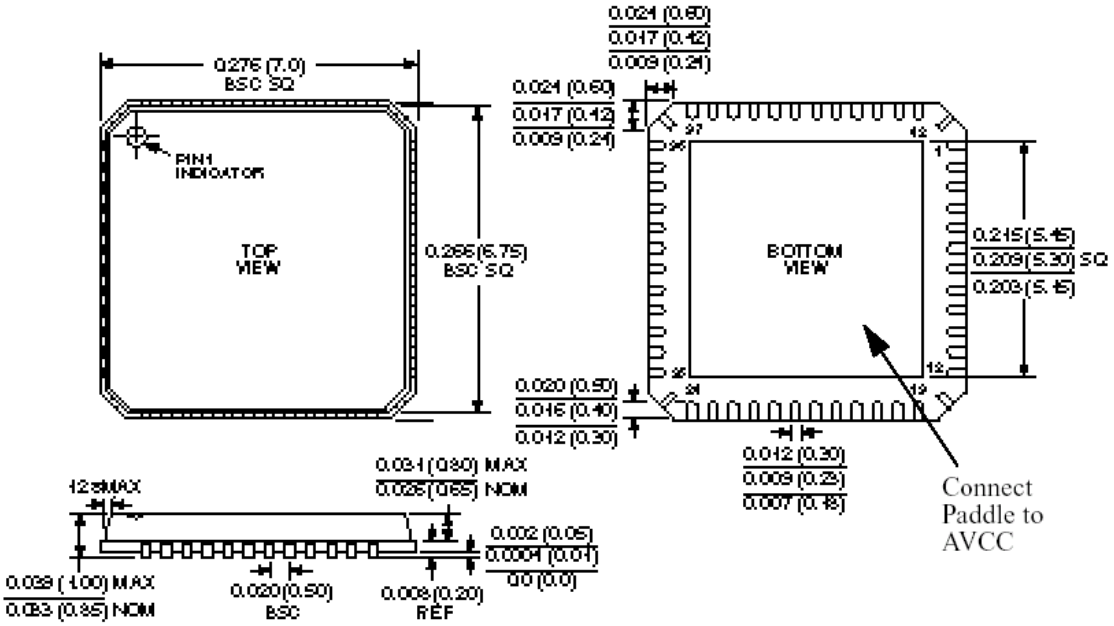
| Pin No. | Name | I/O | Level | Description |
|---|---|---|---|---|
| 2,26,28, Exposed Pad | VCC | P | 3.3V | Analog Power |
| 3,9,27,29, 42 | VEE | G | 0V | Analog ground |
| 20,35,36,47 | VCC | P | 3.3V | Digital supply |
| 1 | THRADJ | I/O | Analog I/O | LOS threshold setting resistor |
| 4 | VREGF | I/O | Analog I/O | Reference capacitor |
| 5 | PIN | I | Analog current | Differential data signal input |
| 6 | NIN | I | Analog current | Differential data signal input |
| 7 | SLICEP | I | Analog voltage | Slice level |
| 8 | SLICEN | I | Analog voltage | Slice level |
| 10 | LOL | O | LVTTL / LVCMOS | High level indicates loss of lock |
| 11 | XO | O | Analog output | Crystal oscillator |
| 12 | XO | O | Analog output | Crystal oscillator |
| 13 | REFCLKN | I | Any | Differential reference clock |
| 14 | REFCLKP | I | Any | Differential reference clock |
| 15 | REFSEL | I | LVTTL / LVCMOS | Reference source select |
| 17 | TDINP | I | CML | Differential test data input |
| 18 | TDINN | I | CML | Differential test data input |
| 21 | CF1 | I/O | Analog I/O | Frequency loop capacitor |
| 23 | REFSEL1 | I | LVTTL / LVCMOS | Reference rate select |
| 24 | REFSEL0 | I | LVTTL / LVCMOS | Reference rate select |
| 25 | CF2 | I/O | Analog I/O | Frequency loop capacitor |
| 30 | SEL2 | I | LVTTL / LVCMOS | Data rate select |
| 31 | SEL1 | I | LVTTL / LVCMOS | Data rate select |
| 32 | SEL0 | I | LVTTL / LVCMOS | Data rate select |
| 37 | DATAOUTN | O | CML | Differential recovered data |
| 38 | DATAOUTP | O | CML | Differential recovered data |
| 39 | SQUELCH | I | LVTTL / LVCMOS | Disable clock and data outputs |
| 40 | CLKOUTN | O | CML | Differential retimed clock |
| 41 | CLKOUTP | O | CML | Differential retimed clock |
| 44 | BYPASS | I | LVTTL / LVCMOS | Disable clock and data recovery |
| 45 | SDOUT | O | LVTTL / LVCMOS | High level indicates loss of signal |
| 48 | LOOPEN | I | LVTTL / LVCMOS | Enable high speed test data inputs |

**ADN2809 PIN CONFIGURATION**



## Mechanical Outline Dimensions

Dimensions shown in millimeters and (inches).




CONTROLLING DIMENSIONS ARE IN MILLIMETERS