I²C® CMOS 8 × 12 Unbuffered Analog Switch Array With Dual/Single Supplies

ADG2128

FEATURES

- I²C-compatible interface
  - 3.4 MHz high speed I²C option
- 32-lead LFCSP_VQ (5 mm × 5 mm)
- Double-buffered input logic
  - Simultaneous update of multiple switches
- Up to 300 MHz bandwidth
- Fully specified at dual ±5 V/single +12 V operation
- On resistance 35 Ω maximum
- Low quiescent current < 20 µA

APPLICATIONS

- AV switching in TV
- Automotive infotainment
- AV receivers
- CCTV
- Ultrasound applications
- KVM switching
- Telecom applications
- Test equipment/instrumentation
- PBX systems

GENERAL DESCRIPTION

The ADG2128 is an analog cross point switch with an array size of 8 × 12. The switch array is arranged so that there are eight columns by 12 rows, for a total of 96 switch channels. The array is bidirectional, and the rows and columns can be configured as either inputs or outputs. Each of the 96 switches can be addressed and configured through the I²C-compatible interface. Standard, full speed, and high speed (3.4 MHz) I²C interfaces are supported. Any simultaneous switch combination is allowed. An additional feature of the ADG2128 is that switches can be updated simultaneously, using the LDSW command. In addition, a $\overline{\text{RESET}}$ option allows all of the switch channels to be reset/off. At power-on, all switches are in the off condition. The device is packaged in a 32-lead, 5 mm × 5 mm LFCSP_VQ.

FUNCTIONAL BLOCK DIAGRAM

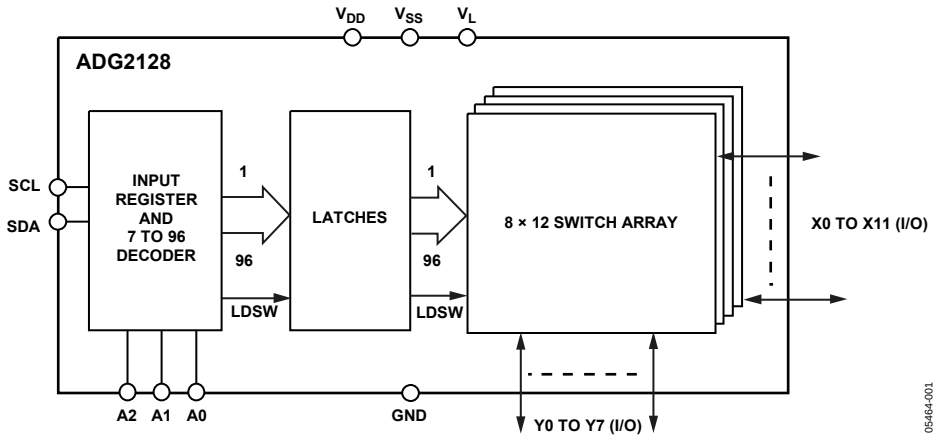

Figure 1.

Rev. A

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5/06—Rev. 0 to Rev. A

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1/06—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, V_L = 5 V, GND = 0 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 1.

	B Version		Y Version			
Parameter	**+25°C**	**−40°C to +85°C**	**+25°C**	**−40°C to +125°C**	**Unit**	**Conditions**
ANALOG SWITCH						
Analog Signal Range		V_{DD} − 2 V		V_{DD} − 2 V	V max	
On Resistance, R_{ON}	30		30		Ω typ	V_{DD} = +10.8 V, V_{IN} = 0 V, I_S = −10 mA
	35	40	35	42	Ω max	
	32		32		Ω typ	V_{DD} = +10.8 V, V_{IN} = +1.4 V, I_S = −10 mA
	37	42	37	47	Ω max	
	45		45		Ω typ	V_{DD} = +10.8 V, V_{IN} = +5.4 V, I_S = −10 mA
	50	57	50	62	Ω max	
On Resistance Matching	4.5		4.5		Ω typ	V_{DD} = +10.8 V, V_{IN} = 0 V, I_S = −10 mA
Between Channels, ΔR_{ON}	8	9	8	10	Ω max	
On Resistance Flatness, $R_{FLAT(ON)}$	2.3		2.3		Ω typ	V_{DD} = 10.8 V, V_{IN} = 0 V to +1.4 V, I_S = −10 mA
	3.5	4	3.5	5	Ω max	
	14.5		14.5		Ω typ	V_{DD} = 10.8 V, V_{IN} = 0 V to +5.4 V, I_S = −10 mA
	18	20	18	22	Ω max	
LEAKAGE CURRENTS						V_{DD} = 13.2 V
Channel Off Leakage, I_{OFF}	±0.03		±0.03		µA typ	V_X = 7 V/1 V, V_Y = 1 V/7 V
Channel On Leakage, I_{ON}	±0.03		±0.03		µA typ	V_X = V_Y = 1 V or 7 V
DYNAMIC CHARACTERISTICS[2]						
C_{OFF}	11		11		pF typ	
C_{ON}	18.5		18.5		pF typ	
t_{ON}	170		170		ns typ	R_L = 300 Ω, C_L = 35 pF
	185	190	185	195	ns max	
t_{OFF}	210		210		ns typ	R_L = 300 Ω, C_L = 35 pF
	250	255	250	260	ns max	
THD + N	0.04		0.04		% typ	R_L = 10 kΩ, f = 20 Hz to 20 kHz, V_S = 1 V p-p
PSRR			90		dB typ	f = 20 kHz; without decoupling; see Figure 24
−3 dB Bandwidth	210		210		MHz typ	Individual inputs to outputs
	16.5		16.5		MHz typ	8 inputs to 1 output
Off Isolation	−69		−69		dB typ	R_L = 75 Ω, C_L = 5 pF, f = 5 MHz
Channel-to-Channel Crosstalk						R_L = 75 Ω, C_L = 5 pF, f = 5 MHz
Adjacent Channels	−63		−63		dB typ	
Nonadjacent Channels	−76		−76		dB typ	
Differential Gain	0.4		0.4		% typ	R_L = 75 Ω, C_L = 5 pF, f = 5 MHz
Differential Phase	0.6		0.6		° typ	R_L = 75 Ω, C_L = 5 pF, f = 5 MHz
Charge Injection	−3.5		−3.5		pC typ	V_S = 4 V, R_S = 0 Ω, C_L = 1 nF
LOGIC INPUTS (Ax, $\overline{RESET}$)[2]						
Input High Voltage, V_{INH}		2.0		2.0	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Leakage Current, I_{IN}	0.005		0.005		µA typ	
		±1		±1	µA max	
Input Capacitance, C_{IN}	7		7		pF typ	

Parameter	B Version +25°C	B Version −40°C to +85°C	Y Version +25°C	Y Version −40°C to +125°C	Unit	Conditions
LOGIC INPUTS (SCL, SDA)[2]						
Input High Voltage, V_{INH}		0.7 V_L		0.7 V_L	V min	
		V_L + 0.3		V_L + 0.3	V max	
Input Low Voltage, V_{INL}		−0.3		−0.3	V min	
		0.3 V_L		0.3 V_L	V max	
Input Leakage Current, I_{IN}	0.005		0.005		µA typ	V_{IN} = 0 V to V_L
		±1		±1	µA max	
Input Hysteresis		0.05 V_L		0.05 V_L	V min	
Input Capacitance, C_{IN}	7		7		pF typ	
LOGIC OUTPUT (SDA)[2]						
Output Low Voltage, V_{OL}		0.4		0.4	V max	I_{SINK} = 3 mA
		0.6		0.6	V max	I_{SINK} = 6 mA
Floating State Leakage Current		±1		±1	µA max	
POWER REQUIREMENTS						
I_{DD}	0.05		0.05		µA typ	Digital inputs = 0 V or V_L
		1		1	µA max	
I_{SS}	0.05		0.05		µA typ	Digital inputs = 0 V or V_L
		1		1	µA max	
I_L						Digital inputs = 0 V or V_L
Interface Inactive	0.3		0.3		µA typ	
		2		2	µA max	
Interface Active: 400 kHz f_{SCL}	0.1		0.1		mA typ	
		0.2		0.2	mA max	
Interface Active: 3.4 MHz f_{SCL}	0.4		0.4		mA typ	-HS model only
		1.2		1.7	mA max	

[1] Temperature range is as follows: B version: −40°C to +85°C; Y version: −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, V_L = 5 V, GND = 0 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 2.

Parameter	B Version +25°C	B Version −40°C to +125°C	Y Version +25°C	Y Version −40°C to +125°C	Unit	Conditions
ANALOG SWITCH						
Analog Signal Range				V_{DD} − 2 V	V max	
On Resistance, R_{ON}	34		34		Ω typ	V_{DD} = +4.5 V, V_{SS} = −4.5 V, V_{IN} = V_{SS}, I_S = −10 mA
	40	45	40	50	Ω max	
	50		50		Ω typ	V_{DD} = +4.5 V, V_{SS} = −4.5 V, V_{IN} = 0 V, I_S = −10 mA
	55	65	55	70	Ω max	
	66		66		Ω typ	V_{DD} = +4.5 V, V_{SS} = −4.5 V, V_{IN} = +1.4 V, I_S = −10 mA
	75	85	75	95	Ω max	
On Resistance Matching	4.5		4.5		Ω typ	V_{DD} = +4.5 V, V_{SS} = −4.5 V, V_{IN} = V_{SS}, I_S = −10 mA
Between Channels, ΔR_{ON}	8	9	8	10	Ω max	
On Resistance Flatness, $R_{FLAT(ON)}$	17		17		Ω typ	V_{DD} = +4.5 V, V_{SS} = −4.5 V, V_{IN} = V_{SS} to 0 V, I_S = −10 mA
	20	23	20	25	Ω max	
	34		34		Ω typ	V_{DD} = +4.5 V, V_{SS} = −4.5 V, V_{IN} = V_{SS} to +1.4 V, I_S = −10 mA
	42	45	42	48	Ω max	
LEAKAGE CURRENTS						V_{DD} = 5.5 V, V_{SS} = 5.5 V
Channel Off Leakage, I_{OFF}	±0.03		±0.03		µA typ	V_X = +4.5 V/−2 V, V_Y = −2 V/+4.5 V
Channel On Leakage, I_{ON}	±0.03		±0.03		µA typ	V_X = V_Y = −2 V or +4.5 V
DYNAMIC CHARACTERISTICS[2]						
C_{OFF}	6		6		pF typ	
C_{ON}	9.5		9.5		pF typ	
t_{ON}	170		170		ns typ	R_L = 300 Ω, C_L = 35 pF
	200	215	200	220	ns max	
t_{OFF}	210		210		ns typ	R_L = 300 Ω, C_L = 35 pF
	250	255	250	260	ns max	
THD + N	0.04		0.04		% typ	R_L = 10 kΩ, f = 20 Hz to 20 kHz, V_S = 1 V p-p
PSRR			90		dB typ	f = 20 kHz; without decoupling; see Figure 24
−3 dB Bandwidth	300		300		MHz typ	Individual inputs to outputs
	18		18		MHz typ	8 inputs to 1 output
Off Isolation	−66		−64		dB typ	R_L = 75 Ω, C_L = 5 pF, f = 5 MHz
Channel-to-Channel Crosstalk						R_L = 75 Ω, C_L = 5 pF, f = 5 MHz
Adjacent Channels	−62		−62		dB typ	
Nonadjacent Channels	−79		−79		dB typ	
Differential Gain	1.5		1.5		% typ	R_L = 75 Ω, C_L = 5 pF, f = 5 MHz
Differential Phase	1.8		1.8		° typ	R_L = 75 Ω, C_L = 5 pF, f = 5 MHz
Charge Injection	−3		−3		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF
LOGIC INPUTS (Ax, $\overline{RESET}$)[2]						
Input High Voltage, V_{INH}		2.0		2.0	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Leakage Current, I_{IN}	0.005		0.005		µA typ	
		±1		±1	µA max	
Input Capacitance, C_{IN}	7		7		pF typ	
LOGIC INPUTS (SCL, SDA)[2]						
Input High Voltage, V_{INH}		0.7 V_L		0.7 V_L	V min	
		V_L + 0.3		V_L + 0.3	V max	
Input Low Voltage, V_{INL}		−0.3		−0.3	V min	
		0.3 V_L		0.3 V_L	V max	

Parameter	B Version +25°C	B Version −40°C to +125°C	Y Version +25°C	Y Version −40°C to +125°C	Unit	Conditions
Input Leakage Current, I_{IN}	0.005		0.005		µA typ	V_{IN} = 0 V to V_L
		±1		±1	µA max	
Input Hysteresis		0.05 V_L		0.05 V_L	V min	
Input Capacitance, C_{IN}	7		7		pF typ	
LOGIC OUTPUT (SDA)[2]						
Output Low Voltage, V_{OL}		0.4		0.4	V max	I_{SINK} = 3 mA
		0.6		0.6	V max	I_{SINK} = 6 mA
Floating State Leakage Current		±1		±1	µA max	
POWER REQUIREMENTS						
I_{DD}	0.05		0.005		µA typ	Digital inputs = 0 V or V_L
		1		1	µA max	
I_{SS}	0.05		0.005		µA typ	Digital inputs = 0 V or V_L
		1		1	µA max	
I_L						Digital inputs = 0 V or V_L
Interface Inactive	0.3		0.3		µA typ	
		2		2	µA max	
Interface Active: 400 kHz f_{SCL}	0.1		0.1		mA typ	
		0.1		0.1	mA max	
Interface Active: 3.4 MHz f_{SCL}	0.4		0.4		mA typ	-HS model only
		0.3		0.3	mA max	

[1] Temperature range is as follows: B version: −40°C to +85°C; Y version: −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

I²C TIMING SPECIFICATIONS

V_{DD} = 5 V to 12 V; V_{SS} = −5 V to 0 V; V_L = 5 V; GND = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted (see Figure 2).

Table 3.

Parameter[1]	Conditions	ADG2108 Limit at T_{MIN}, T_{MAX} Min	Max	Unit	Description
f_{SCL}	Standard mode		100	kHz	Serial clock frequency
	Fast mode		400	kHz	
	High speed mode[2]				
	C_B = 100 pF maximum		3.4	MHz	
	C_B = 400 pF maximum		1.7	MHz	
t_1	Standard mode	4		µs	t_{HIGH}, SCL high time
	Fast mode	0.6		µs	
	High speed mode[2]				
	C_B = 100 pF maximum	60		ns	
	C_B = 400 pF maximum	120		ns	
t_2	Standard mode	4.7		µs	t_{LOW}, SCL low time
	Fast mode	1.3		µs	
	High speed mode[2]				
	C_B = 100 pF maximum	160		ns	
	C_B = 400 pF maximum	320		ns	
t_3	Standard mode	250		ns	$t_{SU;DAT}$, data setup time
	Fast mode	100		ns	
	High speed mode[2]	10		ns	
t_4[3]	Standard mode	0	3.45	µs	$t_{HD;DAT}$, data hold time
	Fast mode	0	0.9	µs	
	High speed mode[2]				
	C_B = 100 pF maximum	0	70	ns	
	C_B = 400 pF maximum	0	150	ns	
t_5	Standard mode	4.7		µs	$t_{SU;STA}$, setup time for a repeated start condition
	Fast mode	0.6		µs	
	High speed mode[2]	160		ns	
t_6	Standard mode	4		µs	$t_{HD;STA}$, hold time for a repeated start condition
	Fast mode	0.6		µs	
	High speed mode[2]	160		ns	
t_7	Standard mode	4.7		µs	t_{BUF}, bus free time between a stop and a start condition
	Fast mode	1.3		µs	
t_8	Standard mode	4		µs	$t_{SU;STO}$, setup time for a stop condition
	Fast mode	0.6		µs	
	High speed mode[2]	160		ns	
t_9	Standard mode		1000	ns	t_{RDA}, rise time of SDA signal
	Fast mode	20 + 0.1 C_B	300	ns	
	High speed mode[2]				
	C_B = 100 pF maximum	10	80	ns	
	C_B = 400 pF maximum	20	160	ns	
t_{10}	Standard mode		300	ns	t_{FDA}, fall time of SDA signal
	Fast mode	20 + 0.1 C_B	300	ns	
	High speed mode[2]				
	C_B = 100 pF maximum	10	80	ns	
	C_B = 400 pF maximum	20	160	ns	

Parameter[1]	Conditions	ADG2108 Limit at T_{MIN}, T_{MAX} Min	Max	Unit	Description
t_{11}	Standard mode		1000	ns	t_{RCL}, rise time of SCL signal
	Fast mode	20 + 0.1 C_B	300	ns	
	High speed mode[2]				
	C_B = 100 pF maximum	10	40	ns	
	C_B = 400 pF maximum	20	80	ns	
t_{11A}	Standard mode		1000	ns	t_{RCL1}, rise time of SCL signal after a repeated start condition and after an acknowledge bit
	Fast mode	20 + 0.1 C_B	300	ns	
	High speed mode[2]				
	C_B = 100 pF maximum	10	80	ns	
	C_B = 400 pF maximum	20	160	ns	
t_{12}	Standard mode		300	ns	t_{FCL}, fall time of SCL signal
	Fast mode	20 + 0.1 C_B	300	ns	
	High speed mode[2]				
	C_B = 100 pF maximum	10	40	ns	
	C_B = 400 pF maximum	20	80	ns	
t_{SP}	Fast mode	0	50	ns	Pulse width of suppressed spike
	High speed mode[2]	0	10	ns	

[1] Guaranteed by initial characterization. All values measured with input filtering enabled. C_B refers to capacitive load on the bus line; t_R and t_F are measured between 0.3 V_{DD} and 0.7 V_{DD}.
[2] High speed I²C is available only in -HS models.
[3] A device must provide a data hold time for SDA to bridge the undefined region of the SCL falling edge.

TIMING DIAGRAM

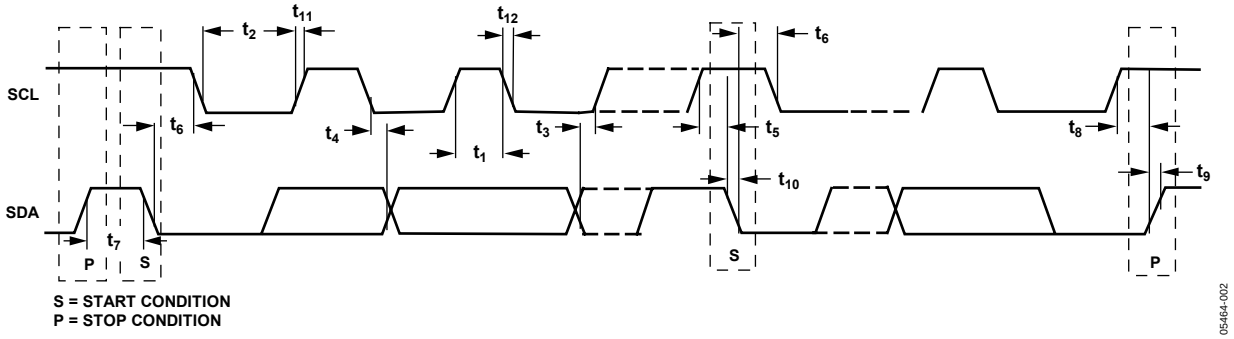

Figure 2. Timing Diagram for 2-Wire Serial Interface

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to V_{SS}	15 V
V_{DD} to GND	−0.3 V to +15 V
V_{SS} to GND	+0.3 V to −7 V
V_L to GND	−0.3 V to +7 V
Analog Inputs	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Digital Inputs	−0.3 V to V_L + 0.3 V or 30 mA, whichever occurs first
Continuous Current	
10 V on Input; Single Input Connected to Single Output	65 mA
1 V on Input; Single Input Connected to Single Output	90 mA
10 V on Input; Eight Inputs Connected to Eight Outputs	25 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
32-Lead LFCSP_VQ	
θ_{JA} Thermal Impedance	108.2°C/W
Reflow Soldering (Pb Free)	
Peak Temperature	260°C (+0/−5)
Time at Peak Temperature	10 sec to 40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

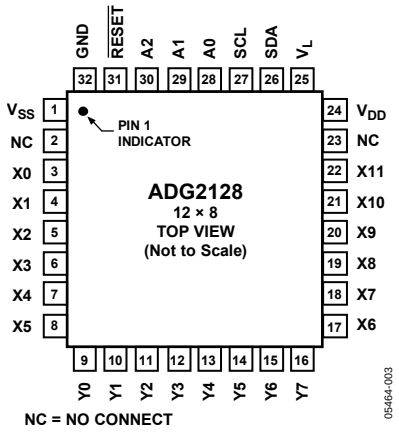

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions[1]

Pin No.	Mnemonic	Description
1	V_{SS}	Negative Power Supply in a Dual-Supply Application. For single-supply applications, this pin should be tied to GND.
2, 23	NC	No Connect.
3 to 8, 17 to 22	X0 to X11	Can be inputs or outputs.
9 to 16	Y0 to Y7	Can be inputs or outputs.
24	V_{DD}	Positive Power Supply Input.
25	V_L	Logic Power Supply Input.
26	SDA	Digital I/O. Bidirectional open drain data line. External pull-up resistor required.
27	SCL	Digital Input, Serial Clock Line. Open drain input that is used in conjunction with SDA to clock data into the device. External pull-up resistor required.
28	A0	Logic Input. Address pin that sets the least significant bit of the 7-bit slave address.
29	A1	Logic Input. Address pin that sets the second least significant bit of the 7-bit slave address.
30	A2	Logic Input. Address pin that sets the third least significant bit of the 7-bit slave address.
31	$\overline{\text{RESET}}$	Active Low Logic Input. When this pin is low, all switches are open, and appropriate registers are cleared to 0.
32	GND	Ground Reference Point for All Circuitry on the ADG2128.

[1] It is recommended that the exposed paddle be soldered to V_{SS} to improve heat dissipation and crosstalk.

TYPICAL PERFORMANCE CHARACTERISTICS

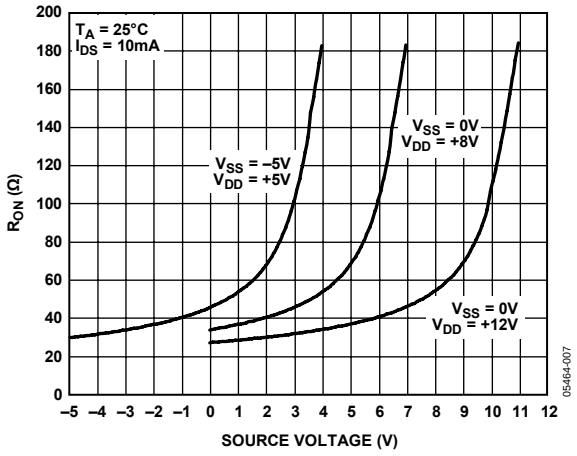

Figure 4. Signal Range

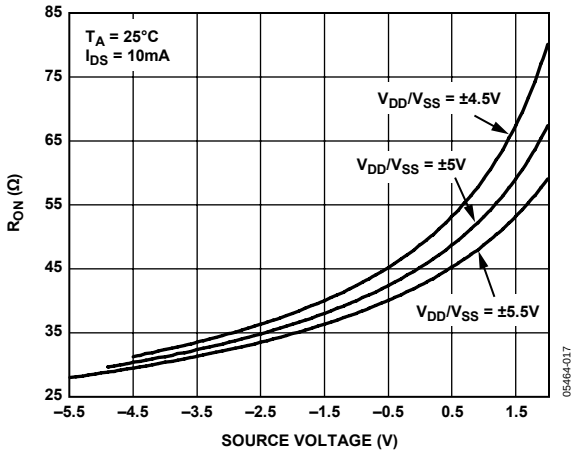

Figure 5. R_{ON} vs. Source Voltage, Dual ±5 V Supplies

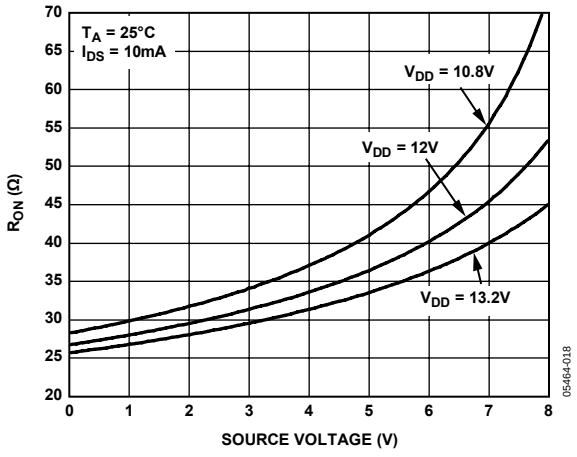

Figure 6. R_{ON} vs. Supplies, V_{DD} = 12 V ± 10%

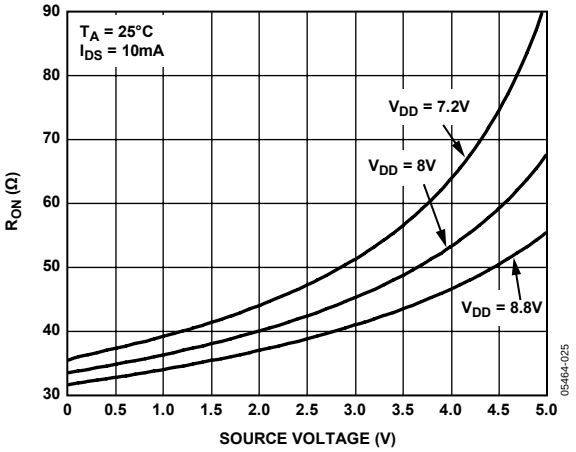

Figure 7. R_{ON} vs. Source Voltage, V_{DD} = 8 V ± 10%

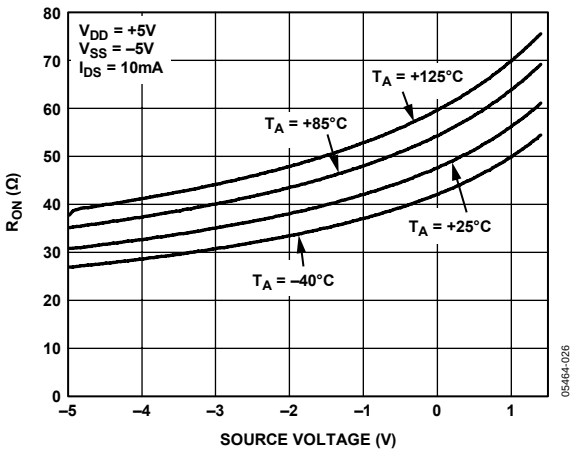

Figure 8. R_{ON} vs. Temperature, Dual ±5 V Supplies

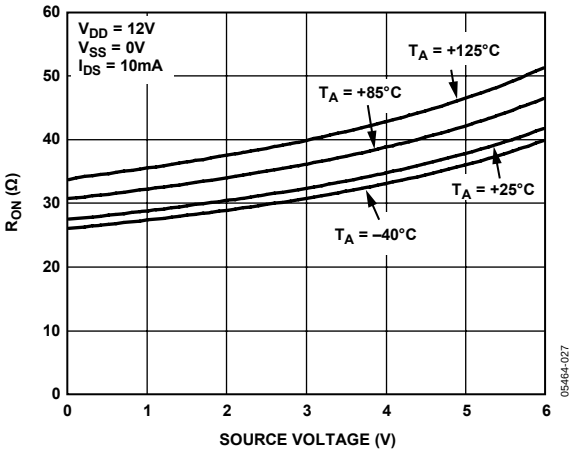

Figure 9. R_{ON} vs. Temperature, V_{DD} = 12 V

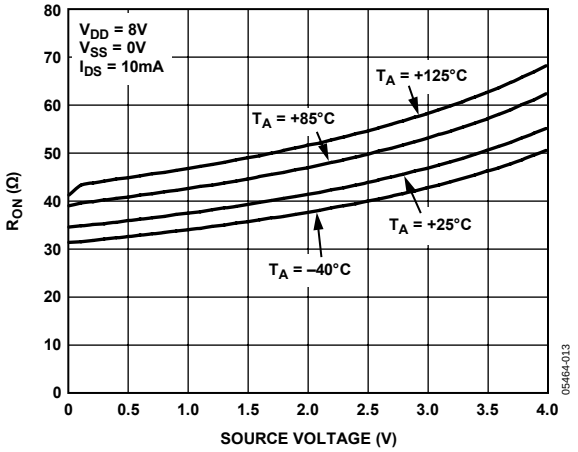

Figure 10. R_{ON} vs. Temperature, V_{DD} = 8 V

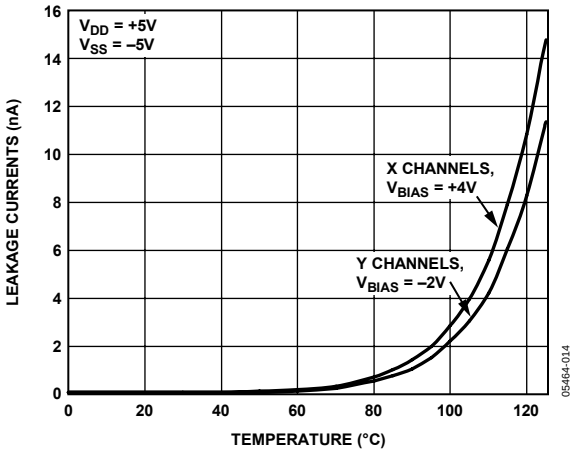

Figure 11. On Leakage vs. Temperature, Dual ±5 V Supplies

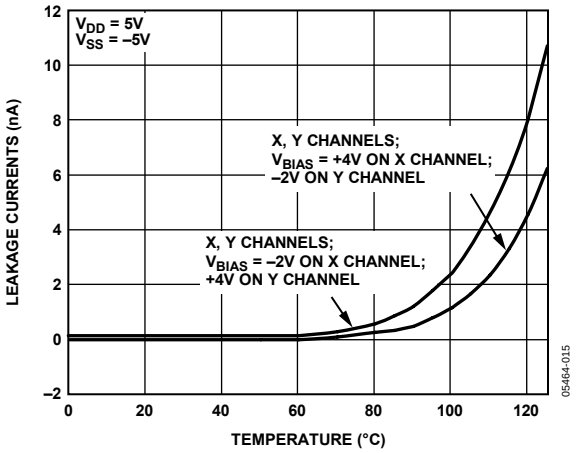

Figure 12. Off Leakage vs. Temperature, Dual ±5 V Supplies

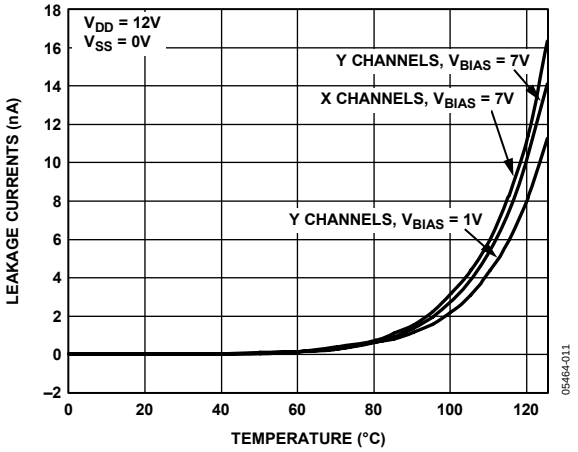

Figure 13. On Leakage vs. Temperature, 12 V Single Supply

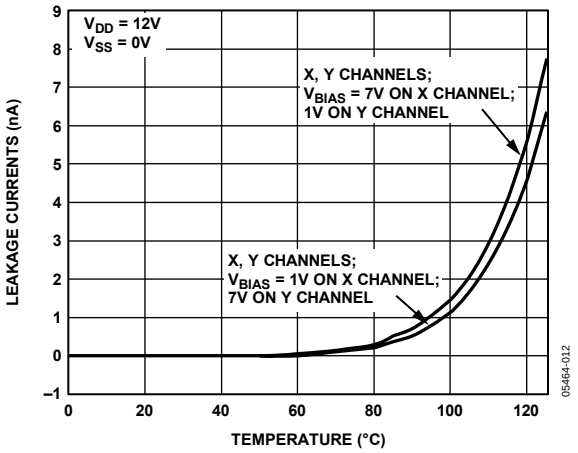

Figure 14. Off Leakage vs. Temperature, 12 V Single Supply

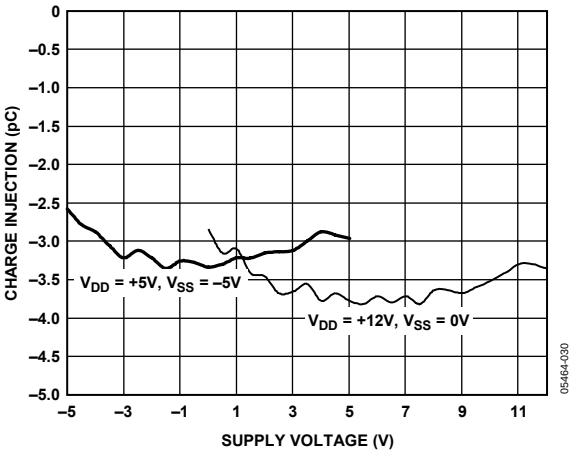

Figure 15. Charge Injection vs. Supply Voltage

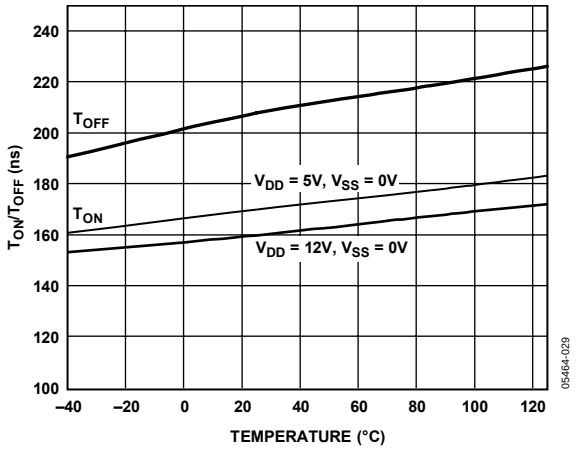

Figure 16. T_{ON}/T_{OFF} Times vs. Temperature

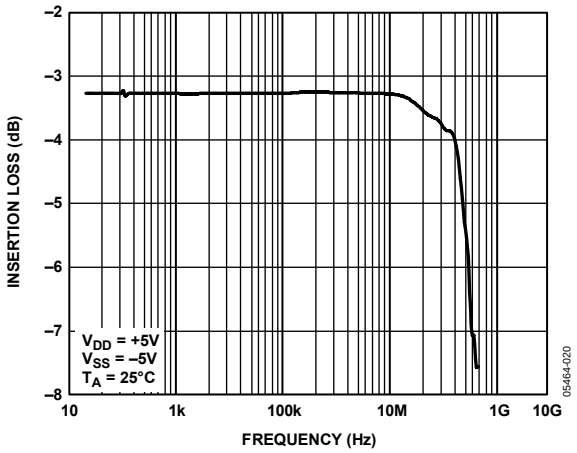

Figure 17. Individual Inputs to Individual Outputs Bandwidth, Dual ±5 V Supply

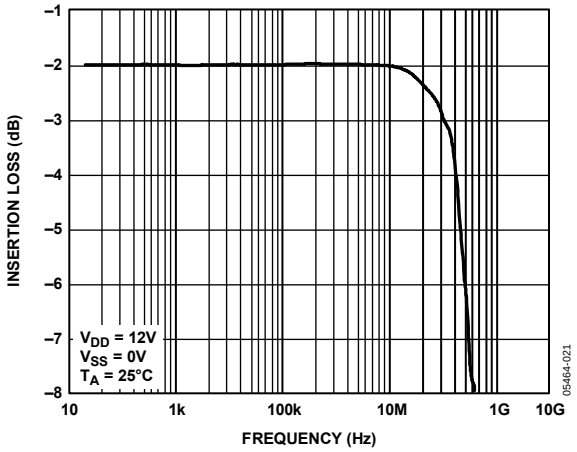

Figure 18. Individual Inputs to Individual Outputs Bandwidth, 12 V Single Supply

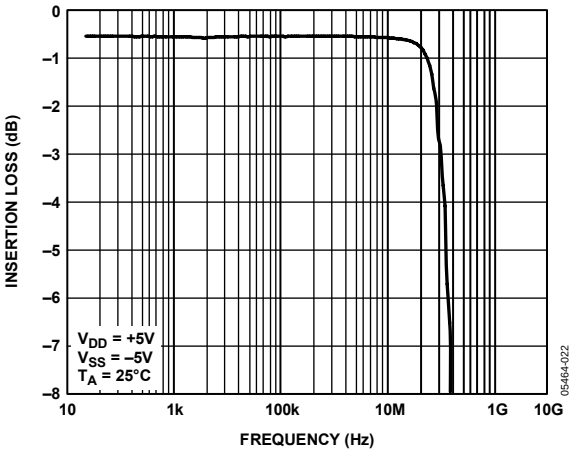

Figure 19. One Input to Eight Outputs Bandwidth, 5 V Dual Supply

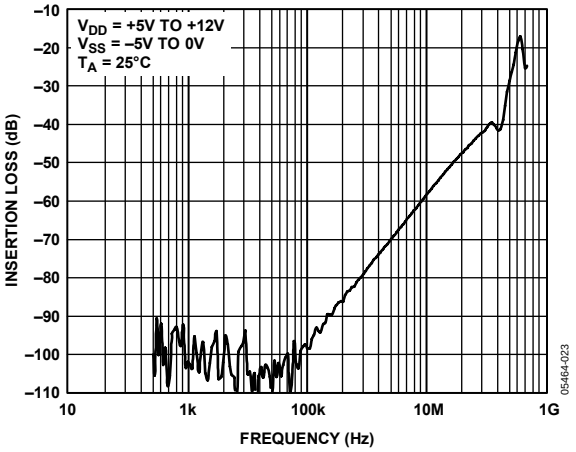

Figure 20. Off Isolation vs. Frequency

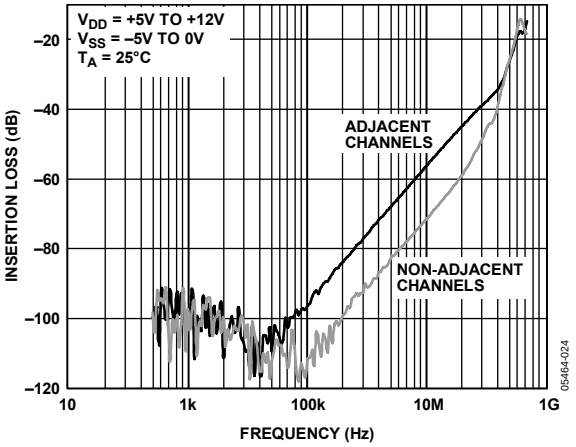

Figure 21. Crosstalk vs. Frequency

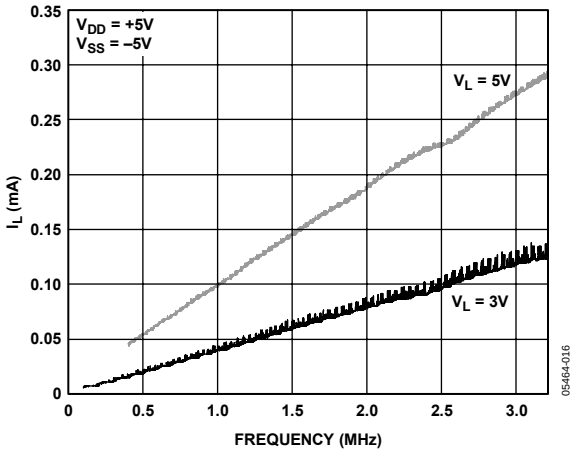

Figure 22. Digital Current (I_L) vs. Frequency

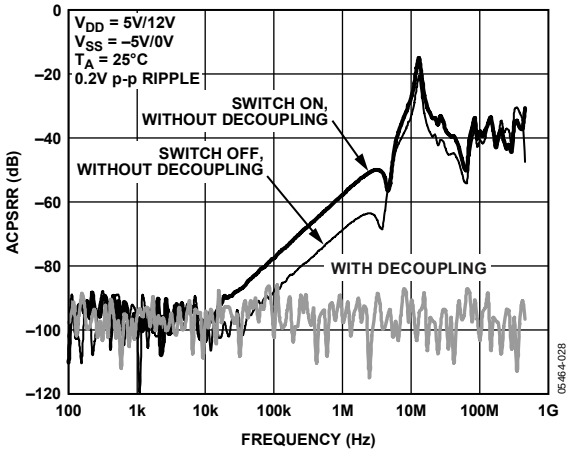

Figure 24. ACPSRR

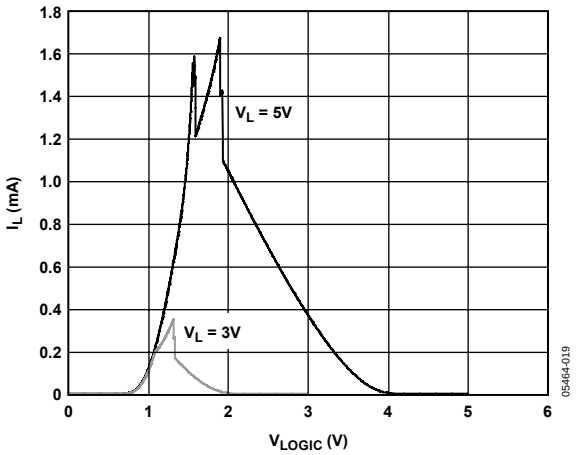

Figure 23. Digital Current (I_L) vs. V_{LOGIC} for Varying Digital Supply Voltage

TEST CIRCUITS

The test circuits show measurements on one channel for clarity, but the circuit applies to any of the switches in the matrix.

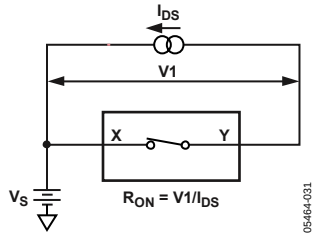

Figure 25. On Resistance

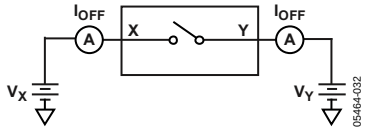

Figure 26. Off Leakage

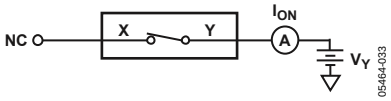

Figure 27. On Leakage

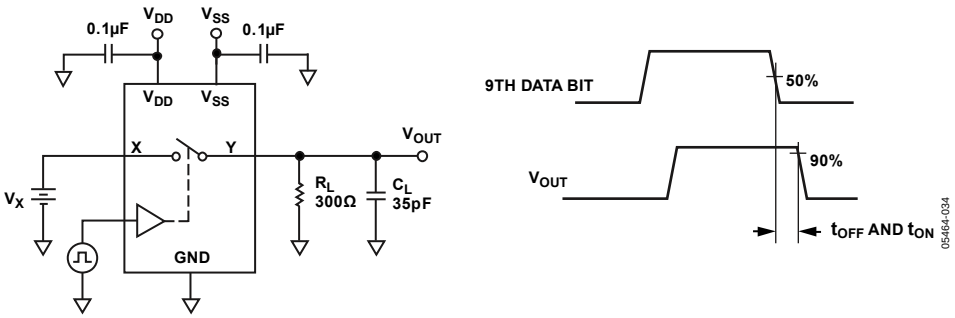

Figure 28. Switching Times, t_{ON}, t_{OFF}

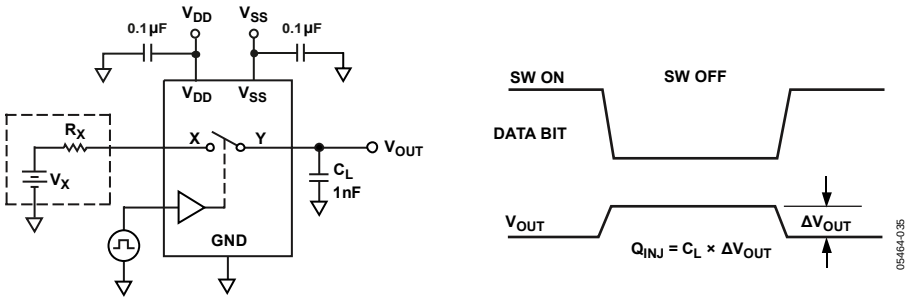

Figure 29. Charge Injection

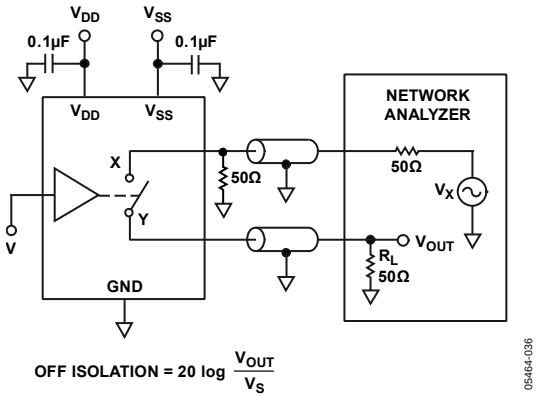

Figure 30. Off Isolation

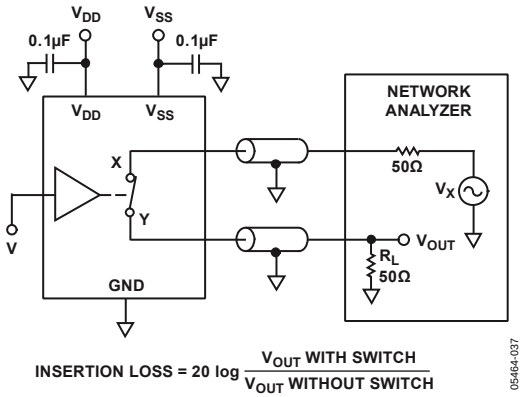

Figure 31. Bandwidth

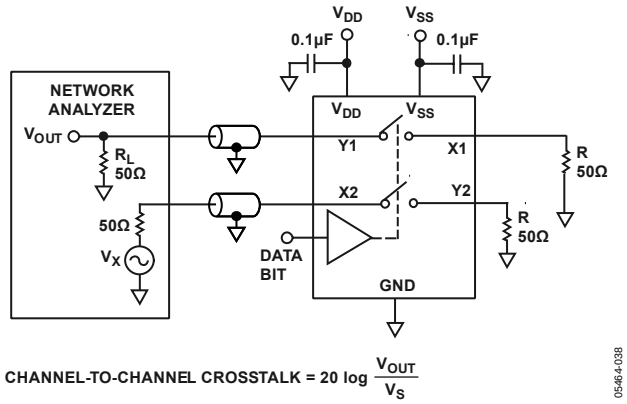

Figure 32. Channel-to-Channel Crosstalk

TERMINOLOGY

On Resistance (R_{ON})
The series on-channel resistance measured between the X input/output and the Y input/output.

On Resistance Match (ΔR_{ON})
The channel-to-channel matching of on resistance when channels are operated under identical conditions.

On Resistance Flatness ($R_{FLAT(ON)}$)
The variation of on resistance over the specified range produced by the specified analog input voltage change with a constant load current.

Channel Off Leakage (I_{OFF})
The sum of leakage currents into or out of an off channel input.

Channel On Leakage (I_{ON})
The current loss/gain through an on-channel resistance, creating a voltage offset across the device.

Input Leakage Current (I_{IN})
The current flowing into a digital input when a specified low level or high level voltage is applied to that input.

Input Off Capacitance (C_{OFF})
The capacitance between an analog input and ground when the switch channel is off.

Input/Output On Capacitance (C_{ON})
The capacitance between the inputs or outputs and ground when the switch channel is on.

Digital Input Capacitance (C_{IN})
The capacitance between a digital input and ground.

Output On Switching Time (t_{ON})
The time required for the switch channel to close. The time is measured from 50% of the logic input change to the time the output reaches 10% of the final value.

Output Off Switching Time (t_{OFF})
The time required for the switch to open. This time is measured from 50% of the logic input change to the time the output reaches 90% of the switch off condition.

Total Harmonic Distortion + Noise (THD + N)
The ratio of the harmonic amplitudes plus noise of a signal to the fundamental.

−3 dB Bandwidth
The frequency at which the output is attenuated by 3 dB.

Off Isolation
The measure of unwanted signal coupling through an off switch.

Crosstalk
The measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Differential Gain
The measure of how much color saturation shift occurs when the luminance level changes. Both attenuation and amplification can occur; therefore, the largest amplitude change between any two levels is specified and is expressed as a percentage of the largest chrominance amplitude.

Differential Phase
The measure of how much hue shift occurs when the luminance level changes. It can be a negative or positive value and is expressed in degrees of subcarrier phase.

Charge Injection
The measure of the glitch impulse transferred from the digital input to the analog output during on/off switching.

Input High Voltage (V_{INH})
The minimum input voltage for Logic 1.

Input Low Voltage (V_{INL})
The maximum input voltage for Logic 0.

Output Low Voltage (V_{OL})
The minimum input voltage for Logic 1.

Input Low Voltage (V_{INL})
The maximum output voltage for Logic 0.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

THEORY OF OPERATION

The ADG2128 is an analog cross point switch with an array size of 8 × 12. The 12 rows are referred to as the X input/output lines, while the eight columns are referred to as the Y input/output lines. The device is fully flexible in that it connects any X line or number of X lines with any Y line when turned on. Similarly, it connects any X line with any number of Y lines when turned on.

Control of the ADG2128 is carried out via an I²C interface. The device can be operated from single supplies of up to 13.2 V or from dual ±5 V supplies. The ADG2128 has many attractive features, such as the ability to reset all the switches, the ability to update many switches at the same time, and the option of reading back the status of any switch. All of these features are described in more detail here in the Theory of Operation section.

$\overline{\text{RESET}}$/POWER-ON RESET

The ADG2128 offers the ability to reset all of the 96 switches to the off state. This is done through the $\overline{\text{RESET}}$ pin. When the $\overline{\text{RESET}}$ pin is low, all switches are open (off), and appropriate registers are cleared. Note that the ADG2128 also has a power-on reset block. This ensures that all switches are in the off condition on power-up of the device. In addition, all internal registers are filled with 0s and remain so until a valid write to the ADG2128 takes place.

LOAD SWITCH (LDSW)

LDSW is an active high command that allows a number of switches to be simultaneously updated. This is useful in applications where it is important to have synchronous transmission of signals. There are two LDSW modes: the transparent mode and the latched mode.

Transparent Mode

In this mode, the switch position changes after the new word is written in. LDSW is set to 1.

Latched Mode

In this mode, the switch positions are not updated at the same time that the input registers are written to. This is achieved by setting LDSW to 0 for each word (apart from the last word) written to the device. Then, setting LDSW to 1 for the last word allows all of the switches in that sequence to be simultaneously updated.

READBACK

Readback of the switch array conditions is also offered when in standard mode and fast mode. Readback enables the user to check the status of the switches of the ADG2128. This is very useful when debugging a system.

SERIAL INTERFACE

The ADG2128 is controlled via an I²C-compatible serial bus. The parts are connected to this bus as a slave device (no clock is generated by the switch).

HIGH SPEED I²C INTERFACE

In addition to standard and full speed I²C, the ADG2188 also supports the high speed (3.4 MHz) I²C interface. Only the -HS models provide this added performance. See the Ordering Guide for details.

SERIAL BUS ADDRESS

The ADG2128 has a 7-bit slave address. The four MSBs are hard coded to 1110, and the three LSBs are determined by the state of Pin A0, Pin A1, and Pin A2. By offering the facility to hardware configure Pin A0, Pin A1, and Pin A2, up to eight of these devices can be connected to a single serial bus.

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, defined as when a high-to-low transition on the SDA line occurs while SCL is high. This indicates that an address/data stream follows. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/$\overline{W}$ bit that determines the direction of the data transfer, that is, whether data is written to or read from the slave device.
2. The peripheral whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse, known as the acknowledge bit. At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is 1 (high), the master reads from the slave device. If the R/$\overline{W}$ bit is 0 (low), the master writes to the slave device.
3. Data is transmitted over the serial bus in sequences of nine clock pulses: eight data bits followed by an acknowledge bit from the receiver of the data. Transitions on the SDA line must occur during the low period of the clock signal, SCL, and remain stable during the high period of SCL, because a low-to-high transition when the clock is high can be interpreted as a stop signal.
4. When all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse and then high during the 10th clock pulse to establish a stop condition.

Refer to Figure 33 and Figure 34 for a graphical explanation of the serial data transfer protocol.

WRITING TO THE ADG2128

INPUT SHIFT REGISTER

The input shift register is 24 bits wide. A 3-byte write is necessary when writing to this register and is done under the control of the serial clock input, SCL. The contents of the three bytes of the input shift register are shown in Figure 33 and described in Table 6.

Figure 33. Data-Words

Table 6. Input Shift Register Bit Function Descriptions

Bit	Mnemonic	Description
DB23 to DB17	1110xxx	The MSBs of the ADG2128 are set to 1110. The LSBs of the address byte are set by the state of the three address pins, Pin A0, Pin A1, and Pin A2.
DB16	R/$\overline{W}$	Controls whether the ADG2128 slave device is read from or written to. If R/$\overline{W}$ = 1, the ADG2128 is being read from. If R/$\overline{W}$ = 0, the ADG2128 is being written to.
DB15	Data	Controls whether the switch is to be open (off) or closed (on). If Data = 0, the switch is open/off. If Data = 1, the switch is closed/on.
DB14 to DB11	AX3 to AX0	Controls I/Os X0 to X11. See Table 7 for the decode truth table.
DB10 to DB8	AY2 to AY0	Controls I/Os Y0 to Y7. See Table 7 for the decode truth table.
DB7 to DB1	X	Don't care.
DB0	LDSW	This bit is useful when a number of switches need to be simultaneously updated. If LDSW = 1, the switch position changes after the new word is read. If LDSW = 0, the input data is latched, but the switch position is not changed.

As shown in Table 6, Bit DB11 to Bit DB14 control the X input/output lines, while Bit DB8 to Bit DB10 control the Y input/output lines. Table 7 shows the truth table for these bits. Note the full coding sequence is written out for Channel Y0, and Channel Y1 to Channel Y7 follow a similar pattern. Note also that the $\overline{\text{RESET}}$ pin must be high when writing to the device.

Table 7. Address Decode Truth Table

DB15 DATA	DB14 AX3	DB13 AX2	DB12 AX1	DB11 AX0	DB10 AY2	DB9 AY1	DB8 AY0	Switch Configuration
1	0	0	0	0	0	0	0	X0 to Y0 (on)
0	0	0	0	0	0	0	0	X0 to Y0 (off)
1	0	0	0	1	0	0	0	X1 to Y0 (on)
0	0	0	0	1	0	0	0	X1 to Y0 (off)
1	0	0	1	0	0	0	0	X2 to Y0 (on)
0	0	0	1	0	0	0	0	X2 to Y0 (off)
1	0	0	1	1	0	0	0	X3 to Y0 (on)
0	0	0	1	1	0	0	0	X3 to Y0 (off)
1	0	1	0	0	0	0	0	X4 to Y0 (on)
0	0	1	0	0	0	0	0	X4 to Y0 (off)
1	0	1	0	1	0	0	0	X5 to Y0 (on)
0	0	1	0	1	0	0	0	X5 to Y0 (off)
X	0	1	1	0	0	0	0	Reserved
X	0	1	1	1	0	0	0	Reserved
1	1	0	0	0	0	0	0	X6 to Y0 (on)
0	1	0	0	0	0	0	0	X6 to Y0 (off)
1	1	0	0	1	0	0	0	X7 to Y0 (on)
0	1	0	0	1	0	0	0	X7 to Y0 (off)
1	1	0	1	0	0	0	0	X8 to Y0 (on)
0	1	0	1	0	0	0	0	X8 to Y0 (off)

DB15 DATA	DB14 AX3	DB13 AX2	DB12 AX1	DB11 AX0	DB10 AY2	DB9 AY1	DB8 AY0	Switch Configuration
1	1	0	1	1	0	0	0	X9 to Y0 (on)
0	1	0	1	1	0	0	0	X9 to Y0 (off)
1	1	1	0	0	0	0	0	X10 to Y0 (on)
0	1	1	0	0	0	0	0	X10 to Y0 (off)
1	1	1	0	1	0	0	0	X11 to Y0 (on)
0	1	1	0	1	0	0	0	X11 to Y0 (off)
X	1	1	1	0	0	0	0	Reserved
X	1	1	1	1	0	0	0	Reserved
1	0	0	0	0	0	0	1	X0 to Y1 (on)
0	0	0	0	0	0	0	1	X0 to Y1 (off)
..	..	..		..	..	..	..	
1	1	1	0	1	0	0	1	X11 to Y1 (on)
1	0	0	0	0	0	1	0	X0 to Y2 (on)
0	0	0	0	0	0	1	0	X0 to Y2 (off)
..	..	..	..	..	..	..	..	
1	1	1	0	1	0	1	0	X11 to Y2 (on)
1	0	0	0	0	0	1	1	X0 to Y3 (on)
0	0	0	0	0	0	1	1	X0 to Y3 (off)
..	..	..	..	..	..	..	..	
1	1	1	0	1	0	1	1	X11 to Y3 (on)
1	0	0	0	0	1	0	0	X0 to Y4 (on)
0	0	0	0	0	1	0	0	X0 to Y4 (off)
..	..	..	..	..	..	..	..	
1	1	1	0	1	1	0	0	X11 to Y4 (on)
1	0	0	0	0	1	0	1	X0 to Y5 (on)
0	0	0	0	0	1	0	1	X0 to Y5 (off)
..	..	..	..	..	..	..	..	
1	1	1	0	1	1	0	1	X11 to Y5 (on)
1	0	0	0	0	1	1	0	X0 to Y6 (on)
0	0	0	0	0	1	1	0	X0 to Y6 (off)
..	..	..	..	..	..	..	..	
1	1	1	0	1	1	1	0	X11 to Y6 (on)
1	0	0	0	0	1	1	1	X0 to Y7 (on)
0	0	0	0	0	1	1	1	X0 to Y7 (off)
..	..	..	..	..	..	..	..	
1	1	1	0	1	1	1	1	X11 to Y7 (on)

WRITE OPERATION

When writing to the ADG2128, the user must begin with an address byte and R/$\overline{W}$ bit, after which the switch acknowledges that it is prepared to receive data by pulling SDA low. This address byte is followed by the two 8-bit words. The write operations for the switch array are shown in Figure 34. Note that it is only the condition of the switch corresponding to the bits in the data bytes that changes state. All other switches retain their previous condition.

READ OPERATION

Readback on the ADG2128 has been designed to work as a tool for debug and can be used to output the status of any of the 96 switches of the device. The readback function is a 2-step sequence that works as follows:

1. Select the relevant X line that you wish to read back from. Note that there are eight switches connecting that X line to the eight Y lines. The next step involves writing to the ADG2128 to tell the part that you would like to know the status of those eight switches.
   a. Enter the I²C address of the ADG2128, and set the R/$\overline{W}$ bit to 0 to indicate that you are writing to the device.
   b. Enter the readback address for the X line of interest, the addresses of which are shown in Table 8. Note that the ADG2128 is expecting a 2-byte write; therefore, be sure to enter another byte of don't cares. (see Figure 35).
   c. The ADG2128 then places the status of those eight switches in a register that can be read back.
2. The second step involves reading back from the register that holds the status of the eight switches associated with your X line of choice.
   a. As before, enter the I²C address of the ADG2128. This time, set the R/$\overline{W}$ bit to 1 to indicate that you would like to read back from the device.
   b. As with a write to the device, the ADG2128 outputs a 2-byte sequence during readback. Therefore, the first eight bits of data out that are read back are all 0s. The next eight bits of data that come back are the status of the eight Y lines attached to that particular X line. If the bit is a 1, then the switch is closed (on); similarly, if it is a 0, the switch is open (off).

The entire read sequence is shown in Figure 35.

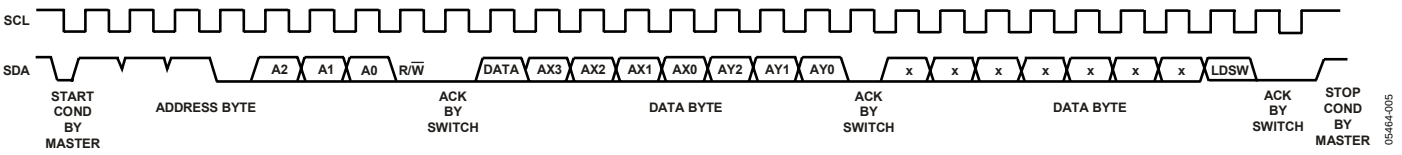

Figure 34. Write Operation

Table 8. Readback Addresses for Each X Line

X Line	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
X0	0	0	1	1	0	1	0	0
X1	0	0	1	1	1	1	0	0
X2	0	1	1	1	0	1	0	0
X3	0	1	1	1	1	1	0	0
X4	0	0	1	1	0	1	0	1
X5	0	0	1	1	1	1	0	1
X6	0	1	1	1	0	1	0	1
X7	0	1	1	1	1	1	0	1
X8	0	0	1	1	0	1	1	0
X9	0	0	1	1	1	1	1	0
X10	0	1	1	1	0	1	1	0
X11	0	1	1	1	1	1	1	0

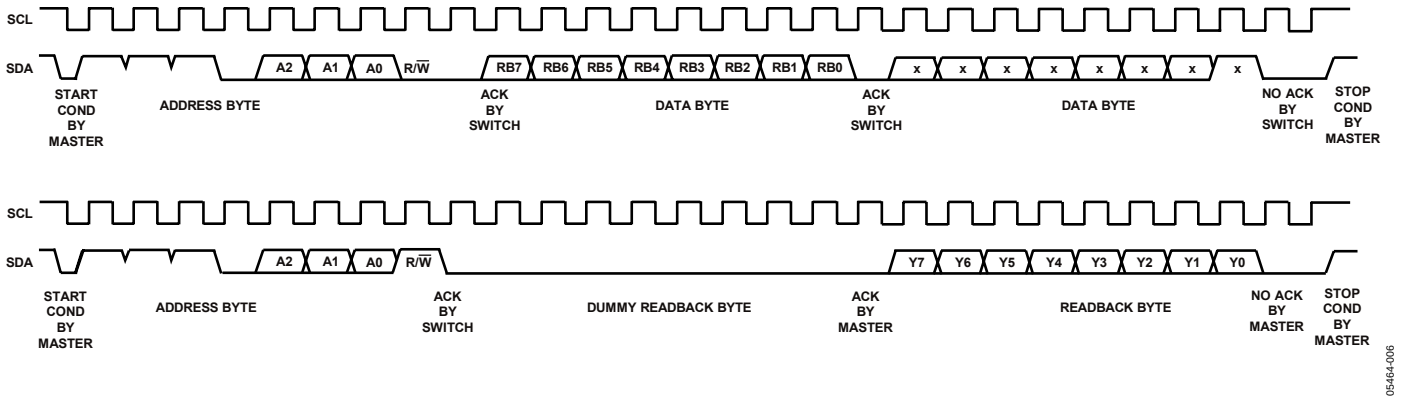

Figure 35. Read Operation

EVALUATION BOARD

The ADG2128 evaluation board allows designers to evaluate the high performance ADG2128 8 × 12 switch array with minimum effort.

The evaluation kit includes a populated, tested ADG2128 printed circuit board. The evaluation board interfaces to the USB port of a PC, or it can be used as a standalone evaluation board. Software is available with the evaluation board that allows the user to easily program the ADG2128 through the USB port. Schematics of the evaluation board are shown in Figure 36 and Figure 37. The software runs on any PC that has Microsoft® Windows® 2000 or Windows XP installed.

USING THE ADG2128 EVALUATION BOARD

The ADG2128 evaluation kit is a test system designed to simplify the evaluation of the ADG2128. Each input/output of the part comes with a socket specifically chosen for easy audio/video evaluation. An application note is also available with the evaluation board and gives full information on operating the evaluation board.

POWER SUPPLY

The ADG2128 evaluation board can be operated with both single and dual supplies. V_{DD} and V_{SS} are supplied externally by the user. The V_L supply can be applied externally, or the USB port can be used to power the digital circuitry.

SCHEMATICS

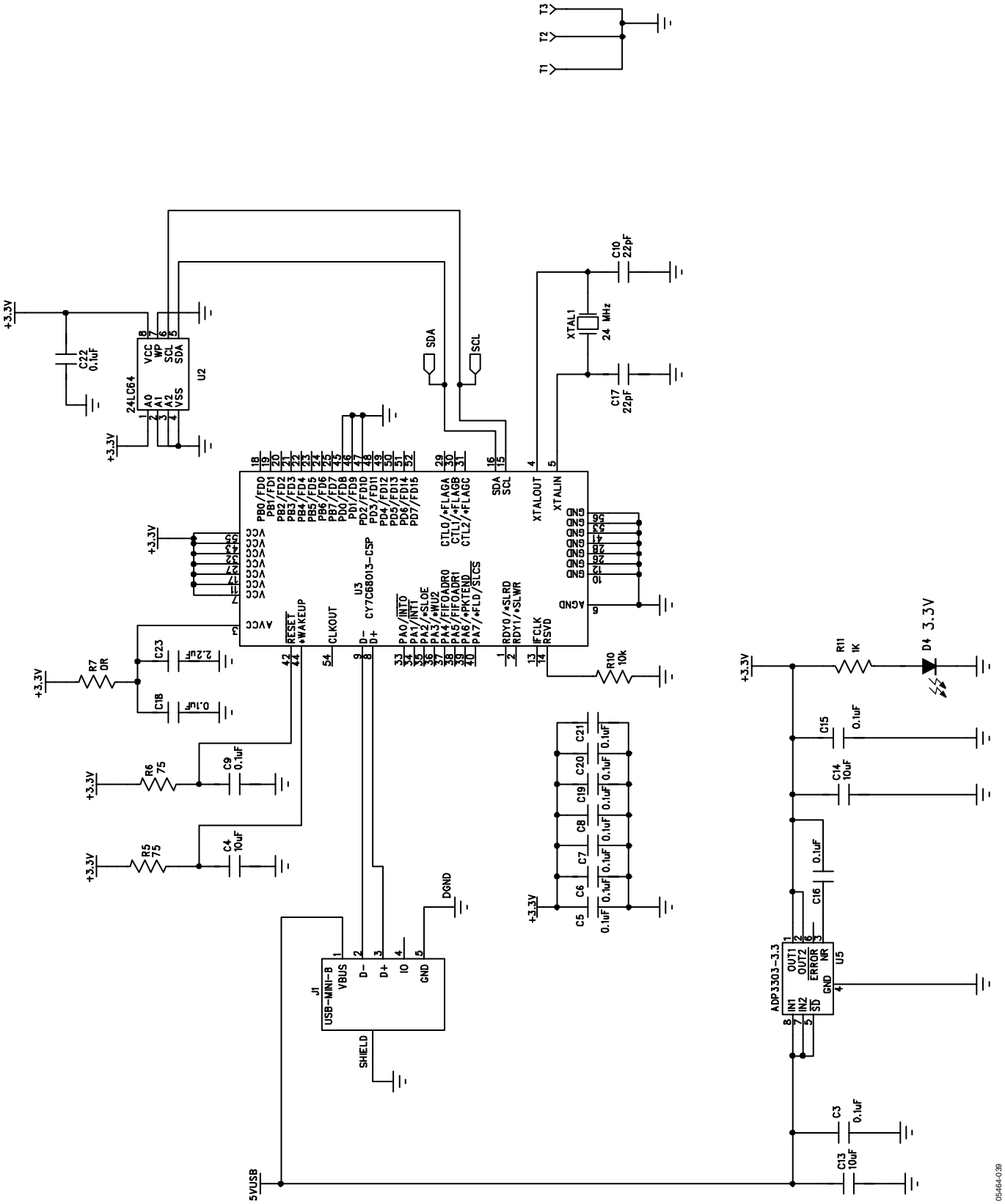

Figure 36. EVAL-ADG2128EB Schematic, USB Controller Section

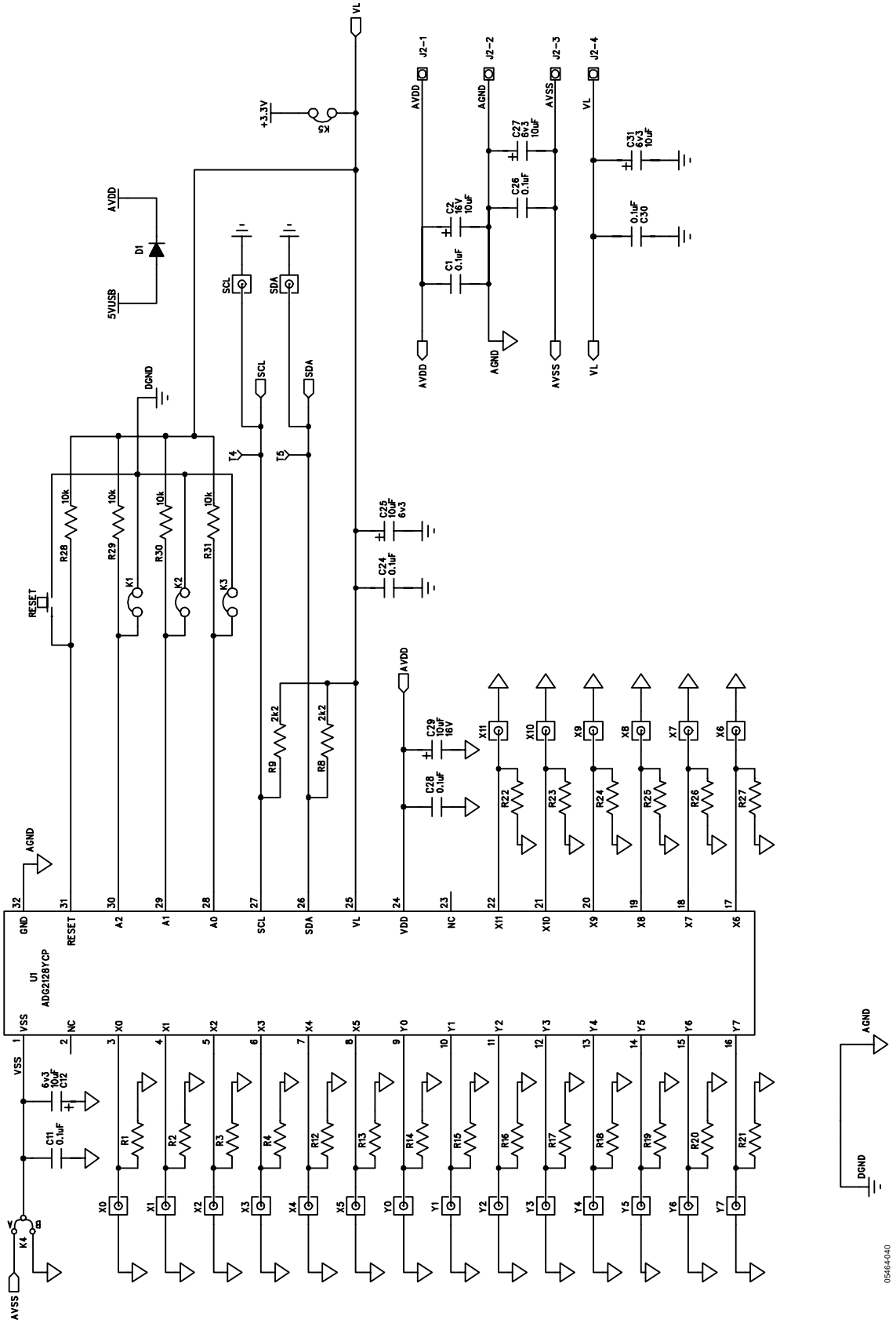

Figure 37. EVAL-ADG2128EB Schematic, Chip Section

OUTLINE DIMENSIONS

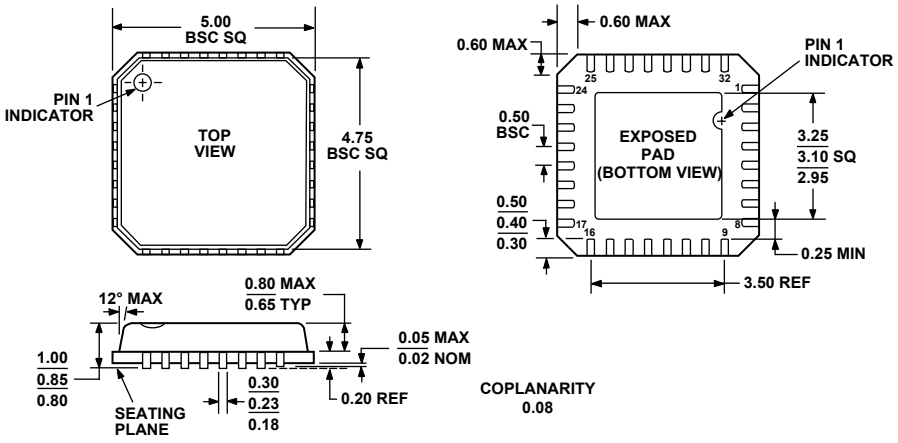

Figure 38. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm x 5 mm Body, Very Thin Quad
(CP-32-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	I^2C Speed	Package Description	Package Option
ADG2128BCPZ-REEL[1]	−40°C to +85°C	100 kHz, 400 kHz	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-3
ADG2128BCPZ-REEL7[1]	−40°C to +85°C	100 kHz, 400 kHz	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-3
ADG2128BCPZ-HS-RL7[1]	−40°C to +85°C	100 kHz, 400 kHz, 3.4 MHz	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-3
ADG2128YCPZ-REEL[1]	−40°C to +125°C	100 kHz, 400 kHz	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-3
ADG2128YCPZ-REEL7[1]	−40°C to +125°C	100 kHz, 400 kHz	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-3
ADG2128YCPZ-HS-RL7[1]	−40°C to +125°C	100 kHz, 400 kHz, 3.4 MHz	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-3
EVAL-ADG2128EB			Evaluation Board	

[1] Z = Pb-free part.

NOTES

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

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