

Low Capacitance, Low Charge Injection, $\pm 15 \text{ V/} \pm 12 \text{ V} i \text{CMOS}^{\text{TM}}$ Quad SPST Switches

ADG1211/ADG1212/ADG1213

FEATURES

1 pF off capacitance 2.6 pF on capacitance <1 pC charge injection 33 V supply range 120 Ω on resistance Fully specified at ±15 V, +12 V No V_L supply required 3 V logic-compatible inputs Rail-to-rail operation 16-lead TSSOP and 16-lead LFCSP Typical power consumption: <0.03 μW

APPLICATIONS

Automatic test equipment Data acquisition systems Battery-powered systems Sample-and-hold systems Audio signal routing Video signal routing Communication systems

GENERAL DESCRIPTION

The ADG1211/ADG1212/ADG1213 are monolithic complementary metal-oxide semiconductor (CMOS) devices containing four independently selectable switches designed on an *i*CMOS (industrial CMOS) process. *i*CMOS is a modular manufacturing process combining high voltage CMOS and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-andhold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth make the parts suitable for video signal switching.

FUNCTIONAL BLOCK DIAGRAM

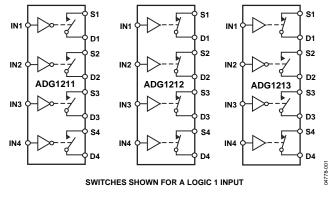


Figure 1.

*i*CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

The ADG1211/ADG1212/ADG1213 contain four independent single-pole/single-throw (SPST) switches. The ADG1211 and ADG1212 differ only in that the digital control logic is inverted. The ADG1211 switches are turned on with Logic 0 on the appropriate control input, while Logic 1 is required for the ADG1212. The ADG1213 has two switches with digital control logic similar to that of the ADG1211; the logic is inverted on the other two switches. The ADG1213 exhibits break-beforemake switching action for use in multiplexer applications.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

PRODUCT HIGHLIGHTS

- 1. Ultralow capacitance.
- 2. <1 pC charge injection.
- 3. 3 V logic-compatible digital inputs: $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V.
- 4. No V_L logic power supply required.
- 5. Ultralow power dissipation: $<0.03 \mu$ W.
- 6. 16-lead TSSOP and 3 mm \times 3 mm LFCSP packages.

Rev. 0

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REVISION HISTORY

7/05—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

 V_{DD} = 15 V \pm 10%, V_{SS} = –15 V \pm 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	Y Version ¹ -40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V _{DD} to V _{SS}	V	
On Resistance (R _{ON})	120			Ωtyp	$V_{s} = \pm 10 V$, $I_{s} = -1 mA$; Figure 20
	190	230	260	Ωmax	$V_{DD} = +13.5 \text{ V}, V_{SS} = -13.5 \text{ V}$
On Resistance Match Between Channels (ΔR_{ON})	2.5			Ωtyp	$V_{s} = \pm 10 V$, $I_{s} = -1 mA$
	6	10	11	Ωmax	
On Resistance Flatness (R _{FLAT(ON)})	20			Ωtyp	$V_s = -5 V/0 V/+5 V$; $I_s = -1 mA$
	57	72	79	Ωmax	
LEAKAGE CURRENTS					$V_{DD} = +16.5 \text{ V}, V_{SS} = -16.5 \text{ V}$
Source Off Leakage, Is (Off)	±0.02			nA typ	$V_s = \pm 10 V$, $V_D = \mp 10 V$; Figure 21
	±0.1	±0.6	±1	nA max	_
Drain Off Leakage, I_D (Off)	±0.02			nA typ	$V_s = \pm 10 \text{ V}, V_D = \mp 10 \text{ V};$ Figure 21
	±0.1	±0.6	±1	nA max	
Channel On Leakage, I _D , I _S (On)	±0.02			nA typ	$V_{s} = V_{D} = \pm 10 V$; Figure 22
	±0.1	±0.6	±1	nA max	
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.0	V min	
Input Low Voltage, V _{INL}			0.8	V max	
Input Current, IINL or IINH	0.005			μA typ	$V_{IN} = V_{INL} \text{ or } V_{INH}$
			±0.1	μA max	
Digital Input Capacitance, C _{IN}	2.5			pF typ	
DYNAMIC CHARACTERISTICS ²					
ton	105			ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$
	125	160	185	ns max	V _s = 10 V; Figure 23
toff	40			ns typ	$R_L = 300 \ \Omega, C_L = 35 \ pF$
	50	60	60	ns max	V _s = 10 V; Figure 23
Break-Before-Make Time Delay, t _D	25			ns typ	$R_L = 300 \ \Omega, C_L = 35 \ pF$
(ADG1213 Only)			10	ns min	$V_{s1} = V_{s2} = 10 V$; Figure 24
Charge Injection	-0.3			pC typ	$V_s = 0 V$, $R_s = 0 \Omega$, $C_L = 1 nF$; Figure 25
Off Isolation	80			dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; Figure 26
Channel-to-Channel Crosstalk	90			dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; Figure 27
Total Harmonic Distortion + Noise	0.15			% typ	$R_L = 10 \text{ k}\Omega$, 5 V rms, f = 20 Hz to 20 kHz
–3 dB Bandwidth	1000			MHz typ	$R_L = 50 \Omega$, $C_L = 5 pF$; Figure 28
C _s (Off)	0.9			pF typ	$V_s = 0 V, f = 1 MHz$
	1.1			pF max	$V_s = 0 V, f = 1 MHz$
C _D (Off)	1			pF typ	$V_s = 0 V$, $f = 1 MHz$
	1.2			pF max	$V_s = 0 V, f = 1 MHz$
C _D , C _s (On)	2.6			pF typ	$V_s = 0 V, f = 1 MHz$
	3			pF max	$V_{s} = 0 V, f = 1 MHz$

		Y Version ¹			
Parameter	25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					$V_{DD} = +16.5 \text{ V}, \text{ V}_{SS} = -16.5 \text{ V}$
I _{DD}	0.001			μA typ	Digital inputs = $0 V \text{ or } V_{DD}$
			1.0	μA max	
I _{DD}	220			μA typ	Digital inputs = 5 V
			320	μA max	
Iss	0.001			μA typ	Digital inputs = $0 V \text{ or } V_{DD}$
			1.0	μA max	
I _{ss}	0.001			μA typ	Digital inputs = 5 V
			1.0	μA max	

 1 Temperature range for Y version is $-40^\circ C$ to $+125^\circ C.$ 2 Guaranteed by design, not subject to production test.

SINGLE SUPPLY

 V_{DD} = 12 V \pm 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter 25°C +85°C +125°C Unit Test Conditions/Comm ANALOG SWITCH 0 V to Voo 0 V to Voo 0 V to Voo 0 V to 00 0 typ V = 0 V to 10 V, Is = -1 n Analog Signal Range 300 Ω typ V = 0 V to 10 V, Is = -1 n 0 V to 00 0 typ V = 0 V to 10 V, Is = -1 n On Resistance Match Between Channels (ΔRow) 12 26 27 Ω max Voo = 10.8 V, Vs = 0 V 0 V to 10 V, Is = -1 n Co Resistance Flatness (ReLorow) 60 Ω typ V = 0 V to 10 V, Is = -1 n 0 typ V = 0 V to 10 V, Is = -1 n Source Off Leakage, Is (Off) ± 0.0 $n A$ typ V = 1 V 10 V, Vo = 10 V/1 $n A$ typ V = 1 V 10 V, Vo = 10 V/1 Drain Off Leakage, Is (Off) ± 0.0 $n A$ max $n A$ typ V = 1 V 10 V, Vo = 10 V/1 Input Urrent, Ise, or Isen ± 0.1 ± 0.6 ± 1 $n A$ max Input Urrent, Ise, or Isen ± 0.1 ± 0.6 ± 1 $n A$ max Input Urrent, Ise, or Isen 0.001 μA max μA max Digital Input Current,			Y Version ¹			
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		25%	-40°C to	-40°C to	11	
Analog Signal Range $0 \vee to V_{bo}$ V On Resistance (Row) 300 Ω typ $V_5 = 0 \vee to 10 \vee, I_5 = -1 n$ On Resistance Match Between Channels (ARow) 4.5 Ω typ $V_5 = 0 \vee to 10 \vee, I_5 = -1 n$ On Resistance Flatness (Returtow) 12 26 27 Ω max On Resistance Flatness (Returtow) 60 Ω typ $V_5 = 3 V/6 V/9 \vee, I_5 = -1 n$ LEAKAGE CURRENTS $V_{00} = 13.2 \vee, V_{S5} = 0 \vee$ $V_{00} = 13.2 \vee, V_{S5} = 0 \vee$ Source Off Leakage, Is (Off) ± 0.02 nA typ $V_5 = 1 V/10 \vee, V_0 = 10 V/1$ Drain Off Leakage, Is (Off) ± 0.02 nA typ $V_5 = 1 V/10 \vee, V_0 = 10 V/1$ ± 0.1 ± 0.6 ± 1 nA max $V_5 = 1 V/10 \vee, V_0 = 10 V/1$ Channel On Leakage, Is, Is (On) ± 0.1 ± 0.6 ± 1 nA max Input Current, Issi, or Issi 0.001 μA typ $V_{98} = V_{98}$. $V_{98} = V_{98}$ DyNAMIC CHARACTERISTICS ² 0.001 μA max pF typ $V_{98} = 8 V; Figure 23$ torf 155 190 225		25°C	+85°C	+125°C	Unit	Test Conditions/Comments
$\begin{array}{c c c c c c c c c c c c c c c c c c c $				$0 \times t_{2} \times t_{2}$	V	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		200		U V to V _{DD}		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $				60 F		$V_s = 0 V \text{ to } 10 V$, $I_s = -1 \text{ mA}$; Figure 20
Channels (ΔRow) 12 26 27 Ω max On Resistance Flatness (RELATION) 60 Ω typ $V_5 = 3 V/6 V/9 V, I_5 = -1 n$ LEAKAGE CURRENTS $V_{00} = 13.2 V, V_{50} = 0 V$ NA typ $V_5 = 1 V/10 V, V_5 = 10 V/1$ Source Off Leakage, Is (Off) ± 0.02 nA typ $V_5 = 1 V/10 V, V_5 = 10 V/1$ Drain Off Leakage, Is (Off) ± 0.02 nA typ $V_5 = 1 V/10 V, V_5 = 10 V/1$ Drain Off Leakage, Is (Off) ± 0.02 nA typ $V_5 = 1 V/10 V, V_5 = 10 V/1$ DIGITAL INPUTS ± 0.1 ± 0.6 ± 1 nA max Input High Voltage, V_ML 0.001 μ max μ Digital Input Current, INL or INH 0.001 μ A max pF typ DYNAMIC CHARACTERISTICS ² Δ n ns typ $R_L = 300 \Omega, C_L = 35 pF$ Δ or 120 ns typ $R_L = 300 \Omega, C_L = 35 pF$ ns typ Δ or D D D D N Digital Input Current, INL or INP $E_1 = 0.00 \Omega, C_L = 35 pF$ N N			567	625	-	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Channels (ΔR _{ON})				Ωtyp	$V_s = 0 V \text{ to } 10 V, I_s = -1 \text{ mA}$
$\begin{array}{c c c c c c c c c c c c c c c c c c c $			26	27		
Source Off Leakage, Is (Off) ± 0.02 nA typ Ns = 1 V/10 V, V_D = 10 V/10 Drain Off Leakage, I _D (Off) ± 0.02 nA typ Ns = 1 V/10 V, V_D = 10 V/10 Channel On Leakage, I _D (Off) ± 0.02 nA typ Ns = 1 V/10 V, V_D = 10 V/10 DIGITAL INPUTS ± 0.02 nA max nA typ Vs = V_D = 1 V or 10 V; Figure 10 Input High Voltage, V_NH ± 0.6 ± 1 nA max NA typ Vs = V_D = 1 V or 10 V; Figure 10 DIGITAL INPUTS ± 0.1 ± 0.6 ± 1 nA max VN = V_NL or V_NH Input High Voltage, V_NL 0.001 ω W max μ typ VN = V_NL or V_NH Digital Input Carpacitance, C_IN 3 μ pF typ VN = 8 V; Figure 23 TorF 120 ns typ RL = 300 Ω , CL = 35 pF ns typ RL = 300 Ω , CL = 35 pF MAGE 155 190 225 ns typ RL = 300 Ω , CL = 35 pF MAGE 10 ns max Vs = 8 V; Figure 23 ns typ RL = 300 Ω , CL = 35 pF Break-Before-Make Time Delay, To 50 <td></td> <td>60</td> <td></td> <td></td> <td>Ωtyp</td> <td>$V_s = 3 V/6 V/9 V$, $I_s = -1 mA$</td>		60			Ωtyp	$V_s = 3 V/6 V/9 V$, $I_s = -1 mA$
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	AKAGE CURRENTS					$V_{DD} = 13.2 \text{ V}, V_{SS} = 0 \text{ V}$
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Source Off Leakage, Is (Off)	±0.02			nA typ	$V_{s} = 1 \text{ V}/10 \text{ V}, V_{D} = 10 \text{ V}/1 \text{ V};$ Figure 21
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		±0.1	±0.6	±1	nA max	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Drain Off Leakage, I _D (Off)	±0.02			nA typ	$V_{s} = 1 \text{ V}/10 \text{ V}, V_{D} = 10 \text{ V}/1 \text{ V};$ Figure 21
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		±0.1	±0.6	±1	nA max	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Channel On Leakage, I _D , I _S (On)	±0.02			nA typ	$V_{s} = V_{D} = 1 V \text{ or } 10 V;$ Figure 22
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	_	±0.1	±0.6	±1		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	GITAL INPUTS					
$\begin{array}{c c c c c c c c c c c c c c c c c c c $				2.0	V min	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $						
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	-	0.001		0.0		
Digital Input Capacitance, C_{IN} 3 pF typ DYNAMIC CHARACTERISTICS ² ns typ R _L = 300 Ω , C_L = 35 pF toN 120 ns typ R _L = 300 Ω , C_L = 35 pF toFF 45 ns typ R _L = 300 Ω , C_L = 35 pF 65 75 85 ns max $V_5 = 8 V$; Figure 23 Break-Before-Make Time Delay, to 50 ns typ R _L = 300 Ω , $C_L = 35 pF$ (ADG1213 Only) 50 ns min $V_{51} = V_{52} = 8 V$; Figure 24 Charge Injection 0 pC typ $V_5 = 6 V$, $R_5 = 0 \Omega$, $C_L = 1 r$ Off Isolation 80 dB typ R _L = 50 Ω , $C_L = 5 pF$, f = 1 -3 dB Bandwidth 900 MHz typ R _L = 50 Ω , $C_L = 5 pF$; Figu C _S (Off) 1.2 pF typ $V_5 = 6 V$, f = 1 MHz L4 pF typ $V_5 = 6 V$, f = 1 MHz C _D (Off) 1.3 pF typ $V_5 = 6 V$, f = 1 MHz C _D , C _S (On) 3.2 pF typ $V_5 = 6 V$, f = 1 MHz		0.001		+0.1		
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		3		20.1		
$\begin{array}{cccccccccccccccccccccccccccccccccccc$		<u> </u>			prop	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$		120			nc tun	$P_{1} = 200 O_{1} C_{2} = 25 pE_{2}$
torr45ns typ $R_L = 300 \Omega, C_L = 35 pF$ 657585ns max $V_S = 8 V$; Figure 23Break-Before-Make Time Delay, tp50ns typ $R_L = 300 \Omega, C_L = 35 pF$ (ADG1213 Only)10ns min $V_{S1} = V_{S2} = 8 V$; Figure 24Charge Injection0pC typ $V_S = 6 V, R_S = 0 \Omega, C_L = 1 n$ Off Isolation80dB typ $R_L = 50 \Omega, C_L = 5 pF, f = 1$ Channel-to-Channel Crosstalk90MHz typ $R_L = 50 \Omega, C_L = 5 pF, f = 1$ -3 dB Bandwidth900MHz typ $R_L = 50 \Omega, C_L = 5 pF, f = 1$ $C_S (Off)$ 1.2 $pF typ$ $V_S = 6 V, f = 1 MHz$ $C_D (Off)$ 1.3 $pF typ$ $V_S = 6 V, f = 1 MHz$ $C_D, C_S (On)$ 3.2 $pF typ$ $V_S = 6 V, f = 1 MHz$			100	225		-
Break-Before-Make Time Delay, to (ADG1213 Only)657585ns max ns typ $V_S = 8 V$; Figure 23 ns typ $R_L = 300 \Omega, C_L = 35 pF$ ns minCharge Injection010ns min $V_{S1} = V_{S2} = 8 V$; Figure 24 pC typ $V_S = 6 V, R_S = 0 \Omega, C_L = 1 r$ dB typOff Isolation80dB typ $R_L = 50 \Omega, C_L = 5 pF, f = 1$ 			190	225		_
Break-Before-Make Time Delay, t_D 50ns typ $R_L = 300 \Omega, C_L = 35 pF$ (ADG1213 Only)10ns min $V_{S1} = V_{S2} = 8 V$; Figure 24Charge Injection0pC typ $V_S = 6 V, R_S = 0 \Omega, C_L = 1 n$ Off Isolation80dB typ $R_L = 50 \Omega, C_L = 5 pF, f = 1$ Channel-to-Channel Crosstalk90dB typ $R_L = 50 \Omega, C_L = 5 pF, f = 1$ -3 dB Bandwidth900MHz typ $R_L = 50 \Omega, C_L = 5 pF; FigureCs (Off)1.2pF typV_S = 6 V, f = 1 MHzC_D (Off)1.3pF typV_S = 6 V, f = 1 MHzC_D, C_S (On)3.2pF typV_S = 6 V, f = 1 MHz$			75	05		-
			75	85		
$ \begin{array}{c cccc} Charge Injection & 0 & pC typ & V_S = 6 V, R_S = 0 \Omega, C_L = 1 n \\ Off Isolation & 80 & dB typ & R_L = 50 \Omega, C_L = 5 pF, f = 1 \\ Channel-to-Channel Crosstalk & 90 & dB typ & R_L = 50 \Omega, C_L = 5 pF, f = 1 \\ -3 dB Bandwidth & 900 & MHz typ & R_L = 50 \Omega, C_L = 5 pF, figu \\ C_S (Off) & 1.2 & pF typ & V_S = 6 V, f = 1 MHz \\ I.4 & pF max & V_S = 6 V, f = 1 MHz \\ C_D (Off) & 1.3 & pF typ & V_S = 6 V, f = 1 MHz \\ 1.5 & pF max & V_S = 6 V, f = 1 MHz \\ C_D, C_S (On) & 3.2 & pF typ & V_S = 6 V, f = 1 MHz \\ \end{array} $		50				-
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	•			10		5
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	C					$V_{s} = 6 V, R_{s} = 0 \Omega, C_{L} = 1 nF;$ Figure 25
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $						$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; Figure 26
$ \begin{array}{c} C_{s} \mbox{ (Off)} & 1.2 & pF \ typ & V_{s} = 6 \ V, \ f = 1 \ MHz \\ 1.4 & pF \ max & V_{s} = 6 \ V, \ f = 1 \ MHz \\ C_{D} \ (Off) & 1.3 & pF \ typ & V_{s} = 6 \ V, \ f = 1 \ MHz \\ 1.5 & pF \ max & V_{s} = 6 \ V, \ f = 1 \ MHz \\ C_{D}, \ C_{s} \ (On) & 3.2 & pF \ typ & V_{s} = 6 \ V, \ f = 1 \ MHz \\ \end{array} $						$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; Figure 27
$ \begin{array}{c} 1.4 & pF max \\ C_D (Off) & 1.3 & pF typ \\ L.5 & pF max \\ C_D, C_S (On) & 3.2 & pF typ \\ \end{array} \begin{array}{c} V_S = 6 \ V, \ f = 1 \ MHz \\ V_S = 6 \ V, \ f = 1 \ MHz \ Mz \\ V_S = 6 \ V, \ f = 1 \ MHz \ Mz \ Mz \ Mz \ Mz \ Mz \ Mz \ M$	-3 dB Bandwidth	900			MHz typ	$R_L = 50 \Omega$, $C_L = 5 pF$; Figure 28
$ \begin{array}{c} C_{D} \ (Off) \\ L.5 \\ C_{D}, C_{S} \ (On) \end{array} \begin{array}{c} 1.3 \\ 1.5 \\ 3.2 \end{array} \begin{array}{c} pF \ typ \\ pF \ max \\ pF \ typ \end{array} \begin{array}{c} V_{S} = 6 \ V, \ f = 1 \ MHz \\ V_{S} = 6 \ V, \ f = 1 \ MHz \end{array} $	Ls (Off)	1.2			pF typ	$V_{s} = 6 V, f = 1 MHz$
1.5 $pF max$ $V_s = 6 V, f = 1 MHz$ $C_D, C_S (On)$ 3.2 $pF typ$ $V_s = 6 V, f = 1 MHz$		1.4			pF max	$V_{s} = 6 V, f = 1 MHz$
$C_D, C_S (On)$ 3.2 pF typ $V_S = 6 V, f = 1 MHz$	L _D (Off)	1.3			pF typ	$V_{s} = 6 V, f = 1 MHz$
		1.5			pF max	$V_{s} = 6 V, f = 1 MHz$
	C _D , C _s (On)	3.2			pF typ	$V_{s} = 6 V, f = 1 MHz$
$ 3.9 $ $ pF max V_s = 6 V, f = 1 MHz$		3.9			pF max	$V_{s} = 6 V, f = 1 MHz$
POWER REQUIREMENTS V _{DD} = 13.2 V	WER REQUIREMENTS					
		0.001			μA tvp	Digital inputs = $0 \text{ V or } V_{DD}$
1.0 µA max				1.0		
I_{DD} 220 $\mu A typ$ Digital inputs = 5 V	חח	220			-	Digital inputs = 5 V
$320 \qquad \mu A max$				320		

 1 Temperature range for Y version is –40°C to +125°C. 2 Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

 $T_A = 25^{\circ}C$, unless otherwise noted.

Table 3.	
Parameter	Rating
V _{DD} to V _{SS}	35 V
V _{DD} to GND	–0.3 V to +25 V
V _{ss} to GND	+0.3 V to -25 V
Analog Inputs ¹	V _{ss} – 0.3 V to V _{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs ¹	GND – 0.3 V to V _{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current per Channel, S or D	25 mA
Operating Temperature Range	
Automotive (Y Version)	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, θJA Thermal Impedance (4-Layer Board)	112°C/W
16-Lead LFCSP, θ _{JA} Thermal Impedance	72.7°C/W
Reflow Soldering Peak Temperature, Pb free	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

Table 4. ADG1211/ADG1212 Truth Table

ADG1211 INx	ADG1212 INx	Switch Condition	
0	1	On	
1	0	Off	

Table 5. ADG1213 Truth Table

ADG1213 INx	Switch 1, 4	Switch 2, 3
0	Off	On
1	On	Off

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

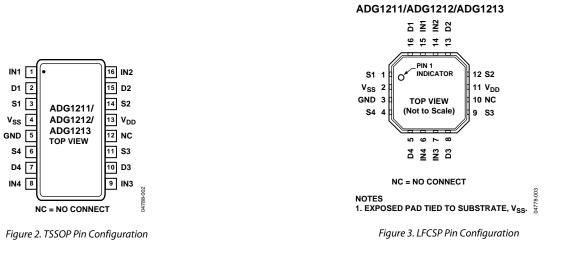


Table 6. Pin Function Descriptions

Pin No.			
TSSOP	LFCSP	Mnemonic	Description
1	15	IN1	Logic Control Input.
2	16	D1	Drain Terminal. Can be an input or output.
3	1	S1	Source Terminal. Can be an input or output.
4	2	Vss	Most Negative Power Supply Potential.
5	3	GND	Ground (0 V) Reference.
6	4	S4	Source Terminal. Can be an input or output.
7	5	D4	Drain Terminal. Can be an input or output.
8	6	IN4	Logic Control Input.
9	7	IN3	Logic Control Input.
10	8	D3	Drain Terminal. Can be an input or output.
11	9	S3	Source Terminal. Can be an input or output.
12	10	NC	No Connection.
13	11	V _{DD}	Most Positive Power Supply Potential.
14	12	S2	Source Terminal. Can be an input or output.
15	13	D2	Drain Terminal. Can be an input or output.
16	14	IN2	Logic Control Input.

TERMINOLOGY

Idd

The positive supply current.

Iss The negative supply current.

 $\mathbf{V}_{D}\left(\mathbf{V}s\right)$ The analog voltage on Terminals D and S.

R_{ON} The ohmic resistance between D and S.

R_{FLAT(ON)}

Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

Is (Off) The source leakage current with the switch off.

 $I_{\rm D}$ (Off) The drain leakage current with the switch off.

 $\mathbf{I}_{\mathrm{D}}, \mathbf{I}_{\mathrm{S}}\left(\mathbf{On}\right)$ The channel leakage current with the switch on.

 $\label{eq:Vinl} V_{\text{INL}}$ The maximum input voltage for Logic 0.

V_{INH} The minimum input voltage for Logic 1.

$$\begin{split} I_{\text{INL}}\left(I_{\text{INH}}\right) \\ \text{The input current of the digital input.} \end{split}$$

Cs (Off)

The off switch source capacitance, measured with reference to ground.

 $C_{\rm D}$ (Off) The off switch drain capacitance, measured with reference to ground. $C_D, C_S(On)$

The on switch capacitance, measured with reference to ground.

C_{IN} The digital input capacitance.

ton The delay between applying the digital control input and the output switching on. See Figure 23.

t_{OFF} The delay between applying the digital control input and the output switching off. See Figure 23.

Charge Injection A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth The frequency at which the output is attenuated by 3 dB.

On Response The frequency response of the on switch.

Insertion Loss The loss due to the on resistance of the switch.

THD + N The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

TYPICAL PERFORMANCE CHARACTERISTICS

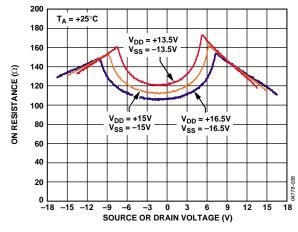


Figure 4. On Resistance as a Function of V_D (V_S) for Dual Supply

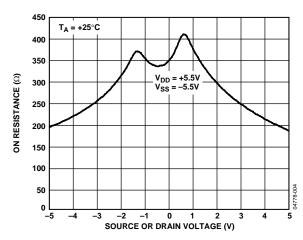


Figure 5. On Resistance as a Function of V_D (V_s) for Dual Supply

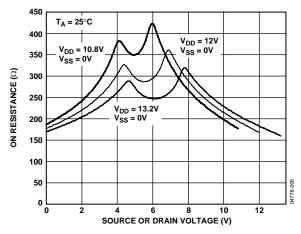


Figure 6. On Resistance as a Function of V_D (V_S) for Single Supply

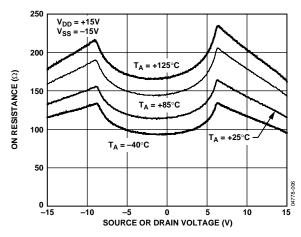


Figure 7. On Resistance as a Function of V_D (V_s) for Different Temperatures, Dual Supply

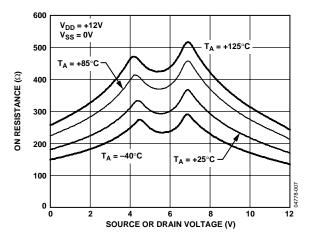


Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

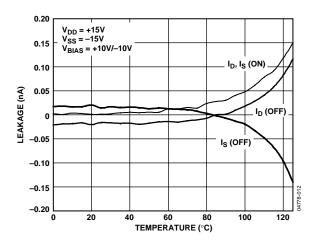


Figure 9. Leakage Currents as a Function of Temperature, Dual Supply

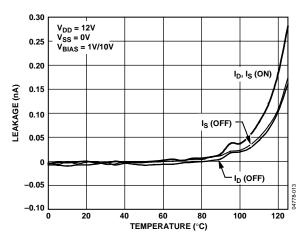
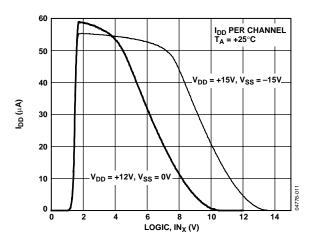


Figure 10. Leakage Currents as a Function of Temperature, Single Supply





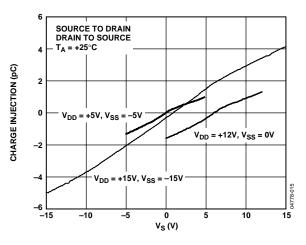


Figure 12. Charge Injection vs. Source Voltage

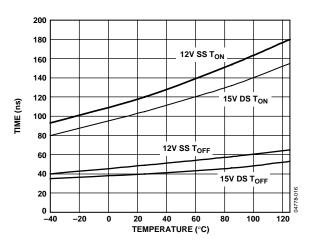
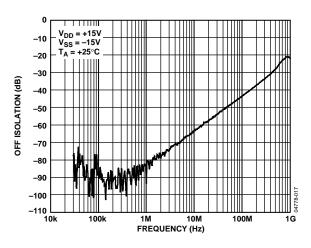


Figure 13. TON/TOFF Times vs. Temperature





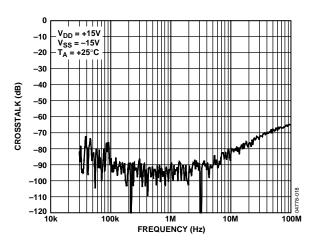
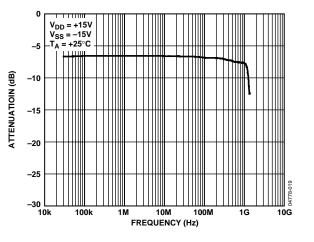
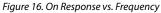


Figure 15. Crosstalk vs. Frequency





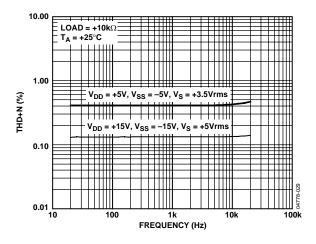


Figure 17. THD + N vs. Frequency

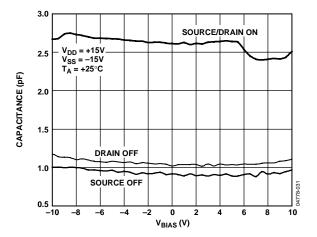


Figure 18. Capacitance vs. Source Voltage, Dual Supply

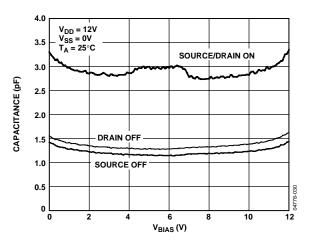
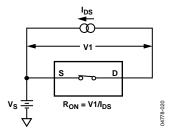


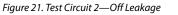
Figure 19. Capacitance vs. Source Voltage, Single Supply

TEST CIRCUITS



 $v_{s} = v_{D} = v_{D}$

Figure 20. Test Circuit 1—On Resistance





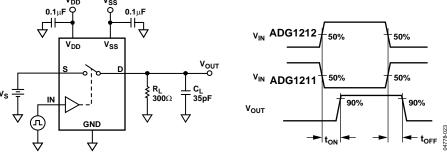


Figure 23. Test Circuit 4—Switching Times

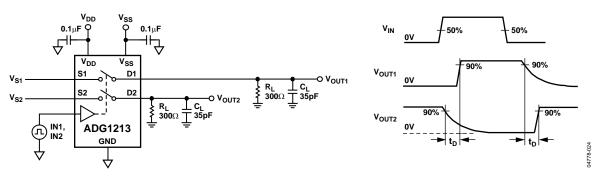


Figure 24. Test Circuit 5—Break-Before-Make Time Delay

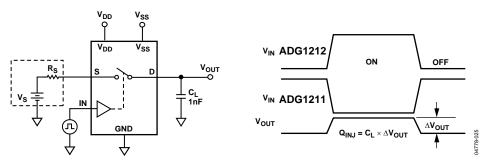


Figure 25. Test Circuit 6—Charge Injection

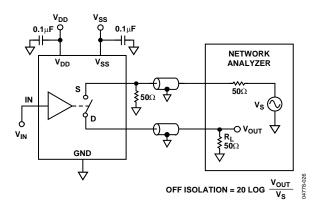


Figure 26. Test Circuit 7—Off Isolation

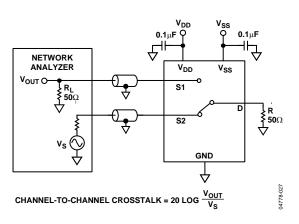


Figure 27. Test Circuit 8—Channel-to-Channel Crosstalk

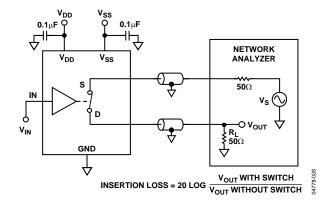


Figure 28. Test Circuit 9—Bandwidth

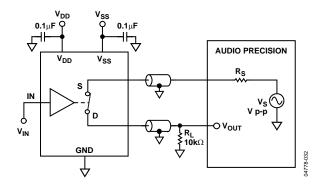
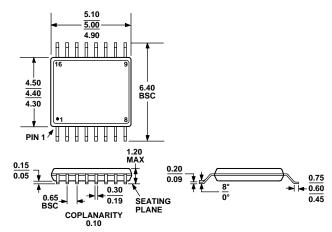


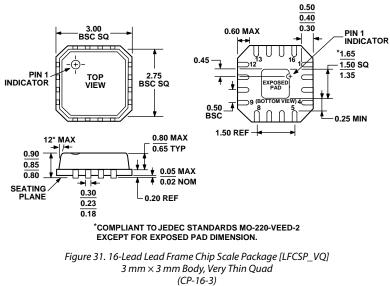
Figure 29. Test Circuit 10—THD + Noise

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153AB

Figure 30. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16) Dimensions shown in millimeters



Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG1211YRUZ ¹	-40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1211YRUZ-REEL ¹	-40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1211YRUZ-REEL71	-40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1211YCPZ-500RL71	-40°C to +125°C	Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-3
ADG1211YCPZ-REEL71	-40°C to +125°C	Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-3
ADG1212YRUZ ¹	-40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1212YRUZ-REEL ¹	-40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1212YRUZ-REEL71	-40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1212YCPZ-500RL71	-40°C to +125°C	Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-3
ADG1212YCPZ-REEL71	-40°C to +125°C	Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-3
ADG1213YRUZ ¹	-40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1213YRUZ-REEL ¹	-40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1213YRUZ-REEL71	-40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1213YCPZ-500RL71	-40°C to +125°C	Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-3
ADG1213YCPZ-REEL71	-40°C to +125°C	Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-3

 1 Z = Pb-free part.

NOTES



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