ANALOG DEVICES

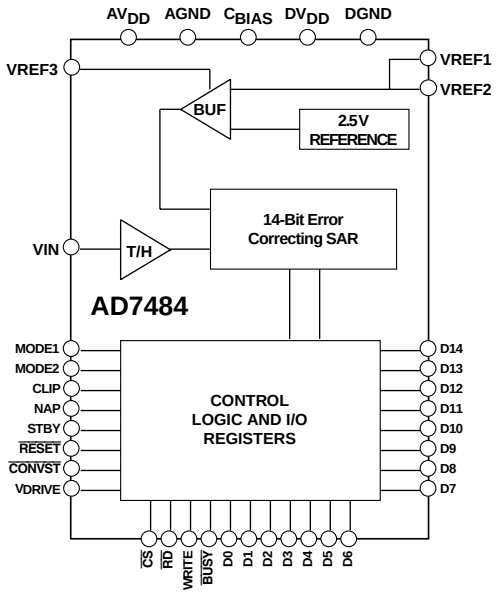
3MSPS, 14-Bit SAR ADC

Preliminary Technical Data — AD7484

FEATURES

Fast Throughput Rate: 3Msps
Wide Input Bandwidth: 50MHz
No Pipeline Delays with SAR ADC
Excellent DC Accuracy Performance
Two Parallel Interface Modes
Low Power:
90mW (Full-Power) and 5mW (NAP Mode)
Standby Mode: 1µA max
Single +5V Supply Operation
Internal +2.5V Reference
Full-Scale Overrange Mode (using 15th bit)
System Offset Removal via User Access Offset Register
Nominal 0 to +2.5V Input with Shifted Range Capability
Pin Compatible Upgrade of 12-Bit AD7482

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7484 is a 14-bit, high speed, low power, successive-approximation ADC. The part features a parallel interface with throughput rates up to 3Msps. The part contains a low-noise, wide bandwidth track/hold amplifier which can handle input frequencies in excess of 50MHz.

The conversion process is a proprietary algorithmic successive-approximation technique which results in no pipeline delays. The input signal is sampled and a conversion is initiated on the falling edge of the $\overline{\text{CONVST}}$ signal. The conversion process is controlled via an internally trimmed oscillator. Interfacing is via standard parallel signal lines making the part directly compatible with microcontrollers and DSPs.

The AD7484 provides excellent ac and dc performance specifications. Factory trimming ensures high dc accuracy resulting in very low INL, offset and gain errors.

The part uses advanced design techniques to achieve very low power dissipation at high throughput rates. Power consumption in normal mode of operation is 90mW. There are two power-saving modes: a NAP mode, which keeps the reference circuitry alive for a quick power up while consuming 5mW and a STANDBY mode which reduces power consumption to a mere 5µW.

The AD7484 features an on-board +2.5V reference but the part can also accomodate an externally-provided +2.5V reference source. The nominal analog input range is 0 to +2.5V but an offset shift capability allows this nominal range to be offset by +/-200mV. This allows the user considerable flexibility in setting the bottom end reference point of the signal range, a useful feature when using single-supply op-amps.

The AD7484 also provides the user with an 8% overrange capability via a 15th bit. Thus, if the analog input range strays outside the nominal by up to 8%, the user can still accurately resolve the signal by using the 15th bit.

The AD7484 is powered from a +4.75V to +5.25V supply. The part also provides a V_{DRIVE} pin which allows the user to set the voltage levels for the digital interface lines. The range for this V_{DRIVE} pin is from +2.7V to +5.25V. The part is housed in a 48-pin LQFP package and is specified over a -40°C to +85°C temperature range.

REV. PrC 7/13/01

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD7484–SPECIFICATIONS

(T_A = 25°C, V_{DD} = 4.75 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25 V, f_{SAMPLE} = 3MSPS)

Parameter	Specification	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			F_{IN} = 100kHz Sine Wave
Signal to Noise + Distortion (SINAD)[2]	78	dB min	
Signal to Noise Ratio (SNR)[2]	78	dB min	
Total Harmonic Distortion (THD)[2]	-90	dB max	
Peak Harmonic or Spurious Noise (SFDR)[2]	TBD	dB max	
Intermodulation Distortion (IMD)[2]			
Second Order Terms	TBD	dB typ	
Third Order Terms	TBD	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	10	ps typ	
Full Power Bandwidth	50	MHz typ	@ 3 dB
	TBD	MHz typ	@0.1 dB
DC ACCURACY			
Resolution	14	Bits	
Integral Nonlinearity[2]	TBD	LSB max	
	±1	LSB typ	
Differential Nonlinearity[2]	TBD	LSB max	Guaranteed No Missed Codes to 14 bits
	±1	LSB typ	
Offset Error[2]	±1.5	LSB max	
Gain Error[2]	±1.5	LSB max	
ANALOG INPUT			
Input Voltage	-200	mV min	
	+2.7	Volts max	
DC Leakage Current	TBD	µA max	
Input Capacitance	10	pF typ	
REFERENCE INPUT/OUTPUT			
V_{REF} Input Voltage	+2.5	Volts	±1% for specified performance
V_{REF} Input DC Leakage Current	±1	µA max	
V_{REF} Input Capacitance	TBD	pF max	
V_{REF} Output Voltage	+2.5	V nom	
V_{REF} Error @ 25°C	TBD	mV max	
V_{REF} Error T_{MIN} to T_{MAX}	TBD	mV max	
V_{REF} Output Impedance	TBD	kΩ typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	TBD	V min	
Input Low Voltage, V_{INL}	0.4	V max	
Input Current, I_{IN}	TBD	µA max	
Input Capacitance, C_{IN}[2]	TBD	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} - 0.2	V min	
Output Low Voltage, V_{OL}	0.4	V max	
Floating-State Leakage Current	TBD	µA max	
Floating-State Output Capacitance[2,3]	TBD	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	TBD	ns max	
Track/Hold Acquisition Time	TBD	ns max	Sine Wave Input
	TBD	ns max	Full-Scale Step Input
Throughput Rate	3	MSPS max	
POWER REQUIREMENTS			
V_{DD}	+5	Volts	±5%
V_{DRIVE}	+2.7	V min	
	+5.25	V max	
I_{DD} Normal Mode (Static)	TBD	mA typ	
Normal Mode (Operational)	18	mA typ	
NAP Mode	1	mA typ	
Standby Mode	1	µA max	

Parameter	Specification	Units	Test Conditions/Comments
POWER REQUIREMENTS *(continued)*			
Power Dissipation			
Normal Mode (Operational)	90	mW max	
NAP Mode	5	mW max	
Standby Mode	5	µW max	

NOTES
[1]Temperature ranges as follows: –40°C to +85°C.
[2]See Terminology
[3]Sample tested @ +25°C to ensure compliance
Specifications subject to change without notice.

TIMING CHARACTERISTICS [1,2] (V_{DD} = 5 V ±5%, AGND = DGND = 0 V, V_{REF} = Internal; All specifications T_{MIN} to T_{MAX} and valid for V_{DRIVE} = 2.7 V to 5.25 V unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units
Data Read					
Acquisition Time	t_{ACQ}	TBD			ns
Conversion Time	t_{CONV}			TBD	ns
Quiet Time before Conversion start	t_{QUIET}	TBD			ns
Quiet Time during Conversion	t_{QUIET2}	TBD			ns
$\overline{CONVST}$ Pulse Width	t_1	TBD			ns
$\overline{CONVST}$ falling edge to $\overline{BUSY}$ falling edge	t_2	TBD		TBD	ns
$\overline{CS}$ falling edge to $\overline{RD}$ falling edge	t_3	TBD			ns
Bus Access Time	t_4		TBD		ns
$\overline{CONVST}$ falling edge to new Data valid	t_5			TBD	ns
$\overline{BUSY}$ rising edge to new Data valid	t_6			TBD	ns
Bus Relinquish Time	t_7		TBD		ns
$\overline{RD}$ rising edge to $\overline{CS}$ rising edge	t_8	TBD			ns
Data Write					
WRITE Pulse Width	t_9	TBD			ns
Data Setup time	t_{10}	TBD			ns
Data Hold time	t_{11}	TBD			ns
$\overline{CS}$ falling edge to WRITE rising edge	t_{12}	TBD			ns
WRITE falling edge to $\overline{CS}$ rising edge	t_{13}	TBD			ns

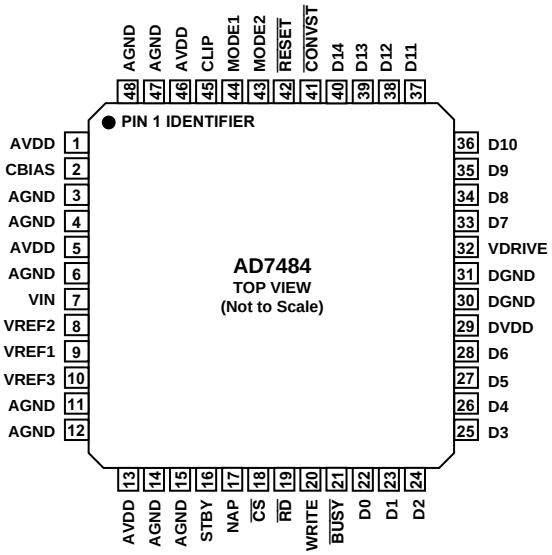
ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND .....-0.3 V to +7 V
V_{DRIVE} to GND .....-0.3 V to +7 V
Analog Input Voltage to GND .. -0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to GND .. -0.3 V to DV_{DD} + 0.3 V
REF IN to GND ..... -0.3 V to AV_{DD} + 0.3 V
Input Current to Any Pin Except Supplies ..... ±10mA
Operating Temperature Range
  Commercial ..... –40°C to +85°C
  Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
48-Pin LQFP Package, Power Dissipation .....TBD
  θ_{JA} Thermal Impedance ..... 50°C/W
  θ_{JC} Thermal Impedance ..... 10°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 secs) ..... +215°C
    Infared (15 secs) ..... +220°C
ESD .....TBD

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Option
AD7484BST	-40°C to +85°C	Low-profile Quad Flat Pack	ST-48
EVAL-AD7484CB[1]		Evaluation Board	
EVAL-CONTROL BRD2[2]		Controller Board	

NOTES
[1]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
[2]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7484 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Description
AVDD	Positive power supply for analog circuitry.
C_{BIAS}	Decoupling pin for internal bias voltage. A 100nF capacitor should be placed between this pin and AGND.
AGND	Power supply ground for analog circuitry.
VIN	Analog input. Single-ended analog input channel.
VREF1	Reference Output. VREF1 connects to the output of the internal 2.5V reference. A 1µF capacitor must be placed between this pin and AGND.
VREF2	Reference Input. A 1µF capacitor must be placed between this pin and AGND. When using an external voltage reference source, the reference voltage should be applied to this pin.
VREF3	Reference decoupling pin. When using the internal reference, a 100nF must be connected from this pin to AGND. When using an external reference source, this pin should be connected directly to AGND.
STBY	Standby logic input. When this pin is logic high, the device will be placed in Standby mode. See Power Saving Section for further details.
NAP	Nap logic input. When this pin is logic high, the device will be placed in a very low power mode. See Power Saving Section for further details.
DVDD	Positive power supply for digital circuitry.
DGND	Ground reference for digital circuitry.
V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin will determine at what voltage the interface logic of the AD7484 will operate.
$\overline{CONVST}$	Convert Start Logic Input. A conversion is initiated on the falling edge of $\overline{CONVST}$ signal. The input track/hold amplifier goes from track mode to hold mode and the conversion process commences.
$\overline{RESET}$	Reset Logic Input. A logic 0 on this pin resets the internal state machine and terminates a conversion that may be in progress. Holding this pin low keeps the part in a reset state.
MODE2	Operating Mode Logic Input. See Table 3 for details.
MODE1	Operating Mode Logic Input. See Table 3 for details.
CLIP	Logic input. A logic high on this pin enables output clipping. In this mode, any input voltage that is greater than positive full scale or less than negative full scale will be clipped to all 1's or all 0's respectively. Further details are given in the Offset / Overrange setion.
$\overline{CS}$	Chip Select Logic Input. This pin is used in conjunction with $\overline{RD}$ to access the conversion result. The data bus is brought out of tri-state and the current contents of the output register driven onto the data lines following the falling edge of both $\overline{CS}$ and $\overline{RD}$. $\overline{CS}$ is also used in conjunction with WRITE to perform a write to the Offset Register. $\overline{CS}$ can be hardwired permanently low.
$\overline{RD}$	Read Logic Input. Used in conjunction with $\overline{CS}$ to access the conversion result.
WRITE	Write Logic Input. Used in conjunction with $\overline{CS}$ to write data to the Offset Register. When the desired offset word has been placed on the data bus, the WRITE line should be pulsed high. It is the falling edge of this pulse which latches in the word into the Offset Register.
$\overline{BUSY}$	Busy Logic Output. This pin indicates the status of the conversion process. The $\overline{BUSY}$ signal goes low after the falling edge of $\overline{CONVST}$ and stays low for the duration of the conversion. In Parallel Mode 2, the $\overline{BUSY}$ signal returns high when the conversion result has been clocked into the output register. In Parallel Mode 1, the $\overline{BUSY}$ signal returns high as soon as the conversion has been completed but the conversion result does not get clocked into the output register until the falling edge of the next $\overline{CONVST}$ pulse.
D0 - D13	Data I/O Bits (D13 is MSB). These are tri-state pins that are controlled by $\overline{CS}$, $\overline{RD}$ and WRITE. The operating voltage level for these pins is determined by the V_{DRIVE} input.
D14	Data Output Bit for overranging. If the over range feature is not used, this pin should be pulled to DGND via a 100kΩ resistor.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e AGND + 0.5 LSB

Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., V_{REF} – 1.5 LSB) after the offset error has been adjusted out.

Track/Hold Acquisition Time
Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track/hold returns to track mode).

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

Signal to (*Noise* + *Distortion*) = (6.02 *N* + 1.76) *dB*

Thus for a 14-bit converter, this is 86.04 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7484 it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7484 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

CIRCUIT DESCRIPTION

CONVERTER OPERATION

The AD7484 is a 14-bit error correcting successive approximation analog-to-digital converter based around a capacitive DAC. It provides the user with track/hold, reference, A/D converter and versatile interface logic functions on a single chip. The normal analog input signal range that the AD7484 can convert is 0 to 2.5 Volts. By using the offset and overrange features on the ADC, the AD7484 can convert analog input signals from -200mV to +2.7V while operating from a single +5V supply. The part requires a +2.5V reference which can be provided from the part's own internal reference or an external reference source. Figure 1 shows a very simplified schematic of the ADC. The Control Logic, SAR and the Capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back to a balanced condition.

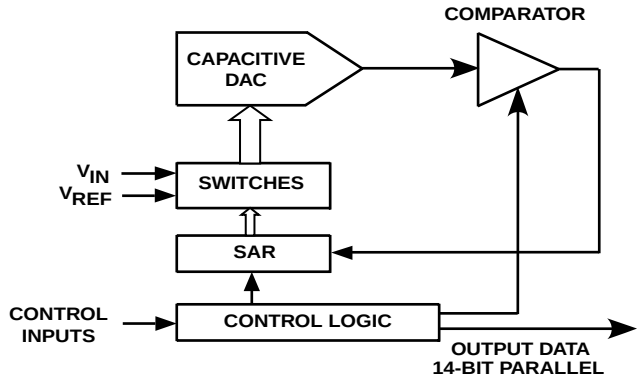


Figure 1. Simplified Block Diagram of AD7484

Conversion is initiated on the AD7484 by pulsing the $\overline{\text{CONVST}}$ input. On the falling edge of $\overline{\text{CONVST}}$, the track/hold goes from track to hold mode and the conversion sequence is started. Conversion time for the part is TBD nS. Figure 2 shows the ADC during conversion. When conversion starts, SW2 will open and SW1 will move to position B causing the comparator to become unbalanced. The ADC then runs through its successive approximation routine and brings the comparator back into a balanced condition. When the comparator is rebalanced, the conversion result is available in the SAR register.

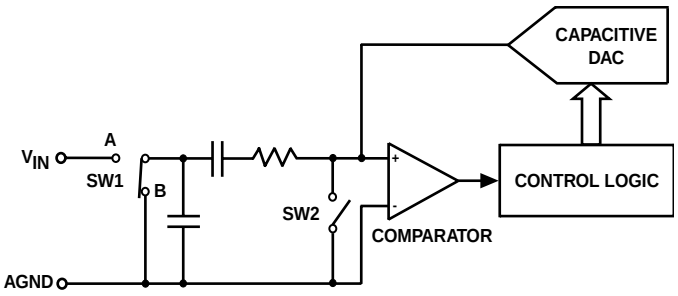


Figure 2. ADC Conversion Phase

At the end of conversion, the track/hold returns to tracking mode and the acquisition time begins. The track/hold acquisition time is TBD nS. Figure 3 shows the ADC during its acquistition phase. SW2 is closed and SW1 is in position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on V_{IN}.

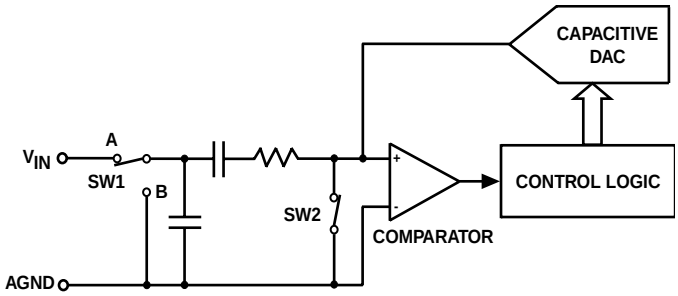


Figure 3. ADC Acquisition Phase

ADC TRANSFER FUNCTION

The output coding of the AD7484 is straight binary. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, etc.). The LSB size is V_{REF} / 16384. The nominal transfer characteristic for the AD7484 in shown in figure 4 below. This transfer characteristic may be shifted as detailed in the Offset/Overrange section.

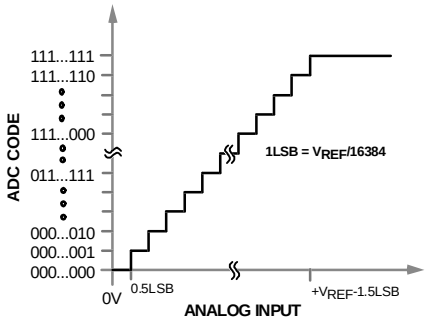


Figure 4. AD7484 Transfer Characteristic

POWER SAVING

The AD7484 uses advanced design techniques to achieve very low power dissipation at high throughput rates. In addition to this the AD7484 features two power saving modes, Nap Mode and Standby Mode. These modes are selected by bringing either the NAP or STBY pin to a logic high respectively.

When operating the AD7484 in normal, fully powered mode, the current consumption is 18mA during conversion and the quiescent current is 5mA. Operating at a throughput rate of 1MSPS, the conversion time of 300nS contributes 27mW to the overall power dissipation.

(300nS / 1µS) x (5V x 18mA) = 27mW

For the remaining 700nS of the cycle, the AD7484 dissipates 17.5mW of power.

(700nS / 1µS) x (5V x 5mA) = 17.5mW

Thus the power dissipated during each cycle is:

27mW + 17.5mW = 44.5mW

Figure 5 below shows the AD7484 conversion sequence operating in normal mode.

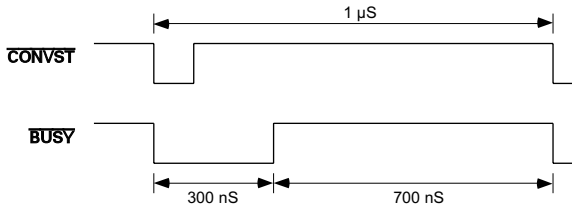


Figure 5. Normal Mode Power Dissipation

In NAP mode, all the internal circuitry except for the internal reference is powered down. In this mode, the power dissipation of the AD7484 is reduced to 5mW. When exiting NAP mode a minimum of 100nS must be waited before initiating a conversion. This is necessary to allow the internal circuitry to settle after power-up and for the track/hold to properly acquire the analog input signal.

If the AD7484 is put into NAP mode after each conversion, the average power dissipation will be reduced but the throughput rate will be limited by the power-up time. Using the AD7484 with a throughput rate of 1MSPS while placing the part in NAP mode after each conversion would result in average power dissipation as follows: The power-up and conversion phase will contribute 36mW to the overall power dissipation.

(400nS / 1µS) x (5V x 18mA) = 36mW

While in NAP mode for the rest of the cycle, the AD7484 dissipates only 3mW of power.

(600nS / 1µS) x (5V x 1mA) = 3mW

Thus the power dissipated during each cycle is:

36mW + 3mW = 39mW

Figure 6 shows the AD7484 conversion sequence if putting the part into NAP mode after each conversion.

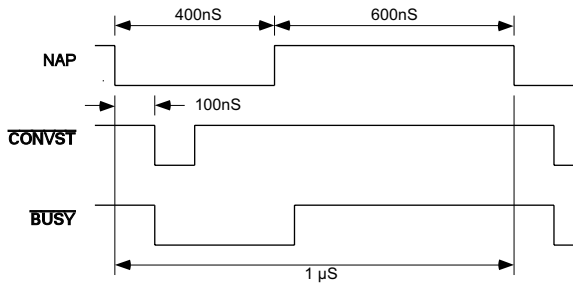


Figure 6. NAP Mode Power Dissipation

Figures 7 and 8 show a typical graphical representation of Power vs. Throughput for the AD7484 when in Normal and Nap modes respectively.

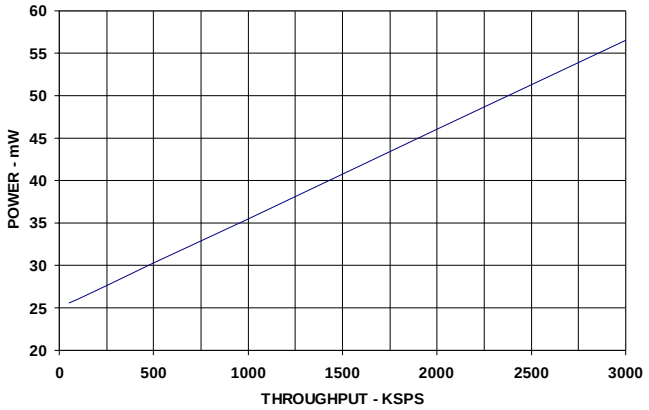


Figure 7. Normal Mode - Power vs. Throughput

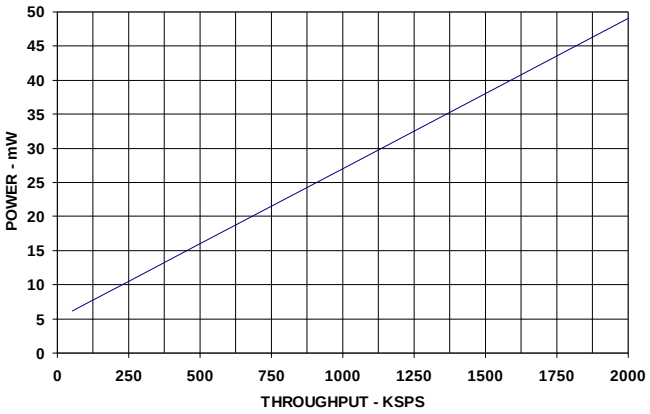


Figure 8. Nap Mode - Power vs. Throughput

In STANDBY mode, all the internal circuitry is powered down and the power consumption of the AD7484 is reduced to 5µW. The power-up time necessary before a conversion can be initiated is longer because the internal reference has been powered down. If using the internal reference of the AD7484, the ADC must be brought out of STANDBY mode 200µS before a conversion is initiated. Initiating a conversion before the required power-up time has elapsed will result in incorrect conversion data. If an external reference source is used and kept powered up while the AD7484 is in STANDBY mode, the power-up time required will be reduced.

OFFSET / OVERRANGE

The AD7484 provides a ±8% overrange capability as well as a programmable Offset Register. The overrange capability is achieved by the use of a 15th bit (D14) and the CLIP input. If the CLIP input is at logic high and the contents of the offset register are zero, then the AD7484 operates as a normal 14-bit ADC. If the input voltage is greater than the full-scale voltage, the data output from the ADC will be all 1's. Similarly, if the input voltage is lower than the zero-scale voltage, the data output from the ADC will be all 0's. In this case D14 acts as an overrange indicator. It is set to a 1 if the analog input voltage is outside the nominal 0 to +2.5V range.

If the Offset Register contains any value other than zero, the contents of the register are added to the SAR result at the end of conversion. This has the effect of shifting the transfer function of the ADC as shown in Figure 9 and Figure 10. However, it should be noted that with the CLIP input set to logic high, the maximum and minimum codes that the AD7484 will ouput will be 0x3FFF and 0x0000 respectively. Further details are given in Table 1 and Table 2.

Figure 9 shows the effect of writing a positive value to the Offset Register. If, for example, the contents of the Offset Register contained the value 1024, then the value of the analog input voltage for which the ADC would transition from reading all 0's to 000...001 (the bottom reference point) would be:

0.5LSB - (1024 LSBs) = -156.326mV

The analog input voltage for which the ADC would read full-scale (0x3FFF) in this example would be:

2.5V -1.5LSBs - (1024 LSBs) = 2.34352V

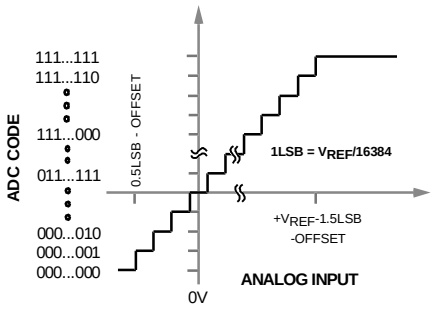


Figure 9. Transfer Characteristic With Positive Offset

The effect of writing a negative value to the Offset Register is shown in Figure 10. If a value of -512 was written to the Offset Register, the bottom end reference point would now occur at:

0.5LSB - (-512 LSBs)= +78.20mV

Following from this, the analog input voltage needed to produce a full-scale (0x3FFF) result from the ADC would now be:

2.5V - 1.5LSBs - (-512 LSBs) = 2.5779V

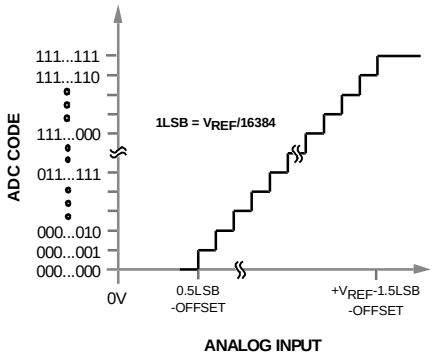


Figure 10. Transfer Characteristic With NegativeOffset

Table 1 below shows the expected ADC result for a given analog input voltage with different offset values and with CLIP tied to logic high. The combined advantages of the offset and overrange features of the AD7484 are shown clearly in Table 2. It shows the same range of analog input and offset values as Table 1 but with the clipping feature disabled.

OFFSET	-512	0	+1024	
VIN	ADC DATA, D[0:13]			D14
-200mV	0	0	0	1
-156.3mV	0	0	0	1
0V	0	0	1024	0
+78.2mV	0	512	1536	0
+2.3435V	14847	15359	16383	0
+2.5V	15871	16383	16383	0
+2.5779V	16383	16383	16383	1
+2.7V	16383	16383	16383	1

Table 1. Clipping Enabled (CLIP = 1)

OFFSET	-512	0	+1024
VIN	ADC DATA, D[0:14]		
-200mV	-1822	-1310	-286
-156.3mV	-1536	-1024	0
0V	-512	0	1024
+78.2mV	0	512	1536
+2.3435V	14847	15359	16383
+2.5V	15871	16383	17407
+2.5779V	16383	16895	17919
+2.7V	17182	17694	18718

Table 2. Clipping Disabled (CLIP = 0)

Values from -1310 to +1310 may be written to the Offset Register. These values correspond to an offset of ±200mV. A write to the Offset Register is performed by writing a 15-bit word to the part as detailed in the Interfacing sections. The 12 LSBs of the 15-bit word contain the offset value, the 3 MSBs must be set to zero. Failure to write zeros to the 3 MSBs may result in the incorrect operation of the device.

PARALLEL INTERFACE

The AD7484 features two parallel interfacing modes. These modes are selected by the Mode pins as detailed in Table 3.

	Mode 2	Mode 1
Not Used	**0**	**0**
Parallel Mode 1	**0**	**1**
Parallel Mode 2	**1**	**0**
Not Used	**1**	**1**

Table 3. AD7484 Operating Modes

In Parallel Mode 1, the data in the output register is updated and available for reading when $\overline{BUSY}$ returns high at the end of a conversion. This mode should be used if the conversion data is required immediately after the conversion has completed. An example where this may be of use is if the AD7484 were operating at much lower throughput rates in conjunction with Nap Mode (for power-saving reasons) and the input signal being compared with set limits. If the limits were exceeded, the ADC would then be woken up and commence sampling at full speed. Figure 12 shows a timing diagram for the AD7484 operating in Parallel Mode 1.

In Parallel Mode 2, the data in the output register is not updated until the next falling edge of $\overline{CONVST}$. This mode could be used where a single sample delay is not vital to the system operation. This may occur, for example, in a system where a large amount of samples are taken at high speed before a Fast Fourier Transform is performed for frequency analysis of the input signal. Figure 13 shows a timing diagram for the AD7484 operating in Parallel Mode 2.

Reading Data from the AD7484

Data is read from the part via a 15-bit parallel data bus with the standard $\overline{CS}$ and $\overline{RD}$ signals. The $\overline{CS}$ and $\overline{RD}$ signals are internally gated to enable the conversion result onto the data bus. The data lines D0 to D14 leave their high impedance state when both $\overline{CS}$ and $\overline{RD}$ are logic low. Therefore, $\overline{CS}$ may be permanently tied logic low if required and the $\overline{RD}$ signal used to access the conversion result. Figures 12 and 13 show timing specifications called t_{QUIET} and t_{QUIET2}. The quiet time, t_{QUIET}, is the amount of time that should be left after any data bus activity before the next conversion is initiated. The second quiet time, t_{QUIET2}, is the period during a conversion where activity on the data bus should be avoided. Reading a result from the AD7484 while the latter half of the conversion is in progress will result in the degradation of performance by about TBD dB.

Writing to the AD7484

The AD7484 features a user accessible offset register. This allows the bottom of the transfer function to be shifted by ±200mV. This feature is explained in more detail in the Offset / Overrange section.

To write to the offset register a 15-bit word is written to the AD7484 with the 12 LSBs containing the offset value in 2's complement format. The 3 MSBs must be set to zero. The offset value must be within the range -1310 to +1310, corresponding to an offset from -200mV to +200mV. The value written to the offset register is stored and used until power is removed from the device. The value stored may be updated at any time between conversions by another write to the device. Table 4 shows some examples of offset register values and their effective offset voltage. Figure 14 shows a timing diagram for writing to the AD7484.

Code (Dec)	D14-D12	D11-D0 (2's Comp)	Offset (mV)
-1310	000	101011100010	-200
-512	000	111000000000	-78.12
+256	000	000100000000	+39.06
+1310	000	010100011110	+200

Table 4. Offset Register Examples

Typical Connection

Figure 11 shows a typical connection diagram for the AD7484 operating in Parallel Mode 1. Conversion is initiated by a falling edge on $\overline{CONVST}$. Once $\overline{CONVST}$ goes low, the $\overline{BUSY}$ signal goes low and at the end of conversion, the rising edge of $\overline{BUSY}$ is used to activate an Interrupt Service Routine. The $\overline{CS}$ and $\overline{RD}$ lines are then activated to read the 14 data bits (15 bits if using the overrange feature).

In Figure 11 the V_{DRIVE} pin is tied to DV_{DD}, which results in logic output levels being either 0 V or DV_{DD}. The voltage applied to V_{DRIVE} controls the voltage value of the output logic signals. For example, if DV_{DD} is supplied by a 5 V supply and V_{DRIVE} by a 3 V supply, the logic output levels would be either 0 V or 3 V. This feature allows the AD7484 to interface to 3 V devices while still enabling the ADC to process signals at 5 V supply.

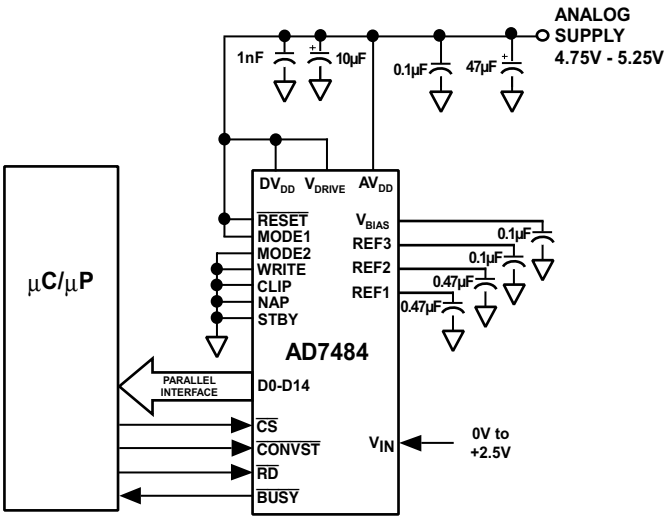


Figure 11. AD7484 Typical Connection Diagram

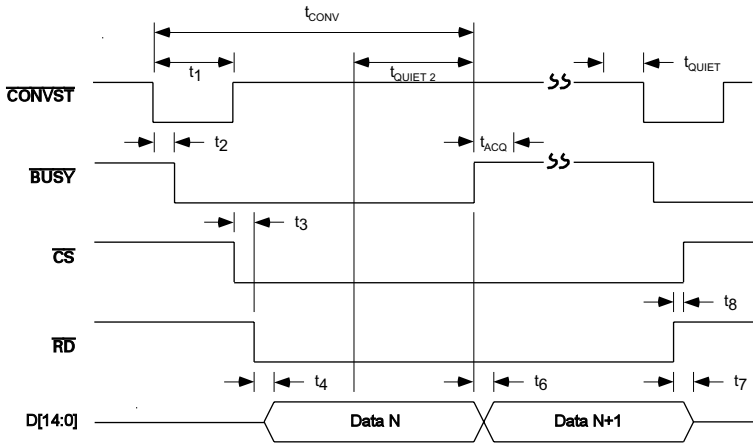


Figure 12. Parallel Mode 1 Read Cycle

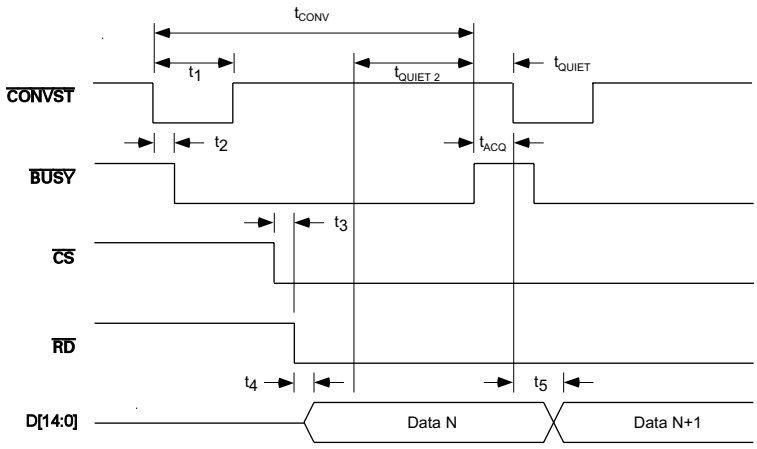


Figure 13. Parallel Mode 2 Read Cycle

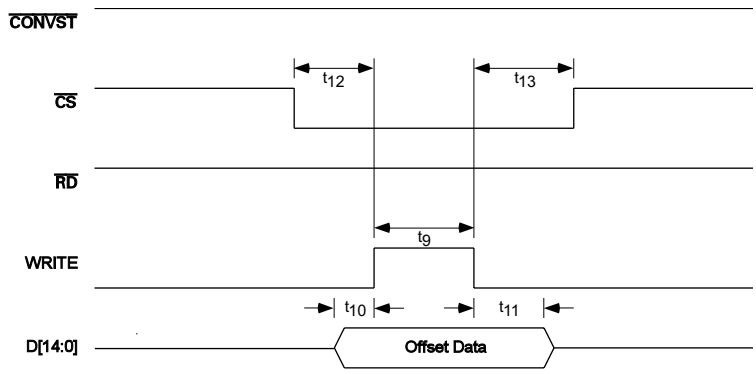


Figure 14. Parallel Mode Write Cycle

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Pin LQFP Package (ST-48)