查询AD7150供应商

Ultra Low Power, 2 Channel, Capacitance Converter for Proximity Sensing

Preliminary Technical Data

AD7150

FEATURES

- Ultra low power
  - 3.3 V, 90 uA
- Response time 10 ms
- Adaptive environmental compensation
- Two independent capacitance input channels
  - Sensor capacitance (C_{SENS}) 0 up to 14 pF
  - Sensitivity to 0.8 fF
- EMC tested
- Two modes of operation:
  - Standalone with fixed settings
  - Interfaced to a uC for user-defined settings
- Two proximity detection output flags
- 2-wire serial interface (I^2C®-compatible)
- Operating temperature:
  - -40°C to +125°C
- 10-lead uSOIC package

APPLICATIONS

- Proximity sensing
- Contact-less switching
- Position detection
- Level detection

GENERAL DESCRIPTION

The AD7150 delivers a complete signal processing solution for capacitive proximity sensors, featuring an ultra low power converter with fast response time.

The AD7150 uses Analog Devices' capacitance to digital converter (CDC) technology, which combines features important for interfacing to real sensors, such as a high input sensitivity and a high tolerance of both input parasitic ground capacitance and leakage current.

The integrated adaptive threshold algorithm compensates for any variations in the sensor capacitance due to environmental factors like humidity and temperature, or changes in the dielectric material over time.

By default, the AD7150 operates in standalone mode using the fixed power up settings and indicates detection on two digital outputs. Alternatively, the AD7150 can be interfaced to a uC via I^2C interface, the internal registers can be programmed with user-defined settings and the data and status can be read from the part.

The AD7150 operates from a 3.3 V power supply. It is specified over the temperature range of -40°C to +125°C.

FUNCTIONAL BLOCK DIAGRAM

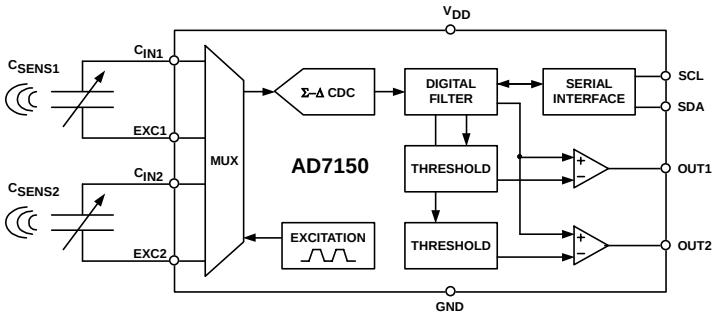

Figure 1.

Rev. PrD, 8. November 2006

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REVISION HISTORY

Pre-Release Preliminary Datasheet

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PRELIMINARY SPECIFICATIONS

V_{DD} = 3.0 V to 3.6 V; GND = 0 V; –40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CAPACITIVE INPUT					
Capacitive Input Ranges		4		pF[1]	
		2		pF	
		1		pF	
		0.5		pF	
Resolution		2.0		fF[1]	4 pF Range
		1.6		fF	2 pF Range
		1.4		fF	1 pF Range
		0.8		fF	0.5 pF Range
Allowed Capacitance to GND			100	pF	
Response time			10	ms	
Power Supply Rejection		TBD		fF/V	
Channel-to-Channel Isolation		TBD		dB	
CAPDAC [2]					
Full Range	10			pF	
Resolution		160		fF	
AutoDAC Increment / Decrement	25		75	% of C_{IN} Range	
LOGIC OUTPUTS (OUT1, OUT2)					
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = 8 mA
V_{OH} Output High Voltage	V_{DD} – 0.6			V	I_{SOURCE} = 8 mA
SERIAL INTERFACE LOGIC INPUTS (SCL, SDA)					
V_{IH} Input High Voltage	2.1			V	
V_{IL} Input Low Voltage			0.8	V	
Hysteresis		150		mV	
Input Leakage Current (SCL)		±0.1	±1	µA	
OPEN-DRAIN OUTPUT (SDA)					
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = –6.0 mA
I_{OH} Output High Leakage Current		0.1	1	µA	V_{OUT} = V_{DD}
POWER REQUIREMENTS					
V_{DD}-to-GND Voltage	3.0		3.6	V	V_{DD} = 3.3 V, nominal
I_{DD} Current [3]		90	100	µA	–40°C to +85°C
			180	µA	–40°C to +125°C
I_{DD} Current Power-Down Mode [3]		1	TBD	µA	–40°C to +85°C
			TBD	uA	–40°C to +125°C

[1] Capacitance units: 1 pF = 10^{-12} F; 1 fF = 10^{-15} F.
[2] The CAPDAC can be used to shift (offset) the input range. The total capacitance of the sensor can be therefore up to sum of the max CAPDAC value and the input range. With the auto CAPDAC feature, the CAPDAC is adjusted automatically when the CDC input value is lower than 25% or higher than 75% of the CDC input range.
[3] Digital inputs equal to V_{DD} or GND

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TIMING SPECIFICATIONS

V_{DD} = 3.0 V to 3.6 V; GND = 0 V; Input Logic 0 = 0 V; Input Logic 1 = V_{DD}; –40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL INTERFACE[1, 2]					See Figure 2
SCL Frequency	0		400	kHz	
SCL High Pulse Width, t_{HIGH}	0.6			µs	
SCL Low Pulse Width, t_{LOW}	1.3			µs	
SCL, SDA Rise Time, t_R			0.3	µs	
SCL, SDA Fall Time, t_F			0.3	µs	
Hold Time (Start Condition), $t_{HD;STA}$	0.6			µs	After this period, the first clock is generated
Set-Up Time (Start Condition), $t_{SU;STA}$	0.6			µs	Relevant for repeated start condition
Data Set-Up Time, $t_{SU;DAT}$	0.1			µs	
Set-Up Time (Stop Condition), $t_{SU;STO}$	0.6			µs	
Data Hold Time, $t_{HD;DAT}$ (Master)	0			µs	
Bus-Free Time (Between Stop and Start Condition, t_{BUF})	1.3			µs	

[1] Sample tested during initial release to ensure compliance.
[2] All input signals are specified with input rise/fall times = 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Output load = 10 pF.

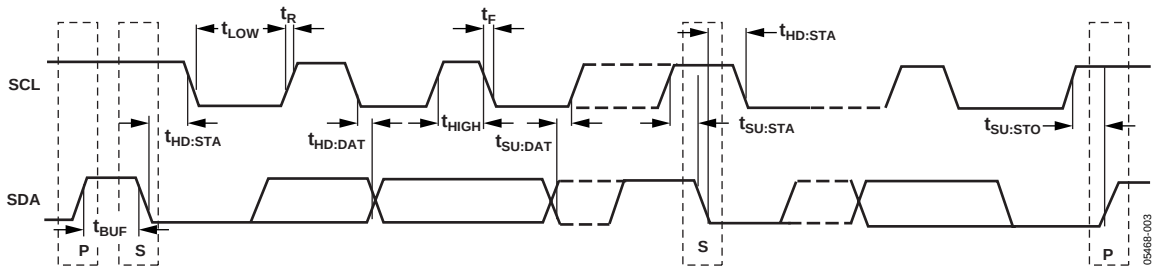

Figure 2. Serial Interface Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Positive Supply Voltage V_{DD} to GND	–0.3 V to + 3.9 V
Voltage on any Input or Output to GND	–0.3 V to V_{DD} + 0.3 V
ESD Rating (ESD Association Human Body Model, S5.1)	TBD V
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
uSOIC Package θ_{JA}, (Thermal Impedance-to-Air)	206°C/W
uSOIC Package θ_{JC}, (Thermal Impedance-to-Case)	44 °C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

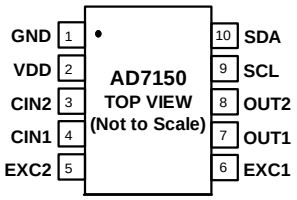

Figure 3. AD7150 Pin Configuration(10-Lead MSOP)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground Pin.
2	VDD	Power Supply Voltage. This pin should be decoupled to GND, using a low impedance capacitor, for example 0.1 µF X7R multilayer ceramic.
3	CIN2	CDC Capacitive Input Channel 2. The measured capacitance (sensor) is connected between the EXC2 pin and CIN2 pin. If not used, this pin can be left open circuit or connected to GND.
4	CIN1	CDC Capacitive Input Channel 1. The measured capacitance (sensor) is connected between the EXC1 pin and CIN1 pin. If not used, this pin can be left open circuit or connected to GND.
5	EXC2	CDC Excitation Output. The measured capacitance is connected between the EXC2 pin and CIN2 pin. If not used, this pin should be left as an open circuit.
6	EXC1	CDC Excitation Output. The measured capacitance is connected between the EXC1 pin and CIN1 pin. If not used, this pin should be left as an open circuit.
7	OUT1	Logic output. High level on this output indicates proximity detected on capacitive input 1.
8	OUT2	Logic output. High level on this output indicates proximity detected on capacitive input 2.
9	SCL	Serial Interface Clock Input. Connects to the master clock line. Requires a pull-up resistor if not provided elsewhere in the system.
10	SDA	Serial Interface Bidirectional Data. Connects to the master data line. Requires a pull-up resistor if not provided elsewhere in the system.

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TYPICAL PERFORMANCE CHARACTERISTICS

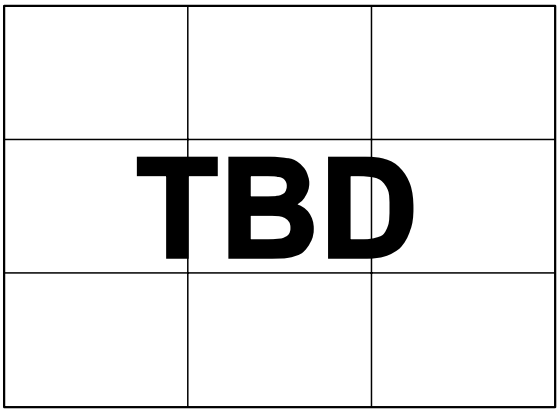

Figure 4.

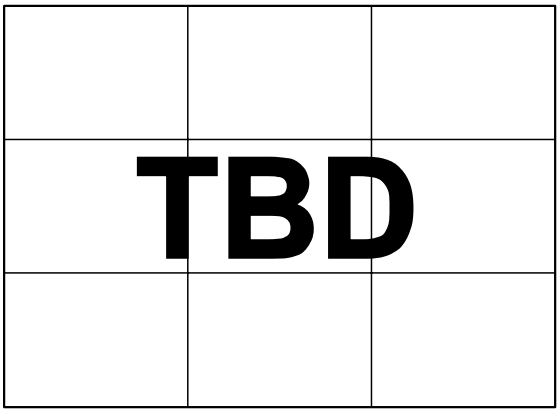

Figure 7.

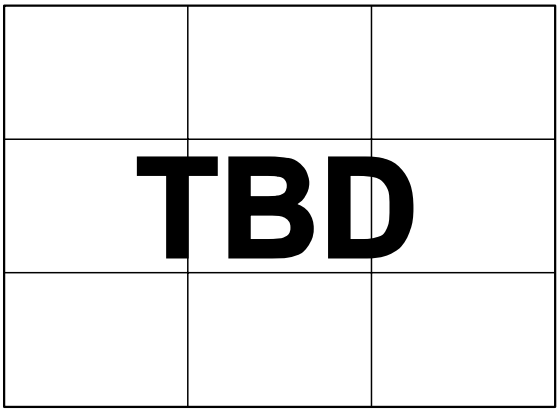

Figure 5.

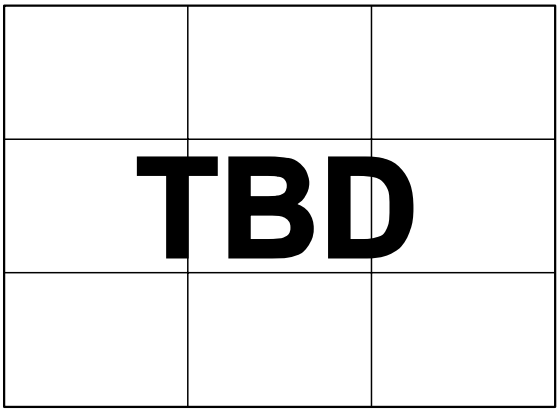

Figure 8.

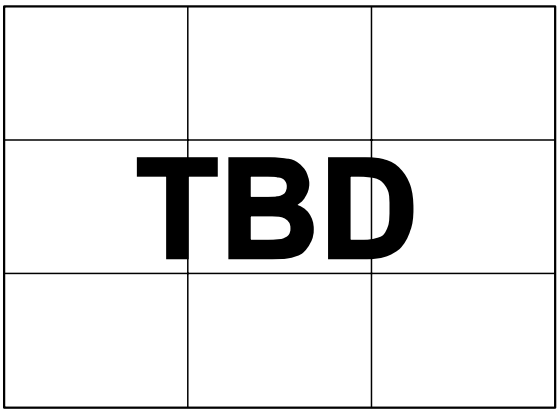

Figure 6.

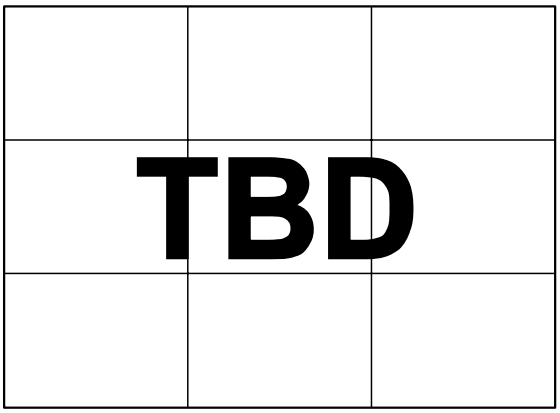

Figure 9.

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ARCHITECTURE AND MAIN FEATURES

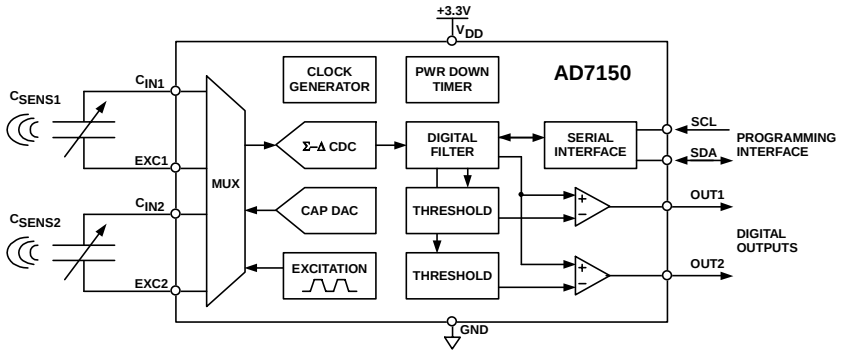

Figure 10. AD7150 Block Diagram

OVERVIEW

The AD7150 core is a high performance capacitance to digital converter (CDC), which allows the part to be interfaced directly to a capacitive sensor.

The comparators compare the CDC result with thresholds, either fixed or dynamically adjusted by the on-chip adaptive threshold algorithm engine. Thus, the outputs indicate a defined change in the input sensor capacitance.

The AD7150 also integrates an excitation source and CAPDAC for the capacitive inputs, an input multiplexer, a complete clock generator, a power down timer, control logic, and an I2C-compatible serial interface for configuring the part and accessing the internal CDC data, status, etc., if required in the system. See Figure 10.

CAPACITANCE TO DIGITAL CONVERTER

Figure 11 shows the CDC simplified functional diagram. The converter consists of a second order Σ-Δ (or charge balancing) modulator and a third order digital filter. The measured capacitance C_X is connected between an excitation source and the Σ-Δ modulator input. The excitation signal is applied on the C_X during the conversion and the modulator continuously samples the charge going through the C_X. The digital filter processes the modulator output, which is a stream of 0s and 1s containing the information in 0 and 1 density. The data are processed by the adaptive threshold engine and output comparators; the data can be also read through the serial interface.

The AD7150 is designed for floating capacitive sensors. Therefore, both C_X plates have to be isolated from ground or any other fixed potential node in the system.

The AD7150 features slew rate limiting on the excitation voltage output, which decrease the energy of higher harmonics on the excitation signal and dramatically improves the system EMC radiation performance.

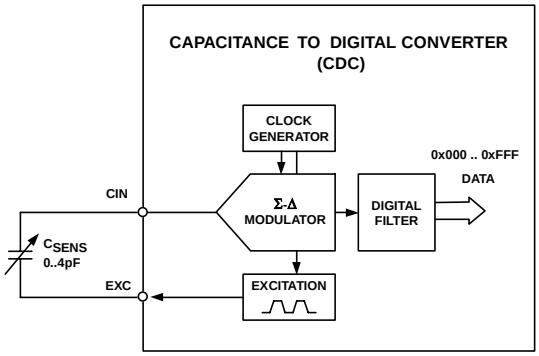

Figure 11. CDC Simplified Block Diagram

CAPDAC

The AD7150 CDC core maximum full-scale input range is 4 pF. However, the part can accept a higher capacitance on the input and the offset (not-changing component) capacitance up to 10 pF can be balanced by a programmable on-chip CAPDAC.

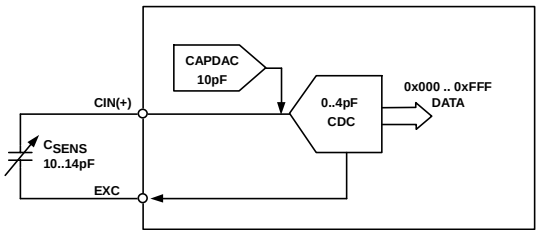

Figure 12. Using CAPDAC

The CAPDAC can be understood as a negative capacitance connected internally to the CIN pin. The CAPDAC has a 6-bit resolution and a monotonic transfer function. The example in Figure 12 shows how to use the CAPDAC to shift the CDC 4 pF input range to measure capacitance between 10 pF to 14 pF.

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COMPARATOR AND THRESHOLD MODES

The AD7150 comparators and their thresholds can be programmed to operate in several different modes. In an adaptive mode, the threshold is dynamically adjusted and the comparator output will indicate fast changes and ignore slow changes in the input (sensor) capacitance Alternatively, the threshold can be programmed a constant (fixed) value and the output will indicate all changes in the input capacitance.

The AD7150 logic output (active high) indicates either positive or negative change in the input capacitance, in both adaptive and fixed threshold modes; see Figure 13 and Figure 14.

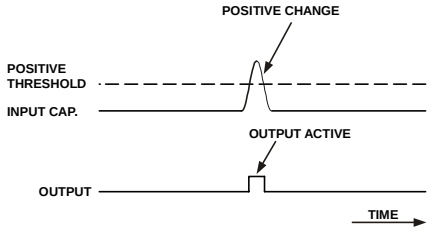

Figure 13. Positive Threshold Mode
Indicates positive change in input capacitance

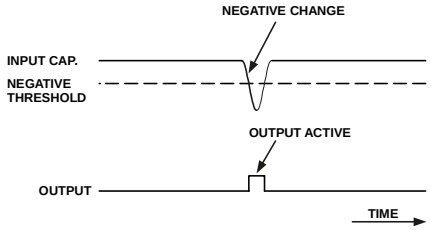

Figure 14. Negative Threshold Mode
Indicates negative change in input capacitance

Additionally, for the adaptive mode only, the comparators can work as "window" comparators, indicating input either inside or outside selected sensitivity band; see Figure 15 and Figure 16.

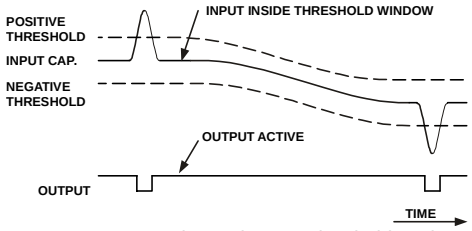

Figure 15. In-Window (Adaptive) Threshold Mode

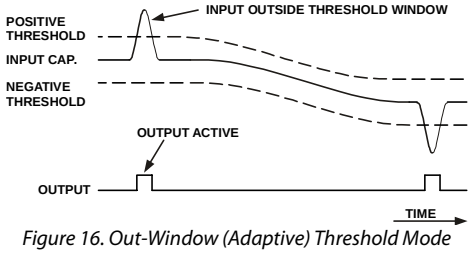

Figure 16. Out-Window (Adaptive) Threshold Mode

ADAPTIVE THRESHOLD

In an adaptive mode, the threshold(s) are dynamically adjusted, ensuring indication of fast changes (for example an object moving close to a capacitive proximity sensor) and eliminating slow changes in the sensor capacitance (usually caused by environment changes – e.g. humidity or temperature - or changes in the sensor dielectric material over time.). See Figure 17.

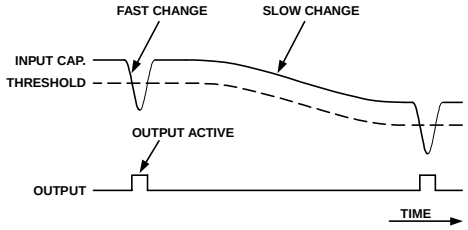

Figure 17. Adaptive Threshold
Indicates fast changes and eliminates slow changes in input capacitance

DATA AVERAGE

The adaptive threshold algorithm is based on an average calculated from previous CDC output data. The response of the average to an input capacitance step change (more exactly, response to the change in the CDC output data) is an exponential settling curve, which can be characterized by equation:

$$Average(N) = Average(0) + Change(1 - e^{N / TimeConst})$$

Where Average(N) is the value of average N complete CDC conversion cycles after a step change on the input, Average(0) is the value before the step change, and the TimeConstant can be selected in range between 2 and 65536 in steps of power of 2 by programming the ThrSettling bits in the setup registers. See Figure 18. See Register Descriptions.

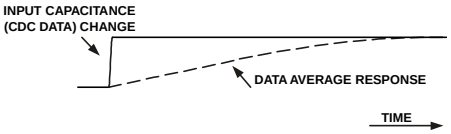

Figure 18 .Data Average Response to Data Step Change

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SENSITIVITY

In adaptive threshold mode, the output comparator threshold is set as a defined distance ("sensitivity") above the data average, below the data average, or both, depending on the selected threshold mode of operation – see Figure 19. The sensitivity value is programmable in range of 0 to 255 LSBs of the 12-bit CDC converter. See Register Descriptions.

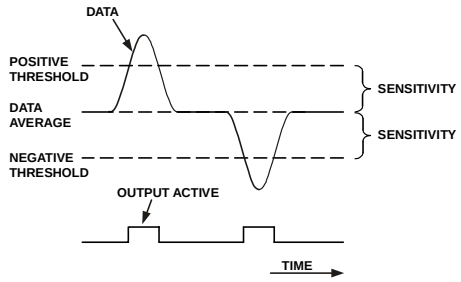

Figure 19. Threshold Sensitivity

HYSTERESIS

In adaptive threshold mode, the comparator features hysteresis. The hysteresis is fixed to ¼ of the threshold sensitivity and can be programmable ON or OFF. The comparator does not have any hysteresis in the fixed threshold mode.

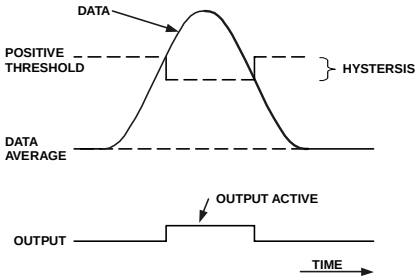

Figure 20. Threshold Hysteresis

TIMEOUT

In case of a large long change in the capacitive input, when the data average adapting to a new condition might take too long, a timeout can be set.

The timeout becomes active (counting) when the CDC data goes outside the band of data average ± sensitivity. When the timeout elapses (a defined number of CDC conversions is counted), the data average, and thus the thresholds, are forced to follow the new CDC data value immediately. See Figure 21.

The timeout can be set independently for "approaching" – for change in data towards the threshold, and for "receding" – for change in data away from the threshold. See Figure 22 and Figure 23. See Register Descriptions.

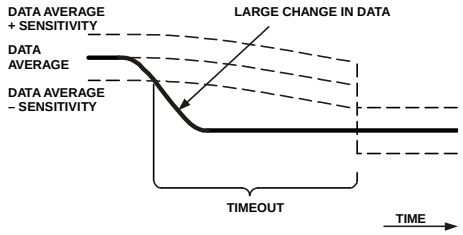

Figure 21. Threshold Timeout after a Large Change in CDC Data

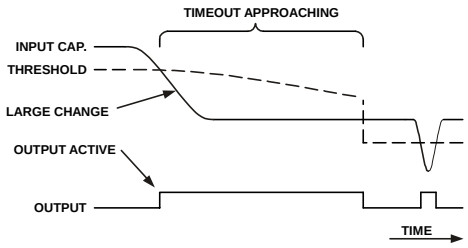

Figure 22. Approaching Timeout in Negative Threshold Mode Shortens False Output Trigger

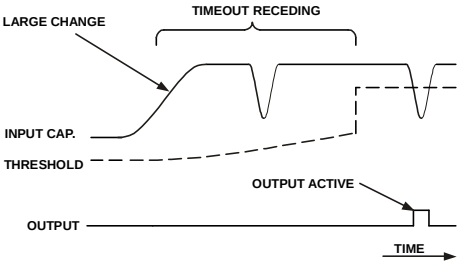

Figure 23. Positive Timeout in Negative Threshold Mode Shortens Period of Missing Output Trigger

AUTO CAPDAC ADJUSTMENT

In adaptive threshold mode, the part can dynamically adjust the CAPDAC to keep the CDC in an optimal operating capacitive range. When the AutoDAC function is enabled, the CAPDAC value is automatically incremented when the data average exceeds ¾ of the CDC full range, and the CAPDAC value is decremented when the data average goes below ¼ or the CDC full range. The AutoDAC increment or decrement step depends on the selected CDC capacitive input range. See Register Descriptions.

POWER DOWN TIMER

In power sensitive applications, the AD7150 can be set to automatically enter power down mode after a programmed period of time, in which the outputs have not been activated. The AD7150 can be then returned to a normal operational mode either via the serial interface or by power supply off – on sequence.

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REGISTER DESCRIPTIONS

Table 5. Register Summary

	Pointer			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Register	**(Dec)**	**(Hex)**	**Dir**	**Default Value**							
Status	0	0x00	R	PwrDown	$\overline{\text{DacStep2}}$	OUT2	$\overline{\text{DacStep1}}$	OUT1	C1/C2	$\overline{\text{RDY2}}$	$\overline{\text{RDY1}}$
				0	1	0	1	0	0	1	1
Ch1 Data H	1	0x01	R	Channel 1 Data – high byte, 0x00							
Ch1 Data L	2	0x02	R	Channel 1 Data – low byte, 0x00							
Ch2 Data H	3	0x03	R	Channel 2 Data – high byte, 0x00							
Ch2 Data L	4	0x04	R	Channel 2 Data – low byte, 0x00							
Ch1 Average H	5	0x05	R	Channel 1 Average – high byte, 0x00							
Ch1 Average L	6	0x06	R	Channel 1 Average – low byte, 0x00							
Ch2 Average H	7	0x07	R	Channel 2 Average – high byte, 0x00							
Ch2 Average L	8	0x08	R	Channel 2 Average – low byte, 0x00							
Ch1 Sens / Thr H	9	0x09	R/W	Channel 1 Sensitivity (adaptive) / Threshold – high byte (fixed), 0x08							
Ch1Tout / Thr L	10	0x0A	R/W	Channel 1 Timeout (adaptive) / Threshold – low byte (fixed), 0x86							
Ch1 Setup	11	0x0B	R/W	RngH1	RngL1	-	$\overline{\text{Hyst1}}$	ThrSettling1 – 4-Bit Value			
				0	0	0	0	0x0B			
Ch2 Sens / Thr H	12	0x0C	R/W	Channel 2 Sensitivity (adaptive) / Threshold (fixed) – high byte, 0x08							
Ch2 Tout / Thr L	13	0x0D	R/W	Channel 2 Timeout (adaptive) / Threshold (fixed) – low byte, 0x86							
Ch2 Setup	14	0x0E	R/W	RngH2	RngL2	-	$\overline{\text{Hyst2}}$	ThrSettling2 – 4-Bit Value			
				0	0	0	0	0x0B			
Configuration	15	0x0F	R/W	ThrFixed	ThrMD1	ThrMD0	EnCh1	EnCh2	MD2	MD1	MD0
				0	0	0	1	1	0	0	1
Power Down Timer	16	0x10	R/W	–	–	Power Down Timeout – 6-Bit Value					
				0	0	0x00					
Ch1 CAPDAC	17	0x11	R/W	DacEn1	DacAuto1	Channel 1 CAPDAC – 6-Bit Value					
				0	0	0x00					
Ch2 CAPDAC	18	0x12	R/W	DacEn2	DacAuto2	Channel 2 CAPDAC – 6-Bit Value					
				0	0	0x00					
Serial Number 3	19	0x13	R	Serial Number – byte 3 (MSB)							
Serial Number 2	20	0x14	R	Serial Number – byte 2							
Serial Number 1	21	0x15	R	Serial Number – byte 1							
Serial Number 0	22	0x16	R	Serial Number – byte 0 (LSB)							
Chip ID	23	0x17	R	Chip Identification Code							

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STATUS REGISTER

Address Pointer 0x00
8 Bits, Read Only, Default Value 0x53

This register indicates the status of the part. The register can be read via the 2-wire serial interface to query status of the outputs, check the CDC finished conversion and whether the CAPDAC has been changed by the auto CAPDAC function.

Table 6. Status Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	PwrDown	$\overline{\text{DacStep2}}$	OUT2	$\overline{\text{DacStep1}}$	OUT1	C1/C2	$\overline{\text{RDY2}}$	$\overline{\text{RDY1}}$
Default	0	1	0	1	0	0	1	1

Table 7.

Bit	Mnemonic	Description
7	PwrDown	PwrDown = 1 indicates that the part is in a power down mode.
6	$\overline{\text{DacStep2}}$	$\overline{\text{DacStep2}}$ = 0 indicates that the CAPDAC Ch2 was changed after the last CDC conversion as part of the AutoDac function The bit value is updated after each finished CDC conversion on this channel.
5	OUT2	OUT2 = 1 indicates that the Ch2 data (CIN2 capacitance) crossed the threshold, according to the selected comparator mode of operation. The bit value is updated after each finished CDC conversion on this channel.
4	$\overline{\text{DacStep1}}$	$\overline{\text{DacStep1}}$ = 0 indicates that the CAPDAC Ch2 was changed during the last conversion as part of the AutoDac function The bit value is updated after each finished CDC conversion on this channel.
3	OUT1	OUT1 = 1 indicates that the Ch1 data (CIN1 capacitance) crossed the threshold, according to the selected comparator mode of operation. The bit value is updated after each finished CDC conversion on this channel.
2	C1/C2	The C1/C2 = 0 indicates the last finished CDC conversion was on channel 1, The C1/C2 = 1 indicates the last finished CDC conversion was on channel 2
1	$\overline{\text{RDY2}}$	$\overline{\text{RDY2}}$ = 0 indicates finished CDC conversion on Ch2. The bit is reset back to 1 when the Ch2 data register is read via serial interface or after the part reset or power-up.
0	$\overline{\text{RDY1}}$	$\overline{\text{RDY1}}$= 0 indicates finished CDC conversion on Ch1. The bit is reset back to 1 when the Ch1 data register is read via serial interface or after the part reset or power-up.

DATA REGISTERS

Ch1 Address Pointer 0x01, 0x02
Ch2 Address Pointer 0x03,0x04
16 Bits, Read-Only, Default Value 0x0000

CDC output data. The AD7150 has a 12-bit converter, the 12-bit result is mapped to the 12 MSB (most significant bits) of the 16-bit data register and the 4 LSB (least significant bits) are always 0.

The register is updated after a finished conversion on the capacitive channel, with one exception: When the serial interface read operation from the data register is in progress, the data register is not updated and the new capacitance conversion result is lost.

The stop condition on the serial interface is considered to be the end of the read operation. Therefore, to prevent incorrect data reading through the serial interface, the two bytes of the data register should be read sequentially using the register address pointer auto-increment feature of the serial interface.

AVERAGE REGISTERS

Ch1 Address Pointer 0x05, 0x06
Ch2 Address Pointer 0x07,0x08
16 Bits, Read-Only, Default Value 0x0000

Average calculated from the previous CDC data. The 12-bit CDC result corresponds to the 12 MSB of the average register.

The settling time of the average can be set by programming the ThrSettling bits in the setup register. The average register is overwritten directly with the CDC output data, i.e., the history is forgotten, if the timeout is enabled and elapses.

FIXED THRESHOLD REGISTERS

Ch1 Address Pointer 0x09, 0x0A
Ch2 Address Pointer 0x0C,0x0D
16 Bits, Read/Write, Factory Preset 0x0886

Set a constant threshold for the output comparator in the fixed threshold mode. The 12-bit CDC result corresponds to the 12 MSB of the threshold register. The threshold registers are not accessible in the adaptive threshold mode.

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SENSITIVITY REGISTERS

Ch1 Address Pointer 0x09
Ch2 Address Pointer 0x0C
8 Bits, Read/Write, Factory Preset 0x08

Sensitivity register sets the distance of the positive threshold above the data average, and the distance of the negative threshold below the data average, in the adaptive threshold mode.

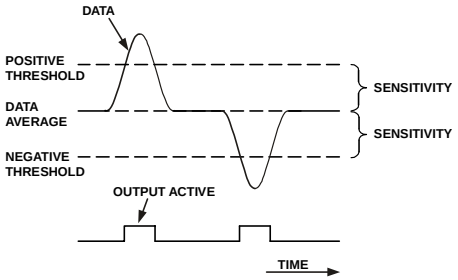

Figure 24. Threshold Sensitivity

The sensitivity is an 8-bit value and is mapped to the lower 8 bits of the 12-bit CDC data, i.e., corresponds to the 16-bit data register as shown in Figure 39.

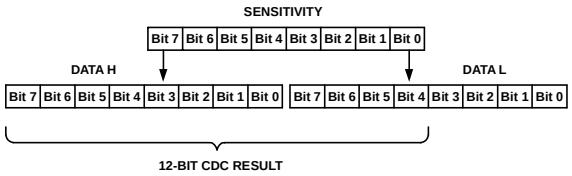

Figure 25. Threshold Timeout after a Large Negative Change in CDC Data

TIMEOUT REGISTERS

Ch1 Address Pointer 0x0A
Ch2 Address Pointer 0x0D
8 Bits, Read/Write, Factory Preset 0x86

Table 8. Timeout Register Bit Map

Bit	Bit 7-4	Bit 3-0
Mnemonic	TimeOutApr	TimeOutRec
Default	0x08	0x06

The registers set timeouts for the adaptive threshold mode.

The approaching timeout starts when the CDC data cross the data average±sensitivity band in direction towards the threshold, according to the selected positive, negative or window threshold mode. The approaching timeout elapses after $2^{\text{TimeOutApr}}$ conversion cycles.

The receding timeout starts when the CDC data cross the data average±sensitivity band in direction away from the threshold, according to the selected positive or negative threshold mode. The receding timeout is not used in the window threshold modes. The receding timeout elapses after $2^{\text{TimeOutRec}}$ conversion cycles.

When either approaching or receding timeout elapses (i.e., after the defined number of CDC conversions is counted), the data average, and thus the thresholds, are forced to follow the new CDC data value immediately.

Timeout register = 0 disables both timeouts

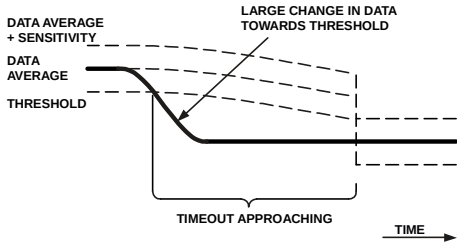

Figure 26. Threshold Timeout Approaching after a Large Change in CDC Data towards Threshold

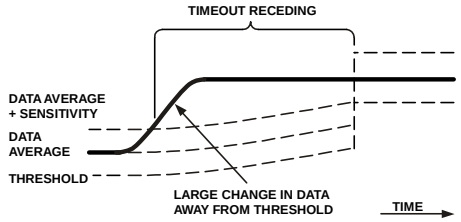

Figure 27. Threshold Timeout Receding after a Large Change in CDC Data away from Threshold

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SETUP REGISTERS

Ch1 Address Pointer 0x0B
Ch2 Address Pointer 0x0E
8 Bits, Read/Write, Factory Preset 0x0B

Table 9. Setup Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	RngH	RngL	-	$\overline{\text{Hyst}}$	ThrSettling1 – 4-Bit Value			
Default	0	0	0	0	0x0B			

Table 10.

Bit	Mnemonic	Description
7 6	RngH RngL	Range bits set the CDC input range. Also determine step for AutoDAC function RngH / RngL / Cin Range (pF) / AutoDAC Step (CAPDAC LSB) 0 / 0 / 2 / 4 0 / 1 / 0.5 / 1 1 / 0 / 1 / 2 1 / 1 / 4 / 8
5	-	This bit must be 0 for proper operation.
4	$\overline{\text{Hyst}}$	$\overline{\text{Hyst}}$ = 1 disables hysteresis in adaptive threshold mode. Bit has no effect in fixed threshold mode - hysteresis is always disabled in the fixed threshold mode.
3 2 1 0	ThrSettling	Determines the settling time constant of the data average, and thus the settling time of the adaptive thresholds. The response of the average to an input capacitance step change (more exact, response to the change in the CDC output data) is an exponential settling curve, characterized by equation: $Average(N) = Average(0) + Change(1 - e^{N / TimeConst})$ Where Average(N) is the value of average after N complete CDC conversion cycles after a step change on the input, Average(0) is the value before the step change, and the TimeConstant can be selected in range between 2 and 65536 conversion cycle multiples, in steps of power of 2, by programming the ThrSettling bits: $TimeConst = 2^{(ThrSettling+1)}$

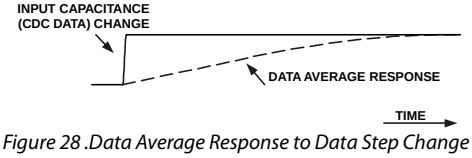

Figure 28 .Data Average Response to Data Step Change

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CONFIGURATION REGISTER

Address Pointer 0x0F

8 Bits, Read/Write, Factory Preset 0x19

Table 11. Configuration Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	ThrFixed	ThrMD1	ThrMD0	EnCh1	EnCh2	MD2	MD1	MD0
Default	0	0	0	1	1	0	0	1

Table 12.

<table>
<tr><th>Bit</th><th>Mnemonic</th><th>Description</th></tr>
<tr><td>7</td><td>ThrFixed</td><td>ThrFixed = 1 sets the fixed threshold mode. The outputs reflect comparison of data and a fixed (constant) value of the threshold registers.
ThrFixed = 0 sets the adaptive threshold mode. The outputs reflect comparison of data to the adaptive thresholds, which is set dynamically based on the previous data and according to the other settings.</td></tr>
<tr><td>6
5</td><td>ThrMD1
ThrMD0</td><td>These bits set the output comparators mode.
<table>
<tr><th rowspan="2">ThrMD1</th><th rowspan="2">ThrMD0</th><th rowspan="2">Threshold Mode</th><th colspan="2">OUTPUT ACTIVE WHEN</th></tr>
<tr><th>Adaptive Threshold Mode</th><th>Fixed Threshold Mode</th></tr>
<tr><td>0</td><td>0</td><td>Negative</td><td>data < average – sensitivity</td><td>Data < Threshold</td></tr>
<tr><td>0</td><td>1</td><td>Positive</td><td>data > average + sensitivity</td><td>Data > Threshold</td></tr>
<tr><td>1</td><td>0</td><td>In-Window</td><td>data > average – sensitivity
AND
data < average + sensitivity</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>Out-Window</td><td>data < average – sensitivity
OR
data > average + sensitivity</td><td>-</td></tr>
</table></td></tr>
<tr><td>4</td><td>EnCh1</td><td>Enables conversion on channel 1</td></tr>
<tr><td>3</td><td>EnCh2</td><td>Enables conversion on channel 2</td></tr>
<tr><td>2
1
0</td><td>MD2
MD1
MD0</td><td>Converter mode of operation setup.
<table>
<tr><th>MD2</th><th>MD1</th><th>MD0</th><th>Mode</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Idle</td><td>Part is fully powered up, but performing no conversion</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Cont. conversion</td><td>Part is repeatedly performing conversions on the enabled channel(s). If two channels are enabled, part is sequentially switching between them.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Single conversion</td><td>Part performs a single conversion on the enabled channel. If two channels are enabled, the part will perform two conversions, one on each channel. After finishing the conversion(s), the part goes to the idle mode.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Power-Down</td><td>Powers down the on-chip circuits, except the digital interface.</td></tr>
<tr><td>1</td><td>X</td><td>X</td><td>Reserved</td><td>Do not use these modes.</td></tr>
</table></td></tr>
</table>

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POWER DOWN TIMER REGISTER

Address Pointer 0x10
8 Bits, Read/Write, Factory Preset 0x00

Table 13. Setup Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	–	–	Power Down Timeout – 6-Bit Value					
Default	0	0	0xPP					

Table 14.

Bit	Mnemonic	Description
7-6	-	These bits must be 0 for proper operation
5-0	Power Down Timeout	Defines period duration of the power down timeout. If the output comparator outputs have not been activated during the programmed period, the part enters automatically power down mode. The part can be then returned to a normal operational mode either via the serial interface or by power supply off – on sequence. The period is programmable in steps of 4 hours. For example, setting value to 0x06 sets the duration to 24 hours, the maximum value of 0x3F corresponds to approximately 10.5 days. Value of 0x00 disables the power down timeout and the part will not enter power down mode automatically.

CAP DAC B REGISTERS

Ch1 Address Pointer 0x11
Ch2 Address Pointer 0x12
8 Bits, Read/Write, Factory Preset 0x00

Table 15. Setup Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	DacEn	DacAuto1	Channel 1 CAPDAC – 6-Bit Value					
Default	P	P	0xPP					

Table 16.

Bit	Mnemonic	Description
7	DacEn	DacEn = 1 enables capacitive DAC
6	DacAuto	DacAuto = 1 enables the AutoDAC function in the adaptive threshold mode. When the AutoDAC function is enabled, the part dynamically adjust the CAPDAC to keep the CDC in an optimal operating capacitive range. The CAPDAC value is automatically incremented when the data average exceeds ¾ of the CDC full range, and the CAPDAC value is decremented when the data average goes below ¼ or the CDC full range. The AutoDAC increment or decrement step depends on the selected CDC capacitive input range. Bit has no effect in fixed threshold mode - AutoDAC function is always disabled in the fixed threshold mode.
5-0	CAPDAC	CAPDAC value, Code 0x00 ≈ 0 pF, Code 0x3F ≈ CAPDAC full range.

SERIAL NUMBER REGISTERS

Address Pointer 0x13, 0x14, 0x15, 0x16
32 Bits, Read Only, 0xXXXX

Register holds a serial number, unique for each individual part.

CHIP ID REGISTERS

Address Pointer 0x17
8 Bits, Read Only, 0xXX

Chip identification code, used in factory manufacturing and test.

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SERIAL INTERFACE

The AD7150 supports an I²C-compatible 2-wire serial interface. The two wires on the I²C bus are called SCL (clock) and SDA (data). These two wires carry all addressing, control, and data information one bit at a time over the bus to all connected peripheral devices. The SDA wire carries the data, while the SCL wire synchronizes the sender and receiver during the data transfer. I²C devices are classified as either master or slave devices. A device that initiates a data transfer message is called a master, while a device that responds to this message is called a slave.

To control the AD7150 device on the bus, the following protocol must be followed. First, the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that the start byte follows. This 8-bit start byte is made up of a 7-bit address plus an R/W bit indicator.

All peripherals connected to the bus respond to the start condition and shift in the next 8 bits (7-bit address + R/W bit). The bits arrive MSB first. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as the acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. An exception to this is the general call address, which is described later in this document. The idle condition is where the device monitors the SDA and SCL lines waiting for the start condition and the correct address byte. The R/W bit determines the direction of the data transfer. A Logic 0 LSB in the start byte means that the master writes information to the addressed peripheral. In this case the AD7150 becomes a slave receiver. A Logic 1 LSB in the start byte means that the master reads information from the addressed peripheral. In this case, the AD7150 becomes a slave transmitter. In all instances, the AD7150 acts as a standard slave device on the I²C bus.

The start byte address for the AD7150 is 0x90 for a write and 0x91 for a read.

READ OPERATION

When a read is selected in the start byte, the register that is currently addressed by the address pointer is transmitted on to the SDA line by the AD7150. This is then clocked out by the master device and the AD7150 awaits an acknowledge from the master.

If an acknowledge is received from the master, the address auto-incrementer automatically increments the address pointer register and outputs the next addressed register content on to the SDA line for transmission to the master. If no acknowledge is received, the AD7150 return to the idle state and the address pointer is not incremented. The address pointers' auto-incrementer allow block data to be written or read from the starting address and subsequent incremental addresses.

In continuous conversion mode, the address pointers' auto-incrementer should be used for reading a conversion result. That means, the three data bytes should be read using one multibyte read transaction rather than three separate single byte transactions. The single byte data read transaction may result in the data bytes from two different results being mixed. The same applies for six data bytes if both the capacitive and the voltage/temperature channel are enabled.

The user can also access any unique register (address) on a one-to-one basis without having to update all the registers. The address pointer register contents cannot be read.

If an incorrect address pointer location is accessed or, if the user allows the auto-incrementer to exceed the required register address, the following applies:

- In read mode, the AD7150 continues to output various internal register contents until the master device issues a no acknowledge, start, or stop condition. The address pointers' auto-incrementer's contents are reset to point to the status register at address 0x00 when a stop condition is received at the end of a read operation. This allows the status register to be read (polled) continually without having to constantly write to the address pointer.
- In write mode, the data for the invalid address is not loaded into the AD7150 registers but an acknowledge is issued by the AD7150.

WRITE OPERATION

When a write is selected, the byte following the start byte is always the register address pointer (subaddress) byte, which points to one of the internal registers on the AD7150. The address pointer byte is automatically loaded into the address pointer register and acknowledged by the AD7150. After the address pointer byte acknowledge, a stop condition, a repeated start condition, or another data byte can follow from the master. A stop condition is defined by a low-to-high transition on SDA while SCL remains high. If a stop condition is ever encountered by the AD7150, it returns to its idle condition and the address pointer is reset to address 0x00.

If a data byte is transmitted after the register address pointer byte, the AD7150 load this byte into the register that is currently addressed by the address pointer register, send an acknowledge, and the address pointer auto-incrementer automatically increments the address pointer register to the next internal register address. Thus, subsequent transmitted data bytes are loaded into sequentially incremented addresses.

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If a repeated start condition is encountered after the address pointer byte, all peripherals connected to the bus respond exactly as outlined above for a start condition, that is, a repeated start condition is treated the same as a start condition. When a master device issues a stop condition, it relinquishes control of the bus, allowing another master device to take control of the bus. Hence, a master wanting to retain control of the bus issues successive start conditions known as repeated start conditions.

AD7150 RESET

To reset the AD7150 without having to reset the entire I²C bus, an explicit reset command is provided. This uses a particular address pointer word as a command word to reset the part and upload all default settings. The AD7150 do not respond to the I²C bus commands (do not acknowledge) during the default values upload for approximately TBD µs.

The reset command address word is 0xBF.

GENERAL CALL

When a master issues a slave address consisting of seven 0s with the eighth bit (R/W bit) set to 0, this is known as the general call address. The general call address is for addressing every device connected to the I²C bus. The AD7150 acknowledge this address and read in the following data byte.

If the second byte is 0x06, the AD7150 are reset, completely uploading all default values. The AD7150 do not respond to the I²C bus commands (do not acknowledge) during the default values upload for approximately TBD µs.

The AD7150 do not acknowledge any other general call commands.

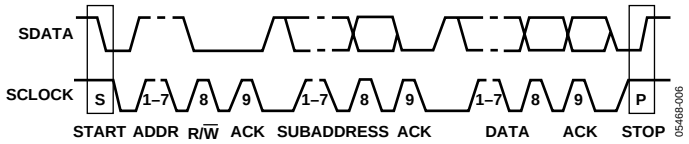

Figure 29. Bus Data Transfer

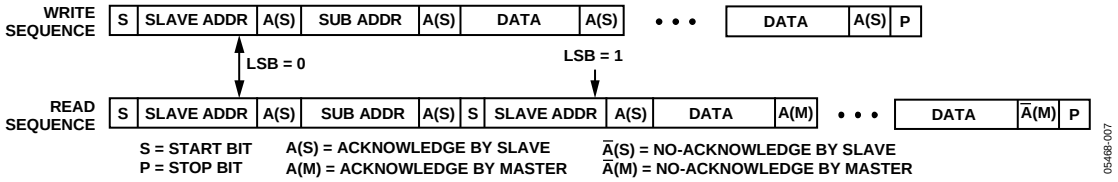

Figure 30. Write and Read Sequences

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HARDWARE DESIGN CONSIDERATIONS

OVERVIEW

The AD7150 is an interface to capacitive sensors.

On the input side, the sensor (C_X) can be connected directly between the AD7150 EXC and the C_{IN} pins. The way how is it connected and the electrical parameters of the sensor connection, such as parasitic resistance or capacitance, can affect the system performance. Therefore, any circuit with additional components in the capacitive front end, such as overvoltage protection, has to be carefully designed considering the AD7150 specified limits and information provided in this section.

On the output side, the AD7150 can work as a standalone device, using the power-up default register settings and flagging the result on digital outputs. Alternatively, the AD7150 can be interfaced to a microcontroller via the 2-wire serial interface, offering flexibility by overwriting the AD7150 register values from the host with a user specific setup.

PARASITIC CAPACITANCE TO GROUND

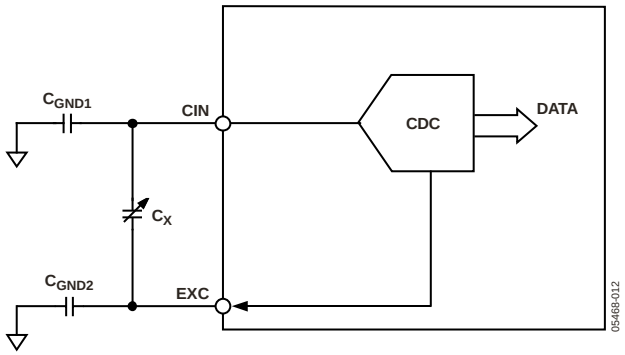

Figure 31. Parasitic Capacitance to Ground

The CDC architecture used in the AD7150 measures the capacitance C_X connected between the EXC pin and the C_{IN} pin. In theory, any capacitance C_{GND} to ground should not affect the CDC result (see Figure 31).

The practical implementation of the circuitry in the chip implies certain limits and the result is gradually affected by capacitance to ground. See the allowed capacitance to GND in the specification table for C_{IN} and excitation.

Further details will be specified after the AD7150 characterization.

PARASITIC RESISTANCE TO GROUND

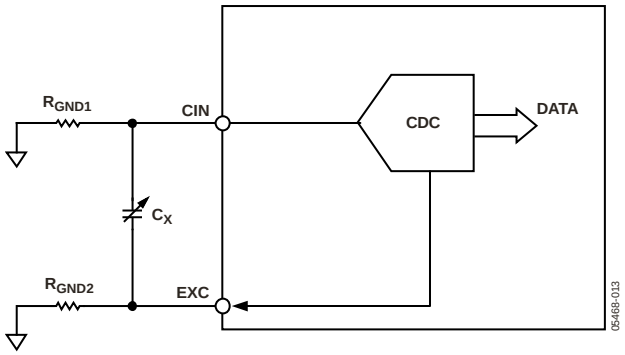

Figure 32. Parasitic Resistance to Ground

The AD7150 CDC result would be affected by a leakage current from the C_X to ground, therefore the C_X should be isolated from the ground. (The equivalent resistance between the C_X and ground should be maximized – see Figure 32).

The limit will be specified after the AD7150 characterization.

PARASITIC PARALLEL RESISTANCE

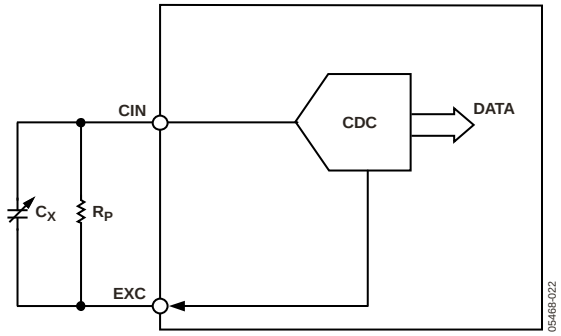

Figure 33. Parasitic Parallel Resistance

The AD7150 CDC measures the charge transfer between EXC pin and C_{IN} pin. Any resistance connected in parallel to the measured capacitance C_X (see Figure 33), such as the parasitic resistance of the sensor, also transfers charge. Therefore, the parallel resistor is seen as an additional capacitance in the output data. The equivalent parallel capacitance (or error caused by the parallel resistance) can be approximately calculated as

$$C_P = \frac{1}{R_P \times F_{EXC} \times 4}$$

Where R_P is the parallel resistance and F_{EXC} is the excitation frequency.

Further details will be specified after the AD7150 characterization.

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PARASITIC SERIAL RESISTANCE

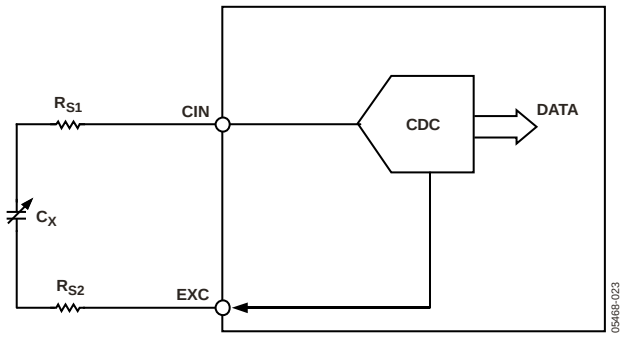

Figure 34. Parasitic Serial Resistance

The AD7150 CDC result is affected by a resistance in series with the measured capacitance. The total serial resistance, which refers to R_{S1} + R_{S2} on Figure 34, should be in order of hundreds Ω.

Further details will be specified after the AD7150 characterization.

INPUT OVERVOLTAGE PROTECTION

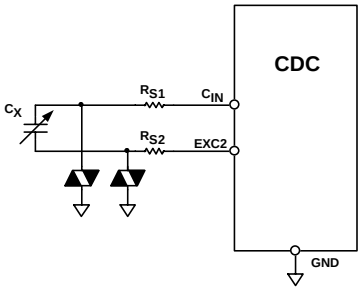

Figure 35. AD7150 C_{IN} Overvoltage Protection

The AD7150 capacitive input has an internal ESD protection. However, some applications may require an additional overvoltage protection depending on the application specific requirements. Any additional circuit in the capacitive front end has to be carefully designed, especially with respect to the limits recommended for max. capacitance to ground, max. serial resistance, max. leakage, etc.

Further details will be specified after the AD7150 characterization.

INPUT EMC PROTECTION

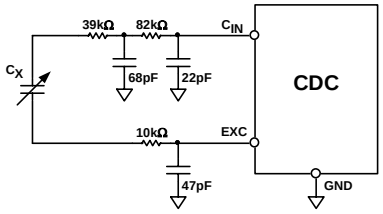

Figure 36. AD7150 C_{IN} EMC Protection

Some applications may have specific requirements for EMC protection. Figure 36 shows one of the possible input circuit configurations improving the system EMC robustness.

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APPLICATION EXAMPLES

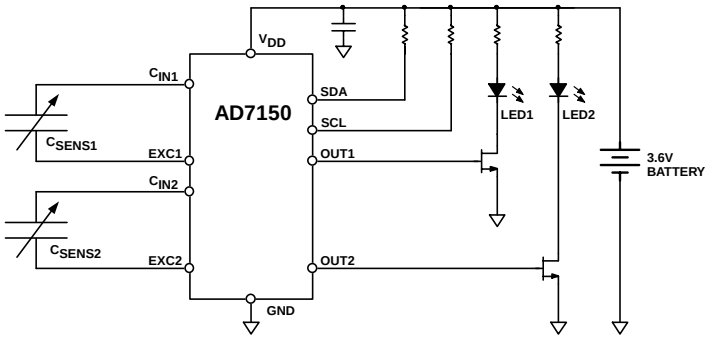

Figure 37. AD7150 Standalone Operation Application Diagram

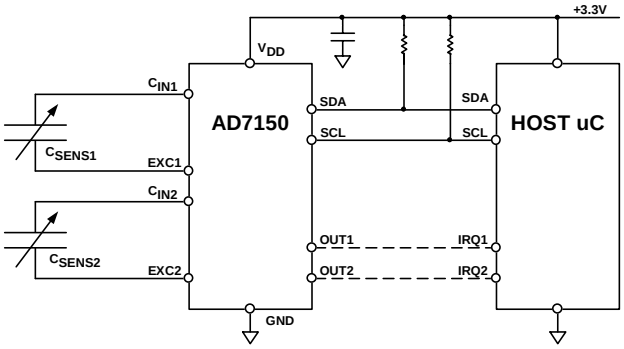

Figure 38. AD7150 Interfaced to a Host Microcontroller

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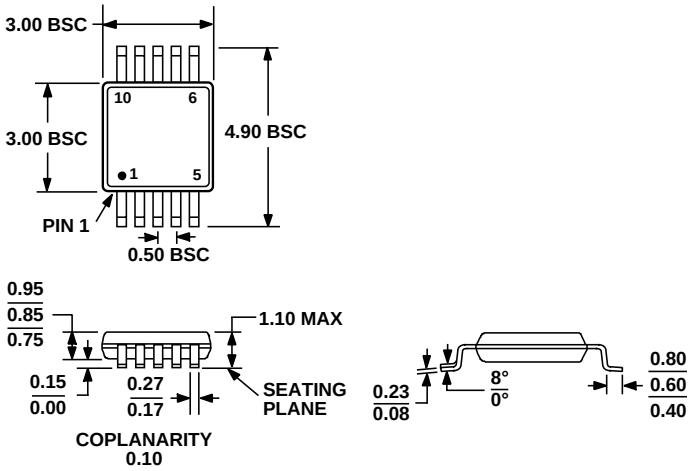

Figure 39. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

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