



# Programmable Controller for Capacitance Touch Sensors

## AD7143

### FEATURES

- Programmable capacitance-to-digital converter
  - 25 ms update rate (@ maximum sequence length)
  - Better than 1 fF resolution
  - 8 capacitance sensor input channels
  - No external RC tuning components required
- Automatic conversion sequencer
- On-chip automatic calibration logic
  - Automatic compensation for environmental changes
  - Automatic adaptive threshold and sensitivity levels
- On-chip RAM to store calibration data
- I<sup>2</sup>C<sup>®</sup>-compatible serial interface
- Separate VDRIVE level for serial interface
- Interrupt output for host controller
- 16-lead, 4 mm x 4 mm LFCSP-VQ
- 2.6 V to 3.6 V supply voltage
- Low operating current
  - Full power mode: less than 1 mA
  - Low power mode: 50  $\mu$ A

### APPLICATIONS

- Personal music and multimedia players
- Cell phones
- Digital still cameras
- Smart hand-held devices
- Television, A/V, and remote controls
- Gaming consoles

### GENERAL DESCRIPTION

The AD7143 is an integrated capacitance-to-digital converter (CDC) with on-chip environmental calibration for use in systems requiring a novel user input method. The AD7143 interfaces to external capacitance sensors implementing functions, such as capacitive buttons, scroll bars, and scroll wheels.

The CDC has eight inputs channeled through a switch matrix to a 16-bit, 250 kHz sigma-delta ( $\Sigma$ - $\Delta$ ) capacitance-to-digital converter. The CDC is capable of sensing changes in the capacitance of the external sensors and uses this information to register a sensor activation. The external sensors can be arranged as a series of buttons, as a scroll bar or wheel, or as a combination of sensor types. By programming the registers, the user has full control over the CDC setup. High resolution sensors require software to run on the host processor.

### FUNCTIONAL BLOCK DIAGRAM

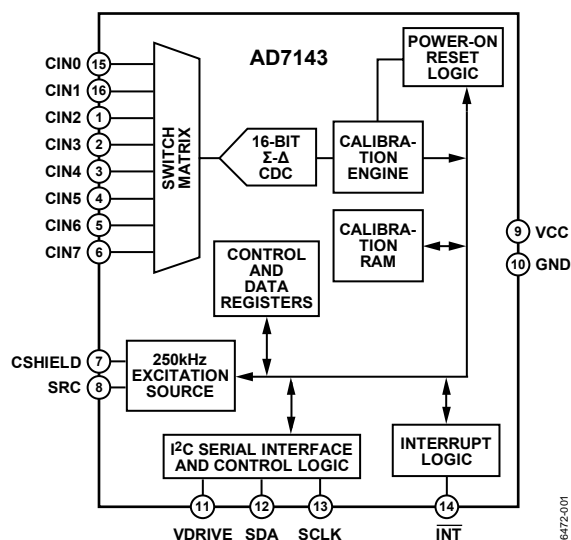


Figure 1.

The AD7143 has on-chip calibration logic to account for changes in the ambient environment. The calibration sequence is performed automatically and at continuous intervals, while the sensors are not touched. This ensures that there are no false or nonregistering touches on the external sensors due to a changing environment.

The AD7143 has an I<sup>2</sup>C-compatible serial interface and a separate VDRIVE pin for I<sup>2</sup>C serial interface operating voltages between 1.65 V and 3.6 V.

The AD7143 is available in a 16-lead, 4 mm x 4 mm LFCSP-VQ and operates from a 2.6 V to 3.6 V supply. The operating current consumption is less than 1 mA, falling to 50  $\mu$ A in low power mode (conversion interval of 400 ms).

Rev. 0

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## REVISION HISTORY

1/07—Revision 0: Initial Version

## SPECIFICATIONS

$V_{CC} = 2.6 \text{ V to } 3.6 \text{ V}$ ,  $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ , unless otherwise noted.

Table 1.

| Parameter                                   | Min                           | Typ                | Max             | Unit          | Test Conditions/Comments  |
|---|-------------------------------|--------------------|-----------------|---------------|---|
| <b>CAPACITANCE-TO-DIGITAL CONVERTER</b>     |                               |                    |                 |               |   |
| Update Rate                                 | 23                            | 25                 | 26              | ms            | Eight conversion stages in sequencer, decimation = 256                        |
| Resolution                                  |                               | 16                 |                 | Bit           |   |
| CIN Input Range <sup>1</sup>                |                               | $\pm 2$            |                 | pF            |   |
| No Missing Codes                            | 16                            |                    |                 | Bit           | Guaranteed by design, but not production tested                               |
| CIN Input Leakage                           |                               | 25                 |                 | nA            |   |
| Total Unadjusted Error                      |                               |                    | $\pm 20$        | %             |   |
| Output Noise (Peak-to-Peak)                 |                               | 7                  |                 | Codes         | Decimation rate = 128   |
|   |                               | 3                  |                 | Codes         | Decimation rate = 256   |
| Output Noise (RMS)                          |                               | 0.8                |                 | Codes         | Decimation rate = 128   |
|   |                               | 0.5                |                 | Codes         | Decimation rate = 256   |
| Parasitic Capacitance                       |                               |                    | 40              | pF            | Parasitic capacitance to ground, per CIN input guaranteed by characterization |
| C <sub>BULK</sub> Offset Range <sup>1</sup> |                               | $\pm 20$           |                 | pF            |   |
| C <sub>BULK</sub> Offset Resolution         |                               | 156.25             |                 | fF            |   |
| Low Power Mode Delay Accuracy               |                               |                    | 5               | %             | % of 200 ms, 400 ms, 600 ms, or 800 ms  |
| <b>EXCITATION SOURCE</b>                    |                               |                    |                 |               |   |
| Frequency                                   | 237.5                         | 240                | 262.5           | kHz           |   |
| Output Voltage                              |                               |                    | V <sub>CC</sub> | V             |   |
| Short-Circuit Source Current                |                               | 20                 |                 | mA            |   |
| Short-Circuit Sink Current                  |                               | 50                 |                 | mA            |   |
| Maximum Output Load                         |                               | 250                |                 | pF            | Capacitance load on source to ground  |
| C <sub>SHIELD</sub> Output Drive            |                               | 10                 |                 | $\mu\text{A}$ |   |
| C <sub>SHIELD</sub> Bias Level              |                               | V <sub>CC</sub> /2 |                 | V             |   |
| <b>LOGIC INPUTS (SCLK, SDA)</b>             |                               |                    |                 |               |   |
| V <sub>IH</sub> Input High Voltage          | $0.7 \times V_{\text{DRIVE}}$ |                    |                 | V             |   |
| V <sub>IL</sub> Input Low Voltage           |                               |                    | 0.4             | V             |   |
| I <sub>IH</sub> Input High Voltage          | -1                            |                    |                 | $\mu\text{A}$ | V <sub>IN</sub> = GND   |
| I <sub>IL</sub> Input Low Voltage           |                               |                    | 1               | $\mu\text{A}$ |   |
| Hysteresis                                  |                               | 150                |                 | mV            |   |
| <b>OPEN-DRAIN OUTPUTS (SCLK, SDA, INT)</b>  |                               |                    |                 |               |   |
| V <sub>OL</sub> Output Low Voltage          |                               |                    | 0.4             | V             | I <sub>SINK</sub> = -1 mA   |
| I <sub>OH</sub> Output High Leakage Current |                               | +0.1               | $\pm 1$         | $\mu\text{A}$ |   |
| <b>POWER</b>                                |                               |                    |                 |               |   |
| V <sub>CC</sub>                             | 2.6                           | 3.3                | 3.6             | V             |   |
| V <sub>DRIVE</sub>                          | 1.65                          |                    | 3.6             | V             |   |
| I <sub>CC</sub>                             |                               | 0.9                | 1               | mA            | In full power mode  |
|   |                               |                    | 20              | $\mu\text{A}$ | Low power mode, converter idle, T <sub>A</sub> = 25°C                         |
|   |                               | 16                 | 30              | $\mu\text{A}$ | Low power mode, converter idle  |
|   |                               |                    | 4.5             | $\mu\text{A}$ | Full shutdown, T <sub>A</sub> = 25°C  |
|   |                               | 2.25               | 15              | $\mu\text{A}$ | Full shutdown   |

<sup>1</sup> C<sub>IN</sub> and C<sub>BULK</sub> are defined as follows:

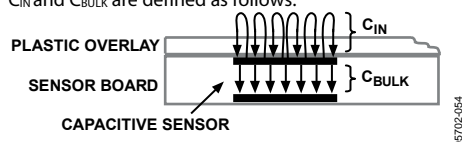


Table 2. Typical Average Current in Low Power Mode,  $V_{CC} = 3.6\text{ V}$ ,  $T = 25^\circ\text{C}$ , Load of 50 pF on SRC Pin

| Low Power Mode Delay | Decimation Rate | Number of Conversion Stages, Current Values Expressed in $\mu\text{A}$ |      |      |      |      |      |      |       |
|----------------------|-----------------|--|------|------|------|------|------|------|-------|
|                      |                 | 1  | 2    | 3    | 4    | 5    | 6    | 7    | 8     |
| 200 ms               | 128             | 26.4   | 33.3 | 40.1 | 46.9 | 53.5 | 60   | 66.5 | 72.8  |
|                      | 256             | 35.6   | 49.1 | 62.2 | 74.9 | 87.3 | 99.3 | 111  | 122.3 |
| 400 ms               | 128             | 21.3   | 24.8 | 28.3 | 31.7 | 35.2 | 38.6 | 42   | 45.4  |
|                      | 256             | 26   | 32.9 | 39.7 | 46.5 | 53.1 | 59.6 | 66.1 | 72.4  |
| 600 ms               | 128             | 19.6   | 21.9 | 24.3 | 26.6 | 28.9 | 31.2 | 33.5 | 35.8  |
|                      | 256             | 22.7   | 27.4 | 32   | 25.6 | 41.1 | 45.6 | 50   | 54.4  |
| 800 ms               | 128             | 18.7   | 20.5 | 22.2 | 24   | 25.7 | 27.5 | 29.2 | 31    |
|                      | 256             | 21.1   | 24.6 | 28.1 | 31.5 | 35   | 38.4 | 41.8 | 45.2  |

Table 3. Maximum Average Current in Low Power Mode,  $V_{CC} = 3.6\text{ V}$ , Load of 50 pF on SRC Pin

| Low Power Mode Delay | Decimation Rate | Number of Conversion Stages, Current Values Expressed in $\mu\text{A}$ |      |      |       |       |       |       |       |
|----------------------|-----------------|--|------|------|-------|-------|-------|-------|-------|
|                      |                 | 1  | 2    | 3    | 4     | 5     | 6     | 7     | 8     |
| 200 ms               | 128             | 42.2   | 50.5 | 58.7 | 66.7  | 74.6  | 82.3  | 90.0  | 97.5  |
|                      | 256             | 53.2   | 69.3 | 84.9 | 100.0 | 114.6 | 128.7 | 142.5 | 155.8 |
| 400 ms               | 128             | 36.1   | 40.4 | 44.5 | 48.7  | 52.8  | 56.9  | 60.9  | 64.5  |
|                      | 256             | 41.8   | 50.1 | 58.2 | 66.2  | 74.1  | 82.0  | 89.5  | 97.1  |
| 600 ms               | 128             | 34.1   | 37.0 | 39.7 | 42.5  | 45.3  | 48.1  | 50.8  | 53.4  |
|                      | 256             | 37.9   | 43.5 | 49.0 | 54.5  | 60.0  | 65.2  | 70.5  | 75.7  |
| 800 ms               | 128             | 33.1   | 35.2 | 37.3 | 39.4  | 41.5  | 43.6  | 45.7  | 47.7  |
|                      | 256             | 35.9   | 40.1 | 44.3 | 48.4  | 52.6  | 56.6  | 60.7  | 64.7  |

## I<sup>2</sup>C TIMING SPECIFICATIONS

$T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 2.6\text{ V}$  to  $3.6\text{ V}$ , unless otherwise noted. Sample tested at  $25^{\circ}\text{C}$  to ensure compliance. All input signals timed from a voltage level of  $1.6\text{ V}$ .

Table 4. I<sup>2</sup>C Timing Specifications<sup>1</sup>

| Parameter         | Limit | Unit              | Description   |
|-------------------|-------|-------------------|---|
| $f_{\text{SCLK}}$ | 400   | kHz max           |   |
| $t_1$             | 0.6   | $\mu\text{s}$ min | Start condition hold time, $t_{\text{HD; STA}}$                   |
| $t_2$             | 1.3   | $\mu\text{s}$ min | Clock low period, $t_{\text{LOW}}$                                |
| $t_3$             | 0.6   | $\mu\text{s}$ min | Clock high period, $t_{\text{HIGH}}$                              |
| $t_4$             | 100   | ns min            | Data setup time, $t_{\text{SU; DAT}}$                             |
| $t_5$             | 300   | ns min            | Data hold time, $t_{\text{HD; DAT}}$                              |
| $t_6$             | 0.6   | $\mu\text{s}$ min | Stop condition setup time, $t_{\text{SU; STO}}$                   |
| $t_7$             | 0.6   | $\mu\text{s}$ min | Start condition setup time, $t_{\text{SU; STA}}$                  |
| $t_8$             | 1.3   | $\mu\text{s}$ min | Bus free time between stop and start conditions, $t_{\text{BUF}}$ |
| $t_R$             | 300   | ns max            | Clock/data rise time  |
| $t_F$             | 300   | ns max            | Clock/data fall time  |

<sup>1</sup> Guaranteed by design, not production tested.

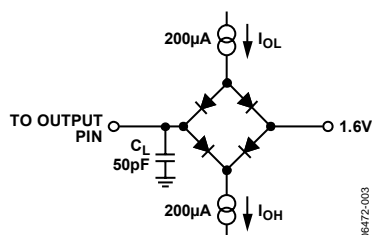


Figure 2. Load Circuit for Digital Output Timing Specifications

## ABSOLUTE MAXIMUM RATINGS

| Parameter   | Rating                            |
|---|-----------------------------------|
| VCC to GND  | −0.3 V to +3.6 V                  |
| Analog Input Voltage to GND                           | −0.3 V to VCC + 0.3 V             |
| Digital Input Voltage to GND                          | −0.3 V to VDRIVE + 0.3 V          |
| Digital Output Voltage to GND                         | −0.3 V to VDRIVE + 0.3 V          |
| Input Current to Any Pin Except Supplies <sup>1</sup> | 10 mA                             |
| ESD Rating (Human Body Model)                         | 2.5 kV                            |
| Operating Temperature Range                           | −40°C to +150°C                   |
| Storage Temperature Range                             | −65°C to +150°C                   |
| Junction Temperature                                  | 150°C                             |
| LFCSP_VQ  |                                   |
| Power Dissipation                                     | 450 mW                            |
| $\theta_{JA}$ Thermal Impedance                       | 135.7°C/W                         |
| IR Reflow Peak Temperature                            | 260°C ( $\pm 0.5^\circ\text{C}$ ) |
| Lead Temperature (Soldering 10 sec)                   | 300°C                             |

<sup>1</sup> Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

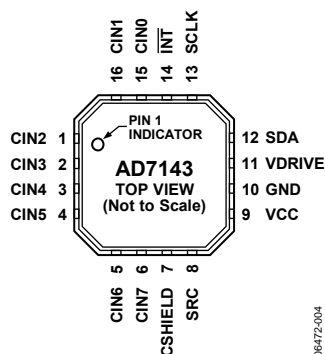


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Description  |
|---------|----------|--|
| 1       | CIN2     | Capacitance Sensor Input.  |
| 2       | CIN3     | Capacitance Sensor Input.  |
| 3       | CIN4     | Capacitance Sensor Input.  |
| 4       | CIN5     | Capacitance Sensor Input.  |
| 5       | CIN6     | Capacitance Sensor Input.  |
| 6       | CIN7     | Capacitance Sensor Input.  |
| 7       | CSHIELD  | CDC Shield Potential Output. Requires 10 nF capacitor to ground.                               |
| 8       | SRC      | CDC Excitation Source Output.  |
| 9       | VCC      | CDC Supply Voltage.  |
| 10      | GND      | Ground Reference Point for All CDC Circuitry. Tie to ground plane.                             |
| 11      | VDRIVE   | I <sup>2</sup> C Serial Interface Operating Voltage  |
| 12      | SDA      | I <sup>2</sup> C Serial Data Input/Output. SDA requires pull-up resistor.                      |
| 13      | SCLK     | Clock Input for Serial Interface. SCLK requires pull-up resistor.                              |
| 14      | INT      | General-Purpose Open-Drain Interrupt Output. Programmable polarity; requires pull-up resistor. |
| 15      | CIN0     | Capacitance Sensor Input.  |
| 16      | CIN1     | Capacitance Sensor Input.  |

## TYPICAL PERFORMANCE CHARACTERISTICS

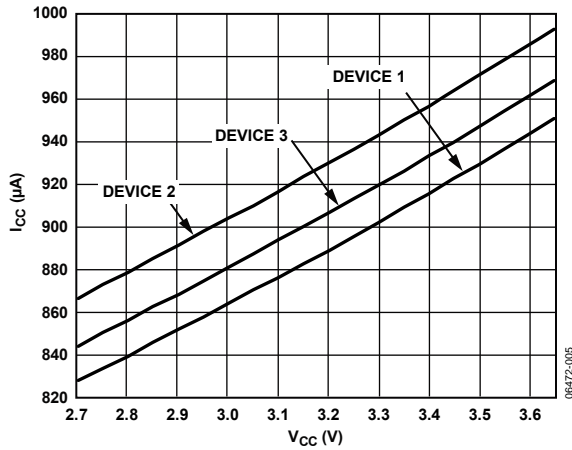


Figure 4. Supply Current vs. Supply Voltage

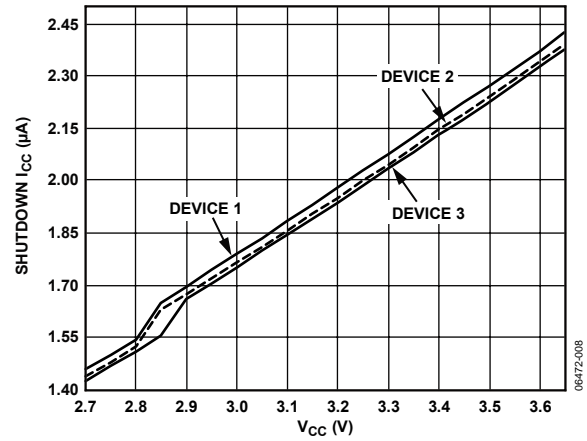


Figure 7. Shutdown Supply Current vs. Supply Voltage

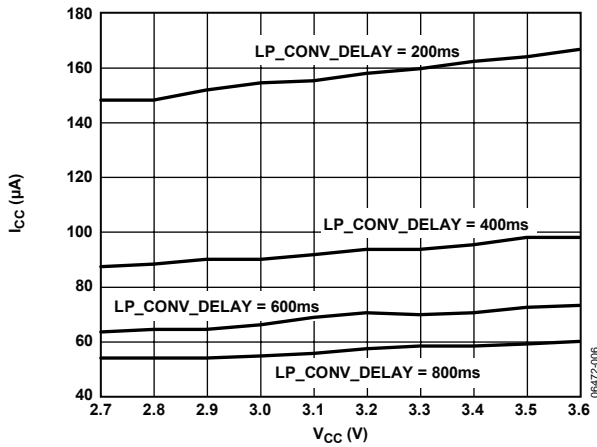
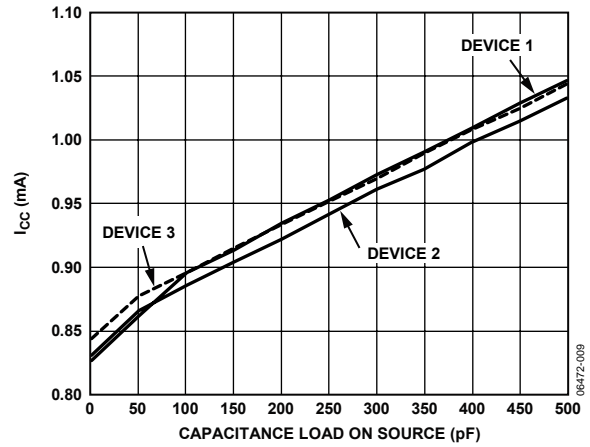
Figure 5. Low Power Supply Current vs. Supply Voltage,  
Decimation Rate = 256

Figure 8. Supply Current vs. Capacitive Load on SRC

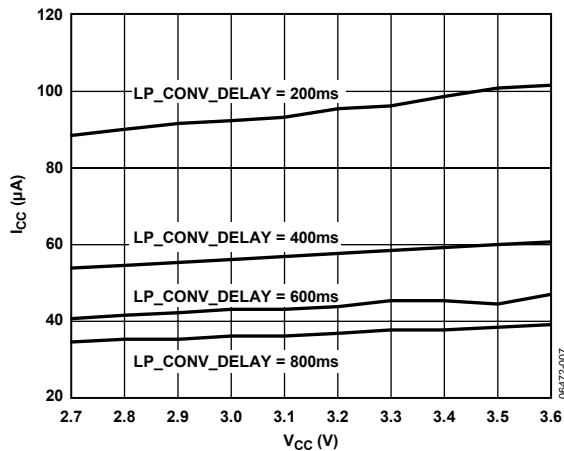
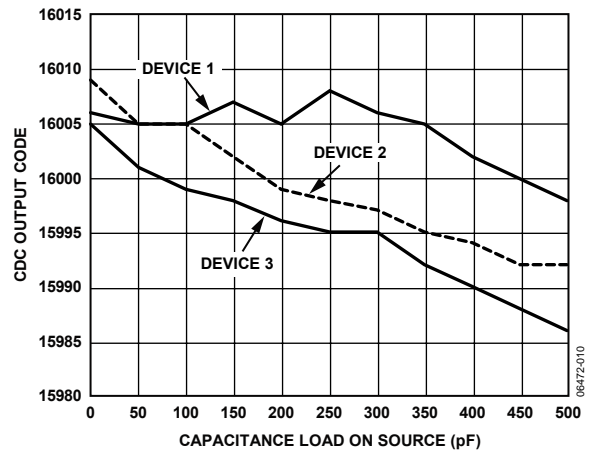
Figure 6. Low Power Supply Current vs. Supply Voltage  
Decimation Rate = 128

Figure 9. Output Code vs. Capacitive Load on SRC



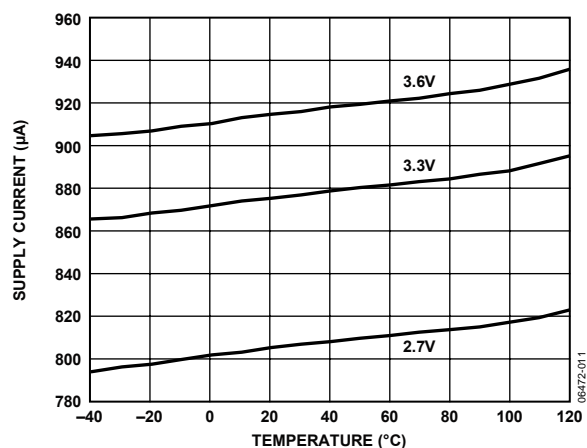


Figure 10. Supply Current vs. Temperature

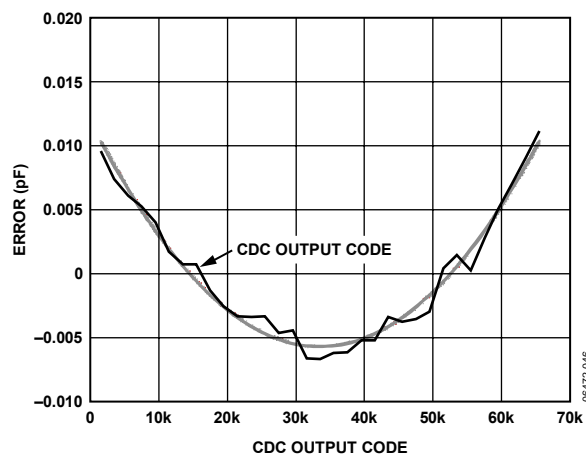


Figure 13. 3.3 V Linearity Error

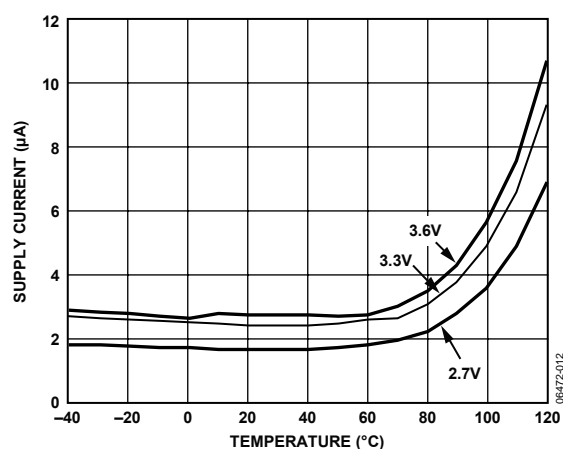


Figure 11. Shutdown Supply Current vs. Temperature

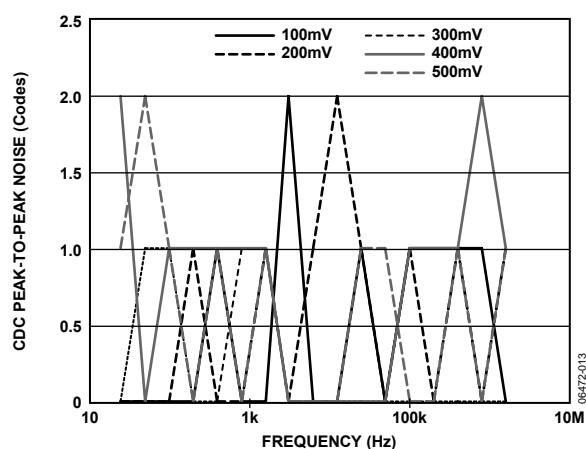


Figure 14. Power Supply Sine Wave Rejection

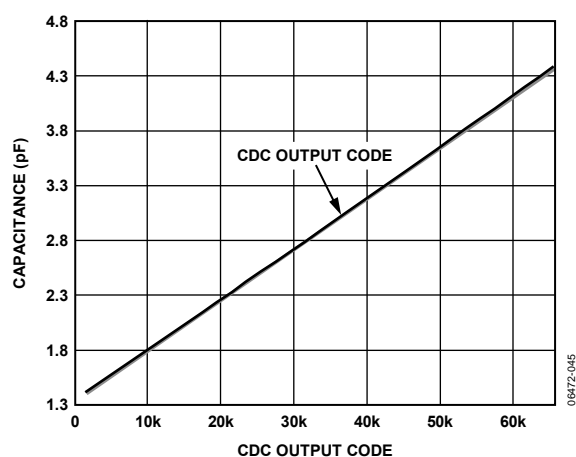


Figure 12. 3.3 V Linearity

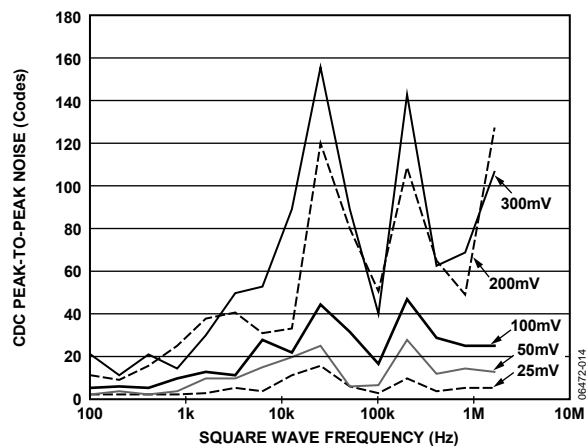


Figure 15. Power Supply Square Wave Rejection

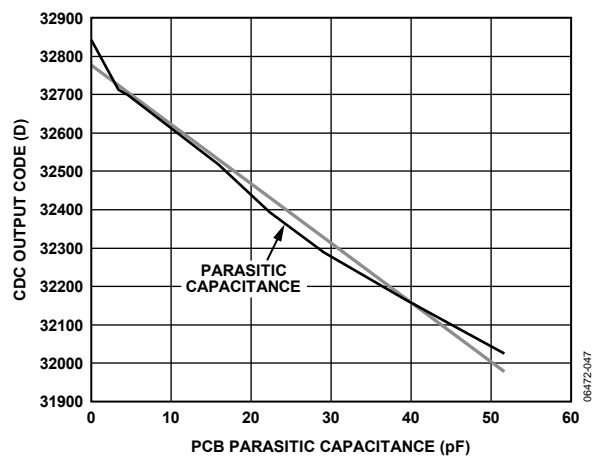


Figure 16. CDC Output Codes vs. Parasitic Capacitance

## THEORY OF OPERATION

The AD7143 is a capacitance-to-digital converter (CDC) with on-chip environmental compensation, intended for use in portable systems requiring high resolution user input. The internal circuitry consists of a 16-bit,  $\Sigma$ - $\Delta$  converter that converts a capacitive input signal into a digital value. There are eight input pins, CIN0 to CIN7, on the AD7143. A switch matrix routes the input signals to the CDC. The result of each capacitance-to-digital conversion is stored in on-chip registers. The host subsequently reads the results over the serial interface. The AD7143 has an I<sup>2</sup>C interface, ensuring that the parts are compatible with a wide range of host processors.

The AD7143 interfaces with up to eight external capacitance sensors. These sensors can be arranged as buttons, scroll bars, wheels, or as a combination of sensor types. The external sensors consist of electrodes on a single or multiple layer PCB that interface directly to the AD7143.

The AD7143 can be set up to implement any set of input sensors by programming the on-chip registers. The registers can also be programmed to control features such as averaging, offsets, and gains for each of the external sensors. There is a sequencer on-chip to control how each of the capacitance inputs is polled.

The AD7143 has on-chip digital logic and 528 words of RAM used for environmental compensation. The effects of humidity, temperature, and other environmental factors can effect the operation of capacitance sensors. Transparent to the user, the AD7143 performs continuous calibration to compensate for these effects, allowing the AD7143 to give error-free results at all times.

The AD7143 requires some minor companion software that runs on the host or other microcontroller to implement high resolution sensor functions, such as a scroll bar or wheel. However, no host software is required to implement buttons, including 8-way button functionality. Button sensors are implemented completely in digital logic on-chip with the status of each button reported in interrupt status registers.

The AD7143 can be programmed to operate in either full power mode, or in low power automatic wake-up mode. The automatic wake-up mode is particularly suited for portable devices that require low power operation giving the user significant power savings coupled with full functionality.

The AD7143 has an interrupt output,  $\overline{\text{INT}}$ , to indicate when new data has been placed into the registers.  $\overline{\text{INT}}$  is used to interrupt the host on sensor activation.

The AD7143 operates from a 2.6 V to 3.6 V supply, and is available in a 16-lead, 4 mm × 4 mm LFCSP\_VQ.

## CAPACITANCE SENSING THEORY

The AD7143 uses a method of sensing capacitance known as the shunt method. Using this method, an excitation source is connected to a transmitter generating an electric field to a receiver. The field lines measured at the receiver are translated into the digital domain by a  $\Sigma$ - $\Delta$  converter. When a finger, or other grounded object, interferes with the electric field, some of the field lines are shunted to ground and do not reach the receiver (see Figure 17). Therefore, the total capacitance measured at the receiver decreases when an object comes close to the induced field.

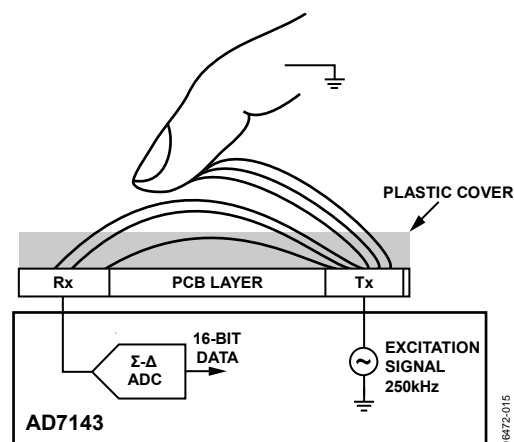


Figure 17. Single Layer Sensing Capacitance Method

In practice, the excitation source and  $\Sigma$ - $\Delta$  ADC are implemented on the AD7143, while the transmitter and receiver are constructed on a PCB that comprises the external sensor.

## Registering a Sensor Activation

When a sensor is approached, the total capacitance associated with that sensor, measured by the AD7143, changes. When the capacitance changes to such an extent that a set threshold is exceeded, the AD7143 registers this as a sensor touch and then automatically updates the internal interrupt status registers.

Preprogrammed threshold levels are used to determine if a change in capacitance is due to a button being activated. If the capacitance exceeds one of the threshold limits, the AD7143 registers this as a true button activation. The same threshold principle is used to determine if other types of sensors, such as sliders or scroll wheels, are activated.

### Complete Solution for Capacitance Sensing

Analog Devices, Inc. provides a complete solution for capacitance sensing. The two main elements to the solution are the sensor PCB and the AD7143.

If the application requires high resolution sensors, such as scroll bars or wheels, software is required that runs on the host processor. (No software is required for button sensors.) The memory requirements for the host depend upon the sensor, and are typically 9 kB of code and 600 bytes of data memory.

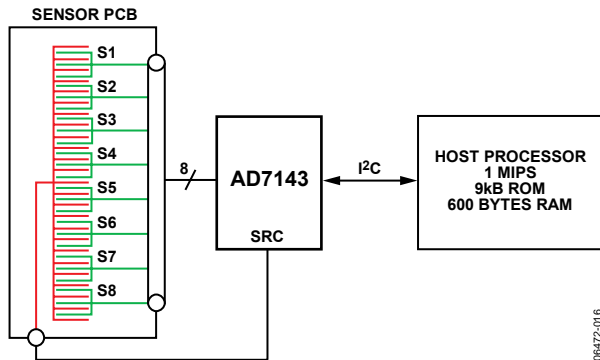


Figure 18. Three Part Capacitance Sensing Solution

Analog Devices supplies the sensor PCB footprint design libraries to the customer based on the customer's specifications, and supplies any necessary software on an open-source basis.

### OPERATING MODES

The AD7143 has three operating modes. Full power mode, where the device is always fully powered, is suited for applications where power is not a concern. One example is game consoles that have an ac power supply. Low power mode, where the part automatically powers down, is tailored to give significant power savings over full power mode, and is suited for mobile applications where power must be conserved. In shutdown mode, the part shuts down completely.

The POWER\_MODE bits (Bit 0 and Bit 1) of the control register set the operating mode on the AD7143. The control register is at Address 0x000. Table 6 shows the POWER\_MODE settings for each operating mode. To put the AD7143 into shutdown mode, set the POWER\_MODE bits to either 01 or 11.

Table 6. POWER\_MODE Settings

| POWER_MODE Bits | Operating Mode     |
|-----------------|--------------------|
| 00              | Full power mode    |
| 01              | Full shutdown mode |
| 10              | Low power mode     |
| 11              | Full shutdown mode |

The power-on default setting of the POWER\_MODE bits is 00, full power mode.

### Full Power Mode

In full power mode, all sections of the AD7143 remain fully powered at all times. While a sensor is being touched, the AD7143 processes the sensor data. If no sensor is touched, the AD7143 measures the ambient capacitance level and uses this data for the on-chip compensation routines. In full power mode, the AD7143 converts at a constant rate. See the CDC Conversion Sequence Time section for more information.

### Low Power Mode

When in low power mode, the AD7143 POWER\_MODE bits are set to 10 upon device initialization. If the external sensors are not touched, the AD7143 reduces its conversion frequency, thereby greatly reducing its power consumption. The part remains in a reduced power state when the sensors are not touched. Every LP\_CONV\_DELAY ms (200 ms, 400 ms, 600 ms or 800 ms), the AD7143 performs a conversion and uses this data to update the compensation logic. When an external sensor is touched, the AD7143 begins a conversion sequence every 25 ms to read back data from the sensors.

In low power mode, the total current consumption of the AD7143 is an average of the current used during a conversion, and the current used while the AD7143 is waiting for the next conversion to begin. For example, when LP\_CONV\_DELAY is 400 ms, the AD7143 typically uses 0.9 mA current for 25 ms and 15  $\mu$ A for 400 ms of the conversion interval. Note that these conversion timings can be altered through the register settings. See the CDC Conversion Sequence Time section for more information.

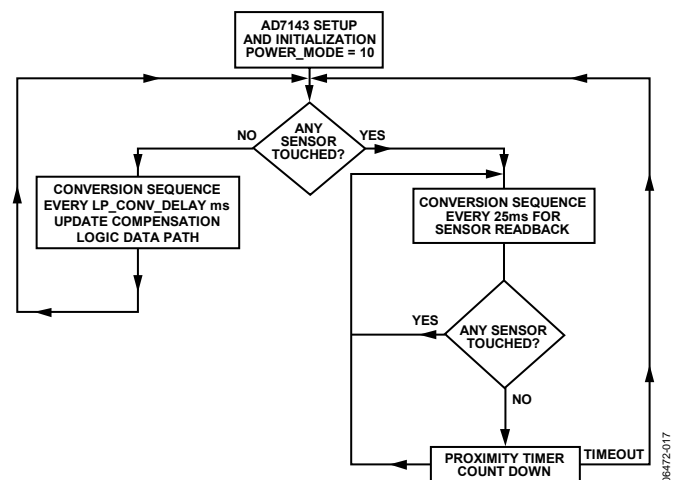


Figure 19. Low Power Mode Operation

The time taken for the AD7143 to go from a full power state to a reduced power state, once the user stops touching the external sensors, is configurable. Once the sensors are not touched, the PWR\_DWN\_TIMEOUT bits, in the Ambient Compensation Ctrl 0 Register at Address 0x002, control the amount of time necessary for the device to return to a reduced power state.

## CAPACITANCE SENSOR INPUT CONFIGURATION

Each input connection from the external capacitance sensors to the AD7143 converter can be uniquely configured by using the registers in Table 38 and Table 39. These registers are used to configure input pin connection setups, sensor offsets, sensor sensitivities, and sensor limits for each stage. Each sensor can be individually optimized. For example, a button sensor connected to STAGE0 can have a different sensitivity and offset values than a button with a different function that is connected to a different stage.

### CIN INPUT MULTIPLEXER SETUP

The CIN\_CONNECTION\_SETUP registers in Table 38 list the available options for connecting the sensor input pin to the CDC.

The AD7143 has an on-chip multiplexer to route the input signals from each pin to the input of the converter. Each input pin can be tied to either the negative or the positive input of the CDC or can be left floating. Each input can also be internally connected to the  $C_{SHIELD}$  signal to help prevent cross coupling. If an input is not used, always connect it to  $C_{SHIELD}$ .

Connecting a CINx input pin to the positive CDC input results in a decrease in CDC output code when the corresponding sensor is activated. Connecting a CINx input pin to the negative CDC input results in an increase in CDC output code when the corresponding sensor is activated.

Two bits in each sequencer stage register control the mux setting for the input pin.

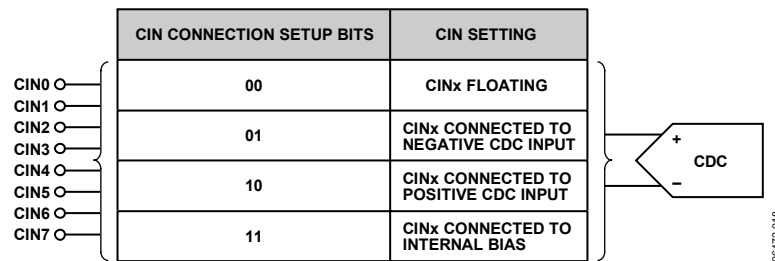


Figure 20. Input Mux Configuration Options

## CAPACITANCE-TO-DIGITAL CONVERTER

The capacitance-to-digital converter on the AD7143 has a  $\Sigma$ - $\Delta$  architecture with 16-bit resolution. Eight possible inputs to the CDC are connected to the input of the converter through a switch matrix. The sampling frequency of the CDC is 250 kHz.

### OVERSAMPLING THE CDC OUTPUT

The decimation rate, or oversampling ratio, is determined by Bits[9:8] of the PWR\_CONTROL register located at Address 0x000 and listed in Table 7.

Table 7. CDC Decimation Rate

| Decimation Bit Value | Decimation Rate | CDC Output Rate Per Stage |
|----------------------|-----------------|---------------------------|
| 00                   | 256             | 3.072 ms                  |
| 01                   | 128             | 1.525 ms                  |
| 10 <sup>1</sup>      | —               | —                         |
| 11 <sup>1</sup>      | —               | —                         |

<sup>1</sup> Do not use this setting.

The decimation process on the AD7143 is an averaging process where a number of samples are taken and the averaged result is output. Due to the architecture of the digital filter employed, the amount of samples taken (per stage) is equal to  $3 \times$  the decimation rate. Therefore,  $3 \times 256$  or  $3 \times 128$  samples are averaged to obtain each stage result.

The decimation process reduces the amount of noise present in the final CDC result. However, the higher the decimation rate, the lower the output rate per stage thus, a trade-off is possible between a noise free signal and speed of sampling.

### CAPACITANCE SENSOR OFFSET CONTROL

There are two programmable DACs on board the AD7143 to null any capacitance sensor offsets. These offsets are associated with printed circuit board capacitance or capacitance due to any other source, such as connectors. In Figure 21,  $C_{IN}$  is the capacitance of the input sensors, while  $C_{BULK}$  is the capacitance between layers of the sensor PCB.  $C_{BULK}$  can be offset using the on-board DACs.

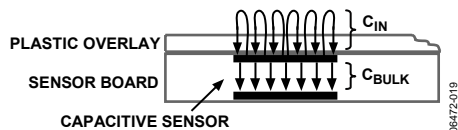


Figure 21. Capacitances Around the Sensor PCB

A simplified block diagram in Figure 22 shows how to apply the STAGE\_OFFSET registers to null the offsets. The 7-bit POS\_AFE\_OFFSET and NEG\_AFE\_OFFSET registers program the offset DAC to provide 0.16 pF resolution offset adjustment over a range of  $\pm 20$  pF. Apply the positive and negative offsets to either the positive or the negative CDC input using the NEG\_AFE\_OFFSET register and POS\_AFE\_OFFSET register. This process is only required once during the initial capacitance sensor characterization.

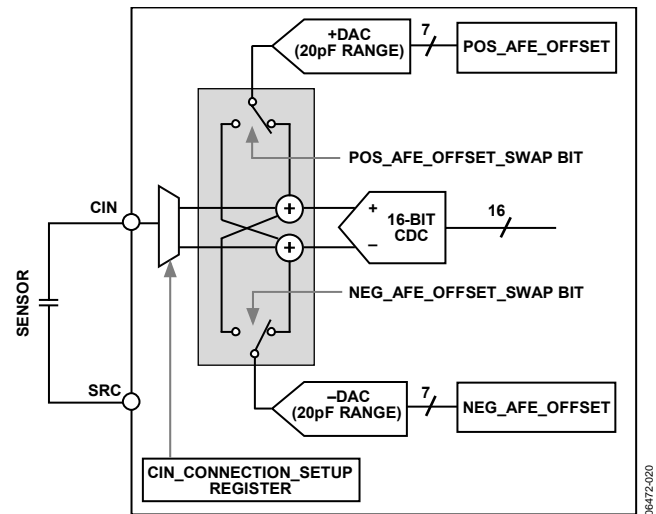


Figure 22. Analog Front-End Offset Control

### CONVERSION SEQUENCER

The AD7143 has an on-chip sequencer to implement conversion control for the input channels. Up to eight conversion stages can be performed in sequence. Each of the eight conversion stages can measure an input from a different sensor. By using the Bank 2 registers, each stage can be uniquely configured to support multiple capacitance sensor interface requirements. For example, a sensor S1 can be assigned to STAGE1 and sensor S2 assigned to STAGE2.

The AD7143 on-chip sequence controller provides conversion control beginning with STAGE0. Figure 23 shows a block diagram of the CDC conversion stages and CIN inputs. A conversion sequence is a sequence of CDC conversions starting at STAGE0 and ending at the stage determined by the value programmed in the SEQUENCE\_STAGE\_NUM register. Depending on the number and type of capacitance sensors used, not all conversion stages are required. Use the SEQUENCE\_STAGE\_NUM register to set the number of conversions in one sequence, depending on the sensor interface requirements. For example, this register is set to 5 if the CIN inputs are mapped to only six stages. In addition, set the STAGE\_CAL\_EN registers according to the number of stages that are used.

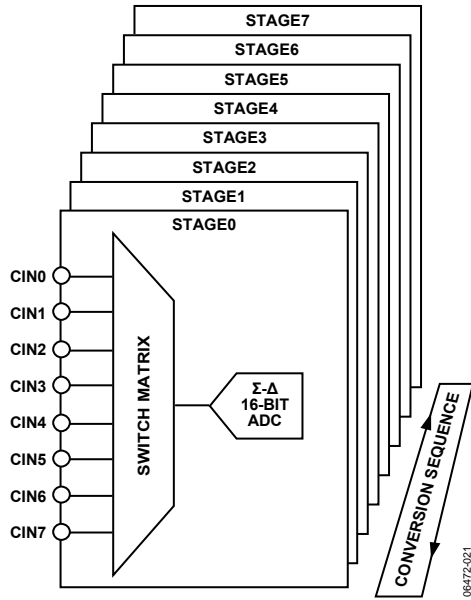


Figure 23. CDC Conversion Stages

The number of required conversion stages depends completely on the number of sensors attached to the AD7143. Figure 24 shows how many conversion stages are required for each sensor, and how many inputs each sensor requires to the AD7143.

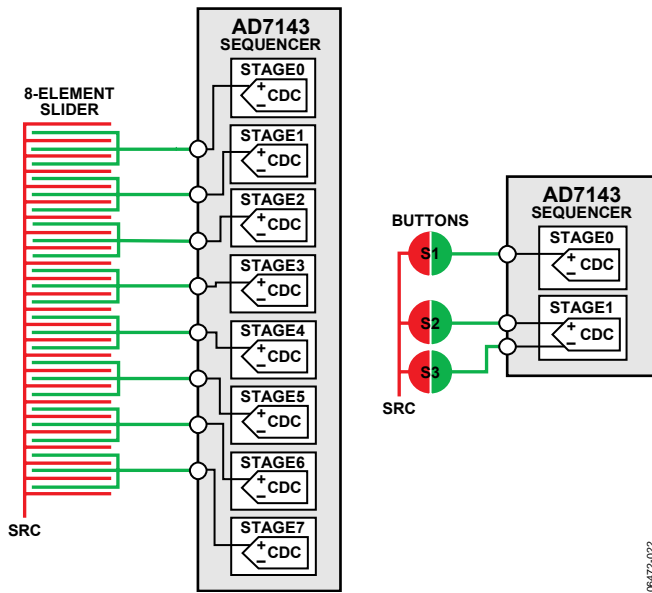


Figure 24. Sequencer Setup for Sensors

A button sensor generally requires one sequencer stage. However, it is possible to configure two button sensors to operate differentially for special applications where the user should not press both buttons simultaneously, such as a with rocker zoom switch on a digital camera.

In this case, only one button from the pair is activated at a time; pressing both buttons together activates neither button. This example is shown in Figure 24 for sensor buttons S2 and S3.

A scroll bar or slider requires eight stages. The result from each stage is used by the host software to determine the user's position on the scroll bar. The algorithm that performs this process is available from Analog Devices free of charge, upon signing a software license. Scroll wheels also require eight stages.

### CDC CONVERSION SEQUENCE TIME

The time required for one complete measurement for all eight stages by the CDC is defined as the CDC conversion sequence time. The `SEQUENCE_STAGE_NUM` register and `DECIMATION` register determine the conversion time as listed in Table 8.

Table 8. CDC Conversion Times for Full Power Mode

| SEQUENCE_STAGE_NUM | Conversion Time (ms) |                  |
|--------------------|----------------------|------------------|
|                    | Decimation = 128     | Decimation = 256 |
| 0                  | 1.525                | 3.072            |
| 1                  | 3.072                | 6.144            |
| 2                  | 4.608                | 9.216            |
| 3                  | 6.144                | 12.288           |
| 4                  | 7.68                 | 15.25            |
| 5                  | 9.216                | 18.432           |
| 6                  | 10.752               | 21.504           |
| 7                  | 12.288               | 24.576           |

For example, while operating with a decimation rate of 128, if the `SEQUENCE_STAGE_NUM` register is set to 5 for the conversion of six stages in a sequence, the conversion sequence time is 9.216 ms.

### Full Power Mode CDC Conversion Sequence Time

The full power mode CDC conversion sequence time for all eight stages is set by configuring the `SEQUENCE_STAGE_NUM` register and the `DECIMATION` register as outlined in Table 8.

Figure 25 shows a simplified timing diagram of the full power CDC conversion time. The full power mode CDC conversion time  $t_{\text{CONV\_FP}}$  is set using Table 8.

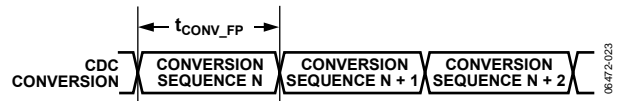


Figure 25. Full Power Mode CDC Conversion Sequence Time



### Low Power Mode CDC Conversion Sequence Time with Delay

The frequency of each CDC conversion while operating in the low power automatic wake-up mode is controlled by using the LP\_CONV\_DELAY register located at Address 0x000[3:2], in addition to the registers listed in Table 8.

This feature provides some flexibility for optimizing the conversion time to meet system requirements vs. AD7143 power consumption. For example, maximum power savings is achieved when the LP\_CONV\_DELAY register is set to 3. With a setting of 3, the AD7143 automatically wakes up, performing a conversion every 800 ms.

**Table 9. LP\_CONV\_DELAY Settings**

| LP_CONV_DELAY Bits | Delay Between Conversions |
|--------------------|---------------------------|
| 00                 | 200 ms                    |
| 01                 | 400 ms                    |
| 10                 | 600 ms                    |
| 11                 | 800 ms                    |

Figure 26 shows a simplified timing example of the low power CDC conversion time. As shown, the low power CDC conversion time is set by  $t_{\text{CONV\_FP}}$  and the LP\_CONV\_DELAY register.

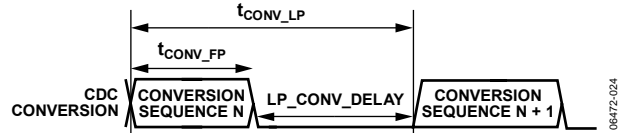


Figure 26. Low Power Mode CDC Conversion Sequence Time

### CDC CONVERSION RESULTS

Certain high-resolution sensors require the host to read back the CDC conversion results for processing. The registers required for host processing are located in the Bank 3 registers. The host processes the data readback from these registers using a software algorithm to determine position information. In addition to the results registers in the Bank 3 registers, the AD7143 provides the 16-bit CDC output data directly starting at Address 0x00B of Bank 1. Reading back the CDC 16-bit conversion data register allows for customer-specific application data processing.



## NONCONTACT PROXIMITY DETECTION

The AD7143 internal signal processing continuously monitors all capacitance sensors for noncontact proximity detection. This feature provides the ability to detect when a user is approaching a sensor, immediately disabling all internal calibration while the AD7143 is automatically configured to detect a valid contact.

The proximity control register bits are described in Table 10. FP\_PROXIMITY\_CNT register bits and LP\_PROXIMITY\_CNT register bits control the length of the calibration disable period after proximity is detected in full power and low power modes. The calibration is disabled during this time and enabled again at the end of this period if the user is no longer approaching, or in contact with, the sensor. Figure 27 and Figure 28 show examples of how these registers are used to set the full and low power mode calibration disable periods.

*Calibration disable period in full power mode =*  
 $(FP\_PROXIMITY\_CNT \times 16 \times \text{Time for one conversion sequence in full power mode})$

*Calibration disable period in low power mode =*  
 $(LP\_PROXIMITY\_CNT \times 4 \times \text{Time for one conversion sequence in low power mode})$

### RECALIBRATION

In certain situations, the proximity flag can be set for a long period, such as when a user hovers over a sensor for a long time. The environmental calibration on the AD7143 is suspended while the proximity is detected, but changes may occur to the ambient capacitance level during the proximity event. Even when the user has left the sensor untouched, the proximity flag may still be set. This could occur if the user interaction creates some moisture on the sensor causing the new sensor value to be different from the expected value. In this case, the AD7143 automatically forces an internal recalibration. This ensures that the ambient values are recalibrated, regardless of how long the user hovers over a sensor.

The AD7143 recalibrates automatically when the measured CDC value exceeds the stored ambient value by an amount determined by PROXIMITY\_RECAL\_LVL, for a set period known as the recalibration timeout. In full power mode, the recalibration

timeout is controlled by FP\_PROXIMITY\_RECAL and in low power mode, it is controlled by LP\_PROXIMITY\_RECAL.

*Recalibration timeout in full power mode =*  
 $FP\_PROXIMITY\_RECAL \times \text{Time for one conversion sequence in full power mode}$

*Recalibration timeout in low power mode =*  
 $LP\_PROXIMITY\_RECAL \times \text{Time taken for one conversion sequence in low power mode}$

Figure 29 and Figure 30 show examples of using the FP\_PROXIMITY\_RECAL and LP\_PROXIMITY\_RECAL register bits to force a recalibration while operating in the full and low power modes. These figures show the result of a user approaching a sensor then leaving the sensor while the proximity detection remains active after the user discontinues contact with the sensor. This situation could occur if the user interaction created some moisture on the sensor causing the new sensor value to be different from the expected value. In this case, the internal recalibration is applied to automatically recalibrate the sensor. The forced recalibration event takes two interrupt cycles; therefore, it should not be set again during this interval.

### PROXIMITY SENSITIVITY

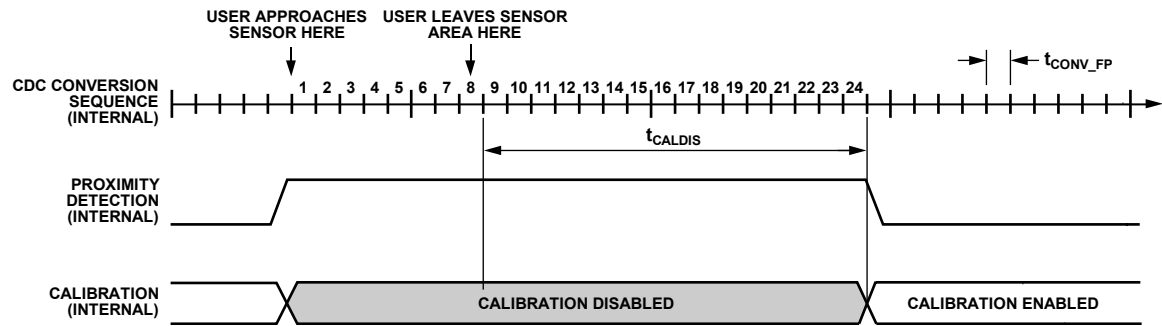
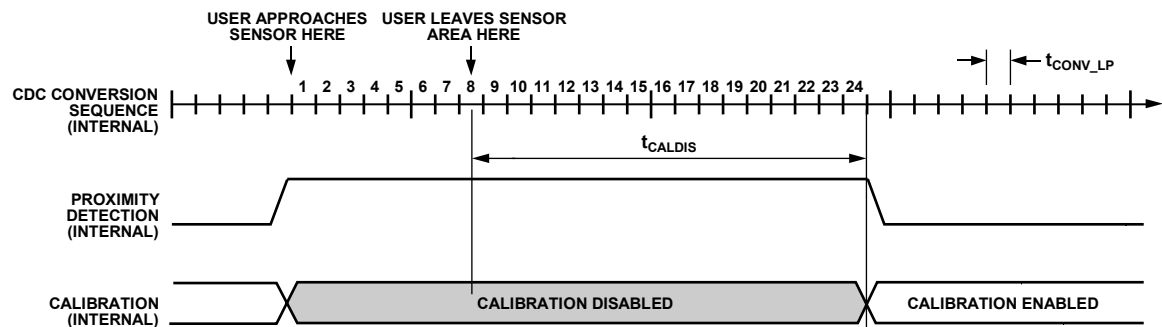
The fast filter in Figure 31 is used to detect when someone is in close proximity to the sensor. Two conditions set the internal proximity detection signal using Comparator 1 and Comparator 2.

Comparator 1 detects when a user is approaching a sensor. The PROXIMITY\_DETECTION\_RATE register controls the sensitivity of Comparator 1. Consider, for example, if the PROXIMITY\_DETECTION\_RATE is set to 4, the Proximity 1 signal is set when the absolute difference between WORD1 and WORD3 exceeds four LSB codes.

Comparator 2 detects when a user hovers over a sensor or approaches a sensor very slowly. The PROXIMITY\_RECAL\_LVL register (Address 0x003) controls the sensitivity of Comparator 2. For example, if PROXIMITY\_RECAL\_LVL is set to 75, the Proximity 2 signal is set when the absolute difference between the fast filter average value and the ambient value exceeds 75 LSB codes.

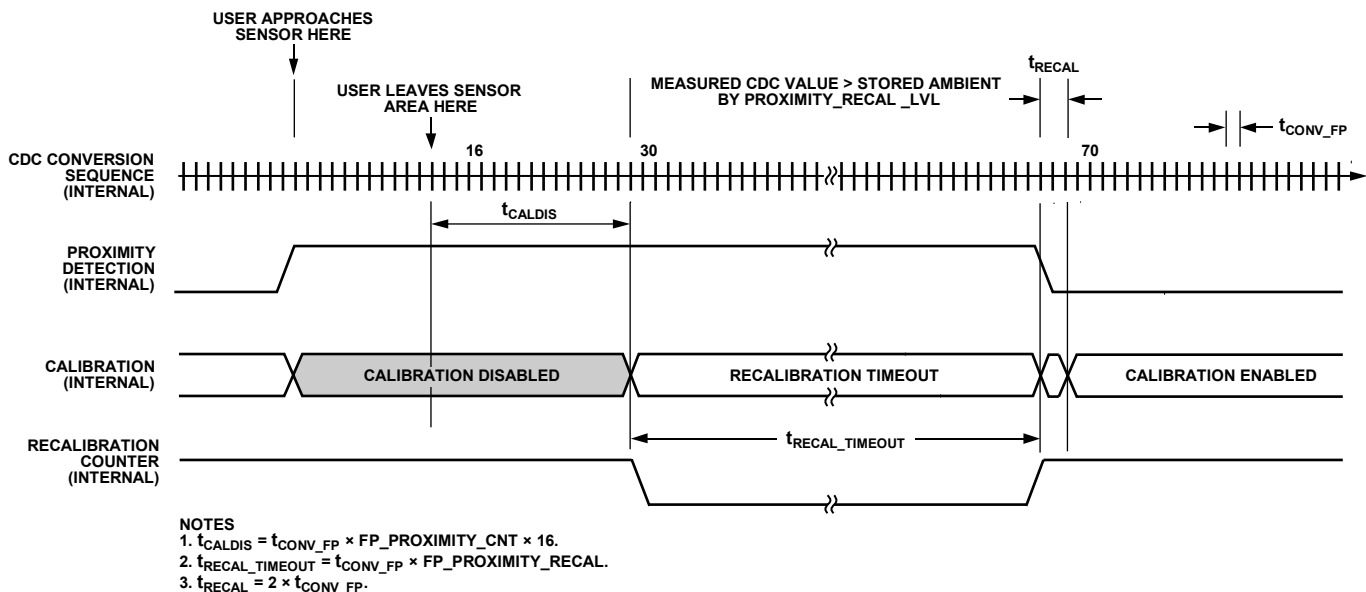
**Table 10. Proximity Control Registers (See Figure 31)**

| Register                 | Length | Register Address | Description                                     |
|--------------------------|--------|------------------|---|
| FP_PROXIMITY_CNT         | 4 bits | 0x002 [7:4]      | Calibration disable time in full power mode     |
| LP_PROXIMITY_CNT         | 4 bits | 0x002 [11:8]     | Calibration disable time in low power mode      |
| FP_PROXIMITY_RECAL       | 8 bits | 0x004 [9:0]      | Full power mode proximity recalibration control |
| LP_PROXIMITY_RECAL       | 6 bits | 0x004 [15:10]    | Low power mode proximity recalibration control  |
| PROXIMITY_RECAL_LVL      | 8 bits | 0x003 [13:8]     | Proximity recalibration level                   |
| PROXIMITY_DETECTION_RATE | 6 bits | 0x003 [7:0]      | Proximity detection rate                        |

Figure 27. Full Power Mode Proximity Detection Example with  $FP\_PROXIMITY\_CNT = 1$ 

## NOTES

1. SEQUENCE CONVERSION TIME  $t_{CONV\_LP} = t_{CONV\_FP} + LP\_CONV\_DELAY$ .
2. PROXIMITY IS SET WHEN USER APPROACHES THE SENSOR AT WHICH TIME THE INTERNAL CALIBRATION IS DISABLED.
3.  $t_{CALDIS} = (t_{CONV\_LP} \times LP\_PROXIMITY\_CNT \times 4)$ .

Figure 28. Low Power Mode Proximity Detection with  $LP\_PROXIMITY\_CNT = 4$  and  $LP\_CONV\_DELAY = 0$ 

## NOTES

1.  $t_{CALDIS} = t_{CONV\_FP} \times FP\_PROXIMITY\_CNT \times 16$ .
2.  $t_{RECAL\_TIMEOUT} = t_{CONV\_FP} \times FP\_PROXIMITY\_RECAL$ .
3.  $t_{RECAL} = 2 \times t_{CONV\_FP}$ .

Figure 29. Full Power Mode Proximity Detection with Forced Recalibration Example with  $FP\_PROXIMITY\_CNT = 1$  and  $FP\_PROXIMITY\_RECAL = 40$ 

Note that in Figure 29, the sequence conversion time,  $t_{CONV\_FP}$ , is determined from Table 8.

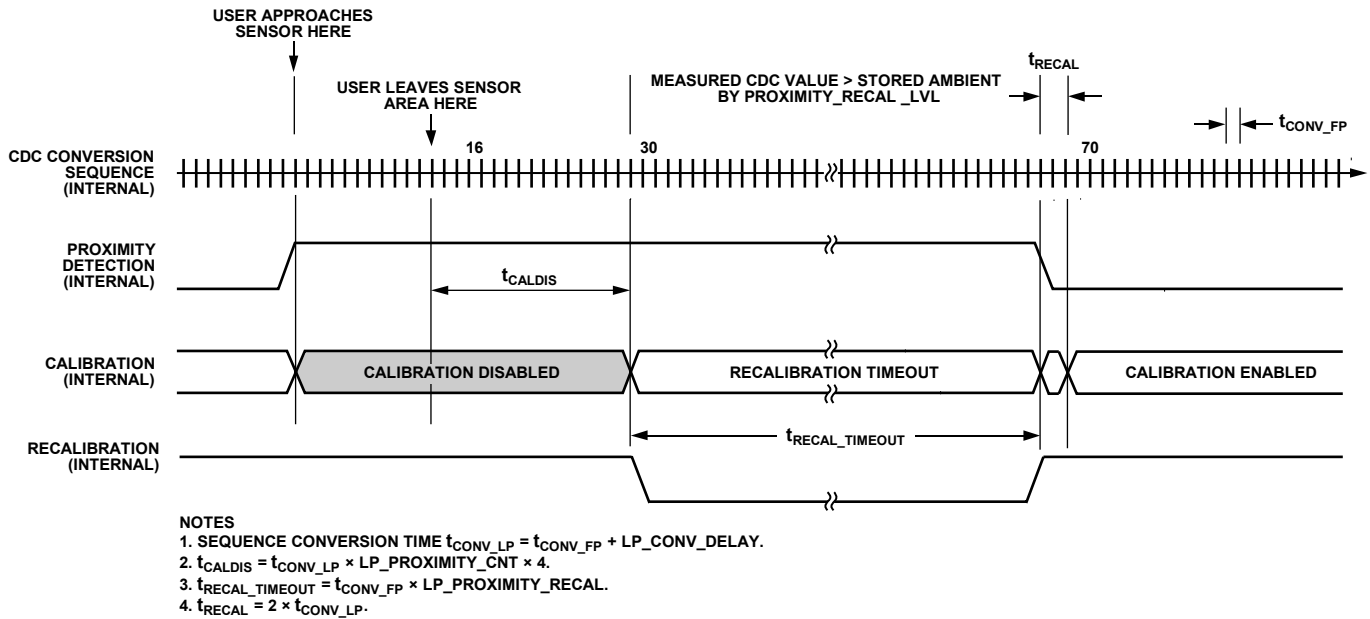


Figure 30. Low Power Mode Proximity Detection with Forced Recalibration Example with  $LP\_PROXIMIT\_CNT = 4$  and  $LP\_PROXIMITY\_RECAL = 10$

### FF\_SKIP\_CNT

The proximity detection fast FIFO is used by the on-chip logic to determine if proximity is detected. The fast FIFO expects to receive samples from the converter at a set rate. Using FF\_SKIP\_CNT normalizes the frequency of the samples going into the FIFO, regardless of how many conversion stages are in a sequence. In Register 0x02, Bits[3:0] are the fast filter skip control, FF\_SKIP\_CNT. This value determines which CDC samples are not used (skipped) in the proximity detection fast FIFO.

Determining the FF\_SKIP\_CNT value is required only once during the initial setup of the capacitance sensor interface.

Table 11 shows how FF\_SKIP\_CNT controls the update rate to the fast FIFO. The recommended value for FF\_SKIP\_CNT when using all 12 conversion stages on the AD7143 is

$FF\_SKIP\_CNT = 0000 = \text{no samples skipped}$

### SLOW FIFO

As shown in Figure 31, a number of FIFOs are implemented on the AD7143. These FIFOs are located in Bank 3 of the on-chip memory. The slow FIFOs are used by the on-chip logic to monitor the ambient capacitance level from each sensor.

#### AVG\_FP\_SKIP and AVG\_LP\_SKIP

In Register 0x001, Bits[13:12] are the slow FIFO skip control for full power mode, AVG\_FP\_SKIP. Bits[15:14] in the same register are the slow FIFO skip control for low power mode, AVG\_LP\_SKIP. These values determine which CDC samples are not used (skipped) in the slow FIFO. Changing these values slows down or speeds up the rate at which the ambient

capacitance value tracks the measured capacitance value read by the converter.

Slow FIFO update rate in full power mode is equal to

$$AVG\_FP\_SKIP \times [(3 \times \text{Decimation Rate}) \times (SEQUENCE\_STAGE\_NUM + 1) \times (FF\_SKIP\_CNT + 1) \times 4 \times 10^{-7}]$$

Slow FIFO update rate in low power mode is equal to

$$(AVG\_LP\_SKIP + 1) \times [(3 \times \text{Decimation Rate}) \times (SEQUENCE\_STAGE\_NUM + 1) \times (FF\_SKIP\_CNT + 1) \times 4 \times 10^{-7}] / [(FF\_SKIP\_CNT + 1) + LP\_CONV\_DELAY]$$

The slow FIFO is used by the on-chip logic to track the ambient capacitance value. The slow FIFO expects to receive samples from the converter at a rate of 33 ms to 40 ms. AVG\_FP\_SKIP and AVG\_LP\_SKIP are used to normalize the frequency of the samples going into the FIFO, regardless of how many conversion stages are in a sequence.

Determining the AVG\_FP\_SKIP and AVG\_LP\_SKIP value is only required once during the initial setup of the capacitance sensor interface. Recommended values for these settings when using all 12 conversion stages on the AD7143 are

$AVG\_FP\_SKIP = 00 = \text{skip 3 samples}$

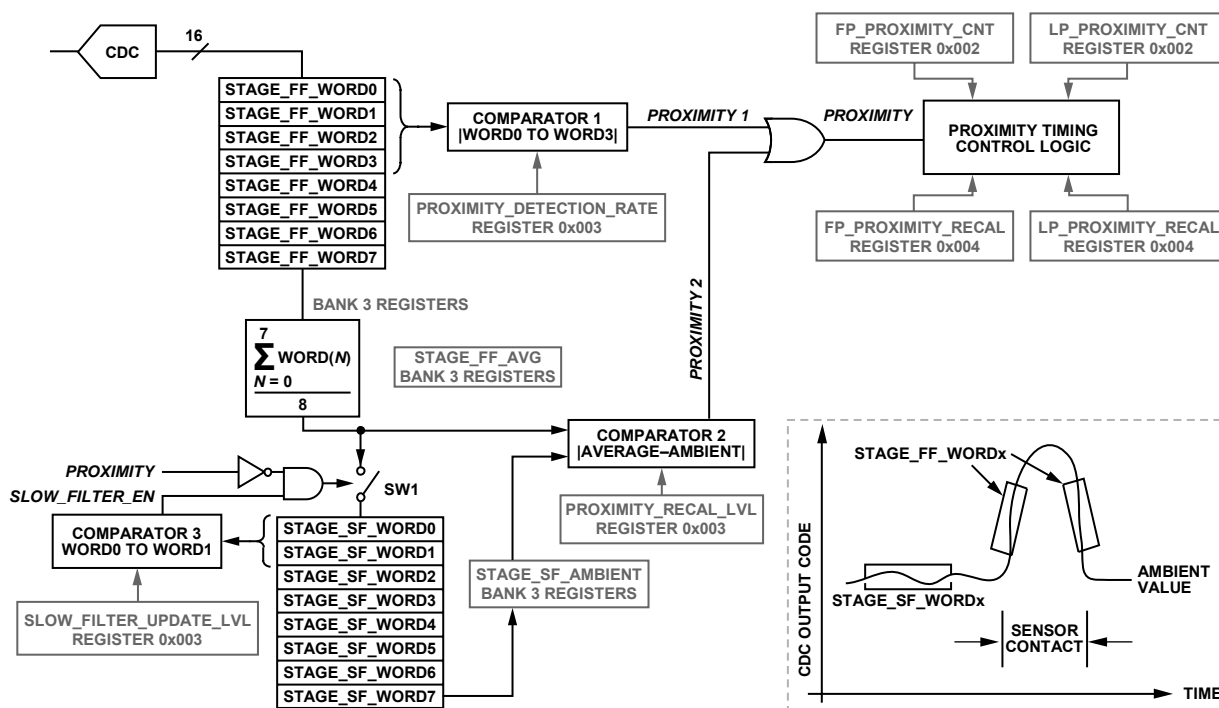
$AVG\_LP\_SKIP = 00 = \text{no samples skipped}$

### SLOW\_FILTER\_UPDATE\_LVL

The SLOW\_FILTER\_UPDATE\_LVL controls whether or not the most recent CDC measurement goes into the slow FIFO (slow filter). The slow filter is updated when the difference between the current CDC value and last value pushed into the slow FIFO is greater than SLOW\_FILTER\_UPDATE\_LVL. This variable is in Ambient Control Register 1, at Address 0x003.

Table 11. FF\_SKIP\_CNT Settings

| FF_SKIP_CNT | FAST FIFO Update Rate  |  |
|-------------|--|--|
|             | Decimation = 128   | Decimation = 256   |
| 0           | $1.525 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$  | $3.072 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$  |
| 1           | $3.072 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$  | $6.144 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$  |
| 2           | $4.608 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$  | $9.216 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$  |
| 3           | $6.144 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$  | $12.288 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$ |
| 4           | $7.68 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$   | $15.25 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$  |
| 5           | $9.216 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$  | $18.432 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$ |
| 6           | $10.752 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$ | $21.504 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$ |
| 7           | $12.288 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$ | $24.576 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$ |
| 8           | $13.824 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$ | $27.648 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$ |
| 9           | $15.25 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$  | $30.72 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$  |
| 10          | $16.896 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$ | $33.792 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$ |
| 11          | $18.432 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$ | $25.864 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$ |
| 12          | $19.968 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$ | $39.925 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$ |
| 13          | $21.504 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$ | $43.008 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$ |
| 14          | $23.04 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$  | $46.08 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$  |
| 15          | $24.576 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$ | $49.152 \times (\text{SEQUENCE\_STAGE\_NUM} + 1) \text{ ms}$ |



## NOTES

1. *SLOW\_FILTER\_EN* IS SET AND *SW1* IS CLOSED WHEN  $|STAGE\_SF\_WORD\ 0\ TO\ STAGE\_SF\_WORD\ 1|$  EXCEEDS THE VALUE PROGRAMMED IN THE *SLOW\_FILTER\_UPDATE\_LVL* REGISTER PROVIDING *PROXIMITY* IS NOT SET.
2. *PROXIMITY 1* IS SET WHEN  $|STAGE\_FF\_WORD\ 0\ TO\ STAGE\_FF\_WORD\ 3|$  EXCEEDS THE VALUE PROGRAMMED IN THE *PROXIMITY\_DETECTION\_RATE* REGISTER.
3. *PROXIMITY 2* IS SET WHEN  $|AVERAGE-AMBIENT|$  EXCEEDS THE VALUE PROGRAMMED IN THE *PROXIMITY\_RECAL\_LVL* REGISTER.
4. DESCRIPTION OF COMPARATOR FUNCTIONS:  
 COMPARATOR 1: USED TO DETECT WHEN A USER IS APPROACHING OR LEAVING A SENSOR.  
 COMPARATOR 2: USED TO DETECT WHEN A USER IS HOVERING OVER A SENSOR, OR APPROACHING A SENSOR VERY SLOWLY.  
 ALSO USED TO DETECT IF THE SENSOR AMBIENT LEVEL HAS CHANGED AS A RESULT OF THE USER INTERACTION.  
 FOR EXAMPLE, HUMIDITY OR DIRT LEFT BEHIND ON SENSOR.  
 COMPARATOR 3: USED TO ENABLE THE SLOW FILTER UPDATE RATE. THE SLOW FILTER IS UPDATED WHEN *SLOW\_FILTER\_EN* IS SET AND *PROXIMITY* IS NOT SET.

Figure 31. AD7143 Proximity Detection and Environmental Calibration

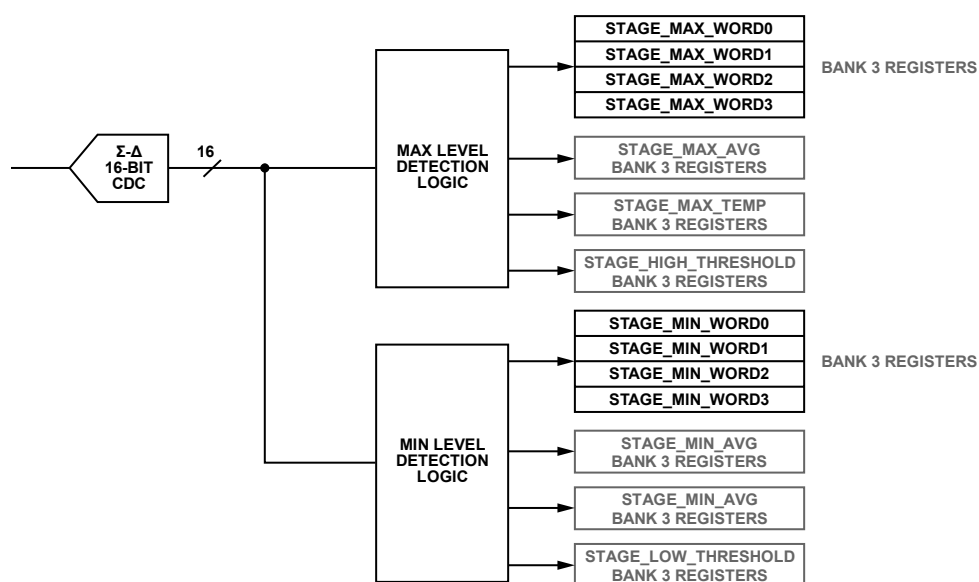


Figure 32. AD7143 Maximum and Minimum Level Detection Logic

## ENVIRONMENTAL CALIBRATION

The AD7143 provides on-chip capacitance sensor calibration to automatically adjust for environmental conditions that have an effect on the capacitance sensor ambient levels. Capacitance sensor output levels are sensitive to temperature, humidity, and in some cases, dirt. The AD7143 achieves optimal and reliable sensor performance by continuously monitoring the CDC ambient levels and correcting for any changes by adjusting the `STAGE_HIGH_THRESHOLD` and `STAGE_LOW_THRESHOLD` register values as described in Equation 1 and Equation 2. The CDC ambient level is defined as the capacitance sensor output level during periods when the user is not approaching or in contact with the sensor.

The compensation logic runs automatically on every conversion after configuration when the AD7143 is not being touched. This allows the AD7143 to account for rapidly changing environmental conditions.

The ambient compensation control registers located at Address 0x002, Address 0x003 and Address 0x004 give the host access to general setup and controls for the compensation algorithm. The RAM stores the compensation data for each conversion stage, as well as setup information specific to each stage.

Figure 33 shows an example of an ideal capacitance sensor behavior where the CDC ambient level remains constant regardless of the environmental conditions. The CDC output shown is for a pair of differential button sensors, where one sensor caused an increase, and the other a decrease in measured capacitance when activated.

The positive and negative sensor threshold levels are calculated as a percentage of the `STAGE_OFFSET_HIGH` and `STAGE_OFFSET_LOW` values based on the threshold sensitivity settings and the ambient value. These values for this example are sufficient to detect a sensor contact, resulting with the AD7143 asserting the `INT` output when the threshold levels are exceeded.

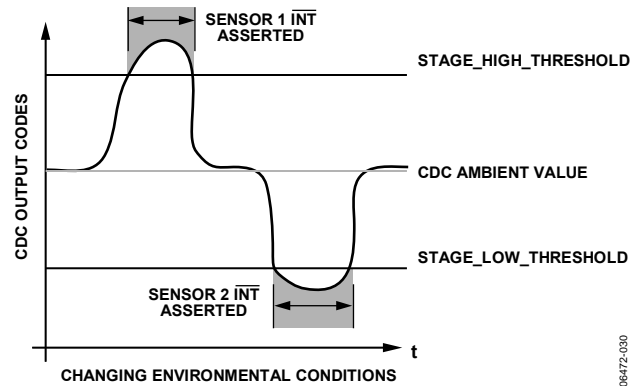


Figure 33. Ideal Sensor Behavior with a Constant Ambient Level

## CAPACITANCE SENSOR BEHAVIOR WITHOUT CALIBRATION

Figure 34 shows the typical behavior of a capacitance sensor with no applied calibration. This figure shows ambient levels drifting over time as environmental conditions change. The ambient level drift has resulted in the detection of a missed user contact on Sensor 2.

This is a result of the initial `STAGE_LOW_THRESHOLD` remaining constant while the ambient levels drifted upward beyond the detection range. The Capacitance Sensor Behavior with Calibration section describes how the AD7143 adaptive calibration algorithm prevents errors such as this from occurring.

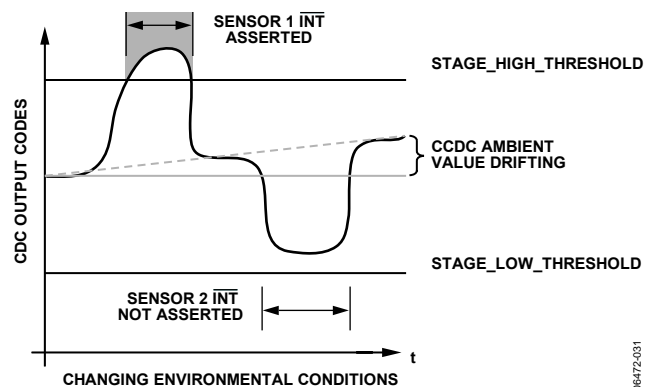


Figure 34. Typical Sensor Behavior without Calibration Applied

## CAPACITANCE SENSOR BEHAVIOR WITH CALIBRATION

The AD7143 on-chip adaptive calibration algorithm prevents sensor detection errors, such as the one shown in Figure 34. This is achieved by monitoring the CDC ambient levels and readjusting the initial STAGE\_OFFSET\_HIGH and STAGE\_OFFSET\_LOW values according to the amount of ambient drift measured on each sensor.

The internal STAGE\_HIGH\_THRESHOLD and STAGE\_LOW\_THRESHOLD values, shown in Equation 1 and Equation 2, are automatically updated based on the new STAGE\_OFFSET\_HIGH and STAGE\_OFFSET\_LOW values. This closed-loop routine ensures the reliability and repeatable operation of every sensor connected to the AD7143 under dynamic environmental conditions. Figure 35 shows a simplified example of how the AD7143 applies the adaptive calibration process resulting in no interrupt errors under changing CDC ambient levels due to environmental conditions.

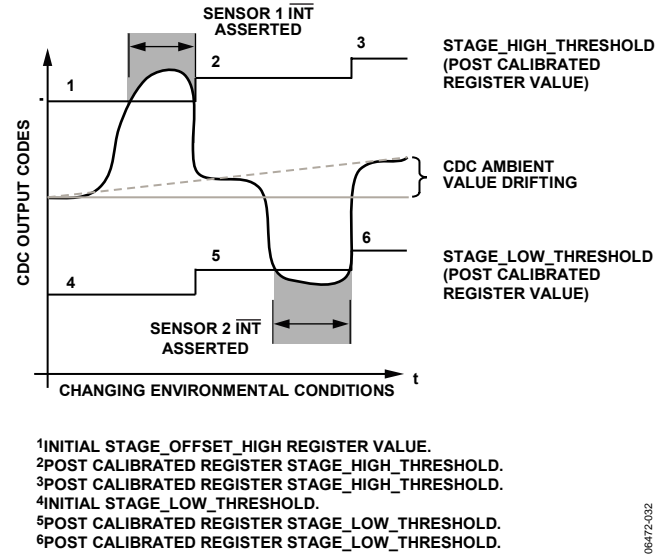


Figure 35. Typical Sensor Behavior with Calibration Applied on the Data Path

### On-Chip Logic Stage High Threshold Calculation

$$\text{STAGE\_HIGH\_THRESHOLD} = \text{STAGE\_SF\_AMBIENT} + \left( \frac{\text{STAGE\_OFFSET\_HIGH}}{4} \right) + \left( \frac{\left( \frac{\text{STAGE\_OFFSET\_HIGH} - \frac{\text{STAGE\_OFFSET\_HIGH}}{4}}{16} \right)}{16} \right) \times \text{POS\_THRESHOLD\_SENSITIVITY} \quad (1)$$

### On-Chip Logic Stage Low Threshold Calculation

$$\text{STAGE\_LOW\_THRESHOLD} = \text{STAGE\_SF\_AMBIENT} + \left( \frac{\text{STAGE\_OFFSET\_LOW}}{4} \right) + \left( \frac{\left( \frac{\text{STAGE\_OFFSET\_LOW} - \frac{\text{STAGE\_OFFSET\_LOW}}{4}}{16} \right)}{16} \right) \times \text{NEG\_THRESHOLD\_SENSITIVITY} \quad (2)$$



Table 12. Additional Information about Environmental Calibration and Adaptive Threshold Registers

| Register                  | Location | Description  |
|---------------------------|----------|--|
| NEG_THRESHOLD_SENSITIVITY | Bank 2   | Used in Equation 2. This value is programmed once at start up.   |
| NEG_PEAK_DETECT           | Bank 2   | Used by Internal Adaptive Threshold Logic Only. The NEG_PEAK_DETECT is set to a percentage of the difference between the ambient CDC value and the minimum average CDC value. If the output of the CDC gets within the NEG_PEAK_DETECT percentage of the minimum average, only then is the minimum average value updated.  |
| POS_THRESHOLD_SENSITIVITY | Bank 2   | Used in Equation 1. This value is programmed once at startup.  |
| POS_PEAK_DETECT           | Bank 2   | Used by Internal Adaptive Threshold Logic Only. The POS_PEAK_DETECT is set to a percentage of the difference between the ambient CDC value, and the maximum average CDC value. If the output of the CDC gets within the POS_PEAK_DETECT percentage of the minimum average, only then is the maximum average value updated.   |
| STAGE_OFFSET_LOW          | Bank 2   | Used in Equation 2. An initial value (based on sensor characterization) is programmed into this register at startup. The AD7143 on-chip calibration algorithm automatically updates this register based on the amount of sensor drift due to changing ambient conditions. Set to 80% of the STAGE_OFFSET_LOW_CLAMP value.  |
| STAGE_OFFSET_HIGH         | Bank 2   | Used in Equation 1. An initial value (based on sensor characterization) is programmed into this register at startup. The AD7143 on-chip calibration algorithm automatically updates this register based on the amount of sensor drift due to changing ambient conditions. Set to 80% of the STAGE_OFFSET_HIGH_CLAMP value.   |
| STAGE_OFFSET_HIGH_CLAMP   | Bank 2   | Used by Internal Environmental Calibration and Adaptive Threshold Algorithms Only. An initial value (based on sensor characterization) is programmed into this register at startup. The value in this register prevents a user from causing a sensor output value to exceed the expected nominal value. Set to the maximum expected sensor response, maximum change in CDC output code.  |
| STAGE_OFFSET_LOW_CLAMP    | Bank 2   | Used by Internal Environmental Calibration and Adaptive Threshold Algorithms Only. An initial value (based on sensor characterization) is programmed into this register at startup. The value in this register prevents a user from causing a sensor output value to exceed the expected nominal value. Set to the minimum expected sensor response, minimum change in CDC output code . |
| STAGE_SF_AMBIENT          | Bank 3   | Used in Equation 1 and Equation 2. This is the ambient sensor output, when the sensor is not touched, as calculated using the slow FIFO.   |
| STAGE_HIGH_THRESHOLD      | Bank 3   | Equation 1 Value.  |
| STAGE_LOW_THRESHOLD       | Bank 3   | Equation 2 Value.  |



## ADAPTIVE THRESHOLD AND SENSITIVITY

The AD7143 provides an on-chip self-learning adaptive threshold and sensitivity algorithm. This algorithm continuously monitors the output levels of each sensor and automatically rescales the threshold levels proportionally to the sensor area covered by the user. As a result, the AD7143 maintains optimal threshold and sensitivity levels for all types of users regardless of their finger sizes.

The threshold level is always referenced from the ambient level and is defined as the CDC converter output level that must be exceeded for a valid sensor contact. The sensitivity level is defined as how sensitive the sensor is before a valid contact is registered.

Figure 36 provides an example of how the adaptive threshold and sensitivity algorithm works. The positive and negative sensor threshold levels are calculated as a percentage of the `STAGE_OFFSET_HIGH` and `STAGE_OFFSET_LOW` values based on the threshold sensitivity settings and the ambient value.

On configuration, initial estimates are supplied for both `STAGE_OFFSET_HIGH` and `STAGE_OFFSET_LOW` after which the calibration engine automatically adjusts the `STAGE_HIGH_THRESHOLD` and `STAGE_LOW_THRESHOLD` values for sensor response.

Reference A in Figure 36 shows an under sensitive threshold level for a small finger user, demonstrating the disadvantages of a fixed threshold level. By enabling the adaptive threshold and sensitivity algorithm, the positive and negative threshold levels are determined by the `POS_THRESHOLD_SENSITIVITY` and `NEG_THRESHOLD_SENSITIVITY` register values and the most recent average maximum sensor output value. These registers can be used to select 16 different positive and negative sensitivity levels ranging between 25% and 95.32% of the most recent average maximum output level referenced from the ambient value. The smaller the sensitivity percentage setting, the easier it is to trigger a sensor activation. Reference B shows that the positive adaptive threshold level is set at almost mid-sensitivity with a 62.51% threshold level by setting `POS_THRESHOLD_SENSITIVITY = 1000`. Figure 36 also provides a similar example for the negative threshold level with `NEG_THRESHOLD_SENSITIVITY = 0001`.

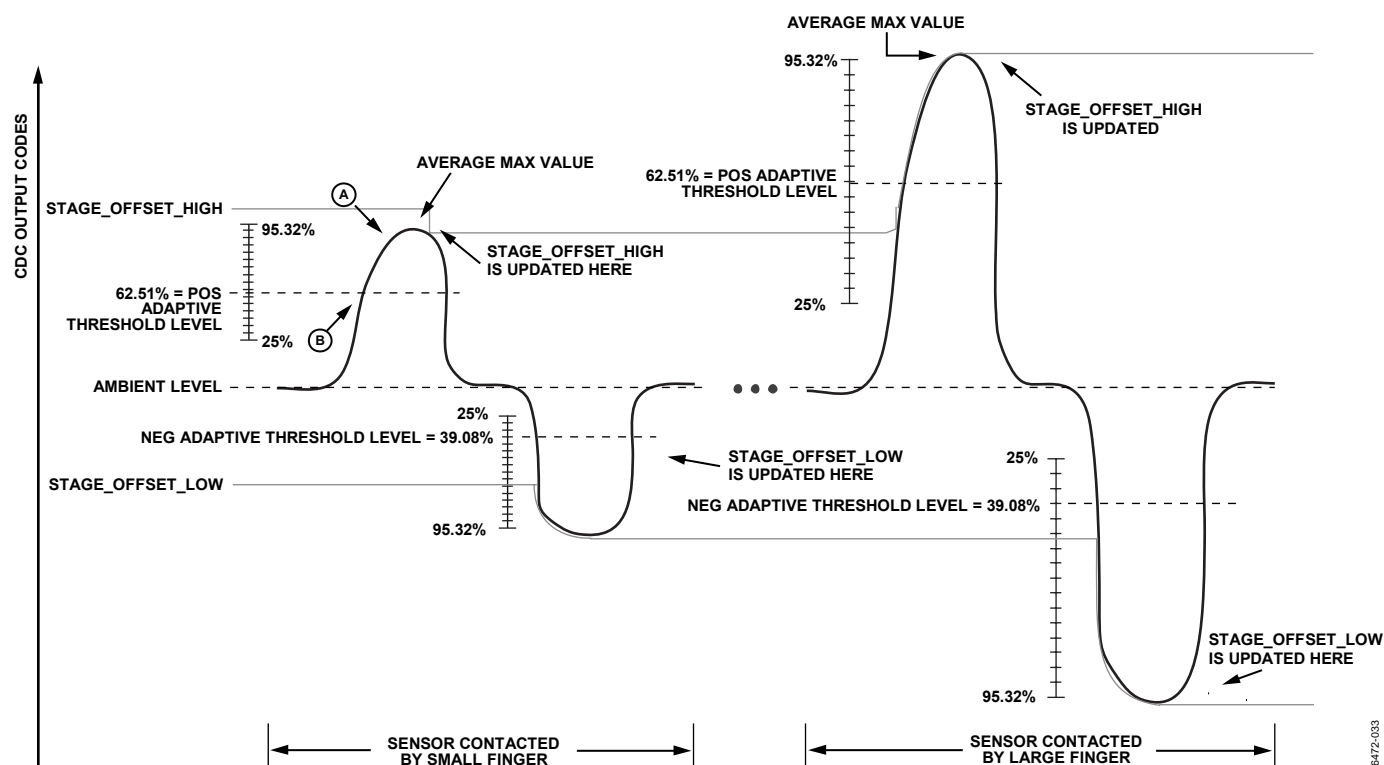


Figure 36. Threshold Sensitivity Example with `POS_THRESHOLD_SENSITIVITY = 1000` and `NEG_THRESHOLD_SENSITIVITY = 0011`

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## INTERRUPT OUTPUT

The AD7143 has an interrupt output that triggers an interrupt service routine on the host processor. The  $\overline{\text{INT}}$  signal is on Pin 14, and is an open-drain output. There are two types of interrupt events on the AD7143: a CDC conversion complete interrupt and a sensor touch interrupt. Each interrupt has enable and status registers described in Table 13. The conversion complete and sensor threshold interrupts can be enabled on a per conversion stage basis. The status registers indicate what type of interrupt triggered the  $\overline{\text{INT}}$  pin. Status registers are cleared, and the  $\overline{\text{INT}}$  signal is reset high, during a read operation of the interrupt status registers. The signal returns high as soon as the read address has been set up.

### CDC CONVERSION COMPLETE INTERRUPT

The AD7143 interrupt signal asserts low to indicate the completion of a conversion stage, and new conversion result data is available in the registers.

The interrupt can be independently enabled for each conversion stage. Each conversion stage complete interrupt can be enabled via the `STAGE_COMPLETE_EN` register (Address 0x007). This register has a bit that corresponds to each conversion stage. Setting this bit to 1 enables the interrupt for that stage. Clearing this bit to 0 disables the conversion complete interrupt for that stage. Figure 38 shows an end of conversion interrupt timing with the `STAGE0` interrupt enabled.

In normal operation, the AD7143's interrupt is enabled only for the last stage in a conversion sequence as shown in Figure 38.

Register 0x00A is the conversion complete interrupt status register. Each bit in this register corresponds to a conversion stage. If a bit is set, it means that the conversion complete interrupt for the corresponding stage was triggered. This register is cleared on a read, provided the underlying condition that triggered the interrupt has gone away.

### SENSOR TOUCH INTERRUPT

The sensor touch interrupt mode is implemented when the host processor requires an interrupt only when a sensor is contacted.

Configuring the AD7143 into this mode results in the interrupt being asserted when the user makes contact with the sensor and again when the user lifts off the sensor. The second interrupt is required to alert the host processor that the user is no longer contacting the sensor.

The registers located at Address 0x005 and Address 0x006 are used to enable the interrupt output for each stage. The registers located at Address 0x008 and Address 0x009 are used to read back the interrupt status for each stage.

Figure 37 shows the interrupt output timing during contact with one of the sensors connected to `STAGE0` while operating in the sensor touch interrupt mode. For a low limit configuration, the interrupt output is asserted as soon as the sensor is contacted and again after the user has stopped contacting the sensor.

Note that the interrupt output remains low until the host processor reads back the interrupt status registers located at Address 0x008 and Address 0x009.

The interrupt output is asserted when there is a change in the threshold status bits. This could indicate that a user is now touching the sensor(s) for the first time, the number of sensors being touched has changed, or the user is no longer touching the sensor(s). Reading the status bits in the interrupt status register shows the current sensor activations.

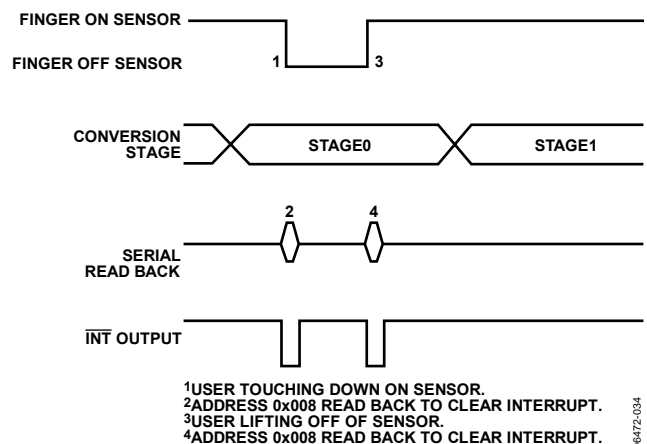
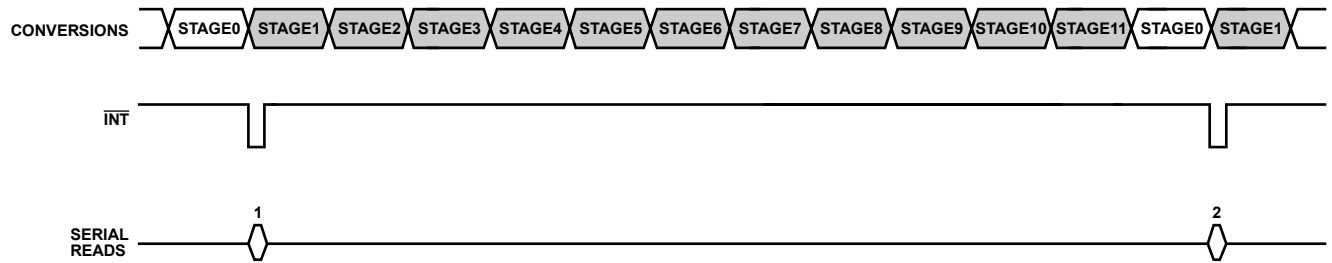


Figure 37. Example of Sensor Touch Interrupt

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Table 13. Interrupt Mode Registers

| Interrupt Mode          | Interrupt Enable Register Address | Interrupt Status Register Address | Notes  |
|-------------------------|-----------------------------------|-----------------------------------|--|
| Sensor Touch            |                                   |                                   | Interrupt asserted when the user contacts a sensor. See Figure 37. |
| Low                     | 0x005                             | 0x008                             | Enable for the CIN inputs connected to the CDC positive stage.     |
| High                    | 0x006                             | 0x009                             | Enable for the CIN inputs connected to the CDC negative stage.     |
| CDC Conversion Complete | 0x007                             | 0x00A                             | Continuous interrupt at the end of each STAGEx that is enabled.    |



## NOTES

1. THIS IS AN EXAMPLE OF A CDC CONVERSION COMPLETE INTERRUPT.
2. THIS TIMING EXAMPLE SHOWS THAT THE INTERRUPT OUTPUT HAS BEEN ENABLED TO BE ASSERTED AT THE END OF A CONVERSION CYCLE FOR STAGE0 ONLY.
3. STAGEx CONFIGURATION PROGRAMMING NOTES FOR STAGE0, STAGE5, AND STAGE9 (x = 0, 5, 9)  
 STAGEx\_LOW\_INT\_EN (ADDRESS 0x005) = 0  
 STAGEx\_HIGH\_INT\_EN (ADDRESS 0x006) = 0  
 STAGEx\_COMPLETE\_EN (ADDRESS 0x007) = 1

Figure 38. Example of Configuring the Registers for End of Conversion Interrupt Setup

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## SERIAL INTERFACE

The AD7143 is available with a fixed address I<sup>2</sup>C-compatible interface.

### I<sup>2</sup>C COMPATIBLE INTERFACE

The AD7143 supports the industry standard 2-wire I<sup>2</sup>C serial interface protocol. The two wires associated with the I<sup>2</sup>C timing are the SCLK and the SDA inputs. The SDA is an I/O pin that allows both register write and register readback operations. The AD7143 is always a slave device on the I<sup>2</sup>C serial interface bus.

The AD7143 has a single fixed 7-bit device address, Address 0101 110. The AD7143 responds when the master device sends its device address over the bus. The AD7143 cannot initiate data transfers on the bus.

**Table 14. AD7143 I<sup>2</sup>C Fixed Device Address**

| DEV<br>A6 | DEV<br>A5 | DEV<br>A4 | DEV<br>A3 | DEV<br>A2 | DEV<br>A1 | DEV<br>A0 |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 0         | 1         | 0         | 1         | 1         | 1         | 0         |

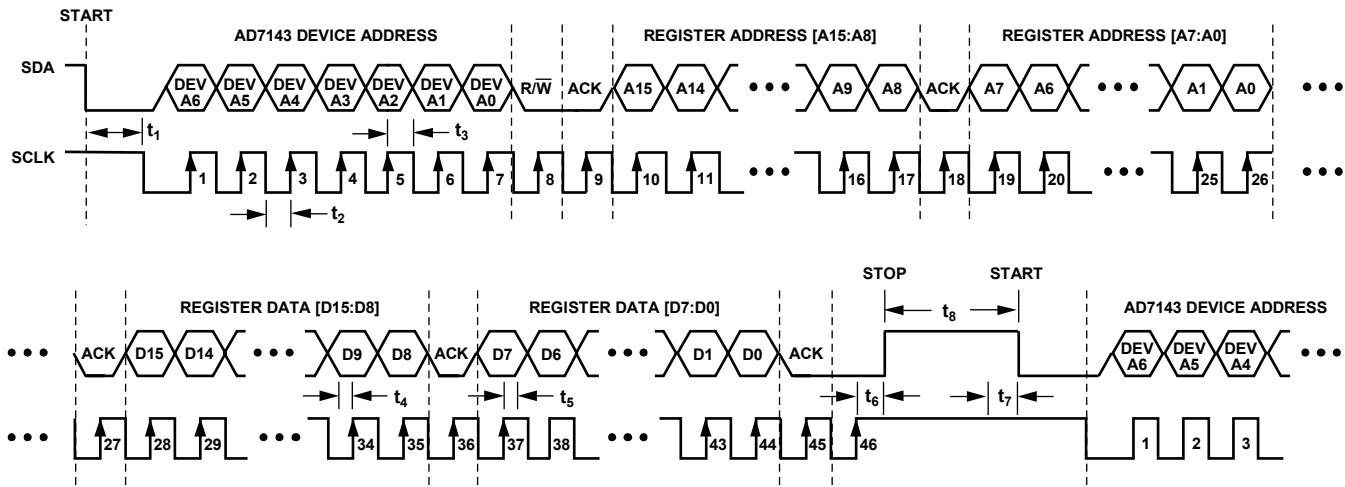
### Data Transfer

Data is transferred over the I<sup>2</sup>C serial interface in 8-bit bytes. The master initiates a data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line, SDA, while the serial clock line, SCLK, remains high. This indicates that an address/data stream follows.

All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/W bit that determines the direction of the data transfer. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as the acknowledge bit. All other devices on the bus now remain idle while the selected device waits for data to be read from, or written to it. If the R/W bit is a 0, the master writes to the slave device. If the R/W bit is a 1, the master reads from the slave device.

Data is sent over the serial bus in a sequence of nine clock pulses, eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, since a low-to-high transition when the clock is high can be interpreted as a stop signal. The number of data bytes transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

When all data bytes are read or written, a stop condition is established. A stop condition is defined by a low-to-high transition on SDA while SCLK remains high. If the AD7143 encounters a stop condition, it returns to its idle condition, and the address pointer register resets to Address 0x00.



#### NOTES

1. A START CONDITION AT THE BEGINNING IS DEFINED AS A HIGH-TO-LOW TRANSITION ON SDA WHILE SCLK REMAINS HIGH.
2. A STOP CONDITION AT THE END IS DEFINED AS A LOW-TO-HIGH TRANSITION ON SDA WHILE SCLK REMAINS HIGH.
3. 7-BIT DEVICE ADDRESS [DEV A6:DEV A0] = [0 1 0 1 1 1 0].
4. 16-BIT REGISTER ADDRESS [A15:A0] = [X, X, X, X, X, X, X, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0], WHERE X ARE DON'T CARE BITS.
5. REGISTER ADDRESS [A15:A8] AND REGISTER ADDRESS [A7:A0] ARE ALWAYS SEPARATED BY A LOW ACK BIT.
6. REGISTER DATA [D15:D8] AND REGISTER DATA [D7:D0] ARE ALWAYS SEPARATED BY A LOW ACK BIT.

Figure 39. Example of I<sup>2</sup>C Timing for Single Register Write Operation

### Writing Data over the I<sup>2</sup>C Bus

The process for writing to the AD7143 over the I<sup>2</sup>C bus is shown in Figure 39 and Figure 41. The device address is sent over the bus followed by the  $\overline{R/\overline{W}}$  bit set to 0. This is followed by two bytes of data that contain the 10-bit address of the internal data register to be written. The following bit map shows the upper register address bytes. Note that Bit 7 to Bit 2 in the upper address byte are don't care bits. The address is contained in the 10 LSBs of the register address bytes.

| MSB |   |   |   |   |   | LSB                    |                        |
|-----|---|---|---|---|---|------------------------|------------------------|
| 7   | 6 | 5 | 4 | 3 | 2 | 1                      | 0                      |
| X   | X | X | X | X | X | Register Address Bit 9 | Register Address Bit 8 |

The following bit map shows the lower register address bytes.

| MSB              |                  |                  |                  |                  |                  | LSB              |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| 7                | 6                | 5                | 4                | 3                | 2                | 1                | 0                |
| Reg. Addr. Bit 7 | Reg. Addr. Bit 6 | Reg. Addr. Bit 5 | Reg. Addr. Bit 4 | Reg. Addr. Bit 3 | Reg. Addr. Bit 2 | Reg. Addr. Bit 1 | Reg. Addr. Bit 0 |

The third data byte contains the 8 MSBs of the data to be written to the internal register. The fourth data byte contains the 8 LSBs of data to be written to the internal register.

The AD7143 address pointer register automatically increments after each write. This allows the master to sequentially write to all registers on the AD7143 in the same write transaction. However, the address pointer register does not wrap around after the last address.

Any data written to the AD7143 after the address pointer has reached its maximum value is discarded.

All registers on the AD7143 are 16-bit. Two consecutive 8-bit data bytes are combined and written to the 16-bit registers. To avoid errors, all writes to the device must contain an even number of data bytes.

To finish the transaction, the master generates a stop condition on SDA, or generates a repeat start condition if the master is to maintain control of the bus.

### Reading Data over the I<sup>2</sup>C Bus

To read from the AD7143, the address pointer register must first be set to the address of the required internal register. The master performs a write transaction, and writes to the AD7143 to set the address pointer. The master then outputs a repeat start condition to keep control of the bus, or, if this is not possible, ends the write transaction with a stop condition. A read transaction is initiated, with the  $\overline{R/\overline{W}}$  bit set to 1.

The AD7143 supplies the upper eight bits of data from the addressed register in the first readback byte, followed by the lower eight bits in the next byte. This is shown in Figure 40 and Figure 41.

Because the address pointer automatically increases after each read, the AD7143 continues to output readback data until the master puts a no acknowledge and stop condition on the bus. If the address pointer reaches its maximum value, and the master continues to read from the part, the AD7143 repeatedly sends data from the last register addressed.



## NOTES

1. A START CONDITION AT THE BEGINNING IS DEFINED AS A HIGH-TO-LOW TRANSITION ON SDA WHILE SCLK REMAINS HIGH.
2. A STOP CONDITION AT THE END IS DEFINED AS A LOW-TO-HIGH TRANSITION ON SDA WHILE SCLK REMAINS HIGH.
3. THE MASTER GENERATES THE ACK AT THE END OF THE READBACK TO SIGNAL THAT IT DOES NOT WANT ADDITIONAL DATA.
4. 7-BIT DEVICE ADDRESS [DEV A6:DEV A0] = [0 1 0 1 1 1 0].
5. 16-BIT REGISTER ADDRESS[A15:A0] = [X, X, X, X, X, X, X, X, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0], WHERE THE UPPER LSB Xs ARE DON'T CARE BITS.
6. REGISTER ADDRESS [A15:A8] AND REGISTER ADDRESS [A7:A0] ARE ALWAYS SEPARATED BY LOW ACK BITS.
7. REGISTER DATA [D15:D8] AND REGISTER DATA [D7:D0] ARE ALWAYS SEPARATED BY A LOW ACK BIT.
8. THE R/W BIT IS SET TO A1 TO INDICATE A READBACK OPERATION.

Figure 40. Example of I²C Timing for Single Register Readback Operation

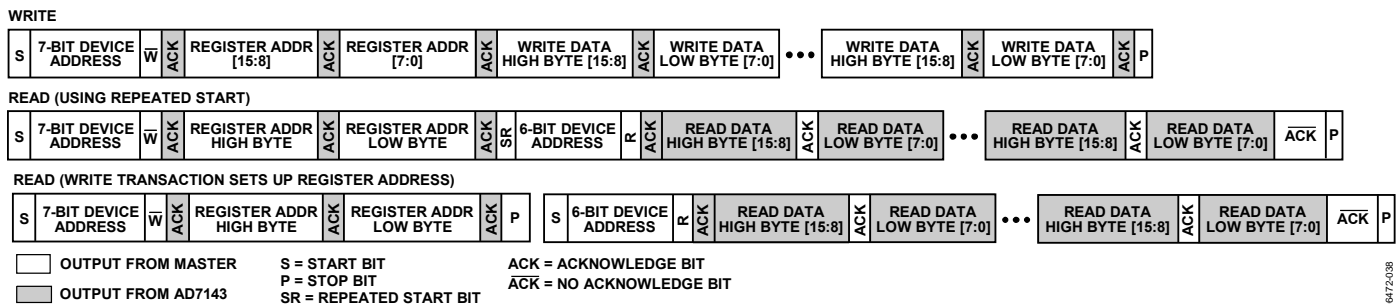


Figure 41. Example of Sequential I²C Write and Readback Operation

## PCB DESIGN GUIDELINES

### CAPACITIVE SENSOR BOARD MECHANICAL SPECIFICATIONS

Table 15.

| Parameter  | Symbol            | Min | Typ | Max | Unit |
|--|-------------------|-----|-----|-----|------|
| Distance from Edge of Any Sensor to Edge of Metal Object   | $D_1$             | 1.0 |     |     | mm   |
| Distance Between Sensor Edges <sup>1</sup>   | $D_2 = D_3 = D_4$ | 0   |     |     | mm   |
| Distance Between Bottom of Sensor Board and Controller Board or Metal Casing <sup>2</sup> (4-Layer, 2-Layer, and Flex Circuit) | $D_5$             |     | 1.0 |     | mm   |

<sup>1</sup> The distance is dependent on the application and the positioning of the switches relative to each other and with respect to the user's finger positioning and handling. Adjacent sensors, with 0 minimum space between them, are implemented differentially.

<sup>2</sup> The 1.0 mm specification is meant to prevent direct sensor board contact with any conductive material. This specification does not guarantee no EMI coupling from the controller board to the sensors. Address potential EMI coupling issues by placing a grounded metal shield between the capacitive sensor board and the main controller board as shown in Figure 44.

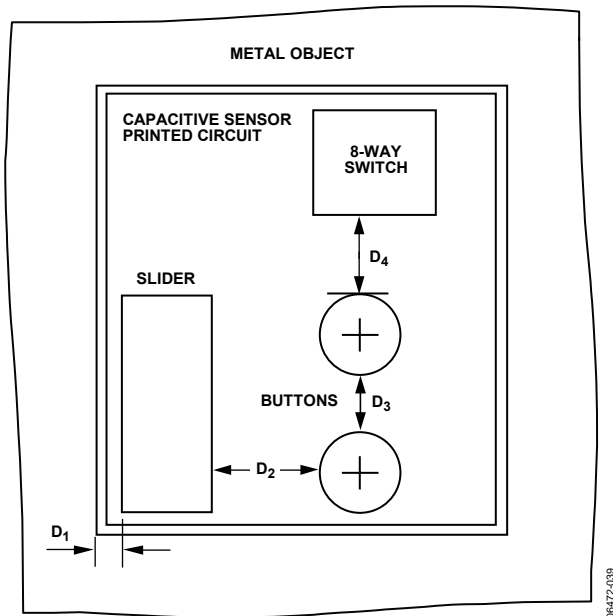


Figure 42. Capacitive Sensor Board Mechanicals Top View

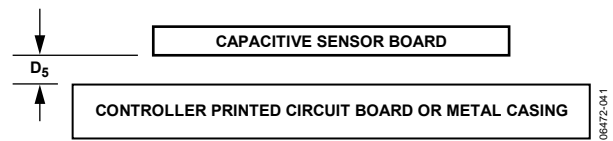


Figure 44. Capacitive Sensor Board with Grounded Shield

### CHIP SCALE PACKAGES

The lands on the chip scale package (CP-16-13) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length, and 0.05 mm wider than the package land width. Center the land on the pad to maximize the solder joint size.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. To avoid shorting, provide a clearance of at least 0.25 mm between the thermal pad and the inner edges of the land pattern on the printed circuit board.

Thermal vias can be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at a 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. copper to plug the via.

Connect the printed circuit board thermal pad to GND.

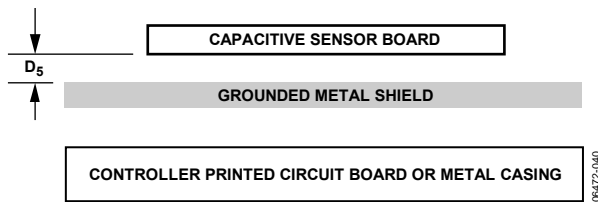


Figure 43. Capacitive Sensor Board Mechanicals Side View

## POWER-UP SEQUENCE

When the AD7143 is powered up, the following sequence is recommended when initially developing the AD7143 and Host  $\mu$ C serial interface:

1. Turn on the power supplies to the AD7143.
  2. Write to the Bank 2 registers at Address 0x080 through Address 0x0DF. These registers are contiguous, so a sequential register write sequence can be applied.
- Note: The Bank 2 register values are unique for each application. Register values are provided by Analog Devices after the sensor board has been developed.
3. Write to the Bank 1 registers at Address 0x000 through Address 0x007 as outlined below. These registers are contiguous so a sequential register write sequence can be applied

Caution: At this time, Address 0x001 must remain set to default value 0x0000 during this contiguous write operation.

Register values:

Address 0x000 = 0x00B2

Address 0x001 = 0x0000

Address 0x002 = 0x0690

Address 0x003 = 0x0664

Address 0x004 = 0x290F

Address 0x005 = 0x0000

Address 0x006 = 0x0000

Address 0x007 = 0x0001 (The AD7143 interrupt is asserted approximately every 25 ms.)

4. Write to the Bank 1 register, Address 0x001 = 0x0FFF.
5. Read back the corresponding interrupt status register at Address 0x008, Address 0x009, or Address 0x00A. This is determined by the interrupt output configuration as explained in the Interrupt Output section.

Note: The specific registers required to be readback depend on each application. Analog Devices provides this information after the sensor board has been developed.

6. Repeat Step 5 each time  $\overline{\text{INT}}$  is asserted.

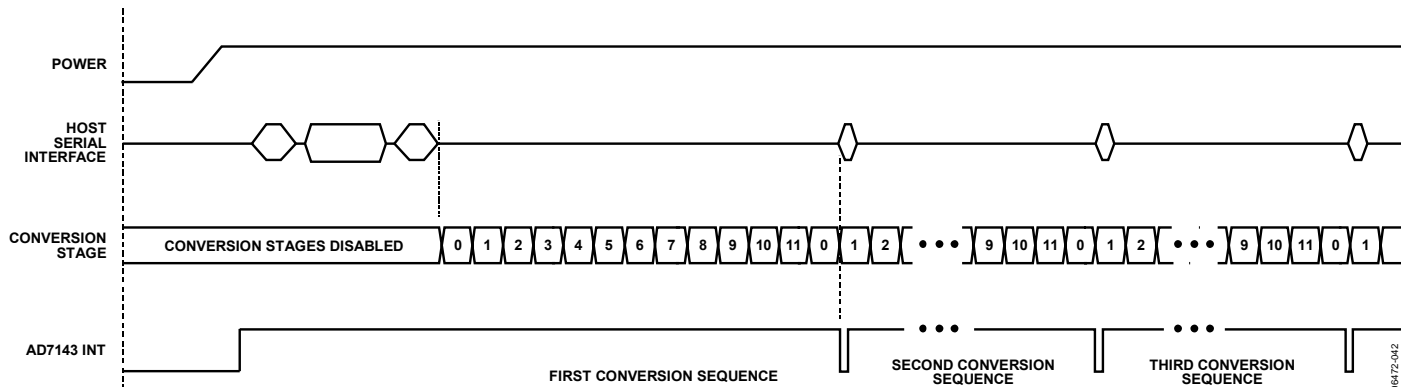


Figure 45. Recommended Start-Up Sequence



## TYPICAL APPLICATION CIRCUITS

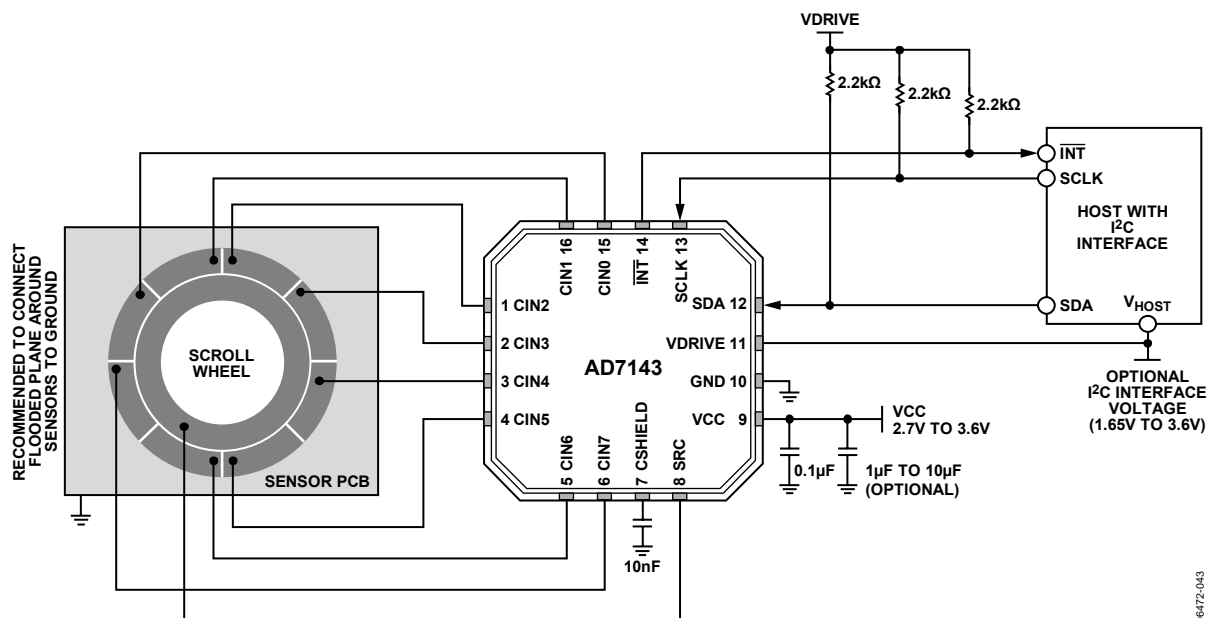


Figure 46. Typical Application Circuit with I²C Interface

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## REGISTER MAP

The AD7143 address space is divided into three different register banks, referred to as Bank 1, Bank 2, and Bank 3. Figure 47 illustrates the division of these three banks.

Bank 1 registers contain control registers, CDC conversion control registers, interrupt enable registers, interrupt status registers, CDC 16-bit conversion data registers, device ID registers, and proximity status registers.

Bank 2 registers contain the configuration registers used for uniquely configuring the CIN inputs for each conversion stage. Initialize the Bank 2 configuration registers immediately after power-up to obtain valid CDC conversion result data.

Bank 3 registers contain the results of each conversion stage. These registers automatically update at the end of each conversion sequence. Although these registers are primarily used by the AD7143 internal data processing, they are accessible by the host processor for additional external data processing, if desired.

Default values are undefined for Bank 2 registers and Bank 3 registers until after power up and configuration of the Bank 2 registers.

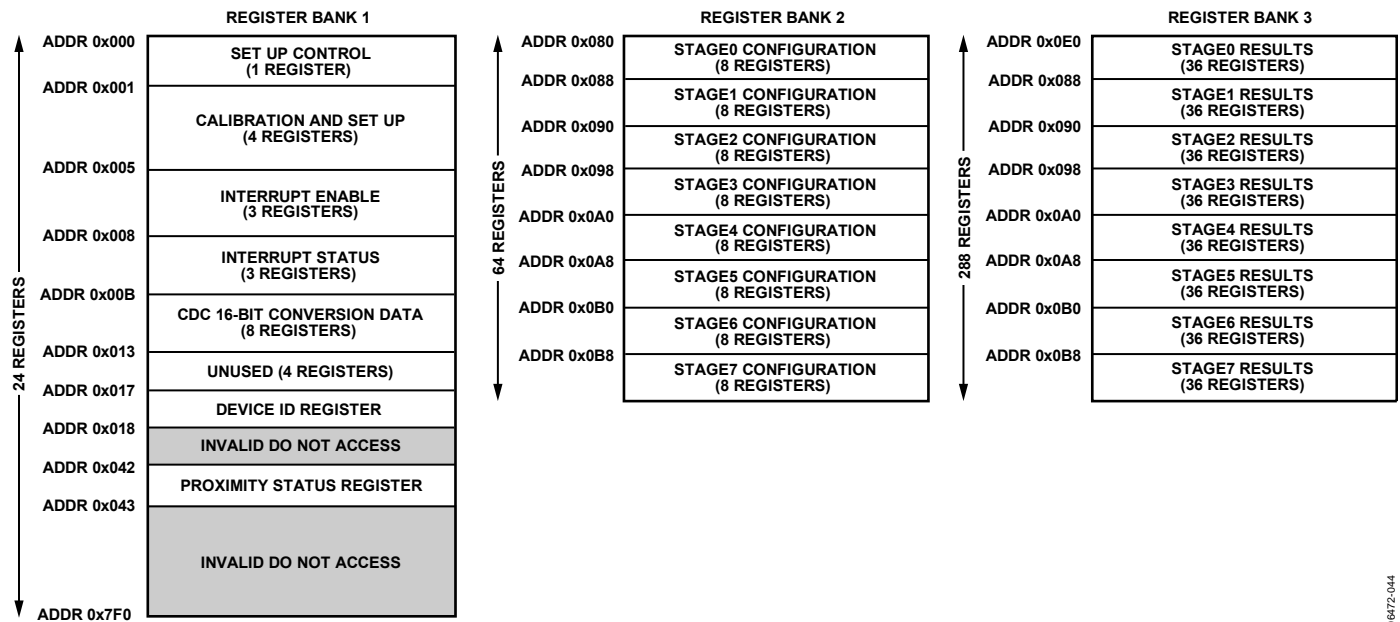


Figure 47. Layout of Bank 1 Registers, Bank 2 Registers, and Bank 3 Registers

## DETAILED REGISTER DESCRIPTIONS

### BANK 1 REGISTERS

All addresses and default values are expressed in hexadecimal format.

Table 16. PWR\_CONTROL Register

| Address | Data Bit | Default | Type | Name               | Description  |
|---------|----------|---------|------|--------------------|--|
| 0x000   | [1:0]    | 0       | R/W  | POWER_MODE         | Operating modes<br>00 = full power mode (normal operation, CDC conversions approximately every 25 ms)<br>01 = full shutdown mode (no CDC conversions)<br>10 = low power mode (automatic wake-up operation)<br>11 = full shutdown mode (no CDC conversions) |
|         | [3:2]    | 0       |      | LP_CONV_DELAY      | Low power mode conversion delay<br>00 = 200 ms<br>01 = 400 ms<br>10 = 600 ms<br>11 = 800 ms  |
|         | [7:4]    | 0       |      | SEQUENCE_STAGE_NUM | Number of stages in sequence (N + 1)<br>0000 = 1 conversion stage in sequence<br>0001 = 2 conversion stages in sequence<br>.....<br>Maximum value = 1011 = 12 conversion stages per sequence   |
|         | [9:8]    | 0       |      | DECIMATION         | ADC decimation factor<br>00 = decimate by 256<br>01 = decimate by 128<br>10 = do not use this setting<br>11 = do not use this setting  |
|         | [10]     | 0       |      | SW_RESET           | Software reset control (self-clearing)<br>1 = resets all registers to default values   |
|         | [11]     | 0       |      | INT_POL            | Interrupt polarity control<br>0 = active low<br>1 = active high  |
|         | [12]     | 0       |      | EXCITATION_SOURCE  | Excitation source control for Pin 15<br>0 = enable output<br>1 = disable output  |
|         | [13]     | 0       |      | Unused             | Set unused register bits = 0   |
|         | [15:14]  | 0       |      | CDC_BIAS           | CDC bias current control<br>00 = normal operation<br>01 = normal operation + 20%<br>10 = normal operation + 35%<br>11 = normal operation + 50%   |

Table 17. STAGE\_CAL\_EN Register

| Address | Data Bit | Default | Type | Name          | Description  |
|---------|----------|---------|------|---------------|--|
| 0x001   | [0]      | 0       | R/W  | STAGE0_CAL_EN | STAGE0 calibration enable<br>0 = disable<br>1 = enable   |
|         | [1]      | 0       |      | STAGE1_CAL_EN | STAGE1 calibration enable<br>0 = disable<br>1 = enable   |
|         | [2]      | 0       |      | STAGE2_CAL_EN | STAGE2 calibration enable<br>0 = disable<br>1 = enable   |
|         | [3]      | 0       |      | STAGE3_CAL_EN | STAGE3 calibration enable<br>0 = disable<br>1 = enable   |
|         | [4]      | 0       |      | STAGE4_CAL_EN | STAGE4 calibration enable<br>0 = disable<br>1 = enable   |
|         | [5]      | 0       |      | STAGE5_CAL_EN | STAGE5 calibration enable<br>0 = disable<br>1 = enable   |
|         | [6]      | 0       |      | STAGE6_CAL_EN | STAGE6 calibration enable<br>0 = disable<br>1 = enable   |
|         | [7]      | 0       |      | STAGE7_CAL_EN | STAGE7 calibration enable<br>0 = disable<br>1 = enable   |
|         | [11:8]   | 0       |      | Unused        | Set unused register bits = 0   |
|         | [13:12]  | 0       |      | AVG_FP_SKIP   | Full power mode skip control<br>00 = skip 3 samples<br>01 = skip 7 samples<br>10 = skip 15 samples<br>11 = skip 31 samples |
|         | [15:14]  | 0       |      | AVG_LP_SKIP   | Low power mode skip control<br>00 = use all samples<br>01 = skip 1 sample<br>10 = skip 2 samples<br>11 = skip 3 samples    |

Table 18. AMB\_COMP\_CTRL0 Register

| Address | Data Bit | Default | Type | Name             | Description  |
|---------|----------|---------|------|------------------|--|
| 0x002   | [3:0]    | 0       | R/W  | FF_SKIP_CNT      | Fast filter skip control (N+1)<br>0000 = no sequence of results are skipped<br>0001 = one sequence of results is skipped for every one allowed into Fast FIFO<br>0010 = two sequences of results are skipped for every one allowed into Fast FIFO<br>1011 = maximum value = 12 sequences of results are skipped for every one allowed into Fast FIFO |
|         | [7:4]    | F       |      | FP_PROXIMITY_CNT | Full power mode proximity period   |
|         | [11:8]   | F       |      | LP_PROXIMITY_CNT | Low power mode proximity period  |
|         | [13:12]  | 0       |      | PWR_DOWN_TIMEOUT | Full power to low power mode time out control<br>00 = $1.25 \times (\text{FP\_PROXIMITY\_CNT})$<br>01 = $1.50 \times (\text{FP\_PROXIMITY\_CNT})$<br>10 = $1.75 \times (\text{FP\_PROXIMITY\_CNT})$<br>11 = $2.00 \times (\text{FP\_PROXIMITY\_CNT})$  |
|         | [14]     | 0       |      | FORCED_CAL       | Forced calibration control<br>0 = normal operation<br>1 = forces all conversion stages to recalibrate  |
|         | [15]     | 0       |      | CONV_RESET       | Conversion reset control (self-clearing)<br>0 = normal operation<br>1 = resets the conversion sequence back to STAGE0  |

Table 19. AMB\_COMP\_CTRL1 Register

| Address | Data Bit | Default | Type | Name                     | Description                   |
|---------|----------|---------|------|--------------------------|-------------------------------|
| 0x003   | [7:0]    | 64      | R/W  | PROXIMITY_RECAL_LVL      | Proximity recalibration level |
|         | [13:8]   | 1       |      | PROXIMITY_DETECTION_RATE | Proximity detection rate      |
|         | [15:14]  | 0       |      | SLOW_FILTER_UPDATE_LVL   | Slow filter update level      |

Table 20. AMB\_COMP\_CTRL2 Register

| Address | Data Bit | Default | Type | Name               | Description  |
|---------|----------|---------|------|--------------------|--|
| 0x004   | [9:0]    | 3FF     | R/W  | FP_PROXIMITY_RECAL | Full power mode proximity recalibration time control |
|         | [15:10]  | 3F      |      | LP_PROXIMITY_RECAL | Low power mode proximity recalibration time control  |

Table 21. STAGE\_LOW\_INT\_EN Register

| Address | Data Bit | Default | Type | Name              | Description  |
|---------|----------|---------|------|-------------------|--|
| 0x005   | [0]      | 0       | R/W  | STAGE0_LOW_INT_EN | STAGE0 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE0 low threshold is exceeded |
|         | [1]      | 0       |      | STAGE1_LOW_INT_EN | STAGE1 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE0 low threshold is exceeded |
|         | [2]      | 0       |      | STAGE2_LOW_INT_EN | STAGE2 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE0 low threshold is exceeded |
|         | [3]      | 0       |      | STAGE3_LOW_INT_EN | STAGE3 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE0 low threshold is exceeded |
|         | [4]      | 0       |      | STAGE4_LOW_INT_EN | STAGE4 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE0 low threshold is exceeded |
|         | [5]      | 0       |      | STAGE5_LOW_INT_EN | STAGE5 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE0 low threshold is exceeded |
|         | [6]      | 0       |      | STAGE6_LOW_INT_EN | STAGE6 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE0 low threshold is exceeded |
|         | [7]      | 0       |      | STAGE7_LOW_INT_EN | STAGE7 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE0 low threshold is exceeded |
|         | [11:8]   | 0       |      | Unused            | Set unused register bits = 0   |
|         | [15:12]  | 0       |      | TESTMODE          | Set test mode register bits = 0 (at all times)   |

Table 22. STAGE\_HIGH\_INT\_EN Register

| Address | Data Bit | Default | Type | Name               | Description  |
|---------|----------|---------|------|--------------------|--|
| 0x006   | [0]      | 0       | R/W  | STAGE0_HIGH_INT_EN | STAGE0 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE0 high threshold is exceeded |
|         | [1]      | 0       |      | STAGE1_HIGH_INT_EN | STAGE1 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE0 high threshold is exceeded |
|         | [2]      | 0       |      | STAGE2_HIGH_INT_EN | STAGE2 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE0 high threshold is exceeded |
|         | [3]      | 0       |      | STAGE3_HIGH_INT_EN | STAGE3 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE0 high threshold is exceeded |
|         | [4]      | 0       |      | STAGE4_HIGH_INT_EN | STAGE4 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE0 high threshold is exceeded |
|         | [5]      | 0       |      | STAGE5_HIGH_INT_EN | STAGE5 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE0 high threshold is exceeded |
|         | [6]      | 0       |      | STAGE6_HIGH_INT_EN | STAGE6 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE0 high threshold is exceeded |
|         | [7]      | 0       |      | STAGE7_HIGH_INT_EN | STAGE7 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE0 high threshold is exceeded |
|         | [15:8]   |         |      | Unused             | Set unused register bits = 0   |

Table 23. STAGE\_COMPLETE\_INT\_EN Register

| Address | Data Bit | Default | Type | Name               | Description   |
|---------|----------|---------|------|--------------------|---|
| 0x007   | [0]      | 0       | R/W  | STAGE0_COMPLETE_EN | STAGE0 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted at completion of STAGE0 conversion |
|         | [1]      | 0       |      | STAGE1_COMPLETE_EN | STAGE1 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted at completion of STAGE1 conversion |
|         | [2]      | 0       |      | STAGE2_COMPLETE_EN | STAGE2 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted at completion of STAGE2 conversion |
|         | [3]      | 0       |      | STAGE3_COMPLETE_EN | STAGE3 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted at completion of STAGE3 conversion |
|         | [4]      | 0       |      | STAGE4_COMPLETE_EN | STAGE4 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted at completion of STAGE4 conversion |
|         | [5]      | 0       |      | STAGE5_COMPLETE_EN | STAGE5 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted at completion of STAGE5 conversion |
|         | [6]      | 0       |      | STAGE6_COMPLETE_EN | STAGE6 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted at completion of STAGE6 conversion |
|         | [7]      | 0       |      | STAGE7_COMPLETE_EN | STAGE7 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted at completion of STAGE7 conversion |
|         | [11:8]   | 0       |      | Unused             | Set unused register bits = 0  |
|         | [12]     | 0       |      | TESTMODE           | Set test mode register bits = 0 at all times  |
|         | [15:13]  |         |      | Unused             | Set unused register bits = 0  |

Table 24. STAGE\_LOW\_LIMIT\_INT Register<sup>1</sup>

| Address | Data Bit | Default | Type | Name                 | Description   |
|---------|----------|---------|------|----------------------|---|
| 0x008   | [0]      | 0       | R    | STAGE0_LOW_LIMIT_INT | STAGE0 CDC conversion low limit interrupt result<br>1 indicates STAGE0_LOW_THRESHOLD value exceeded |
|         | [1]      | 0       |      | STAGE1_LOW_LIMIT_INT | STAGE1 CDC conversion low limit interrupt result<br>1 indicates STAGE1_LOW_THRESHOLD value exceeded |
|         | [2]      | 0       |      | STAGE2_LOW_LIMIT_INT | STAGE2 CDC conversion low limit interrupt result<br>1 indicates STAGE2_LOW_THRESHOLD value exceeded |
|         | [3]      | 0       |      | STAGE3_LOW_LIMIT_INT | STAGE3 CDC conversion low limit interrupt result<br>1 indicates STAGE3_LOW_THRESHOLD value exceeded |
|         | [4]      | 0       |      | STAGE4_LOW_LIMIT_INT | STAGE4 CDC conversion low limit interrupt result<br>1 indicates STAGE4_LOW_THRESHOLD value exceeded |
|         | [5]      | 0       |      | STAGE5_LOW_LIMIT_INT | STAGE5 CDC conversion low limit interrupt result<br>1 indicates STAGE5_LOW_THRESHOLD value exceeded |
|         | [6]      | 0       |      | STAGE6_LOW_LIMIT_INT | STAGE6 CDC conversion low limit interrupt result<br>1 indicates STAGE6_LOW_THRESHOLD value exceeded |
|         | [7]      | 0       |      | STAGE7_LOW_LIMIT_INT | STAGE7 CDC conversion low limit interrupt result<br>1 indicates STAGE7_LOW_THRESHOLD value exceeded |
|         | [15:8]   |         |      | Unused               | Set unused register bits = 0  |

<sup>1</sup> Registers self-clear to 0 after readback, provided that the limits are not exceeded.



Table 25. STAGE\_HIGH\_LIMIT\_INT Register<sup>1</sup>

| Address | Data Bit | Default | Type | Name                  | Description   |
|---------|----------|---------|------|-----------------------|---|
| 0x009   | [0]      | 0       | R    | STAGE0_HIGH_LIMIT_INT | STAGE0 CDC conversion high limit interrupt result<br>1 indicates STAGE0_HIGH_THRESHOLD value exceeded |
|         | [1]      | 0       |      | STAGE1_HIGH_LIMIT_INT | STAGE1 CDC conversion high limit interrupt result<br>1 indicates STAGE1_HIGH_THRESHOLD value exceeded |
|         | [2]      | 0       |      | STAGE2_HIGH_LIMIT_INT | Stage2 CDC conversion high limit interrupt result<br>1 indicates STAGE2_HIGH_THRESHOLD value exceeded |
|         | [3]      | 0       |      | STAGE3_HIGH_LIMIT_INT | STAGE3 CDC conversion high limit interrupt result<br>1 indicates STAGE3_HIGH_THRESHOLD value exceeded |
|         | [4]      | 0       |      | STAGE4_HIGH_LIMIT_INT | STAGE4 CDC conversion high limit interrupt result<br>1 indicates STAGE4_HIGH_THRESHOLD value exceeded |
|         | [5]      | 0       |      | STAGE5_HIGH_LIMIT_INT | STAGE5 CDC conversion high limit interrupt result<br>1 indicates STAGE5_HIGH_THRESHOLD value exceeded |
|         | [6]      | 0       |      | STAGE6_HIGH_LIMIT_INT | STAGE6 CDC conversion high limit interrupt result<br>1 indicates STAGE6_HIGH_THRESHOLD value exceeded |
|         | [7]      | 0       |      | STAGE7_HIGH_LIMIT_INT | STAGE7 CDC conversion high limit interrupt result<br>1 indicates STAGE7_HIGH_THRESHOLD value exceeded |
|         | [15:8]   |         |      | Unused                | 1 indicates STAGE7_HIGH_THRESHOLD value exceeded<br>Set unused register bits = 0                      |

<sup>1</sup> Registers self-clear to 0 after readback, provided that the limits are not exceeded.

Table 26. STAGE\_COMPLETE\_LIMIT\_INT Register<sup>1</sup>

| Address | Data Bit | Default | Type | Name                       | Description   |
|---------|----------|---------|------|----------------------------|---|
| 0x00A   | [0]      | 0       | R    | STAGE0_COMPLETE_STATUS_INT | STAGE0 conversion complete register interrupt status<br>1 indicates STAGE0 conversion completed |
|         | [1]      | 0       |      | STAGE1_COMPLETE_STATUS_INT | STAGE1 conversion complete register interrupt status<br>1 indicates STAGE0 conversion completed |
|         | [2]      | 0       |      | STAGE2_COMPLETE_STATUS_INT | STAGE2 conversion complete register interrupt status<br>1 indicates STAGE0 conversion completed |
|         | [3]      | 0       |      | STAGE3_COMPLETE_STATUS_INT | STAGE3 conversion complete register interrupt status<br>1 indicates STAGE0 conversion completed |
|         | [4]      | 0       |      | STAGE4_COMPLETE_STATUS_INT | STAGE4 conversion complete register interrupt status<br>1 indicates STAGE0 conversion completed |
|         | [5]      | 0       |      | STAGE5_COMPLETE_STATUS_INT | STAGE5 conversion complete register interrupt status<br>1 indicates STAGE0 conversion completed |
|         | [6]      | 0       |      | STAGE6_COMPLETE_STATUS_INT | STAGE6 conversion complete register interrupt status<br>1 indicates STAGE0 conversion completed |
|         | [7]      | 0       |      | STAGE7_COMPLETE_STATUS_INT | STAGE7 conversion complete register interrupt status<br>1 indicates STAGE0 conversion completed |
|         | [15:8]   | 0       |      | Unused                     | 1 indicates STAGE0 conversion completed   |

<sup>1</sup> Registers self-clear to 0 after readback, provided that the limits are not exceeded.

Table 27. CDC 16-Bit Conversion Data Registers

| Address | Data Bit | Default | Type | Name          | Description                       |
|---------|----------|---------|------|---------------|-----------------------------------|
| 0x00B   | [15:0]   | 0       | R    | ADC_RESULT_S0 | STAGE0 CDC 16-bit conversion data |
| 0x00C   | [15:0]   | 0       | R    | ADC_RESULT_S1 | STAGE1 CDC 16-bit conversion data |
| 0x00D   | [15:0]   | 0       | R    | ADC_RESULT_S2 | STAGE2 CDC 16-bit conversion data |
| 0x00E   | [15:0]   | 0       | R    | ADC_RESULT_S3 | STAGE3 CDC 16-bit conversion data |
| 0x00F   | [15:0]   | 0       | R    | ADC_RESULT_S4 | STAGE4 CDC 16-bit conversion data |
| 0x010   | [15:0]   | 0       | R    | ADC_RESULT_S5 | STAGE5 CDC 16-bit conversion data |
| 0x011   | [15:0]   | 0       | R    | ADC_RESULT_S6 | STAGE6 CDC 16-bit conversion data |
| 0x012   | [15:0]   | 0       | R    | ADC_RESULT_S7 | STAGE7 CDC 16-bit conversion data |

Table 28. Device ID Register

| Address | Data Bit | Default | Type | Name          | Description              |
|---------|----------|---------|------|---------------|--------------------------|
| 0x017   | [3:0]    | 0       | R    | REVISION_CODE | AD7143 revision code     |
|         | [15:4]   | E63     | R    | DEVID         | AD7143 device ID = 0xE63 |

Table 29. Proximity Status Register

| Address | Data Bit | Default | Type | Name                    | Description  |
|---------|----------|---------|------|-------------------------|--|
| 0x042   | [0]      | 0       | R    | STAGE0_PROXIMITY_STATUS | STAGE0 proximity status register<br>1 indicates proximity detected on STAGE0 |
|         | [1]      | 0       | R    | STAGE1_PROXIMITY_STATUS | STAGE1 proximity status register<br>1 indicates proximity detected on STAGE1 |
|         | [2]      | 0       | R    | STAGE2_PROXIMITY_STATUS | STAGE2 proximity status register<br>1 indicates proximity detected on STAGE2 |
|         | [3]      | 0       | R    | STAGE3_PROXIMITY_STATUS | STAGE3 proximity status register<br>1 indicates proximity detected on STAGE3 |
|         | [4]      | 0       | R    | STAGE4_PROXIMITY_STATUS | STAGE4 proximity status register<br>1 indicates proximity detected on STAGE4 |
|         | [5]      | 0       | R    | STAGE5_PROXIMITY_STATUS | STAGE5 proximity status register<br>1 indicates proximity detected on STAGE5 |
|         | [6]      | 0       | R    | STAGE6_PROXIMITY_STATUS | STAGE6 proximity status register<br>1 indicates proximity detected on STAGE6 |
|         | [7]      | 0       | R    | STAGE7_PROXIMITY_STATUS | STAGE7 proximity status register<br>1 indicates proximity detected on STAGE7 |
|         | [15:8]   |         |      | Unused                  | Set unused register bits = 0   |

## BANK 2 REGISTERS

All address values are expressed in hexadecimal format.

Table 30. STAGE0 Configuration Registers

| Address | Data Bit | Default | Type | Name                     | Description                                     |
|---------|----------|---------|------|--------------------------|---|
| 0x080   | [15:0]   | X       | R/W  | STAGE0_CONNECTION[6:0]   | STAGE0 CIN(6:0) connection setup (see Table 38) |
| 0x081   | [15:0]   | X       | R/W  | STAGE0_CONNECTION 7      | STAGE0 CIN7 connection setup (see Table 39)     |
| 0x082   | [15:0]   | X       | R/W  | STAGE0_AFE_OFFSET        | STAGE0 AFE offset control (see Table 40)        |
| 0x083   | [15:0]   | X       | R/W  | STAGE0_SENSITIVITY       | STAGE0 sensitivity control (see Table 41)       |
| 0x084   | [15:0]   | X       | R/W  | STAGE0_OFFSET_LOW        | STAGE0 initial offset low value                 |
| 0x085   | [15:0]   | X       | R/W  | STAGE0_OFFSET_HIGH       | STAGE0 initial offset high value                |
| 0x086   | [15:0]   | X       | R/W  | STAGE0_OFFSET_HIGH_CLAMP | STAGE0 offset high clamp value                  |
| 0x087   | [15:0]   | X       | R/W  | STAGE0_OFFSET_LOW_CLAMP  | STAGE0 offset low clamp value                   |

Table 31. STAGE1 Configuration Registers

| Address | Data Bit | Default | Type | Name                     | Description                                     |
|---------|----------|---------|------|--------------------------|---|
| 0x088   | [15:0]   | X       | R/W  | STAGE1_CONNECTION[6:0]   | STAGE1 CIN(6:0) connection setup (see Table 38) |
| 0x089   | [15:0]   | X       | R/W  | STAGE1_CONNECTION 7      | STAGE1 CIN7 connection setup (see Table 39)     |
| 0x08A   | [15:0]   | X       | R/W  | STAGE1_AFE_OFFSET        | STAGE1 AFE offset control (see Table 40)        |
| 0x08B   | [15:0]   | X       | R/W  | STAGE1_SENSITIVITY       | STAGE1 sensitivity control (see Table 41)       |
| 0x08C   | [15:0]   | X       | R/W  | STAGE1_OFFSET_LOW        | STAGE1 initial offset low value                 |
| 0x08D   | [15:0]   | X       | R/W  | STAGE1_OFFSET_HIGH       | STAGE1 initial offset high value                |
| 0x08E   | [15:0]   | X       | R/W  | STAGE1_OFFSET_HIGH_CLAMP | STAGE1 offset high clamp value                  |
| 0x08F   | [15:0]   | X       | R/W  | STAGE1_OFFSET_LOW_CLAMP  | STAGE1 offset low clamp value                   |

Table 32. STAGE2 Configuration Registers

| Address | Data Bit | Default | Type | Name                     | Description                                     |
|---------|----------|---------|------|--------------------------|---|
| 0x090   | [15:0]   | X       | R/W  | STAGE2_CONNECTION[6:0]   | STAGE2 CIN(6:0) connection setup (see Table 38) |
| 0x091   | [15:0]   | X       | R/W  | STAGE2_CONNECTION 7      | STAGE2 CIN7 connection setup (see Table 39)     |
| 0x092   | [15:0]   | X       | R/W  | STAGE2_AFE_OFFSET        | STAGE2 AFE offset control (see Table 40)        |
| 0x093   | [15:0]   | X       | R/W  | STAGE2_SENSITIVITY       | STAGE2 sensitivity control (see Table 41)       |
| 0x094   | [15:0]   | X       | R/W  | STAGE2_OFFSET_LOW        | STAGE2 initial offset low value                 |
| 0x095   | [15:0]   | X       | R/W  | STAGE2_OFFSET_HIGH       | STAGE2 initial offset high value                |
| 0x096   | [15:0]   | X       | R/W  | STAGE2_OFFSET_HIGH_CLAMP | STAGE2 offset high clamp value                  |
| 0x097   | [15:0]   | X       | R/W  | STAGE2_OFFSET_LOW_CLAMP  | STAGE2 offset low clamp value                   |

Table 33. STAGE3 Configuration Registers

| Address | Data Bit | Default | Type | Name                     | Description                                     |
|---------|----------|---------|------|--------------------------|---|
| 0x098   | [15:0]   | X       | R/W  | STAGE3_CONNECTION[6:0]   | STAGE3 CIN(6:0) connection setup (see Table 38) |
| 0x099   | [15:0]   | X       | R/W  | STAGE3_CONNECTION 7      | STAGE3 CIN7 connection setup (see Table 39)     |
| 0x09A   | [15:0]   | X       | R/W  | STAGE3_AFE_OFFSET        | STAGE3 AFE offset control (see Table 40)        |
| 0x09B   | [15:0]   | X       | R/W  | STAGE3_SENSITIVITY       | STAGE3 sensitivity control (see Table 41)       |
| 0x09C   | [15:0]   | X       | R/W  | STAGE3_OFFSET_LOW        | STAGE3 initial offset low value                 |
| 0x09D   | [15:0]   | X       | R/W  | STAGE3_OFFSET_HIGH       | STAGE3 initial offset high value                |
| 0x09E   | [15:0]   | X       | R/W  | STAGE3_OFFSET_HIGH_CLAMP | STAGE3 offset high clamp value                  |
| 0x09F   | [15:0]   | X       | R/W  | STAGE3_OFFSET_LOW_CLAMP  | STAGE3 offset low clamp value                   |

Table 34. STAGE4 Configuration Registers

| Address | Data Bit | Default | Type | Name                     | Description                                     |
|---------|----------|---------|------|--------------------------|---|
| 0x0A0   | [15:0]   | X       | R/W  | STAGE4_CONNECTION[6:0]   | STAGE4 CIN(6:0) connection setup (see Table 38) |
| 0x0A1   | [15:0]   | X       | R/W  | STAGE4_CONNECTION 7      | STAGE4 CIN7 connection setup (see Table 39)     |
| 0x0A2   | [15:0]   | X       | R/W  | STAGE4_AFE_OFFSET        | STAGE4 AFE offset control (see Table 40)        |
| 0x0A3   | [15:0]   | X       | R/W  | STAGE4_SENSITIVITY       | STAGE4 sensitivity control (see Table 41)       |
| 0x0A4   | [15:0]   | X       | R/W  | STAGE4_OFFSET_LOW        | STAGE4 initial offset low value                 |
| 0x0A5   | [15:0]   | X       | R/W  | STAGE4_OFFSET_HIGH       | STAGE4 initial offset high value                |
| 0x0A6   | [15:0]   | X       | R/W  | STAGE4_OFFSET_HIGH_CLAMP | STAGE4 offset high clamp value                  |
| 0x0A7   | [15:0]   | X       | R/W  | STAGE4_OFFSET_LOW_CLAMP  | STAGE4 offset low clamp value                   |

Table 35. STAGE5 Configuration Registers

| Address | Data Bit | Default | Type | Name                     | Description                                     |
|---------|----------|---------|------|--------------------------|---|
| 0x0A8   | [15:0]   | X       | R/W  | STAGE5_CONNECTION[6:0]   | STAGE5 CIN(6:0) connection setup (see Table 38) |
| 0x0A9   | [15:0]   | X       | R/W  | STAGE5_CONNECTION 7      | STAGE5 CIN7 connection setup (see Table 39)     |
| 0x0AA   | [15:0]   | X       | R/W  | STAGE5_AFE_OFFSET        | STAGE5 AFE offset control (see Table 40)        |
| 0x0AB   | [15:0]   | X       | R/W  | STAGE5_SENSITIVITY       | STAGE5 sensitivity control (see Table 41)       |
| 0x0AC   | [15:0]   | X       | R/W  | STAGE5_OFFSET_LOW        | STAGE5 initial offset low value                 |
| 0x0AD   | [15:0]   | X       | R/W  | STAGE5_OFFSET_HIGH       | STAGE5 initial offset high value                |
| 0x0AE   | [15:0]   | X       | R/W  | STAGE5_OFFSET_HIGH_CLAMP | STAGE5 offset high clamp value                  |
| 0x0AF   | [15:0]   | X       | R/W  | STAGE5_OFFSET_LOW_CLAMP  | STAGE5 offset low clamp value                   |

Table 36. STAGE6 Configuration Registers

| Address | Data Bit | Default | Type | Name                     | Description                                     |
|---------|----------|---------|------|--------------------------|---|
| 0x0B0   | [15:0]   | X       | R/W  | STAGE6_CONNECTION[6:0]   | STAGE6 CIN(6:0) connection setup (see Table 38) |
| 0x0B1   | [15:0]   | X       | R/W  | STAGE6_CONNECTION 7      | STAGE6 CIN7 connection setup (see Table 39)     |
| 0x0B2   | [15:0]   | X       | R/W  | STAGE6_AFE_OFFSET        | STAGE6 AFE offset control (see Table 40)        |
| 0x0B3   | [15:0]   | X       | R/W  | STAGE6_SENSITIVITY       | STAGE6 sensitivity control (see Table 41)       |
| 0x0B4   | [15:0]   | X       | R/W  | STAGE6_OFFSET_LOW        | STAGE6 initial offset low value                 |
| 0x0B5   | [15:0]   | X       | R/W  | STAGE6_OFFSET_HIGH       | STAGE6 initial offset high value                |
| 0x0B6   | [15:0]   | X       | R/W  | STAGE6_OFFSET_HIGH_CLAMP | STAGE6 offset high clamp value                  |
| 0x0B7   | [15:0]   | X       | R/W  | STAGE6_OFFSET_LOW_CLAMP  | STAGE6 offset low clamp value                   |

Table 37. STAGE7 Configuration Registers

| Address | Data Bit | Default | Type | Name                     | Description                                     |
|---------|----------|---------|------|--------------------------|---|
| 0x0B8   | [15:0]   | X       | R/W  | STAGE7_CONNECTION[6:0]   | STAGE7 CIN(6:0) connection setup (see Table 38) |
| 0x0B9   | [15:0]   | X       | R/W  | STAGE7_CONNECTION 7      | STAGE7 CIN7 connection setup (see Table 39)     |
| 0x0BA   | [15:0]   | X       | R/W  | STAGE7_AFE_OFFSET        | STAGE7 AFE offset control (see Table 40)        |
| 0x0BB   | [15:0]   | X       | R/W  | STAGE7_SENSITIVITY       | STAGE7 sensitivity control (see Table 41)       |
| 0x0BC   | [15:0]   | X       | R/W  | STAGE7_OFFSET_LOW        | STAGE7 initial offset low value                 |
| 0x0BD   | [15:0]   | X       | R/W  | STAGE7_OFFSET_HIGH       | STAGE7 initial offset high value                |
| 0x0BE   | [15:0]   | X       | R/W  | STAGE7_OFFSET_HIGH_CLAMP | STAGE7 offset high clamp value                  |
| 0x0BF   | [15:0]   | X       | R/W  | STAGE7_OFFSET_LOW_CLAMP  | STAGE7 offset low clamp value                   |

Table 38. STAGEX Detailed CIN (0:6) Connection Setup Description (X = 0 to 6)

| Data Bit | Default | Type | Name                  | Description   |
|----------|---------|------|-----------------------|---|
| [1:0]    | X       | R/W  | CIN0_CONNECTION_SETUP | CIN0 connection setup<br>00 = CIN0 not connected to CDC inputs<br>01 = CIN0 connected to CDC negative input<br>10 = CIN0 connected to CDC positive input<br>11 = CIN0 connected to BIAS (connect unused CIN inputs) |
| [3:2]    | X       | R/W  | CIN1_CONNECTION_SETUP | CIN1 connection setup<br>00 = CIN1 not connected to CDC inputs<br>01 = CIN1 connected to CDC negative input<br>10 = CIN1 connected to CDC positive input<br>11 = CIN1 connected to BIAS (connect unused CIN inputs) |
| [5:4]    | X       | R/W  | CIN2_CONNECTION_SETUP | CIN2 connection setup<br>00 = CIN2 not connected to CDC inputs<br>01 = CIN2 connected to CDC negative input<br>10 = CIN2 connected to CDC positive input<br>11 = CIN2 connected to BIAS (connect unused CIN inputs) |
| [7:6]    | X       | R/W  | CIN3_CONNECTION_SETUP | CIN3 connection setup<br>00 = CIN3 not connected to CDC inputs<br>01 = CIN3 connected to CDC negative input<br>10 = CIN3 connected to CDC positive input<br>11 = CIN3 connected to BIAS (connect unused CIN inputs) |
| [9:8]    | X       | R/W  | CIN4_CONNECTION_SETUP | CIN4 connection setup<br>00 = CIN4 not connected to CDC inputs<br>01 = CIN4 connected to CDC negative input<br>10 = CIN4 connected to CDC positive input<br>11 = CIN4 connected to BIAS (connect unused CIN inputs) |
| [11:10]  | X       | R/W  | CIN5_CONNECTION_SETUP | CIN5 connection setup<br>00 = CIN5 not connected to CDC inputs<br>01 = CIN5 connected to CDC negative input<br>10 = CIN5 connected to CDC positive input<br>11 = CIN5 connected to BIAS (connect unused CIN inputs) |
| [13:12]  | X       | R/W  | CIN6_CONNECTION_SETUP | CIN6 connection setup<br>00 = CIN6 not connected to CDC inputs<br>01 = CIN6 connected to CDC negative input<br>10 = CIN6 connected to CDC positive input<br>11 = CIN6 connected to BIAS (connect unused CIN inputs) |
| [15:14]  | X       |      | Unused                |   |

Table 39. STAGEX Detailed CIN7 Connection Setup Description

| Data Bit | Default | Type | Name                   | Description   |
|----------|---------|------|------------------------|---|
| [1:0]    | X       | R/W  | CIN7_CONNECTION_SETUP  | CIN7 connection setup<br>00 = CIN7 not connected to CDC inputs<br>01 = CIN7 connected to CDC negative input<br>10 = CIN7 connected to CDC positive input<br>11 = CIN7 connected to BIAS (connect unused CIN inputs) |
| [13:2]   | X       | R/W  | Unused                 |   |
| [14]     | X       | R/W  | NEG_AFE_OFFSET_DISABLE | Negative AFE offset enable control<br>0 = enable<br>1 = disable   |
| [15]     | X       | R/W  | POS_AFE_OFFSET_DISABLE | Positive AFE offset enable control<br>0 = enable<br>1 = disable   |

Table 40. STAGEX Detailed Offset Control Description (X = 0 to 7)

| Data Bit | Default | Type | Name                | Description  |
|----------|---------|------|---------------------|--|
| [6:0]    | X       | R/W  | NEG_AFE_OFFSET      | Negative AFE offset setting (20 pF range)<br>1 LSB value = 0.16 pF of offset   |
| [7]      | X       | R/W  | NEG_AFE_OFFSET_SWAP | Negative AFE offset swap control<br>0 = NEG_AFE_OFFSET applied to CDC negative input<br>1 = NEG_AFE_OFFSET applied to CDC positive input |
| [14:8]   | X       | R/W  | POS_AFE_OFFSET      | Positive AFE offset setting (20 pF range)<br>1 LSB value = 0.16 pF of offset   |
| [15]     | X       | R/W  | POS_AFE_OFFSET_SWAP | Positive AFE offset swap control<br>0 = POS_AFE_OFFSET applied to CDC positive input<br>1 = POS_AFE_OFFSET applied to CDC negative input |

Table 41. STAGEX Detailed Sensitivity Control Description (X = 0 to 7)

| Data Bit | Default | Type | Name                      | Description   |
|----------|---------|------|---------------------------|---|
| [3:0]    | X       | R/W  | NEG_THRESHOLD_SENSITIVITY | Negative threshold sensitivity control<br>0000 = 25%, 0001 = 29.73%, 0010 = 34.40%, 0011 = 39.08%<br>0100 = 43.79%, 0101 = 48.47%, 0110 = 53.15%<br>0111 = 57.83%, 1000 = 62.51%, 1001 = 67.22%<br>1010 = 71.90%, 1011 = 76.58%, 1100 = 81.28%<br>1101 = 85.96%, 1110 = 90.64%, 1111 = 95.32% |
| [6:4]    | X       | R/W  | NEG_PEAK_DETECT           | Negative peak detect setting<br>000 = 40% level, 001 = 50% level, 010 = 60% level<br>011 = 70% level, 100 = 80% level, 101 = 90% level  |
| [7]      | X       | R/W  | Unused                    |   |
| [11:8]   | X       | R/W  | POS_THRESHOLD_SENSITIVITY | Positive threshold sensitivity control<br>0000 = 25%, 0001 = 29.73%, 0010 = 34.40%, 0011 = 39.08%<br>0100 = 43.79%, 0101 = 48.47%, 0110 = 53.15%<br>0111 = 57.83%, 1000 = 62.51%, 1001 = 67.22%<br>1010 = 71.90%, 1011 = 76.58%, 1100 = 81.28%<br>1101 = 85.96%, 1110 = 90.64%, 1111 = 95.32% |
| [14:12]  | X       | R/W  | POS_PEAK_DETECT           | Positive peak detect setting<br>000 = 40% level, 001 = 50% level, 010 = 60% level<br>011 = 70% level, 100 = 80% level, 101 = 90% level  |
| [15]     | X       | R/W  | Unused                    |   |

**BANK 3 REGISTERS**

All address values are expressed in hexadecimal format.

**Table 42. STAGE0 Results Registers**

| Address | Data Bit | Default | Type | Name                     | Description  |
|---------|----------|---------|------|--------------------------|--|
| 0x0E0   | [15:0]   | X       | R/W  | STAGE0_CONV_DATA         | STAGE0 CDC 16-bit conversion data<br>(copy of data in STAGE0_CONV_DATA register) |
| 0x0E1   | [15:0]   | X       | R/W  | STAGE0_FF_WORD0          | STAGE0 fast FIFO WORD0   |
| 0x0E2   | [15:0]   | X       | R/W  | STAGE0_FF_WORD1          | STAGE0 fast FIFO WORD1   |
| 0x0E3   | [15:0]   | X       | R/W  | STAGE0_FF_WORD2          | STAGE0 fast FIFO WORD2   |
| 0x0E4   | [15:0]   | X       | R/W  | STAGE0_FF_WORD3          | STAGE0 fast FIFO WORD3   |
| 0x0E5   | [15:0]   | X       | R/W  | STAGE0_FF_WORD4          | STAGE0 fast FIFO WORD4   |
| 0x0E6   | [15:0]   | X       | R/W  | STAGE0_FF_WORD5          | STAGE0 fast FIFO WORD5   |
| 0x0E7   | [15:0]   | X       | R/W  | STAGE0_FF_WORD6          | STAGE0 fast FIFO WORD6   |
| 0x0E8   | [15:0]   | X       | R/W  | STAGE0_FF_WORD7          | STAGE0 fast FIFO WORD7   |
| 0x0E9   | [15:0]   | X       | R/W  | STAGE0_SF_WORD0          | STAGE0 slow FIFO WORD0   |
| 0x0EA   | [15:0]   | X       | R/W  | STAGE0_SF_WORD1          | STAGE0 slow FIFO WORD1   |
| 0x0EB   | [15:0]   | X       | R/W  | STAGE0_SF_WORD2          | STAGE0 slow FIFO WORD2   |
| 0x0EC   | [15:0]   | X       | R/W  | STAGE0_SF_WORD3          | STAGE0 slow FIFO WORD3   |
| 0x0ED   | [15:0]   | X       | R/W  | STAGE0_SF_WORD4          | STAGE0 slow FIFO WORD4   |
| 0x0EE   | [15:0]   | X       | R/W  | STAGE0_SF_WORD5          | STAGE0 slow FIFO WORD5   |
| 0x0EF   | [15:0]   | X       | R/W  | STAGE0_SF_WORD6          | STAGE0 slow FIFO WORD6   |
| 0x0F0   | [15:0]   | X       | R/W  | STAGE0_SF_WORD7          | STAGE0 slow FIFO WORD7   |
| 0x0F1   | [15:0]   | X       | R/W  | STAGE0_SF_AMBIENT        | STAGE0 slow FIFO ambient value   |
| 0x0F2   | [15:0]   | X       | R/W  | STAGE0_FF_AVG            | STAGE0 fast FIFO average value   |
| 0x0F3   | [15:0]   | X       | R/W  | STAGE0_PEAK_DETECT_WORD0 | STAGE0 peak FIFO WORD0 value   |
| 0x0F4   | [15:0]   | X       | R/W  | STAGE0_PEAK_DETECT_WORD1 | STAGE0 peak FIFO WORD1 value   |
| 0x0F5   | [15:0]   | X       | R/W  | STAGE0_MAX_WORD0         | STAGE0 maximum value FIFO WORD0  |
| 0x0F6   | [15:0]   | X       | R/W  | STAGE0_MAX_WORD1         | STAGE0 maximum value FIFO WORD1  |
| 0x0F7   | [15:0]   | X       | R/W  | STAGE0_MAX_WORD2         | STAGE0 maximum value FIFO WORD2  |
| 0x0F8   | [15:0]   | X       | R/W  | STAGE0_MAX_WORD3         | STAGE0 maximum value FIFO WORD3  |
| 0x0F9   | [15:0]   | X       | R/W  | STAGE0_MAX_AVG           | STAGE0 average maximum FIFO value  |
| 0x0FA   | [15:0]   | X       | R/W  | STAGE0_HIGH_THRESHOLD    | STAGE0 high threshold value  |
| 0x0FB   | [15:0]   | X       | R/W  | STAGE0_MAX_TEMP          | STAGE0 temporary maximum value   |
| 0x0FC   | [15:0]   | X       | R/W  | STAGE0_MIN_WORD0         | STAGE0 minimum value FIFO WORD0  |
| 0x0FD   | [15:0]   | X       | R/W  | STAGE0_MIN_WORD1         | STAGE0 minimum value FIFO WORD1  |
| 0x0FE   | [15:0]   | X       | R/W  | STAGE0_MIN_WORD2         | STAGE0 minimum value FIFO WORD2  |
| 0x0FF   | [15:0]   | X       | R/W  | STAGE0_MIN_WORD3         | STAGE0 minimum value FIFO WORD3  |
| 0x100   | [15:0]   | X       | R/W  | STAGE0_MIN_AVG           | STAGE0 average minimum FIFO value  |
| 0x101   | [15:0]   | X       | R/W  | STAGE0_LOW_THRESHOLD     | STAGE0 low threshold value   |
| 0x102   | [15:0]   | X       | R/W  | STAGE0_MIN_TEMP          | STAGE0 temporary minimum value   |
| 0x103   | [15:0]   | X       | R/W  | Unused                   |  |



Table 43. STAGE1 Results Registers

| Address | Data Bit | Default | Type | Name                  | Description  |
|---------|----------|---------|------|-----------------------|--|
| 0x104   | [15:0]   | X       | R/W  | STAGE1_CONV_DATA      | STAGE1 CDC 16-bit conversion data<br>(copy of data in STAGE1_CONV_DATA register) |
| 0x105   | [15:0]   | X       | R/W  | STAGE1_FF_WORD0       | STAGE1 fast FIFO WORD0   |
| 0x106   | [15:0]   | X       | R/W  | STAGE1_FF_WORD1       | STAGE1 fast FIFO WORD1   |
| 0x107   | [15:0]   | X       | R/W  | STAGE1_FF_WORD2       | STAGE1 fast FIFO WORD2   |
| 0x108   | [15:0]   | X       | R/W  | STAGE1_FF_WORD3       | STAGE1 fast FIFO WORD3   |
| 0x109   | [15:0]   | X       | R/W  | STAGE1_FF_WORD4       | STAGE1 fast FIFO WORD4   |
| 0x10A   | [15:0]   | X       | R/W  | STAGE1_FF_WORD5       | STAGE1 fast FIFO WORD5   |
| 0x10B   | [15:0]   | X       | R/W  | STAGE1_FF_WORD6       | STAGE1 fast FIFO WORD6   |
| 0x10C   | [15:0]   | X       | R/W  | STAGE1_FF_WORD7       | STAGE1 fast FIFO WORD7   |
| 0x10D   | [15:0]   | X       | R/W  | STAGE1_SF_WORD0       | STAGE1 slow FIFO WORD0   |
| 0x10E   | [15:0]   | X       | R/W  | STAGE1_SF_WORD1       | STAGE1 slow FIFO WORD1   |
| 0x10F   | [15:0]   | X       | R/W  | STAGE1_SF_WORD2       | STAGE1 slow FIFO WORD2   |
| 0x110   | [15:0]   | X       | R/W  | STAGE1_SF_WORD3       | STAGE1 slow FIFO WORD3   |
| 0x111   | [15:0]   | X       | R/W  | STAGE1_SF_WORD4       | STAGE1 slow FIFO WORD4   |
| 0x112   | [15:0]   | X       | R/W  | STAGE1_SF_WORD5       | STAGE1 slow FIFO WORD5   |
| 0x113   | [15:0]   | X       | R/W  | STAGE1_SF_WORD6       | STAGE1 slow FIFO WORD6   |
| 0x114   | [15:0]   | X       | R/W  | STAGE1_SF_WORD7       | STAGE1 slow FIFO WORD7   |
| 0x115   | [15:0]   | X       | R/W  | STAGE1_SF_AMBIENT     | STAGE1 slow FIFO ambient value   |
| 0x116   | [15:0]   | X       | R/W  | STAGE1_FF_AVG         | STAGE1 fast FIFO average value   |
| 0x117   | [15:0]   | X       | R/W  | STAGE1_CDC_WORD0      | STAGE1 CDC FIFO WORD0  |
| 0x118   | [15:0]   | X       | R/W  | STAGE1_CDC_WORD1      | STAGE1 CDC FIFO WORD1  |
| 0x119   | [15:0]   | X       | R/W  | STAGE1_MAX_WORD0      | STAGE1 maximum value FIFO WORD0  |
| 0x11A   | [15:0]   | X       | R/W  | STAGE1_MAX_WORD1      | STAGE1 maximum value FIFO WORD1  |
| 0x11B   | [15:0]   | X       | R/W  | STAGE1_MAX_WORD2      | STAGE1 maximum value FIFO WORD2  |
| 0x11C   | [15:0]   | X       | R/W  | STAGE1_MAX_WORD3      | STAGE1 maximum value FIFO WORD3  |
| 0x11D   | [15:0]   | X       | R/W  | STAGE1_MAX_AVG        | STAGE1 average maximum FIFO value  |
| 0x11E   | [15:0]   | X       | R/W  | STAGE1_HIGH_THRESHOLD | STAGE1 high threshold value  |
| 0x11F   | [15:0]   | X       | R/W  | STAGE1_MAX_TEMP       | STAGE1 temporary maximum value   |
| 0x120   | [15:0]   | X       | R/W  | STAGE1_MIN_WORD0      | STAGE1 minimum value FIFO WORD0  |
| 0x121   | [15:0]   | X       | R/W  | STAGE1_MIN_WORD1      | STAGE1 minimum value FIFO WORD1  |
| 0x122   | [15:0]   | X       | R/W  | STAGE1_MIN_WORD2      | STAGE1 minimum value FIFO WORD2  |
| 0x123   | [15:0]   | X       | R/W  | STAGE1_MIN_WORD3      | STAGE1 minimum value FIFO WORD3  |
| 0x124   | [15:0]   | X       | R/W  | STAGE1_MIN_AVG        | STAGE1 average minimum FIFO value  |
| 0x125   | [15:0]   | X       | R/W  | STAGE1_LOW_THRESHOLD  | STAGE1 low threshold value   |
| 0x126   | [15:0]   | X       | R/W  | STAGE1_MIN_TEMP       | STAGE1 temporary minimum value   |
| 0x127   | [15:0]   | X       | R/W  | Unused                |  |



Table 44. STAGE2 Results Registers

| Address | Data Bit | Default | Type | Name                  | Description  |
|---------|----------|---------|------|-----------------------|--|
| 0x128   | [15:0]   | X       | R/W  | STAGE2_CONV_DATA      | STAGE2 CDC 16-bit conversion data<br>(copy of data in STAGE2_CONV_DATA register) |
| 0x129   | [15:0]   | X       | R/W  | STAGE2_FF_WORD0       | STAGE2 fast FIFO WORD0   |
| 0x12A   | [15:0]   | X       | R/W  | STAGE2_FF_WORD1       | STAGE2 fast FIFO WORD1   |
| 0x12B   | [15:0]   | X       | R/W  | STAGE2_FF_WORD2       | STAGE2 fast FIFO WORD2   |
| 0x12C   | [15:0]   | X       | R/W  | STAGE2_FF_WORD3       | STAGE2 fast FIFO WORD3   |
| 0x12D   | [15:0]   | X       | R/W  | STAGE2_FF_WORD4       | STAGE2 fast FIFO WORD4   |
| 0x12E   | [15:0]   | X       | R/W  | STAGE2_FF_WORD5       | STAGE2 fast FIFO WORD5   |
| 0x12F   | [15:0]   | X       | R/W  | STAGE2_FF_WORD6       | STAGE2 fast FIFO WORD6   |
| 0x130   | [15:0]   | X       | R/W  | STAGE2_FF_WORD7       | STAGE2 fast FIFO WORD7   |
| 0x131   | [15:0]   | X       | R/W  | STAGE2_SF_WORD0       | STAGE2 slow FIFO WORD0   |
| 0x132   | [15:0]   | X       | R/W  | STAGE2_SF_WORD1       | STAGE2 slow FIFO WORD1   |
| 0x133   | [15:0]   | X       | R/W  | STAGE2_SF_WORD2       | STAGE2 slow FIFO WORD2   |
| 0x134   | [15:0]   | X       | R/W  | STAGE2_SF_WORD3       | STAGE2 slow FIFO WORD3   |
| 0x135   | [15:0]   | X       | R/W  | STAGE2_SF_WORD4       | STAGE2 slow FIFO WORD4   |
| 0x125   | [15:0]   | X       | R/W  | STAGE2_SF_WORD5       | STAGE2 slow FIFO WORD5   |
| 0x137   | [15:0]   | X       | R/W  | STAGE2_SF_WORD6       | STAGE2 slow FIFO WORD6   |
| 0x138   | [15:0]   | X       | R/W  | STAGE2_SF_WORD7       | STAGE2 slow FIFO WORD7   |
| 0x139   | [15:0]   | X       | R/W  | STAGE2_SF_AMBIENT     | STAGE2 slow FIFO ambient value   |
| 0x13A   | [15:0]   | X       | R/W  | STAGE2_FF_AVG         | STAGE2 fast FIFO average value   |
| 0x13B   | [15:0]   | X       | R/W  | STAGE2_CDC_WORD0      | STAGE2 CDC FIFO WORD0  |
| 0x13C   | [15:0]   | X       | R/W  | STAGE2_CDC_WORD1      | STAGE2 CDC FIFO WORD1  |
| 0x13D   | [15:0]   | X       | R/W  | STAGE2_MAX_WORD0      | STAGE2 maximum value FIFO WORD0  |
| 0x13E   | [15:0]   | X       | R/W  | STAGE2_MAX_WORD1      | STAGE2 maximum value FIFO WORD1  |
| 0x13F   | [15:0]   | X       | R/W  | STAGE2_MAX_WORD2      | STAGE2 maximum value FIFO WORD2  |
| 0x140   | [15:0]   | X       | R/W  | STAGE2_MAX_WORD3      | STAGE2 maximum value FIFO WORD3  |
| 0x141   | [15:0]   | X       | R/W  | STAGE2_MAX_AVG        | STAGE2 average maximum FIFO value  |
| 0x142   | [15:0]   | X       | R/W  | STAGE2_HIGH_THRESHOLD | STAGE2 high threshold value  |
| 0x143   | [15:0]   | X       | R/W  | STAGE2_MAX_TEMP       | STAGE2 temporary maximum value   |
| 0x144   | [15:0]   | X       | R/W  | STAGE2_MIN_WORD0      | STAGE2 minimum value FIFO WORD0  |
| 0x145   | [15:0]   | X       | R/W  | STAGE2_MIN_WORD1      | STAGE2 minimum value FIFO WORD1  |
| 0x146   | [15:0]   | X       | R/W  | STAGE2_MIN_WORD2      | STAGE2 minimum value FIFO WORD2  |
| 0x147   | [15:0]   | X       | R/W  | STAGE2_MIN_WORD3      | STAGE2 minimum value FIFO WORD3  |
| 0x148   | [15:0]   | X       | R/W  | STAGE2_MIN_AVG        | STAGE2 average minimum FIFO value  |
| 0x149   | [15:0]   | X       | R/W  | STAGE2_LOW_THRESHOLD  | STAGE2 low threshold value   |
| 0x14A   | [15:0]   | X       | R/W  | STAGE2_MIN_TEMP       | STAGE2 temporary minimum value   |
| 0x14B   | [15:0]   | X       | R/W  | Unused                |  |

Table 45. STAGE3 Results Registers

| Address | Data Bit | Default | Type | Name                  | Description  |
|---------|----------|---------|------|-----------------------|--|
| 0x14C   | [15:0]   | X       | R/W  | STAGE3_CONV_DATA      | STAGE3 CDC 16-bit conversion data<br>(copy of data in STAGE3_CONV_DATA register) |
| 0x14D   | [15:0]   | X       | R/W  | STAGE3_FF_WORD0       | STAGE3 fast FIFO WORD0   |
| 0x14E   | [15:0]   | X       | R/W  | STAGE3_FF_WORD1       | STAGE3 fast FIFO WORD1   |
| 0x14F   | [15:0]   | X       | R/W  | STAGE3_FF_WORD2       | STAGE3 fast FIFO WORD2   |
| 0x150   | [15:0]   | X       | R/W  | STAGE3_FF_WORD3       | STAGE3 fast FIFO WORD3   |
| 0x151   | [15:0]   | X       | R/W  | STAGE3_FF_WORD4       | STAGE3 fast FIFO WORD4   |
| 0x152   | [15:0]   | X       | R/W  | STAGE3_FF_WORD5       | STAGE3 fast FIFO WORD5   |
| 0x153   | [15:0]   | X       | R/W  | STAGE3_FF_WORD6       | STAGE3 fast FIFO WORD6   |
| 0x154   | [15:0]   | X       | R/W  | STAGE3_FF_WORD7       | STAGE3 fast FIFO WORD7   |
| 0x155   | [15:0]   | X       | R/W  | STAGE3_SF_WORD0       | STAGE3 slow FIFO WORD0   |
| 0x156   | [15:0]   | X       | R/W  | STAGE3_SF_WORD1       | STAGE3 slow FIFO WORD1   |
| 0x157   | [15:0]   | X       | R/W  | STAGE3_SF_WORD2       | STAGE3 slow FIFO WORD2   |
| 0x158   | [15:0]   | X       | R/W  | STAGE3_SF_WORD3       | STAGE3 slow FIFO WORD3   |
| 0x159   | [15:0]   | X       | R/W  | STAGE3_SF_WORD4       | STAGE3 slow FIFO WORD4   |
| 0x15A   | [15:0]   | X       | R/W  | STAGE3_SF_WORD5       | STAGE3 slow FIFO WORD5   |
| 0x15B   | [15:0]   | X       | R/W  | STAGE3_SF_WORD6       | STAGE3 slow FIFO WORD6   |
| 0x15C   | [15:0]   | X       | R/W  | STAGE3_SF_WORD7       | STAGE3 slow FIFO WORD7   |
| 0x15D   | [15:0]   | X       | R/W  | STAGE3_SF_AMBIENT     | STAGE3 slow FIFO ambient value   |
| 0x15E   | [15:0]   | X       | R/W  | STAGE3_FF_AVG         | STAGE3 fast FIFO average value   |
| 0x15F   | [15:0]   | X       | R/W  | STAGE3_CDC_WORD0      | STAGE3 CDC FIFO WORD0  |
| 0x160   | [15:0]   | X       | R/W  | STAGE3_CDC_WORD1      | STAGE3 CDC FIFO WORD1  |
| 0x161   | [15:0]   | X       | R/W  | STAGE3_MAX_WORD0      | STAGE3 maximum value FIFO WORD0  |
| 0x162   | [15:0]   | X       | R/W  | STAGE3_MAX_WORD1      | STAGE3 maximum value FIFO WORD1  |
| 0x163   | [15:0]   | X       | R/W  | STAGE3_MAX_WORD2      | STAGE3 maximum value FIFO WORD2  |
| 0x164   | [15:0]   | X       | R/W  | STAGE3_MAX_WORD3      | STAGE3 maximum value FIFO WORD3  |
| 0x165   | [15:0]   | X       | R/W  | STAGE3_MAX_AVG        | STAGE3 average maximum FIFO value  |
| 0x166   | [15:0]   | X       | R/W  | STAGE3_HIGH_THRESHOLD | STAGE3 high threshold value  |
| 0x167   | [15:0]   | X       | R/W  | STAGE3_MAX_TEMP       | STAGE3 temporary maximum value   |
| 0x168   | [15:0]   | X       | R/W  | STAGE3_MIN_WORD0      | STAGE3 minimum value FIFO WORD0  |
| 0x169   | [15:0]   | X       | R/W  | STAGE3_MIN_WORD1      | STAGE3 minimum value FIFO WORD1  |
| 0x16A   | [15:0]   | X       | R/W  | STAGE3_MIN_WORD2      | STAGE3 minimum value FIFO WORD2  |
| 0x16B   | [15:0]   | X       | R/W  | STAGE3_MIN_WORD3      | STAGE3 minimum value FIFO WORD3  |
| 0x16C   | [15:0]   | X       | R/W  | STAGE3_MIN_AVG        | STAGE3 average minimum FIFO value  |
| 0x16D   | [15:0]   | X       | R/W  | STAGE3_LOW_THRESHOLD  | STAGE3 low threshold value   |
| 0x16E   | [15:0]   | X       | R/W  | STAGE3_MIN_TEMP       | STAGE3 temporary minimum value   |
| 0x16F   | [15:0]   | X       | R/W  | Unused                |  |

Table 46. STAGE4 Results Registers

| Address | Data Bit | Default | Type | Name                  | Description  |
|---------|----------|---------|------|-----------------------|--|
| 0x170   | [15:0]   | X       | R/W  | STAGE4_CONV_DATA      | STAGE4 CDC 16-bit conversion data<br>(copy of data in STAGE4_CONV_DATA register) |
| 0x171   | [15:0]   | X       | R/W  | STAGE4_FF_WORD0       | STAGE4 fast FIFO WORD0   |
| 0x172   | [15:0]   | X       | R/W  | STAGE4_FF_WORD1       | STAGE4 fast FIFO WORD1   |
| 0x173   | [15:0]   | X       | R/W  | STAGE4_FF_WORD2       | STAGE4 fast FIFO WORD2   |
| 0x174   | [15:0]   | X       | R/W  | STAGE4_FF_WORD3       | STAGE4 fast FIFO WORD3   |
| 0x175   | [15:0]   | X       | R/W  | STAGE4_FF_WORD4       | STAGE4 fast FIFO WORD4   |
| 0x176   | [15:0]   | X       | R/W  | STAGE4_FF_WORD5       | STAGE4 fast FIFO WORD5   |
| 0x177   | [15:0]   | X       | R/W  | STAGE4_FF_WORD6       | STAGE4 fast FIFO WORD6   |
| 0x178   | [15:0]   | X       | R/W  | STAGE4_FF_WORD7       | STAGE4 fast FIFO WORD7   |
| 0x179   | [15:0]   | X       | R/W  | STAGE4_SF_WORD0       | STAGE4 slow FIFO WORD0   |
| 0x17A   | [15:0]   | X       | R/W  | STAGE4_SF_WORD1       | STAGE4 slow FIFO WORD1   |
| 0x17B   | [15:0]   | X       | R/W  | STAGE4_SF_WORD2       | STAGE4 slow FIFO WORD2   |
| 0x17C   | [15:0]   | X       | R/W  | STAGE4_SF_WORD3       | STAGE4 slow FIFO WORD3   |
| 0x17D   | [15:0]   | X       | R/W  | STAGE4_SF_WORD4       | STAGE4 slow FIFO WORD4   |
| 0x17E   | [15:0]   | X       | R/W  | STAGE4_SF_WORD5       | STAGE4 slow FIFO WORD5   |
| 0x17F   | [15:0]   | X       | R/W  | STAGE4_SF_WORD6       | STAGE4 slow FIFO WORD6   |
| 0x180   | [15:0]   | X       | R/W  | STAGE4_SF_WORD7       | STAGE4 slow FIFO WORD7   |
| 0x181   | [15:0]   | X       | R/W  | STAGE4_SF_AMBIENT     | STAGE4 slow FIFO ambient value   |
| 0x182   | [15:0]   | X       | R/W  | STAGE4_FF_AVG         | STAGE4 fast FIFO average value   |
| 0x183   | [15:0]   | X       | R/W  | STAGE4_CDC_WORD0      | STAGE4 CDC FIFO WORD0  |
| 0x184   | [15:0]   | X       | R/W  | STAGE4_CDC_WORD1      | STAGE4 CDC FIFO WORD1  |
| 0x185   | [15:0]   | X       | R/W  | STAGE4_MAX_WORD0      | STAGE4 maximum value FIFO WORD0  |
| 0x186   | [15:0]   | X       | R/W  | STAGE4_MAX_WORD1      | STAGE4 maximum value FIFO WORD1  |
| 0x187   | [15:0]   | X       | R/W  | STAGE4_MAX_WORD2      | STAGE4 maximum value FIFO WORD2  |
| 0x188   | [15:0]   | X       | R/W  | STAGE4_MAX_WORD3      | STAGE4 maximum value FIFO WORD3  |
| 0x189   | [15:0]   | X       | R/W  | STAGE4_MAX_AVG        | STAGE4 average maximum FIFO value  |
| 0x18A   | [15:0]   | X       | R/W  | STAGE4_HIGH_THRESHOLD | STAGE4 high threshold value  |
| 0x18B   | [15:0]   | X       | R/W  | STAGE4_MAX_TEMP       | STAGE4 temporary maximum value   |
| 0x18C   | [15:0]   | X       | R/W  | STAGE4_MIN_WORD0      | STAGE4 minimum value FIFO WORD0  |
| 0x18D   | [15:0]   | X       | R/W  | STAGE4_MIN_WORD1      | STAGE4 minimum value FIFO WORD1  |
| 0x18E   | [15:0]   | X       | R/W  | STAGE4_MIN_WORD2      | STAGE4 minimum value FIFO WORD2  |
| 0x18F   | [15:0]   | X       | R/W  | STAGE4_MIN_WORD3      | STAGE4 minimum value FIFO WORD3  |
| 0x190   | [15:0]   | X       | R/W  | STAGE4_MIN_AVG        | STAGE4 average minimum FIFO value  |
| 0x191   | [15:0]   | X       | R/W  | STAGE4_LOW_THRESHOLD  | STAGE4 low threshold value   |
| 0x192   | [15:0]   | X       | R/W  | STAGE4_MIN_TEMP       | STAGE4 temporary minimum value   |
| 0x193   | [15:0]   | X       | R/W  | Unused                |  |

Table 47. STAGE5 Results Registers

| Address | Data Bit | Default | Type | Name                  | Description  |
|---------|----------|---------|------|-----------------------|--|
| 0x194   | [15:0]   | X       | R/W  | STAGE5_CONV_DATA      | STAGE5 CDC 16-bit conversion data<br>(copy of data in STAGE5_CONV_DATA register) |
| 0x195   | [15:0]   | X       | R/W  | STAGE5_FF_WORD0       | STAGE5 fast FIFO WORD0   |
| 0x196   | [15:0]   | X       | R/W  | STAGE5_FF_WORD1       | STAGE5 fast FIFO WORD1   |
| 0x197   | [15:0]   | X       | R/W  | STAGE5_FF_WORD2       | STAGE5 fast FIFO WORD2   |
| 0x198   | [15:0]   | X       | R/W  | STAGE5_FF_WORD3       | STAGE5 fast FIFO WORD3   |
| 0x199   | [15:0]   | X       | R/W  | STAGE5_FF_WORD4       | STAGE5 fast FIFO WORD4   |
| 0x19A   | [15:0]   | X       | R/W  | STAGE5_FF_WORD5       | STAGE5 fast FIFO WORD5   |
| 0x19B   | [15:0]   | X       | R/W  | STAGE5_FF_WORD6       | STAGE5 fast FIFO WORD6   |
| 0x19C   | [15:0]   | X       | R/W  | STAGE5_FF_WORD7       | STAGE5 fast FIFO WORD7   |
| 0x19D   | [15:0]   | X       | R/W  | STAGE5_SF_WORD0       | STAGE5 slow FIFO WORD0   |
| 0x19E   | [15:0]   | X       | R/W  | STAGE5_SF_WORD1       | STAGE5 slow FIFO WORD1   |
| 0x19F   | [15:0]   | X       | R/W  | STAGE5_SF_WORD2       | STAGE5 slow FIFO WORD2   |
| 0x1A0   | [15:0]   | X       | R/W  | STAGE5_SF_WORD3       | STAGE5 slow FIFO WORD3   |
| 0x1A1   | [15:0]   | X       | R/W  | STAGE5_SF_WORD4       | STAGE5 slow FIFO WORD4   |
| 0x1A2   | [15:0]   | X       | R/W  | STAGE5_SF_WORD5       | STAGE5 slow FIFO WORD5   |
| 0x1A3   | [15:0]   | X       | R/W  | STAGE5_SF_WORD6       | STAGE5 slow FIFO WORD6   |
| 0x1A4   | [15:0]   | X       | R/W  | STAGE5_SF_WORD7       | STAGE5 slow FIFO WORD7   |
| 0x1A5   | [15:0]   | X       | R/W  | STAGE5_SF_AMBIENT     | STAGE5 slow FIFO ambient value   |
| 0x1A6   | [15:0]   | X       | R/W  | STAGE5_FF_AVG         | STAGE5 fast FIFO average value   |
| 0x1A7   | [15:0]   | X       | R/W  | STAGE5_CDC_WORD0      | STAGE5 CDC FIFO WORD0  |
| 0x1A8   | [15:0]   | X       | R/W  | STAGE5_CDC_WORD1      | STAGE5 CDC FIFO WORD1  |
| 0x1A9   | [15:0]   | X       | R/W  | STAGE5_MAX_WORD0      | STAGE5 maximum value FIFO WORD0  |
| 0x1AA   | [15:0]   | X       | R/W  | STAGE5_MAX_WORD1      | STAGE5 maximum value FIFO WORD1  |
| 0x1AB   | [15:0]   | X       | R/W  | STAGE5_MAX_WORD2      | STAGE5 maximum value FIFO WORD2  |
| 0x1AC   | [15:0]   | X       | R/W  | STAGE5_MAX_WORD3      | STAGE5 maximum value FIFO WORD3  |
| 0x1AD   | [15:0]   | X       | R/W  | STAGE5_MAX_AVG        | STAGE5 average maximum FIFO value  |
| 0x1AE   | [15:0]   | X       | R/W  | STAGE5_HIGH_THRESHOLD | STAGE5 high threshold value  |
| 0x1AF   | [15:0]   | X       | R/W  | STAGE5_MAX_TEMP       | STAGE5 temporary maximum value   |
| 0x1B0   | [15:0]   | X       | R/W  | STAGE5_MIN_WORD0      | STAGE5 minimum value FIFO WORD0  |
| 0x1B1   | [15:0]   | X       | R/W  | STAGE5_MIN_WORD1      | STAGE5 minimum value FIFO WORD1  |
| 0x1B2   | [15:0]   | X       | R/W  | STAGE5_MIN_WORD2      | STAGE5 minimum value FIFO WORD2  |
| 0x1B3   | [15:0]   | X       | R/W  | STAGE5_MIN_WORD3      | STAGE5 minimum value FIFO WORD3  |
| 0x1B4   | [15:0]   | X       | R/W  | STAGE5_MIN_AVG        | STAGE5 average minimum FIFO value  |
| 0x1B5   | [15:0]   | X       | R/W  | STAGE5_LOW_THRESHOLD  | STAGE5 low threshold value   |
| 0x1B6   | [15:0]   | X       | R/W  | STAGE5_MIN_TEMP       | STAGE5 temporary minimum value   |
| 0x1B7   | [15:0]   | X       | R/W  | Unused                |  |

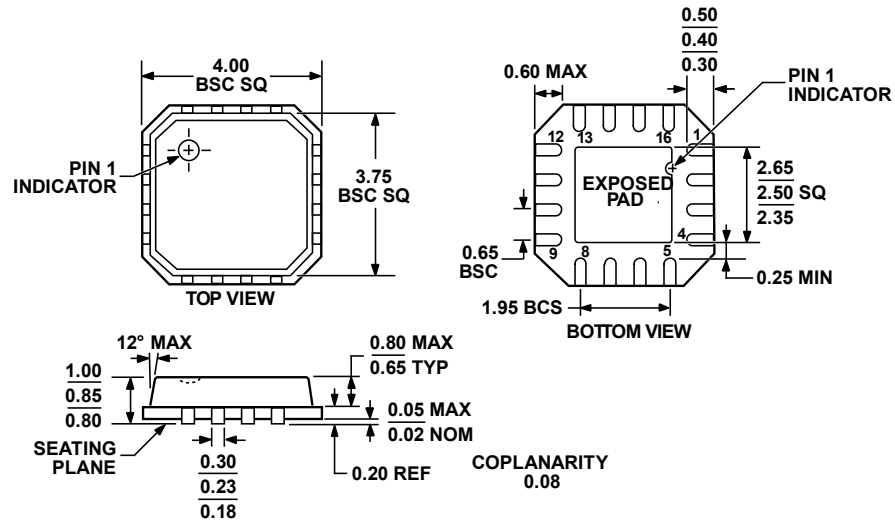
Table 48. STAGE6 Results Registers

| Address | Data Bit | Default | Type | Name                  | Description  |
|---------|----------|---------|------|-----------------------|--|
| 0x1B8   | [15:0]   | X       | R/W  | STAGE6_CONV_DATA      | STAGE6 CDC 16-bit conversion data<br>(copy of data in STAGE6_CONV_DATA register) |
| 0x1B9   | [15:0]   | X       | R/W  | STAGE6_FF_WORD0       | STAGE6 fast FIFO WORD0   |
| 0x1BA   | [15:0]   | X       | R/W  | STAGE6_FF_WORD1       | STAGE6 fast FIFO WORD1   |
| 0x1BB   | [15:0]   | X       | R/W  | STAGE6_FF_WORD2       | STAGE6 fast FIFO WORD2   |
| 0x1BC   | [15:0]   | X       | R/W  | STAGE6_FF_WORD3       | STAGE6 fast FIFO WORD3   |
| 0x1BD   | [15:0]   | X       | R/W  | STAGE6_FF_WORD4       | STAGE6 fast FIFO WORD4   |
| 0x1BE   | [15:0]   | X       | R/W  | STAGE6_FF_WORD5       | STAGE6 fast FIFO WORD5   |
| 0x1BF   | [15:0]   | X       | R/W  | STAGE6_FF_WORD6       | STAGE6 fast FIFO WORD6   |
| 0x1C0   | [15:0]   | X       | R/W  | STAGE6_FF_WORD7       | STAGE6 fast FIFO WORD7   |
| 0x1C1   | [15:0]   | X       | R/W  | STAGE6_SF_WORD0       | STAGE6 slow FIFO WORD0   |
| 0x1C2   | [15:0]   | X       | R/W  | STAGE6_SF_WORD1       | STAGE6 slow FIFO WORD1   |
| 0x1C3   | [15:0]   | X       | R/W  | STAGE6_SF_WORD2       | STAGE6 slow FIFO WORD2   |
| 0x1C4   | [15:0]   | X       | R/W  | STAGE6_SF_WORD3       | STAGE6 slow FIFO WORD3   |
| 0x1C5   | [15:0]   | X       | R/W  | STAGE6_SF_WORD4       | STAGE6 slow FIFO WORD4   |
| 0x1C6   | [15:0]   | X       | R/W  | STAGE6_SF_WORD5       | STAGE6 slow FIFO WORD5   |
| 0x1C7   | [15:0]   | X       | R/W  | STAGE6_SF_WORD6       | STAGE6 slow FIFO WORD6   |
| 0x1C8   | [15:0]   | X       | R/W  | STAGE6_SF_WORD7       | STAGE6 slow FIFO WORD7   |
| 0x1C9   | [15:0]   | X       | R/W  | STAGE6_SF_AMBIENT     | STAGE6 slow FIFO ambient value   |
| 0x1CA   | [15:0]   | X       | R/W  | STAGE6_FF_AVG         | STAGE6 fast FIFO average value   |
| 0x1CB   | [15:0]   | X       | R/W  | STAGE6_CDC_WORD0      | STAGE0 CDC FIFO WORD0  |
| 0x1CC   | [15:0]   | X       | R/W  | STAGE6_CDC_WORD1      | STAGE6 CDC FIFO WORD1  |
| 0x1CD   | [15:0]   | X       | R/W  | STAGE6_MAX_WORD0      | STAGE6 maximum value FIFO WORD0  |
| 0x1CE   | [15:0]   | X       | R/W  | STAGE6_MAX_WORD1      | STAGE6 maximum value FIFO WORD1  |
| 0x1CF   | [15:0]   | X       | R/W  | STAGE6_MAX_WORD2      | STAGE6 maximum value FIFO WORD2  |
| 0x1D0   | [15:0]   | X       | R/W  | STAGE6_MAX_WORD3      | STAGE6 maximum value FIFO WORD3  |
| 0x1D1   | [15:0]   | X       | R/W  | STAGE6_MAX_AVG        | STAGE6 average maximum FIFO value  |
| 0x1D2   | [15:0]   | X       | R/W  | STAGE6_HIGH_THRESHOLD | STAGE6 high threshold value  |
| 0x1D3   | [15:0]   | X       | R/W  | STAGE6_MAX_TEMP       | STAGE6 temporary maximum value   |
| 0x1D4   | [15:0]   | X       | R/W  | STAGE6_MIN_WORD0      | STAGE6 minimum value FIFO WORD0  |
| 0x1D5   | [15:0]   | X       | R/W  | STAGE6_MIN_WORD1      | STAGE6 minimum value FIFO WORD1  |
| 0x1D6   | [15:0]   | X       | R/W  | STAGE6_MIN_WORD2      | STAGE6 minimum value FIFO WORD2  |
| 0x1D7   | [15:0]   | X       | R/W  | STAGE6_MIN_WORD3      | STAGE6 minimum value FIFO WORD3  |
| 0x1D8   | [15:0]   | X       | R/W  | STAGE6_MIN_AVG        | STAGE6 average minimum FIFO value  |
| 0x1D9   | [15:0]   | X       | R/W  | STAGE6_LOW_THRESHOLD  | STAGE6 low threshold value   |
| 0x1DA   | [15:0]   | X       | R/W  | STAGE6_MIN_TEMP       | STAGE6 temporary minimum value   |
| 0x1DB   | [15:0]   | X       | R/W  | Unused                |  |

Table 49. STAGE7 Results Registers

| Address | Data Bit | Default | Type | Name                  | Description  |
|---------|----------|---------|------|-----------------------|--|
| 0x1DC   | [15:0]   | X       | R/W  | STAGE7_CONV_DATA      | STAGE7 CDC 16-bit conversion data<br>(copy of data in STAGE7_CONV_DATA register) |
| 0x1DD   | [15:0]   | X       | R/W  | STAGE7_FF_WORD0       | STAGE7 fast FIFO WORD0   |
| 0x1DE   | [15:0]   | X       | R/W  | STAGE7_FF_WORD1       | STAGE7 fast FIFO WORD1   |
| 0x1DF   | [15:0]   | X       | R/W  | STAGE7_FF_WORD2       | STAGE7 fast FIFO WORD2   |
| 0x1E0   | [15:0]   | X       | R/W  | STAGE7_FF_WORD3       | STAGE7 fast FIFO WORD3   |
| 0x1E1   | [15:0]   | X       | R/W  | STAGE7_FF_WORD4       | STAGE7 fast FIFO WORD4   |
| 0x1E2   | [15:0]   | X       | R/W  | STAGE7_FF_WORD5       | STAGE7 fast FIFO WORD5   |
| 0x1E3   | [15:0]   | X       | R/W  | STAGE7_FF_WORD6       | STAGE7 fast FIFO WORD6   |
| 0x1E4   | [15:0]   | X       | R/W  | STAGE7_FF_WORD7       | STAGE7 fast FIFO WORD7   |
| 0x1E5   | [15:0]   | X       | R/W  | STAGE7_SF_WORD0       | STAGE7 slow FIFO WORD0   |
| 0x1E6   | [15:0]   | X       | R/W  | STAGE7_SF_WORD1       | STAGE7 slow FIFO WORD1   |
| 0x1E7   | [15:0]   | X       | R/W  | STAGE7_SF_WORD2       | STAGE7 slow FIFO WORD2   |
| 0x1E8   | [15:0]   | X       | R/W  | STAGE7_SF_WORD3       | STAGE7 slow FIFO WORD3   |
| 0x1E9   | [15:0]   | X       | R/W  | STAGE7_SF_WORD4       | STAGE7 slow FIFO WORD4   |
| 0x1EA   | [15:0]   | X       | R/W  | STAGE7_SF_WORD5       | STAGE7 slow FIFO WORD5   |
| 0x1EB   | [15:0]   | X       | R/W  | STAGE7_SF_WORD6       | STAGE7 slow FIFO WORD6   |
| 0x1EC   | [15:0]   | X       | R/W  | STAGE7_SF_WORD7       | STAGE7 slow FIFO WORD7   |
| 0x1ED   | [15:0]   | X       | R/W  | STAGE7_SF_AMBIENT     | STAGE7 slow FIFO ambient value   |
| 0x1EE   | [15:0]   | X       | R/W  | STAGE7_FF_AVG         | STAGE7 fast FIFO average value   |
| 0x1EF   | [15:0]   | X       | R/W  | STAGE7_CDC_WORD0      | STAGE7 CDC FIFO WORD0  |
| 0x1F0   | [15:0]   | X       | R/W  | STAGE7_CDC_WORD1      | STAGE7 CDC FIFO WORD1  |
| 0x1F1   | [15:0]   | X       | R/W  | STAGE7_MAX_WORD0      | STAGE7 maximum value FIFO WORD0  |
| 0x1F2   | [15:0]   | X       | R/W  | STAGE7_MAX_WORD1      | STAGE7 maximum value FIFO WORD1  |
| 0x1F3   | [15:0]   | X       | R/W  | STAGE7_MAX_WORD2      | STAGE7 maximum value FIFO WORD2  |
| 0x1F4   | [15:0]   | X       | R/W  | STAGE7_MAX_WORD3      | STAGE7 maximum value FIFO WORD3  |
| 0x1F5   | [15:0]   | X       | R/W  | STAGE7_MAX_AVG        | STAGE7 average maximum FIFO value  |
| 0x1F6   | [15:0]   | X       | R/W  | STAGE7_HIGH_THRESHOLD | STAGE7 high threshold value  |
| 0x1F7   | [15:0]   | X       | R/W  | STAGE7_MAX_TEMP       | STAGE7 temporary maximum value   |
| 0x1F8   | [15:0]   | X       | R/W  | STAGE7_MIN_WORD0      | STAGE7 minimum value FIFO WORD0  |
| 0x1F9   | [15:0]   | X       | R/W  | STAGE7_MIN_WORD1      | STAGE7 minimum value FIFO WORD1  |
| 0x1FA   | [15:0]   | X       | R/W  | STAGE7_MIN_WORD2      | STAGE7 minimum value FIFO WORD2  |
| 0x1FB   | [15:0]   | X       | R/W  | STAGE7_MIN_WORD3      | STAGE7 minimum value FIFO WORD3  |
| 0x1FC   | [15:0]   | X       | R/W  | STAGE7_MIN_AVG        | STAGE7 average minimum FIFO value  |
| 0x1FD   | [15:0]   | X       | R/W  | STAGE7_LOW_THRESHOLD  | STAGE7 low threshold value   |
| 0x1FE   | [15:0]   | X       | R/W  | STAGE7_MIN_TEMP       | STAGE7 temporary minimum value   |
| 0x1FF   | [15:0]   | X       | R/W  | Unused                |  |

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC.

Figure 48. 16-Lead Lead Frame Chip Scale Package [LFCSP\_VQ]  
4 mm × 4 mm Very Thin Quad  
(CP-16-13)  
Dimensions shown in millimeters

031006-A

## ORDERING GUIDE

| Model                           | Temperature Range | Serial Interface Description | Package Description | Package Option |
|---------------------------------|-------------------|------------------------------|---------------------|----------------|
| AD7143ACPZ-1REEL <sup>1</sup>   | −40°C to +85°C    | I <sup>2</sup> C Interface   | 16-Lead LFCSP_VQ    | CP-16-13       |
| AD7143ACPZ-1500RL7 <sup>1</sup> | −40°C to +85°C    | I <sup>2</sup> C Interface   | 16-Lead LFCSP_VQ    | CP-16-13       |
| EVAL-AD7143-1EBZ <sup>1</sup>   |                   | I <sup>2</sup> C Interface   | Evaluation Board    |                |

<sup>1</sup> Z = Pb-free part.

## NOTES

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