Programmable Capacitance-to-Digital Converter with Environmental Compensation

Preliminary Technical Data

AD7142/AD7142-1

FEATURES

Programmable capacitance-to-digital converter
- **30 Hz update rate (@ maximum sequence length)**
- **Better than one femto Farad resolution**
- **14 capacitance sensor input channels**
- **No external RC tuning components required**
- **Automatic conversion sequencer**

On-chip automatic calibration logic
- **Automatic compensation for environmental changes**
- **Automatic adaptive threshold and sensitivity levels**

On-chip RAM to store calibration data
SPI®- or I²C®- (AD7142-1) compatible serial interface
Separate V_{DRIVE} level for serial interface
Interrupt output and GPIO
32-lead, 5 mm x 5 mm LFCSP
2.7 V to 3.3 V supply voltage
Low operating current
- **Full power mode: less than1 mA**
- **Low power mode: 50 µA**

APPLICATIONS

Personal music and multimedia players
Cell phones
Digital still cameras
Smart hand-held devices
Television, A/V and remote controls
Gaming consoles

FUNCTIONAL BLOCK DIAGRAM

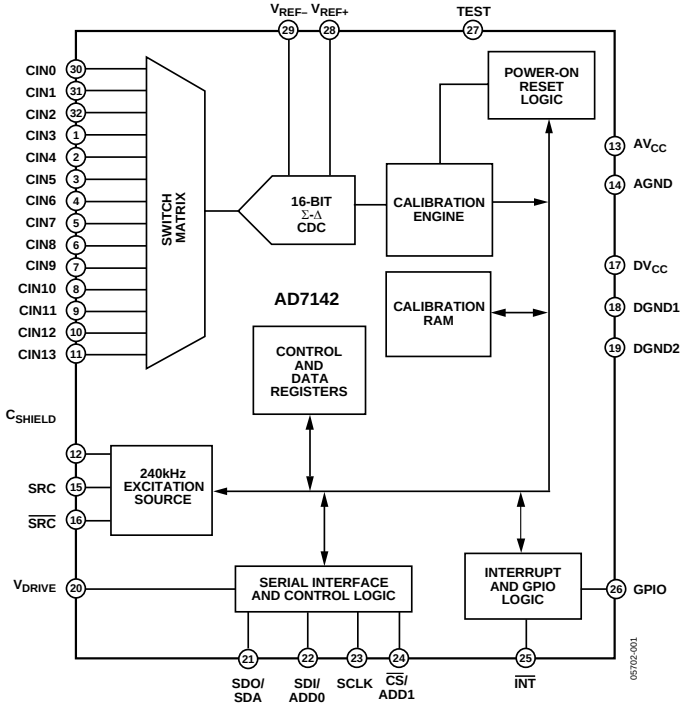

Figure 1.

GENERAL DESCRIPTION

The AD7142 and AD7142-1 are integrated capacitance-to-digital converters (CDCs) with on-chip environmental calibration for use in systems requiring a novel user input method. The AD7142 and AD7142-1 can interface to external capacitance sensors implementing functions such as capacitive buttons, scroll bars, or joypads.

The CDC has 14 inputs, channeled through a switch matrix to a 16-bit, 240 kHz sigma-delta (Σ-Δ) capacitance-to-digital converter. The CDC is capable of sensing changes in the capacitance of the external sensors and uses this information to register a sensor activation. The external sensors can be arranged as a series of buttons, as a scroll bar or wheel, or as a combination of sensor types. By programming the registers, the user has full control over the CDC setup. High resolution scroll bar sensors require software to run on the host processor.

The AD7142 and AD7142-1 have on-chip calibration logic to account for changes in the ambient environment. The calibration sequence is performed automatically and at continuous intervals, while the sensors are not touched. This ensures that there are no false or nonregistering touches on the external sensors due to a changing environment.

The AD7142 has an SPI-compatible serial interface, and the AD7142-1 has an I²C-compatible serial interface. Both versions of AD7142 have an interrupt output, as well as a general-purpose input output (GPIO).

The AD7142 and AD7142-1 are available in a 32-lead, 5 mm × 5 mm LFCSP package and operate from a 2.7 V to 3.3 V supply. The operating current consumption is less than 1 mA, falling to 50 µA in low power mode (conversion interval of 400 ms).

Rev. PrD

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REVISION HISTORY

12/05—Preliminary Version D

7/05—Preliminary Version C

2/05—Preliminary Version B

1/05—Preliminary Version A

SPECIFICATIONS

V_{CC} = 2.7 V to 3.3 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CAPACITANCE-TO-DIGITAL CONVERTER					
Update Rate	30			Hz	Maximum programmed sequence length
Resolution		16		Bit	
Range		±2		pF	
No Missing Codes	16			Bit	Guaranteed by design, but not production tested
Total Unadjusted Error			TBD	fF	
Power Supply Rejection		500		aF/V	
Output Noise (Peak-to-Peak)		10		aF/√Hz	
Parasitic Capacitance			60	pF	Parasitic capacitance to ground, guaranteed by characterization
EXCITATION SOURCE					
Frequency	TBD	240	TBD	kHz	
Output Voltage			AV_{CC}	V	
Short-Circuit Current		10		mA	
Maximum Output Load		500		pF	Capacitance load on source to ground
C_{SHIELD} Output Drive		10		µA	
C_{SHIELD} Bias Level		$AV_{CC}/2$		V	
LOGIC INPUTS (SDI, SCLK, $\overline{CS}$, SDA, GPI, TEST)					
V_{IH} Input High Voltage	0.7 x V_{DRIVE}			V	
V_{IL} Input Low Voltage			0.3 x V_{DRIVE}	V	
I_{IH} Input High Voltage	−1			µA	
I_{IL} Input Low Voltage			1	µA	
Hysteresis		150		mV	
OPEN-DRAIN OUTPUTS (SDO, SDA, $\overline{INT}$)					
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = −1 mA
I_{OH} Output High Leakage Current		0.1	1	µA	V_{OUT} = V_{DRIVE}
LOGIC OUTPUTS					
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = 1 mA, V_{DRIVE} = 1.6 V to DV_{CC} + 0.3 V
V_{OH} Output High Voltage	V_{DRIVE} − 0.6			V	I_{SOURCE} = 1 mA
Floating State Leakage Current			±10	µA	Pin tri-stated
POWER					
AV_{CC}, DV_{CC}	2.7		3.6	V	
V_{DRIVE}	1.65		DV_{CC} + 0.3	V	Serial interface operating voltage
I_{CC}		1	TBD	mA	Full power mode
		50	TBD	µA	Low power mode (conversion delay = 400 ms)
		2	TBD	µA	Full shutdown

SPI TIMING SPECIFICATIONS AD7142

T_A = −40°C to +105°C; V_{DRIVE} = 1.8 V to 3.6 V; AV_{CC}, DV_{CC} = 2.7 V to 3.6 V, unless otherwise noted. Sample tested at 25°C to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.6 V.

Table 2. SPI Timing Specifications

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCLK}[1]	10	kHz min	
	10	MHz max	
t_1	5	ns min	$\overline{CS}$ falling edge to first SCLK falling edge
t_2	20	ns min	SCLK high pulse width
t_3	20	ns min	SCLK low pulse width
t_4	15	ns min	SDI set-up time
t_5	15	ns min	SDI hold time
t_6	20	ns max	SDO access time after SCLK falling edge
t_7	16	ns max	$\overline{CS}$ rising edge to SDO high impedance
t_8	TBD	ns	SCLK rising edge to $\overline{CS}$ high

[1] Mark/space ratio (duty cycle) for the DCLK input is 40/60 to 60/40.

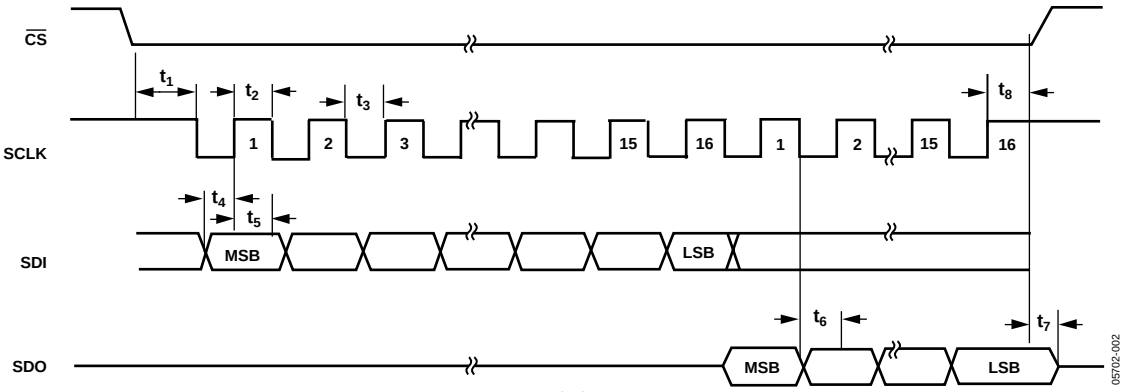


Figure 2. SPI Detailed Timing Diagram

I²C TIMING SPECIFICATIONS AD7142-1

T_A = −40°C to +105°C; V_{DRIVE} = 1.8 V to 3.6 V; AV_{CC}, DV_{CC} = 2.7 V to 3.6 V, unless otherwise noted.
Sample tested at 25°C to ensure compliance. All input signals timed from a voltage level of 1.6 V.

Table 3. I²C Timing Specifications[1]

Parameter	Limit	Unit	Description
f_{SCLK}	400	kHz max	
t_1	0.6	µs min	Start condition hold time, $t_{HD; STA}$
t_2	1.3	µs min	Clock low period, between 10% points, t_{LOW}
t_3	0.6	µs min	Clock high period, between 90% points, t_{HIGH}
t_4	100	ns min	Data setup time , $t_{SU; DAT}$
t_5	50	ns min	Data hold time, $t_{HD; DAT}$
t_6	0.6	µs min	Stop condition setup time, $t_{SU; STO}$
t_7	0.6	µs min	Start condition setup time, $t_{SU; STA}$
t_8	1.3	µs min	Bus free time between stop and start conditions, t_{BUF}
t_R	300	ns max	Clock/data rise time
t_F	300	ns max	Clock/data fall time

[1] Guaranteed by design, but not production tested.

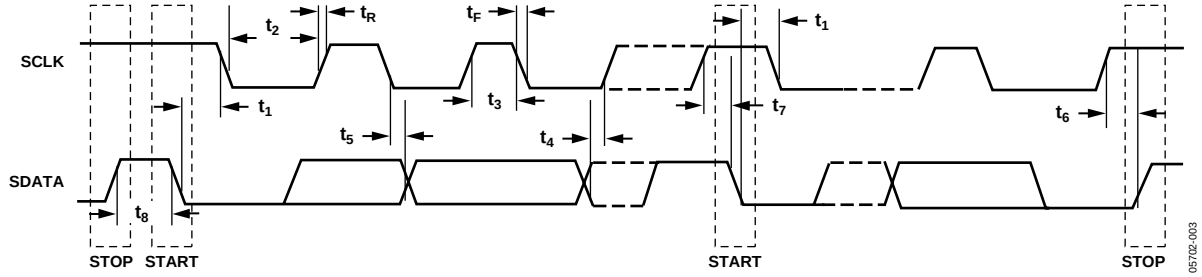


Figure 3. I²C Detailed Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
AV_{CC} to AGND, DV_{CC} to DGND	−0.3 V to +3.6 V
Analog Input Voltage to AGND	−0.3 V to AV_{CC} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to V_{DRIVE} + 0.3 V
Input Current to Any Pin Except Supplies[1]	10 mA
ESD Rating	2.5 kV
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
LFCSP Package	
Power Dissipation	450 mW
θ_{JA} Thermal Impedance	135.7°C/W
IR Reflow Peak Temperature	260°C (±0.5°C)
Lead Temperature (Soldering 10 sec)	300°C

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

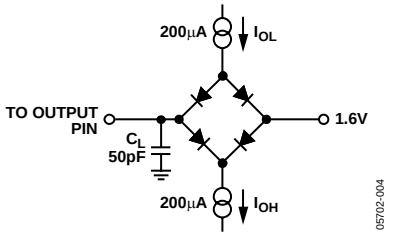


Figure 4. Load Circuit for Digital Output Timing Specifications

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

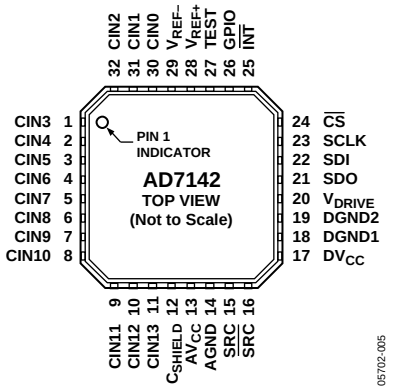


Figure 5. AD7142, 32-Lead LFCSP Pin Configuration

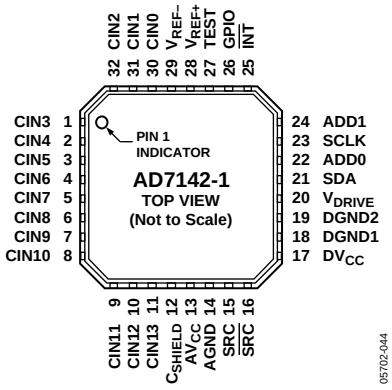


Figure 6. AD7142-1, 32-Lead LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Name	Description
1	CIN3	Capacitance Sensor Input.
2	CIN4	Capacitance Sensor Input.
3	CIN5	Capacitance Sensor Input.
4	CIN6	Capacitance Sensor Input.
5	CIN7	Capacitance Sensor Input.
6	CIN8	Capacitance Sensor Input.
7	CIN9	Capacitance Sensor Input.
8	CIN10	Capacitance Sensor Input.
9	CIN11	Capacitance Sensor Input.
10	CIN12	Capacitance Sensor Input.
11	CIN13	Capacitance Sensor Input.
12	C_{SHIELD}	CDC Shield Potential Output. Requires 10 nF capacitor to ground. Connect to external shield.
13	AV_{CC}	CDC Supply Voltage.
14	AGND	Analog Ground Reference Point for All CDC Circuitry. Tie to analog ground plane.
15	SRC	CDC Excitation Source Output.
16	$\overline{SRC}$	Inverted Excitation Source Output.
17	DV_{CC}	Digital Core Supply Voltage.
18	DGND1	Digital Ground.
19	DGND2	Digital Ground.
20	V_{DRIVE}	Serial Interface Operating Voltage Supply.
21	SDO	AD7142 SPI Serial Data Output.
	SDA	AD7142-1 I^2C Serial Data Input/Output. SDA requires pull-up resistor.
22	SDI	AD7142 SPI Serial Data Input.
	ADD0	AD7142-1 I^2C Address Bit 0.
23	SCLK	Clock Input for Serial Interface.
24	$\overline{CS}$	AD7142 SPI Chip Select Signal.
	ADD1	AD7142-1 I^2C Address Bit 1.
25	$\overline{INT}$	General Purpose Interrupt Output. Programmable polarity. Requires pull-up resistor.
26	GPIO	Programmable GPIO.
27	TEST	Factory Test Pin. Tie to ground.
28	V_{REF+}	CDC Positive Reference Input. Normally tied to analog power.
29	V_{REF-}	CDC Negative Reference Input. Tie to analog ground.
30	CIN0	Capacitance Sensor Input.
31	CIN1	Capacitance Sensor Input.
32	CIN2	Capacitance Sensor Input.

TYPICAL PERFORMANCE CHARACTERISTICS

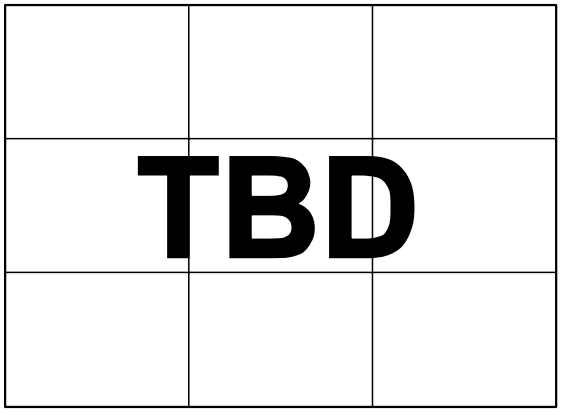


Figure 7. Supply Current vs. AV_{DD}

THEORY OF OPERATION

The AD7142 and AD7142-1 are capacitance-to-digital converters (CDCs) with on-chip environmental compensation, intended for use in portable systems requiring high resolution user input. The internal circuitry consists of a 16-bit, Σ-Δ converter that converts a capacitive input signal into a digital value. There are 14 input pins on the AD7142 and AD7142-1, CIN0 to CIN13. A switch matrix routes the input signals to the CDC. The result of each capacitance-to-digital conversion is stored in on-chip registers. The host subsequently reads the results over the serial interface. The AD7142 contains an SPI interface and the AD7142-1 has an I²C interface ensuring that the parts are compatible with a wide range of host processors. Because the AD7142 and AD7142-1 are identical parts, with the exception of the serial interface, AD7142 refers to both the AD7142 and AD7142-1 throughout this data sheet.

The AD7142 interfaces with to up to 14 external capacitance sensors. These sensors can be arranged as buttons, scroll bars, joypads, or as a combination of sensor types. The external sensors consist of electrodes on a 2- or 4-layer PCB that interfaces directly to the AD7142.

The AD7142 can be set up to implement any set of input sensors by programming the on-chip registers. The registers can also be programmed to control features such as averaging, offsets, and gains for each of the external sensors. There is a sequencer on-chip to control how each of the capacitance inputs is polled.

The AD7142 has on-chip digital logic and 528 words of RAM that are used for environmental compensation. The effects of humidity, temperature, and other environmental factors can effect the operation of capacitance sensors. Transparent to the user, the AD7142 performs continuous calibration to compensate for these effects, allowing the AD7142 to give error-free results at all times.

The AD7142 requires some minor companion software that runs on the host or other microcontroller to implement sensor functions such as a scroll bar or joypad. However, no companion software is required to implement buttons, including 8-way button functionality. The algorithms required for button sensors are implemented in digital logic on-chip.

The AD7142 can be programmed to operate in either always powered mode, or in an automatic wake-up mode. The auto wake-up mode is particularly suited for portable devices that require low power operation giving the user significant power savings coupled with full functionality.

The AD7142 has a general interrupt output, $\overline{\text{INT}}$, to indicate when new data has been placed into the registers. $\overline{\text{INT}}$ is used to interrupt the host on sensor activation. The AD7142 operates from a 2.7 V to 3.6 V supply, and is available in a 32-lead, 5 mm × 5 mm LFCSP.

CAPACITANCE SENSING THEORY

The AD7142 uses a method of sensing capacitance known as the shunt method. Using this method, an excitation source is connected to a transmitter generating an electric field to a receiver. The field lines measured at the receiver are translated into the digital domain by a Σ-Δ converter. When a finger, or other grounded object, interferes with the electric field, some of the field lines are shunted to ground and do not reach the receiver (see Figure 8). Therefore, the total capacitance measured at the receiver decreases when an object comes close to the induced field.

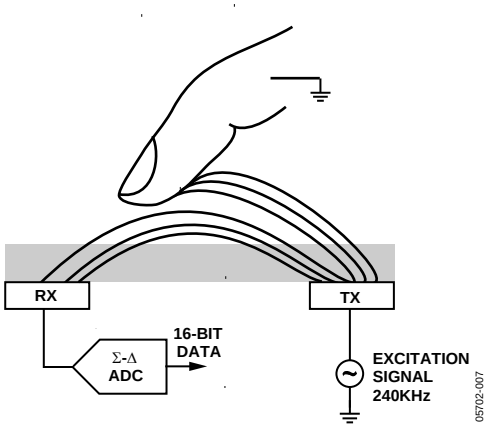


Figure 8. Sensing Capacitance Method

In practice, the excitation source and Σ-Δ ADC are implemented on the AD7142, while the transmitter and receiver are constructed on a PCB that makes up the external sensor.

Registering a Sensor Activation

When a sensor is approached, the total capacitance associated with that sensor, measured by the AD7142, changes. When the capacitance changes to such an extent that a set threshold is exceeded, the AD7142 registers this as a sensor touch.

For example, consider the case of two button sensors that are connected to the AD7142 in a differential manner. When one button is activated, the AD7142 registers an increase in capacitance; if the other button is activated, the AD7142 registers a decrease in capacitance. If neither of the buttons are activated, the AD7142 measures the background or ambient capacitance level.

Preprogrammed threshold levels are used to determine if a change in capacitance is due to a button being activated. If the capacitance exceeds one of the threshold limits, the AD7142 registers this as a true button activation.

The same thresholds principle is used to determine if other types of sensors, such as sliders or joypads, are activated.

Complete Solution for Capacitance Sensing

Analog Devices provides a complete solution for capacitance sensing. The two main elements to the solution are the sensor PCB and the AD7142.

If the application requires sensors in the shape of a slider or joypad, software is required that runs on the host processor. (No software is required for button sensors.) The software typically requires 3 kB of code and 500 bytes of data memory for a slider sensor.

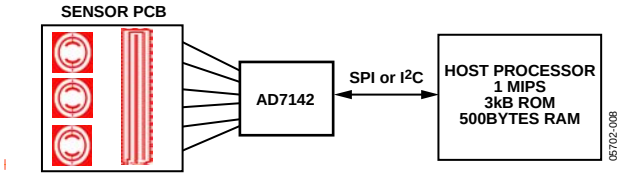


Figure 9. 3-Part Capacitance Sensing Solution

Analog Devices supplies the sensor PCB design to the customer based on the customer's specifications, and supplies any necessary software on an open-source basis. Standard sensor designs are also available as PCB library components.

OPERATING MODES

The AD7142 has three operating modes. Full power mode, where the device is always fully powered, is suited for applications where power is not a concern, for example game consoles that have an ac power supply. Low power mode, where the part automatically powers down, is tailored to give significant power savings over full power mode, and is suited for mobile applications where power must be conserved. The AD7142 also has a complete shutdown mode.

The POWER_MODE bits (Bit 0 and Bit 1) of the control register set the operating mode on the AD7142. The control register is at Address 0x000.

Table 6. POWER_MODE Settings

POWER_MODE Bits	Operating Mode
00	Full power mode
01	Full shutdown mode
10	Low power mode
11	Full shutdown mode

Table 6 shows the POWER_MODE settings for each operating mode. To put the AD7142 into shutdown mode, set the POWER_MODE bits to either 01 or 11.

The power-on default setting of the POWER_MODE bits is 00, full power mode.

Full Power Mode

In full power mode, all sections of the AD7142 remain fully powered at all times. While a sensor is being touched, the AD7142 processes the sensor data. If no sensor is touched, the AD7142 measures the ambient capacitance level and uses this data for the on-chip compensation routines. In full power mode, the AD7142 converts at a constant rate. See the CDC Conversion Time section for more information.

Low Power Mode

When in low power mode, the AD7142 POWER_MODE bits are set to 10 upon device initialization. If the external sensors are not touched, the AD7142 reduces its conversion frequency, thereby greatly reducing its power consumption. The part remains in a low power state while the sensors are not touched. Every 400 ms, the AD7142 performs a conversion and uses this data to update the compensation logic. When an external sensor is touched, the AD7142 begins a conversion sequence every 40 ms to read back data from the sensors. In low power mode, the total current consumption of the AD7142 is an average of the current used during a conversion, and the current used while the AD7142 is waiting for the next conversion to begin. For example, when the low power mode conversion interval is 400 ms, the AD7142 uses typically 0.9 mA current for 40 ms, and 15 µA for 360 ms of the conversion interval. (Note that these conversion timings can be altered through the register settings. See the CDC Conversion Time section for more information.)

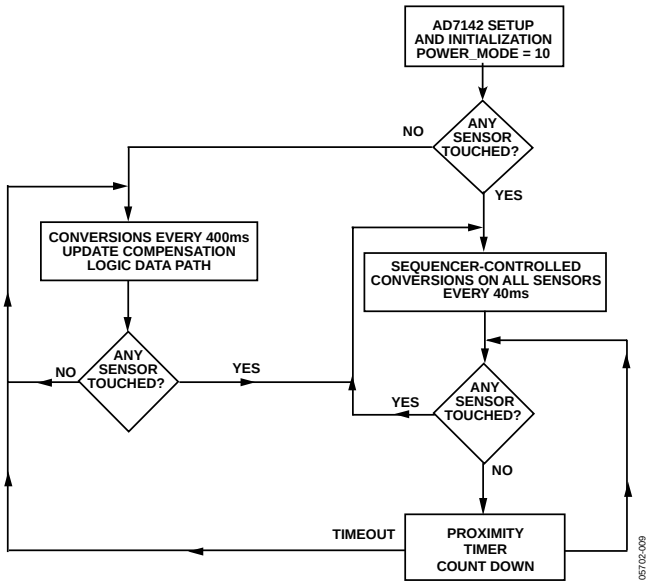


Figure 10. Low Power Mode Operation

CAPACITANCE SENSOR INPUT CONFIGURATION

Each stage of the AD7142 capacitance sensors can be uniquely configured by using the registers in Table 53 and Table 54. These registers are used to configure input pin connection set ups, sensor offsets, sensor sensitivities, and sensor limits for each stage. Apply this feature to optimize the function of each sensor to the application. For example, a button sensor connected to STAGE0 may require a different sensitivity and offset values than a button with a different function that is connected to a different stage.

CIN INPUT MULTIPLEXER SETUP

The CIN_CONNECTION_SETUP registers in Table 53 list the different options that are provided for connecting the sensor input pin to the CDC converter.

The AD7142 has an on-chip multiplexer to route the input signals from each pin to the input of the converter. Each input pin can be tied to either the negative or the positive input of the CDC, or it can be left floating. Each input can also be internally connected to the C_{SHIELD} signal to help prevent cross coupling. If an input is not used, always connect it to $C_{SHIELD.}$

For each input pin, CIN0 to CIN13, the multiplexer settings can be set on a per sequencer stage basis. For example, CIN0 is connected to the negative CDC input for conversion STAGE1, left floating for sequencer STAGE1, and so on for all twelve conversion stages.

Two bits in each register control the mux setting for the input pin.

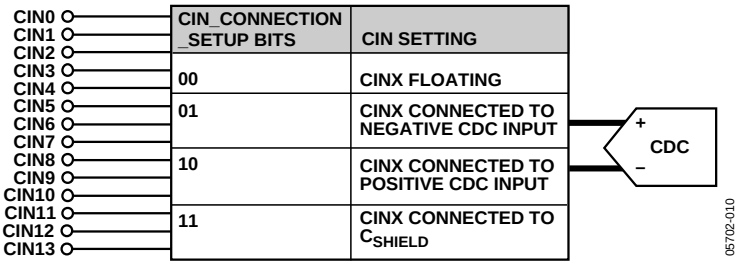


Figure 11. Input Mux Configuration Options

CAPACITIANCE-TO-DIGITAL CONVERTER

The capacitance-to-digital converter on the AD7142 has a sigma-delta (Σ-Δ) architecture with 16-bit resolution. There are 14 possible inputs to the CDC that are connected to the input of the converter through a switch matrix. The sampling frequency of the CDC is 240 kHz.

OVERSAMPLING THE CDC OUTPUT

It is possible to sample the result of any CDC conversion at a rate less than 240 kHz. The decimation rate, or over–sampling ratio, is determined by Bits[9:8] of the control register, as listed in Table 7.

Table 7. CDC Decimation Rate

Decimation Bit Value	Decimation Rate	CDC Sample Rate
00	256	312.5 Hz
01	128	625 Hz
10	64	1.25 kHz
11	64	1.25 kHz

The decimation process on the AD7142 is an averaging process where a number of samples are taken and the averaged result is output. The amount of samples taken is set equal to the decimation rate, so 256, 128, or 64 samples are averaged to obtain the CDC output.

The decimation process reduces the amount of noise present in the final CDC result. However, the higher the decimation rate, the lower the sampling frequency, thus, a tradeoff is required between a noise-free signal and speed of sampling.

CAPACITANCE SENSOR OFFSET CONTROL

Apply the STAGE_OFFSET registers to null any capacitance sensor offsets associated with printed circuit board parasitic capacitance, or capacitance due to any other source, such as connectors. This is only required once during the initial capacitance sensor characterization.

A simplified block diagram in Figure 12 shows how to apply the STAGE_OFFSET registers to null the offsets. The 7-bit POS_AFE_OFFSET and NEG_AFE_OFFSET registers provide 0.16 pF resolution offset adjustment over a range of 20 pF. Apply the positive and negative offsets to either the positive or the negative CDC input using the NEG_AFE_OFFSET and POS_AFE_OFFSET registers.

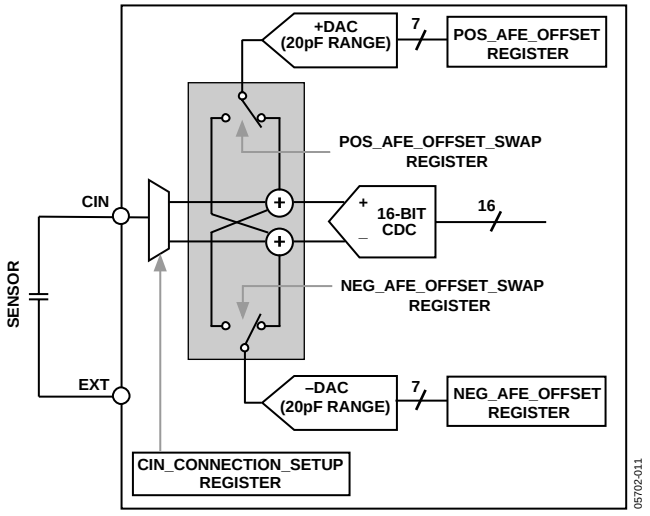


Figure 12. Analog Front End Offset Control

CONVERSION SEQUENCER

The AD7142 has an on-chip sequencer to implement conversion control for the input channels. Up to 12 conversion stages can be performed in sequence. By using the Bank 2 registers, each stage can be uniquely configured to support multiple capacitance sensor interface requirements. For example, a slider sensor can be assigned to STAGE1 with a button sensor assigned to STAGE2.

The AD7142 on-chip sequencer controller provides conversion control beginning with STAGE0. Figure 13 shows a block diagram of the CDC conversion stages and CIN inputs. A conversion sequence is defined as a sequence of CDC conversion starting at STAGE0 and ending at the stage determined by the value programmed in the SEQUENCE_STAGE_NUM register. In Figure 14, the conversion sequence is from STAGE0 through STAGE5. Depending on the number and type of capacitance sensors that are used, not all conversion stages are required. Use the SEQUENCE_STAGE_NUM register to set the number of conversions in one sequence, depending on the sensor interface requirements. For example, this register would be set to 5 if the CIN inputs were mapped to only six stages as shown in Figure 14. In addition, set the STAGE_CAL_EN registers according to the number of stages that are used.

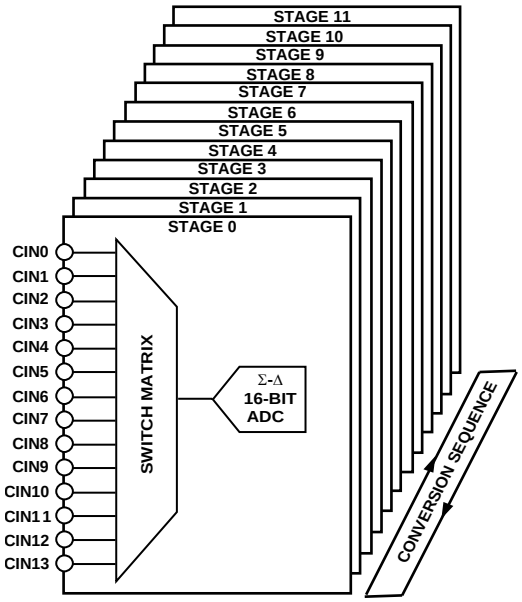


Figure 13. AD7142 CDC Conversion Stages

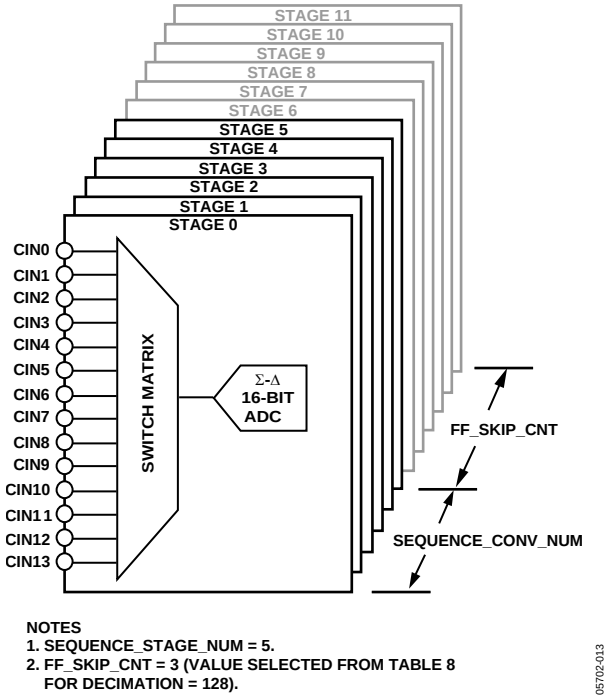


Figure 14. Example Using SEQUENCE_CON_NUM and FF_SKIP_CNT Registers

The number of required conversion stages depends wholly on the number of sensors attached to the AD7142. Figure 15 shows how many conversion stages are required for each sensor, and how many inputs to the AD7142 each sensor requires.

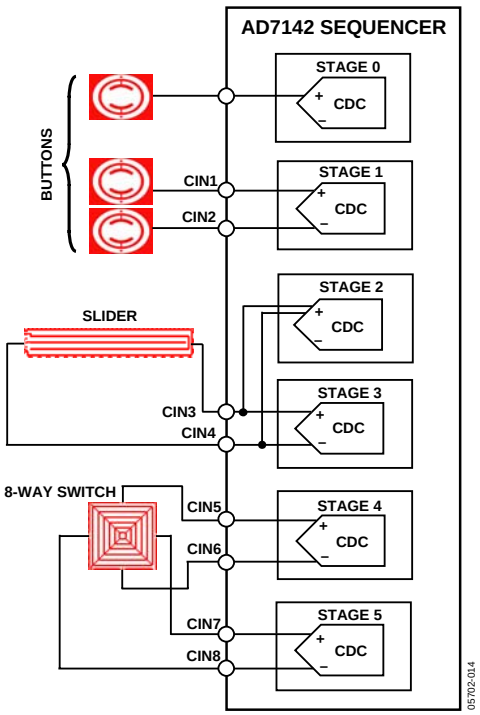


Figure 15. Sequencer Setup for Sensors

A button sensor generally requires one sequencer stage; however, it is possible to configure two button sensors to operate differentially. Only one button from the pair can be activated at a time; pressing both buttons together results in neither button being activated. This configuration requires one conversion stage.

A slider sensor requires two stages: one stage for sensor activation; the other stage for measuring positional data from the slider. In Figure 15, the slider activation uses STAGE2, while the positional data uses STAGE3.

The 8-way switch is made from two pairs of differential buttons. It, therefore, requires two conversion stages, one for each of the differential button pairs. The buttons are orientated so that one pair makes up the top and bottom portions of the 8-way switch; the other pair makes up the left and right portions of the 8-way switch.

CDC CONVERSION TIME

The time required for one complete measurement by the CDC is defined as the CDC conversion time. For optimal system performance, configure the AD7142 CDC conversion time within a range of 35 ms to 40 ms. The SEQUENCE_STAGE_NUM, FF_SKIP_CNT, and DECIMATION registers determine the conversion time as listed in Table 8.

Table 8. CDC Conversion Times for Full Power Mode

	DECIMATION = 64		DECIMATION = 128		DECIMATION = 256	
SEQUENCE_STAGE_NUM	FF_SKIP_CNT	CDC Conversion Time (ms)	FF_SKIP_CNT	CDC Conversion Time (ms)	FF_SKIP_CNT	CDC Conversion Time (ms)
0	11	9.2	11	18.4	11	36.5
1	11	18.4	11	36.8	5	36.5
2	11	27.6	7	36.8	3	36.5
3	11	36.8	5	36.8	2	36.5
4	9	38.4	4	38.4	2	46.0
5	7	36.8	3	36.8	1	36.8
6	6	37.6	2	32.2	1	43.0
7	5	36.8	2	36.8	1	49.1
8	4	34.5	2	41.4	0	27.6
9	4	38.4	1	30.7	0	30.7
10	3	33.8	1	33.8	0	33.7
11	3	36.8	1	36.8	0	36.8

For example, while operating with a decimation rate of 128, if the SEQUENCE_STAGE_NUM register is set to 5 for the conversion of six stages in a sequence, the FF_SKIP_CNT register should be set to 3 resulting in a conversion time of 36.8 ms. This example is shown in Figure 14.

Determining the FF_SKIP_CNT value is only required one time during the initial setup of the capacitance sensor interface. This value determines which CDC samples are not used (skipped) in the proximity detection fast FIFO.

Full Power Mode CDC Conversion Time

The full power mode CDC conversion time is set by configuring the SEQUENCE_STAGE_NUM, FF_SKIP_CNT and DECIMATION registers as outlined in Table 8.

Figure 16 shows a simplified timing diagram of the full power CDC conversion time. The full power mode CDC conversion time t_{CONV_FP} is set using Table 8.

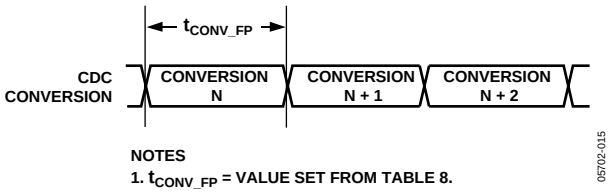


Figure 16. Full Power Mode CDC Conversion Time

Low Power Mode CDC Conversion Time with Delay

The frequency of each CDC conversion while operating in the low power automatic wake up mode is controlled by using the LP_CONV_DELAY register bits (Bits[3:2] in Register 0x00), in addition to the registers listed in Table 8. This feature provides some flexibility for optimizing the conversion time to meet system requirements vs. AD7142 power consumption. For example, maximum power savings is achieved when the LP_CONV_DELAY is set to 3. With a setting of 3, the AD7142 automatically wakes up, performing a conversion every 400 ms.

Table 9. LP_CONV_DELAY Settings

LP_CONV_DELAY BITS	Delay Between Conversions
00	100 ms
01	200 ms
10	300 ms
11	400 ms

Figure 17 shows a simplified timing example of the low power CDC conversion time. As shown, the low power CDC conversion time is set by t_{CONV_FP} and the LP_CONV_DELAY register.

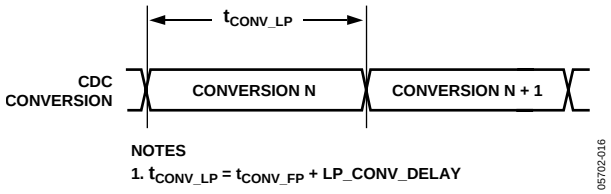


Figure 17. Low Power Mode CDC Conversion Time CDC Conversion Results

CDC CONVERSION RESULTS

Certain applications, such as a slider function, require reading back the CDC conversion results for host processing. The registers required for host processing are located in Register Bank 3. The host processes the data read back from these registers to determine relative position information.

In addition to the results registers in Bank 3, the AD7142 provides the 16-bit CDC output data directly starting at Address 0x00B of Register Bank 1. Reading back the CDC 16-bit conversion data register allows for customer specific application data processing.

NON-CONTACT PROXIMITY DETECTION

The AD7142 internal signal processing continuously monitors all capacitance sensors for non-contact proximity detection. This feature provides the ability to detect when a user is approaching a sensor, at which time all internal calibration is immediately disabled while the AD7142 is automatically configured to detect a valid contact.

The proximity control register bits are described in Table 10. The FP_PROXIMITY_CNT and LP_PROXIMITY_CNT register bits control how long the calibration disable period is after proximity is detected. The calibration is disabled during this time and enabled again at the end of this period provided that the user is no longer approaching, or in contact with, the sensor. Figure 18 and Figure 19 show examples of how these registers are used to set the full and low power mode calibration disable periods.

Recalibration

In the event of a very long proximity detection event, such as a user hovering over a sensor for a long period of time, the FP_PROXIMITY_RECAL and LP_PROXIMITY_RECAL bits in register 0x004 can be applied to force a recalibration. This feature ensures that the ambient values are recalibrated regardless of how long the user may be hovering over a sensor. A recalibration ensures maximum AD7142 sensor performance. Figure 20 and Figure 21 show examples of using the FP_PROXIMITY_RECAL and LP_PROXIMITY_RECAL register bits to force a recalibration while operating in the full and low power modes. These figures show a user approaching a sensor followed by the user leaving the sensor while the proximity detection remained active after the user left the sensor. This situation could occur if the user interaction created some moisture on the sensor for example thus causing the new sensor value to be different from the expected value. In this case, the internal recalibration would be applied to automatically recalibrate the sensor. The force calibration event takes two interrupt cycles: nothing should be read from or written to the AD7142 during the recalibration period.

Proximity Sensitivity

There are two conditions that set the internal proximity detection signal as described in Figure 22 with Comparator 1 and Comparator 2. Comparator 1 detects when a user is approaching a sensor. The sensitivity of Comparator 1 is controlled by PROXIMITY_DETECTION_RATE. For example, if PROXIMITY_DETECTION_RATE is set to 4, the Proximity 1 signal is set when the absolute difference between WORD1 and WORD3 exceed four LSB codes. Comparator 2 detects when a user is hovering over a sensor or approaches a sensor very slowly. The sensitivity of Comparator 2 is controlled by the PROXIMITY_RECAL_LVL in Register 0x003. For example, if PROXIMITY_RECAL_LVL is set to 75, the Proximity 2 signal is set when the absolute difference between the fast filter average value and the ambient value exceeds 75 LSB codes.

Table 10. Proximity Control Registers (Refer to Figure 22)

Register	Length (Bits)	Register Address	Description
FP_PROXIMITY_CNT	4	0x002	Full power mode proximity control
LP_PROXIMITY_CNT	4	0x002	Low power mode proximity control
FP_PROXIMITY_RECAL	8	0x004	Full power mode proximity recalibration control
LP_PROXIMITY_RECAL	6	0x004	Low power mode proximity recalibration control
PROXIMITY_RECAL_LVL	8	0x003	Proximity recalibration level
PROXIMITY_DETECTION_RATE	6	0x003	Proximity detection rate

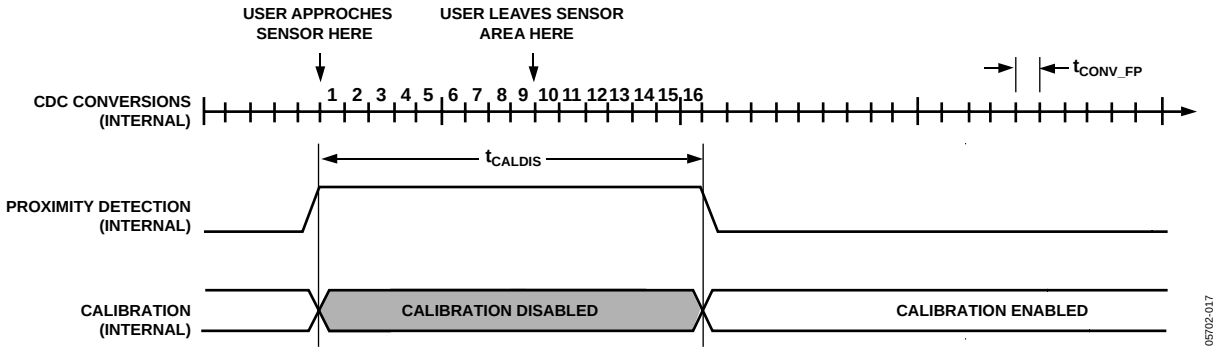


Figure 18. Full Power Mode Proximity Detection Example with FP_PROXIMITY = 1

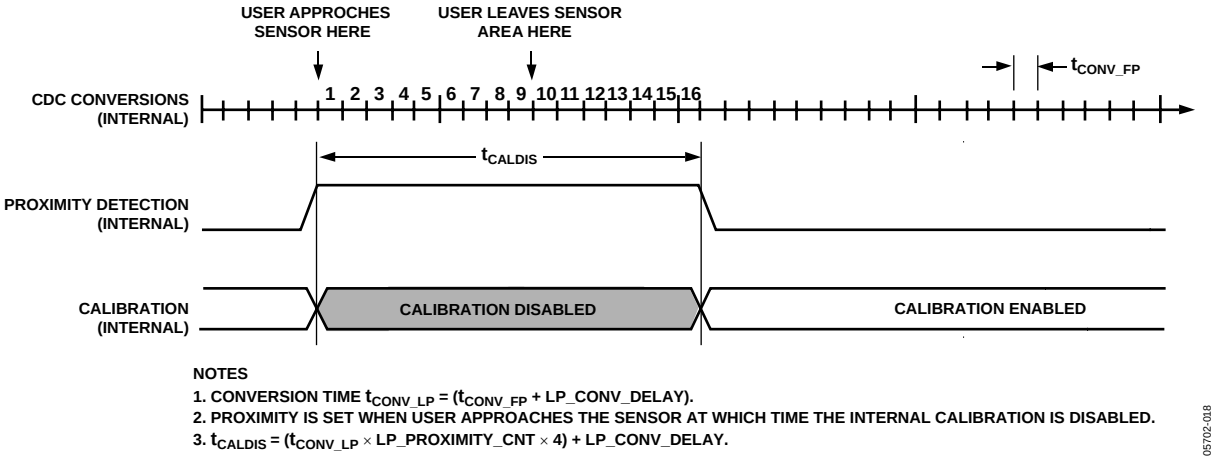


Figure 19. Low Power Mode Proximity Detection with LP_PROXIMITY = 4 and LP_CONV_DELAY = 0

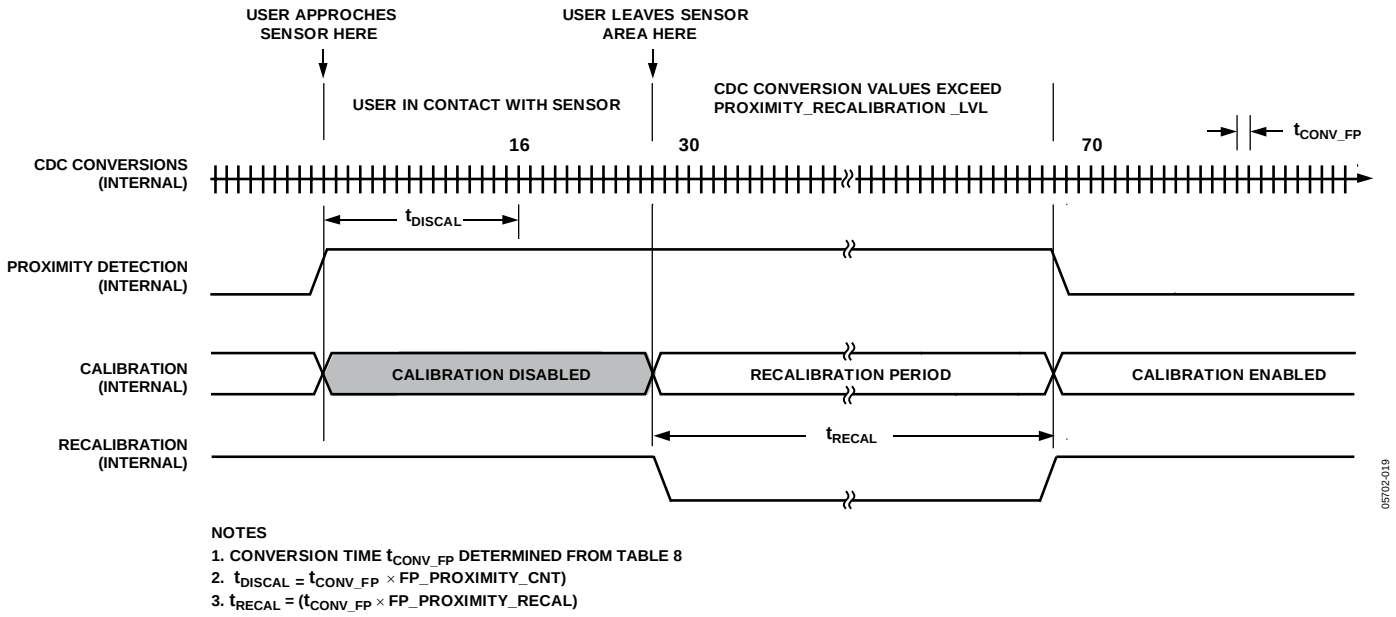


Figure 20. Full Power Mode Proximity Detection with Forced Recalibration Example with FP_PROXIMITY = 1 and FP_PROXIMITY_RECAL = 40

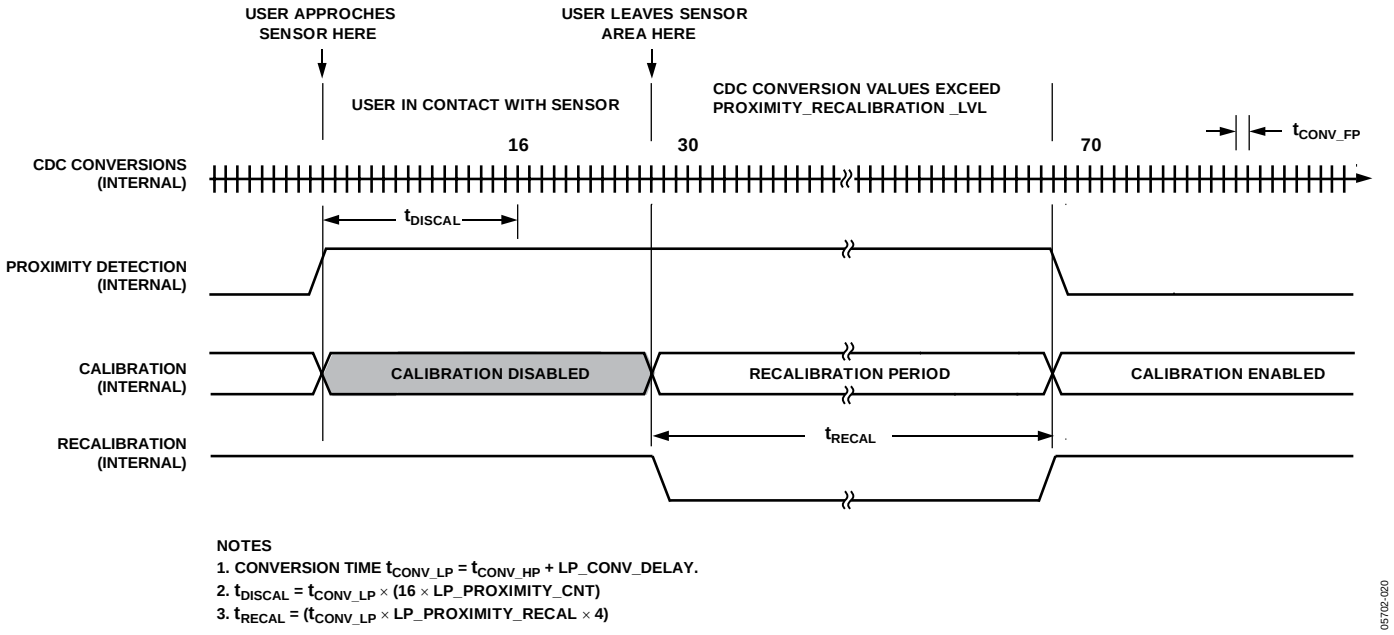
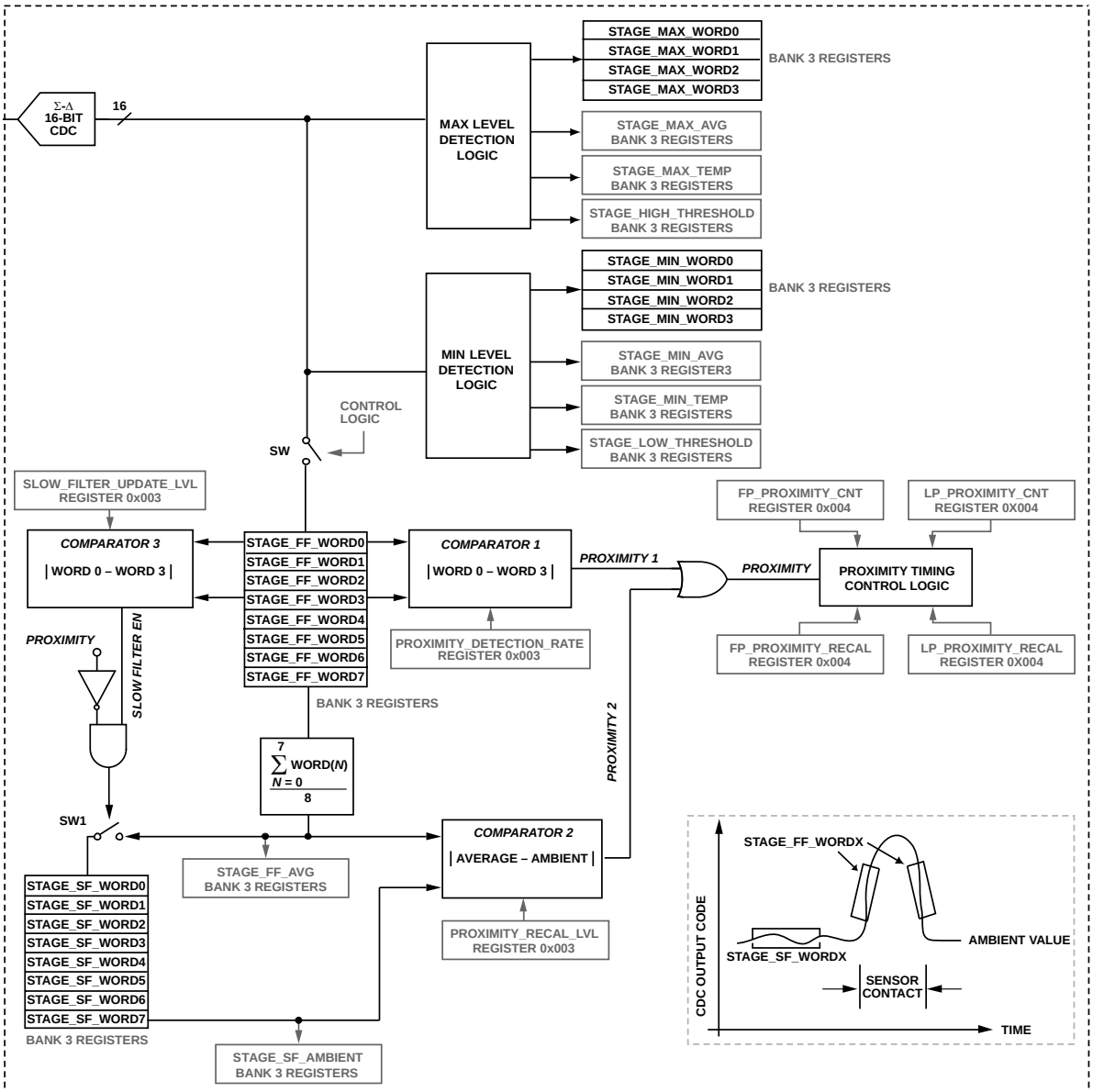


Figure 21. Low Power Mode Proximity Detection with Forced Recalibration Example with LP_PROXIMITY = 4 and LP_PROXIMITY_RECAL = 10



NOTES

1. ***SLOW FILTER EN*** **IS SET AND SW1 IS CLOSED WHEN /WORD 0–WORD 3/ EXCEEDS THE VALUE PROGRAMMED IN THE SLOW_FILTER_UPDATE REGISTER PROVIDING *PROXIMITY* IS NOT SET.**
2. ***PROXIMITY 1*** **IS SET WHEN /WORD 0–WORD 3/ EXCEEDS THE VALUE PROGRAMMED IN THE PROXIMITY_DETECTION_RATE REGISTER.**
3. ***PROXIMITY 2*** **IS SET WHEN /AVERAGE–AMBIENT/ EXCEEDS THE VALUE PROGRAMMED IN THE PROXIMITY_RECAL_LVL REGISTER.**
4. **DESCRIPTION OF COMPARATOR FUNCTIONS:**
   COMPARATOR 1: USED TO DETECT WHEN A USER IS APPROACHING OR LEAVING A SENSOR.
   COMPARATOR 2: USED TO DETECT WHEN A USER IS HOVERING OVER A SENSOR, OR APPROACHING A SENSOR VERY SLOWLY.
   ALSO USED TO DETECT IF THE SENSOR AMBIENT LEVEL HAS CHANGED AS A RESULT OF THE USER INTERACTION.
   FOR EXAMPLE, HUMIDITY OR DIRT LEFT BEHIND ON SENSOR.
   COMPARATOR 3: USED TO ENABLE THE SLOW FILTER UPDATE RATE. THE SLOW FILTER IS UPDATED WHEN *SLOW FILTER EN* IS SET AND *PROXIMITY* IS NOT SET.

Figure 22. AD7142 Proximity Detection and Environmental Calibration

ENVIRONMENTAL CALIBRATION

The AD7142 provides on-chip capacitance sensor calibration to automatically adjust for environmental conditions that have an effect on the capacitance sensor ambient levels. Capacitance sensor output levels are sensitive to temperature, humidity, and in some cases, dirt. The AD7142 achieves optimal and reliable sensor performance by continuously monitoring the CDC ambient levels and correcting for any changes by adjusting the initial STAGE_OFFSET_HIGH and STAGE_OFFSET_LOW register values. The CDC ambient level is defined as the capacitance sensor output level during periods when the user is not approaching or in contact with the sensor.

The compensation logic runs automatically on every conversion after configuration when the AD7142 is not being touched. This allows the AD7142 to account for rapidly changing environmental conditions.

The ambient compensation control registers give the host access to general setup and controls for the compensation algorithm. The RAM stores the compensation data for each conversion stage, as well as setup information specific to each stage.

Figure 23 shows an example of an ideal capacitance sensor behavior where the CDC ambient level remains constant regardless of the environmental conditions. In this example, the initial settings programmed in the STAGE_OFFSET_HIGH and STAGE_OFFSET_LOW registers are sufficient to detect a sensor contact resulting with the AD7142 asserting the $\overline{\text{INT}}$ output when the offset levels are exceeded.

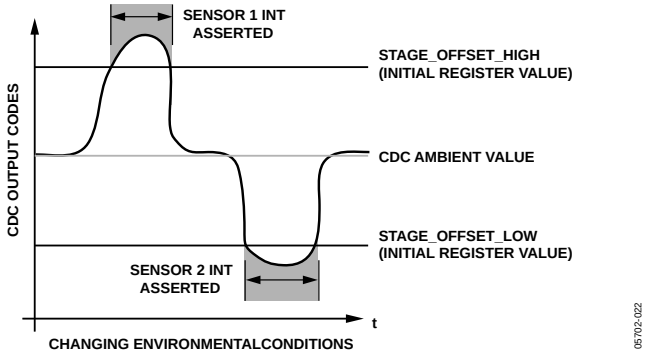


Figure 23. Ideal Sensor Behavior with a Constant Ambient Level

Capacitance Sensor Behavior Without Calibration

Figure 24 shows the typical behavior of a capacitance sensor with no applied calibration. This figure shows ambient levels drifting over time as environmental conditions change. The ambient level drift has resulted in the detection of a missed user contact on Sensor 2. This is a result of the initial low offset level remaining constant while the ambient levels drifted upward beyond the detection range. The Capacitance Sensor Behavior with Calibration section describes how the AD7142 adaptive calibration algorithm prevents errors such as this from occurring.

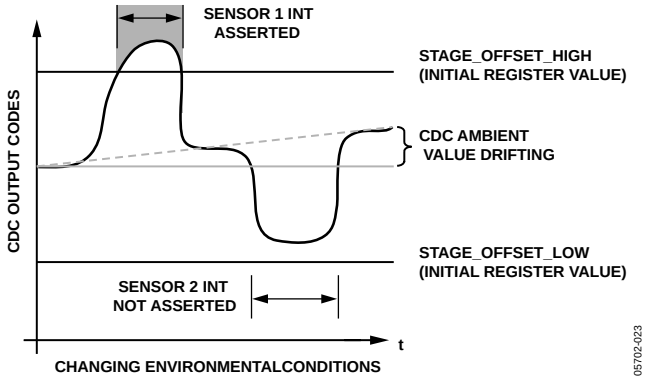


Figure 24. Typical Sensor Behavior without Calibration Applied

Capacitance Sensor Behavior with Calibration

The AD7142 on-chip adaptive calibration algorithm prevents sensor detection errors such the one shown in Figure 24. This is achieved by monitoring the CDC ambient levels and internally adjusting the initial offset level register values according to the amount of ambient drift measured on each sensor. This closed loop routine ensures the reliability and repeatability operation of every sensor connected to the AD7142 under dynamic environmental conditions. Figure 25 shows a simplified example of how the AD7142 applies the adaptive calibration process resulting in no interrupt errors under changing CDC ambient levels due to environmental conditions.

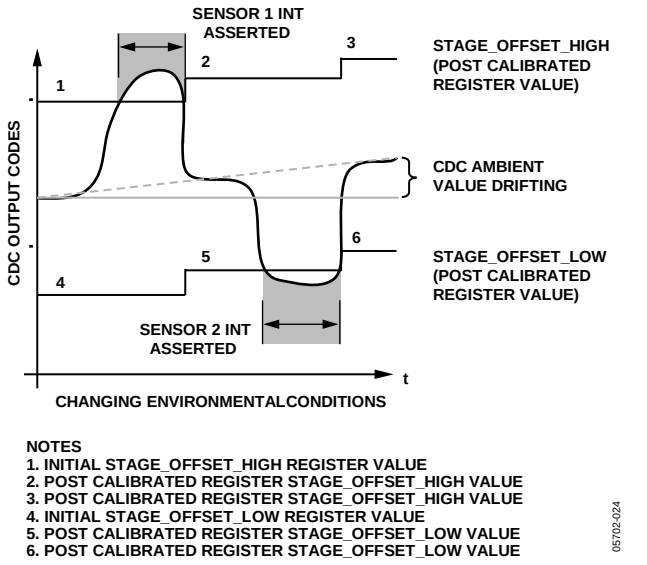


Figure 25. Typical Sensor Behavior with Calibration Applied on the Data Path

ADAPTIVE THRESHOLD AND SENSITIVITY

The AD7142 provides an on-chip self-learning adaptive threshold and sensitivity algorithm. This algorithm continuously monitors the output levels of each sensor and automatically rescales the threshold levels proportionally to the sensor area covered by the user. As a result, the AD7142 maintains optimal threshold and sensitivity levels for all types of users regardless of their finger sizes.

The threshold level is always referenced from the ambient level and is defined as the CDC converter output level that must be exceeded for a valid sensor contact. The sensitivity level is defined as how sensitive the sensor is before a valid contact is registered.

Figure 26 provides an example of how the adaptive threshold and sensitivity algorithm works. In a case where the adaptive threshold and sensitivity algorithm are disabled, the positive and negative sensor threshold levels are set by the STAGE_OFFSET_HIGH and STAGE_OFFSET_LOW initial values. Reference A in Figure 26 shows that this results in an under sensitive threshold level for a small finger user, demonstrating the disadvantages of a fixed threshold level. By enabling the adaptive threshold and sensitivity algorithm, the positive and negative threshold levels are determined by the POS_THRESHOLD_SENSITIVITY and NEG_THRESHOLD_SENSITIVITY register values and the most recent average maximum sensor output value. These registers can be used to select 16 different positive and negative sensitivity levels ranging between 25% and 95.32% of the most recent average maximum output level referenced from the ambient value. Reference B shows that the positive adaptive threshold level is set at almost mid sensitivity with a 62.51% threshold level by setting POS_THRESHOLD_SENSITIVITY = 1000. Figure 26 also provides a similar example for the negative threshold level with NEG_THRESHOLD_SENSITIVITY = 0001.

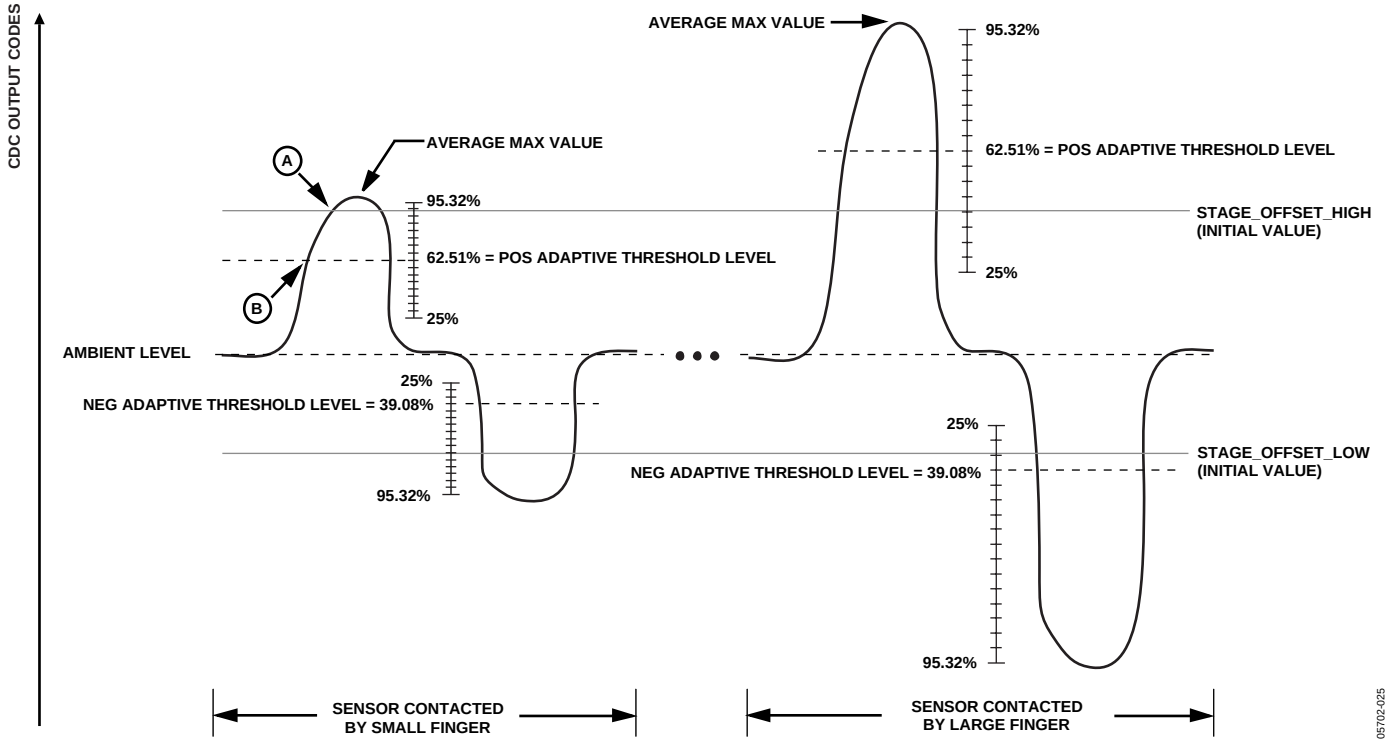


Figure 26. Threshold Sensitivity Example with POS_THRESHOLD_SENSITIVITY = 1000 and NEG_THRESHOLD_SENSITIVITY = 0011

INTERRUPT OUTPUT

The AD7142 has an interrupt output that triggers an interrupt service routine on the host processor. The $\overline{INT}$ signal is on Pin 25, and is an open-drain output. There are three types of interrupt events on the AD7142: a CDC conversion complete interrupt, a sensor threshold interrupt, and a GPIO interrupt. Each interrupt has enable and status registers. The conversion complete and sensor threshold interrupts can be enabled on a per conversion stage basis. The status registers indicate what type of interrupt triggered the $\overline{INT}$ pin. Status registers are cleared, and the $\overline{INT}$ signal is reset high, during a read operation. The signal returns high as soon as the read address has been set up.

CDC CONVERSION COMPLETE INTERRUPT

The AD7142 interrupt signal asserts low to indicate the completion of a conversion stage, and new conversion result data is available in the registers.

The interrupt can be independently enabled for each conversion stage. Each conversion stage complete interrupt can be enabled via the CDC Conversion Completion register (Address 0x007). This register has a bit that corresponds to each conversion stage. Setting this bit to 1 enables the interrupt for that stage. Clearing this bit to 0 disables the conversion complete interrupt for that stage.

In normal operation, the AD7142 is set up to interrupt enable the last stage only in a conversion sequence. For example, if there are five conversion stages, the conversion complete interrupt for STAGE4 is enabled. $\overline{INT}$ only asserts when all five conversion stages are complete, and the host can read new data from all five result registers. The interrupt is cleared by reading the status register.

Register 0x00A is the conversion completion status register. Each bit in this register corresponds to a conversion stage. If a bit is set, it means that the conversion complete interrupt for the corresponding stage was triggered. This register is cleared on a read, provided the underlying condition that triggered the interrupt has gone away. (For a detailed register description, see Table 24.)

SENSOR THRESHOLD INTERRUPT

The AD7142 interrupt signal asserts low to indicate that a conversion result exceeds either the high or low threshold limits for that sensor. When a conversion result from a sensor exceeds the threshold limits, it indicates the sensor has been touched.

The sensor threshold interrupt can be enabled independently for each conversion stage via the interrupt configuration registers. Register 0x05 is the low threshold interrupt enable register. Each bit in the register corresponds to the threshold low interrupt for conversion STAGE0 to STAGE11. Register 0x006 is the high threshold enable register. Each bit in this register, corresponds to the high threshold interrupt enable for conversion STAGE0 to STAGE11. Setting a bit to 1 enables the interrupt for that stage. Clearing a bit to 0 disables the interrupt for that stage.

When a conversion result exceeds a low threshold, the status bit corresponding to that conversion stage is set in the CDC low limit status register at Address 0x008. (For a detailed register description, see Table 22.) If a conversion stage result exceeds a high limit, the status bit corresponding to that stage is set in the CDC high limit status register at Address 0x009. (For a detailed register description, see Table 23.) All bits in the status registers are cleared on read back, if all conversion results are within the threshold limits.

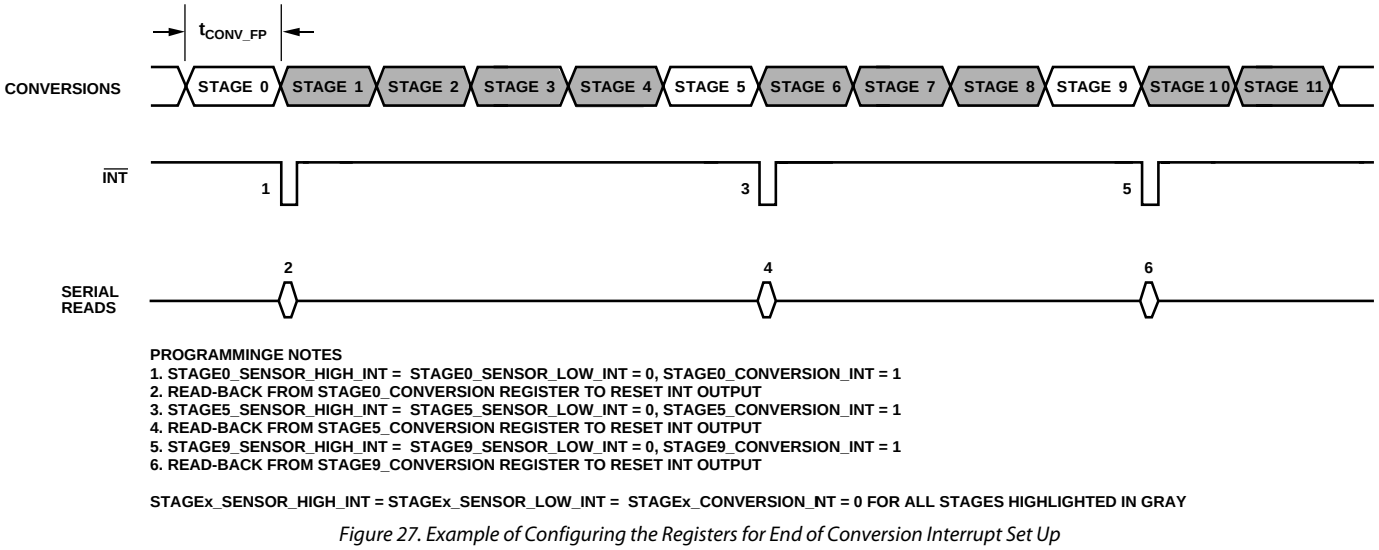


Figure 27. Example of Configuring the Registers for End of Conversion Interrupt Set Up

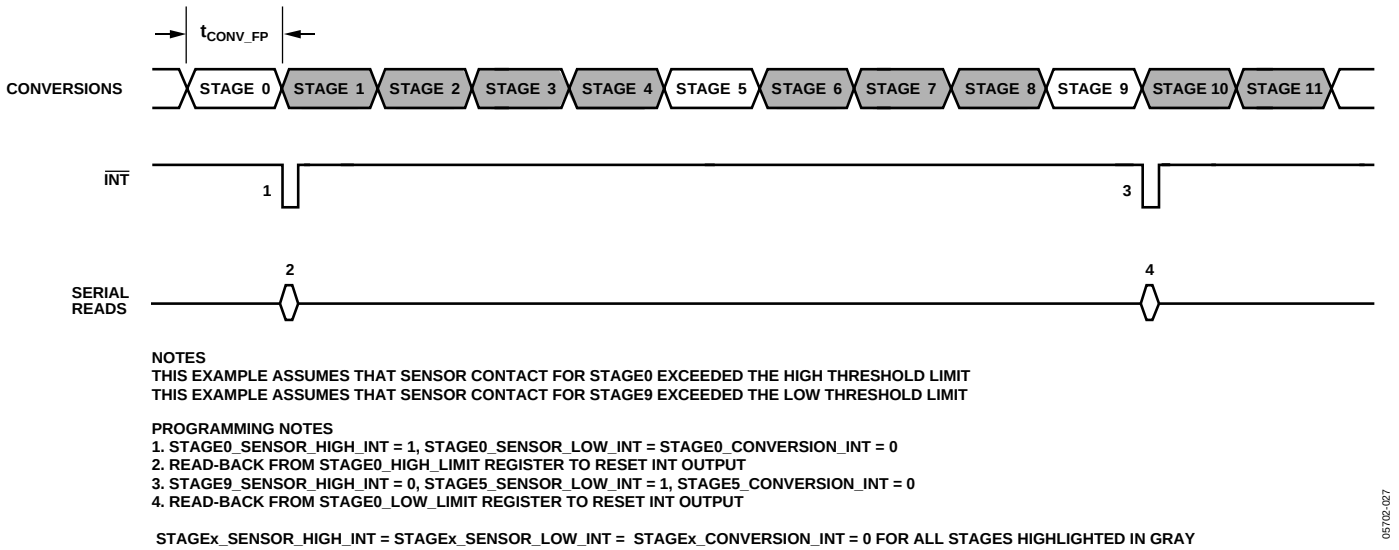


Figure 28. Example of Configuring the Registers for Sensor Interrupt Set Up

Table 11. GPIO Interrupt Behavior

GPIO_INPUT_CONFIG	GPIO Pin	GPIO_STATUS	$\overline{\text{INT}}$	$\overline{\text{INT}}$ Behavior
00 = negative level triggered	1	0	1	Not triggered
00 = negative level triggered	0	1	0	Asserted while signal on GPIO pin is low
01 = positive edge triggered	1	1	0	Pulses low at low to high GPIO transition
01 = positive edge triggered	0	0	1	Not triggered
10 = negative edge triggered	1	0	1	Pulses low at high to low GPIO transition
10 = negative edge triggered	0	1	0	Not triggered
11 = positive level triggered	1	1	0	Asserted while signal on GPIO pin is high
11 = positive level triggered	0	0	1	Not triggered

GPIO $\overline{\text{INT}}$ OUTPUT CONTROL

The $\overline{\text{INT}}$ output signal can be controlled by the GPIO pin when the GPIO is configured as an input. The GPIO is configured as an input by setting the GPIO_SETUP bits in the interrupt configuration register to 01. See GPIO section for more information on how to configure the GPIO.

Enable the GPIO interrupt by setting the GPIO_INT_EN bit in Register 0x007 to 1, or disable by clearing this bit to 0. The GPIO status bit in the CDC conversion completion register reflects the status of the GPIO interrupt. This bit is set to 1 when the GPIO has triggered $\overline{\text{INT}}$. The bit is cleared on read back from the register, provided the condition that caused the interrupt has gone away.

The GPIO interrupt can be set to trigger on a rising edge, falling edge, high level, or low level at the GPIO input pin. Table 11 shows how the settings of the GPIO_INPUT_CONFIG bits in the interrupt configuration register affect the behavior of $\overline{\text{INT}}$.

Figure 29 to Figure 32 show how the interrupt output is cleared on a read from the CDC conversion completion register.

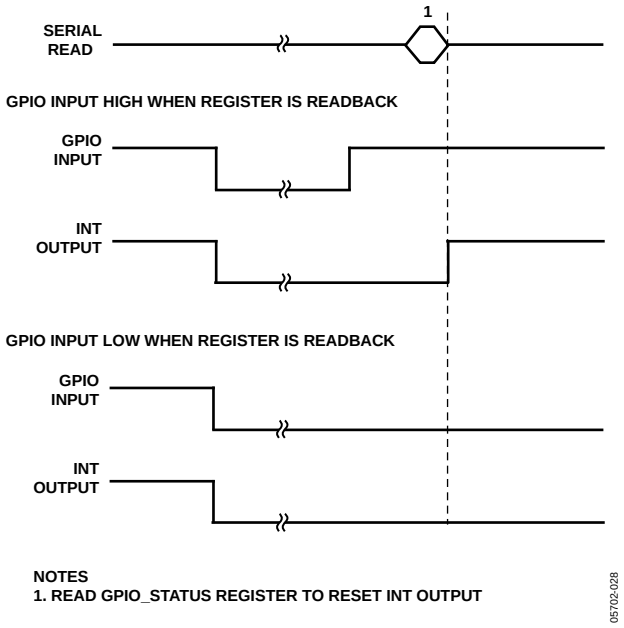


Figure 29. $\overline{INT}$ Output Controlled by the GPIO Input Example, GPIO_SETUP = 01, GPIO_INPUT_CONFIG = 00

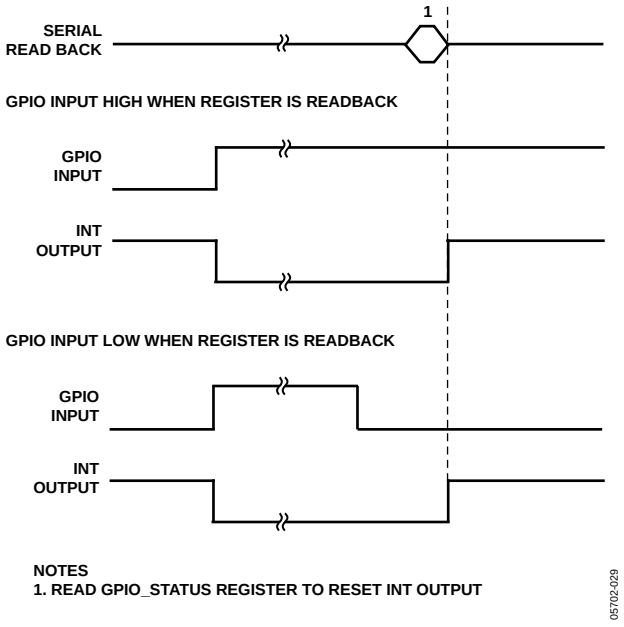


Figure 30. $\overline{INT}$ Output Controlled by the GPIO Input Example, GPIO_SETUP = 01, GPIO_INPUT_CONFIG = 01

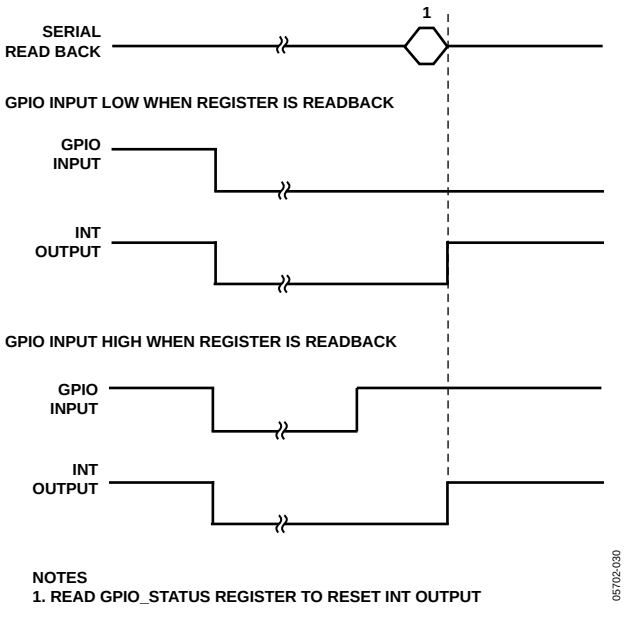


Figure 31. $\overline{INT}$ Output Controlled by the GPIO Input Example, GPIO_SETUP = 01, GPIO_INPUT_CONFIG = 10

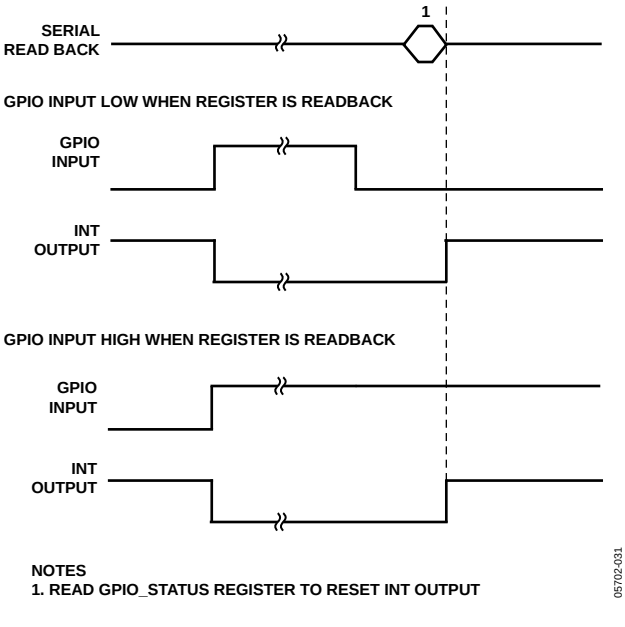


Figure 32. $\overline{INT}$ Output Controlled by the GPIO Input Example, GPIO_SETUP = 01, GPIO_INPUT_CONFIG = 11

OUTPUTS

EXCITATION SOURCE

The excitation source on board the AD7142 is as square wave source with a frequency of 240 kHz. This excitation source forms the capacitance field between the transmitter and receiver in the external capacitance sensor PCB. The source is output from the AD7142 on two pins, the SRC pin and the $\overline{SRC}$ pin (outputs an inverted version of the source square wave). The $\overline{SRC}$ signal offsets large external sensor capacitances. In current applications, $\overline{SRC}$ is not used.

The source output can be disabled from both output pins separately by writing to the control register (Address 0x000). Setting Bit 12 in this register to 1 disables the source output on the SRC pin. Setting Bit 13 in this register to 1 disables the inverted source output on the $\overline{SRC}$ pin.

C_{SHIELD} OUTPUT

To prevent leakage from the external capacitance sensors, the sensor traces are shielded. The AD7142 has a voltage output that can be used as the potential for any shield traces, C_{SHIELD}. The C_{SHIELD} voltage is equal to $V_{DD}/2$.

The C_{SHIELD} potential is derived from the output of the AD7142 internal amplifier, and is of equal potential to the CIN input lines. Because the shield is at the same potential as the sensor traces, no leakage to ground occurs.

To eliminate any ringing on the C_{SHIELD} output, connect a 10 nF capacitor between the C_{SHIELD} pin and ground.

C_{SHIELD} is connected to layer three on a four-layer sensor PCB to provide shielding for the sensors. On a two-layer PCB construction, C_{SHIELD} is used in place of a ground plane around the sensors, on both layers of the PCB.

Figure 33 shows how the sensor traces are shielded by running traces connected to the shield potential around the sensor traces.

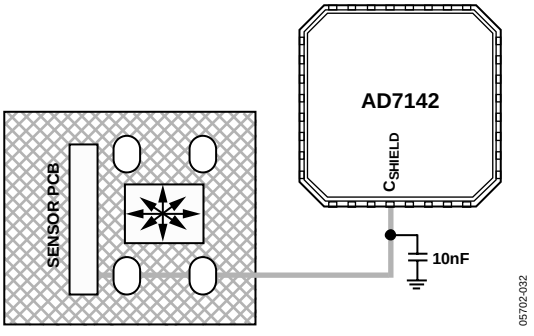


Figure 33. Shielding the Sensor Traces

GPIO

The AD7142 has one GPIO pin, Pin 26. It can be configured as an input or an output. The GPIO_SETUP bits in the interrupt configuration register determine how the GPIO pin is configured.

Table 12. GPIO_SETUP Bits

GPIO_SETUP	GPIO Configuration
00	GPIO disabled
01	Input
10	Output low
11	Output high

When the GPIO is configured as an output, the voltage level on the pin is set to either a low level or a high level, as defined by the GPIO_SETUP bits, shown in Table 12.

When the GPIO is configured as an input, the GPIO_INPUT_CONFIGURATON bits in the interrupt configuration register determine the response of the AD7142 to a signal on the GPIO pin. The GPIO can be configured as either active high or active low, as well as either edge triggered or level triggered, as listed in Table 13.

Table 13. GPIO_INPUT_CONFIGURATION Bits

GPIO_INPUT_CONFIGURATION	GPIO Configuration
00	Triggered on negative level (active low)
01	Triggered on positive edge (active high)
10	Triggered on negative edge (active low)
11	Triggered on positive level (active high)

When GPIO is configured as an input, it triggers the interrupt output on the AD7142. Table 11 lists the interrupt output behavior for each of the GPIO configuration setups.

SERIAL INTERFACE

The AD7142 is available with an SPI serial interface. The AD7142-1 is available with an I²C interface. Both parts are exactly the same, with the exception of the serial interface.

SPI INTERFACE

The AD7142 has a 4-wire serial peripheral interface (SPI). The SPI has a data input pin (SDI) for inputting data to the device, a data output pin (SDO) for reading data back from the device, and a data clock pin (SCLK) for clocking data into and out of the device. A chip select pin ($\overline{CS}$) enables or disables the serial interface. $\overline{CS}$ is required for correct operation of the SPI interface. Data is clocked out of the AD7142 on the negative edge of SCLK, and data is clocked into the device on the positive edge of SCLK.

SPI Command Word

All data transactions on the SPI bus begin with the master taking $\overline{CS}$ low and sending out the command word. This indicates to the AD7142 whether the transaction is a read or a write, and gives the address of the register from which to begin the data transfer.

Table 14. SPI Command Word

15					10	9	0
1	1	1	0	0	R/$\overline{W}$	Register Address	

Bits[15:11] of the command word must be set to 11100 to successfully begin a bus transaction.

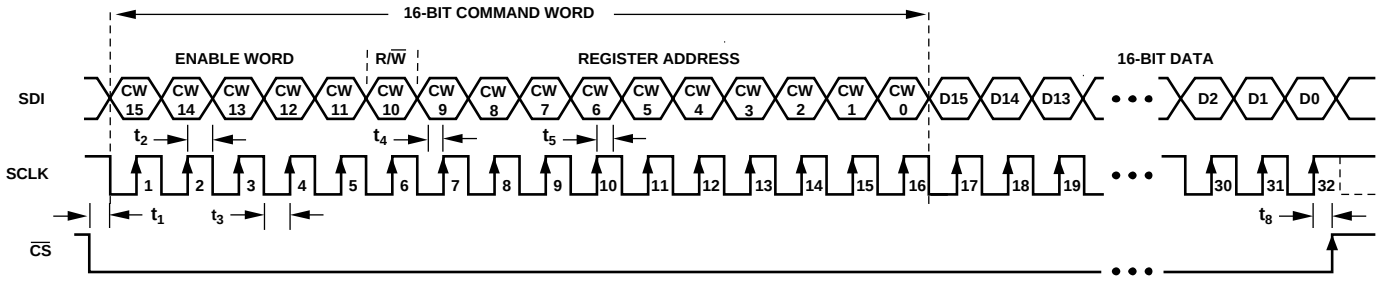
Bit 10 is the read/write bit; 1 indicates a read, and 0 indicates a write.

Bits[9:0] contain the target register address. When reading or writing to more than one register, this address indicates the address of the first register to be written to or read from.

Writing Data

Data is written to the AD7142 in 16-bit words. The first word written to the device is the command word, with the read/write bit set to 0. The master then supplies the 16-bit input data-word on the SDI line. The AD7142 clocks the data into the register addressed in the command word. If there is more than one word of data to be clocked in, the AD7142 automatically increments the address pointer, and clock the next data-word into the next register.

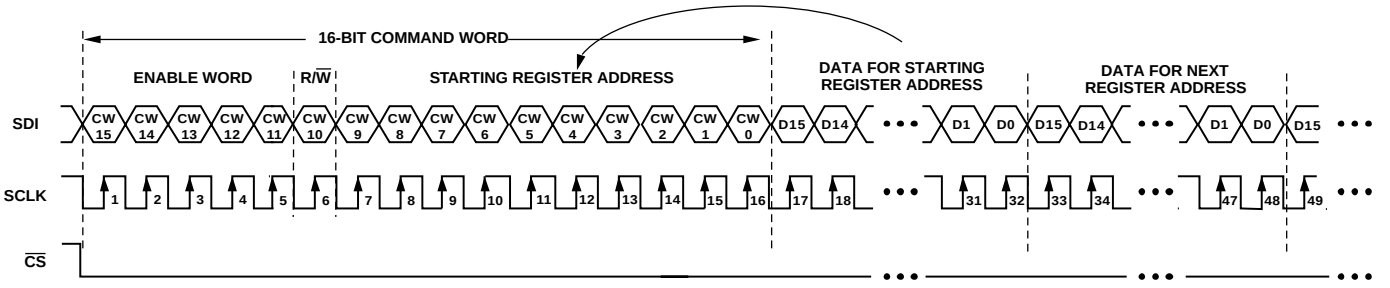
The AD7142 continues to clock in data on the SDI line until either the master finishes the write transition by pulling $\overline{CS}$ high, or until the address pointer reaches its maximum value. The AD7142 address pointer does not wrap around. When it reaches its maximum value, any data provided by the master on the SDI line is ignored by the AD7142.



NOTES
1. SDI BITS ARE LATCHED ON SCLK RISING EDGES. SCLK MAY IDLE HIGH OR LOW BETWEEN WRITE OPERATIONS.
2. ALL 32 BITS MUST BE WRITTEN: 16 BITS FOR CONTROL WORD AND 16 BITS FOR DATA.
3. 16-BIT COMMAND WORD SETTINGS FOR SERIAL WRITE OPERATION:
   CW[15:11] = 11100 (ENABLE WORD)
   CW[10] = 0 (R/$\overline{W}$)
   CW[9:0] = [AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0] (10-BIT MSB JUSTIFIED REGISTER ADDRESS)

05702-033

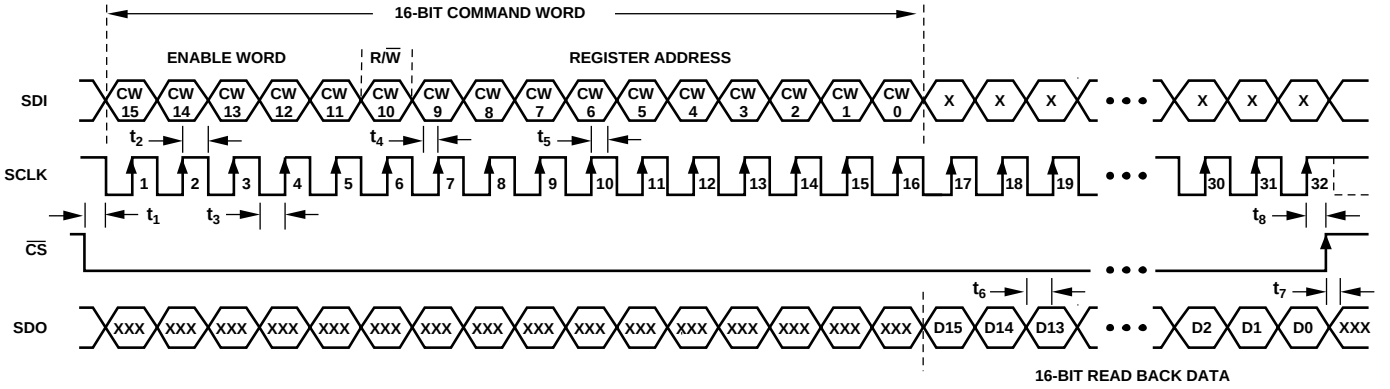
Figure 34. Single Register Write SPI Timing



NOTES
1. MULTIPLE SEQUENTIAL REGISTERS MAY BE LOADED CONTINUOUSLY.
2. THE FIRST (LOWEST ADDRESS) REGISTER ADDRESS IS WRITTEN, FOLLOWED BY MULTIPLE 16-BIT DATA-WORDS.
3. THE ADDRESS WILL AUTOMATICALLY INCREMENT WITH EACH 16-BIT DATA-WORD (ALL 16 BITS MUST BE WRITTEN).
4. CS IS HELD LOW UNTIL THE LAST DESIRED REGISTER HAS BEEN LOADED.
5. 16-BIT COMMAND WORD SETTINGS FOR SEQUENTIAL WRITE OPERATION:
   CW[15:11] = 11100 (ENABLE WORD)
   CW[10] = 0 (R/W)
   CW[9:0] = [AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0] (STARTING MSB JUSTIFIED REGISTER ADDRESS)

05702-034

Figure 35. Sequential Register Write SPI Timing



NOTES
1. SDI BITS ARE LATCHED ON SCLK RISING EDGES. SCLK MAY IDLE HIGH OR LOW BETWEEN WRITE OPERATIONS.
2. THE 16-BIT CONTROL WORD MUST BE WRITTEN ON SDI: 5-BITS FOR ENABLE WORD, 1 BIT FOR R/W AND 10-BITS FOR REGISTER ADDRESS.
3. THE REGISTER DATA WILL BE READ BACK ON THE SDO PIN.
4. X DENOTES DON'T CARE.
5. XXX DENOTES HIGH IMPEDANCE TRISTATE OUTPUT.
6. CS IS HELD LOW UNTIL ALL REGISTER BITS HAVE BEEN READ BACK.
7. 16-BIT COMMAND WORD SETTINGS FOR SINGLE READ-BACK OPERATION:
   CW[15:11] = 11100 (ENABLE WORD)
   CW[10] = 1 (R/W)
   CW[9:0] = AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0 (10-BIT MSB JUSTIFIED REGISTER ADDRESS)

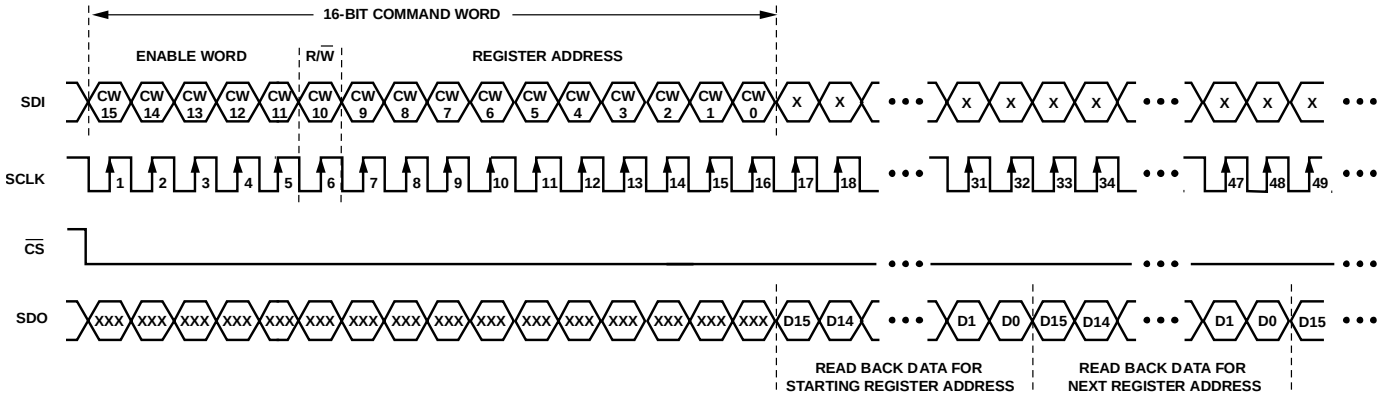
05702-035

Figure 36. Single Register Readback SPI Timing

Reading Data

A read transaction begins when the master writes the command word to the AD7142 with the read/write bit set to 1. The master then supplies 16 clock pulses per data-word to be read, and the AD7142 clocks out data from the addressed register on the SDO line. The first data-word is clocked out on the first falling edge of CS following the command word, as shown in Figure 36.

The AD7142 continues to clock out data on the SDO line provided the master continues to supply the clock signal on SCLK. The read transaction finishes when the master takes CS high. If the AD7142 address pointer reaches its maximum value, then the AD7142 repeatedly clocks out data from the addressed register. The address pointer does not wrap around.



NOTES
1. MULTIPLE REGISTERS MAY BE READ BACK CONTINUOUSLY.
2. THE 16-BIT CONTROL WORD MUST BE WRITTEN ON SDI: 5-BITS FOR ENABLE WORD, 1 BIT FOR R/W AND 10-BITS FOR REGISTER ADDRESS.
3. THE ADDRESS WILL AUTOMATICALLY INCREMENT WITH EACH 16-BIT DATA-WORD BEING READ BACK ON THE SDO PIN.
4. CS IS HELD LOW UNTIL ALL REGISTER BITS HAVE BEEN READ BACK.
5. X DENOTES DON'T CARE.
6. XXX DENOTES HIGH IMPEDANCE TRISTATE OUTPUT.
7. 16-BIT COMMAND WORD SETTINGS FOR SEQUENTIAL READ-BACK OPERATION:
   CW[15:11] = 11100 (ENABLE WORD)
   CW[10] = 1 (R/W)
   CW[9:0] = AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0 (STARTING MSB JUSTIFIED REGISTER ADDRESS)

05702-036

Figure 37. Sequential Register Readback SPI Timing

I²C INTERFACE

The AD7142-1 supports the JEDEC industry standard 2-wire I²C serial interface protocol. The two wires associated with the I²C timing are the SCLK and the SDA inputs. The SDA is an I/O pin that allows both register write and register readback operations. The AD7142-1 is always a slave device on the I²C serial interface bus.

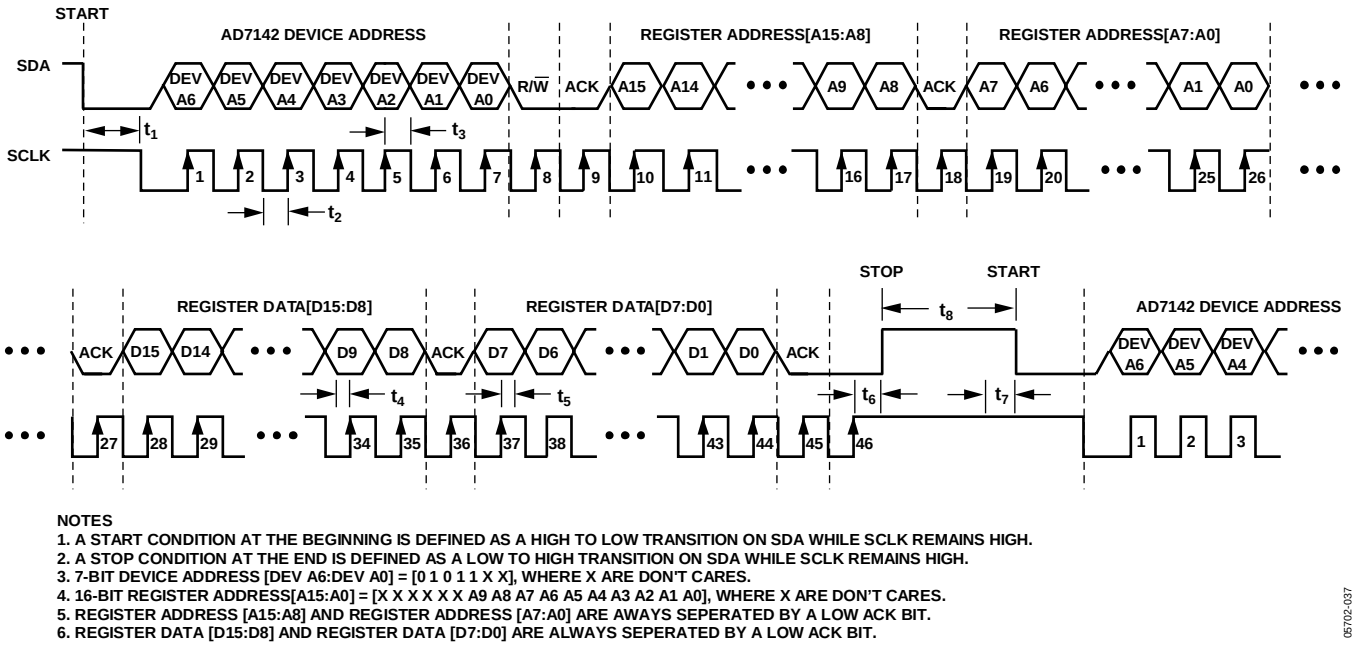
It has a 7-bit device address, Address 0101 1XX. The lower two bits are set by tying the Add0 and Add1 pins high or low. The AD7142-1 responds when the master device sends its device address over the bus. The AD7142-1 cannot initiate data transfers on the bus.

Table 15.AD7142-1 I²C Device Address

ADD1	ADD0	I²C Address
0	0	0101 100
0	1	0101 101
1	0	0101 110
1	1	0101 111

Data Transfer

1. Data is transferred over the I²C serial interface in 8-bit bytes. The master initiates a data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line, SDA, while the serial clock line, SCLK, remains high. This indicates that an address/data stream follows.
2. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/$\overline{W}$ bit that determines the direction of the data transfer. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as the acknowledge bit. All other devices on the bus now remain idle while the selected device waits for data to be read from, or written to it. If the R/$\overline{W}$ bit is a zero, the master writes to the slave device. If the R/$\overline{W}$ bit is a one, the master reads from the slave device.
3. Data is sent over the serial bus in a sequence of nine clock pulses, eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, since a low-to-high transition when the clock is high can be interpreted as a stop signal. The number of data bytes transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.
4. When all data bytes are read or written, a stop condition is established. A stop condition is defined by a low-to-high transition on SDA while SCLK remains high. If the AD7142 encounters a stop condition, it returns to its idle condition, and the address pointer resets to Address 0x00.



NOTES
1. A START CONDITION AT THE BEGINNING IS DEFINED AS A HIGH TO LOW TRANSITION ON SDA WHILE SCLK REMAINS HIGH.
2. A STOP CONDITION AT THE END IS DEFINED AS A LOW TO HIGH TRANSITION ON SDA WHILE SCLK REMAINS HIGH.
3. 7-BIT DEVICE ADDRESS [DEV A6:DEV A0] = [0 1 0 1 1 X X], WHERE X ARE DON'T CARES.
4. 16-BIT REGISTER ADDRESS[A15:A0] = [X X X X X X A9 A8 A7 A6 A5 A4 A3 A2 A1 A0], WHERE X ARE DON'T CARES.
5. REGISTER ADDRESS [A15:A8] AND REGISTER ADDRESS [A7:A0] ARE AWAYS SEPERATED BY A LOW ACK BIT.
6. REGISTER DATA [D15:D8] AND REGISTER DATA [D7:D0] ARE ALWAYS SEPERATED BY A LOW ACK BIT.

05702-037

Figure 38. Example of I²C Timing for Single Register Write Operation

Writing Data over the I²C Bus

The process for writing to the AD7142-1 over the I²C bus is shown in Figure 38 and Figure 40. The device address is sent over the bus followed by the R/$\overline{W}$ bit set to 0. This is followed by two bytes of data that contain the 10-bit address of the internal data register to be written. The upper and lower register address bytes are shown in Table 16. Note that Bit 7 to Bit 2 in the upper address byte are don't cares. The address is contained in the 10 LSBs of the register address bytes.

Table 16. AD7142-1 Internal Register I²C Addressing: Register Address Upper Byte

7	6	5	4	3	2	1	0
X	X	X	X	X	X	Register Address Bit 9	Register Address Bit 8

Table 17. AD7142-1 Internal Register I²C Addressing: Register Address Lower Byte

7	6	5	4	3	2	1	0
Reg Add Bit 7	Reg Add Bit 6	Reg Add Bit 5	Reg Add Bit 4	Reg Add Bit 3	Reg Add Bit 2	Reg Add Bit 1	Reg Add Bit 0

The third data byte contains the eight MSBs of the data to be written to the internal register. The fourth byte of data contains the eight LSBs of data to be written to the internal register.

The AD7142-1 address pointer register automatically increments after each write. This allows the master to sequentially write to all registers on the AD7142-1 in the same write transaction. However, the address pointer does not wrap around after the last address. Any data written to the AD7142-1 after the address pointer has reached its maximum value is discarded.

All registers on the AD7142-1 are 16-bit. Two consecutive 8-bit data bytes are combined and written to the 16-bit registers. To avoid errors, all writes to the device must contain an even number of data bytes.

To finish the transaction, the master generates a stop condition on SDO, or generates a repeat start condition if the master is to maintain control of the bus.

Reading Data over the I²C Bus

To read from the AD7142-1, the address pointer must first be set to the address of the required internal register. The master performs a write transaction, and writes to the AD7142-1 to set the address pointer. The master then outputs a repeat start condition to keep control of the bus, or if this is not possible, ends the write transaction with a stop condition. A read transaction is initiated, with the R/$\overline{W}$ bit set to 1.

The AD7142-1 supplies the upper eight bits of data from the addressed register in the first readback byte, followed by the lower eight bits in the next byte. This is shown in Figure 39 and Figure 40.

Because the address pointer automatically increases after each read, the AD7142-1 continues to output readback data until the master puts a no acknowledge and stop condition on the bus. If the address pointer reaches its maximum value, and the master continues to read from the part, the AD7142-1 repeatedly sends data from the last register addressed.

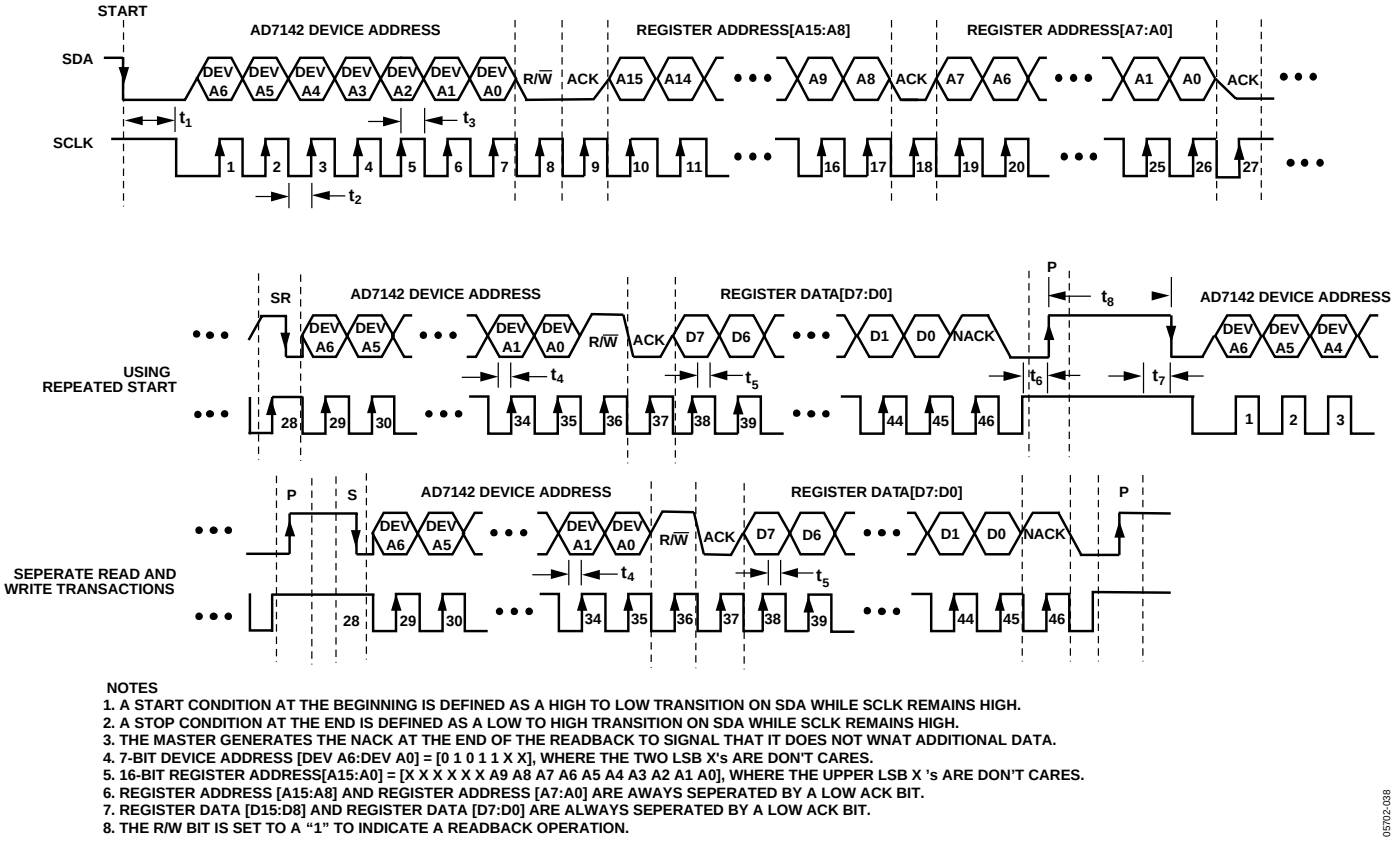


Figure 39. Example of I²C Timing for Single Register Readback Operation

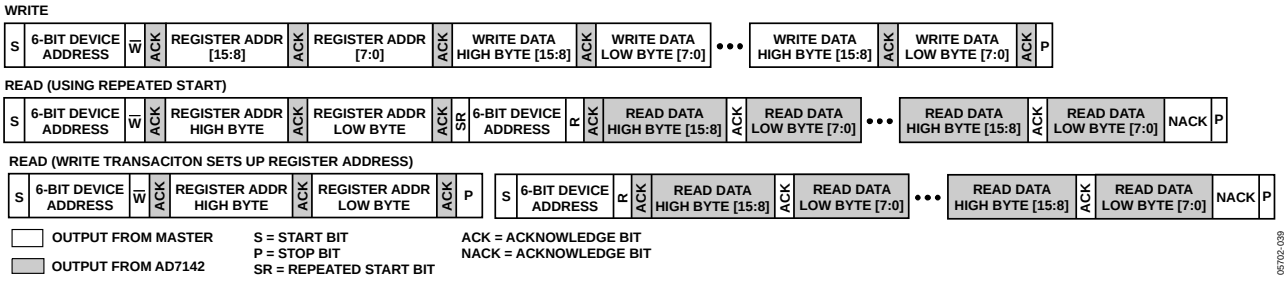


Figure 40. Example of Sequential I²C Write and Readback Operation

V_{DRIVE} INPUT

The supply voltage to all pins associated with both the I²C and SPI serial interfaces (SDO, SDI, SCLK, SDA, and $\overline{CS}$) is separate from the main V_{CC} supply and is connected to the V_{DRIVE} pin.

This allows the AD7142 to be connected directly to processors whose supply voltage is less than the minimum operating voltage of the AD7142 without the need for external level-shifters. The V_{DRIVE} pin can be connected to voltage supplies as low as 1.6 V and as high as V_{CC}.

PCB DESIGN GUIDELINES

CAPACITIVE SENSOR BOARD MECHANICAL SPECIFICATIONS

Table 18.

Parameter	Symbol	Min	Typ	Max	Unit
Distance from Edge of Any Sensor to Edge of Metal Object	D_1	1.0			mm
Distance Between Sensor Edges[1]	$D_2 = D_3 = D_4$	0			mm
Distance Between Bottom of Sensor Board and Controller Board or Metal Casing[2] (4-Layer, 2-Layer And Flex Circuit)	D_5		1.0		mm

[1] The distance is dependent on the application and the positioning of the switches relative to each other and with respect to the user's finger positioning and handling. Adjacent sensors, with 0 minimum space between them, are implemented differentially.

[2] The 1.0 mm specification is meant to prevent any direct sensor board contact with any conductive material. This specification does not guarantee no EMI coupling from the controller board to the sensors. Address potential EMI coupling issues by placing a grounded metal shield between the capacitive sensor board and the main controller board as shown in Figure 43.

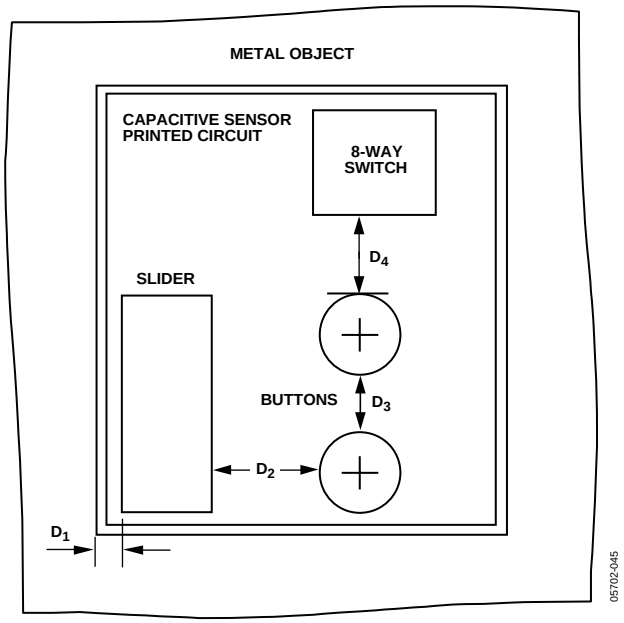


Figure 41. Capacitive Sensor Board Mechanicals Top View

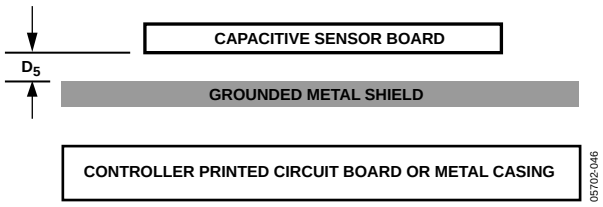


Figure 42. Capacitive Sensor Board Mechanicals Side View

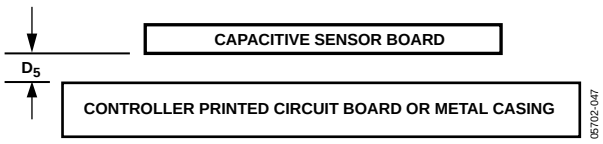


Figure 43. Capacitive Sensor Board with Grounded Shield

CHIP SCALE PACKAGES

The lands on the chip scale package (CP-32-3) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length, and 0.05 mm wider than the package land width. Center the land on the pad to maximize the solder joint size.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. To avoid shorting, provide a clearance of at least 0.25 mm between the thermal pad and the inner edges of the land pattern on the printed circuit board.

Thermal vias can be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at a 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. copper to plug the via.

Connect the printed circuit board thermal pad to GND.

POWER-UP SEQUENCE

When the AD7142 is powered up, the following sequence is recommended:

1. Turn on the power supplies to the AD7142.
2. Load all of the required Bank 2 configuration registers.
3. Load Bank 1 registers at Address 0x000 through Address 0x004 (except Register Address 0x001 Bits[11:0]) and Register Address 0x045 to configure the AD7142.
4. Load Bank 1 registers at Address 0x005 through Address 0x007. This enables the interrupt operation.
5. Set calibration enable bits for each conversion stage, Register Address 0x001 Bits[11:0]. Wait for three interrupt cycles. After the third interrupt, valid data is available in the AD7142 registers.
6. Read back either the CDC conversion limit or CDC conversion completion registers to reset the $\overline{\text{INT}}$ output as explained in the Interrupt Output section.
7. Repeat Step 5 every time $\overline{\text{INT}}$ is asserted.

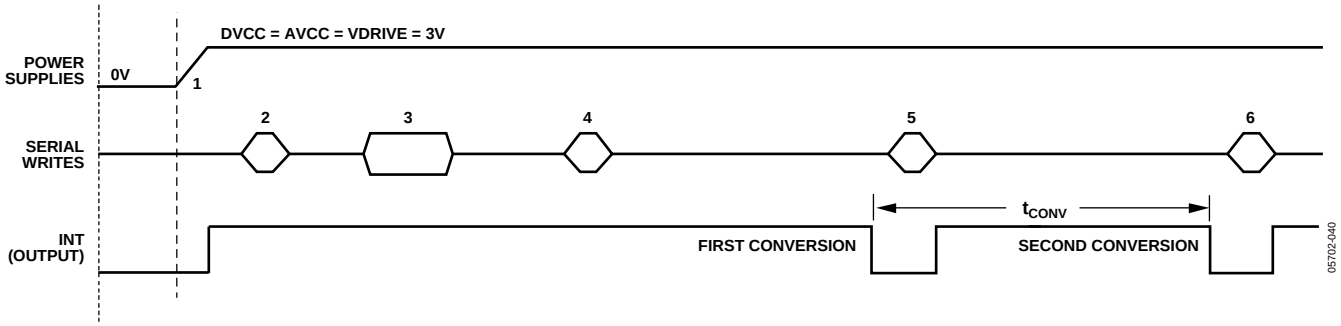


Figure 44. Recommended Start-Up Sequence

TYPICAL APPLICATION CIRCUITS

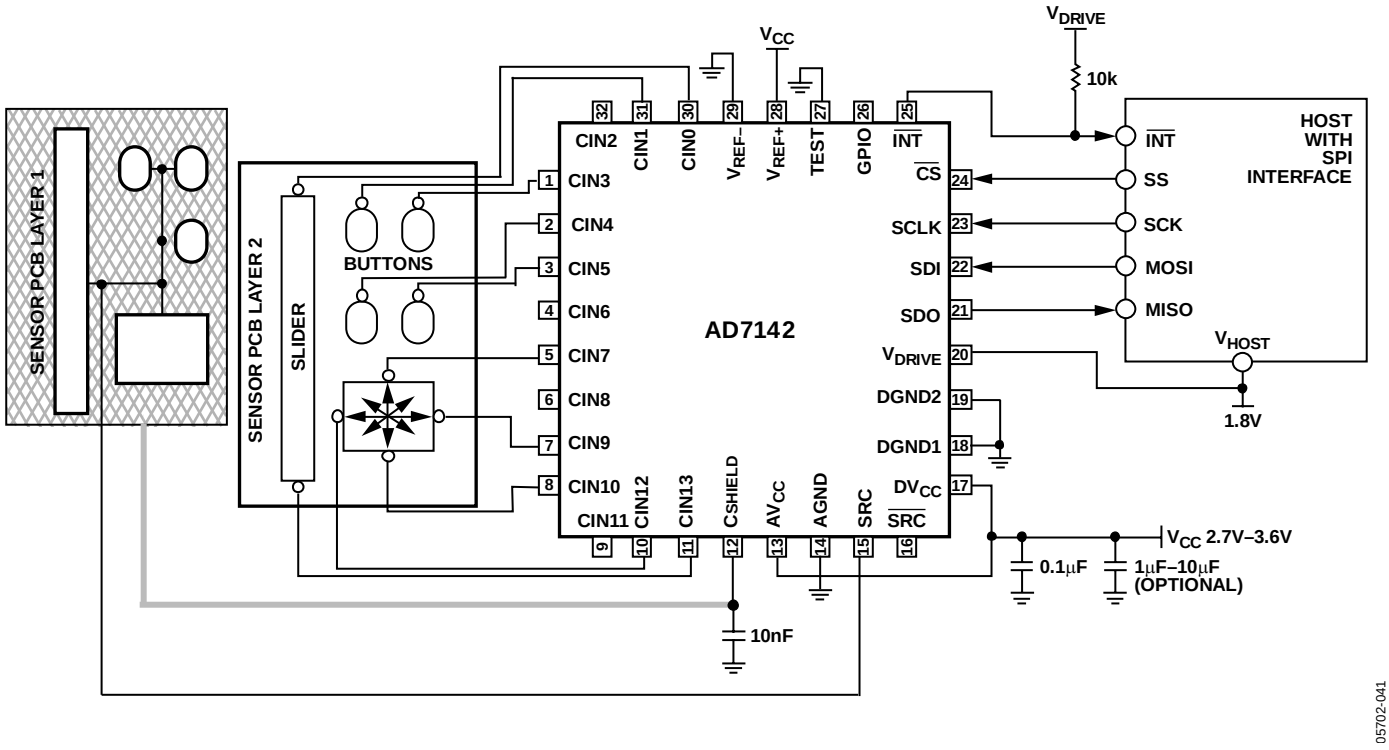


Figure 45. Typical Application Circuit with SPI Interface

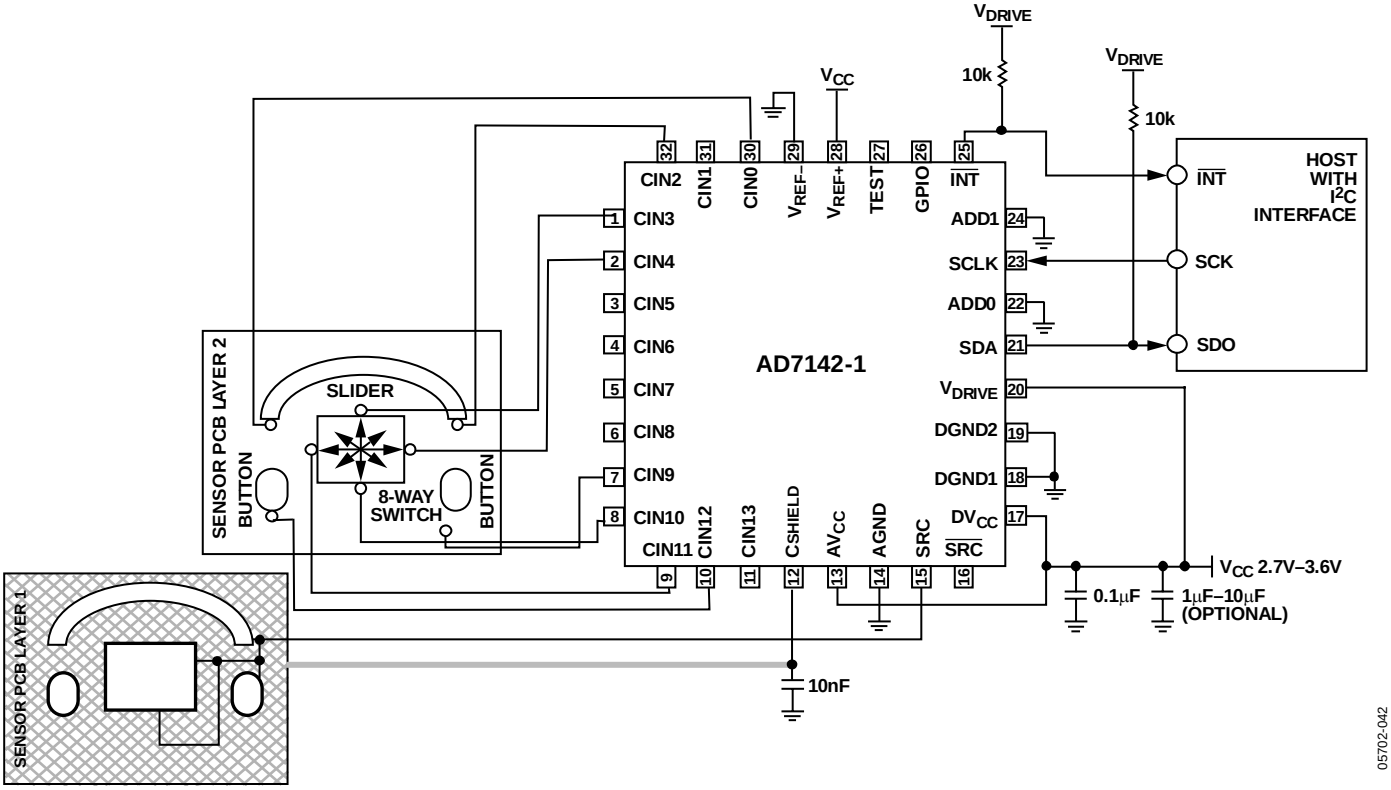


Figure 46. Typical Application Circuit with I²C Interface

REGISTER MAP

The AD7142 address space is divided into three different register banks, referred to as Register Bank 1, Register Bank 2, and Register Bank 3. Figure 47 illustrates the division of these three banks.

Register Bank 1 contains setup and conversion control registers, interrupt configuration registers, and CDC conversion limit and completion registers. Register Bank 1 also contains the 16-bit ADC raw data for all 12 conversion stages and the AD7142 device ID register.

Register Bank 2 contains the conversion stage configuration registers used for uniquely configuring the CIN inputs for each conversion stage. Initialize the Bank 2 configuration registers immediately after power-up to obtain valid CDC conversion result data.

Register Bank 3 contains the results of each conversion stage. These registers automatically update at the end of each conversion sequence. Although these registers are primarily used by the AD7142 internal data processing, they are accessible by the host processor for additional external data processing, if desired.

Default values are undefined for Register Bank 2 and Register Bank 3 until after power up and configuration of Register Bank 2.

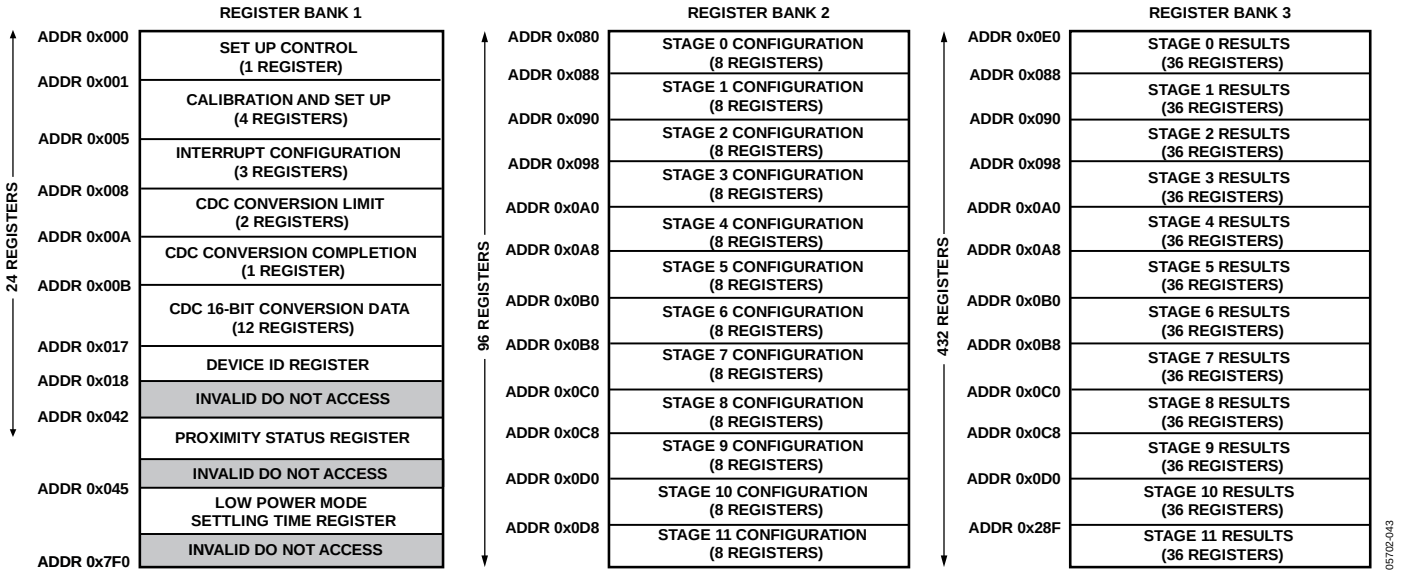


Figure 47. Layout of Bank 1, Bank 2, and Bank 3 Registers

DETAILED REGISTER DESCRIPTIONS

BANK 1 REGISTERS

All addresses and default values are expressed in hexadecimal.

Table 19. Control Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
000	[1:0]	0	R/W	POWER_MODE	Operating Modes 00 = full power mode (Normal operation, CDC conversions approximately every 36 ms) 01 = full shutdown mode (No CDC conversions) 10 = low power mode (Automatic wake up operation) 11 = Full Shutdown Mode (No CDC conversions)
	[3:2]	0		LP_CONV_DELAY	Low Power Mode Conversion Delay 00 = 100 ms 01 = 200 ms 10 = 300 ms 11 = 400 ms
	[7:4]	0		SEQUENCE_STAGE_NUM	Number of Stages in Sequence (N + 1) 0000 = 1 conversion stage in sequence 0001 = 2 conversion stages in sequence …… Maximum value = 1011 = 12 conversion stages per sequence
	[9:8]	0		DECIMATION	ADC Decimation Factor 00 = decimate by 256 01 = decimate by 128 10 = decimate by 64 11 = decimate by 64
	[10]	0		SW_RESET	Software Reset Control (Self-Clearing) 1 = resets all registers to default values
	[11]	0		INT_POL	Interrupt Polarity Control 0 = active low 1 = active high
	[12]	0		EXCITATION_SOURCE	Excitation Source Control for Pin 15 0 = enable output 1 = disable output
	[13]	0		$\overline{\text{SRC}}$	Excitation Source Control for Pin 16 0 = enable output 1 = disable output
	[15:14]	0		CDC_BIAS	CDC Bias Current Control 00 = normal operation 01 = normal operation + 20% 10 = normal operation + 35% 11 = normal operation + 50%

Table 20. CDC Conversion Control Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
001	[0]	0	R/W	STAGE0_CAL_EN	STAGE0 Calibration Enable 0 = disable 1 = enable
	[1]	0		STAGE1_CAL_EN	STAGE1 Calibration Enable 0 = disable 1 = enable
	[2]	0		STAGE2_CAL_EN	STAGE2 Calibration Enable 0 = disable 1 = enable
	[3]	0		STAGE3_CAL_EN	STAGE3 Calibration Enable 0 = disable 1 = enable
	[4]	0		STAGE4_CAL_EN	STAGE4 Calibration Enable 0 = disable 1 = enable
	[5]	0		STAGE5_CAL_EN	STAGE5 Calibration Enable 0 = disable 1 = enable
	[6]	0		STAGE6_CAL_EN	STAGE6 Calibration Enable 0 = disable 1 = enable
	[7]	0		STAGE7_CAL_EN	STAGE7 Calibration Enable 0 = disable 1 = enable
	[8]	0		STAGE8_CAL_EN	STAGE8 Calibration Enable 0 = disable 1 = enable
	[9]	0		STAGE9_CAL_EN	STAGE9 Calibration Enable 0 = disable 1 = enable
	[10]	0		STAGE10_CAL_EN	STAGE10 Calibration Enable 0 = disable 1 = enable
	[11]	0		STAGE11_CAL_EN	STAGE11 Calibration Enable 0 = disable 1 = enable
	[13:12]	0		AVG_FP_SKIP	Full Power Mode Skip Control 00 = skip 3 samples 01 = skip 7 samples 10 = skip 15 samples 11 = skip 31 samples
	[15:14]	0		AVG_LP_SKIP	Low Power Mode Skip Control 00 = use all samples 01 = skip 1 sample 10 = skip 2 samples 11 = skip 3 samples

Address	Data Bit Content	Default Value	Type	Name	Description
002	[3:0]	0	R/W	FF_SKIP_CNT	Fast Filter Skip Control (N+1) 0000 = 1 conversion skipped in each stage 0001 = 2 conversions skipped in each stage …… 1011 = max value = 12 conversions skipped in each stage
	[7:4]	F		FP_PROXIMITY_CNT	Full Power Mode Proximity Period
	[11:8]	F		LP_PROXIMITY_CNT	Low Power Mode Proximity Period
	[13:12]	0		PWR_DOWN_TIMEOUT	Power Down Time Out Control 00 = 1.25 × (LP_PROXIMITY_CNT) 01 = 1.50 × (LP_PROXIMITY_CNT) 10 = 1.75 × (LP_PROXIMITY_CNT) 11 = 2.00 × (LP_PROXIMITY_CNT)
	[14]	0		FORCED_CAL	Forced Calibration Control 0 = normal operation 1 = forces all conversion stages to recalibrate
	[15]	0		CONV_RESET	Conversion Reset Control (Self-Clearing) 0 = normal operation 1 = resets the conversion sequence back to STAGE0.
003	[7:0]	64	R/W	PROXIMITY_RECAL_LVL	Proximity Recalibration Level
	[13:8]	1		PROXIMITY_DETECTION_RATE	Proximity Detection Rate
	[15:14]	0		SLOW_FILTER_UPDATE_LVL	Slow Filter Update Level
004	[9:0]	3FF	R/W	FP_PROXIMITY_RECAL	Full Power Mode Proximity Recalibration Time Control
	[15:10]	3F		LP_PROXIMITY_RECAL	Low Power Mode Proximity Recalibration Time Control

Table 21. Interrupt Configuration Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
005	[0]	0	R/W	STAGE0_LOW_INT_EN	STAGE0 Low Interrupt Enable 0 = interrupt source disabled 1 = $\overline{\text{INT}}$ asserted if STAGE0 low reference is exceeded
	[1]	0		STAGE1_LOW_INT_EN	STAGE1 Low Interrupt Enable 0 = interrupt source disabled 1 = $\overline{\text{INT}}$ asserted if STAGE0 low reference is exceeded
	[2]	0		STAGE2_LOW_INT_EN	STAGE2 Low Interrupt Enable 0 = interrupt source disabled 1 = $\overline{\text{INT}}$ asserted if STAGE0 low reference is exceeded
	[3]	0		STAGE3_LOW_INT_EN	STAGE3 Low Interrupt Enable 0 = interrupt source disabled 1 = $\overline{\text{INT}}$ asserted if STAGE0 low reference is exceeded
	[4]	0		STAGE4_LOW_INT_EN	STAGE4 Low Interrupt Enable 0 = interrupt source disabled 1 = $\overline{\text{INT}}$ asserted if STAGE0 low reference is exceeded
	[5]	0		STAGE5_LOW_INT_EN	STAGE5 Low Interrupt Enable 0 = interrupt source disabled 1 = $\overline{\text{INT}}$ asserted if STAGE0 low reference is exceeded
	[6]	0		STAGE6_LOW_INT_EN	STAGE6 Low Interrupt Enable 0 = interrupt source disabled 1 = $\overline{\text{INT}}$ asserted if STAGE0 low reference is exceeded

Address	Data Bit Content	Default Value	Type	Name	Description
	[7]	0		STAGE7_LOW_INT_EN	STAGE7 Low Interrupt Enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE0 low reference is exceeded
	[8]	0		STAGE8_LOW_INT_EN	STAGE8 Low Interrupt Enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE0 low reference is exceeded
	[9]	0		STAGE9_LOW_INT_EN	STAGE9 Low Interrupt Enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE0 low reference is exceeded
	[10]	0		STAGE10_LOW_INT_EN	STAGE10 Low Interrupt Enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE0 low reference is exceeded
	[11]	0		STAGE11_LOW_INT_EN	STAGE11 Low Interrupt Enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE0 low reference is exceeded
	[13:12]	0		GPIO_SETUP	GPIO Setup 00 = disable GPIO pin 01 = configure GPIO as an input 10 = configure GPIO as an active low output 11 = configure GPIO as an active high output
	[15:14]	0		GPIO_INPUT_CONFIG	GPIO Input Configuration 00 = triggered on negative level 01 = triggered on positive edge 10 = triggered on negative edge 11 = triggered on positive level
006	[0]	0	R/W	STAGE0_HIGH_INT_EN	STAGE0 High Interrupt Enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE0 high reference is exceeded
	[1]	0		STAGE1_HIGH_INT_EN	STAGE1 High Interrupt Enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE0 high reference is exceeded
	[2]	0		STAGE2_HIGH_INT_EN	STAGE2 High Interrupt Enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE0 high reference is exceeded
	[3]	0		STAGE3_HIGH_INT_EN	STAGE3 High Interrupt Enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE0 high reference is exceeded
	[4]	0		STAGE4_HIGH_INT_EN	STAGE4 High Interrupt Enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE0 high reference is exceeded
	[5]	0		STAGE5_HIGH_INT_EN	STAGE5 High Interrupt Enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE0 high reference is exceeded
	[6]	0		STAGE6_HIGH_INT_EN	STAGE6 High Interrupt Enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE0 high reference is exceeded
	[7]	0		STAGE7_HIGH_INT_EN	STAGE7 High Interrupt Enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE0 high reference is exceeded

Address	Data Bit Content	Default Value	Type	Name	Description
	[8]	0		STAGE8_HIGH_INT_EN	STAGE8 High Interrupt Enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE0 high reference is exceeded
	[9]	0		STAGE9_HIGH_INT_EN	STAGE9 Sensor Interrupt Low Limit Control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE10_LOW is exceeded
	[10]	0		STAGE10_HIGH_INT_EN	STAGE10 High Interrupt Enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE0 high reference is exceeded
	[11]	0		STAGE11_HIGH_INT_EN	STAGE11 High Interrupt Enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE0 high reference is exceeded
	[15:12]			Unused	Set Unused Register Bits = 0
007	[0]	0	R/W	STAGE0_COMPLETE_EN	STAGE0 Conversion Interrupt Control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE0 conversion
	[1]	0		STAGE1_COMPLETE_EN	STAGE1 Conversion Interrupt Control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE1 conversion
	[2]	0		STAGE2_COMPLETE_EN	STAGE2 Conversion Interrupt Control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE2 conversion
	[3]	0		STAGE3_COMPLETE_EN	STAGE3 Conversion Interrupt Control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE3 conversion
	[4]	0		STAGE4_COMPLETE_EN	STAGE4 Conversion Interrupt Control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE4 conversion
	[5]	0		STAGE5_COMPLETE_EN	STAGE5 Conversion Interrupt Control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE5 conversion
	[6]	0		STAGE6_COMPLETE_EN	STAGE6 Conversion Interrupt Control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE6 conversion
	[7]	0		STAGE7_COMPLETE_EN	STAGE7 Conversion Interrupt Control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE7 conversion
	[8]	0		STAGE8_COMPLETE_EN	STAGE8 Conversion Complete Interrupt Control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE8 conversion
	[9]	0		STAGE9_COMPLETE_EN	STAGE9 Conversion Interrupt Control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE9 conversion
	[10]	0		STAGE10_COMPLETE_EN	STAGE10 Conversion Interrupt Control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE10 conversion
	[11]	0		STAGE11_COMPLETE_EN	STAGE11 Conversion Interrupt Control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE11 conversion

Address	Data Bit Content	Default Value	Type	Name	Description
	[12]	0		GPIO_INT_EN	Interrupt Control when GPIO Input Pin Changes Level 0 = disabled 1 = enabled
	[15:13]			Unused	Set Unused Register Bits = 0

Table 22. CDC Low Limit Status Register Map[1]

Address	Data Bit Content	Default Value	Type	Name	Description
008	[0]	0	R	STAGE0_LOW_LIMIT	STAGE0 CDC Conversion Low Limit Result 1 = indicates STAGE0_OFFSET_LOW value was exceeded
	[1]	0		STAGE1_LOW_LIMIT	STAGE1 CDC Conversion Low Limit Result 1 = indicates STAGE1_OFFSET_LOW value was exceeded
	[2]	0		STAGE2_LOW_LIMIT	STAGE2 CDC Conversion Low Limit Result 1 = indicates STAGE2_OFFSET_LOW value was exceeded
	[3]	0		STAGE3_LOW_LIMIT	STAGE3 CDC Conversion Low Limit Result 1 = indicates STAGE3_OFFSET_LOW value was exceeded
	[4]	0		STAGE4_LOW_LIMIT	STAGE4 CDC Conversion Low Limit Result 1 = indicates STAGE4_OFFSET_LOW value was exceeded
	[5]	0		STAGE5_LOW_LIMIT	STAGE5 CDC Conversion Low Limit Result 1 = indicates STAGE5_OFFSET_LOW value was exceeded
	[6]	0		STAGE6_LOW_LIMIT	STAGE6 CDC Conversion Low Limit Result 1 = indicates STAGE6_OFFSET_LOW value was exceeded
	[7]	0		STAGE7_LOW_LIMIT	STAGE7 CDC Conversion Low Limit Result 1 = indicates STAGE7_OFFSET_LOW value was exceeded
	[8]	0		STAGE8_LOW_LIMIT	STAGE8 CDC Conversion Low Limit Result 1 = indicates STAGE8_OFFSET_LOW value was exceeded
	[9]	0		STAGE9_LOW_LIMIT	STAGE9 CDC Conversion Low Limit Result 1 = indicates STAGE9_OFFSET_LOW value was exceeded
	[10]	0		STAGE10_LOW_LIMIT	STAGE10 CDC Conversion Low Limit Result 1 = indicates STAGE10_OFFSET_LOW value was exceeded
	[11]	0		STAGE11_LOW_LIMIT	STAGE11 CDC Conversion Low Limit Result 1 = indicates STAGE11_OFFSET_LOW value was exceeded
	[15:12]			Unused	Set Unused Register Bits = 0

[1] Registers self-clear to 0 after readback, provided that the limits are not exceeded.

Table 23.CDC High Limit Status[1]

Address	Data Bit Content	Default Value	Type	Name	Description
009	[0]	0	R	STAGE0_HIGH_LIMIT	STAGE0 CDC Conversion High Limit Result 1 = indicates STAGE0_OFFSET_HIGH value was exceeded
	[1]	0		STAGE1_HIGH_LIMIT	STAGE1 CDC Conversion High Limit Result 1 = indicates STAGE1_OFFSET_HIGH value was exceeded
	[2]	0		STAGE2_HIGH_LIMIT	Stage2 CDC Conversion High Limit Result 1 = indicates STAGE2_OFFSET_HIGH value was exceeded
	[3]	0		STAGE3_HIGH_LIMIT	STAGE3 CDC Conversion High Limit Result 1 = indicates STAGE3_OFFSET_HIGH value was exceeded
	[4]	0		STAGE4_HIGH_LIMIT	STAGE4 CDC Conversion High Limit Result 1 = indicates STAGE4_OFFSET_HIGH value was exceeded
	[5]	0		STAGE5_HIGH_LIMIT	STAGE5 CDC Conversion High Limit Result 1 = indicates STAGE5_OFFSET_HIGH value was exceeded
	[6]	0		STAGE6_HIGH_LIMIT	STAGE6 CDC Conversion High Limit Result 1 = indicates STAGE6_OFFSET_HIGH value was exceeded
	[7]	0		STAGE7_HIGH_LIMIT	STAGE7 CDC Conversion Low Limit Result 1 = indicates STAGE7_OFFSET_HIGH value was exceeded
	[8]	0		STAGE8_HIGH_LIMIT	STAGE8 CDC Conversion High Limit Result 1 = indicates STAGE8_OFFSET_HIGH value was exceeded
	[9]	0		STAGE9_HIGH_LIMIT	STAGE9 CDC Conversion High Limit Result 1 = indicates STAGE9_OFFSET_HIGH value was exceeded
	[10]	0		STAGE10_HIGH_LIMIT	STAGE10 CDC Conversion High Limit Result 1 =indicates STAGE10_OFFSET_HIGH value was exceeded
	[11]	0		STAGE11_HIGH_LIMIT	STAGE11 CDC Conversion High Limit Result 1 = indicates STAGE11_OFFSET_HIGH value was exceeded
	[15:12]			Unused	Set Unused Register Bits = 0

[1] Registers self-clear to 0 after readback, provided that the limits are not exceeded.

Table 24. CDC Conversion Completion Register Map [1]

Address	Data Bit Content	Default Value	Type	Name	Description
00A	[0]	0	R	STAGE0_COMPLETE_STATUS	STAGE0 Conversion Completion Status 1 = indicates STAGE0 conversion completed
	[1]	0		STAGE1_COMPLETE_STATUS	STAGE1 Conversion Completion Status 1 = indicates STAGE0 conversion completed
	[2]	0		STAGE2_COMPLETE_STATUS	STAGE2 Conversion Completion Status 1 = indicates STAGE0 conversion completed
	[3]	0		STAGE3_COMPLETE_STATUS	STAGE3 Conversion Completion Status 1 = indicates STAGE0 conversion completed
	[4]	0		STAGE4_COMPLETE_STATUS	STAGE4 Conversion Completion Status 1 = indicates STAGE0 conversion completed
	[5]	0		STAGE5_COMPLETE_STATUS	STAGE5 Conversion Completion Status 1 = indicates STAGE0 conversion completed
	[6]	0		STAGE6_COMPLETE_STATUS	STAGE6 Conversion Completion Status 1 = indicates STAGE0 conversion completed
	[7]	0		STAGE7_COMPLETE_STATUS	STAGE7 Conversion Completion Status 1 = indicates STAGE0 conversion completed
	[8]	0		STAGE8_COMPLETE_STATUS	STAGE8 Conversion Completion Status 1 = indicates STAGE0 conversion completed
	[9]	0		STAGE9_COMPLETE_STATUS	STAGE9 Conversion Completion Status 1 = indicates STAGE0 conversion completed
	[10]	0		STAGE10_COMPLETE_STATUS	STAGE10 Conversion Completion Status 1 = indicates STAGE0 conversion completed
	[11]	0		STAGE11_COMPLETE_STATUS	STAGE11 Conversion Completion Status 1 = indicates STAGE0 conversion completed
	[12]	0		GPIO_STATUS	GPIO Input Pin Status 1 = indicates level on GPIO pin has changed
	[15:13]			Unused	Set Unused Register Bits = 0

[1] Registers self-clear to 0 after readback.

Table 25. CDC 16-Bit Conversion Data Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
00B	[15:0]	0	R	STAGE0_CONV_DATA	STAGE0 CDC 16-Bit Conversion Data
00C	[15:0]	0	R	STAGE1_CONV_DATA	STAGE1 CDC 16-Bit Conversion Data
00D	[15:0]	0	R	STAGE2_CONV_DATA	STAGE2 CDC 16-Bit Conversion Data
00E	[15:0]	0	R	STAGE3_CONV_DATA	STAGE3 CDC 16-Bit Conversion Data
00F	[15:0]	0	R	STAGE4_CONV_DATA	STAGE4 CDC 16-Bit Conversion Data
010	[15:0]	0	R	STAGE5_CONV_DATA	STAGE5 CDC 16-Bit Conversion Data
011	[15:0]	0	R	STAGE6_CONV_DATA	STAGE6 CDC 16-Bit Conversion Data
012	[15:0]	0	R	STAGE7_CONV_DATA	STAGE7 CDC 16-Bit Conversion Data
013	[15:0]	0	R	STAGE8_CONV_DATA	STAGE8 CDC 16-Bit Conversion Data
014	[15:0]	0	R	STAGE9_CONV_DATA	STAGE9 CDC 16-Bit Conversion Data
015	[15:0]	0	R	STAGE10_CONV_DATA	STAGE10 CDC 16-Bit Conversion Data
016	[15:0]	0	R	STAGE11_CONV_DATA	STAGE11 CDC 16-Bit Conversion Data

Table 26. Device ID Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
017	[3:0]	2	R	REVISION_CODE	AD7142 Revision Code
	[15:4]	E62	R	DEVICE_ID	AD7142 Device ID = 110110100010

Table 27. Proximity Status Register

Address	Data Bit Content	Default Value	Type	Name	Description
042	[0]	0	R	STAGE0_PROXIMITY_STATUS	STAGE0 Proximity Status Register 1 = indicates proximity has been detected on STAGE0
	[1]	0	R	STAGE1_PROXIMITY_STATUS	STAGE1 Proximity Status Register 1 = indicates proximity has been detected on STAGE1
	[2]	0	R	STAGE2_PROXIMITY_STATUS	STAGE2 Proximity Status Register 1 = indicates proximity has been detected on STAGE2
	[3]	0	R	STAGE3_PROXIMITY_STATUS	STAGE3 Proximity Status Register 1 = indicates proximity has been detected on STAGE3
	[4]	0	R	STAGE4_PROXIMITY_STATUS	STAGE4 Proximity Status Register 1 = indicates proximity has been detected on STAGE4
	[5]	0	R	STAGE5_PROXIMITY_STATUS	STAGE5 Proximity Status Register 1 = indicates proximity has been detected on STAGE5
	[6]	0	R	STAGE6_PROXIMITY_STATUS	STAGE6 Proximity Status Register 1 = indicates proximity has been detected on STAGE6
	[7]	0	R	STAGE7_PROXIMITY_STATUS	STAGE7 Proximity Status Register 1 = indicates proximity has been detected on STAGE7
	[8]	0	R	STAGE8_PROXIMITY_STATUS	STAGE8 Proximity Status Register 1 = indicates proximity has been detected on STAGE8
	[9]	0	R	STAGE9_PROXIMITY_STATUS	STAGE9 Proximity Status Register 1 = indicates proximity has been detected on STAGE9
	[10]	0	R	STAGE10_PROXIMITY_STATUS	STAGE10 Proximity Status Register 1 = indicates proximity has been detected on STAGE10
	[11]	0	R	STAGE11_PROXIMITY_STATUS	STAGE11 Proximity Status Register 1 = indicates proximity has been detected on STAGE11
	[15:0]			Unused	Set Unused Register Bits = 0

Table 28. Low Power Mode Settling Time Register

Address	Data Bit Content	Default Value	Type	Name	Description
045	[1:0]	0x3	R/W	Unused—test bits	Set Unused Register Bits = 11 Binary. Note that these bits always read back as 01 binary.
	[14:2]	0x240	R/W	Unused—test bits	Set Unused Register Bits = 0x240
	[15:13]	0x0	R/W	Low power mode settling time	These bits control the settling time of the ADC in low power mode. Each unit of delay is equivalent to one conversion time. Set to 0x2.

BANK 2 REGISTERS

All address values are expressed in hexadecimal.

Table 29. STAGE0 Configuration Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
080	[15:0]	X	R/W	STAGE0_CIN(0:6)_SETUP	STAGE0 CIN(0:6) Connection Set-Up (See Table 53)
081	[15:0]	X	R/W	STAGE0_CIN(7:13)_SETUP	STAGE0 CIN(7:13) Connection Set-Up (See Table 54)
082	[15:0]	X	R/W	STAGE0_AFE_OFFSET	STAGE0 AFE Offset Control (See Table 55)
083	[15:0]	X	R/W	STAGE0_SENSITIVITY	STAGE0 Sensitivity Control (See Table 56)
084	[15:0]	X	R/W	STAGE0_OFFSET_LOW	STAGE0 Initial Offset Low Value
085	[15:0]	X	R/W	STAGE0_OFFSET_HIGH	STAGE0 Initial Offset High Value
086	[15:0]	X	R/W	STAGE0_OFFSET_HIGH_CLAMP	STAGE0 Offset High Clamp Value
087	[15:0]	X	R/W	STAGE0_OFFSET_LOW_CLAMP	STAGE0 Offset Low Clamp Value

Table 30. STAGE1 Configuration Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
088	[15:0]	X	R/W	STAGE1_CIN(0:6)_SETUP	STAGE1 CIN(0:6) Connection Setup (See Table 53)
089	[15:0]	X	R/W	STAGE1_CIN(7:13)_SETUP	STAGE1 CIN(7:13) Connection Setup (See Table 54)
08A	[15:0]	X	R/W	STAGE1_AFE_OFFSET	STAGE1 AFE Offset Control (See Table 55)
08B	[15:0]	X	R/W	STAGE1_SENSITIVITY	STAGE1 Sensitivity Control (See Table 56)
08C	[15:0]	X	R/W	STAGE1_OFFSET_LOW	STAGE1 Initial Offset Low Value
08D	[15:0]	X	R/W	STAGE1_OFFSET_HIGH	STAGE1 Initial Offset High Value
08E	[15:0]	X	R/W	STAGE1_OFFSET_HIGH_CLAMP	STAGE1 Offset High Clamp Value
08F	[15:0]	X	R/W	STAGE1_OFFSET_LOW_CLAMP	STAGE1 Offset Low Clamp Value

Table 31. STAGE2 Configuration Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
090	[15:0]	X	R/W	STAGE2_CIN(0:6)_SETUP	STAGE2 CIN(0:6) Connection Setup (See Table 53)
091	[15:0]	X	R/W	STAGE2_CIN(7:13)_SETUP	STAGE2 CIN(7:13) Connection Setup (See Table 54)
092	[15:0]	X	R/W	STAGE2_AFE_OFFSET	STAGE2 AFE Offset Control (See Table 55)
093	[15:0]	X	R/W	STAGE2_SENSITIVITY	STAGE2 Sensitivity Control (See Table 56)
094	[15:0]	X	R/W	STAGE2_OFFSET_LOW	STAGE2 Initial Offset Low Value
095	[15:0]	X	R/W	STAGE2_OFFSET_HIGH	STAGE2 Initial Offset High Value
096	[15:0]	X	R/W	STAGE2_OFFSET_HIGH_CLAMP	STAGE2 Offset High Clamp Value
097	[15:0]	X	R/W	STAGE2_OFFSET_LOW_CLAMP	STAGE2 Offset Low Clamp Value

Table 32. STAGE3 Configuration Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
098	[15:0]	X	R/W	STAGE3_CIN(0:6)_SETUP	STAGE3 CIN(0:6) Connection Setup (See Table 53)
099	[15:0]	X	R/W	STAGE3_CIN(7:13)_SETUP	STAGE3 CIN(7:13) Connection Setup (See Table 54)
09A	[15:0]	X	R/W	STAGE3_AFE_OFFSET	STAGE3 AFE Offset Control (See Table 55)
09B	[15:0]	X	R/W	STAGE3_SENSITIVITY	STAGE3 Sensitivity Control (See Table 56)
09C	[15:0]	X	R/W	STAGE3_OFFSET_LOW	STAGE3 Initial Offset Low Value
09D	[15:0]	X	R/W	STAGE3_OFFSET_HIGH	STAGE3 Initial Offset High Value
09E	[15:0]	X	R/W	STAGE3_OFFSET_HIGH_CLAMP	STAGE3 Offset High Clamp Value
09F	[15:0]	X	R/W	STAGE3_OFFSET_LOW_CLAMP	STAGE3 Offset Low Clamp Value

Table 33. STAGE4 Configuration Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
0A0	[15:0]	X	R/W	STAGE4_CIN(0:6)_SETUP	STAGE4 CIN(0:6) Connection Setup (See Table 53)
0A1	[15:0]	X	R/W	STAGE4_CIN(7:13)_SETUP	STAGE4 CIN(7:13) Connection Setup (See Table 54)
0A2	[15:0]	X	R/W	STAGE4_AFE_OFFSET	STAGE4 AFE Offset Control (See Table 55)
0A3	[15:0]	X	R/W	STAGE4_SENSITIVITY	STAGE4 Sensitivity Control (See Table 56)
0A4	[15:0]	X	R/W	STAGE4_OFFSET_LOW	STAGE4 Initial Offset Low Value
0A5	[15:0]	X	R/W	STAGE4_OFFSET_HIGH	STAGE4 Initial Offset High Value
0A6	[15:0]	X	R/W	STAGE4_OFFSET_HIGH_CLAMP	STAGE4 Offset High Clamp Value
0A7	[15:0]	X	R/W	STAGE4_OFFSET_LOW_CLAMP	STAGE4 Offset Low Clamp Value

Table 34. STAGE5 Configuration Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
0A8	[15:0]	X	R/W	STAGE5_CIN(0:6)_SETUP	STAGE5 CIN(0:6) Connection Setup (See Table 53)
0A9	[15:0]	X	R/W	STAGE5_CIN(7:13)_SETUP	STAGE5 CIN(7:13) Connection Setup (See Table 54)
0AA	[15:0]	X	R/W	STAGE5_AFE_OFFSET	STAGE5 AFE Offset Control (See Table 55)
0AB	[15:0]	X	R/W	STAGE5_SENSITIVITY	STAGE5 Sensitivity Control (See Table 56)
0AC	[15:0]	X	R/W	STAGE5_OFFSET_LOW	STAGE5 Initial Offset Low Value
0AD	[15:0]	X	R/W	STAGE5_OFFSET_HIGH	STAGE5 Initial Offset High Value
0AE	[15:0]	X	R/W	STAGE5_OFFSET_HIGH_CLAMP	STAGE5 Offset High Clamp Value
0AF	[15:0]	X	R/W	STAGE5_OFFSET_LOW_CLAMP	STAGE5 Offset Low Clamp Value

Table 35. STAGE6 Configuration Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
0B0	[15:0]	X	R/W	STAGE6_CIN(0:6)_SETUP	STAGE6 CIN(0:6) Connection Setup (See Table 53)
0B1	[15:0]	X	R/W	STAGE6_CIN(7:13)_SETUP	STAGE6 CIN(7:13) Connection Setup (See Table 54)
0B2	[15:0]	X	R/W	STAGE6_AFE_OFFSET	STAGE6 AFE Offset Control (See Table 55)
0B3	[15:0]	X	R/W	STAGE6_SENSITIVITY	STAGE6 Sensitivity Control (See Table 56)
0B4	[15:0]	X	R/W	STAGE6_OFFSET_LOW	STAGE6 Initial Offset Low Value
0B5	[15:0]	X	R/W	STAGE6_OFFSET_HIGH	STAGE6 Initial Offset High Value
0B6	[15:0]	X	R/W	STAGE6_OFFSET_HIGH_CLAMP	STAGE6 Offset High Clamp Value
0B7	[15:0]	X	R/W	STAGE6_OFFSET_LOW_CLAMP	STAGE6 Offset Low Clamp Value

Table 36. STAGE7 Configuration Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
0B8	[15:0]	X	R/W	STAGE7_CIN(0:6)_SETUP	STAGE7 CIN(0:6) Connection Setup (See Table 53)
0B9	[15:0]	X	R/W	STAGE7_CIN(7:13)_SETUP	STAGE7 CIN(7:13) Connection Setup (See Table 54)
0BA	[15:0]	X	R/W	STAGE7_AFE_OFFSET	STAGE7 AFE Offset Control (See Table 55)
0BB	[15:0]	X	R/W	STAGE7_SENSITIVITY	STAGE7 Sensitivity Control (See Table 56)
0BC	[15:0]	X	R/W	STAGE7_OFFSET_LOW	STAGE7 Initial Offset Low Value
0BD	[15:0]	X	R/W	STAGE7_OFFSET_HIGH	STAGE7 Initial Offset High Value
0BE	[15:0]	X	R/W	STAGE7_OFFSET_HIGH_CLAMP	STAGE7 Offset High Clamp Value
0BF	[15:0]	X	R/W	STAGE7_OFFSET_LOW_CLAMP	STAGE7 Offset Low Clamp Value

Table 37. STAGE8 Configuration Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
0C0	[15:0]	X	R/W	STAGE8_CIN(0:6)_SETUP	STAGE8 CIN(0:6) Connection Setup (See Table 53)
0C1	[15:0]	X	R/W	STAGE8_CIN(7:13)_SETUP	STAGE8 CIN(7:13) Connection Setup (See Table 54)
0C2	[15:0]	X	R/W	STAGE8_AFE_OFFSET	STAGE8 AFE Offset Control (See Table 55)
0C3	[15:0]	X	R/W	STAGE8_SENSITIVITY	STAGE8 Sensitivity Control (See Table 56)
0C4	[15:0]	X	R/W	STAGE8_OFFSET_LOW	STAGE8 Initial Offset Low Value
0C5	[15:0]	X	R/W	STAGE8_OFFSET_HIGH	STAGE8 Initial Offset High Value
0C6	[15:0]	X	R/W	STAGE8_OFFSET_HIGH_CLAMP	STAGE8 Offset High Clamp Value
0C7	[15:0]	X	R/W	STAGE8_OFFSET_LOW_CLAMP	STAGE8 Offset Low Clamp Value

Table 38. STAGE9 Configuration Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
0C8	[15:0]	X	R/W	STAGE9_CIN(0:6)_SETUP	STAGE9 CIN(0:6) Connection Setup (See Table 53)
0C9	[15:0]	X	R/W	STAGE9_CIN(7:13)_SETUP	STAGE9 CIN(7:13) Connection Setup (See Table 54)
0CA	[15:0]	X	R/W	STAGE9_AFE_OFFSET	STAGE9 AFE Offset Control (See Table 55)
0CB	[15:0]	X	R/W	STAGE9_SENSITIVITY	STAGE9 Sensitivity Control (See Table 56)
0CC	[15:0]	X	R/W	STAGE9_OFFSET_LOW	STAGE9 Initial Offset LOW Value
0CD	[15:0]	X	R/W	STAGE9_OFFSET_HIGH	STAGE9 Initial Offset HIGH Value
0CE	[15:0]	X	R/W	STAGE9_OFFSET_HIGH_CLAMP	STAGE9 Offset High Clamp Value
0CF	[15:0]	X	R/W	STAGE9_OFFSET_LOW_CLAMP	STAGE9 Offset Low Clamp Value

Table 39. STAGE10 Configuration Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
0D0	[15:0]	X	R/W	STAGE10_CIN(0:6)_SETUP	STAGE10 CIN(0:6) Connection Setup (See Table 53)
0D1	[15:0]	X	R/W	STAGE10_CIN(7:13)_SETUP	STAGE10 CIN(7:13) Connection Setup (See Table 54)
0D2	[15:0]	X	R/W	STAGE10_AFE_OFFSET	STAGE10 AFE Offset Control (See Table 55)
0D3	[15:0]	X	R/W	STAGE10_SENSITIVITY	STAGE10 Sensitivity Control (See Table 56)
0D4	[15:0]	X	R/W	STAGE10_OFFSET_LOW	STAGE10 Initial Offset LOW Value
0D5	[15:0]	X	R/W	STAGE10_OFFSET_HIGH	STAGE10 Initial Offset HIGH Value
0D6	[15:0]	X	R/W	STAGE10_OFFSET_HIGH_CLAMP	STAGE10 Offset High Clamp Value
0D7	[15:0]	X	R/W	STAGE10_OFFSET_LOW_CLAMP	STAGE10 Offset Low Clamp Value

Table 40. STAGE11 Configuration Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
0D8	[15:0]	X	R/W	STAGE11_CIN(0:6)_SETUP	STAGE11 CIN(0:6) Connection Setup (See Table 53)
0D9	[15:0]	X	R/W	STAGE11_CIN(7:13)_SETUP	STAGE11 CIN(7:13) Connection Setup (See Table 54)
0DA	[15:0]	X	R/W	STAGE11_AFE_OFFSET	STAGE11 AFE Offset Control (See Table 55)
0DB	[15:0]	X	R/W	STAGE11_SENSITIVITY	STAGE11 Sensitivity Control (See Table 56)
0DC	[15:0]	X	R/W	STAGE11_OFFSET_LOW	STAGE11 Initial Offset LOW Value
0DD	[15:0]	X	R/W	STAGE11_OFFSET_HIGH	STAGE11 Initial Offset HIGH Value
0DE	[15:0]	X	R/W	STAGE11_OFFSET_HIGH_CLAMP	STAGE11 Offset High Clamp Value
0DF	[15:0]	X	R/W	STAGE11_OFFSET_LOW_CLAMP	STAGE11 Offset Low Clamp Value

BANK 3 REGISTERS

All address values are expressed in hexadecimal.

Table 41. STAGE0 Results Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
0E0	[15:0]	X	R/W	STAGE0_CONV_DATA	STAGE0 CDC 16-Bit Conversion Data (Copy of data in STAGE0_CONV_DATA register)
0E1	[15:0]	X	R/W	STAGE0_FF_WORD0	STAGE0 Fast FIFO WORD0
0E2	[15:0]	X	R/W	STAGE0_FF_WORD1	STAGE0 Fast FIFO WORD1
0E3	[15:0]	X	R/W	STAGE0_FF_WORD2	STAGE0 Fast FIFO WORD2
0E4	[15:0]	X	R/W	STAGE0_FF_WORD3	STAGE0 Fast FIFO WORD3
0E5	[15:0]	X	R/W	STAGE0_FF_WORD4	STAGE0 Fast FIFO WORD4
0E6	[15:0]	X	R/W	STAGE0_FF_WORD5	STAGE0 Fast FIFO WORD5
0E7	[15:0]	X	R/W	STAGE0_FF_WORD6	STAGE0 Fast FIFO WORD6
0E8	[15:0]	X	R/W	STAGE0_FF_WORD7	STAGE0 Fast FIFO WORD7
0E9	[15:0]	X	R/W	STAGE0_SF_WORD0	STAGE0 Slow FIFO WORD0
0EA	[15:0]	X	R/W	STAGE0_SF_WORD1	STAGE0 Slow FIFO WORD1
0EB	[15:0]	X	R/W	STAGE0_SF_WORD2	STAGE0 Slow FIFO WORD2
0EC	[15:0]	X	R/W	STAGE0_SF_WORD3	STAGE0 Slow FIFO WORD3
0ED	[15:0]	X	R/W	STAGE0_SF_WORD4	STAGE0 Slow FIFO WORD4
0EE	[15:0]	X	R/W	STAGE0_SF_WORD5	STAGE0 Slow FIFO WORD5
0EF	[15:0]	X	R/W	STAGE0_SF_WORD6	STAGE0 Slow FIFO WORD6
0F0	[15:0]	X	R/W	STAGE0_SF_WORD7	STAGE0 Slow FIFO WORD7
0F1	[15:0]	X	R/W	STAGE0_SF_AMBIENT	STAGE0 Slow FIFO Ambient Value
0F2	[15:0]	X	R/W	STAGE0_FF_AVG	STAGE0 Fast FIFO Average Value
0F3	[15:0]	X	R/W	STAGE0_PEAK_DETECT_WORD0	STAGE0 Peak FIFO WORD0 Value
0F4	[15:0]	X	R/W	STAGE0_PEAK_DETECT_WORD1	STAGE0 Peak FIFO WORD1 Value
0F5	[15:0]	X	R/W	STAGE0_MAX_WORD0	STAGE0 Maximum Value FIFO WORD0
0F6	[15:0]	X	R/W	STAGE0_MAX_WORD1	STAGE0 Maximum Value FIFO WORD1
0F7	[15:0]	X	R/W	STAGE0_MAX_WORD2	STAGE0 Maximum Value FIFO WORD2
0F8	[15:0]	X	R/W	STAGE0_MAX_WORD3	STAGE0 Maximum Value FIFO WORD3
0F9	[15:0]	X	R/W	STAGE0_MAX_AVG	STAGE0 Average Maximum FIFO Value
0FA	[15:0]	X	R/W	STAGE0_HIGH_THRESHOLD	STAGE0 High Threshold Value
0FB	[15:0]	X	R/W	STAGE0_MAX_TEMP	STAGE0 Temporary Maximum Value
0FC	[15:0]	X	R/W	STAGE0_MIN_WORD0	STAGE0 Minimum Value FIFO WORD0
0FD	[15:0]	X	R/W	STAGE0_MIN_WORD1	STAGE0 Minimum Value FIFO WORD1
0FE	[15:0]	X	R/W	STAGE0_MIN_WORD2	STAGE0 Minimum Value FIFO WORD2
0FF	[15:0]	X	R/W	STAGE0_MIN_WORD3	STAGE0 Minimum Value FIFO WORD3
100	[15:0]	X	R/W	STAGE0_MIN_AVG	STAGE0 Average Minimum FIFO Value
101	[15:0]	X	R/W	STAGE0_LOW_THRESHOLD	STAGE0 Low Threshold Value
102	[15:0]	X	R/W	STAGE0_MIN_TEMP	STAGE0 Temporary Minimum Value
103	[15:0]	X	R/W	Unused	

Table 42. STAGE1 Results Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
104	[15:0]	X	R/W	STAGE1_CONV_DATA	STAGE1 CDC 16-Bit Conversion Data (Copy of data in STAGE1_CONV_DATA register)
105	[15:0]	X	R/W	STAGE1_FF_WORD0	STAGE1 Fast FIFO WORD0
106	[15:0]	X	R/W	STAGE1_FF_WORD1	STAGE1 Fast FIFO WORD1
107	[15:0]	X	R/W	STAGE1_FF_WORD2	STAGE1 Fast FIFO WORD2
108	[15:0]	X	R/W	STAGE1_FF_WORD3	STAGE1 Fast FIFO WORD3
109	[15:0]	X	R/W	STAGE1_FF_WORD4	STAGE1 Fast FIFO WORD4
10A	[15:0]	X	R/W	STAGE1_FF_WORD5	STAGE1 Fast FIFO WORD5
10B	[15:0]	X	R/W	STAGE1_FF_WORD6	STAGE1 Fast FIFO WORD6
10C	[15:0]	X	R/W	STAGE1_FF_WORD7	STAGE1 Fast FIFO WORD7
10D	[15:0]	X	R/W	STAGE1_SF_WORD0	STAGE1 Slow FIFO WORD0
10E	[15:0]	X	R/W	STAGE1_SF_WORD1	STAGE1 Slow FIFO WORD1
10F	[15:0]	X	R/W	STAGE1_SF_WORD2	STAGE1 Slow FIFO WORD2
110	[15:0]	X	R/W	STAGE1_SF_WORD3	STAGE1 Slow FIFO WORD3
111	[15:0]	X	R/W	STAGE1_SF_WORD4	STAGE1 Slow FIFO WORD4
112	[15:0]	X	R/W	STAGE1_SF_WORD5	STAGE1 Slow FIFO WORD5
113	[15:0]	X	R/W	STAGE1_SF_WORD6	STAGE1 Slow FIFO WORD6
114	[15:0]	X	R/W	STAGE1_SF_WORD7	STAGE1 Slow FIFO WORD7
115	[15:0]	X	R/W	STAGE1_SF_AMBIENT	STAGE1 Slow FIFO Ambient Value
116	[15:0]	X	R/W	STAGE1_FF_AVG	STAGE1 Fast FIFO Average Value
117	[15:0]	X	R/W	STAGE1_CDC_WORD0	STAGE1 CDC FIFO WORD0
118	[15:0]	X	R/W	STAGE1_CDC_WORD1	STAGE1 CDC FIFO WORD1
119	[15:0]	X	R/W	STAGE1_MAX_WORD0	STAGE1 Maximum Value FIFO WORD0
11A	[15:0]	X	R/W	STAGE1_MAX_WORD1	STAGE1 Maximum Value FIFO WORD1
11B	[15:0]	X	R/W	STAGE1_MAX_WORD2	STAGE1 Maximum Value FIFO WORD2
11C	[15:0]	X	R/W	STAGE1_MAX_WORD3	STAGE1 Maximum Value FIFO WORD3
11D	[15:0]	X	R/W	STAGE1_MAX_AVG	STAGE1 Average Maximum FIFO Value
11E	[15:0]	X	R/W	STAGE1_HIGH_THRESHOLD	STAGE1 High Threshold Value
11F	[15:0]	X	R/W	STAGE1_MAX_TEMP	STAGE1 Temporary Maximum Value
120	[15:0]	X	R/W	STAGE1_MIN_WORD0	STAGE1 Minimum Value FIFO WORD0
121	[15:0]	X	R/W	STAGE1_MIN_WORD1	STAGE1 Minimum Value FIFO WORD1
122	[15:0]	X	R/W	STAGE1_MIN_WORD2	STAGE1 Minimum Value FIFO WORD2
123	[15:0]	X	R/W	STAGE1_MIN_WORD3	STAGE1 Minimum Value FIFO WORD3
124	[15:0]	X	R/W	STAGE1_MIN_AVG	STAGE1 Average Minimum FIFO Value
125	[15:0]	X	R/W	STAGE1_LOW_THRESHOLD	STAGE1 Low Threshold Value
126	[15:0]	X	R/W	STAGE1_MIN_TEMP	STAGE1 Temporary Minimum Value
127	[15:0]	X	R/W	Unused	

Table 43. STAGE2 Results Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
128	[15:0]	X	R/W	STAGE2_CONV_DATA	STAGE2 CDC 16-Bit Conversion Data (Copy of data in STAGE2_CONV_DATA register)
129	[15:0]	X	R/W	STAGE2_FF_WORD0	STAGE2 Fast FIFO WORD0
12A	[15:0]	X	R/W	STAGE2_FF_WORD1	STAGE2 Fast FIFO WORD1
12B	[15:0]	X	R/W	STAGE2_FF_WORD2	STAGE2 Fast FIFO WORD2
12C	[15:0]	X	R/W	STAGE2_FF_WORD3	STAGE2 Fast FIFO WORD3
12D	[15:0]	X	R/W	STAGE2_FF_WORD4	STAGE2 Fast FIFO WORD4
12E	[15:0]	X	R/W	STAGE2_FF_WORD5	STAGE2 Fast FIFO WORD5
12F	[15:0]	X	R/W	STAGE2_FF_WORD6	STAGE2 Fast FIFO WORD6
130	[15:0]	X	R/W	STAGE2_FF_WORD7	STAGE2 Fast FIFO WORD7
131	[15:0]	X	R/W	STAGE2_SF_WORD0	STAGE2 Slow FIFO WORD0
132	[15:0]	X	R/W	STAGE2_SF_WORD1	STAGE2 Slow FIFO WORD1
133	[15:0]	X	R/W	STAGE2_SF_WORD2	STAGE2 Slow FIFO WORD2
134	[15:0]	X	R/W	STAGE2_SF_WORD3	STAGE2 Slow FIFO WORD3
135	[15:0]	X	R/W	STAGE2_SF_WORD4	STAGE2 Slow FIFO WORD4
136	[15:0]	X	R/W	STAGE2_SF_WORD5	STAGE2 Slow FIFO WORD5
137	[15:0]	X	R/W	STAGE2_SF_WORD6	STAGE2 Slow FIFO WORD6
138	[15:0]	X	R/W	STAGE2_SF_WORD7	STAGE2 Slow FIFO WORD7
139	[15:0]	X	R/W	STAGE2_SF_AMBIENT	STAGE2 Slow FIFO Ambient Value
13A	[15:0]	X	R/W	STAGE2_FF_AVG	STAGE2 Fast FIFO Average Value
13B	[15:0]	X	R/W	STAGE2_CDC_WORD0	STAGE2 CDC FIFO WORD0
13C	[15:0]	X	R/W	STAGE2_CDC_WORD1	STAGE2 CDC FIFO WORD1
13D	[15:0]	X	R/W	STAGE2_MAX_WORD0	STAGE2 Maximum Value FIFO WORD0
13E	[15:0]	X	R/W	STAGE2_MAX_WORD1	STAGE2 Maximum Value FIFO WORD1
13F	[15:0]	X	R/W	STAGE2_MAX_WORD2	STAGE2 Maximum Value FIFO WORD2
140	[15:0]	X	R/W	STAGE2_MAX_WORD3	STAGE2 Maximum Value FIFO WORD3
141	[15:0]	X	R/W	STAGE2_MAX_AVG	STAGE2 Average Maximum FIFO Value
142	[15:0]	X	R/W	STAGE2_HIGH_THRESHOLD	STAGE2 High Threshold Value
143	[15:0]	X	R/W	STAGE2_MAX_TEMP	STAGE2 Temporary Maximum Value
144	[15:0]	X	R/W	STAGE2_MIN_WORD0	STAGE2 Minimum Value FIFO WORD0
145	[15:0]	X	R/W	STAGE2_MIN_WORD1	STAGE2 Minimum Value FIFO WORD1
146	[15:0]	X	R/W	STAGE2_MIN_WORD2	STAGE2 Minimum Value FIFO WORD2
147	[15:0]	X	R/W	STAGE2_MIN_WORD3	STAGE2 Minimum Value FIFO WORD3
148	[15:0]	X	R/W	STAGE2_MIN_AVG	STAGE2 Average Minimum FIFO Value
149	[15:0]	X	R/W	STAGE2_LOW_THRESHOLD	STAGE2 Low Threshold Value
14A	[15:0]	X	R/W	STAGE2_MIN_TEMP	STAGE2 Temporary Minimum Value
14B	[15:0]	X	R/W	Unused	

Table 44. STAGE3 Results Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
14C	[15:0]	X	R/W	STAGE3_CONV_DATA	STAGE3 CDC 16-Bit Conversion Data (Copy of data in STAGE3_CONV_DATA register)
14D	[15:0]	X	R/W	STAGE3_FF_WORD0	STAGE3 Fast FIFO WORD0
14E	[15:0]	X	R/W	STAGE3_FF_WORD1	STAGE3 Fast FIFO WORD1
14F	[15:0]	X	R/W	STAGE3_FF_WORD2	STAGE3 Fast FIFO WORD2
150	[15:0]	X	R/W	STAGE3_FF_WORD3	STAGE3 Fast FIFO WORD3
151	[15:0]	X	R/W	STAGE3_FF_WORD4	STAGE3 Fast FIFO WORD4
152	[15:0]	X	R/W	STAGE3_FF_WORD5	STAGE3 Fast FIFO WORD5
153	[15:0]	X	R/W	STAGE3_FF_WORD6	STAGE3 Fast FIFO WORD6
154	[15:0]	X	R/W	STAGE3_FF_WORD7	STAGE3 Fast FIFO WORD7
155	[15:0]	X	R/W	STAGE3_SF_WORD0	STAGE3 Slow FIFO WORD0
156	[15:0]	X	R/W	STAGE3_SF_WORD1	STAGE3 Slow FIFO WORD1
157	[15:0]	X	R/W	STAGE3_SF_WORD2	STAGE3 Slow FIFO WORD2
158	[15:0]	X	R/W	STAGE3_SF_WORD3	STAGE3 Slow FIFO WORD3
159	[15:0]	X	R/W	STAGE3_SF_WORD4	STAGE3 Slow FIFO WORD4
15A	[15:0]	X	R/W	STAGE3_SF_WORD5	STAGE3 Slow FIFO WORD5
15B	[15:0]	X	R/W	STAGE3_SF_WORD6	STAGE3 Slow FIFO WORD6
15C	[15:0]	X	R/W	STAGE3_SF_WORD7	STAGE3 Slow FIFO WORD7
15D	[15:0]	X	R/W	STAGE3_SF_AMBIENT	STAGE3 Slow FIFO Ambient Value
15E	[15:0]	X	R/W	STAGE3_FF_AVG	STAGE3 Fast FIFO Average Value
15F	[15:0]	X	R/W	STAGE3_CDC_WORD0	STAGE3 CDC FIFO WORD0
160	[15:0]	X	R/W	STAGE3_CDC_WORD1	STAGE3 CDC FIFO WORD1
161	[15:0]	X	R/W	STAGE3_MAX_WORD0	STAGE3 Maximum Value FIFO WORD0
162	[15:0]	X	R/W	STAGE3_MAX_WORD1	STAGE3 Maximum Value FIFO WORD1
163	[15:0]	X	R/W	STAGE3_MAX_WORD2	STAGE3 Maximum Value FIFO WORD2
164	[15:0]	X	R/W	STAGE3_MAX_WORD3	STAGE3 Maximum Value FIFO WORD3
165	[15:0]	X	R/W	STAGE3_MAX_AVG	STAGE3 Average Maximum FIFO Value
166	[15:0]	X	R/W	STAGE3_HIGH_THRESHOLD	STAGE3 High Threshold Value
167	[15:0]	X	R/W	STAGE3_MAX_TEMP	STAGE3 Temporary Maximum Value
168	[15:0]	X	R/W	STAGE3_MIN_WORD0	STAGE3 Minimum Value FIFO WORD0
169	[15:0]	X	R/W	STAGE3_MIN_WORD1	STAGE3 Minimum Value FIFO WORD1
16A	[15:0]	X	R/W	STAGE3_MIN_WORD2	STAGE3 Minimum Value FIFO WORD2
16B	[15:0]	X	R/W	STAGE3_MIN_WORD3	STAGE3 Minimum Value FIFO WORD3
16C	[15:0]	X	R/W	STAGE3_MIN_AVG	STAGE3 Average Minimum FIFO Value
16D	[15:0]	X	R/W	STAGE3_LOW_THRESHOLD	STAGE3 Low Threshold Value
16E	[15:0]	X	R/W	STAGE3_MIN_TEMP	STAGE3 Temporary Minimum Value
16F	[15:0]	X	R/W	Unused	

Table 45. STAGE4 Results Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
170	[15:0]	X	R/W	STAGE4_CONV_DATA	STAGE4 CDC 16-Bit Conversion Data (Copy of data in STAGE4_CONV_DATA register)
171	[15:0]	X	R/W	STAGE4_FF_WORD0	STAGE4 Fast FIFO WORD0
172	[15:0]	X	R/W	STAGE4_FF_WORD1	STAGE4 Fast FIFO WORD1
173	[15:0]	X	R/W	STAGE4_FF_WORD2	STAGE4 Fast FIFO WORD2
174	[15:0]	X	R/W	STAGE4_FF_WORD3	STAGE4 Fast FIFO WORD3
175	[15:0]	X	R/W	STAGE4_FF_WORD4	STAGE4 Fast FIFO WORD4
176	[15:0]	X	R/W	STAGE4_FF_WORD5	STAGE4 Fast FIFO WORD5
177	[15:0]	X	R/W	STAGE4_FF_WORD6	STAGE4 Fast FIFO WORD6
178	[15:0]	X	R/W	STAGE4_FF_WORD7	STAGE4 Fast FIFO WORD7
179	[15:0]	X	R/W	STAGE4_SF_WORD0	STAGE4 Slow FIFO WORD0
17A	[15:0]	X	R/W	STAGE4_SF_WORD1	STAGE4 Slow FIFO WORD1
17B	[15:0]	X	R/W	STAGE4_SF_WORD2	STAGE4 Slow FIFO WORD2
17C	[15:0]	X	R/W	STAGE4_SF_WORD3	STAGE4 Slow FIFO WORD3
17D	[15:0]	X	R/W	STAGE4_SF_WORD4	STAGE4 Slow FIFO WORD4
17E	[15:0]	X	R/W	STAGE4_SF_WORD5	STAGE4 Slow FIFO WORD5
17F	[15:0]	X	R/W	STAGE4_SF_WORD6	STAGE4 Slow FIFO WORD6
180	[15:0]	X	R/W	STAGE4_SF_WORD7	STAGE4 Slow FIFO WORD7
181	[15:0]	X	R/W	STAGE4_SF_AMBIENT	STAGE4 Slow FIFO Ambient Value
182	[15:0]	X	R/W	STAGE4_FF_AVG	STAGE4 Fast FIFO Average Value
183	[15:0]	X	R/W	STAGE4_CDC_WORD0	STAGE4 CDC FIFO WORD0
184	[15:0]	X	R/W	STAGE4_CDC_WORD1	STAGE4 CDC FIFO WORD1
185	[15:0]	X	R/W	STAGE4_MAX_WORD0	STAGE4 Maximum Value FIFO WORD0
186	[15:0]	X	R/W	STAGE4_MAX_WORD1	STAGE4 Maximum Value FIFO WORD1
187	[15:0]	X	R/W	STAGE4_MAX_WORD2	STAGE4 Maximum Value FIFO WORD2
188	[15:0]	X	R/W	STAGE4_MAX_WORD3	STAGE4 Maximum Value FIFO WORD3
189	[15:0]	X	R/W	STAGE4_MAX_AVG	STAGE4 Average Maximum FIFO Value
18A	[15:0]	X	R/W	STAGE4_HIGH_THRESHOLD	STAGE4 High Threshold Value
18B	[15:0]	X	R/W	STAGE4_MAX_TEMP	STAGE4 Temporary Maximum Value
18C	[15:0]	X	R/W	STAGE4_MIN_WORD0	STAGE4 Minimum Value FIFO WORD0
18D	[15:0]	X	R/W	STAGE4_MIN_WORD1	STAGE4 Minimum Value FIFO WORD1
18E	[15:0]	X	R/W	STAGE4_MIN_WORD2	STAGE4 Minimum Value FIFO WORD2
18F	[15:0]	X	R/W	STAGE4_MIN_WORD3	STAGE4 Minimum Value FIFO WORD3
190	[15:0]	X	R/W	STAGE4_MIN_AVG	STAGE4 Average Minimum FIFO Value
191	[15:0]	X	R/W	STAGE4_LOW_THRESHOLD	STAGE4 Low Threshold Value
192	[15:0]	X	R/W	STAGE4_MIN_TEMP	STAGE4 Temporary Minimum Value
193	[15:0]	X	R/W	Unused	

Table 46. STAGE5 Results Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
194	[15:0]	X	R/W	STAGE5_CONV_DATA	STAGE5 CDC 16-Bit Conversion Data (Copy of data in STAGE5_CONV_DATA register)
195	[15:0]	X	R/W	STAGE5_FF_WORD0	STAGE5 Fast FIFO WORD0
196	[15:0]	X	R/W	STAGE5_FF_WORD1	STAGE5 Fast FIFO WORD1
197	[15:0]	X	R/W	STAGE5_FF_WORD2	STAGE5 Fast FIFO WORD2
198	[15:0]	X	R/W	STAGE5_FF_WORD3	STAGE5 Fast FIFO WORD3
199	[15:0]	X	R/W	STAGE5_FF_WORD4	STAGE5 Fast FIFO WORD4
19A	[15:0]	X	R/W	STAGE5_FF_WORD5	STAGE5 Fast FIFO WORD5
19B	[15:0]	X	R/W	STAGE5_FF_WORD6	STAGE5 Fast FIFO WORD6
19C	[15:0]	X	R/W	STAGE5_FF_WORD7	STAGE5 Fast FIFO WORD7
19D	[15:0]	X	R/W	STAGE5_SF_WORD0	STAGE5 Slow FIFO WORD0
19E	[15:0]	X	R/W	STAGE5_SF_WORD1	STAGE5 Slow FIFO WORD1
19F	[15:0]	X	R/W	STAGE5_SF_WORD2	STAGE5 Slow FIFO WORD2
1A0	[15:0]	X	R/W	STAGE5_SF_WORD3	STAGE5 Slow FIFO WORD3
1A1	[15:0]	X	R/W	STAGE5_SF_WORD4	STAGE5 Slow FIFO WORD4
1A2	[15:0]	X	R/W	STAGE5_SF_WORD5	STAGE5 Slow FIFO WORD5
1A3	[15:0]	X	R/W	STAGE5_SF_WORD6	STAGE5 Slow FIFO WORD6
1A4	[15:0]	X	R/W	STAGE5_SF_WORD7	STAGE5 Slow FIFO WORD7
1A5	[15:0]	X	R/W	STAGE5_SF_AMBIENT	STAGE5 Slow FIFO Ambient Value
1A6	[15:0]	X	R/W	STAGE5_FF_AVG	STAGE5 Fast FIFO Average Value
1A7	[15:0]	X	R/W	STAGE5_CDC_WORD0	STAGE5 CDC FIFO WORD0
1A8	[15:0]	X	R/W	STAGE5_CDC_WORD1	STAGE5 CDC FIFO WORD1
1A9	[15:0]	X	R/W	STAGE5_MAX_WORD0	STAGE5 Maximum Value FIFO WORD0
1AA	[15:0]	X	R/W	STAGE5_MAX_WORD1	STAGE5 Maximum Value FIFO WORD1
1AB	[15:0]	X	R/W	STAGE5_MAX_WORD2	STAGE5 Maximum Value FIFO WORD2
1AC	[15:0]	X	R/W	STAGE5_MAX_WORD3	STAGE5 Maximum Value FIFO WORD3
1AD	[15:0]	X	R/W	STAGE5_MAX_AVG	STAGE5 Average Maximum FIFO Value
1AE	[15:0]	X	R/W	STAGE5_HIGH_THRESHOLD	STAGE5 High Threshold Value
1AF	[15:0]	X	R/W	STAGE5_MAX_TEMP	STAGE5 Temporary Maximum Value
1B0	[15:0]	X	R/W	STAGE5_MIN_WORD0	STAGE5 Minimum Value FIFO WORD0
1B1	[15:0]	X	R/W	STAGE5_MIN_WORD1	STAGE5 Minimum Value FIFO WORD1
1B2	[15:0]	X	R/W	STAGE5_MIN_WORD2	STAGE5 Minimum Value FIFO WORD2
1B3	[15:0]	X	R/W	STAGE5_MIN_WORD3	STAGE5 Minimum Value FIFO WORD3
1B4	[15:0]	X	R/W	STAGE5_MIN_AVG	STAGE5 Average Minimum FIFO Value
1B5	[15:0]	X	R/W	STAGE5_LOW_THRESHOLD	STAGE5 Low Threshold Value
1B6	[15:0]	X	R/W	STAGE5_MIN_TEMP	STAGE5 Temporary Minimum Value
1B7	[15:0]	X	R/W	Unused	

Table 47. STAGE6 Results Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
1B8	[15:0]	X	R/W	STAGE6_CONV_DATA	STAGE6 CDC 16-Bit Conversion Data (Copy of data in STAGE6_CONV_DATA register)
1B9	[15:0]	X	R/W	STAGE6_FF_WORD0	STAGE6 Fast FIFO WORD0
1BA	[15:0]	X	R/W	STAGE6_FF_WORD1	STAGE6 Fast FIFO WORD1
1BB	[15:0]	X	R/W	STAGE6_FF_WORD2	STAGE6 Fast FIFO WORD2
1BC	[15:0]	X	R/W	STAGE6_FF_WORD3	STAGE6 Fast FIFO WORD3
1BD	[15:0]	X	R/W	STAGE6_FF_WORD4	STAGE6 Fast FIFO WORD4
1BE	[15:0]	X	R/W	STAGE6_FF_WORD5	STAGE6 Fast FIFO WORD5
1BF	[15:0]	X	R/W	STAGE6_FF_WORD6	STAGE6 Fast FIFO WORD6
1C0	[15:0]	X	R/W	STAGE6_FF_WORD7	STAGE6 Fast FIFO WORD7
1C1	[15:0]	X	R/W	STAGE6_SF_WORD0	STAGE6 Slow FIFO WORD0
1C2	[15:0]	X	R/W	STAGE6_SF_WORD1	STAGE6 Slow FIFO WORD1
1C3	[15:0]	X	R/W	STAGE6_SF_WORD2	STAGE6 Slow FIFO WORD2
1C4	[15:0]	X	R/W	STAGE6_SF_WORD3	STAGE6 Slow FIFO WORD3
1C5	[15:0]	X	R/W	STAGE6_SF_WORD4	STAGE6 Slow FIFO WORD4
1C6	[15:0]	X	R/W	STAGE6_SF_WORD5	STAGE6 Slow FIFO WORD5
1C7	[15:0]	X	R/W	STAGE6_SF_WORD6	STAGE6 Slow FIFO WORD6
1C8	[15:0]	X	R/W	STAGE6_SF_WORD7	STAGE6 Slow FIFO WORD7
1C9	[15:0]	X	R/W	STAGE6_SF_AMBIENT	STAGE6 Slow FIFO Ambient Value
1CA	[15:0]	X	R/W	STAGE6_FF_AVG	STAGE6 Fast FIFO Average Value
1CB	[15:0]	X	R/W	STAGE6_CDC_WORD0	STAGE0 CDC FIFO WORD0
1CC	[15:0]	X	R/W	STAGE6_CDC_WORD1	STAGE6 CDC FIFO WORD1
1CD	[15:0]	X	R/W	STAGE6_MAX_WORD0	STAGE6 Maximum Value FIFO WORD0
1CE	[15:0]	X	R/W	STAGE6_MAX_WORD1	STAGE6 Maximum Value FIFO WORD1
1CF	[15:0]	X	R/W	STAGE6_MAX_WORD2	STAGE6 Maximum Value FIFO WORD2
1D0	[15:0]	X	R/W	STAGE6_MAX_WORD3	STAGE6 Maximum Value FIFO WORD3
1D1	[15:0]	X	R/W	STAGE6_MAX_AVG	STAGE6 Average Maximum FIFO Value
1D2	[15:0]	X	R/W	STAGE6_HIGH_THRESHOLD	STAGE6 High Threshold Value
1D3	[15:0]	X	R/W	STAGE6_MAX_TEMP	STAGE6 Temporary Maximum Value
1D4	[15:0]	X	R/W	STAGE6_MIN_WORD0	STAGE6 Minimum Value FIFO WORD0
1D5	[15:0]	X	R/W	STAGE6_MIN_WORD1	STAGE6 Minimum Value FIFO WORD1
1D6	[15:0]	X	R/W	STAGE6_MIN_WORD2	STAGE6 Minimum Value FIFO WORD2
1D7	[15:0]	X	R/W	STAGE6_MIN_WORD3	STAGE6 Minimum Value FIFO WORD3
1D8	[15:0]	X	R/W	STAGE6_MIN_AVG	STAGE6 Average Minimum FIFO Value
1D9	[15:0]	X	R/W	STAGE6_LOW_THRESHOLD	STAGE6 Low Threshold Value
1DA	[15:0]	X	R/W	STAGE6_MIN_TEMP	STAGE6 Temporary Minimum Value
1DB	[15:0]	X	R/W	Unused	

Table 48. STAGE7 Results Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
1DC	[15:0]	X	R/W	STAGE7_CONV_DATA	STAGE7 CDC 16-Bit Conversion Data (Copy of data in STAGE7_CONV_DATA register)
1DD	[15:0]	X	R/W	STAGE7_FF_WORD0	STAGE7 Fast FIFO WORD0
1DE	[15:0]	X	R/W	STAGE7_FF_WORD1	STAGE7 Fast FIFO WORD1
1DF	[15:0]	X	R/W	STAGE7_FF_WORD2	STAGE7 Fast FIFO WORD2
1E0	[15:0]	X	R/W	STAGE7_FF_WORD3	STAGE7 Fast FIFO WORD3
1E1	[15:0]	X	R/W	STAGE7_FF_WORD4	STAGE7 Fast FIFO WORD4
1E2	[15:0]	X	R/W	STAGE7_FF_WORD5	STAGE7 Fast FIFO WORD5
1E3	[15:0]	X	R/W	STAGE7_FF_WORD6	STAGE7 Fast FIFO WORD6
1E4	[15:0]	X	R/W	STAGE7_FF_WORD7	STAGE7 Fast FIFO WORD7
1E5	[15:0]	X	R/W	STAGE7_SF_WORD0	STAGE7 Slow FIFO WORD0
1E6	[15:0]	X	R/W	STAGE7_SF_WORD1	STAGE7 Slow FIFO WORD1
1E7	[15:0]	X	R/W	STAGE7_SF_WORD2	STAGE7 Slow FIFO WORD2
1E8	[15:0]	X	R/W	STAGE7_SF_WORD3	STAGE7 Slow FIFO WORD3
1E9	[15:0]	X	R/W	STAGE7_SF_WORD4	STAGE7 Slow FIFO WORD4
1EA	[15:0]	X	R/W	STAGE7_SF_WORD5	STAGE7 Slow FIFO WORD5
1EB	[15:0]	X	R/W	STAGE7_SF_WORD6	STAGE7 Slow FIFO WORD6
1EC	[15:0]	X	R/W	STAGE7_SF_WORD7	STAGE7 Slow FIFO WORD7
1ED	[15:0]	X	R/W	STAGE7_SF_AMBIENT	STAGE7 Slow FIFO Ambient Value
1EE	[15:0]	X	R/W	STAGE7_FF_AVG	STAGE7 Fast FIFO Average Value
1EF	[15:0]	X	R/W	STAGE7_CDC_WORD0	STAGE7 CDC FIFO WORD0
1F0	[15:0]	X	R/W	STAGE7_CDC_WORD1	STAGE7 CDC FIFO WORD1
1F1	[15:0]	X	R/W	STAGE7_MAX_WORD0	STAGE7 Maximum Value FIFO WORD0
1F2	[15:0]	X	R/W	STAGE7_MAX_WORD1	STAGE7 Maximum Value FIFO WORD1
1F3	[15:0]	X	R/W	STAGE7_MAX_WORD2	STAGE7 Maximum Value FIFO WORD2
1F4	[15:0]	X	R/W	STAGE7_MAX_WORD3	STAGE7 Maximum Value FIFO WORD3
1F5	[15:0]	X	R/W	STAGE7_MAX_AVG	STAGE7 Average Maximum FIFO Value
1F6	[15:0]	X	R/W	STAGE7_HIGH_THRESHOLD	STAGE7 High Threshold Value
1F7	[15:0]	X	R/W	STAGE7_MAX_TEMP	STAGE7 Temporary Maximum Value
1F8	[15:0]	X	R/W	STAGE7_MIN_WORD0	STAGE7 Minimum Value FIFO WORD0
1F9	[15:0]	X	R/W	STAGE7_MIN_WORD1	STAGE7 Minimum Value FIFO WORD1
1FA	[15:0]	X	R/W	STAGE7_MIN_WORD2	STAGE7 Minimum Value FIFO WORD2
1FB	[15:0]	X	R/W	STAGE7_MIN_WORD3	STAGE7 Minimum Value FIFO WORD3
1FC	[15:0]	X	R/W	STAGE7_MIN_AVG	STAGE7 Average Minimum FIFO Value
1FD	[15:0]	X	R/W	STAGE7_LOW_THRESHOLD	STAGE7 Low Threshold Value
1FE	[15:0]	X	R/W	STAGE7_MIN_TEMP	STAGE7 Temporary Minimum Value
1FF	[15:0]	X	R/W	Unused	

Table 49. STAGE8 Results Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
200	[15:0]	X	R/W	STAGE8_CONV_DATA	STAGE8 CDC 16-Bit Conversion Data (Copy of data in STAGE8_CONV_DATA register)
201	[15:0]	X	R/W	STAGE8_FF_WORD0	STAGE8 Fast FIFO WORD0
202	[15:0]	X	R/W	STAGE8_FF_WORD1	STAGE8 Fast FIFO WORD1
203	[15:0]	X	R/W	STAGE8_FF_WORD2	STAGE8 Fast FIFO WORD2
204	[15:0]	X	R/W	STAGE8_FF_WORD3	STAGE8 Fast FIFO WORD3
205	[15:0]	X	R/W	STAGE8_FF_WORD4	STAGE8 Fast FIFO WORD4
206	[15:0]	X	R/W	STAGE8_FF_WORD5	STAGE8 Fast FIFO WORD5
207	[15:0]	X	R/W	STAGE8_FF_WORD6	STAGE8 Fast FIFO WORD6
208	[15:0]	X	R/W	STAGE8_FF_WORD7	STAGE8 Fast FIFO WORD7
209	[15:0]	X	R/W	STAGE8_SF_WORD0	STAGE8 Slow FIFO WORD0
20A	[15:0]	X	R/W	STAGE8_SF_WORD1	STAGE8 Slow FIFO WORD1
20B	[15:0]	X	R/W	STAGE8_SF_WORD2	STAGE8 Slow FIFO WORD2
20C	[15:0]	X	R/W	STAGE8_SF_WORD3	STAGE8 Slow FIFO WORD3
20D	[15:0]	X	R/W	STAGE8_SF_WORD4	STAGE8 Slow FIFO WORD4
20E	[15:0]	X	R/W	STAGE8_SF_WORD5	STAGE8 Slow FIFO WORD5
20F	[15:0]	X	R/W	STAGE8_SF_WORD6	STAGE8 Slow FIFO WORD6
210	[15:0]	X	R/W	STAGE8_SF_WORD7	STAGE8 Slow FIFO WORD7
211	[15:0]	X	R/W	STAGE8_SF_AMBIENT	STAGE8 Slow FIFO Ambient Value
212	[15:0]	X	R/W	STAGE8_FF_AVG	STAGE8 Fast FIFO Average Value
213	[15:0]	X	R/W	STAGE8_CDC_WORD0	STAGE8 CDC FIFO WORD0
214	[15:0]	X	R/W	STAGE8_CDC_WORD1	STAGE8 CDC FIFO WORD1
215	[15:0]	X	R/W	STAGE8_MAX_WORD0	STAGE8 Maximum Value FIFO WORD0
216	[15:0]	X	R/W	STAGE8_MAX_WORD1	STAGE8 Maximum Value FIFO WORD1
217	[15:0]	X	R/W	STAGE8_MAX_WORD2	STAGE8 Maximum Value FIFO WORD2
218	[15:0]	X	R/W	STAGE8_MAX_WORD3	STAGE8 Maximum Value FIFO WORD3
219	[15:0]	X	R/W	STAGE8_MAX_AVG	STAGE8 Average Maximum FIFO Value
21A	[15:0]	X	R/W	STAGE8_HIGH_THRESHOLD	STAGE8 High Threshold Value
21B	[15:0]	X	R/W	STAGE8_MAX_TEMP	STAGE8 Temporary Maximum Value
21C	[15:0]	X	R/W	STAGE8_MIN_WORD0	STAGE8 Minimum Value FIFO WORD0
21D	[15:0]	X	R/W	STAGE8_MIN_WORD1	STAGE8 Minimum Value FIFO WORD1
21E	[15:0]	X	R/W	STAGE8_MIN_WORD2	STAGE8 Minimum Value FIFO WORD2
21F	[15:0]	X	R/W	STAGE8_MIN_WORD3	STAGE8 Minimum Value FIFO WORD3
220	[15:0]	X	R/W	STAGE8_MIN_AVG	STAGE8 Average Minimum FIFO Value
221	[15:0]	X	R/W	STAGE8_LOW_THRESHOLD	STAGE8 Low Threshold Value
222	[15:0]	X	R/W	STAGE8_MIN_TEMP	STAGE7 Temporary Minimum Value
223	[15:0]	X	R/W	Unused	

Table 50. STAGE9 Results Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
224	[15:0]	X	R/W	STAGE9_CONV_DATA	STAGE9 CDC 16-Bit Conversion Data (Copy of data in STAGE9_CONV_DATA register)
225	[15:0]	X	R/W	STAGE9_FF_WORD0	STAGE9 Fast FIFO WORD0
226	[15:0]	X	R/W	STAGE9_FF_WORD1	STAGE9 Fast FIFO WORD1
227	[15:0]	X	R/W	STAGE9_FF_WORD2	STAGE9 Fast FIFO WORD2
228	[15:0]	X	R/W	STAGE9_FF_WORD3	STAGE9 Fast FIFO WORD3
229	[15:0]	X	R/W	STAGE9_FF_WORD4	STAGE9 Fast FIFO WORD4
22A	[15:0]	X	R/W	STAGE9_FF_WORD5	STAGE9 Fast FIFO WORD5
22B	[15:0]	X	R/W	STAGE9_FF_WORD6	STAGE9 Fast FIFO WORD6
22C	[15:0]	X	R/W	STAGE9_FF_WORD7	STAGE9 Fast FIFO WORD7
22D	[15:0]	X	R/W	STAGE9_SF_WORD0	STAGE9 Slow FIFO WORD0
22E	[15:0]	X	R/W	STAGE9_SF_WORD1	STAGE9 Slow FIFO WORD1
22F	[15:0]	X	R/W	STAGE9_SF_WORD2	STAGE9 Slow FIFO WORD2
230	[15:0]	X	R/W	STAGE9_SF_WORD3	STAGE9 Slow FIFO WORD3
231	[15:0]	X	R/W	STAGE9_SF_WORD4	STAGE9 Slow FIFO WORD4
232	[15:0]	X	R/W	STAGE9_SF_WORD5	STAGE9 Slow FIFO WORD5
233	[15:0]	X	R/W	STAGE9_SF_WORD6	STAGE9 Slow FIFO WORD6
234	[15:0]	X	R/W	STAGE9_SF_WORD7	STAGE9 Slow FIFO WORD7
235	[15:0]	X	R/W	STAGE9_SF_AMBIENT	STAGE9 Slow FIFO Ambient Value
236	[15:0]	X	R/W	STAGE9_FF_AVG	STAGE9 Fast FIFO Average Value
237	[15:0]	X	R/W	STAGE9_CDC_WORD0	STAGE9 CDC FIFO WORD0
238	[15:0]	X	R/W	STAGE9_CDC_WORD1	STAGE9 CDC FIFO WORD1
239	[15:0]	X	R/W	STAGE9_MAX_WORD0	STAGE9 Maximum Value FIFO WORD0
23A	[15:0]	X	R/W	STAGE9_MAX_WORD1	STAGE9 Maximum Value FIFO WORD1
23B	[15:0]	X	R/W	STAGE9_MAX_WORD2	STAGE9 Maximum Value FIFO WORD2
23C	[15:0]	X	R/W	STAGE9_MAX_WORD3	STAGE9 Maximum Value FIFO WORD3
23D	[15:0]	X	R/W	STAGE9_MAX_AVG	STAGE9 Average Maximum FIFO Value
23E	[15:0]	X	R/W	STAGE9_HIGH_THRESHOLD	STAGE9 High Threshold Value
23F	[15:0]	X	R/W	STAGE9_MAX_TEMP	STAGE9 Temporary Maximum Value
240	[15:0]	X	R/W	STAGE9_MIN_WORD0	STAGE9 Minimum Value FIFO WORD0
241	[15:0]	X	R/W	STAGE9_MIN_WORD1	STAGE9 Minimum Value FIFO WORD1
242	[15:0]	X	R/W	STAGE9_MIN_WORD2	STAGE9 Minimum Value FIFO WORD2
243	[15:0]	X	R/W	STAGE9_MIN_WORD3	STAGE9 Minimum Value FIFO WORD3
244	[15:0]	X	R/W	STAGE9_MIN_AVG	STAGE9 Average Minimum FIFO Value
245	[15:0]	X	R/W	STAGE9_LOW_THRESHOLD	STAGE9 Low Threshold Value
246	[15:0]	X	R/W	STAGE9_MIN_TEMP	STAGE9 Temporary Minimum Value
247	[15:0]	X	R/W	Unused	

Table 51. STAGE10 Results Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
248	[15:0]	X	R/W	STAGE10_CONV_DATA	STAGE10 CDC 16-Bit Conversion Data (Copy of data in STAGE10_CONV_DATA register)
249	[15:0]	X	R/W	STAGE10_FF_WORD0	STAGE10 Fast FIFO WORD0
24A	[15:0]	X	R/W	STAGE10_FF_WORD1	STAGE10 Fast FIFO WORD1
24B	[15:0]	X	R/W	STAGE10_FF_WORD2	STAGE10 Fast FIFO WORD2
24C	[15:0]	X	R/W	STAGE10_FF_WORD3	STAGE10 Fast FIFO WORD3
24D	[15:0]	X	R/W	STAGE10_FF_WORD4	STAGE10 Fast FIFO WORD4
24E	[15:0]	X	R/W	STAGE10_FF_WORD5	STAGE10 Fast FIFO WORD5
24F	[15:0]	X	R/W	STAGE10_FF_WORD6	STAGE10 Fast FIFO WORD6
250	[15:0]	X	R/W	STAGE10_FF_WORD7	STAGE10 Fast FIFO WORD7
251	[15:0]	X	R/W	STAGE10_SF_WORD0	STAGE10 Slow FIFO WORD0
252	[15:0]	X	R/W	STAGE10_SF_WORD1	STAGE10 Slow FIFO WORD1
253	[15:0]	X	R/W	STAGE10_SF_WORD2	STAGE10 Slow FIFO WORD2
254	[15:0]	X	R/W	STAGE10_SF_WORD3	STAGE10 Slow FIFO WORD3
255	[15:0]	X	R/W	STAGE10_SF_WORD4	STAGE10 Slow FIFO WORD4
256	[15:0]	X	R/W	STAGE10_SF_WORD5	STAGE10 Slow FIFO WORD5
257	[15:0]	X	R/W	STAGE10_SF_WORD6	STAGE10 Slow FIFO WORD6
258	[15:0]	X	R/W	STAGE10_SF_WORD7	STAGE10 Slow FIFO WORD7
259	[15:0]	X	R/W	STAGE10_SF_AMBIENT	STAGE10 Slow FIFO Ambient Value
25A	[15:0]	X	R/W	STAGE10_FF_AVG	STAGE10 Fast FIFO Average Value
25B	[15:0]	X	R/W	STAGE10_CDC_WORD0	STAGE10 CDC FIFO WORD0
25C	[15:0]	X	R/W	STAGE10_CDC_WORD1	STAGE10 CDC FIFO WORD1
25D	[15:0]	X	R/W	STAGE10_MAX_WORD0	STAGE10 Maximum Value FIFO WORD0
25E	[15:0]	X	R/W	STAGE10_MAX_WORD1	STAGE10 Maximum Value FIFO WORD1
25F	[15:0]	X	R/W	STAGE10_MAX_WORD2	STAGE10 Maximum Value FIFO WORD2
260	[15:0]	X	R/W	STAGE10_MAX_WORD3	STAGE10 Maximum Value FIFO WORD3
261	[15:0]	X	R/W	STAGE10_MAX_AVG	STAGE10 Average Maximum FIFO Value
262	[15:0]	X	R/W	STAGE10_HIGH_THRESHOLD	STAGE10 High Threshold Value
263	[15:0]	X	R/W	STAGE10_MAX_TEMP	STAGE10 Temporary Maximum Value
264	[15:0]	X	R/W	STAGE10_MIN_WORD0	STAGE10 Minimum Value FIFO WORD0
265	[15:0]	X	R/W	STAGE10_MIN_WORD1	STAGE10 Minimum Value FIFO WORD1
266	[15:0]	X	R/W	STAGE10_MIN_WORD2	STAGE10 Minimum Value FIFO WORD2
267	[15:0]	X	R/W	STAGE10_MIN_WORD3	STAGE10 Minimum Value FIFO WORD3
268	[15:0]	X	R/W	STAGE10_MIN_AVG	STAGE10 Average Minimum FIFO Value
269	[15:0]	X	R/W	STAGE10_LOW_THRESHOLD	STAGE10 Low Threshold Value
26A	[15:0]	X	R/W	STAGE10_MIN_TEMP	STAGE10 Temporary Minimum Value
26B	[15:0]	X	R/W	Unused	

Table 52. STAGE11 Results Register Map

Address	Data Bit Content	Default Value	Type	Name	Description
26C	[15:0]	X	R/W	STAGE11_CONV_DATA	STAGE11 CDC 16-Bit Conversion Data (Copy of data in STAGE11_CONV_DATA register)
26D	[15:0]	X	R/W	STAGE11_FF_WORD0	STAGE11 Fast FIFO WORD0
26E	[15:0]	X	R/W	STAGE11_FF_WORD1	STAGE11 Fast FIFO WORD1
26F	[15:0]	X	R/W	STAGE11_FF_WORD2	STAGE11 Fast FIFO WORD2
270	[15:0]	X	R/W	STAGE11_FF_WORD3	STAGE11 Fast FIFO WORD3
271	[15:0]	X	R/W	STAGE11_FF_WORD4	STAGE11 Fast FIFO WORD4
272	[15:0]	X	R/W	STAGE11_FF_WORD5	STAGE11 Fast FIFO WORD5
273	[15:0]	X	R/W	STAGE11_FF_WORD6	STAGE11 Fast FIFO WORD6
274	[15:0]	X	R/W	STAGE11_FF_WORD7	STAGE11 Fast FIFO WORD7
275	[15:0]	X	R/W	STAGE11_SF_WORD0	STAGE11 Slow FIFO WORD0
276	[15:0]	X	R/W	STAGE11_SF_WORD1	STAGE11 Slow FIFO WORD1
277	[15:0]	X	R/W	STAGE11_SF_WORD2	STAGE11 Slow FIFO WORD2
278	[15:0]	X	R/W	STAGE11_SF_WORD3	STAGE11 Slow FIFO WORD3
279	[15:0]	X	R/W	STAGE11_SF_WORD4	STAGE11 Slow FIFO WORD4
27A	[15:0]	X	R/W	STAGE11_SF_WORD5	STAGE11 Slow FIFO WORD5
27B	[15:0]	X	R/W	STAGE11_SF_WORD6	STAGE11 Slow FIFO WORD6
27C	[15:0]	X	R/W	STAGE11_SF_WORD7	STAGE11 Slow FIFO WORD7
27D	[15:0]	X	R/W	STAGE11_SF_AMBIENT	STAGE11 Slow FIFO Ambient Value
27E	[15:0]	X	R/W	STAGE11_FF_AVG	STAGE11 Fast FIFO Average Value
27F	[15:0]	X	R/W	STAGE11_CDC_WORD0	STAGE11 CDC FIFO WORD0
280	[15:0]	X	R/W	STAGE11_CDC_WORD1	STAGE11 CDC FIFO WORD1
281	[15:0]	X	R/W	STAGE11_MAX_WORD0	STAGE11 Maximum Value FIFO WORD0
282	[15:0]	X	R/W	STAGE11_MAX_WORD1	STAGE11 Maximum Value FIFO WORD1
283	[15:0]	X	R/W	STAGE11_MAX_WORD2	STAGE11 Maximum Value FIFO WORD2
284	[15:0]	X	R/W	STAGE11_MAX_WORD3	STAGE11 Maximum Value FIFO WORD3
285	[15:0]	X	R/W	STAGE11_MAX_AVG	STAGE11 Average Maximum FIFO Value
286	[15:0]	X	R/W	STAGE11_HIGH_THRESHOLD	STAGE11 High Threshold Value
287	[15:0]	X	R/W	STAGE11_MAX_TEMP	STAGE11 Temporary Maximum Value
288	[15:0]	X	R/W	STAGE11_MIN_WORD0	STAGE11 Minimum Value FIFO WORD0
289	[15:0]	X	R/W	STAGE11_MIN_WORD1	STAGE11 Minimum Value FIFO WORD1
28A	[15:0]	X	R/W	STAGE11_MIN_WORD2	STAGE11 Minimum Value FIFO WORD2
28B	[15:0]	X	R/W	STAGE11_MIN_WORD3	STAGE11 Minimum Value FIFO WORD3
28C	[15:0]	X	R/W	STAGE11_MIN_AVG	STAGE11 Average Minimum FIFO Value
28D	[15:0]	X	R/W	STAGE11_LOW_THRESHOLD	STAGE11 Low Threshold Value
28E	[15:0]	X	R/W	STAGE11_MIN_TEMP	STAGE11 Temporary Minimum Value
28F	[15:0]	X	R/W	Unused	

Table 53. STAGEX Detailed CIN (0:6) Connection Setup Description (X = 0 to 11)

Data Bit Content	Default Value	Type	Name	Description
[1:0]	X	R/W	CIN0_CONNECTION_SETUP	CIN0 Connection Setup 00 = CIN0 not connected to CDC inputs 01 = CIN0 connected to CDC negative input 10 = CIN0 connected to CDC positive input 11 = CIN0 connected to BIAS (connect unused CIN inputs)
[3:2]	X	R/W	CIN1_CONNECTION_SETUP	CIN1 Connection Setup 00 = CIN1 not connected to CDC inputs 01 = CIN1 connected to CDC negative input 10 = CIN1 connected to CDC positive input 11 = CIN1 connected to BIAS (connect unused CIN inputs)
[5:4]	X	R/W	CIN2_CONNECTION_SETUP	CIN2 Connection Setup 00 = CIN2 not connected to CDC inputs 01 = CIN2 connected to CDC negative input 10 = CIN2 connected to CDC positive input 11 = CIN2 connected to BIAS (connect unused CIN inputs)
[7:6]	X	R/W	CIN3_CONNECTION_SETUP	CIN3 Connection Setup 00 = CIN3 not connected to CDC inputs 01 = CIN3 connected to CDC negative input 10 = CIN3 connected to CDC positive input 11 = CIN3 connected to BIAS (connect unused CIN inputs)
[9:8]	X	R/W	CIN4_CONNECTION_SETUP	CIN4 Connection Set-Up 00 = CIN4 not connected to CDC inputs 01 = CIN4 connected to CDC negative input 10 = CIN4 connected to CDC positive input 11 = CIN4 connected to BIAS (connect unused CIN inputs)
[11:10]	X	R/W	CIN5_CONNECTION_SETUP	CIN5 Connection Setup 00 = CIN5 not connected to CDC inputs 01 = CIN5 connected to CDC negative input 10 = CIN5 connected to CDC positive input 11 = CIN5 connected to BIAS (connect unused CIN inputs)
[13:12]	X	R/W	CIN6_CONNECTION_SETUP	CIN6 Connection Setup 00 = CIN6 not connected to CDC inputs 01 = CIN6 connected to CDC negative input 10 = CIN6 connected to CDC positive input 11 = CIN6 connected to BIAS (connect unused CIN inputs)
[15:14]	X		Unused	

Table 54. STAGEX Detailed CIN (7:13) Connection Setup Description (X = 0 to 11)

Data Bit Content	Default Value	Type	Name	Description
[1:0]	X	R/W	CIN7_CONNECTION_SETUP	CIN7 Connection Setup 00 = CIN7 not connected to CDC inputs 01 = CIN7 connected to CDC negative input 10 = CIN7 connected to CDC positive input 11 = CIN7 connected to BIAS (connect unused CIN inputs)
[3:2]	X	R/W	CIN8_CONNECTION_SETUP	CIN8 Connection Setup 00 = CIN8 not connected to CDC inputs 01 = CIN8 connected to CDC negative input 10 = CIN8 connected to CDC positive input 11 = CIN8 connected to BIAS (connect unused CIN inputs)
[5:4]	X	R/W	CIN9_CONNECTION_SETUP	CIN9 Connection Set-Up 00 = CIN9 not connected to CDC inputs 01 = CIN9 connected to CDC negative input 10 = CIN9 connected to CDC positive input 11 = CIN9 connected to BIAS (connect unused CIN inputs)
[7:6]	X	R/W	CIN10_CONNECTION_SETUP	CIN10 Connection Setup 00 = CIN10 not connected to CDC inputs 01 = CIN10 connected to CDC negative input 10 = CIN10 connected to CDC positive input 11 = CIN10 connected to BIAS (connect unused CIN inputs)
[9:8]	X	R/W	CIN11_CONNECTION_SETUP	CIN11 Connection Setup 00 = CIN11 not connected to CDC inputs 01 = CIN11 connected to CDC negative input 10 = CIN11 connected to CDC positive input 11 = CIN11 connected to BIAS (connect unused CIN inputs)
[11:10]	X	R/W	CIN12_CONNECTION_SETUP	CIN12 Connection Setup 00 = CIN12 not connected to CDC inputs 01 = CIN12 connected to CDC negative input 10 = CIN12 connected to CDC positive input 11 = CIN12 connected to BIAS (connect unused CIN inputs)
[13:12]	X	R/W	CIN13_CONNECTION_SETUP	CIN13 Connection Setup 00 = CIN13 not connected to CDC inputs 01 = CIN13 connected to CDC negative input 10 = CIN13 connected to CDC positive input 11 = CIN13 connected to BIAS (connect unused CIN inputs)
[14]	X		NEG_AFE_OFFSET_DISABLE	Negative AFE Offset Enable Control 0 = enable 1 = disable
[15]	X		POS_AFE_OFFSET_DISABLE	Positive AFE offset Enable Control 0 = enable 1 = disable

Table 55. STAGEX Detailed Offset Control Description (X = 0 to 11)

Data Bit Content	Default Value	Type	Name	Description
[6:0]	X	R/W	NEG_AFE_OFFSET	Negative AFE Offset Setting (20 pF Range) 1 LSB value = 0.16 pF of offset
[7]	X	R/W	NEG_AFE_OFFSET_SWAP	Negative AFE Offset Swap Control 0 = NEG_AFE_OFFSET applied to CDC negative input 1 = NEG_AFE_OFFSET applied to CDC positive input
[14:8]	X	R/W	POS_AFE_OFFSET	Positive AFE Offset Setting (20 pF Range) 1 LSB value = 0.16 pF of offset
[15]	X	R/W	POS_AFE_OFFSET_SWAP	Positive AFE Offset Swap Control 0 = POS_AFE_OFFSET applied to CDC positive input 1 = POS_AFE_OFFSET applied to CDC negative input

Table 56. STAGEX Detailed Sensitivity Control Description (X = 0 to 11)

Data Bit Content	Default Value	Type	Name	Description
[3:0]	X	R/W	NEG_THRESHOLD_SENSITIVITY	Negative Threshold Sensitivity Control 0000 = 25%, 0001 = 29.73%, 0010 = 34.40%, 0011 = 39.08% 0100 = 43.79%, 0101 = 48.47%, 0110 = 53.15% 0111 = 57.83%, 1000 = 62.51%, 1001 = 67.22% 1010 = 71.90%, 1011 = 76.58%, 1100 = 81.28% 1101 = 85.96%, 1110 = 90.64%, 1111 = 95.32%
[6:4]	X	R/W	NEG_PEAK_DETECT	Negative Peak Detect Setting 000 = 40% level, 001 = 50% level, 010 = 60% level 011 = 70% level, 100 = 80% Level, 101 = 90% level
[7]	X	R/W	Unused	
[11:8]	X	R/W	POS_THRESHOLD_SENSITIVITY	Positive Threshold Sensitivity Control 0000 = 25%, 0001 = 29.73%, 0010 = 34.40%, 0011 = 39.08% 0100 = 43.79%, 0101 = 48.47%, 0110 = 53.15% 0111 = 57.83%, 1000 = 62.51%, 1001 = 67.22% 1010 = 71.90%, 1011 = 76.58%, 1100 = 81.28% 1101 = 85.96%, 1110 = 90.64%, 1111 = 95.32%
[14:12]	X	R/W	POS_PEAK_DETECT	Positive Peak Detect Setting 000 = 40% level, 001 = 50% level, 010 = 60% level 011 = 70% level, 100 = 80% level, 101 = 90% level
[15]	X	R/W	Unused	

OUTLINE DIMENSIONS

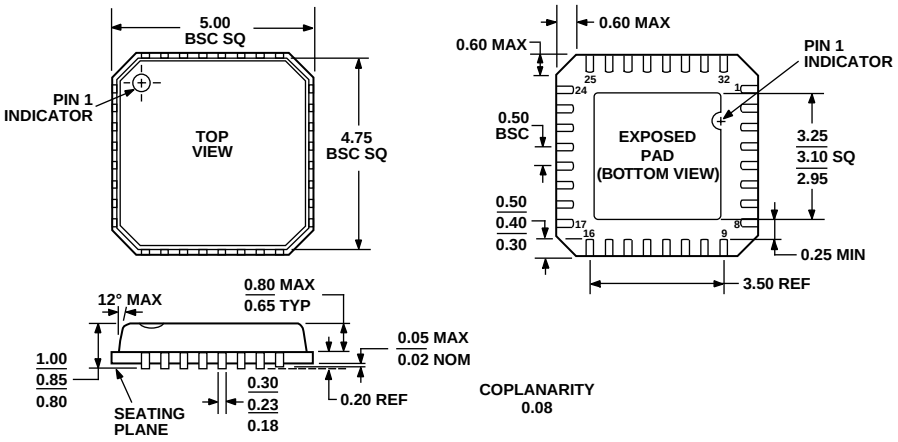


Figure 48. 32-Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Very Thin Quad
(CP-32-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Serial Interface Description	Package Description	Package Option
AD7142ACPZ-REEL[1]	–40°C to +85°C	SPI Interface	32-Lead LFCSP	CP-32-3
AD7142ACPZ-REEL7[1]	–40°C to +85°C	SPI Interface	32-Lead LFCSP	CP-32-3
AD7142-1ACPZ-REEL[1]	–40°C to +85°C	I²C Interface	32-Lead LFCSP	CP-32-3
AD7142-1ACPZ-REEL7[1]	–40°C to +85°C	I²C Interface	32-Lead LFCSP	CP-32-3
Eval-AD7142EB	0°C to +85°C	SPI Interface	Evaluation Board	
Eval-AD7142EB-1	0°C to +85°C	I²C Interface	Evaluation Board	

[1] Z = Pb-free part.

NOTES

NOTES

PR05702-0-12/05(PrD)