40-Channel, 14-Bit, Parallel and Serial Input, Bipolar Voltage-Output DAC

AD5379

FEATURES

- 40-channel DAC in 13 mm × 13 mm 108-lead CSPBGA
- Guaranteed monotonic to 14 bits
- Buffered voltage outputs
  - Output voltage span of 3.5 V × V_{REF}(+)
  - Maximum output voltage span of 17.5 V
- System calibration function allowing user-programmable offset and gain
- Pseudo differential outputs relative to REFGND
- Clear function to user-defined REFGND ($\overline{CLR}$ pin)
- Simultaneous update of DAC outputs ($\overline{LDAC}$ pin)
- DAC increment/decrement mode
- Channel grouping and addressing features
- Interface options:
  - Parallel interface
  - DSP/microcontroller-compatible 3-wire serial interface
- 2.5 V to 5.5 V JEDEC-compliant digital levels
- SDO daisy-chaining option
- Power-on reset
- Digital reset ($\overline{RESET}$ pin and soft reset function)

APPLICATIONS

- Level setting in automatic test equipment (ATE)
- Variable optical attenuators (VOA)
- Optical switches
- Industrial control systems

FUNCTIONAL BLOCK DIAGRAM

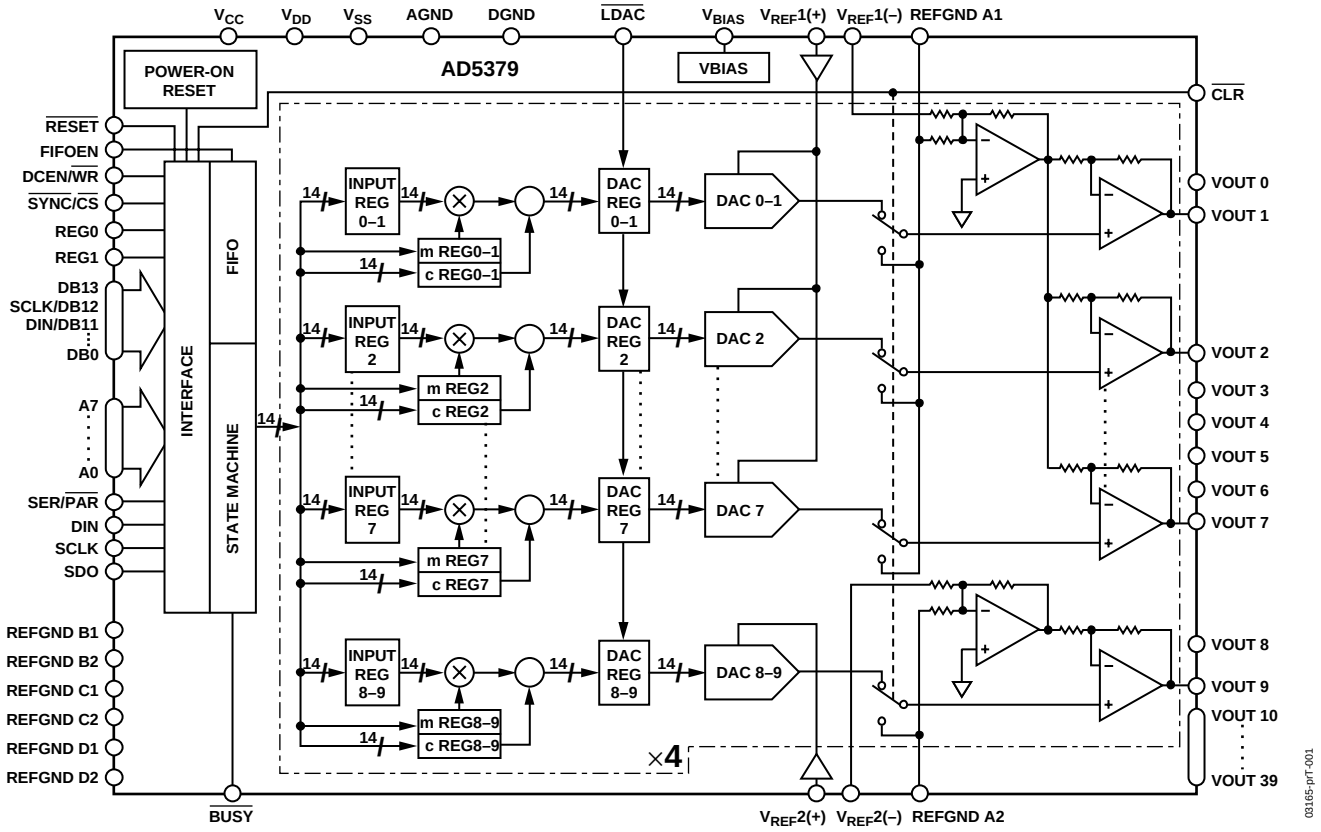

Figure 1.

AD5379—Protected by U.S. Patent No. 5,969,657; other patents pending.

Rev. 0

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REVISION HISTORY

Revision 0: Initial Version

GENERAL DESCRIPTION

The AD5379 contains 40, 14-bit DACs in one CSPBGA package. The AD5379 provides a bipolar output range determined by the voltages applied to the $V_{REF}(+)$ and $V_{REF}(-)$ inputs. The maximum output voltage span is 17.5 V, corresponding to a bipolar output range of −8.75 V to +8.75 V, and is achieved with reference voltages of $V_{REF}(-) = -3.5$ V and $V_{REF}(+) = +5$ V.

The AD5379 offers guaranteed operation over a wide V_{SS}/V_{DD} supply range from ±11.4 V to ±16.5 V. The output amplifier headroom requirement is 2.5 V operating with a load current of 1.5 mA and 2 V operating with a load current of 0.5 mA.

The AD5379 contains a double-buffered parallel interface in which 14 data bits are loaded into one of the input registers under the control of the $\overline{WR}$, $\overline{CS}$, and DAC channel address pins, A0 to A7. It also has a 3-wire serial interface, which is compatible with SPI®, QSPI™, MICROWIRE™, and DSP interface standards and can handle clock speeds of up to 50 MHz.

The DAC outputs are updated on reception of new data into the DAC registers. All the outputs can be updated simultaneously by taking the $\overline{LDAC}$ input low. Each channel has a programmable gain and an offset adjust register.

Each DAC output is gained and buffered on-chip with respect to an external REFGND input. The DAC outputs can also be switched to REFGND via the $\overline{CLR}$ pin.

Table 1. High Channel Count, Low Voltage Single-Supply DACs

Model	Resolution	AV_{DD} Range	Output Channels	Linearity Error (LSB)	Package Description	Package Option
AD5380BST-5	14 Bits	4.5 V to 5.5 V	40	±4	100-Lead LQFP	ST-100
AD5380BST-3	14 Bits	2.7 V to 3.6 V	40	±4	100-Lead LQFP	ST-100
AD5381BST-5	12 Bits	4.5 V to 5.5 V	40	±1	100-Lead LQFP	ST-100
AD5381BST-3	12 Bits	2.7 V to 3.6 V	40	±1	100-Lead LQFP	ST-100
AD5384BBC-5	14 Bits	4.5 V to 5.5 V	40	±4	100-Lead CSPBGA	BC-100
AD5384BBC-3	14 Bits	2.7 V to 3.6 V	40	±4	100-Lead CSPBGA	BC-100
AD5382BST-5	14 Bits	4.5 V to 5.5 V	32	±4	100-Lead LQFP	ST-100
AD5382BST-3	14 Bits	2.7 V to 3.6 V	32	±4	100-Lead LQFP	ST-100
AD5383BST-5	12 Bits	4.5 V to 5.5 V	32	±1	100-Lead LQFP	ST-100
AD5383BST-3	12 Bits	2.7 V to 3.6 V	32	±1	100-Lead LQFP	ST-100
AD5390BST-5	14 Bits	4.5 V to 5.5 V	16	±3	52-Lead LQFP	ST-52
AD5390BCP-5	14 Bits	4.5 V to 5.5 V	16	±3	64-Lead LFCSP	CP-64
AD5390BST-3	14 Bits	2.7 V to 3.6 V	16	±3	52-Lead LQFP	ST-52
AD5390BCP-3	14 Bits	2.7 V to 3.6 V	16	±3	64-Lead LFCSP	CP-64
AD5391BST-5	12 Bits	4.5 V to 5.5 V	16	±1	52-Lead LQFP	ST-52
AD5391BCP-5	12 Bits	4.5 V to 5.5 V	16	±1	64-Lead LFCSP	CP-64
AD5391BST-3	12 Bits	2.7 V to 3.6 V	16	±1	52-Lead LQFP	ST-52
AD5391BCP-3	12 Bits	2.7 V to 3.6 V	16	±1	64-Lead LFCSP	CP-64
AD5392BST-5	14 Bits	4.5 V to 5.5 V	8	±3	52-Lead LQFP	ST-52
AD5392BCP-5	14 Bits	4.5 V to 5.5 V	8	±3	64-Lead LFCSP	CP-64
AD5392BST-3	14 Bits	2.7 V to 3.6 V	8	±3	52-Lead LQFP	ST-52
AD5392BCP-3	14 Bits	2.7 V to 3.6 V	8	±3	64-Lead LFCSP	CP-64

SPECIFICATIONS

V_{CC} = 2.7 V to 5.5 V; V_{DD} = 11.4 V to 16.5 V; V_{SS} = −11.4 V to −16.5 V; V_{REF}(+) = 5 V; V_{REF}(−) = −3.5 V; AGND = DGND = REFGND = 0 V; V_{BIAS} = 5 V; C_L = 200 pF to GND; R_L = 11 kΩ to 3 V; gain = 1; offset = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	A Version[1]	Unit	Test Conditions/Comments[2]
ACCURACY			
Resolution	14	Bits	
Relative Accuracy	±3	LSB max	−40°C to +85°C.
	±2.5	LSB max	0°C to 70°C.
Differential Nonlinearity	−1/+1.5	LSB max	Guaranteed monotonic by design over temperature.
Zero-Scale Error	±12	mV max	−40°C to +85°C.
	±5	mV max	0°C to 70°C.
Full-Scale Error	±12	mV max	−40°C to +85°C.
	±8	mV max	0°C to 70°C.
Gain Error	±8	mV max	−40°C to +85°C.
	±1/±5	mV typ/max	0°C to 70°C.
VOUT Temperature Coefficient	5	ppm FSR/°C typ	Includes linearity, offset, and gain drift. See Figure 11.
DC Crosstalk[2]	0.5	mV max	Typically 100 µV.
REFERENCE INPUTS[2]			
V_{REF}(+) DC Input Impedance	1	MΩ min	Typically 100 MΩ.
V_{REF}(−) DC Input Impedance	8	kΩ min	Typically 12 kΩ.
V_{REF}(+) Input Current	±10	µA max	Per input. Typically ±30 nA.
V_{REF}(+) Range	1.5/5	V min/max	±2% for specified operation.
V_{REF}(−) Range	−3.5/0	V min/max	±2% for specified operation.
REFGND INPUTS[2]			
DC Input Impedance	80	kΩ min	Typically 120 kΩ.
Input Range	±0.5	V min/max	
OUTPUT CHARACTERISTICS[2]			
Output Voltage Range	V_{SS} + 2/ V_{SS} + 2.5	V min	I_{LOAD} = ±0.5 mA/ ±1.5 mA.
	V_{DD} − 2/ V_{DD} − 2.5	V max	I_{LOAD} = ±0.5 mA/ ±1.5 mA.
Short Circuit Current	15	mA max	
Load Current	±1.5	mA max	
Capacitive Load	2200	pF max	
DC Output Impedance	1	Ω max	
DIGITAL INPUTS			JEDEC compliant.
Input High Voltage	1.7	V min	V_{CC} = 2.7 V to 3.6 V.
	2.0	V min	V_{CC} = 3.6 V to 5.5 V.
Input Low Voltage	0.8	V max	V_{CC} = 2.7 V to 5.5 V.
Input Current (with pull-up/pull-down)	±8	µA max	SER/$\overline{PAR}$, FIFOEN, and $\overline{RESET}$ pins only.
Input Current (no pull-up/pull-down)	±1	µA max	All other digital input pins.
Input Capacitance[2]	10	pF max	
DIGITAL OUTPUTS ($\overline{BUSY}$, SDO)			
Output Low Voltage	0.5	V max	Sinking 200 µA.
Output High Voltage (SDO)	V_{CC} − 0.5	V min	Sourcing 200 µA.
High Impedance Leakage Current	−70	µA max	SDO only.
High Impedance Output Capacitance[2]	10	pF typ	

Parameter	A Version[1]	Unit	Test Conditions/Comments[2]
POWER REQUIREMENTS			
V_{CC}	2.7/5.5	V min/max	
V_{DD}	8.5/16.5	V min/max	
V_{SS}	−3/−16.5	V min/max	
Power Supply Sensitivity[2]			
Δ Full Scale/Δ V_{DD}	−75	dB typ	
Δ Full Scale/Δ V_{SS}	−75	dB typ	
Δ Full Scale/Δ V_{CC}	−90	dB typ	
I_{CC}	5	mA max	V_{CC} = 5.5 V, $V_{IH} = V_{CC}$, V_{IL} = GND.
I_{DD}	28	mA max	Outputs unloaded. Typically 20 mA.
I_{SS}	23	mA max	Outputs unloaded. Typically 15 mA.
Power Dissipation			
Power Dissipation Unloaded (P)	850	mW max	V_{DD} = 16.5 V, V_{SS} = −16.5 V.
Power Dissipation loaded (P_{TOTAL})	2000	mW max	$P_{TOTAL} = P + \Sigma(V_{DD} - V_O) \times I_{SOURCE} + \Sigma(V_O - V_{SS}) \times I_{SINK}$.
Junction Temperature	130	°C max	$T_J = T_A + P_{TOTAL} \times \theta_J$.[3]

[1] Temperature range for A Version: −40°C to +85°C. Typical specifications are at 25°C.
[2] Guaranteed by design and characterization, not production tested.
[3] Where θ_J represents the package thermal impedance.

AC CHARACTERISTICS

V_{CC} = 2.7 V to 5.5 V; V_{DD} = 11.4 V to 16.5 V; V_{SS} = −11.4 V to −16.5 V; $V_{REF}(+)$ = 5 V; $V_{REF}(-)$ = −3.5 V; AGND = DGND = REFGND = 0 V; V_{BIAS} = 5 V; C_L = 220 pF; R_L = 11 kΩ to 3 V; gain = 1; offset = 0 V.

Table 3.

Parameter	A Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	20	µs typ	Full-scale change to ±1/2 LSB.
	30	µs max	DAC latch contents alternately loaded with all 0s and all 1s.
Slew Rate	1	V/µs typ	
Digital-to-Analog Glitch Energy	20	nV-s typ	
Glitch Impulse Peak Amplitude	15	mV max	
Channel-to-Channel Isolation	100	dB typ	$V_{REF}(+)$ = 2 V p-p, (1 V_{BIAS}) 1 kHz, $V_{REF}(-)$ = −1 V.
DAC-to-DAC Crosstalk	40	nV-s typ	See the Terminology section. Between DACs inside a group.
	10	nV-s typ	Between DACs from different groups.
Digital Crosstalk	0.1	nV-s typ	
Digital Feedthrough	1	nV-s typ	Effect of input bus activity on DAC output under test.
Output Noise Spectral Density @ 1 kHz	350	nV/(Hz)$^{1/2}$ typ	$V_{REF}(+) = V_{REF}(-)$ = 0 V.

[1] Guaranteed by design and characterization, not production tested.

TIMING CHARACTERISTICS

SERIAL INTERFACE

V_{CC} = 2.7 V to 5.5 V; V_{DD} = 11.4 V to 16.5 V; V_{SS} = −11.4 V to −16.5 V; $V_{REF}(+)$ = 5 V; $V_{REF}(-)$ = −3.5 V; AGND = DGND = REFGND = 0 V; V_{BIAS} = 5 V, FIFOEN = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	20	ns min	SCLK Cycle Time.
t_2	8	ns min	SCLK High Time.
t_3	8	ns min	SCLK Low Time.
t_4	10	ns min	$\overline{SYNC}$ Falling Edge to SCLK Falling Edge Setup Time.
t_5[4]	15	ns min	24th SCLK Falling Edge to $\overline{SYNC}$ Falling Edge.
t_6[4]	25	ns min	Minimum $\overline{SYNC}$ Low Time.
t_7	10	ns min	Minimum $\overline{SYNC}$ High Time.
t_8	5	ns min	Data Setup Time.
t_9	4.5	ns min	Data Hold Time.
t_{10}[4, 5]	30	ns max	24th SCLK Falling Edge to $\overline{BUSY}$ Falling Edge.
t_{11}	330	ns max	$\overline{BUSY}$ Pulse Width Low (Single-Channel Update.) See Table 10.
t_{12}[4]	20	ns min	24th SCLK Falling Edge to $\overline{LDAC}$ Falling Edge.
t_{13}	20	ns min	$\overline{LDAC}$ Pulse Width Low.
t_{14}	150	ns typ	$\overline{BUSY}$ Rising Edge to DAC Output Response Time.
t_{15}	0	ns min	$\overline{BUSY}$ Rising Edge to $\overline{LDAC}$ Falling Edge.
t_{16}	100	ns min	$\overline{LDAC}$ Falling Edge to DAC Output Response Time.
t_{17}	20/30	µs typ/max	DAC Output Settling Time.
t_{18}	10	ns min	$\overline{CLR}$ Pulse Width Low.
t_{19}	350	ns max	$\overline{CLR}$/$\overline{RESET}$ Pulse Activation Time.
t_{20}[6, 7]	25	ns max	SCLK Rising Edge to SDO Valid.
t_{21}[7]	5	ns min	SCLK Falling Edge to $\overline{SYNC}$ Rising Edge.
t_{22}[7]	5	ns min	$\overline{SYNC}$ Rising Edge to SCLK Rising Edge.
t_{23}[7]	20	ns min	$\overline{SYNC}$ Rising Edge to $\overline{LDAC}$ Falling Edge.
t_{24}[5]	30	ns min	$\overline{SYNC}$ Rising Edge to $\overline{BUSY}$ Falling Edge.
t_{25}	10	ns min	$\overline{RESET}$ Pulse Width Low.
t_{26}	120	µs max	$\overline{RESET}$ Time Indicated by $\overline{BUSY}$ Low.

[1] Guaranteed by design and characterization, not production tested.
[2] All input signals are specified with $t_r = t_f$ = 2 ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.2 V.
[3] See Figure 4 and Figure 5.
[4] Standalone mode only.
[5] This is measured with the load circuit of Figure 2.
[6] This is measured with the load circuit of Figure 3.
[7] Daisy-chain mode only.

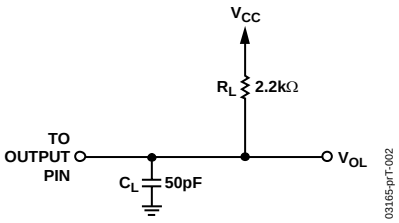


Figure 2. Load Circuit for $\overline{BUSY}$ Timing Diagram

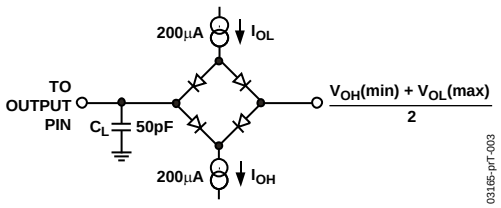


Figure 3. Load Circuit for SDO Timing Diagram (Serial Interface, Daisy-Chain Mode)

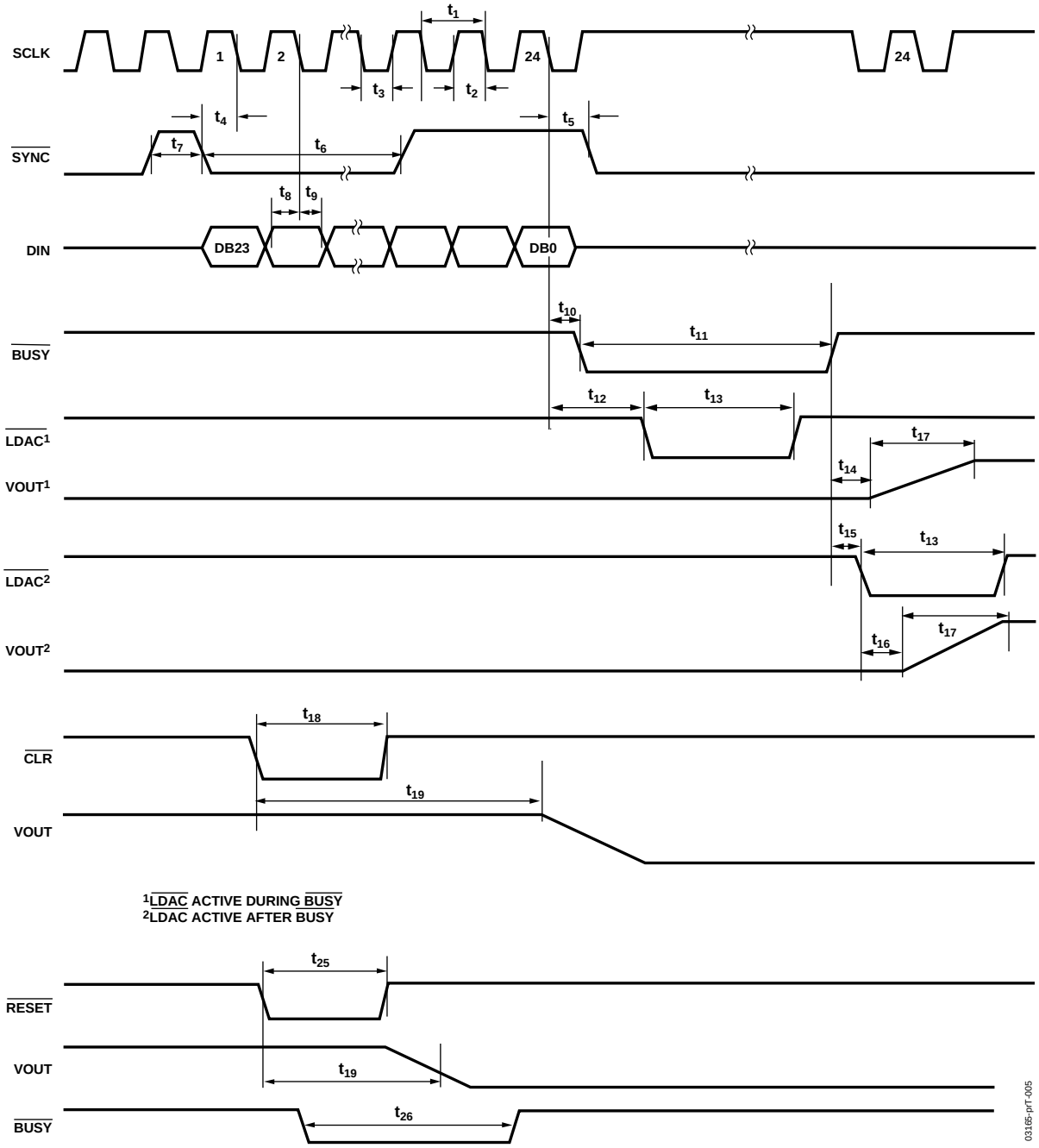


Figure 4. Serial Interface Timing Diagram (Standalone Mode)

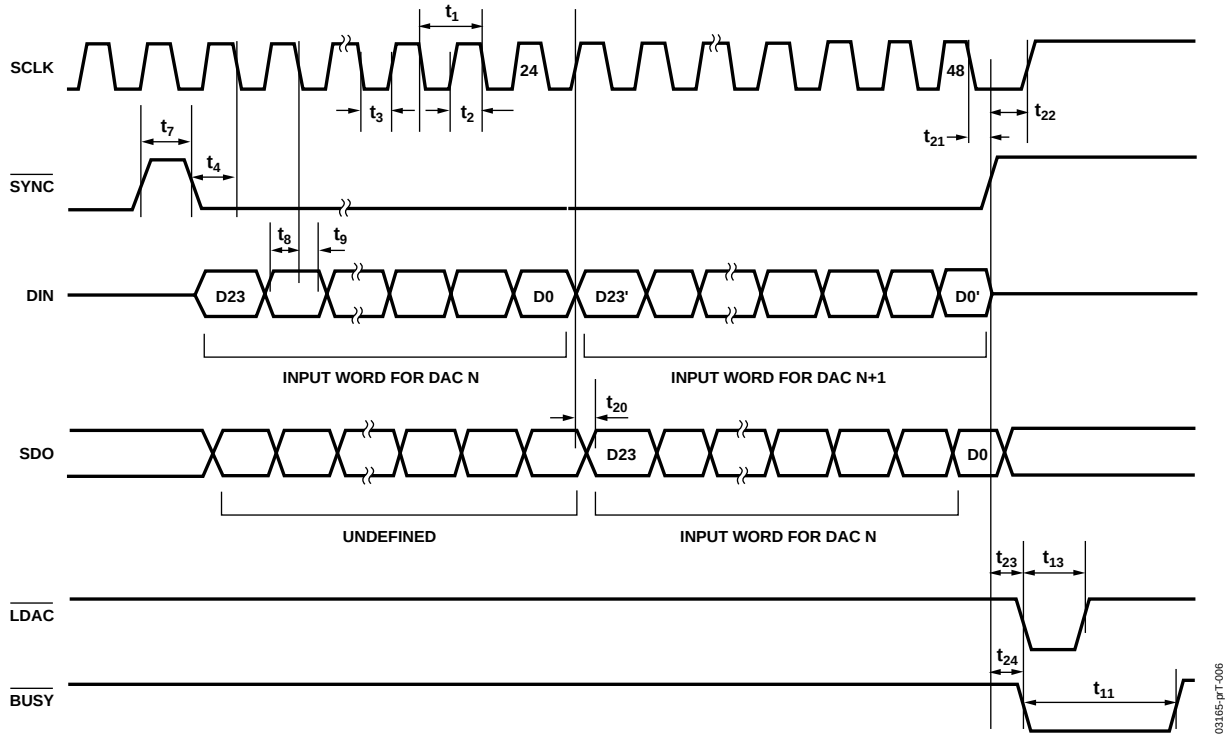


Figure 5. Serial Interface Timing Diagram (Daisy-Chain Mode)

PARALLEL INTERFACE

V_{CC} = 2.7 V to 5.5 V; V_{DD} = 11.4 V to 16.5 V; V_{SS} = −11.4 V to −16.5 V; AGND = DGND = DUTGND = 0 V; $V_{REF}(+)$ = 5 V; $V_{REF}(-)$ = −3.5 V, FIFOEN = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter[1, 2, 3]	Limit at T_{MIN} to T_{MAX}	Unit	Description
t_0	4.5	ns min	REG0, REG1, Address to $\overline{WR}$ Rising Edge Setup Time.
t_1	4.5	ns min	REG0, REG1, Address to $\overline{WR}$ Rising Edge Hold Time.
t_2	10	ns min	$\overline{CS}$ Pulse Width Low.
t_3	10	ns min	$\overline{WR}$ Pulse Width Low.
t_4	0	ns min	$\overline{CS}$ to $\overline{WR}$ Falling Edge Setup Time.
t_5	0	ns min	$\overline{WR}$ to $\overline{CS}$ Rising Edge Hold Time.
t_6	4.5	ns min	Data to $\overline{WR}$ Rising Edge Setup Time.
t_7	4.5	ns min	Data to $\overline{WR}$ Rising Edge Hold Time.
t_8	20	ns min	$\overline{WR}$ Pulse Width High.
t_9	240	ns min	Minimum $\overline{WR}$ Cycle Time (Single-Channel Write).
t_{10}[4]	0/30	ns min/max	$\overline{WR}$ Rising Edge to $\overline{BUSY}$ Falling Edge.
t_{11}[4]	330	ns max	$\overline{BUSY}$ Pulse Width Low (Single-Channel Update). See Table 10.
t_{12}	0	ns min	$\overline{BUSY}$ Rising Edge to $\overline{WR}$ Rising Edge.
t_{13}	30	ns min	$\overline{WR}$ Rising Edge to $\overline{LDAC}$ Falling Edge.
t_{14}	20	ns min	$\overline{LDAC}$ Pulse Width Low.
t_{15}[4]	150	ns typ	$\overline{BUSY}$ Rising Edge to DAC Output Response Time.
t_{16}	20	ns min	$\overline{LDAC}$ Rising Edge to $\overline{WR}$ Rising Edge.
t_{17}	0	ns min	$\overline{BUSY}$ Rising Edge to $\overline{LDAC}$ Falling Edge.
t_{18}	100	ns typ	$\overline{LDAC}$ Falling Edge to DAC Output Response Time.
t_{19}	20/30	µs typ/ max	DAC Output Settling Time.
t_{20}	10	ns min	$\overline{CLR}$ Pulse Width Low.
t_{21}	350	ns max	$\overline{CLR}$/$\overline{RESET}$ Pulse Activation Time.
t_{22}	10	ns min	$\overline{RESET}$ Pulse Width Low.
t_{23}	120	µs max	$\overline{RESET}$ Time Indicated by $\overline{BUSY}$ Low.

[1] Guaranteed by design and characterization, not production tested.
[2] All input signals are specified with $t_r = t_f$ = 2 ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.2 V.
[3] See Figure 6.
[4] Measured with load circuit in Figure 2.

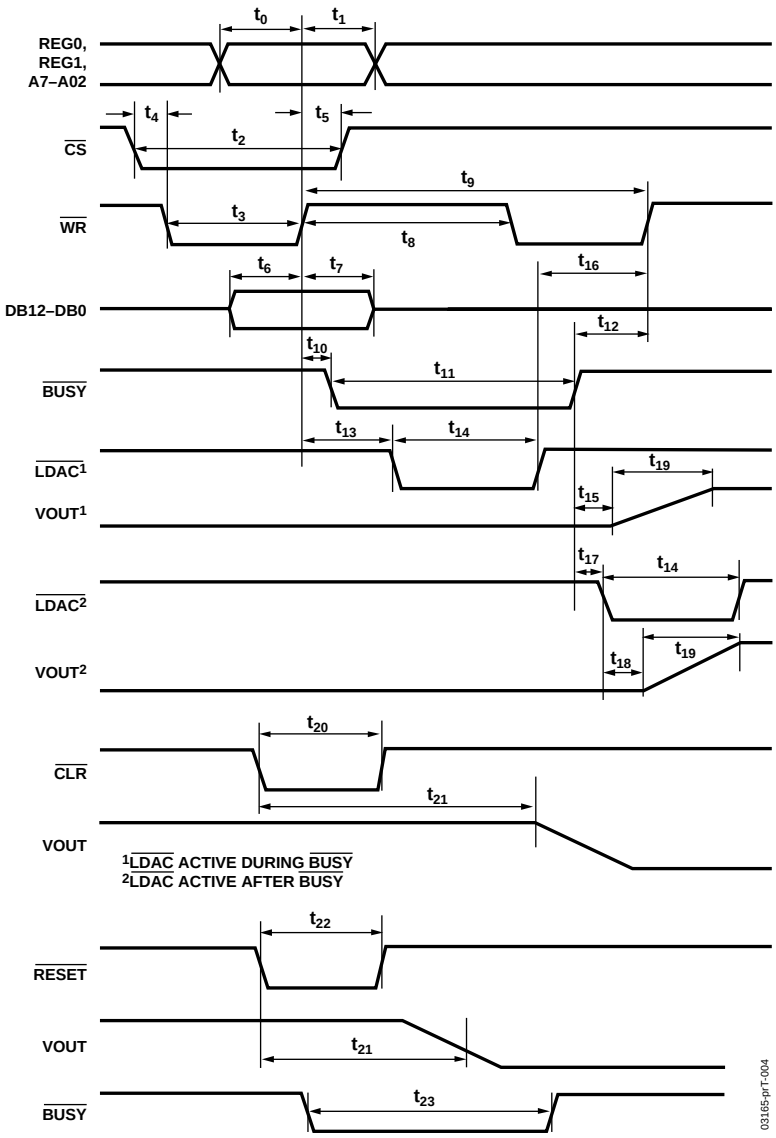


Figure 6. Parallel Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.
Transient currents of up to 100 mA do not cause SCR latch-up.

Table 6.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +17 V
V_{SS} to AGND	−17 V to +0.3 V
V_{CC} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to V_{CC} + 0.3 V
Digital Outputs to DGND	−0.3 V to V_{CC} + 0.3 V
$V_{REF}1(+)$, $V_{REF}2(+)$ to AGND	−0.3 V to +7 V
$V_{REF}1(-)$, $V_{REF}2(-)$ to AGND	V_{SS} − 0.3 V to V_{DD} + 0.3 V
V_{BIAS} to AGND	−0.3 V to +7 V
VOUT0–VOUT39 to AGND	V_{SS} − 0.3 V to V_{DD} + 0.3 V
REFGND to AGND	V_{SS} − 0.3 V to V_{DD} + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
Operating Temperature Range (T_A)	
Industrial (A Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
108-Lead CSPBGA Package	
θ_{JA} Thermal Impedance	37.5°C/W
θ_{JC} Thermal Impedance	8.5°C/W
Reflow Soldering	
Peak Temperature	230°C
Time at Peak Temperature	10 s to 40 s

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

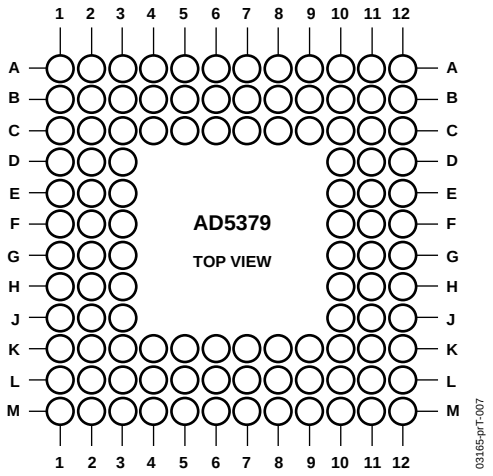


Figure 7. Pin Configuration

Table 7. 108-Lead CSPBGA Ball Configuration

CSPBGA Number	Ball Name	CSPBGA Number	Ball Name	CSPBGA Number	Ball Name	CSPBGA Number	Ball Name
A1	REG0	C4	SER/$\overline{\text{PAR}}$[1]	G1	DB1	K10	VOUT18
A2	$V_{CC}3$	C5	$\overline{\text{LDAC}}$	G2	DB0	K11	VOUT22
A3	DB10	C6	VOUT8	G3	$\overline{\text{BUSY}}$	K12	VOUT23
A4	AGND4	C7	VOUT3	G10	$V_{SS}3$	L1	A7
A5	V_{BIAS}	C8	VOUT4	G11	VOUT29	L2	A6
A6	VOUT5	C9	VOUT9	G12	REFGNDC2	L3	N/C[2]
A7	AGND3	C10	VOUT34	H1	$\overline{\text{WR}}$/DCEN	L4	$\overline{\text{RESET}}$[3]
A8	REFGNDA1	C11	VOUT32	H2	SDO[3]	L5	VOUT17
A9	$V_{DD}5$	C12	VOUT33	H3	$\overline{\text{CS}}$/$\overline{\text{SYNC}}$	L6	AGND2
A10	$V_{SS}5$	D1	DB7	H10	VOUT28	L7	VOUT14
A11	$V_{SS}4$	D2	DB8	H11	VOUT26	L8	VOUT10
A12	$V_{DD}4$	D3	DGND1	H12	VOUT27	L9	$V_{DD}1$
B1	REG1	D10	$V_{REF}1(-)$	J1	A0	L10	$V_{REF}2(+)$
B2	DGND4	D11	VOUT35	J2	A1	L11	VOUT20
B3	DB9	D12	VOUT36	J3	A2	L12	VOUT21
B4	$\overline{\text{CLR}}$	E1	DB5	J10	VOUT19	M1	DGND3
B5	VOUT7	E2	DB6	J11	VOUT24	M2	$V_{CC}2$
B6	VOUT6	E3	$V_{CC}1$	J12	VOUT25	M3	FIFOEN[1]
B7	VOUT0	E10	REFGNDB2	K1	A4	M4	AGND1
B8	VOUT1	E11	VOUT37	K2	A5	M5	VOUT15
B9	VOUT2	E12	VOUT38	K3	A3	M6	VOUT11
B10	VOUT31	F1	DB4	K4	DGND2	M7	REFGNDB1
B11	REFGNDD1	F2	DB3	K5	REFGNDA2	M8	$V_{REF}1(+)$
B12	VOUT30	F3	DB2	K6	$V_{REF}2(-)$	M9	$V_{SS}1$
C1	DB13	F10	$V_{DD}3$	K7	VOUT12	M10	$V_{SS}2$
C2	DB12/SCLK	F11	REFGNDD2	K8	VOUT13	M11	$V_{DD}2$
C3	DB11/DIN	F12	VOUT39	K9	VOUT16	M12	REFGNDC1

[1] Internal 1 MΩ pull-down device on this logic input. Therefore, it can be left floating and defaults to a logic low condition.
[2] N/C—Do not connect to this pin. Internal active pull-up device on these logic inputs. They default to a logic high condition.
[3] Internal 1 MΩ pull-up device on this logic input. Therefore, it can be left floating and defaults to a logic high condition.

Table 8. Pin Function Descriptions

Pin	Function
V_{CC}(1–3)	Logic Power Supply; 2.7 V to 5.5 V. These pins should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
V_{SS}(1–5)	Negative Analog Power Supply; −11.4 V to −16.5 V for specified performance. These pins should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
V_{DD}(1–5)	Positive Analog Power Supply; +11.4 V to +16.5 V for specified performance. These pins should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
AGND(1–4)	Ground for All Analog Circuitry. All AGND pins should be connected to the AGND plane.
DGND(1–4)	Ground for All Digital Circuitry. All DGND pins should be connected to the DGND plane.
V_{REF}1(+), V_{REF}1(−)	Reference Inputs for DACs 0 to 7, 10 to 17, 20 to 27, and 30 to 37. These voltages are referred to AGND.
V_{REF}2(+), V_{REF}2(−)	Reference Inputs for DACs 8, 9, 18, 19, 28, 29, 38, and 39. These reference voltages are referred to AGND.
V_{BIAS}	DAC Bias Voltage Input/Output. This pin provides an access to the on-chip voltage generator voltage and is provided for bypassing and overdriving purposes only. If $V_{REF}(+) > 4.25$ V, V_{BIAS} must be pulled high externally to an equal or higher potential (for example, 5 V). If $V_{REF}(+) < 4.25$ V, the on-chip bias generator can be used. In this case, the V_{BIAS} pin should be decoupled with a 10 nF capacitor to AGND.
VOUT0 to VOUT39	DAC Outputs. Buffered analog outputs for each of the 40 DAC channels. Each analog output is capable of driving an output load of 5 kΩ to ground. Typical output impedance of these amplifiers is 1 Ω.
SER/$\overline{\text{PAR}}$	Interface Select Input. This pin allows the user to select whether the serial or parallel interface is used. This pin has an internal 1 MΩ pull-down resistor, meaning that the default state at power-on is parallel mode. If this pin is tied high, the serial interface is used.
$\overline{\text{SYNC}}$[1]	Active Low Input. This is the frame synchronization signal for the serial interface.
SCLK[1]	Serial Clock Input. Data is clocked into the shift register on the falling edge of SCLK. This pin operates at clock speeds up to 50 MHz.
DIN[1]	Serial Data Input. Data must be valid on the falling edge of SCLK.
SDO[1]	Serial Data Output. CMOS output. SDO can be used for daisy-chaining a number of devices together. Data is clocked out on SDO on the rising edge of SCLK and is valid on the falling edge of SCLK.
DCEN[1]	Daisy-Chain Select Input (level sensitive, active high). When high, this signal is used in conjunction with SER/$\overline{\text{PAR}}$ high to enable serial interface daisy-chain mode.
$\overline{\text{CS}}$	Parallel Interface Chip Select Input (level sensitive, active low). If this pin is low, the device is selected.
$\overline{\text{WR}}$	Parallel Interface Write Input (edge sensitive). The rising edge of $\overline{\text{WR}}$ is used in conjunction with $\overline{\text{CS}}$ low and the address bus inputs to write to the selected AD5379 registers.
DB13 to DB0	Parallel Data Inputs. The AD5379 can accept a straight 14-bit parallel word on DB0 to DB13, where DB13 is the MSB and DB0 is the LSB.
A0 to A7	Parallel Address Inputs. A7 to A4 are decoded to select one group or multiple groups of registers (input registers, gain registers (m) or offset registers (c)) for a data transfer. This pin is used in conjunction with the REG1 and REG0 pins to determine the destination register for the input data. See the Parallel Interface section for details of the address decoding.
REG0	Parallel Interface Register Select Input. This pin is used together with REG1 to select data registers, gain registers, offset registers, increment/decrement mode, or the soft reset function. See Table 11.
$\overline{\text{CLR}}$	Asynchronous Clear Input (level sensitive, active low). When $\overline{\text{CLR}}$ is low, the input to each of the DAC output buffer stages, VOUT0 to VOUT39, is switched to the externally set potential on the relevant REFGND pin. While $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is taken high again, the DAC outputs remain cleared until $\overline{\text{LDAC}}$ is taken low. The contents of input registers and DAC registers 0 to 39 are not affected by taking $\overline{\text{CLR}}$ low.
$\overline{\text{BUSY}}$	Digital Input/Open-Drain Output. This pin must be pulled high with a pull-up resistor for correct operation. $\overline{\text{BUSY}}$ goes low during internal calculations of x2. During this time, the user can continue writing new data to additional ×1, c, and m registers (these are stored in a FIFO), but no further updates to the DAC registers and DAC outputs can take place. If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is low, this event is stored. Because $\overline{\text{BUSY}}$ is bidirectional, it can be pulled low externally to delay $\overline{\text{LDAC}}$ action. $\overline{\text{BUSY}}$ also goes low during power-on reset or when the $\overline{\text{RESET}}$ pin is low. During a $\overline{\text{RESET}}$ operation, the parallel interface is disabled and any events on $\overline{\text{LDAC}}$ are ignored.
$\overline{\text{LDAC}}$	Load DAC Logic Input (active low). If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is inactive (high), the contents of the input registers are transferred to the DAC registers and the DAC outputs are updated. If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is active and internal calculations are taking place, the $\overline{\text{LDAC}}$ event is stored and the DAC registers are updated when $\overline{\text{BUSY}}$ goes inactive. However, any events on $\overline{\text{LDAC}}$ during power-on reset or $\overline{\text{RESET}}$ are ignored.
FIFOEN	FIFO Enable (level sensitive, active high). When connected to DVDD, the internal FIFO is enabled, allowing the user to write to the device at full speed. FIFO is available in both serial and parallel mode. The FIFOEN pin has an internal 1 MΩ pull-down resistor connected to ground, meaning that the FIFO is disabled by default.

Pin	Function
$\overline{\text{RESET}}$	Asynchronous Digital Reset Input (falling edge sensitive). If unused, $\overline{\text{RESET}}$ may be left unconnected; an internal pull-up resistor (1 MΩ) ensures that the $\overline{\text{RESET}}$ input is held high. The function of this pin is equivalent to that of the power-on reset generator. When this pin is taken low, the AD5379 state machine initiates a reset sequence to digitally reset x1, m, c, and x2 registers to their default power-on values. This sequence takes 100 µs (typ). Furthermore, the input to each of the DAC output buffer stages, VOUT0 to VOUT39, is switched to the externally set potential on the relevant REFGND pin. During $\overline{\text{RESET}}$, BUSY goes low and the parallel interface is disabled. All $\overline{\text{LDAC}}$ pulses are ignored until BUSY goes high. When $\overline{\text{RESET}}$ is taken high again, the DAC ouputs remain at REFGND until $\overline{\text{LDAC}}$ is taken low.
REFGNDA1	Reference Ground for DACs 0 to 7. VOUT0 to VOUT7 are referenced to this voltage.
REFGNDA2	Reference Ground for DACs 8 and 9. VOUT8 and VOUT9 are referenced to this voltage.
REFGNDB1	Reference Ground for DACs 10 to 17. VOUT10 to VOUT17 are referenced to this voltage.
REFGNDB2	Reference Ground for DACs 18 and 19. VOUT18 and VOUT19 are referenced to this voltage.
REFGNDC1	Reference Ground for DACs 20 to 27. VOUT20 to VOUT27 are referenced to this voltage.
REFGNDC2	Reference Ground for DACs 28 and 29. VOUT28 and VOUT29 are referenced to this voltage.
REFGNDD1	Reference Ground for DACs 30 to 37. VOUT30 to VOUT37 are referenced to this voltage.
REFGNDD2	Reference Ground for DACs 38 and 39. VOUT38 and VOUT39 are referenced to this voltage.

[1] These serial interface signals do not require separate pins, but share parallel interface pins.

TERMINOLOGY

Relative Accuracy
Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error and is expressed in least significant bits (LSB).

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Zero-Scale Error
Zero-scale error is the error in the DAC output voltage when all 0s are loaded into the DAC register.

Ideally, with all 0s loaded to the DAC and m is all 1s, c is 10 0000 0000 0000:

$$VOUT_{(zero\text{-}scale)} = 2.5 \times V_{REF}(-) - AGND) + REFGND$$

Zero-scale error is a measure of the difference between VOUT (actual) and VOUT (ideal) expressed in mV. Zero-scale error is mainly due to offsets in the output amplifier.

Full-Scale Error
Full-scale error is the error in DAC output voltage when all 1s are loaded into the DAC register.

Ideally, with all 1s loaded to the DAC and m is all 1s, c is 10 0000 0000 0000:

$$VOUT_{(full\text{-}scale)} = 3.5 \times (V_{REF}(+) - AGND) + 2.5 \times (V_{REF}(-) - AGND) + REFGND$$

Full-scale error is a measure of the difference between VOUT (actual) and VOUT (ideal) expressed in mV. It does not include zero-scale error.

Gain Error
Gain error is the difference between full-scale error and zero-scale error. It is expressed in mV.

$$Gain\ Error = Full\text{-}Scale\ Error - Zero\text{-}Scale\ Error$$

VOUT Temperature Coefficient
This includes output error contributions from linearity, offset, and gain drift.

DC Output Impedance
DC output impedance is the effective output source resistance. It is dominated by package lead resistance.

DC Crosstalk
The 40 DAC outputs are buffered by op amps that share common V_{DD} and V_{SS} power supplies. If the dc load current changes in one channel (due to an update), this can result in a further dc change in one or more channel outputs. This effect is more significant at high load currents and reduces as the load currents are reduced. With high impedance loads, the effect is virtually unmeasurable. Multiple V_{DD} and V_{SS} terminals are provided to minimize dc crosstalk.

Output Voltage Settling Time
This is the amount of time it takes for the output of a DAC to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Energy
This is the amount of energy injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 0x1FFF and 0x2000.

Channel-to-Channel Isolation
Channel-to-channel isolation refers to the proportion of input signal from one DAC's reference input that appears at the output of another DAC operating from another reference. It is expressed in dB and measured at midscale.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse that appears at the output of one converter due to both the digital change and subsequent analog output change at another converter. It is specified in nV-s.

Digital Crosstalk
The glitch impulse transferred to the output of one converter due to a change in the DAC register code of another converter is defined as the digital crosstalk and is specified in nV-s.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device's digital inputs can be capacitively coupled both across and through the device to show up as noise on the VOUT pins. It can also be coupled along the supply and ground lines. This noise is digital feedthrough.

Output Noise Spectral Density
This is a measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per √Hz). It is measured by loading all DACs to midscale and measuring noise at the output. It is measured in $nV/(Hz)^{1/2}$.

TYPICAL PERFORMANCE CHARACTERISTICS

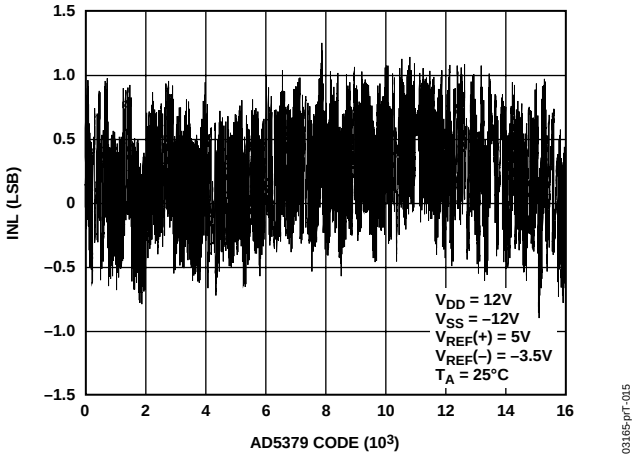


Figure 8. Typical INL Plot

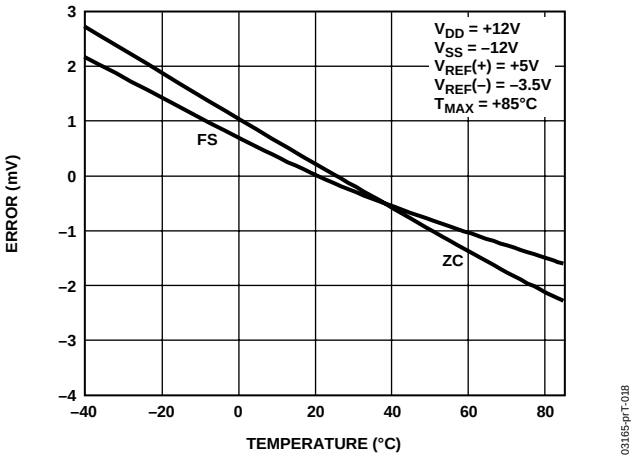


Figure 11. Typical Full-Scale and Zero-Scale Errors vs. Temperature

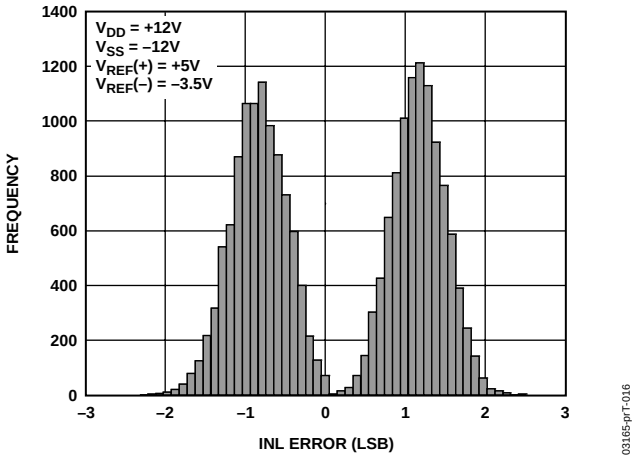


Figure 9. INL Error Distribution (–40°C, +25°C, +85°C Superimposed)

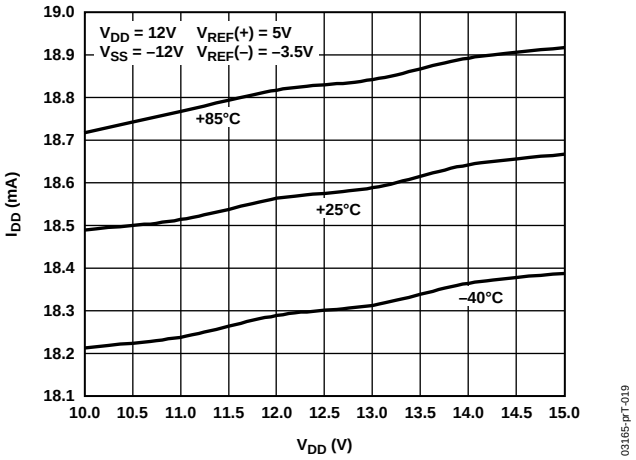


Figure 12. I_{DD} vs. V_{DD} over Temperature

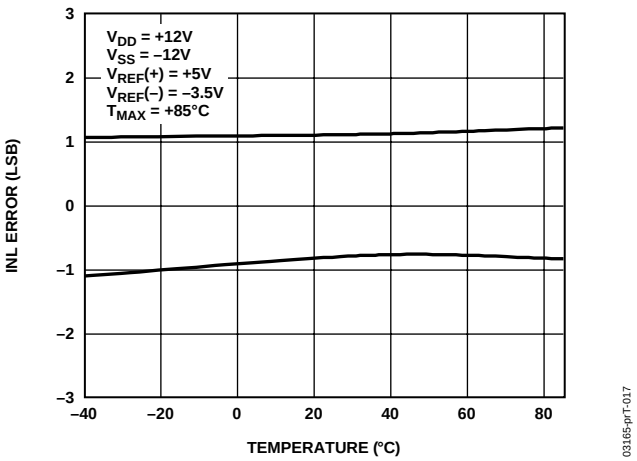


Figure 10. Typical INL Error vs. Temperature

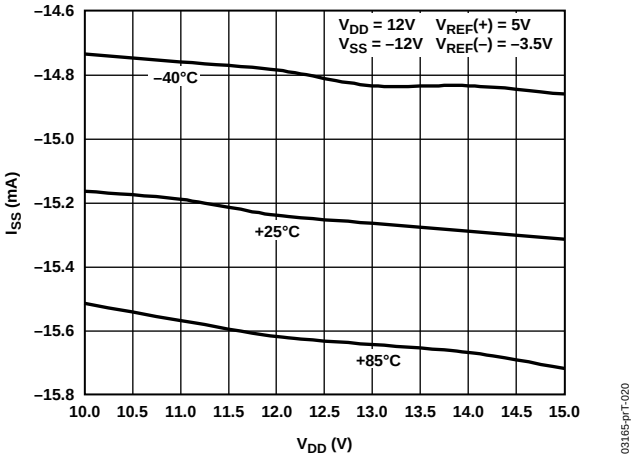


Figure 13.I_{SS} vs. V_{DD} over Temperature

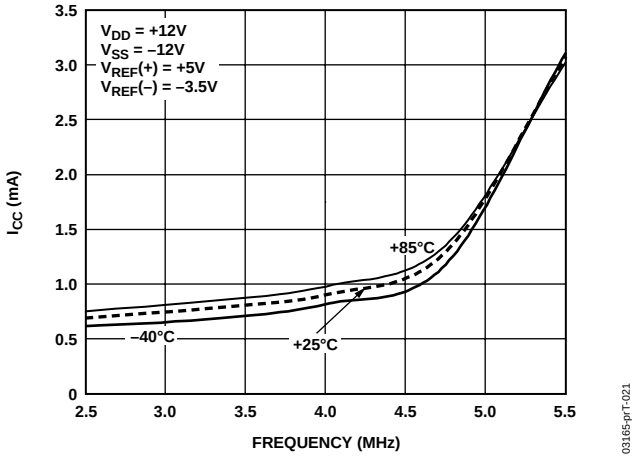


Figure 14. I_{CC} vs. Supply

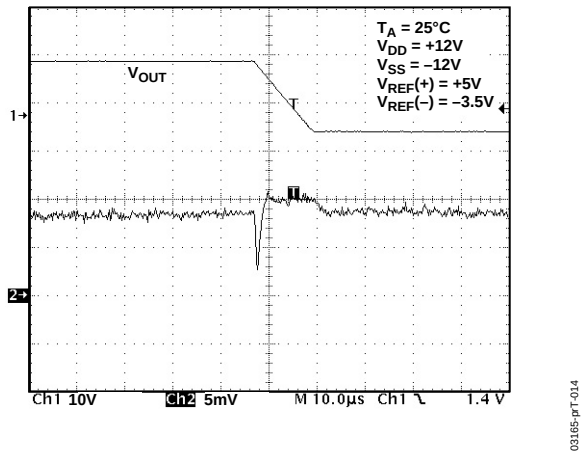


Figure 17. DAC-to-DAC Crosstalk

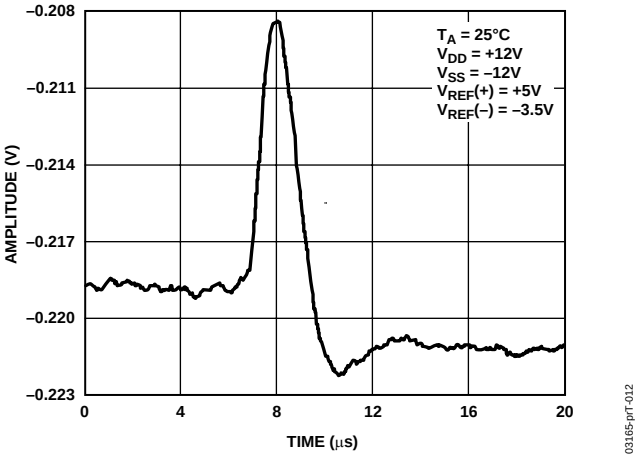


Figure 15. Major Code Transition Glitch Energy

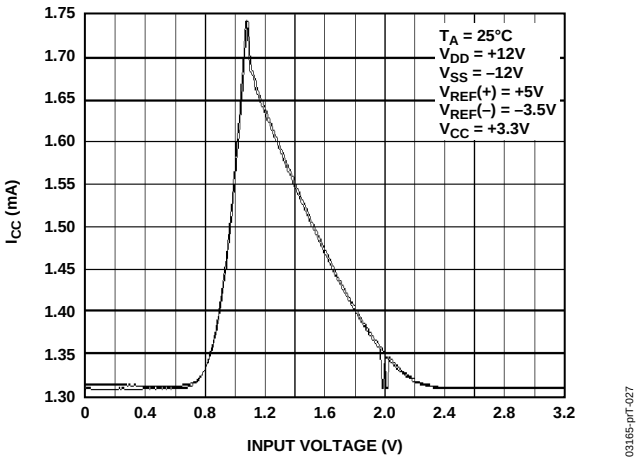


Figure 18. Supply Current vs. Digital Input Voltage

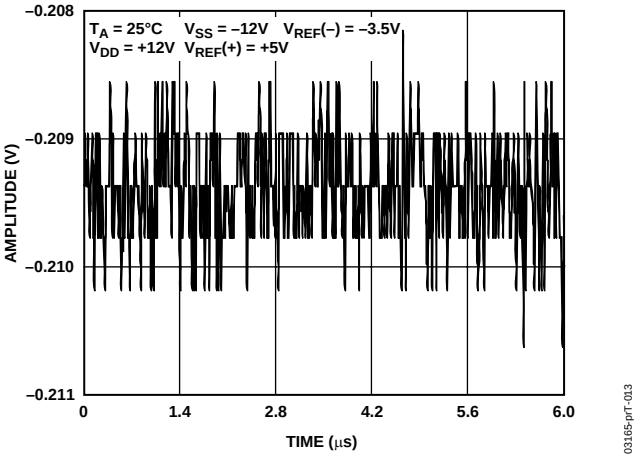


Figure 16. Digital Feedthrough

FUNCTIONAL DESCRIPTION

DAC ARCHITECTURE—GENERAL

The AD5379 contains 40 DAC channels and 40 output amplifiers in a single package. The architecture of a single DAC channel consists of a 14-bit resistor-string DAC followed by an output buffer amplifier. The resistor-string section is simply a string of resistors, each of value R, from $V_{REF}(+)$ to AGND. This type of architecture guarantees DAC monotonicity. The 14-bit binary digital code loaded to the DAC register determines at which node on the string the voltage is tapped off before being fed into the output amplifier. The output amplifier translates the output of the DAC to a wider range. The DAC output is gained up by a factor of 3.5 and offset by the voltage on the $V_{REF}(-)$ pin. See the Transfer Function section.

CHANNEL GROUPS

The 40 DAC channels on the AD5379 are arranged into four groups (A, B, C, D) of 10 channels. In each group, eight channels are connected to $V_{REF}1(+)$ and $V_{REF}1(-)$ and the remaining two channels are connected to $V_{REF}2(+)$ and $V_{REF}2(-)$. Each group has two individual REFGND pins. For example, in Group A, eight channels are connected to REFGNDA1, and the remaining two channels are connected to REFGNDA2. In addition to an input register (x1) and a DAC register (x2), each channel has a gain register (m) and an offset register (c). See Table 17. The inclusion of these registers allows the user to calibrate out errors in the complete signal chain, including the DAC errors.

Table 9 shows the reference and REFGND inputs, and the m and c registers for Group A. Groups B, C, and D are similar.

Table 9. Inputs and Registers for Group A

Channel	Reference	REFGND	m, c Registers
0…7	$V_{REF}1(+)$, $V_{REF}1(-)$	REFGNDA1	m REG0…7 c REG0…7
8…9	$V_{REF}2(+)$, $V_{REF}2(-)$	REFGNDA2	m REG8…9 c REG8…9

TRANSFER FUNCTION

The digital input transfer function for each DAC can be represented as

$$x2 = [(m + 1)/2^{14} \times x1] + (c - 2^{N-1})$$

where:
x2 is the data-word loaded to the resistor string DAC. (Default is 10 0000 0000 0000.)
x1 is the 14-bit data-word written to the DAC input register. (Default is 10 0000 0000 0000.)
m is the 13-bit gain coefficient. (Default is 1 1111 1111 1111.)
c is the 14-bit offset coefficient. (Default is 10 0000 0000 0000.)
n is the DAC resolution. (*n* = 14).

Figure 19 shows a single DAC channel and its associated registers. The power-on values for the m and c registers are full scale and 0x2000, respectively. The user can individually adjust the voltage range on each DAC channel by overwriting the power-on values of m and c. The AD5379 has digital overflow and underflow detection circuitry to clamp the DAC output at full scale or zero scale when the values chosen for x1, m, and c result in x2 being out of range.

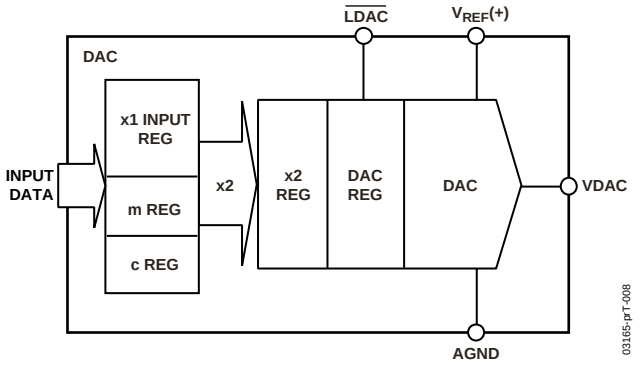


Figure 19. Single DAC Channel

The complete transfer function for the AD5379 can be represented as

$$VOUT = 3.5 \times ((V_{REF}(+) - AGND) \times x2/2^{14}) + 2.5 \times (V_{REF}(-) - AGND) + REFGND$$

where:
x2 is the data word loaded to the resistor string DAC.
$V_{REF}(+)$ is the voltage at the positive reference pin.
$V_{REF}(-)$ is the voltage at the negative reference pin.

Figure 20 shows the output amplifier stage of a single channel. VDAC is the voltage output from the resistor string DAC. The nominal range of VDAC is 1 LSB to full scale.

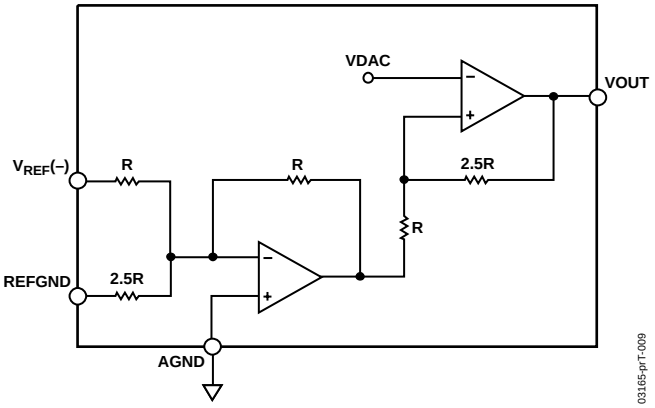


Figure 20. Output Amplifier Stage

V_{BIAS} FUNCTION

The AD5379 has an on-chip voltage generator that provides a bias voltage of 4.25 V (min). The V_{BIAS} pin is provided for bypassing and overdriving purposes only. It is not intended to be used as a supply or a reference. If $V_{REF}(+) > 4.25$ V, V_{BIAS} must be pulled high externally to an equal or higher potential (such as 5 V). The external voltage source should be capable of driving a 50 µA (typical) current sink load.

REFERENCE SELECTION

The voltages applied to $V_{REF}(+)$ and $V_{REF}(-)$ determine the output voltage range and span on VOUT0 to VOUT39. If the offset and gain features are not used (m and c are left at their power-on values), the reference levels required can be calculated as follows:

$$V_{REF}(+)_{min} = (VOUT_{max} - VOUT_{min})/3.5$$
$$V_{REF}(-)_{max} = (AGND + VOUT_{min})/2.5$$

If the offset and gain features of the AD5379 are used, then the output range required is slightly different. The output range chosen should take into account the offset and gain errors that need to be trimmed out. Therefore, the chosen output range should be larger than the actual required range.

The reference levels required can be calculated as follows:

1. Identify the nominal output range on VOUT.
2. Identify the maximum offset span and the maximum gain required on the full output signal range.
3. Calculate the new maximum output range on VOUT including the maximum offset and gain errors expected.
4. Choose the new $VOUT_{max}$ and $VOUT_{min}$ required, keeping the new VOUT limits centered on the nominal values and assuming REFGND is zero (or equal to AGND). Note that V_{DD} and V_{SS} must provide sufficient headroom.
5. Calculate the values of $V_{REF}(+)$ and $V_{REF}(-)$ as follows:

$$V_{REF}(+)_{min} = (VOUT_{max} - VOUT_{min})/3.5$$
$$V_{REF}(-)_{max} = (AGND + VOUT_{min})/2.5$$

In addition, when using reference values other than those suggested ($V_{REF}(+) = 5$ V and $V_{REF}(-) = -3.5$ V), the expected offset error component changes as follows:

$$V_{OFFSET} = 0.125 \times (V_{REF}(-)_A + 0.7 \times V_{REF}(+)_A)$$

where:
$V_{REF}(-)_A$ is the new negative reference value.
$V_{REF}(+)_A$ is the new positive reference value.

If this offset error too large to calibrated out, then it is possible to adjust the negative reference value to account for this using the following equation:

$$V_{REF}(-)_{NEW} = V_{REF}(-)_A - V_{OFFSET}/2.625$$

Reference Selection Example

Nominal Output Range = 10 V; (−2 V to +8 V)
Offset Error = ±100 mV;
Gain Error = ±3%;
REFGND = *AGND* = 0 V;

1) *Gain Error* = ±3%;
=> *Maximum Positive Gain Error* = +3%
=> *Output Range incl. Gain Error* = 10 + 0.03 (10) = 10.3 V

2) Offset Error = ±100 mV;
=> *Maximum Offset Error Span* = 2(100) mV = 0.2 V
=> *Output Range incl. Gain Error and Offset Error* = 10.3 + 0.2 = 10.5 V

3) $V_{REF}(+)$ and $V_{REF}(-)$ Calculation:
Actual Output Range = 10.5 V, that is, −2.25 V to +8.25 V (centered);

=> $V_{REF}(+) = (8.25 + 2.25)/3.5 = 3$ V
$V_{REF}(-) = -2.25/2.5 = -0.9$ V

If the solution yields inconvenient reference levels, the user can adopt one of three approaches:

- Use a resistor divider to divide down a convenient, higher reference level to the required level.
- Select convenient reference levels above $V_{REF}(+)_{min}$ or below $V_{REF}(-)_{max}$. Modify the gain and offset registers to downsize the references digitally. In this way, the user can use almost any convenient reference level, but may reduce performance by overcompaction of the transfer function.
- Use a combination of these two approaches.

CALIBRATION

The user can perform a system calibration by overwriting the default values in the m and c registers for any individual DAC channel as follows:

- Calculate the nominal offset and gain coefficients for the new output range (see previous example).
- Calculate the new m and c values for each channel based on the specified offset and gain errors.

Calibration Example

Nominal Offset Coefficient = 0
Nominal Gain Coefficient = 10/10.5 × 8191 = 0.95238 × 8191 = 7801

Example 1: *Channel 0, Gain Error* = 3%, *Offset Error* = 100 mV
1) Gain Error (3%) *Calibration:* 7801 × 1.03 = 8035
=> *Load Code* "1 1111 0110 0011" to m Register 0

2) Offset Error (100 mV) *Calibration:*
LSB Size = 10.5 / 16384 = 641 μV;
Offset Coefficient for 100 mV Offset = 100 / 0.64 = 156 LSBs
=> *Load* "10 0000 1001 1100" to c Register 0

Example 2: *Channel 1, Gain Error* = −3%, *Offset Error* = −100 mV
1) Gain Error (−3%) *Calibration:* 7801 × 0.97 = 7567
=> *Load Code* "1 1110 1000 1111" to m Register 1

2) Offset Error (−100 mV) *Calibration:*
LSB Size = 10.5 / 16384 = 641 μV;
Offset Coefficient for −100 mV *Offset* = −100 / 0.64 = −156 LSBs
=> *Load* "01 1111 0110 0100" to c Register 1

CLEAR FUNCTION

The clear function on the AD5379 can be implemented in hardware or software.

Hardware Clear

Bringing the $\overline{\text{CLR}}$ pin low switches the outputs, VOUT0 to VOUT39, to the externally set potential on the REFGND pin. This is achieved by switching in REFGND and reconfiguring the output amplifier stages into unity gain buffer mode, thus ensuring VOUT = REFGND. The contents of the input registers and DAC registers are not affected by taking $\overline{\text{CLR}}$ low. When $\overline{\text{CLR}}$ is brought high, the DAC outputs remain cleared until $\overline{\text{LDAC}}$ is taken low. While $\overline{\text{CLR}}$ is low, the value of $\overline{\text{LDAC}}$ is ignored.

Software Clear

Loading a clear code to the x1 registers also enables the user to set VOUT0 to VOUT39 to the REFGND level. The default clear code corresponds to m at full scale and c at midscale (x*2* = x*1*).

Default Clear Code
$= 2^{14} \times (-Output\ Offset)/(Output\ Range)$
$= 2^{14} \times 2.5 \times (AGND - V_{REF}(-))/(3.5 \times (V_{REF}(+) - AGND))$

The more general expression for the clear code is as follows:

$Clear\ Code = (2^{14})/(m + 1) \times (Default\ Clear\ Code - c)$

$\overline{\text{BUSY}}$ AND $\overline{\text{LDAC}}$ FUNCTIONS

The value of x2 is calculated each time the user writes new data to the corresponding x1, c, or m registers. During the calculation of x2, the $\overline{\text{BUSY}}$ output goes low. While $\overline{\text{BUSY}}$ is low, the user can continue writing new data to the x1, m, or c registers, but no DAC output updates can take place. The DAC outputs are updated by taking the $\overline{\text{LDAC}}$ input low. If $\overline{\text{LDAC}}$ goes low while $\overline{\text{BUSY}}$ is active, the $\overline{\text{LDAC}}$ event is stored and the DAC outputs update immediately after $\overline{\text{BUSY}}$ goes high. A user can also hold the $\overline{\text{LDAC}}$ input permanently low. In this case, the DAC outputs update immediately after $\overline{\text{BUSY}}$ goes high.

Table 10. $\overline{\text{BUSY}}$ Pulse Width

	$\overline{\text{BUSY}}$ Pulse Width (ns max)	
Action	**FIFO Enabled**	**FIFO Disabled**
Loading x1, c, or m to 1 channel	530	330
Loading x1, c, or m to 2 channels	700	500
Loading x1, c, or m to 3 channels	900	700
Loading x1, c, or m to 4 channels	1050	850
Loading x1, c, or m to all 40 channels	5500	5300

The value of x2 for a single channel or group of channels is recalculated each time there is a write to any x1 register(s), c register(s), or m register(s). During the calculation of x2, $\overline{\text{BUSY}}$ goes low. The duration of this $\overline{\text{BUSY}}$ pulse depends on the number of channels being updated. For example, if x1, c, or m data is written to one DAC channel, $\overline{\text{BUSY}}$ goes low for 550 ns (max). However, if data is written to two DAC channels, $\overline{\text{BUSY}}$ goes low for 700 ns (max). Note that there are approximately 200 ns of overhead due to FIFO access. See Table 10.

The AD5379 contains an extra feature whereby a DAC register is not updated unless its x2 register has been written to since the last time $\overline{\text{LDAC}}$ was brought low. Normally, when $\overline{\text{LDAC}}$ is brought low, the DAC registers are filled with the contents of the x2 registers. However the AD5379 updates the DAC register only if the x2 data has changed, thereby removing unnecessary digital crosstalk.

FIFO VS. NON-FIFO OPERATION

Two modes of operation are available for loading data to the AD5379 registers: operation with FIFO disabled and operation with FIFO enabled. Operation with FIFO disabled is optimum for single writes to the device. If the system requires significant data transfers to the AD5379, however, then operation with FIFO enabled is more efficient.

When FIFO is enabled, the AD5379 uses an internal FIFO memory to allow high speed successive writes in both serial and parallel modes. This optimizes the interface speed and efficiency, minimizes the total conversion time due to internal digital efficiencies, and minimizes the overhead on the master controller when managing the data transfers. The BUSY signal goes low while instructions in the state machine are being executed.

Table 10 compares operation with FIFO enabled and FIFO disabled for different data transfers to the AD5379. Operation with FIFO enabled is more efficient for all operations except single write operations. When using the FIFO, the user can continue writing new data to the AD5379 while write instructions are being executed. Up to 128 successive instructions can be written to the FIFO at maximum speed. When the FIFO is full, additional writes to the AD5379 are ignored.

$\overline{\text{BUSY}}$ INPUT FUNCTION

Because the $\overline{\text{BUSY}}$ pin is bidirectional and open-drain (for correct operation, use pull-up resistor to digital supply), a second AD5379 or any other device (such as a system controller), can pull $\overline{\text{BUSY}}$ low and, therefore, delay DAC update(s), if required. This is a means of delaying any $\overline{\text{LDAC}}$ action. This feature allows synchronous updates of multiple AD5379 devices in a system at maximum speed. As soon as the last device connected to the $\overline{\text{BUSY}}$ pin is ready, all DACs update automatically. Tying the $\overline{\text{BUSY}}$ pin of multiple devices together enables synchronous updating of all DACs without extra hardware.

POWER-ON RESET FUNCTION

The AD5379 contains a power-on reset generator and state machine. During power-on, $\overline{\text{CLR}}$ becomes active (internally), the power-on state machine resets all internal registers to their default values, and $\overline{\text{BUSY}}$ goes low. This sequence takes 8 ms (typical). The outputs, VOUT0 to VOUT39, are switched to the externally set potential on the REFGND pin. During power-on, the parallel interface is disabled, so it is not possible to write to the part. Any transitions on $\overline{\text{LDAC}}$ during the power-on period are ignored in order to reject initial $\overline{\text{LDAC}}$ pin glitching. A rising edge on $\overline{\text{BUSY}}$ indicates that power-on is complete and that the parallel interface is enabled. All DACs remain in their power-on state until $\overline{\text{LDAC}}$ is used to update the DAC outputs.

$\overline{\text{RESET}}$ INPUT FUNCTION

The AD5379 can be placed in its power-on reset state at any time by activating the $\overline{\text{RESET}}$ pin. The AD5379 state machine initiates a reset sequence to digitally reset the x1, m, c, and x2 registers to their default power-on values. This sequence takes 95 µs (typical), 120 µs (max), 70 µs (min). During this sequence, $\overline{\text{BUSY}}$ goes low. While $\overline{\text{RESET}}$ is low, any transitions on $\overline{\text{LDAC}}$ are ignored. As with the $\overline{\text{CLR}}$ input, while $\overline{\text{RESET}}$ is low, the DAC outputs are switched to REFGND. The outputs remain at REFGND until an $\overline{\text{LDAC}}$ pulse is applied. This reset function can also be implemented via the parallel interface by setting the REG0 and REG1 pins low and writing all 1s to DB13 to DB0 (see Table 16 for soft reset).

INCREMENT/DECREMENT FUNCTION

The AD5379 has a special function register that enables the user to increment or decrement the internal 14-bit input register data (x1) in steps of 0 to 127 LSBs. The increment/decrement function is selected by setting both REG1 and REG0 pins (or bits) low. Address Pins (or bits) A7 to A0 are used to select a DAC channel or group of channels. The amount by which the x1 register is incremented or decremented is determined by the DB6 to DB0 bits/pins. For example, for a 1 LSB increment or decrement, DB6...DB0 = 0000001, while for a 7 LSB increment or decrement, DB6...DB0 = 0000111. DB8 determines whether the input register data is incremented (DB8 = 1) or decremented (DB8 = 0). The maximum amount by which the user is allowed to increment or decrement the data is 127 LSBs, that is, DB6...DB0 = 1111111. The 0 LSB step is included to facilitate software loops in the user's application. See Table 15.

The AD5379 has digital overflow and underflow detection circuitry to clamp at full scale or zero scale when the values chosen for increment or decrement mode are out of range.

INTERFACES

The AD5379 contains a parallel and a serial interface. The active interface is selected via the SER/$\overline{\text{PAR}}$ pin.

The AD5379 uses an internal FIFO memory to allow high speed successive writes in both serial and parallel mode. The user can continue writing new data to the AD5379 while write instructions are being executed. The $\overline{\text{BUSY}}$ signal goes low while instructions in the FIFO are being executed. Up to 120 successive instructions can be written to the FIFO at maximum speed. When the FIFO is full, additional writes to the AD5379 are ignored.

To minimize both the power consumption of the device and on-chip digital noise, the active interface powers up fully only when the device is being written to, that is, on the falling edge of $\overline{\text{WR}}$ or on the falling edge of $\overline{\text{SYNC}}$.

All digital interfaces are 2.5 V LVTTL compatible when operating from a 2.7 V to 3.6 V V_{CC} supply.

PARALLEL INTERFACE

A pull-down on the SER/$\overline{\text{PAR}}$ pin makes the parallel interface the default. If using the parallel interface, the SER/$\overline{\text{PAR}}$ pin can be left unconnected. Figure 6 shows the timing diagram for a parallel write to the AD5379. The parallel interface is controlled by the following pins.

$\overline{\text{CS}}$ Pin

Active low device select pin.

$\overline{\text{WR}}$ Pin

On the rising edge of $\overline{\text{WR}}$, with $\overline{\text{CS}}$ low, the address values at Pins A7 to A0 are latched and data values at Pins DB13 to DB0 are loaded into the selected AD5379 input registers.

REG1, REG0 Pins

The REG1 and REG0 pins determine the destination register of the data being written to the AD5379. See Table 11.

Table 11. Register Selection

REG1	REG0	Register Selected
1	1	Input Data Register (x1)
1	0	Offset Register (c)
0	1	Gain Register (m)
0	0	Special Function Register

DB13 to DB0 Pins

The AD5379 accepts a straight 14-bit parallel word on DB0 to DB13, where DB13 is the MSB and DB0 is the LSB. See Table 12, Table 13, Table 14, Table 15, and Table 16.

A7 to A0 Pins

Each of the 40 DAC channels can be addressed individually. In addition, several channel groupings enable the user to simultaneously write the same data to multiple DAC channels. Address Bits A7 to A4 are decoded to select one group or multiple groups of registers. Address Bits A3 to A0 select one of ten input data registers (x1), offset registers (c), or gain registers (m). See Table 17.

SERIAL INTERFACE

The SER/$\overline{\text{PAR}}$ pin must be tied high to enable the serial interface and disable the parallel interface. The serial interface is controlled by five pins, as follows.

$\overline{\text{SYNC}}$, DIN, SCLK

Standard 3-wire interface pins.

DCEN

Selects standalone mode or daisy-chain mode.

SDO

Data out pin for daisy-chain mode.

Figure 4 and Figure 5 show the timing diagrams for a serial write to the AD5379 in standalone and daisy-chain modes, respectively.

The 24-bit data word format for the serial interface is shown in Figure 21.

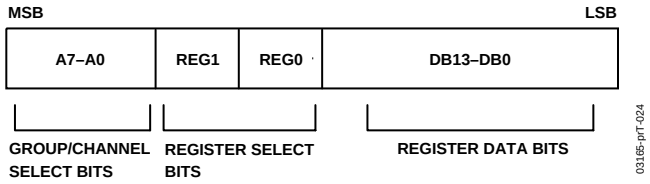


Figure 21. Serial Data Format

Standalone Mode

By connecting the DCEN (daisy-chain enable) pin low, standalone mode is enabled. The serial interface works with both a continuous and a burst serial clock. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle and resets a counter that counts the number of serial clocks to ensure that the correct number of bits is shifted into the serial shift register. Additional edges on $\overline{\text{SYNC}}$ are ignored until 24 bits are shifted in. Once 24 bits are shifted in, the SCLK is ignored. In order for another serial transfer to take place, the counter must be reset by the falling edge of $\overline{\text{SYNC}}$.

Daisy-Chain Mode

For systems that contain several DACs, the SDO pin can be used to daisy-chain several devices together. This daisy-chain mode can be useful in system diagnostics and in reducing the number of serial interface lines.

Connecting the DCEN (daisy-chain enable) pin high enables daisy-chain mode. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. The SCLK is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting this line to the DIN input on the next device in the chain, a multidevice interface is constructed. For each AD5379 in the system, 24 clock pulses are required. Therefore, the total number of clock cycles must equal 24*N*, where *N* is the total number of AD5379 devices in the chain. If fewer than 24 clocks are applied, the write sequence is ignored.

When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ should be taken high. This latches the input data in each device in the daisy chain and prevents any additional data from being clocked into the input shift register.

A continuous SCLK source can be used, if $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles. Alternatively, a burst clock containing the exact number of clock cycles can be used and $\overline{\text{SYNC}}$ taken high after the final clock to latch the data.

When the transfer to all input registers is complete, a common $\overline{\text{LDAC}}$ signal updates all DAC registers, and all analog outputs are updated simultaneously.

DATA DECODING

The AD5379 contains a 14-bit data bus, DB13 to DB0. Depending on the value of REG1 and REG0, this data is loaded into the addressed DAC input register(s), offset (c) register(s), gain (m) register(s), or the special function register.

Table 12. DAC Data Format (REG1 = 1, REG0 = 1)

DB13 to DB0	DAC Output
11 1111 1111 1111	(16383/16384) V_{REF}(+) V
11 1111 1111 1110	(16382/16384) V_{REF}(+) V
10 0000 0000 0001	(8193/16384) V_{REF}(+) V
10 0000 0000 0000	(8192/16384) V_{REF}(+) V
01 1111 1111 1111	(8191/16384) V_{REF}(+) V
00 0000 0000 0001	(1/16384) V_{REF}(+) V
00 0000 0000 0000	0 V

Table 13. Offset Data Format (REG1 = 1, REG0 = 0)

DB13 to DB0	Offset (LSB)
11 1111 1111 1111	+8191
11 1111 1111 1110	+8190
10 0000 0000 0001	+1
10 0000 0000 0000	+0
01 1111 1111 1111	−1
00 0000 0000 0001	−8191
00 0000 0000 0000	−8192

Table 14. Gain Data Format (REG1 = 0, REG0 = 1)

DB12 to DB1	Gain
1 1111 1111 1111	8192/8192
1 1111 1111 1110	8191/8192
1 0000 0000 0001	4098/8192
1 0000 0000 0000	4097/8192
0 1111 1111 1111	4096/8192
0 0000 0000 0001	2/8192
0 0000 0000 0000	1/8192

Table 15. Special Function Data Format (REG1 = 0, REG0 = 0)

DB13 to DB0	Increment/Decrement Step (LSB)
00000 10 1111111	+127
00000 10 0000111	+7
00000 10 0000001	+1
00000 X0 0000000	0
00000 00 0000001	−1
00000 00 0000111	−7
00000 00 1111111	−128

Table 16. Soft Reset (REG1 = 0, REG0 = 0)

DB13 to DB0	DAC Output
11 1111 1111 1111	REFGND

ADDRESS DECODING

The AD5379 contains an 8-bit address bus, A7 to A0. This address bus allows each DAC input register (x1), each offset (c) register, and each gain (m) register to be individually updated.

The REG1 and REG0 bits in the special function register (SFR) (see Table 9) show the decoding for data, offset, and gain registers. Note that when all 40 DAC channels are selected, Address Bits A[3:0] are ignored.

Table 17. DAC Group Addressing

A7	A6	A5	A4	Group
0	0	0	0	All 40 DACs
0	0	0	1	Group 1
0	0	1	0	Group 2
0	0	1	1	Groups 1, 2
0	1	0	0	Group 3
0	1	0	1	Groups 1, 3
0	1	1	0	Groups 2, 3
0	1	1	1	Groups 1, 2, 3
1	0	0	0	Group 4
1	0	0	1	Groups 1, 4
1	0	1	0	Groups 2, 4
1	0	1	1	Groups 1, 2, 4
1	1	0	0	Groups 3, 4
1	1	0	1	Groups 1, 3, 4
1	1	1	0	Groups 2, 3, 4
1	1	1	1	Groups 1, 2, 3, 4

A3	A2	A1	A0	Data/Offset/Gain/INC-DEC Register
0	0	0	0	Register 0
0	0	0	1	Register 1
0	0	1	0	Register 2
0	0	1	1	Register 3
0	1	0	0	Register 4
0	1	0	1	Register 5
0	1	1	0	Register 6
0	1	1	1	Register 7
1	0	0	0	Register 8
1	0	0	1	Register 9

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5379 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5379 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device. For supplies with multiple pins (V_{SS}, V_{DD}, V_{CC}), it is recommended to tie these pins together and to decouple each supply once.

The AD5379 should have ample supply decoupling of 10 µF in parallel with 0.1 µF on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching.

Digital lines running under the device should be avoided, because these couple noise onto the device. The analog ground plane should be allowed to run under the AD5379 to avoid noise coupling. The power supply lines of the AD5379 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching digital signals should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. It is essential to minimize noise on all $V_{REF}(+)$ and $V_{REF}(-)$ lines. The V_{BIAS} pin should be decoupled with a 10 nF capacitor to AGND.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, while signal traces are placed on the solder side.

As is the case for all thin packages, care must be taken to avoid flexing the CSPBGA package and to avoid a point load on the surface of this package during the assembly process.

POWER-ON

An on-chip power supply monitor makes the AD5379 robust to power sequencing. The supply monitor powers up the analog section after ($V_{DD} - \overline{V_{SS}}$) is greater than 7 V (typical). The output buffers power up in $\overline{CLR}$ mode forced to the DUTGND potential, even if V_{CC} remains at 0 V. After V_{SS} is applied, the analog circuitry powers up and the buffered DAC output level settles linearly within the supply range.

TYPICAL APPLICATION CIRCUIT

The high channel count of the AD5379 makes it well suited to applications requiring high levels of integration such as optical and automatic test equipment (ATE) systems. Figure 22 shows the AD5379 as it would be used in an ATE system. Shown here is one pin of a typical logic tester. It is apparent that a number of discrete levels are required for the pin driver, active load circuit, parametric measurement unit, comparators, and clamps.

In addition to the DAC levels required in the ATE system shown, drivers, loads, comparators, and parametric measurement unit functions are also required. Analog Devices provides solutions for all these functions.

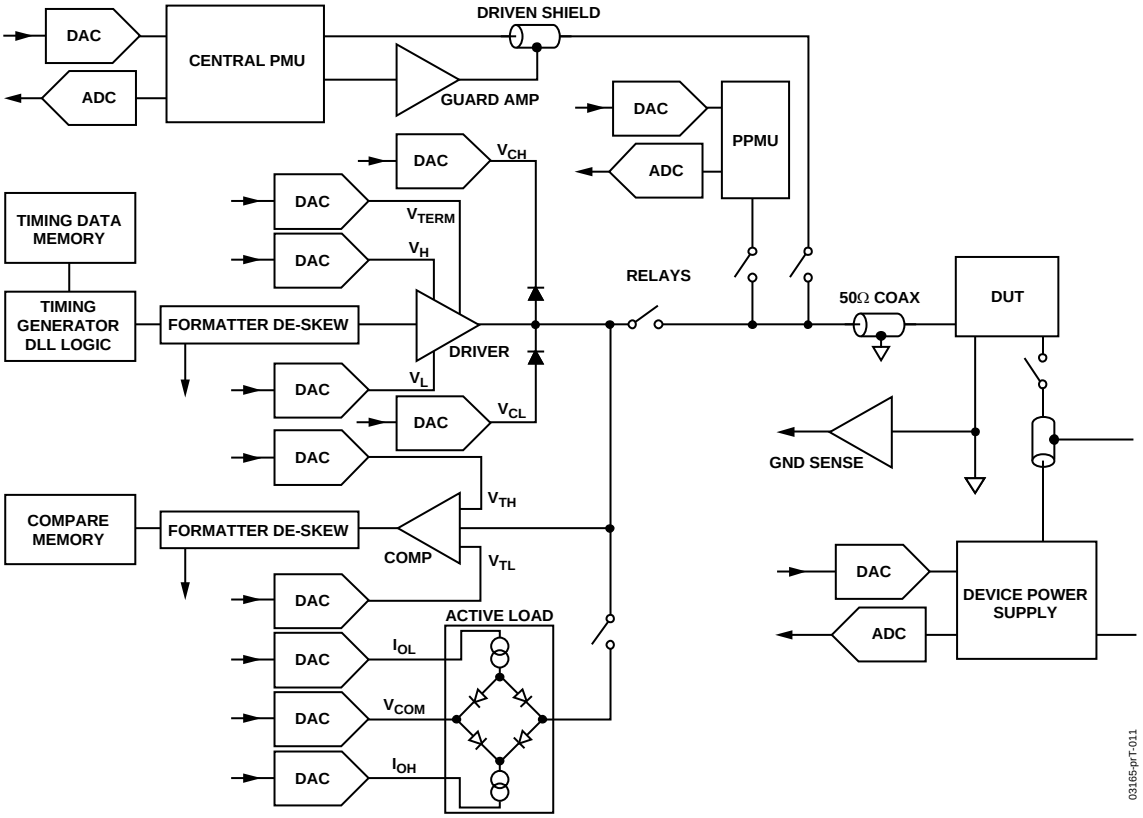
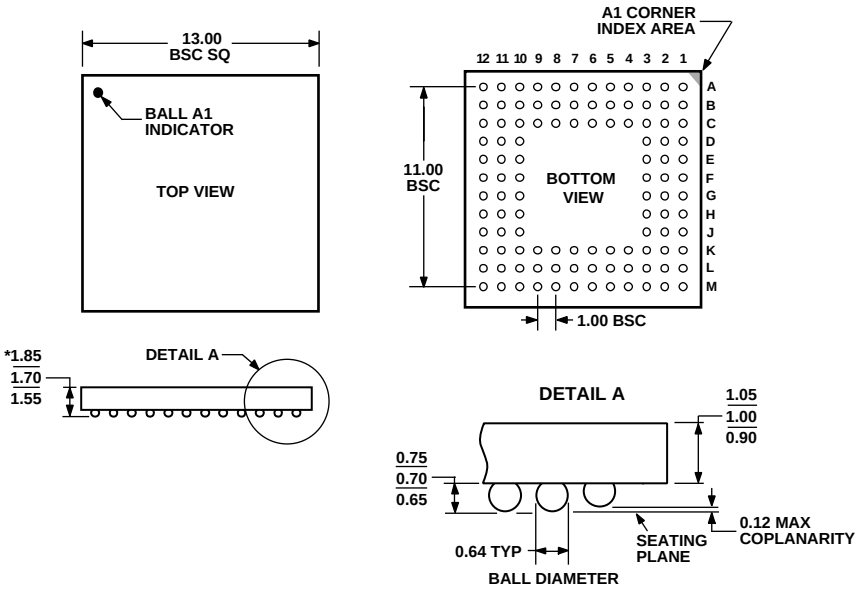


Figure 22. Typical Application Circuit for Logic Tester

OUTLINE DIMENSIONS



*COMPLIANT WITH JEDEC STANDARDS MO-192-AAD-1
EXCEPT FOR PACKAGE HEIGHT (DIMENSION A).

Figure 23. 108-Lead Chip Scale Ball Grid Array [CSPBGA]
(BC-108)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSBs)	Package Description	Package Option
AD5379ABC	−40°C to +85°C	±3	108-Lead CSPBGA	BC-108
EVAL-AD5379EB			Evaluation Board and Software	

D03165–0–4/04(0)