FINAL

Am28F256A

256 Kilobit (32 K x 8-Bit)
CMOS 12.0 Volt, Bulk Erase Flash Memory with Embedded Algorithms

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - — Access times as fast as 70 ns
- **CMOS low power consumption**
  - — 30 mA maximum active current
  - — 100 µA maximum standby current
  - — No data retention power consumption
- **Compatible with JEDEC-standard byte-wide 32-Pin EPROM pinouts**
  - — 32-pin PDIP
  - — 32-pin PLCC
  - — 32-pin TSOP
- **100,000 write/erase cycles minimum**
- **Write and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to V_{CC} +1 V**
- **Embedded Erase Electrical Bulk Chip-Erase**
  - — 1.5 seconds typical chip-erase including pre-programming
- **Embedded Program**
  - — 14 µs typical byte-program including time-out
  - — 0.5 second typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - — Low cost single transistor memory cell
- **Embedded algorithms for completely self-timed write/erase operations**

GENERAL DESCRIPTION

The Am28F256A is a 256 K Flash memory organized as 32 Kbytes of 8 bits each. AMD's Flash memories offer the most cost-effective and reliable read/write non- volatile random access memory. The Am28F256A is packaged in 32-pin PDIP, PLCC, and TSOP versions. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers. The Am28F256A is erased when shipped from the factory.

The standard Am28F256A offers access times as fast as 70 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F256A has separate chip enable (CE#) and output enable (OE#) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F256A uses a command register to manage this functionality, while maintaining a standard JEDEC Flash Standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming.

AMD's Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F256A uses a 12.0V±5% V_{PP} high voltage input to perform the erase and programming functions.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to V_{CC} +1 V.

Embedded Program

The Am28F256A is byte programmable using the Embedded Programming algorithm. The Embedded Programming algorithm does not require the system to time-out or verify the data programmed. The typical room temperature programming time of the Am28F256A is one half second.

Embedded Erase

The entire chip is bulk erased using the Embedded Erase algorithm. The Embedded Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are

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controlled internal to the device. Typical erasure at room temperature is accomplished in 1.5 seconds, including preprogramming.

AMD's Am28F256A is entirely pin and software compatible with AMD's Am28F020A, Am28F256A and Am28F512A Flash memories.

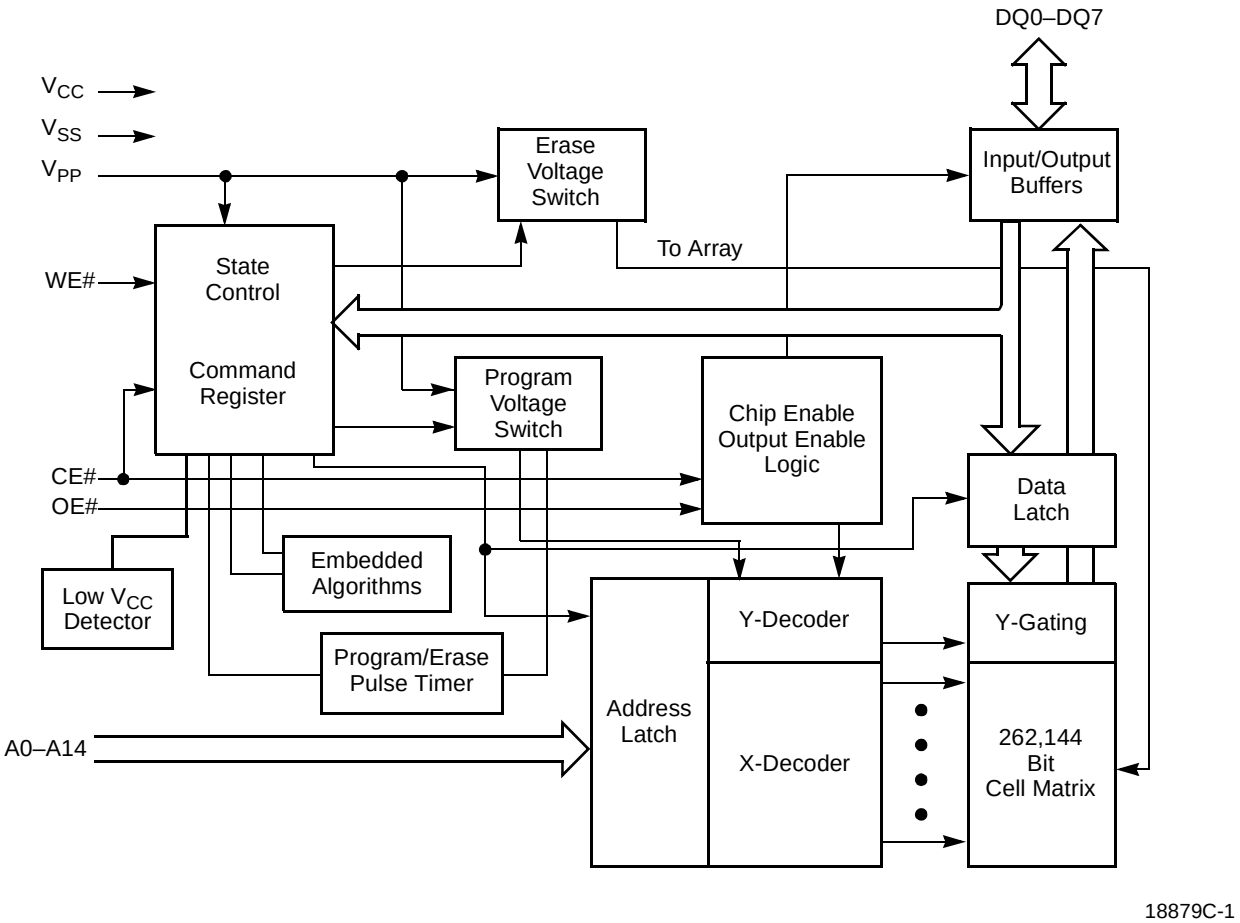
Comparing Embedded Algorithms with Flasherase and Flashrite Algorithms

	Am28F256A with Embedded Algorithms	Am28F256 using AMD Flashrite and Flasherase Algorithms
Embedded Programming Algorithm vs. Flashrite Programming Algorithm	AMD's Embedded Programming algorithm requires the user to only write a program set-up command and a program command (program data and address). The device automatically times the programming pulse width, verifies the programming, and counts the number of sequences. A status bit, Data# Polling, provides the user with the programming operation status.	The Flashrite Programming algorithm requires the user to write a program set-up command, a program command, (program data and address), and a program verify command, followed by a read and compare operation. The user is required to time the programming pulse width in order to issue the program verify command. An integrated stop timer prevents any possibility of overprogramming. Upon completion of this sequence, the data is read back from the device and compared by the user with the data intended to be written; if there is not a match, the sequence is repeated until there is a match or the sequence has been repeated 25 times.
Embedded Erase Algorithm vs. Flasherase Erase Algorithm	AMD's Embedded Erase algorithm requires the user to only write an erase set-up command and erase command. The device automatically pre-programs and verifies the entire array. The device then automatically times the erase pulse width, verifies the erase operation, and counts the number of sequences. A status bit, Data# Polling, provides the user with the erase operation status.	The Flasherase Erase algorithm requires the device to be completely programmed prior to executing an erase command. To invoke the erase operation, the user writes an erase set-up command, an erase command, and an erase verify command. The user is required to time the erase pulse width in order to issue the erase verify command. An integrated stop timer prevents any possibility of overerasure. Upon completion of this sequence, the data is read back from the device and compared by the user with erased data. If there is not a match, the sequence is repeated until there is a match or the sequence has been repeated 1,000 times.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F256A is designed to support either WE# or CE# controlled writes. During a system write cycle, addresses are latched on the falling edge of WE# or CE# whichever occurs last. Data is latched on the rising edge of WE# or CE# whichever occurs first. To simplify the following discussion, the WE# pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the WE# signal.

AMD's Flash technology combines years of EPROM and EEPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F256A electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

BLOCK DIAGRAM

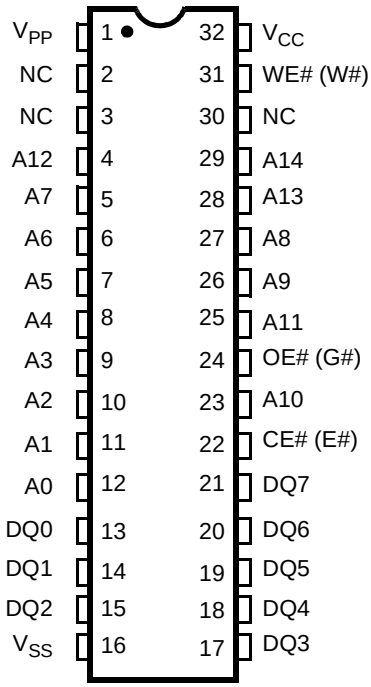


PRODUCT SELECTOR GUIDE

Family Part Number	**Am28F256A**				
Speed Options (V_{CC} = 5.0 V ±10%)	**-70**	**-90**	**-120**	**-150**	**-200**
Max Access Time (ns)	70	90	120	150	200
CE# (E#) Access (ns)	70	90	120	150	200
OE# (G#) Access (ns)	35	35	50	55	55

CONNECTION DIAGRAMS

PDIP



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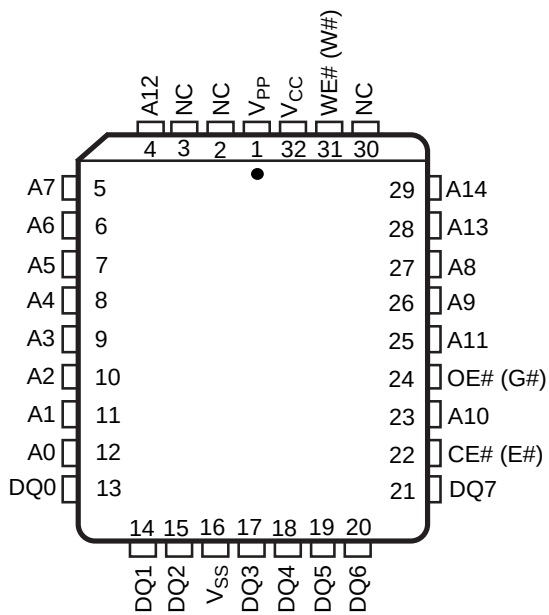
PLCC



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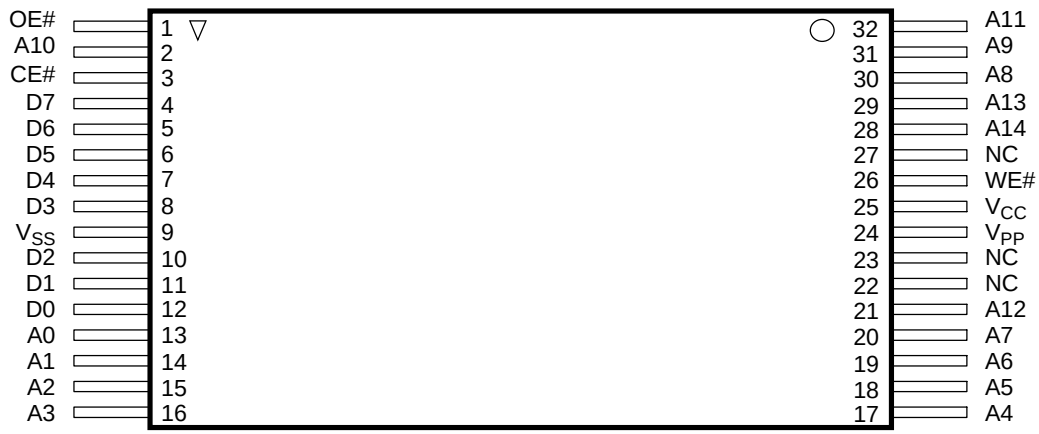
Note: *Pin 1 is marked for orientation.*

CONNECTION DIAGRAMS (continued)

32-Pin — Standard Pinout



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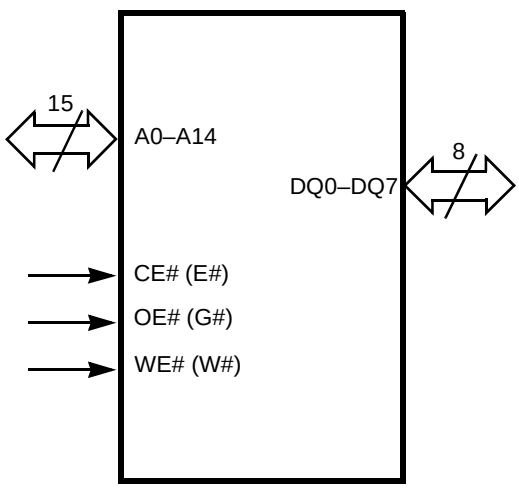
32-Pin — Reverse Pinout

LOGIC SYMBOL



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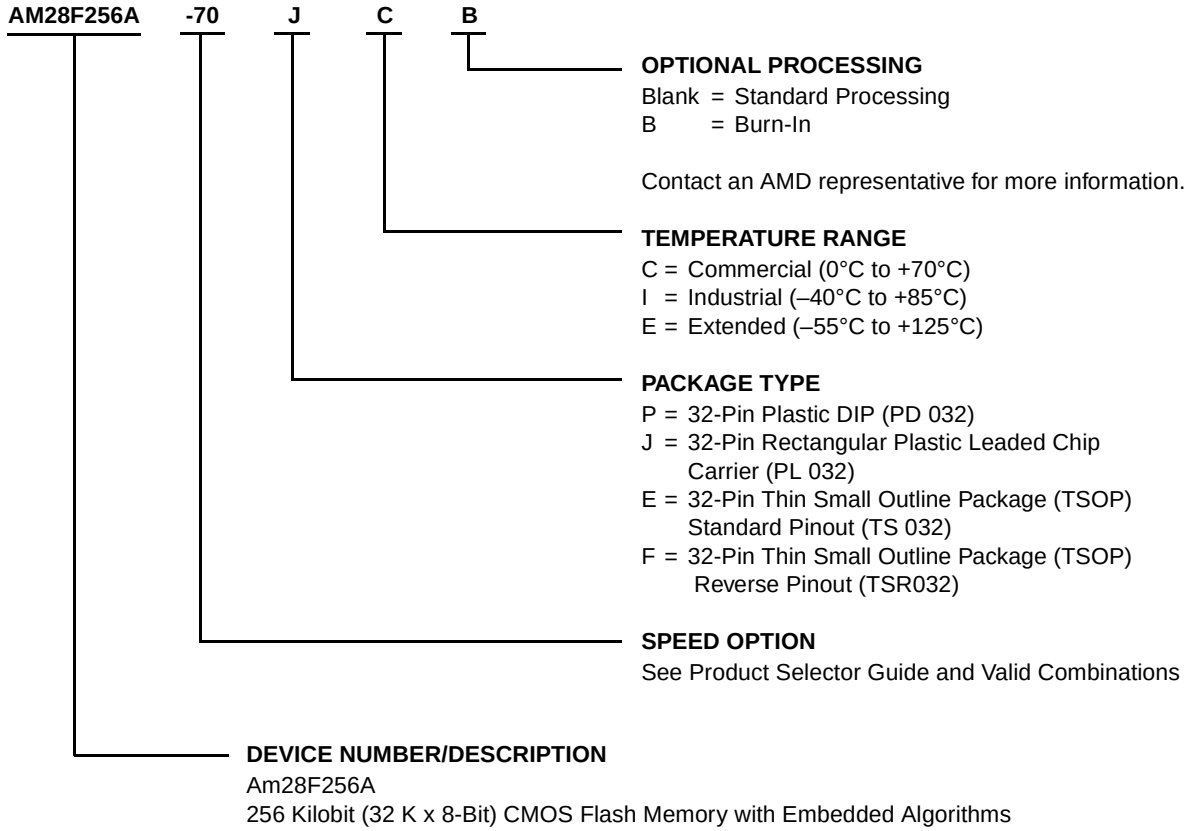
ORDERING INFORMATION

Standard Products



Valid Combinations	
AM28F256A-70 AM28F256A-90 AM28F256A-120 AM28F256A-150 AM28F256A-200	PC, PI, PE, JC, JI, JE, EC, EI, EE, FC, FI, FE

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

A0–A14

Address Inputs for memory locations. Internal latches hold addresses during write cycles.

CE# (E#)

Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.

DQ0-DQ7

Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

NC

No Connect-corresponding pin is not connected internally to the die.

OE# (G#)

Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles. Output Enable is high during command sequencing and program/erase operations.

V_{CC}

Power supply for device operation. (5.0 V ± 5% or 10%)

V_{PP}

Program voltage input. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC}$ +2 V.

V_{SS}

Ground.

WE# (W)

Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse. Write Enable high inhibits writing to the device.

BASIC PRINCIPLES

This section contains descriptions about the device read, erase, and program operations, and write operation status of the Am29FxxxA, 12.0 volt family of Flash devices. References to some tables or figures may be given in generic form, such as “Command Definitions table”, rather than “Table 1”. Refer to the corresponding data sheet for the actual table or figure.

The Am28FxxxA family uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0 V ± 5% high voltage input.

Read Only Memory

Without high V_{PP} voltage, the device functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The device’s command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the device is designed to support either WE# or CE# controlled writes. During a system write cycle, addresses are latched on the falling edge of WE# or CE# whichever occurs last. Data is latched on the rising edge of WE# or CE# whichever occur first. To simplify the following discussion, the WE# pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the WE# signal.

OVERVIEW OF ERASE/PROGRAM OPERATIONS

Embedded Erase Algorithm

AMD now makes erasure extremely simple and reliable. The Embedded Erase algorithm requires the user to only write an erase setup command and erase command. The device will automatically pre-program and verify the entire array. The device automatically times the erase pulse width, provides the erase verify and counts the number of sequences. A status bit, Data# Polling, provides feedback to the user as to the status of the erase operation.

Embedded Programming Algorithm

AMD now makes programming extremely simple and reliable. The Embedded Programming algorithm requires the user to only write a program setup command and a program command. The device automatically times the programming pulse width, provides the program verify and counts the number of sequences. A status bit, Data# Polling, provides feedback to the user as to the status of the programming operation.

DATA PROTECTION

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. The device powers up in its read only state. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, the device locks out write cycles for $V_{CC} < V_{LKO}$ (see DC characteristics section for voltages). When $V_{CC} < V_{LKO}$, the command register is disabled, all internal program/erase circuits are disabled, and the device resets to the read mode. The device ignores all writes until $V_{CC} > V_{LKO}$. The user must ensure that the control pins are in the correct logic state when $V_{CC} > V_{LKO}$ to prevent unintentional writes.

Write Pulse “Glitch” Protection

Noise pulses of less than 10 ns (typical) on OE#, CE# or WE# will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of OE# = V_{IL}, CE#=V_{IH} or WE# = V_{IH}. To initiate a write cycle CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

Power-up of the device with WE# = CE# = V_{IL} and OE# = V_{IH} will not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

FUNCTIONAL DESCRIPTION

Description Of User Modes

Table 1. Am28F256A Device Bus Operations (Notes 7 and 8)

Operation		CE# (E#)	OE# (G#)	WE# (W#)	V_{PP} (Note 1)	A0	A9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A0	A9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01h)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (2Fh)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A0	A9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A0	A9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels. $V_{PPL} = V_{PP} < V_{CC} + 2$ V. See DC Characteristics for voltage levels of V_{PPH}. 0 V < An < V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. *V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} + 2.0 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.*
2. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.*
3. *11.5 < V_{ID} < 13.0 V. Minimum V_{ID} rise time and fall time (between 0 and V_{ID} voltages) is 500 ns.*
4. *Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.*
5. *With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).*
6. *Refer to Table 3 for valid D_{IN} during a write operation.*
7. *All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.*
8. *If $V_{CC} \leq$ 1.0 Volt, the voltage difference between V_{PP} and V_{CC} should not exceed 10.0 volts. Also, the Am28F256 has a V_{PP} rise time and fall time specification of 500 ns minimum.*

READ-ONLY MODE

When V_{PP} is less than V_{CC} + 2 V, the command register is inactive. The device can either read array or autoselect data, or be standby mode.

Read

The device functions as a read only memory when V_{PP} < V_{CC} + 2 V. The device has two control functions. Both must be satisfied in order to output data. CE# controls power to the device. This pin should be used for specific device selection. OE# controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable CE# to valid data at the output pins. The output enable access time is the delay from the falling edge of OE# to valid data at the output pins (assuming the addresses have been stable at least t_{ACC} - t_{OE}).

Standby Mode

The device has two standby modes. The CMOS standby mode (CE# input held at $V_{CC} \pm 0.5$ V), consumes less than 100 µA of current. TTL standby mode (CE# is held at V_{IH}) reduces the current requirements to less than 1 mA. When in the standby mode the outputs are in a high impedance state, independent of the OE# input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when OE# is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to V_{CC} + 2.0 V while using this Auto select mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the device the two bytes are given in the table 2 of the device data sheet. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

Table 2. Am28F256A Auto Select Code

Type	A0	Code (HEX)
Manufacturer Code	V_{IL}	01
Device Code	V_{IH}	2F

ERASE, PROGRAM, AND READ MODE

When V_{PP} is equal to 12.0 V ± 5%, the command register is active. All functions are available. That is, the device can program, erase, read array or autoselect data, or be standby mode.

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing WE# and CE# to V_{IL}, while OE# is at V_{IH}. Addresses are latched on the falling edge of WE#, while data is latched on the rising edge of the WE# pulse. Standard microprocessor write timings are used.

The device requires the OE# pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, OE# must be V_{IH}, and CE# and WE# must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00h (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 3 in the device data sheet defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00h into the command register. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00h (read mode) upon V_{PP} power-up. The 00h (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Am28F256A Command Definitions

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 4)	Write	X	00h/FFh	Read	RA	RD
Read Auto select	Write	X	80h or 90h	Read	00h/01h	01h/2Fh
Embedded Erase Set-up/ Embedded Erase	Write	X	30h	Write	X	30h
Embedded Program Set-up/ Embedded Program	Write	X	10h or 50h	Write	PA	PD
Reset (Note 4)	Write	X	00h/FFh	Write	X	00h/FFh

Notes:

1. *Bus operations are defined in Table 1.*
2. *RA = Address of the memory location to be read.*
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the WE# pulse.
   X = Don't care.
3. *RD = Data read from location RA during read operation.*
   PD = Data to be programmed at location PA. Data latched on the rising edge of WE#.
4. *Please reference Reset Command section.*

FLASH MEMORY PROGRAM/ERASE OPERATIONS

Embedded Erase Algorithm

The automatic chip erase does not require the device to be entirely pre-programmed prior to executing the Embedded set-up erase command and Embedded erase command. Upon executing the Embedded erase command the device automatically will program and verify the entire memory for an all zero data pattern. The system is *not* required to provide any controls or timing during these operations.

When the device is automatically verified to contain an all zero pattern, a self-timed chip erase and verify begin. The erase and verify operation are complete when the data on DQ7 is “1" (see Write Operation Status section) atwhich time the device returns to Read mode. The system is not required to provide any control or timing during these operations.

When using the Embedded Erase algorithm, the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Embedded Erase Set-Up command is a command only operation that stages the device for automatic electrical erasure of all bytes in the array. Embedded Erase Setup is performed by writing 30h to the command register.

To commence automatic chip erase, the command 30h must be written again to the command register. The automatic erase begins on the rising edge of the WE and terminates when the data on DQ7 is “1" (see Write Operation Status section) at which time the device returns to Read mode.

Figure 1 and Table 4 illustrate the Embedded Erase algorithm, a typical command string and bus operation.

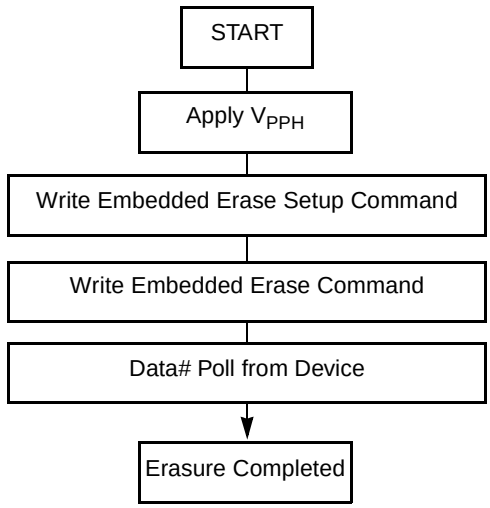


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Figure 1. Embedded Erase Algorithm

Table 4. Embedded Erase Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (see Note)
Write	Embedded Erase Setup Command	Data = 30h
	Embedded Erase Command	Data = 30h
Read		Data# Polling to Verify Erasure
Standby		Compare Output to FFh
Read		Available for Read Operations

Note: *See AC and DC Characteristics for values of V_{PP} parameters. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Functional Description.*

Embedded Programming Algorithm

The Embedded Program Setup is a command only operation that stages the device for automatic programming. Embedded Program Setup is performed by writing 10h or 50h to the command register.

Once the Embedded Setup Program operation is performed, the next WE# pulse causes a transition to an active programming operation. Addresses are latched on the falling edge of CE# or WE# pulse, whichever happens later. Data is latched on the rising edge of WE# or CE#, whichever happens first. The rising edge of WE# also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin. The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to Read mode.

Figure 2 and Table 5 illustrate the Embedded Program algorithm, a typical command string, and bus operation.

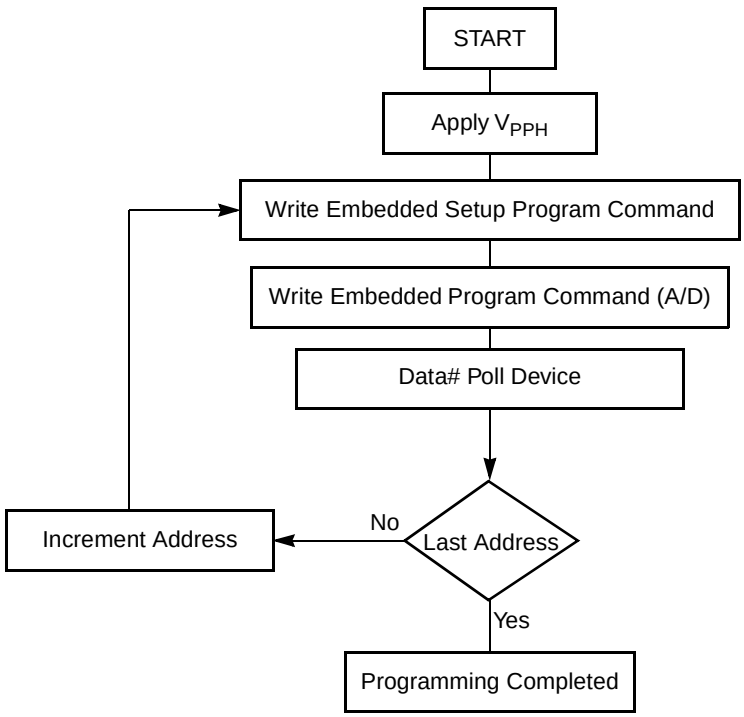

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Figure 2. Embedded Programming Algorithm

Table 5. Embedded Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (see Note)
Write	Embedded Program Setup Command	Data = 10h or 50h
Write	Embedded Program Command	Valid Address/Data
Read		Data# Polling to Verify Completion
Read		Available for Read Operations

Note: *See AC and DC Characteristics for values of V_{PP} parameters. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Functional Description. Device is either powered-down, erase inhibit or program inhibit.*

Write Operation Status

Data Polling—DQ7

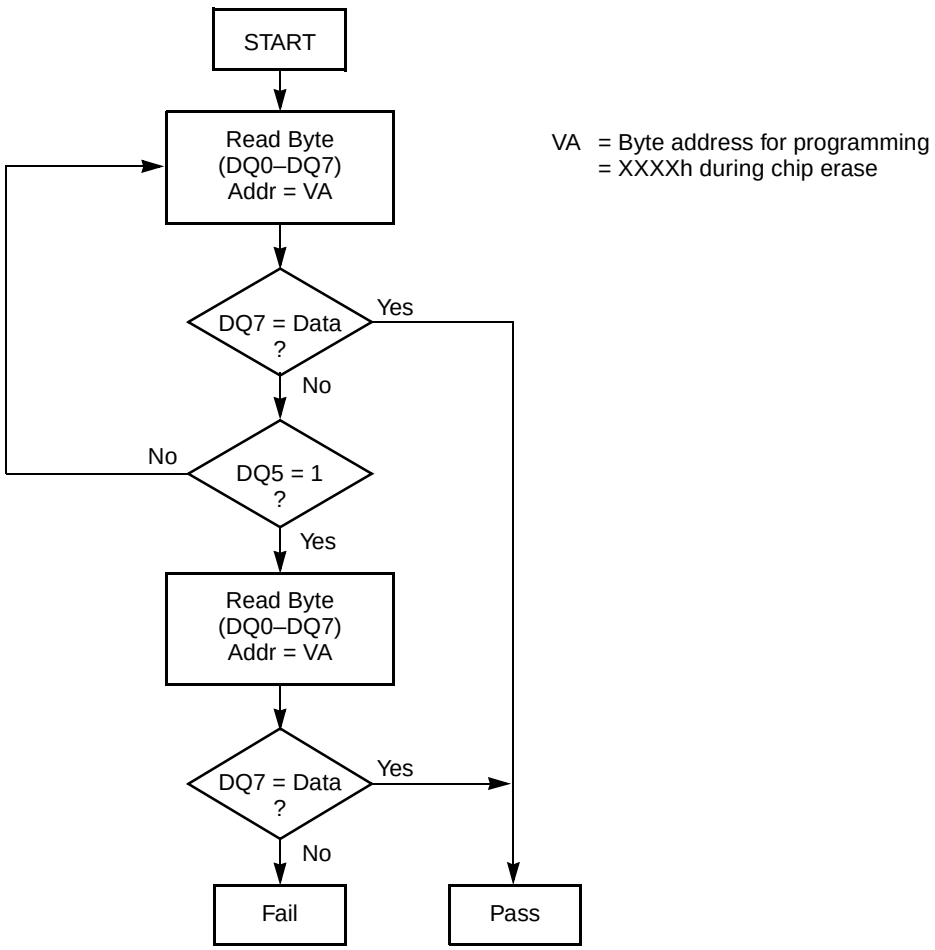
The device features Data# Polling as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Programming algorithm is in operation, an attempt to read the device at a valid address will produce the complement of expected Valid data on DQ7. Upon completion of the Embedded Program algorithm an attempt to read the device at a valid address will produce Valid data on DQ7. The Data# Polling feature is valid after the rising edge of the second WE# pulse of the two write pulse sequence.

While the Embedded Erase algorithm is in operation, DQ7 will read “0" until the erase operation is completed. Upon completion of the erase operation, the data on DQ7 will read “1.” The Data# Polling feature is valid after the rising edge of the second WE# pulse of the two Write pulse sequence.

The Data# Polling feature is only active during Embedded Programming or erase algorithms.

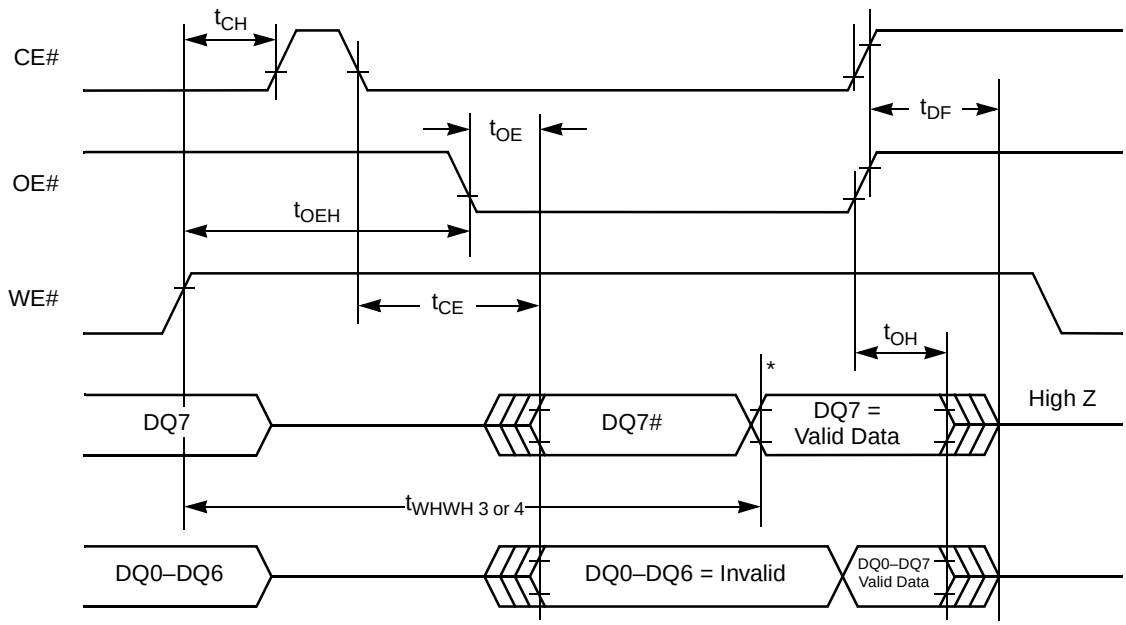
See Figures 3 and 4 for the Data# Polling timing specifications and diagrams. Data# Polling is the standard method to check the write operation status, however, an alternative method is available using Toggle Bit.



18879C-8

Note:
DQ7 is rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5 or after DQ5.

Figure 3. Data# Polling Algorithm



18879C-9

**DQ7 = Valid Data (The device has completed the Embedded operation.)*

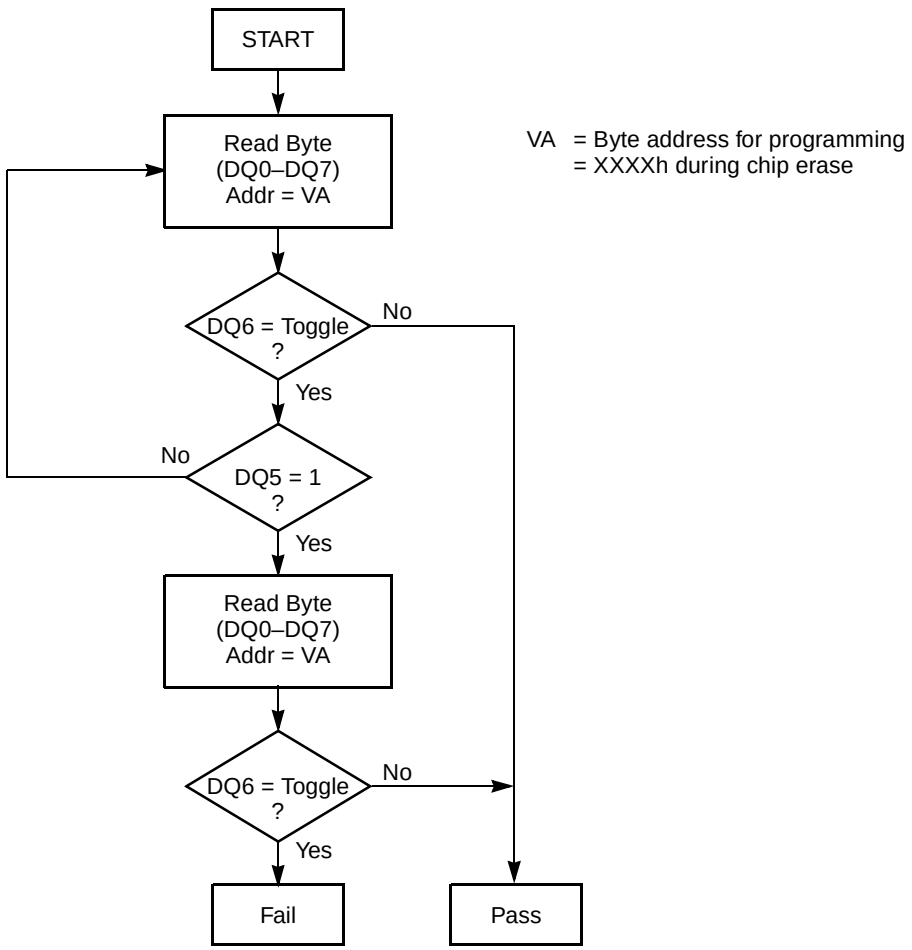
Figure 4. AC Waveforms for Data# Polling during Embedded Algorithm Operations

Toggle Bit—DQ6

The device also features a “Toggle Bit” as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

Successive attempts to read data from the device at a valid address, while the Embedded Program algorithm is in progress, or at any address while the Embedded Erase algorithm is in progress, will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase algorithm is completed, DQ6 will stop toggling to indicate the completion of either Embedded operation. Only on the next read cycle will valid data be obtained. The toggle bit is valid after the rising edge of the first WE# pulse of the two write pulse sequence, unlike Data# Polling which is valid after the rising edge of the second WE# pulse. This feature allows the user to determine if the device is partially through the two write pulse sequence.

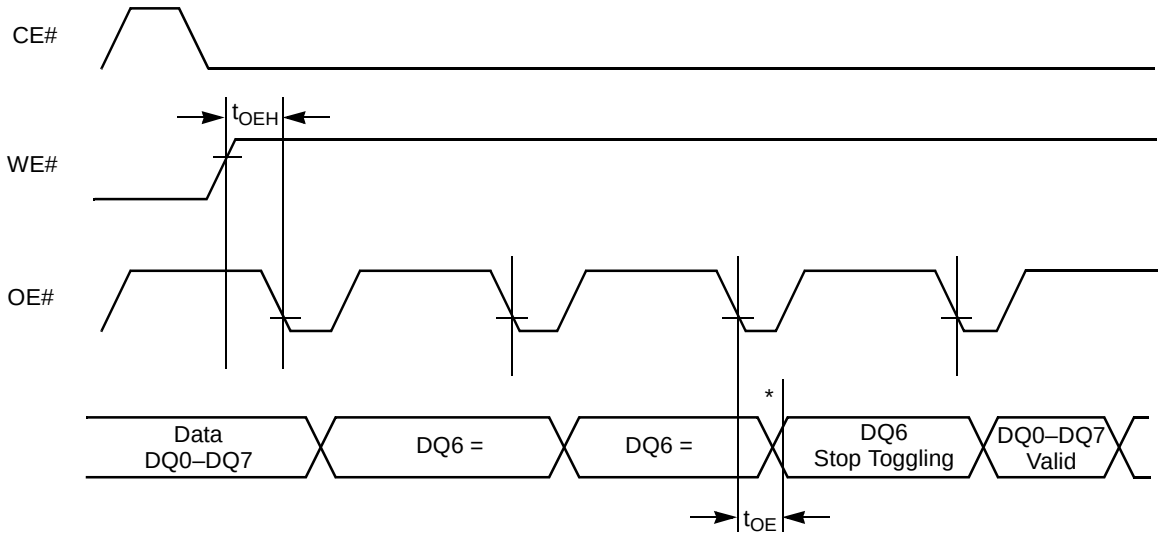
See Figures 5 and 6 for the Toggle Bit timing specifications and diagrams.



18879C-10

Note:
DQ6 is rechecked even if DQ5 = “1” because DQ6 may stop toggling at the same time as DQ5 changing to “1”.

Figure 5. Toggle Bit Algorithm



18879C-11

Note:

**DQ6 stops toggling (The device has completed the Embedded operation.)*

Figure 6. AC Waveforms for Toggle Bit during Embedded Algorithm Operations

DQ5

Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits. This is a failure condition and the device may not be used again (internal pulse count exceeded). Under these conditions DQ5 will produce a “1.” The program or erase cycle was not successfully completed. Data# Polling is the only operating function of the device under this condition. The CE# circuit will partially power down the device under these conditions (to approximately 2 mA). The OE# and WE# pins will control the output disable functions as described in the Command Definitions table in the corresponding device data sheet.

Parallel Device Erasure

The Embedded Erase algorithm greatly simplifies parallel device erasure. Since the erase process is internal to the device, a single erase command can be given to multiple devices concurrently. By implementing a parallel erase algorithm, total erase time may be minimized.

Note that the Flash memories may erase at different rates. If this is the case, when a device is completely erased, use a masking code to prevent further erasure (over-erasure). The other devices will continue to erase until verified. The masking code applied could be the read command (00h).

Power-Up/Power-Down Sequence

The device powers-up in the Read only mode. Power supply sequencing is not required. Note that if $V_{CC} \leq$ 1.0 Volt, the voltage difference between V_{PP} and V_{CC} should not exceed 10.0 Volts. Also, the device has a rise V_{PP} rise time and fall time specification of 500 ns minimum.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset must be written two consecutive times after the Setup Program command (10h or 50h). This will reset the device to the Read mode.

Following any other Flash command, write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The Setup Program command (10h or 50h) is the only command that requires a two-sequence reset cycle. The first Reset command is interpreted as program data. However, FFh data is considered as null data during programming operations (memory cells are only programmed from a logical “1" to “0"). The second Reset command safely aborts the programming operation and resets the device to the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the Setup Program state or not.

In-System Programming Considerations

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the circuit board.

Auto Select Command

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. In order to correctly program any Flash memories in-system, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The device contains an Auto Select operation to supplement traditional PROM programming methodologies. The operation is initiated by writing 80h or 90h into the command register. Following this command, a read cycle address 0000h retrieves the manufacturer code of 01h (AMD). A read cycle from address 0001h returns the device code (see the Auto Select Code table of the corresponding device data sheet). To terminate the operation, it is necessary to write another valid command, such as Reset (00h or FFh), into the register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C
Plastic Packages . . . . . –65°C to +125°C

Ambient Temperature
with Power Applied. . . . . .–55°C to + 125°C

Voltage with Respect To Ground
All pins except A9 and V_{PP}
(Note 1) . . . . . .–2.0 V to +7.0 V

V_{CC} (Note 1). . . . . .–2.0 V to +7.0 V

A9 (Note 2). . . . . .–2.0 V to +14.0 V

V_{PP} (Note 2). . . . . .–2.0 V to +14.0 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V. During voltage transitions, input and I/O pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A9 and V_{PP} pins is –0.5 V. During voltage transitions, A9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 and V_{PP} is +13.0 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . .0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . .–40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A) . . . . . .–55°C to +125°C

V_{CC} Supply Voltages

V_{CC} . . . . . +4.50 V to +5.50 V

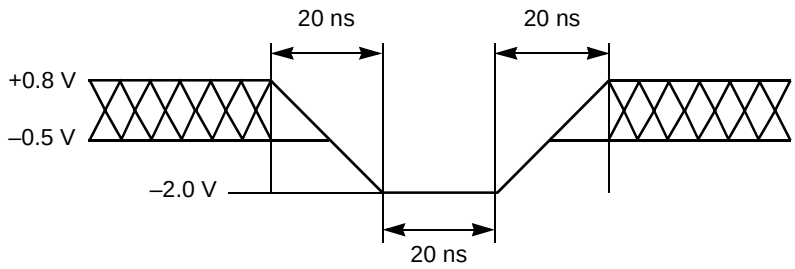
V_{PP} Voltages

Read . . . . . –0.5 V to +12.6 V

Program, Erase, and Verify . . . . . +11.4 V to +12.6 V

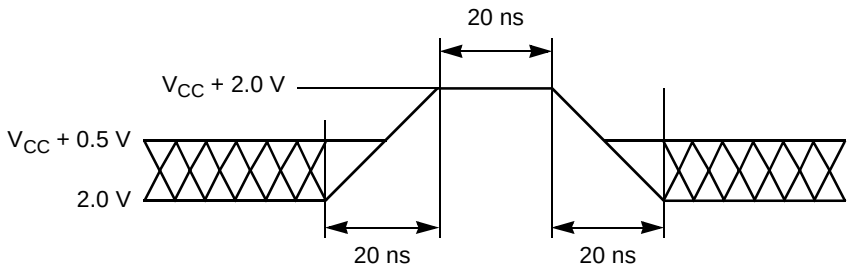
Operating ranges define those limits between which the functionality of the device is guaranteed.

MAXIMUM OVERSHOOT



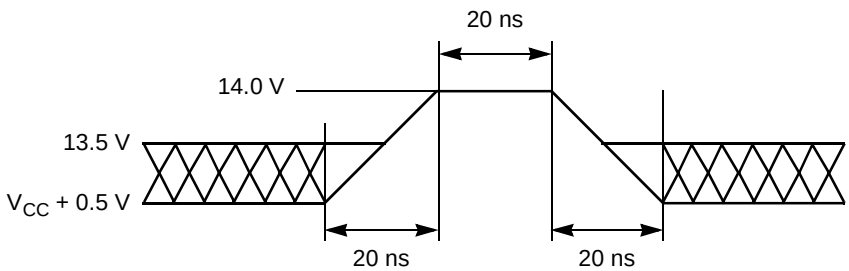
18879C-12

Maximum Negative Input Overshoot



18879C-13

Maximum Positive Input Overshoot



18879C-14

Maximum V_{PP} Overshoot

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1-4)

TTL/NMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, CE# = V_{IH}		0.2	1.0	mA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, CE# = V_{IL}, OE# = V_{IH} I_{OUT} = 0 mA, at 6 MHz		20	30	mA
I_{CC2}	V_{CC} Programming Current	CE# = V_{IL} Programming in Progress (Note 4)		20	30	mA
I_{CC3}	V_{CC} Erase Current	CE# = V_{IL} Erasure in Progress (Note 4)		20	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			±1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
		$V_{PP} = V_{PPL}$			±1.0	
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA, $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min	2.4			V
V_{ID}	A9 Auto Select Voltage	A9 = V_{ID}	11.5		13.0	V
I_{ID}	A9 Auto Select Current	A9 = V_{ID} Max, $V_{CC} = V_{CC}$ Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:*** *Erase/Program are inhibited when $V_{PP} = V_{PPL}$*	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2	3.7		V

Notes:

1. ***Caution:*** *The Am28F256A must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied. If V_{CC} ð 1.0 volt, the voltage difference between V_{PP} and V_{CC} should not exceed 10.0 volts. Also, the Am28F256A has a V_{PP} rise time and fall time specification of 500 ns minimum.*
2. *I_{CC1} is tested with OE# = V_{IH} to simulate open outputs.*
3. *Maximum active power usage is the sum of I_{CC} and I_{PP}*
4. *Not 100% tested.*

DC CHARACTERISTICS

CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, CE# = V_{CC} ±0.5 V		15	100	µA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, CE# = V_{IL}, OE# = V_{IH} I_{OUT} = 0 mA, at 6 MHz		20	30	mA
I_{CC2}	V_{CC} Programming Current	CE# = V_{IL} Programming in Progress (Note 4)		20	30	mA
I_{CC3}	V_{CC} Erase Current	CE# = V_{IL} Erasure in Progress (Note 4)		20	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			±1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA, $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min	0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC}$ Min	V_{CC} –0.4			
V_{ID}	A9 Auto Select Voltage	A9 = V_{ID}	11.5		13.0	V
I_{ID}	A9 Auto Select Current	A9 = V_{ID} Max, $V_{CC} = V_{CC}$ Max		5	50	µA
V_{PPL}	V_{PPL} during Read-Only Operations	***Note:*** *Erase/Program are inhibited when $V_{PP} = V_{PPL}$*	0.0		V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2	3.7		V

Notes:

1. ***Caution:*** *The Am28F256A must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied. If V_{CC} ð 1.0 volt, the voltage difference between V_{PP} and V_{CC} should not exceed 10.0 volts. Also, the Am28F256A has a V_{PP} rise time and fall time specification of 500 ns minimum.*
2. *I_{CC1} is tested with OE# = V_{IH} to simulate open outputs.*
3. *Maximum active power usage is the sum of I_{CC} and I_{PP}*
4. *Not 100% tested.*

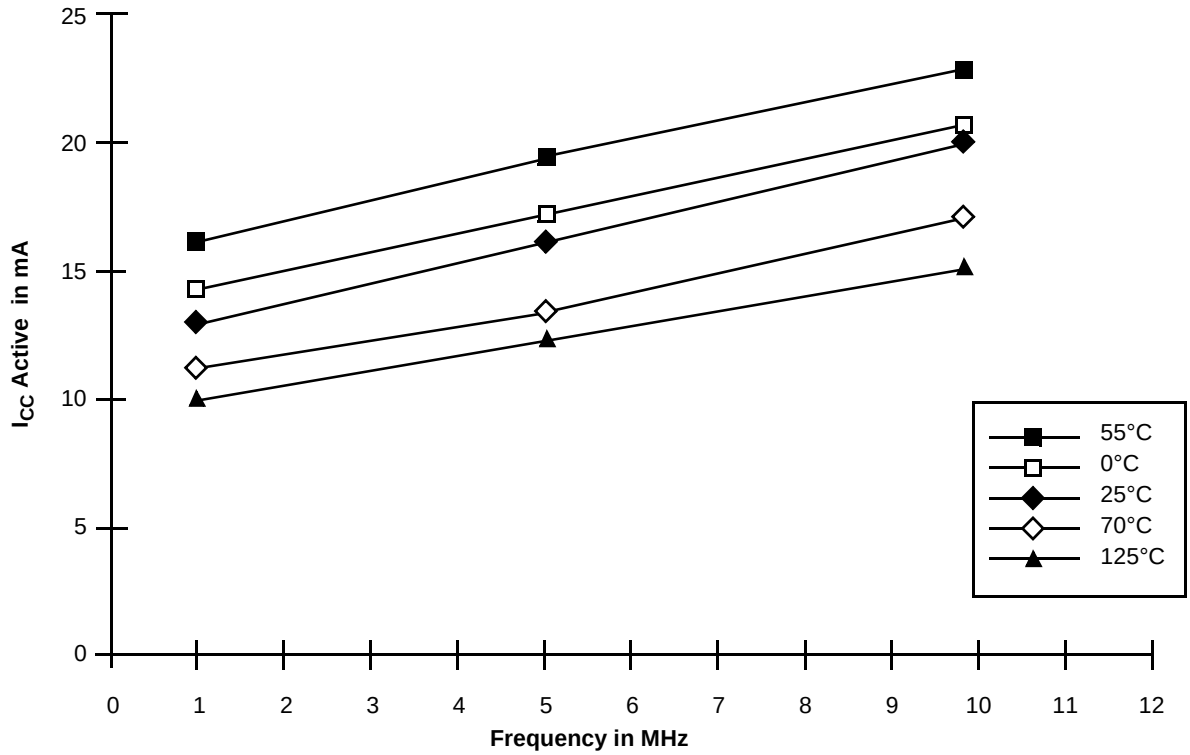


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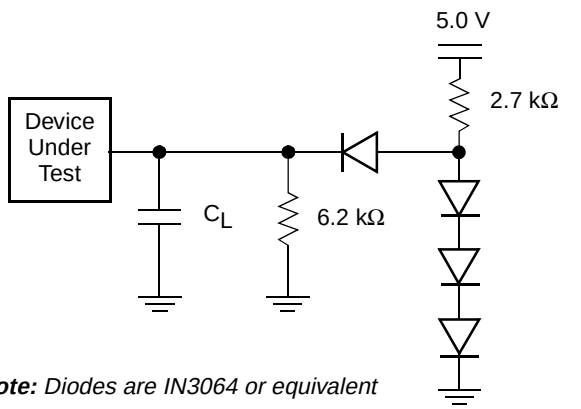
Figure 7. Am28F256A—Average I_{CC} Active vs. Frequency

V_{CC} = 5.5 V, Addressing Pattern = Minmax
Data Pattern = Checkerboard

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

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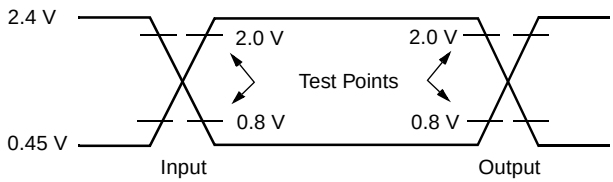
Figure 8. Test Setup

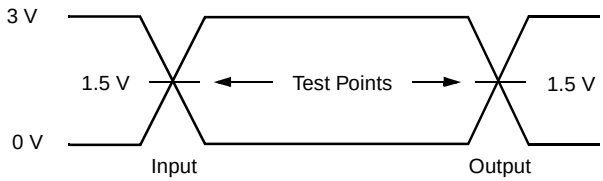
Table 6. Test Specifications

Test Condition	-70	All others	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	≤10		ns
Input Pulse Levels	0.0–3.0	0.45–2.4	V
Input timing measurement reference levels	1.5	0.8, 2.0	V
Output timing measurement reference levels	1.5	0.8, 2.0	V

SWITCHING TEST WAVEFORMS



AC Testing (all speed options except -70): Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤10 ns.



AC Testing for -70 devices: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤10 ns.

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SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AC Characteristics—Read Only Operation

Parameter Symbols		Parameter Description		Am28F256A Speed Options					Unit
JEDEC	Standard			-70	-90	-120	-150	-200	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 2)	Min	70	90	120	150	200	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	Max	70	90	120	150	200	ns
t_{AVQV}	t_{ACC}	Address Access Time	Max	70	90	120	150	200	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Max	35	35	50	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z (Note 2)	Min	0	0	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z (Note 1)	Max	20	20	30	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z (Note 2)	Min	0	0	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z (Note 2)	Max	20	20	30	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, CE#, or OE# Change (Note 2)	Min	0	0	0	0	0	ns
t_{VCS}		V_{CC} Setup Time to Valid Read (Note 2)	Min	50	50	50	50	50	µs

Notes:

1. *Guaranteed by design not tested.*
2. *Not 100% tested.*

AC Characteristics—Write/Erase/Program Operations

Parameter Symbols		Parameter Description		Am28F256A Speed Options					Unit
JEDEC	Standard			-70	-90	-120	-150	-200	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 4)	Min	70	90	120	150	200	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	45	50	60	75	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	45	45	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	10	10	10	10	10	ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm only	Min	10	10	10	10	10	ns
t_{GHWL}		Read Recovery Time before Write	Min	0	0	0	0	0	µs
t_{ELWLE}	t_{CSE}	Chip Enable Embedded Algorithm Setup Time	Min	20	20	20	20	20	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	45	45	50	60	60	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min	20	20	20	20	20	ns
t_{WHWH3}		Embedded Programming Operation (Note 2)	Min	14	14	14	14	14	µs
t_{WHWH4}		Embedded Erase Operation (Note 3)	Typ	5	5	5	5	5	sec
t_{VPEL}		V_{PP} Setup Time to Chip Enable LOW (Note 4)	Min	100	100	100	100	100	ns
t_{VCS}		V_{CC} Setup Time to Chip Enable LOW (Note 4)	Min	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 4)	Min	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 90% V_{PPL} (Note 4)	Min	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 4)	Min	100	100	100	100	100	ns

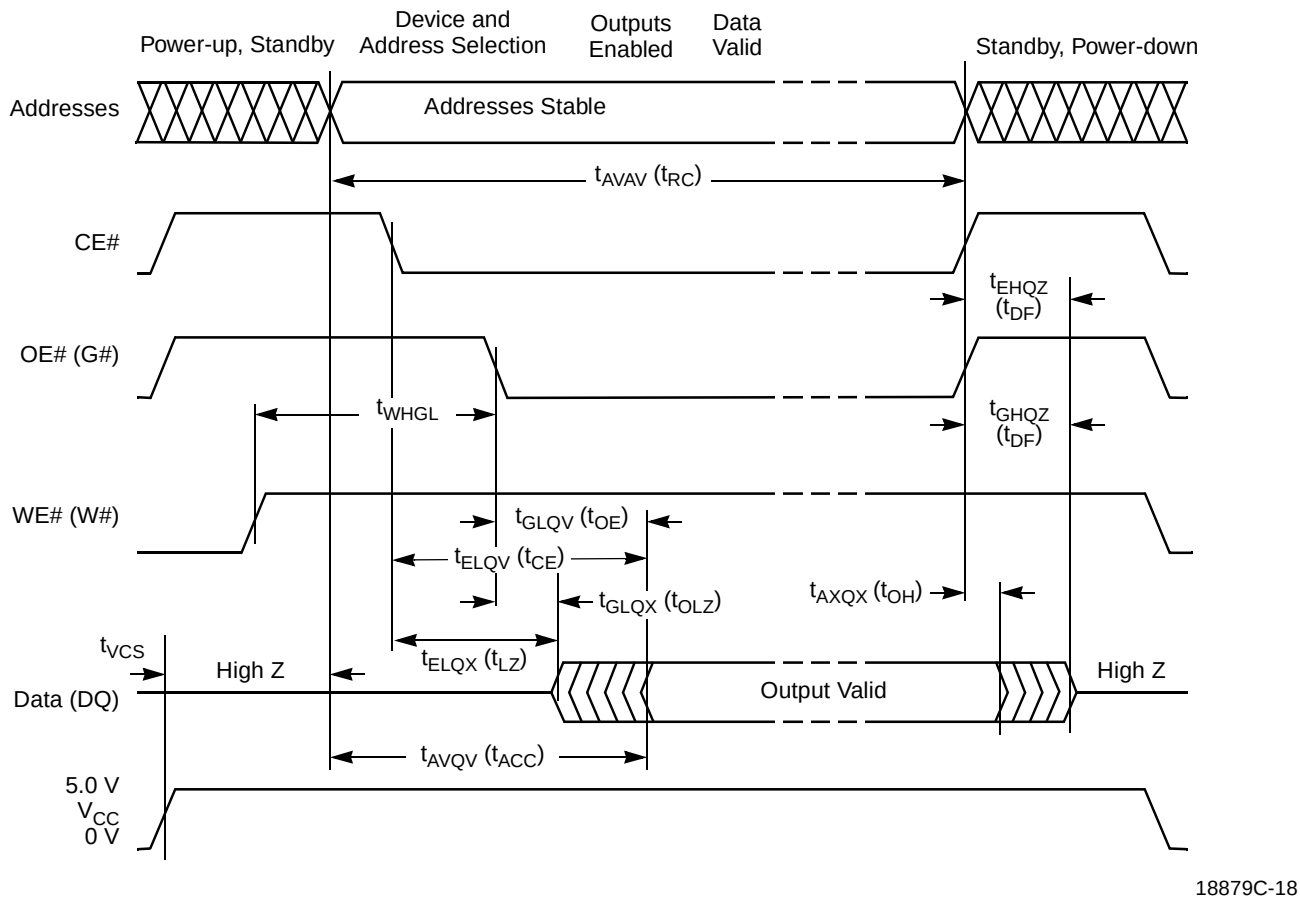
Notes:

1. *Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.*
2. *Embedded program operation of 14 µs consists of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.*
3. *Embedded erase operation of 5 sec consists of 4 sec array pre-programming time and 1 sec array erase time. This is a typical time for one embedded erase operation.*
4. *Not 100% tested.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

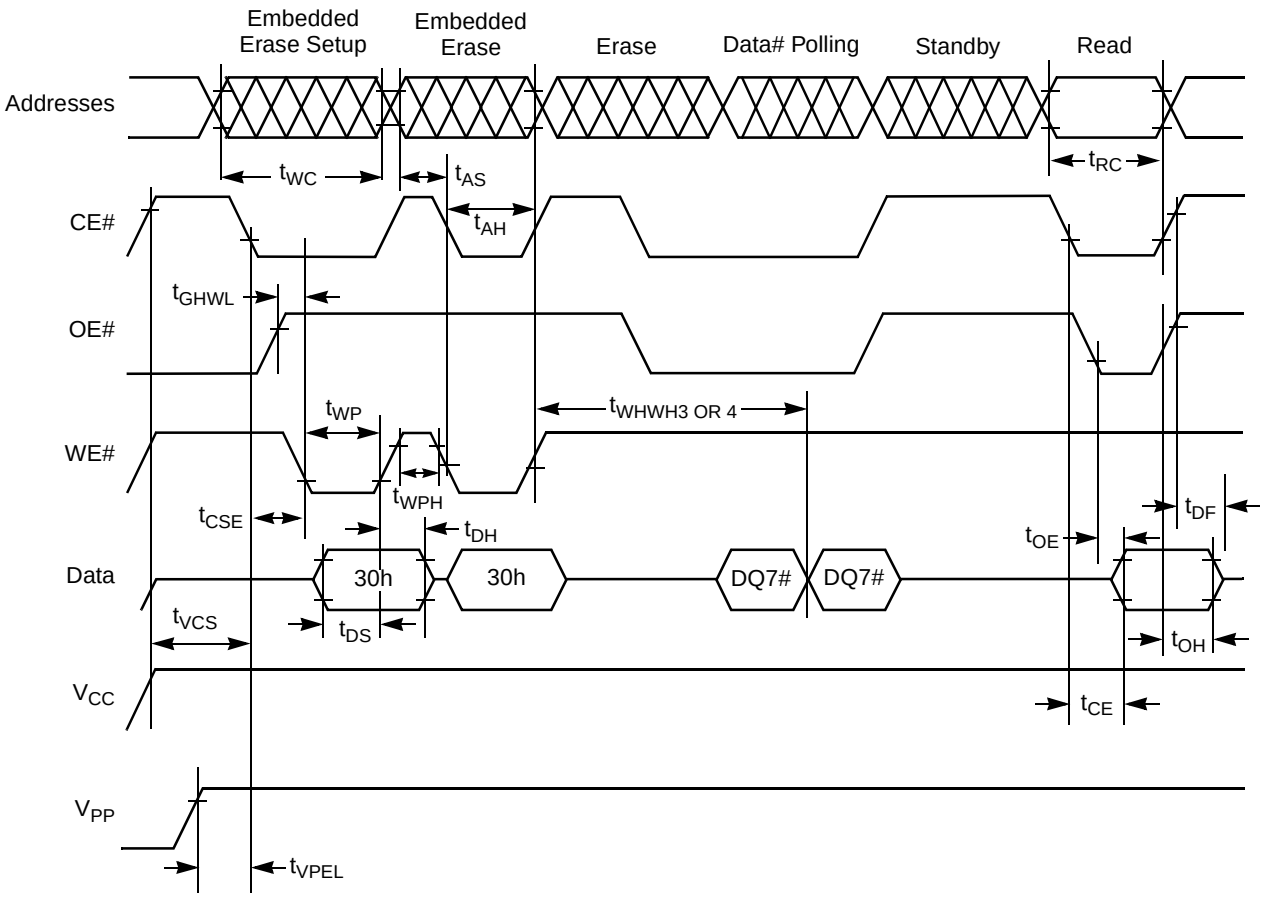
SWITCHING WAVEFORMS



18879C-18

Figure 9. AC Waveforms for Read Operations

SWITCHING WAVEFORMS

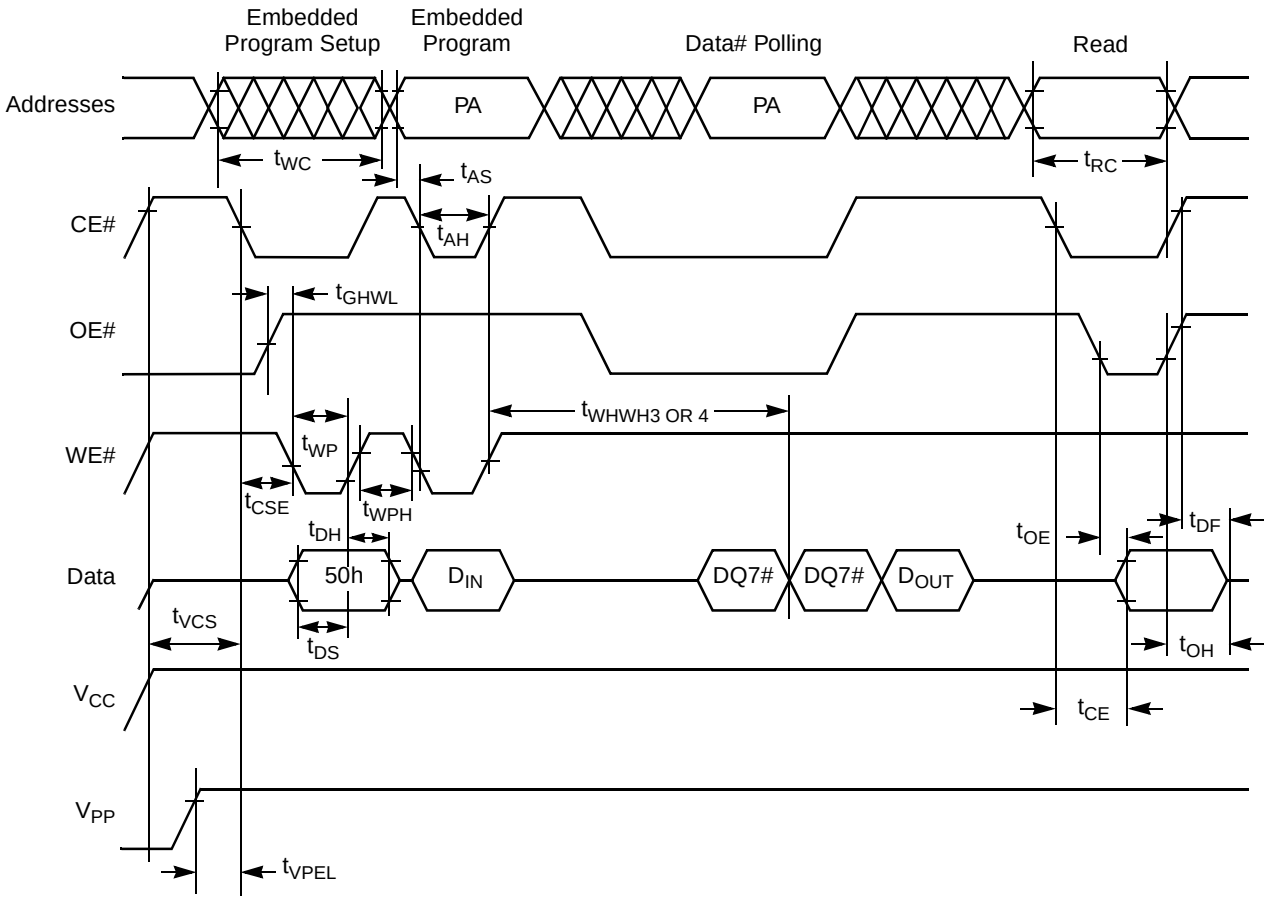


18879C-19

Note:
DQ7# is the complement of the data written to the device.

Figure 10. AC Waveforms for Embedded Erase Operation

SWITCHING WAVEFORMS



18879C-20

Notes:

D_{IN} is data input to the device.

DQ7# is the complement of the data written to the device.

D_{OUT} is the data written to the device.

Figure 11. AC Waveforms for Embedded Programming Operation

AC CHARACTERISTICS—WRITE/ERASE/PROGRAM OPERATIONS

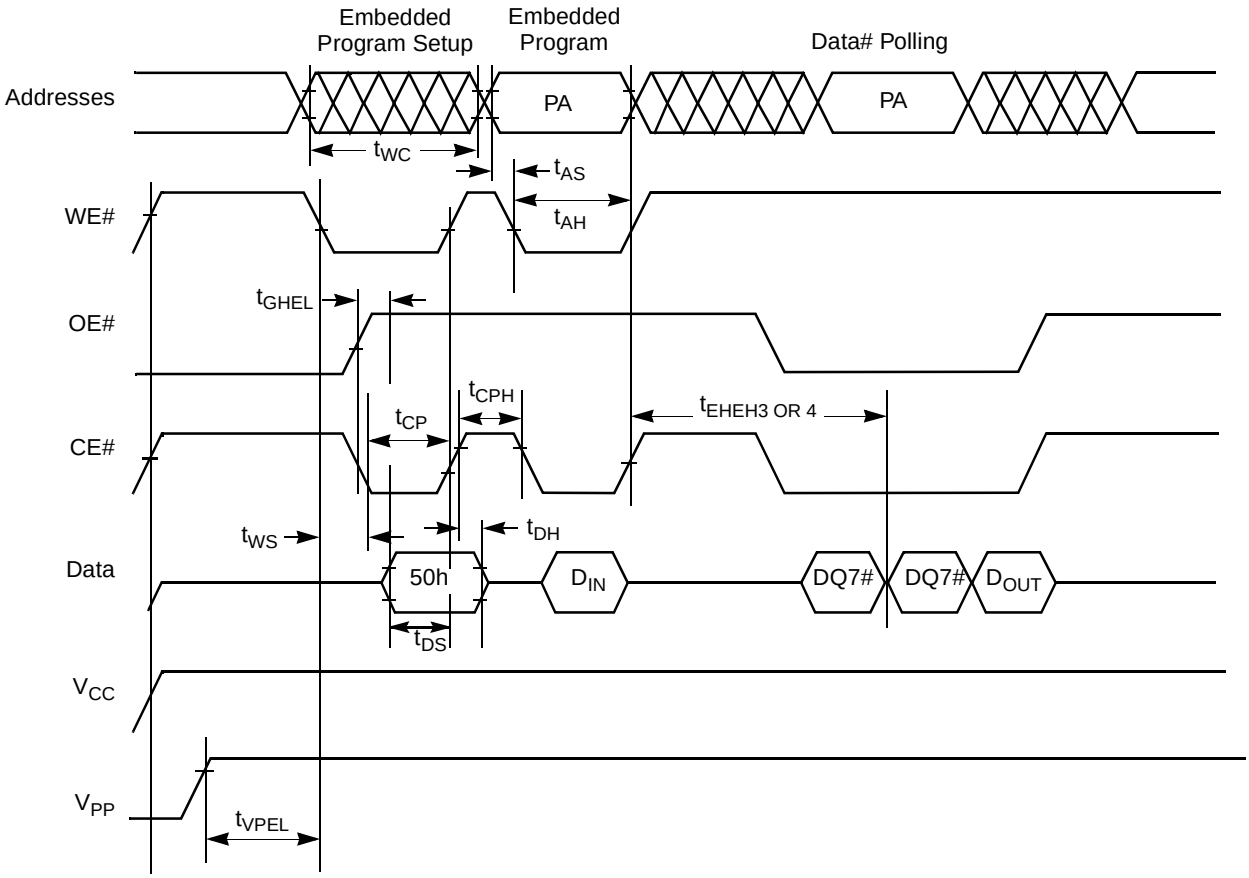
Alternate CE# Controlled Writes

Parameter Symbols		Parameter Description		Am28F256A Speed Options					Unit
JEDEC	Standard			-70	-90	-120	-150	-200	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 4)	Min	70	90	120	150	200	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	45	50	60	75	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	45	45	50	50	50	ns
t_{EHDX}	t_{g}	Data Hold Time	Min	10	10	10	10	10	ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm only	Min	10	10	10	10	10	ns
t_{GHEL}		Read Recovery Time Before Write	Min	0	0	0	0	0	µs
t_{WLEL}	t_{WS}	WE# Setup Time by CE#	Min	0	0	0	0	0	ns
t_{EHWK}	t_{WH}	WE# Hold Time	Min	0	0	0	0	0	ns
t_{ELEH}	t_{CP}	Write Pulse Width	Min	65	65	70	80	80	ns
t_{EHEL}	t_{CPH}	Write Pulse Width HIGH	Min	20	20	20	20	20	ns
t_{EHEH3}		Embedded Programming Operation (Note 2)	Min	14	14	14	14	14	µs
t_{EHEH4}		Embedded Erase Operation (Note 3)	Typ	5	5	5	5	5	sec
t_{VPEL}		V_{PP} Setup Time to Chip Enable LOW (Note 4)	Min	100	100	100	100	100	ns
t_{VCS}		V_{CC} Setup Time to Chip Enable LOW (Note 4)	Min	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 4)	Min	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 90% V_{PPL} (Note 4)	Min	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 4)	Min	100	100	100	100	100	ns

Notes:

1. *Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.*
2. *Embedded program operation of 14 µs consists of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.*
3. *Embedded erase operation of 5 sec consists of 4 sec array pre-programming time and one sec array erase time. This is a typical time for one embedded erase operation.*
4. *Not 100% tested.*

SWITCHING WAVEFORMS



18879C-21

Notes:

1. *D_{IN} is data input to the device.*
2. *DQ7# is complement of the data written to the device.*
3. *D_{OUT} is the data written to the device.*

Figure 12. AC Waveforms for Embedded Programming Operation Using CE# Controlled Writes

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits				Comments
	Min	Typ (Note 1)	Max (Note 2)	Unit	
Chip Erase Time		1	10	sec	Excludes 00h programming prior to erasure
Chip Programming Time		0.5	12.5	sec	Excludes system-level overhead
Write/Erase Cycles	100,000			Cycles	
Byte Programming Time		14		µs	
			96 (Note 3)	ms	

Notes:

1. *25°C, 12 V V_{PP}*
2. *Maximum time specified is lower than worst case. Worst case is derived from the Embedded Algorithm internal counter which allows for a maximum 6000 pulses for both program and erase operations. Typical worst case for program and erase is significantly less than the actual device limit.*
3. *Typical worst case = 84 µs. DQ5 = "1" only after a byte takes longer than 96 ms to program.*

LATCHUP CHARACTERISTICS

Parameter	Min	Max
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A9 and V_{PP})	–1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	–1.0 V	V_{CC} + 1.0 V
Current	–100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	V_{PP} = 0	8	12	pF

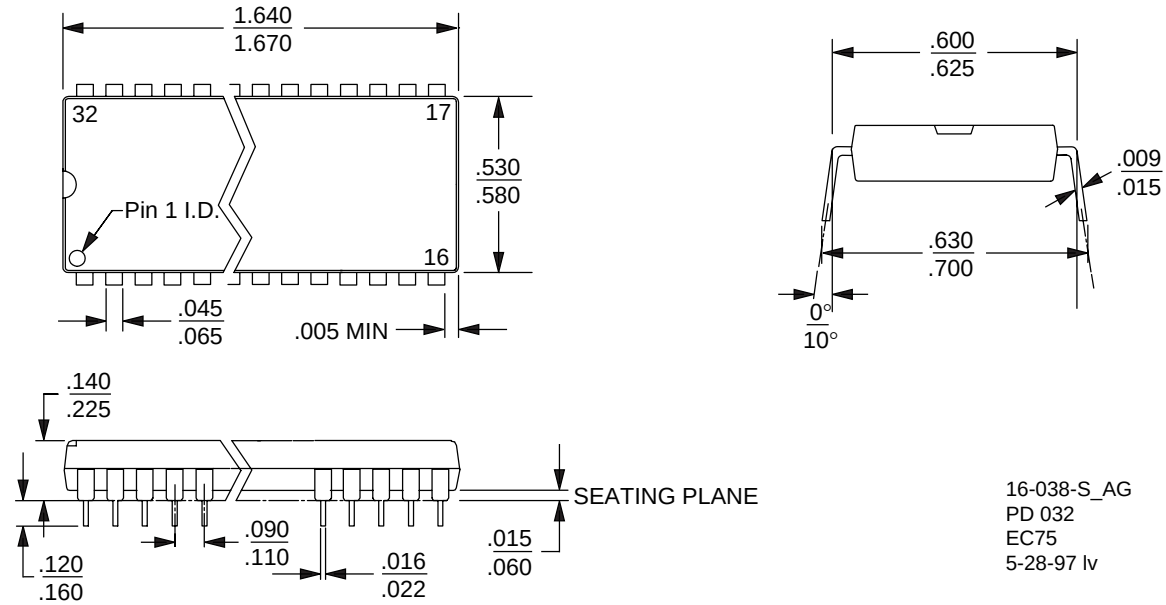
Note: *Sampled, not 100% tested. Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

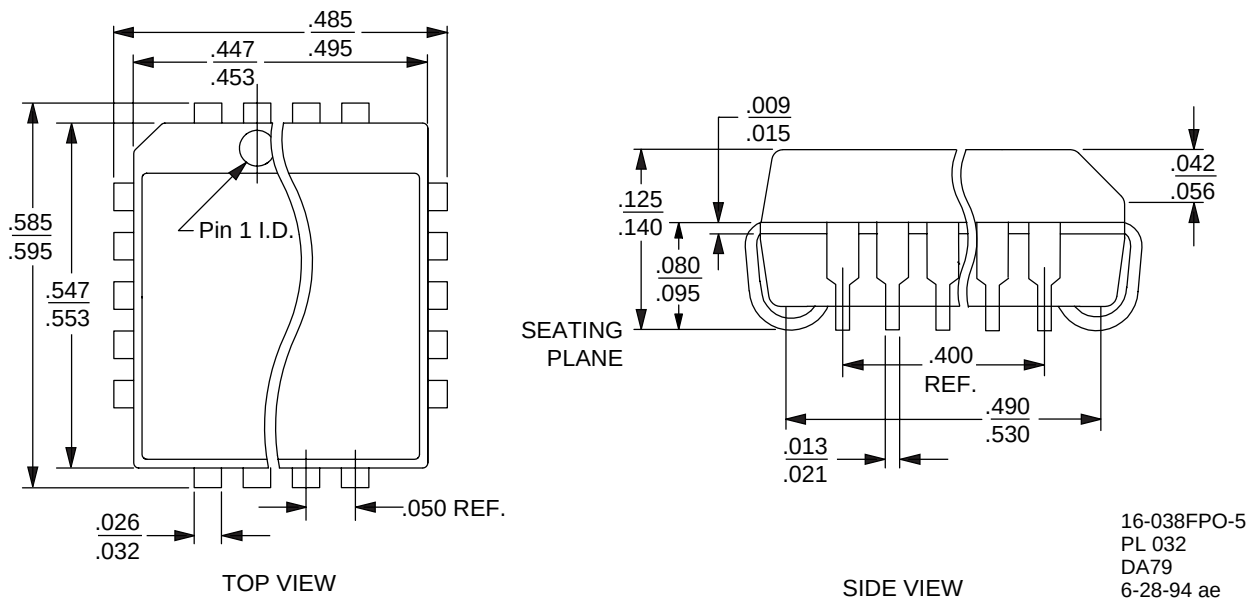
PHYSICAL DIMENSIONS

PD032—32-Pin Plastic DIP (measured in inches)



16-038-S_AG
PD 032
EC75
5-28-97 lv

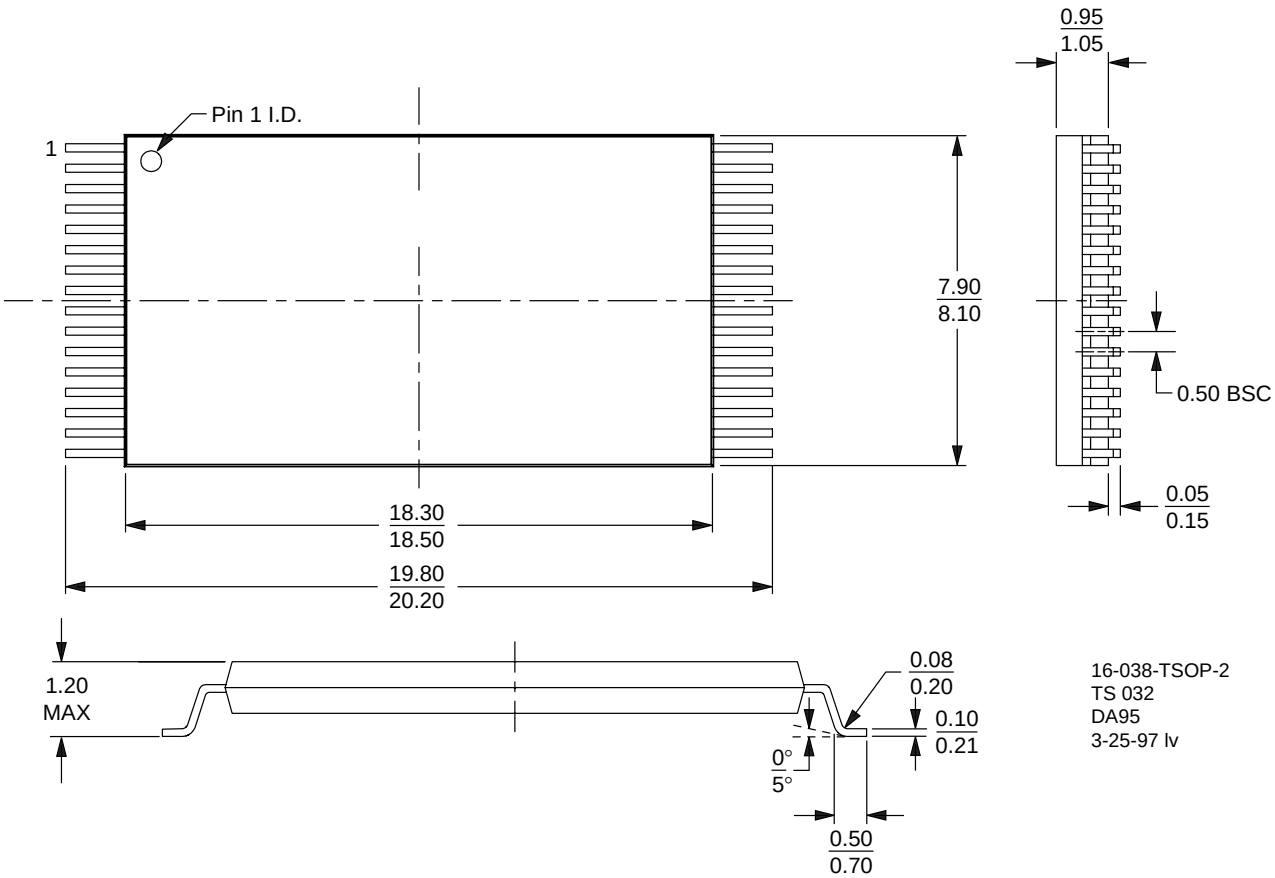
PL032—32-Pin Plastic Leaded Chip Carrier (measured in inches)



16-038FPO-5
PL 032
DA79
6-28-94 ae

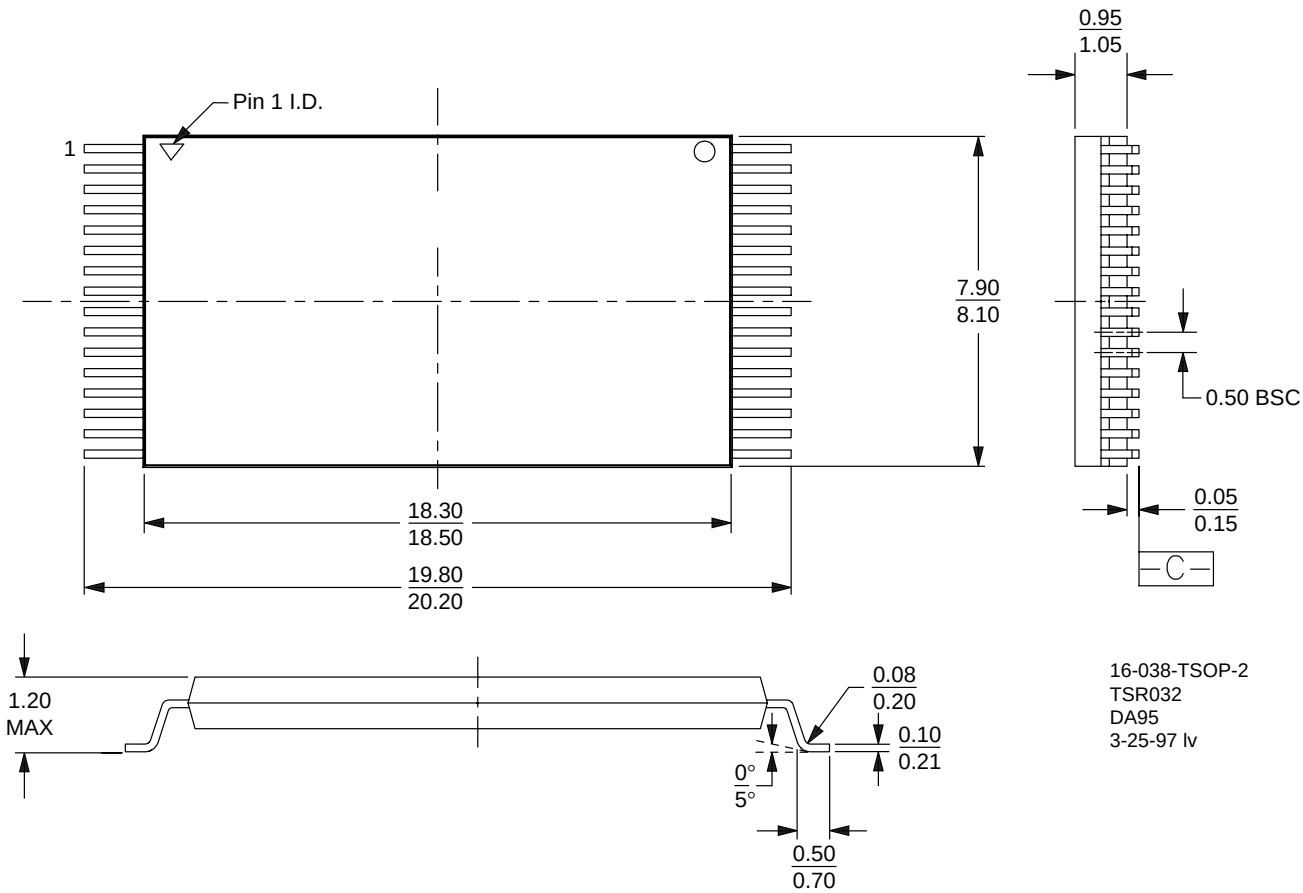
PHYSICAL DIMENSIONS

TS032—32-Pin Standard Thin Small Outline Package (measured in millimeters)



PHYSICAL DIMENSIONS

TSR032—32-Pin Reversed Thin Small Outline Package (measured in millimeters)



DATA SHEET REVISION SUMMARY FOR AM28F256A

Deleted -75, -95, and -250 speed options. Matched formatting to other current data sheets.

Revision C+1

Programming In A PROM Programmer:

Deleted the paragraph "(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system)."

Revision C+2

Product Selector Guide

Corrected maximum access time for -200 to 200 ns.

Erase and Programming Performance

Chip Programming Time—Typical: Changed value from 2 to 0.5 sec.

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