PRELIMINARY

AMD

Am186™ED/EDLV

High Performance, 80C186- and 80C188-Compatible, 16-Bit Embedded Microcontrollers

DISTINCTIVE CHARACTERISTICS

- **E86™ family 80C186- and 80C188-compatible microcontroller with enhanced bus interface**
  - Lower system cost with higher performance
  - 3.3-V ± 0.3-V operation (Am186EDLV microcontrollers)
- **Programmable DRAM Controller**
  - Supports zero-wait-state operation with 50-ns DRAM at 40 MHz, 60-ns @ 33 MHz, 70-ns @ 25 MHz
  - Includes programmable $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability
- **High performance**
  - 20-, 25-, 33-, and 40-MHz operating frequencies
  - Zero-wait-state operation at 40 MHz with 70-ns static memory
  - 1-Mbyte memory address space
  - 64-Kbyte I/O space
- **Enhanced features provide improved memory access and remove the requirement for a 2x clock input**
  - Nonmultiplexed address bus
  - Processor operates at the clock input frequency
  - 8-bit or 16-bit programmable bus sizing including 8-bit boot option
- **Enhanced integrated peripherals**
  - 32 programmable I/O (PIO) pins
  - Two full-featured asynchronous serial ports allow full-duplex, 7-bit, 8-bit, or 9-bit data transfers
  - Serial port hardware handshaking with $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{ENRX}}$, and $\overline{\text{RTR}}$ selectable for each port
  - Improved serial port operation enhances 9-bit DMA support
  - Independent serial port baud rate generators
  - DMA to and from the serial ports
  - Watchdog timer can generate NMI or reset
  - A pulse-width demodulation option
  - A data strobe, true asynchronous bus interface option included for $\overline{\text{DEN}}$
  - Reset configuration register
- **Familiar 80C186 peripherals**
  - Two independent DMA channels
  - Programmable interrupt controller with up to 8 external and 8 internal interrupts
  - Three programmable 16-bit timers
  - Programmable memory and peripheral chip-select logic
  - Programmable wait state generator
  - Power-save clock divider
- **Software-compatible with the 80C186 and 80C188 microcontrollers with widely available native development tools, applications, and system software**
- **A compatible evolution of the Am186EM, Am186ES, and Am186ER microcontrollers**
- **Available in the following packages:**
  - 100-pin, thin quad flat pack (TQFP)
  - 100-pin, plastic quad flat pack (PQFP)

GENERAL DESCRIPTION

The Am186™ED/EDLV microcontrollers are part of the AMD E86™ family of embedded microcontrollers and microprocessors based on the x86 architecture. The Am186ED/EDLV microcontrollers are the ideal upgrade for 80C186/188 designs requiring 80C186/188 compatibility, increased performance, serial communications, a direct bus interface, and more than 64K of memory.

The Am186ED/EDLV microcontrollers integrate a complete DRAM controller to take advantage of low DRAM costs. This reduces memory subsystem costs while maintaining SRAM performance.The Am186ED/EDLV microcontrollers also integrate the functions of a CPU, nonmultiplexed address bus, three timers, watchdog timer, chip selects, interrupt controller, two DMA controllers, two asynchronous serial ports, programmable bus sizing, and programmable I/O (PIO) pins on one chip. Compared to the 80C186/188 microcontrollers, the Am186ED/EDLV microcontrollers enable designers to reduce the size, power consumption, and cost of embedded systems, while increasing reliability, functionality, and performance.

The Am186ED/EDLV microcontrollers have been designed to meet the most common requirements of embedded products developed for the communications, office automation, mass storage, and general embedded markets. Specific applications include PBXs, multiplexers, modems, disk drives, hand-held and desktop terminals, fax machines, printers, photocopiers, and industrial controls.

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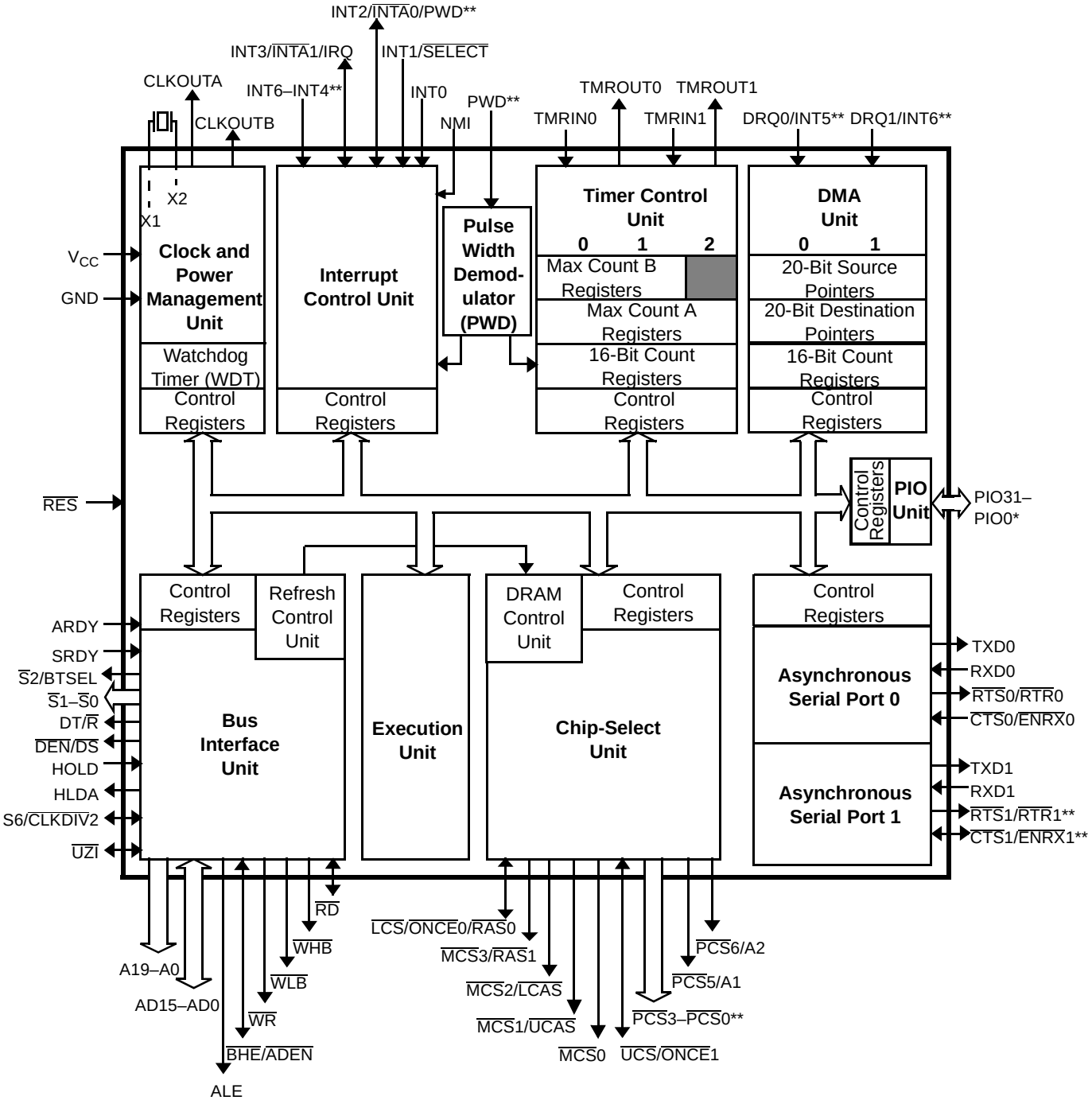
Issue Date: **May 1997**

Am186ED/EDLV MICROCONTROLLERS BLOCK DIAGRAM



Notes:

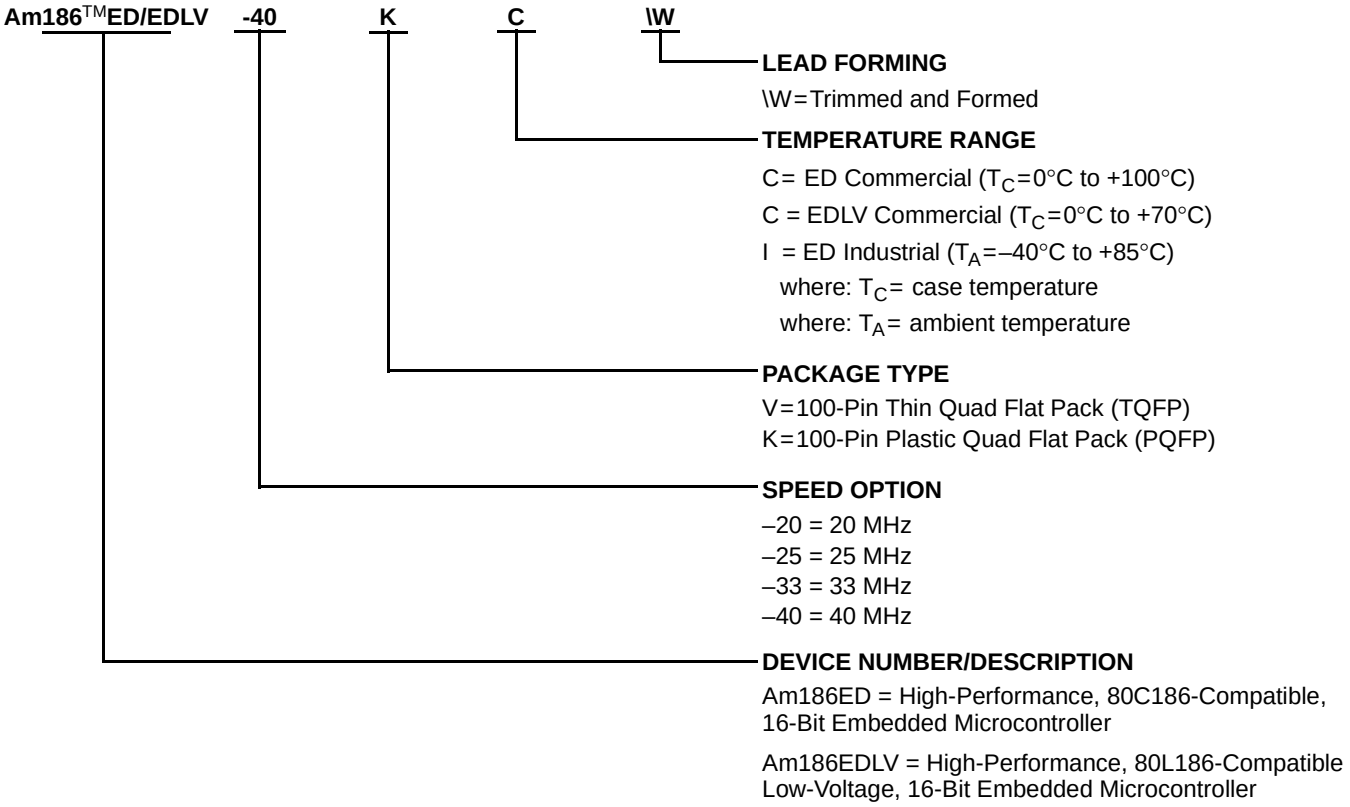
**All PIO signals are shared with other physical pins. See the pin descriptions beginning on page 21 and Table 2 on page 29 for information on shared functions.*

*** RTS1/RTR1 and CTS1/ENRX1 are multiplexed with PCS3 and PCS2, respectively. See the pin descriptions beginning on page 21.*

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (valid combination) is formed by a combination of the elements below.



Valid Combinations	
Am186ED–20 Am186ED–25 Am186ED–33 Am186ED–40	VC\W or KC\W
Am186ED–20 Am186ED–25	KI\W[1]
Am186EDLV–20 Am186EDLV–25	VC\W or KC\W

Note:
The industrial version of the Am186ED is offered only in the PQFP package.

Valid Combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note: *The industrial version of the Am186ED as well as the Am186EDLV are available in 20 and 25 MHz operating frequencies only.*

The Am186ED and Am186EDLV microcontrollers are all functionally the same except for their DC characteristics and available frequencies.

Note: *There is no 188 version of the Am186ED/EDLV. The same 8-bit external bus capabilities can be achieved using the 8-bit boot capability and programmable bus sizing options.*

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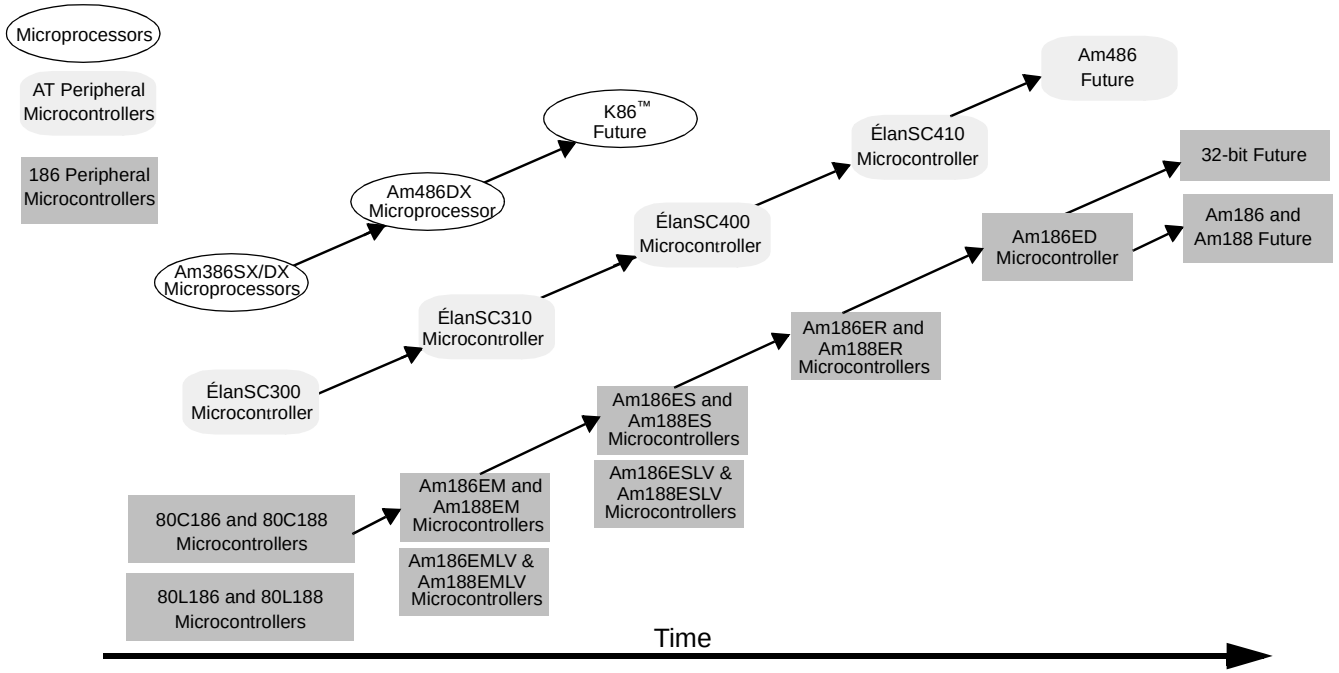

The E86 Family of Embedded Microprocessors and Microcontrollers

RELATED AMD PRODUCTS

E86™ Family Devices

Device	Description
80C186	16-bit microcontroller
80C188	16-bit microcontroller with 8-bit external data bus
80L186	Low-voltage, 16-bit microcontroller
80L188	Low-voltage, 16-bit microcontroller with 8-bit external data bus
Am186EM	High-performance, 80C186-compatible, 16-bit embedded microcontroller
Am188EM	High-performance, 80C188-compatible, 16-bit embedded microcontroller with 8-bit external data bus
Am186EMLV	High-performance, 80C186-compatible, low-voltage, 16-bit embedded microcontroller
Am188EMLV	High-performance, 80C188-compatible, low-voltage, 16-bit embedded microcontroller with 8-bit external data bus
Am186ES	High-performance, 80C186-compatible, 16-bit embedded microcontroller
Am188ES	High-performance, 80C188-compatible, 16-bit embedded microcontroller with 8-bit external data bus
Am186ESLV	High-performance, 80C186-compatible, low-voltage, 16-bit embedded microcontroller
Am188ESLV	High-performance, 80C188-compatible, low-voltage, 16-bit embedded microcontroller with 8-bit external data bus
Am186ED	High-performance, 80C186- and 80C188-compatible, 16-bit embedded microcontroller with 8- or 16-bit external data bus
Am186EDLV	High-performance, 80C186- and 80C188-compatible, low-voltage, 16-bit embedded microcontroller with 8- or 16-bit external data bus
Am186ER	High-performance, 80C186-compatible, low-voltage, 16-bit embedded microcontroller with 32 Kbyte of internal RAM
Am188ER	High-performance, 80C188-compatible, low-voltage, 16-bit embedded microcontroller with 8-bit external data bus and 32 Kbyte of internal RAM
Élan™SC300	High-performance, highly integrated, low-voltage, 32-bit embedded microcontroller
ÉlanSC310	High-performance, single-chip, 32-bit embedded PC/AT microcontroller
ÉlanSC400	Single-chip, low-power, PC/AT-compatible microcontroller
ÉlanSC410	Single-chip, PC/AT-compatible microcontroller
Am386®DX	High-performance, 32-bit embedded microprocessor with 32-bit external data bus
Am386®SX	High-performance, 32-bit embedded microprocessor with 16-bit external data bus
Am486®DX	High-performance, 32-bit embedded microprocessor with 32-bit external data bus

Related Documents

The following documents provide additional information regarding the Am186ED/EDLV microcontrollers:

- *Am186ED/EDLV Microcontrollers User's Manual*, order # 21335
- *Am186 and Am188 Family Instruction Set Manual*, order # 21267
- *FusionE86℠ Catalog*, order # 19255
- *E86 Family Support Tools Brief*, order # 20071
- FusionE86 Development Tools Reference CD, order # 21058

Third-Party Development Support Products

The FusionE86℠ Program of Partnerships for Application Solutions provides the customer with an array of products designed to meet critical time-to-market needs. Products and solutions available from the AMD FusionE86 partners include emulators, hardware and software debuggers, board-level products, and software development tools, among others.

In addition, mature development tools and applications for the x86 platform are widely available in the general marketplace.

Customer Service

The AMD customer service network includes U.S. offices, international offices, and a customer training center. Expert technical assistance is available from the worldwide staff of AMD field application engineers and factory support staff to answer E86 family hardware and software development questions.

Hotline and World Wide Web Support

For answers to technical questions, AMD provides a toll-free number for direct access to our corporate applications hotline. Also available is the AMD World Wide Web home page and FTP site, which provides the latest E86 family product information, including technical information and data on upcoming product releases.

For technical support questions on all E86 products, send E-mail to lpd.support@amd.com.

Corporate Applications Hotline

(800) 222-9323	Toll-free for U.S. and Canada
44-(0) 1276-803-299	U.K. and Europe hotline

World Wide Web Home Page and FTP Site

To access the AMD home page go to: http://www.amd.com.

To download documents and software, ftp to ftp.amd.com and log on as anonymous using your E-mail address as a password. Or via your web browser, go to ftp://ftp.amd.com.

Questions, requests, and input concerning AMD's WWW pages can be sent via E-mail to webmaster@amd.com.

Documentation and Literature

Free E86 family information such as data books, user's manuals, data sheets, application notes, the FusionE86 Partner Solutions Catalog, and other literature is available with a simple phone call. Internationally, contact your local AMD sales office for complete E86 family literature.

Literature Ordering

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(512) 602-5651	Direct dial worldwide
(512) 602-7639	fax
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KEY FEATURES AND BENEFITS

The Am186ED/EDLV microcontrollers extend the AMD family of microcontrollers based on the industry-standard x86 architecture. The Am186ED/EDLV microcontrollers are a higher-performance, highly integrated version of the 80C186/188 microprocessors, offering an attractive migration path. In addition, the Am186ED/EDLV microcontrollers offer application-specific features that can enhance the system functionality of the Am186ES/ESLV and Am188ES/ESLV microcontrollers. Upgrading to the Am186ED/EDLV microcontrollers is an attractive solution for several reasons:

- **Programmable DRAM controller**—Enables system designers to take advantage of low-cost DRAM and fully utilize the performance and flexibility of the x86 architecture. The DRAM controller supports zero wait-state performance with 50-ns DRAM at 40 MHz, or, if required, can be programmed with wait states. The Am186ED/EDLV microcontrollers provide a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh unit.
- **Minimized total system cost**—New and enhanced peripherals and on-chip system interface logic on the Am186ED/EDLV microcontrollers reduce the cost of existing 80C186/188 designs.
- **X86 software compatibility**—80C186/188-compatible and upward-compatible with the other members of the AMD E86 family.

- **Enhanced performance**—The Am186ED/EDLV microcontrollers increase the performance of 80C186/188 systems, and the nonmultiplexed address bus offers unbuffered access to memory.
- **Enhanced functionality**—The enhanced on-chip peripherals of the Am186ED/EDLV microcontrollers include two asynchronous serial ports, 32 PIOs, a watchdog timer, additional interrupt pins, a pulse width demodulation option, DMA directly to and from the serial ports, 8-bit and 16-bit programmable bus sizing, a 16-bit reset configuration register, and enhanced chip-select functionality.

Application Considerations

The integration enhancements of the Am186ED/EDLV microcontrollers provide a high-performance, low-system-cost solution for 16-bit embedded microcontroller designs. The nonmultiplexed address bus eliminates the need for system-support logic to interface memory devices, while the multiplexed address/data bus maintains the value of previously engineered, customer-specific peripherals and circuits within the upgraded design.

Figure 1 illustrates an example system design that uses the integrated peripheral set to achieve high performance with reduced system cost.

Memory Interface

The Am186ED/EDLV microcontrollers integrate a versatile memory controller which supports direct memory accesses to DRAM, SRAM, Flash, EPROM, and ROM. No external glue logic is required and all required control signals are provided. The peripheral chip selects have been enhanced to allow them to overlap the DRAM. This allows a small 1.5K portion of the DRAM memory space to be used for peripherals without bus contention.

The improved memory timing specifications of the Am186ED/EDLV microcontrollers allow for zero-wait-state operation at 40 MHz using 50-ns DRAM, 70-ns SRAM, or 70-ns Flash memory. For 60-ns DRAM one wait state is required at 40 MHz and zero wait states at 33 MHz and below. For 70-ns DRAM two wait states are required at 40 MHz, one wait state at 33 MHz, and zero wait states at 25 MHz and below. This reduces overall system cost by enabling the use of commonly available memory speeds and taking advantage of DRAM's lower cost per bit over SRAM.

Figure 1 also shows an implementation of an RS-232 console or modem communications port. The RS-232 to CMOS voltage-level converter is required for the electrical interface with the external device.

Clock Generation

The integrated clock generation circuitry of the Am186ED/EDLV microcontrollers enables the use of a 1x crystal frequency. The Am186ED design in Figure 1 achieves 40-MHz CPU operation, while using a 40-MHz crystal.

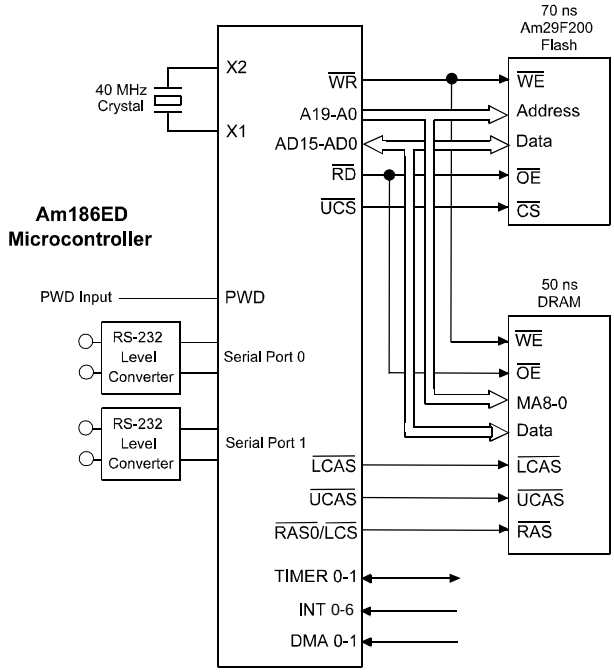


Figure 1. Am186ED Microcontroller Example System Design

Direct Memory Interface Example

Figure 1 illustrates the direct memory interface of the Am186ED microcontroller. The processor's A19–A0 bus connects to the memory address inputs, the AD bus connects to the data inputs and outputs, and the chip selects connect to the memory chip-select inputs. The odd A1–A17 address pins connect to the DRAM multiplexed address bus.

The $\overline{RD}$ output connects to the DRAM Output Enable ($\overline{OE}$) pin for read operations. Write operations use the $\overline{WR}$ output connected to the DRAM Write Enable ($\overline{WE}$) pin. The $\overline{UCAS}$ and $\overline{LCAS}$ pins provide byte selection.

COMPARING THE Am186ES/ESLV TO THE Am186ED/EDLV MICROCONTROLLERS

Compared to the Am186ES/ESLV microcontrollers, the Am186ED/EDLV microcontrollers have the following additional features:

- Integrated DRAM controller
- Enhanced refresh control unit
- Option to overlap DRAM with peripheral chip select (PCS)
- Additional serial port mode for DMA support of 9-bit protocols
- Option to boot from 8- or 16-bit memory
- Improved external bus master support
- PSRAM controller removed

Figure 1 shows an example system using a 40-MHz Am186ED microcontroller. Figure 2 shows a comparable system implementation with an 80C186. Because of its superior integration, the Am186ED/EDLV system does not require the support devices that are required on the 80C186 example system. In addition, the Am186ED/EDLV microcontrollers provide significantly better performance with its 40-MHz clock rate.

Integrated DRAM Controller

The integrated DRAM controller directly interfaces DRAM to support no-wait state DRAM interface up to 40 MHz. Wait states can be inserted to support slower DRAM. All signals required by the DRAM are generated on the Am186ED/EDLV microcontrollers and no external logic is required. The DRAM multiplexed address pins are connected to the odd address pins starting with A1 on the Am186ED/EDLV microcontrollers to MA0 on the DRAM. The correct row and column addresses are generated on these pins during a DRAM access. The $\overline{UCAS}$ and $\overline{LCAS}$ are used to select which byte of the DRAM is accessed during a read or write. The $\overline{RAS}0$ controls the lower bank of DRAM which starts at 00000h in the address map and is bounded by the lower memory size selected in the LMCS register. $\overline{RAS}1$ controls the upper bank of DRAM which ends at FFFFFh and is bounded by the upper memory size in the UMCS register. When $\overline{RAS}1$ is enabled, $\overline{UCS}$ is automatically disabled. Neither, either, or both DRAM banks can be activated.

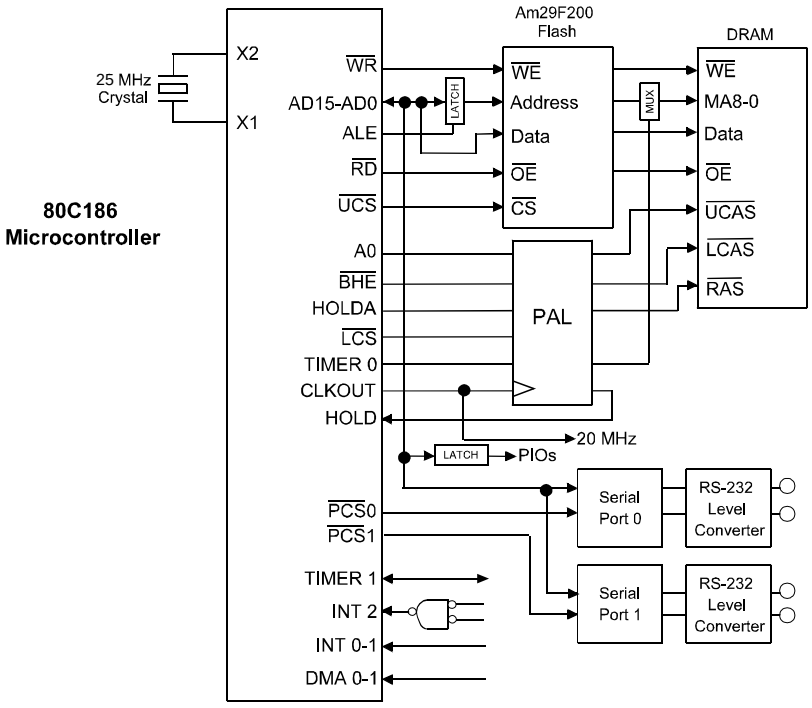


Figure 2. 80C186 Microcontroller Example System Design

Enhanced Refresh Control Unit

The refresh control unit (RCU) is enhanced with two additional bits in the refresh counter to allow for longer refresh periods. The address generated during a refresh has been fixed to FFFFFh. When either bank of DRAM is enabled and the RCU is enabled, a $\overline{CAS}$-before-$\overline{RAS}$ refresh will be generated based on the time period coded into the refresh counter.

Option to Overlap DRAM with $\overline{PCS}$

The peripheral chip selects ($\overline{PCS}$0–$\overline{PCS}$6) can overlap DRAM blocks with different wait states without external or internal bus contention. The $\overline{RAS}$0 or $\overline{RAS}$1 will assert along with the appropriate $\overline{PCS}$. The $\overline{UCAS}$ and $\overline{LCAS}$ will not assert, preventing the DRAM from writing erroneously or driving the data bus during a read. The $\overline{PCS}$ must have the same or higher number of wait states than the DRAM. The $\overline{PCS}$ bus width will be determined by the LSIZ or USIZ bus widths as programmed in the AUXCON register.

Additional Serial Port Mode for DMA Support of 9-bit Protocols

A mode 7 was added to the serial port which enhances the direct memory access (DMA) support for 9-bit protocols. Using mode 2, the serial port can be programmed to interrupt only if the 9th bit is set, ignoring all 9th bit cleared byte receptions. Mode 3 receives all bytes, whether the 9th bit is set or cleared. Mode 7 also receives all bytes whether the 9th bit is set or cleared, but now an interrupt is generated when the 9th bit is set. This allows the DMA to service all receptions, but also allows the CPU to intervene when the trailer (9th bit set) is received. In all modes using DMA, the interrupts other than transmitter ready and character received interrupts can still be generated. This allows the DMA to handle the standard sending and receiving characters while the CPU can intervene when a non-standard event (e.g., framing error) occurs.

Option to Boot from 8- or 16-bit Memory

The Am186ED/EDLV microcontrollers can boot from 8- or 16-bit-wide non-volatile memory, based on the state of the $\overline{S}$2/BTSEL pin. If $\overline{S}$2/BTSEL is pulled High or left floating, an internal pullup sets the boot mode option to 16-bit. If $\overline{S}$2/BTSEL is pulled resistively Low during reset, the boot mode option is for 8-bit. The status of the $\overline{S}$2/BTSEL pin is latched on the rising edge of reset.

If the 8-bit boot option is selected, the width of the memory region associated with $\overline{UCS}$ can be changed in the AUXCON register. This allows for cheaper 8-bit-wide memory to be used for booting the microcontroller, while speed-critical code and data can be executed from 16-bit-wide lower memory. Eight-bit or 16-bit-wide peripherals can be used in the memory area between $\overline{LCS}$ and $\overline{UCS}$ or in the I/O space. The entire memory map can be set to 16-bit or 8-bit or mixed between 8-bit and 16-bit based on the USIZ, LSIZ, MSIZ, and IOSIZ bits in the AUXCON register.

Improved External Bus Master Support

When the bus is arbitrated away from the Am186ED/EDLV microcontrollers using the HOLD pin, the chip selects are driven High (negated) and then held High with an internal ~10-kohm pullup. This allows external bus masters to assert the chip selects by externally pulling them Low, without having to combine the chip selects from the Am186ED/EDLV microcontrollers and the external bus master in logic external to the Am186ED/EDLV microcontrollers. This internal pullup is activated for any bus arbitration, even if the pin is being used as a PIO input.

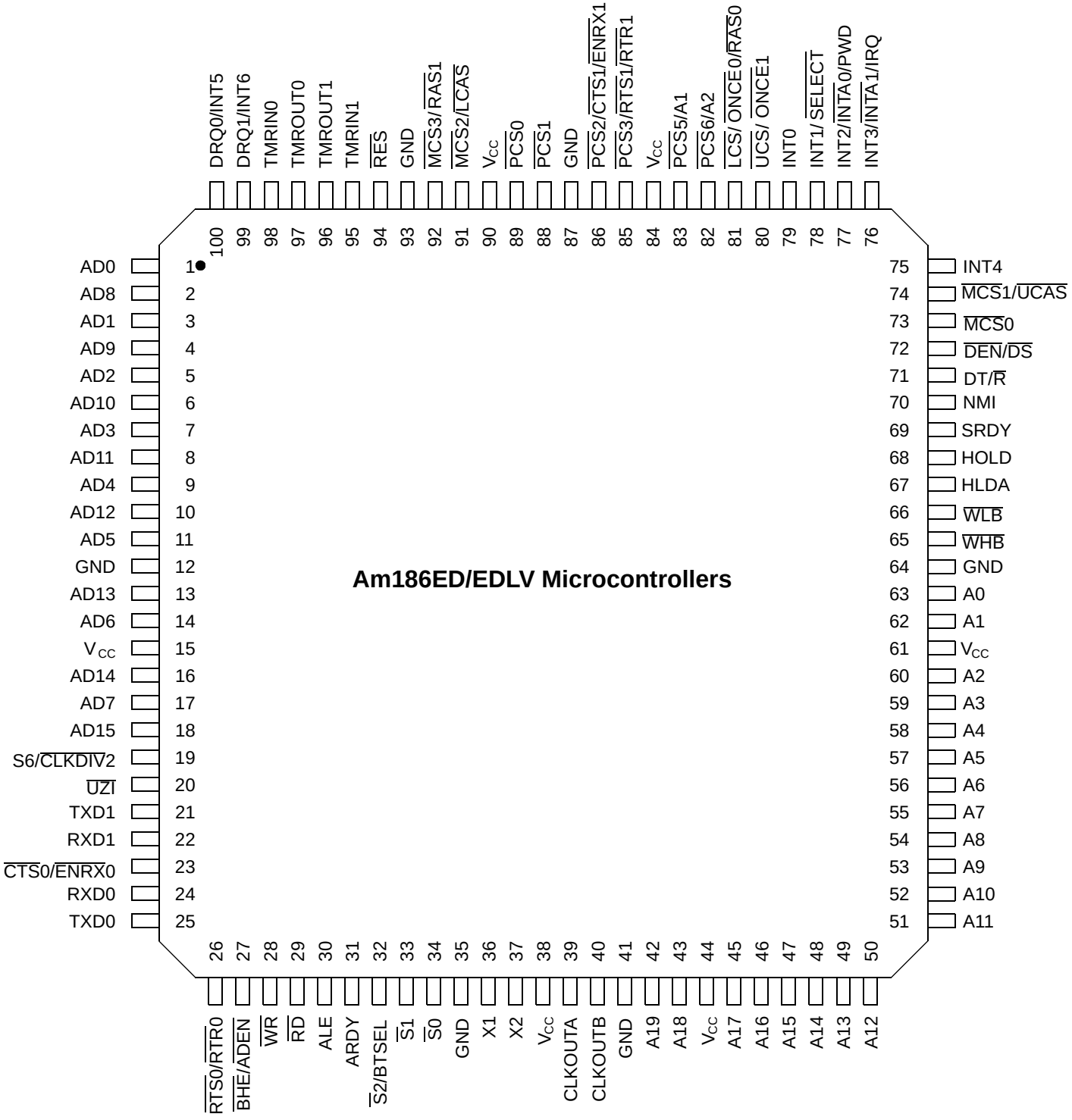
PSRAM Controller Removed

The PSRAM mode found on the Am186ES/ESLV microcontrollers has been removed and replaced with a DRAM controller. This includes removal of the variant PSRAM $\overline{LCS}$ timing and refresh strobe on $\overline{MCS}$3.

TQFP CONNECTION DIAGRAMS AND PINOUTS

Am186ED/EDLV Microcontrollers

Top Side View—100-Pin Thin Quad Flat Pack (TQFP)



Note:
Pin 1 is marked for orientation.

TQFP PIN DESIGNATIONS—Am186ED/EDLV Microcontrollers

Sorted by Pin Number

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	AD0	26	RTS0/RTR0/ PIO20	51	A11	76	INT3/INTA1/IRQ
2	AD8	27	BHE/ADEN	52	A10	77	INT2/INTA0/PWD/ PIO31
3	AD1	28	WR	53	A9	78	INT1/SELECT
4	AD9	29	RD	54	A8	79	INT0
5	AD2	30	ALE	55	A7	80	UCS/ONCE1
6	AD10	31	ARDY	56	A6	81	LCS/ONCE0/ RAS0
7	AD3	32	S2/BTSEL	57	A5	82	PCS6/A2/PIO2
8	AD11	33	S1	58	A4	83	PCS5/A1/PIO3
9	AD4	34	S0	59	A3	84	V_{CC}
10	AD12	35	GND	60	A2	85	PCS3/RTS1/ RTR1/ PIO19
11	AD5	36	X1	61	V_{CC}	86	PCS2/CTS1/ ENRX1/PIO18
12	GND	37	X2	62	A1	87	GND
13	AD13	38	V_{CC}	63	A0	88	PCS1/PIO17
14	AD6	39	CLKOUTA	64	GND	89	PCS0/PIO16
15	V_{CC}	40	CLKOUTB	65	WHB	90	V_{CC}
16	AD14	41	GND	66	WLB	91	MCS2/LCAS/ PIO24
17	AD7	42	A19/PIO9	67	HLDA	92	MCS3/RAS1/ PIO25
18	AD15	43	A18/PIO8	68	HOLD	93	GND
19	S6/CLKDIV2/PIO29	44	V_{CC}	69	SRDY/PIO6	94	RES
20	UZI/PIO26	45	A17/PIO7	70	NMI	95	TMRIN1/PIO0
21	TXD1/PIO27	46	A16	71	DT/R/PIO4	96	TMROUT1/PIO1
22	RXD1/PIO28	47	A15	72	DEN/DS/PIO5	97	TMROUT0/PIO10
23	CTS0/ENRX0/PIO21	48	A14	73	MCS0/PIO14	98	TMRIN0/PIO11
24	RXD0/PIO23	49	A13	74	MCS1/UCAS/ PIO15	99	DRQ1/INT6/PIO13
25	TXD0/PIO22	50	A12	75	INT4/PIO30	100	DRQ0/INT5/PIO12

TQFP PIN DESIGNATIONS—Am186ED/EDLV Microcontrollers

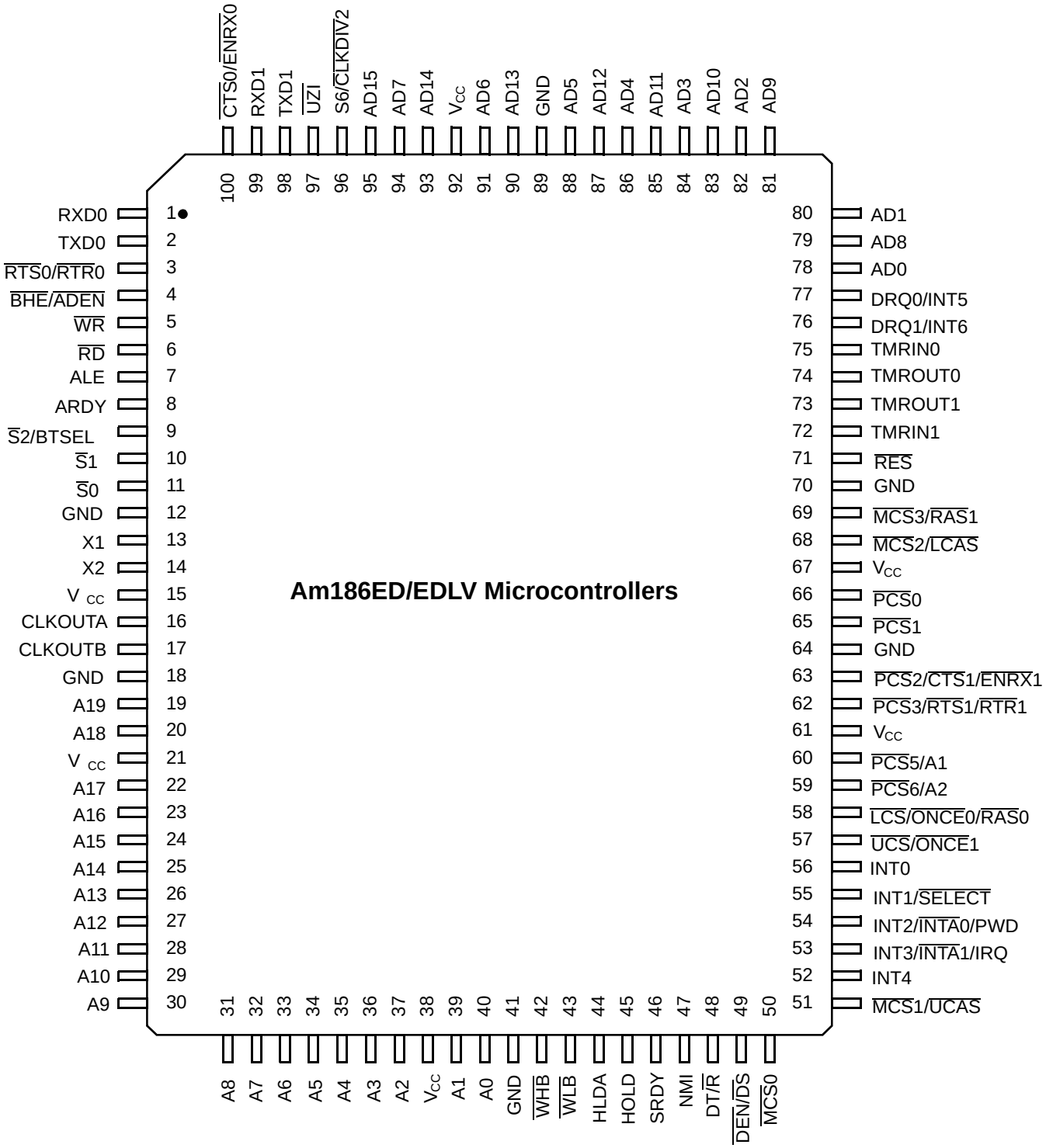
Sorted by Pin Name

Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.
A0	63	AD5	11	GND	87	RXD1	22
A1	62	AD6	14	GND	93	$\overline{S}$0	34
A2	60	AD7	17	HLDA	67	$\overline{S}$1	33
A3	59	AD8	2	HOLD	68	$\overline{S}$2/BTSEL	32
A4	58	AD9	4	INT0	79	S6/$\overline{CLKDIV}$2/ PIO29	19
A5	57	AD10	6	INT1/$\overline{SELECT}$	78	SRDY/PIO6	69
A6	56	AD11	8	INT2/$\overline{INTA}$0/PWD/ PIO31	77	TMRIN0/PIO11	98
A7	55	AD12	10	INT3/$\overline{INTA}$1/IRQ	76	TMRIN1/PIO0	95
A8	54	AD13	13	INT4/PIO30	75	TMROUT0/ PIO10	97
A9	53	AD14	16	$\overline{LCS}$/$\overline{ONCE}$0/$\overline{RAS}$0	81	TMROUT1/PIO1	96
A10	52	AD15	18	$\overline{MCS}$0/PIO14	73	TXD0/PIO22	25
A11	51	ALE	30	$\overline{MCS}$1/$\overline{UCAS}$/ PIO15	74	TXD1	21
A12	50	ARDY	31	$\overline{MCS}$2/$\overline{LCAS}$/PIO24	91	$\overline{UCS}$/$\overline{ONCE}$1	80
A13	49	$\overline{BHE}$/$\overline{ADEN}$	27	$\overline{MCS}$3/$\overline{RAS}$1/PIO25	92	$\overline{UZI}$/PIO26	20
A14	48	CLKOUTA	39	NMI	70	V_{CC}	15
A15	47	CLKOUTB	40	$\overline{PCS}$0/PIO16	89	V_{CC}	38
A16	46	$\overline{CTS}$0/$\overline{ENRX}$0/ PIO21	23	$\overline{PCS}$1/PIO17	88	V_{CC}	44
A17/PIO7	45	$\overline{DEN}$/$\overline{DS}$/PIO5	72	$\overline{PCS}$2/$\overline{CTS}$1/ $\overline{ENRX}$1/PIO18	86	V_{CC}	61
A18/PIO8	43	DRQ0/INT5/PIO12	100	$\overline{PCS}$3/$\overline{RTS}$1/$\overline{RTR}$1/ PIO19	85	V_{CC}	84
A19/PIO9	42	DRQ1/INT6/PIO13	99	$\overline{PCS}$5/A1/PIO3	83	V_{CC}	90
AD0	1	DT/$\overline{R}$/PIO4	71	$\overline{PCS}$6/A2/PIO2	82	$\overline{WHB}$	65
AD1	3	GND	12	$\overline{RD}$	29	$\overline{WLB}$	66
AD2	5	GND	35	$\overline{RES}$	94	$\overline{WR}$	28
AD3	7	GND	41	$\overline{RTS}$0/$\overline{RTR}$0/PIO20	26	X1	36
AD4	9	GND	64	RXD0/PIO23	24	X2	37

PQFP CONNECTION DIAGRAMS AND PINOUTS

Am186ED/EDLV Microcontrollers

Top Side View—100-Pin Plastic Quad Flat Pack (PQFP)



Note:
Pin 1 is marked for orientation.

PQFP PIN DESIGNATIONS—Am186ED/EDLV Microcontrollers

Sorted by Pin Number

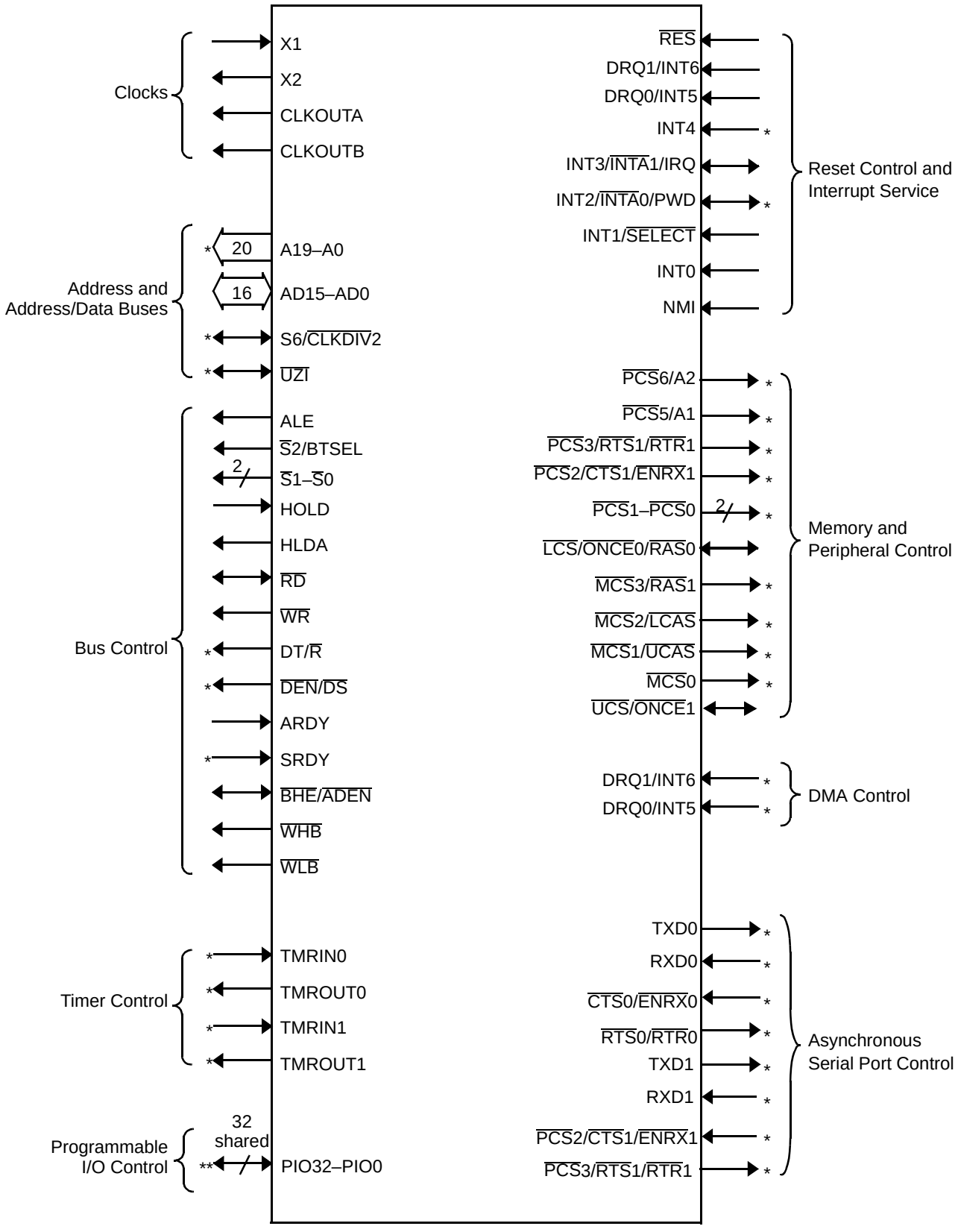
Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	RXD0/PIO23	26	A13	51	$\overline{MCS}$1/$\overline{UCAS}$/PIO15	76	DRQ1/INT6/PIO13
2	TXD0/PIO22	27	A12	52	INT4/PIO30	77	DRQ0/INT5/PIO12
3	$\overline{RTS}$0/$\overline{RTR}$0/ PIO20	28	A11	53	INT3/$\overline{INTA}$1/IRQ	78	AD0
4	$\overline{BHE}$/ADEN	29	A10	54	INT2/$\overline{INTA}$0/PWD/ PIO31	79	AD8
5	$\overline{WR}$	30	A9	55	INT1/$\overline{SELECT}$	80	AD1
6	$\overline{RD}$	31	A8	56	INT0	81	AD9
7	ALE	32	A7	57	$\overline{UCS}$/$\overline{ONCE}$1	82	AD2
8	ARDY	33	A6	58	$\overline{LCS}$/$\overline{ONCE}$0/$\overline{RAS}$0	83	AD10
9	$\overline{S}$2/BTSEL	34	A5	59	$\overline{PCS}$6/A2/PIO2	84	AD3
10	$\overline{S}$1	35	A4	60	$\overline{PCS}$5/A1/PIO3	85	AD11
11	$\overline{S}$0	36	A3	61	V_{CC}	86	AD4
12	GND	37	A2	62	$\overline{PCS}$3/$\overline{RTS}$1/$\overline{RTR}$1/ PIO19	87	AD12
13	X1	38	V_{CC}	63	$\overline{PCS}$2/$\overline{CTS}$1/ $\overline{ENRX}$1/PIO18	88	AD5
14	X2	39	A1	64	GND	89	GND
15	V_{CC}	40	A0	65	$\overline{PCS}$1/PIO17	90	AD13
16	CLKOUTA	41	GND	66	$\overline{PCS}$0/PIO16	91	AD6
17	CLKOUTB	42	$\overline{WHB}$	67	V_{CC}	92	V_{CC}
18	GND	43	$\overline{WLB}$	68	$\overline{MCS}$2/$\overline{LCAS}$/PIO24	93	AD14
19	A19/PIO9	44	HLDA	69	$\overline{MCS}$3/$\overline{RAS}$1/PIO25	94	AD7
20	A18/PIO8	45	HOLD	70	GND	95	AD15
21	V_{CC}	46	SRDY/PIO6	71	$\overline{RES}$	96	S6/$\overline{CLKDIV}$2/PIO29
22	A17/PIO7	47	NMI	72	TMRIN1/PIO0	97	$\overline{UZI}$/PIO26
23	A16	48	DT/$\overline{R}$/PIO4	73	TMROUT1/PIO1	98	TXD1/PIO27
24	A15	49	$\overline{DEN}$/$\overline{DS}$/PIO5	74	TMROUT0/PIO10	99	RXD1/PIO28
25	A14	50	$\overline{MCS}$0/PIO14	75	TMRIN0/PIO11	100	$\overline{CTS}$0/$\overline{ENRX}$0/PIO21

PQFP PIN DESIGNATIONS—Am186ED/EDLV Microcontrollers

Sorted by Pin Name

Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.
A0	40	AD5	88	GND	70	RXD1/PIO28	99
A1	39	AD6	91	GND	89	$\overline{S}$0	11
A2	37	AD7	94	HLDA	44	$\overline{S}$1	10
A3	36	AD8	79	HOLD	45	$\overline{S}$2/BTSEL	9
A4	35	AD9	81	INT0	56	S6/$\overline{CLKDIV}$2/ PIO29	96
A5	34	AD10	83	INT1/$\overline{SELECT}$	55	SRDY/PIO6	46
A6	33	AD11	85	INT2/$\overline{INTA}$0/ PWD/PIO31	54	TMRIN0/PIO11	75
A7	32	AD12	87	INT3/$\overline{INTA}$1/IRQ	53	TMRIN1/PIO0	72
A8	31	AD13	90	INT4/PIO30	52	TMROUT0/ PIO10	74
A9	30	AD14	93	$\overline{LCS}$/$\overline{ONCE}$0/$\overline{RAS}$0	58	TMROUT1/PIO1	73
A10	29	AD15	95	$\overline{MCS}$0/PIO14	50	TXD0/PIO22	2
A11	28	ALE	7	$\overline{MCS}$1/$\overline{UCAS}$/PIO15	51	TXD1/PIO27	98
A12	27	ARDY	8	$\overline{MCS}$2/$\overline{LCAS}$/PIO24	68	$\overline{UCS}$/$\overline{ONCE}$1	57
A13	26	$\overline{BHE}$/$\overline{ADEN}$	4	$\overline{MCS}$3/$\overline{RAS}$1/PIO25	69	$\overline{UZI}$/PIO26	97
A14	25	CLKOUTA	16	NMI	47	V_{CC}	15
A15	24	CLKOUTB	17	$\overline{PCS}$0/PIO16	66	V_{CC}	21
A16	23	$\overline{CTS}$0/$\overline{ENRX}$0/ PIO21	100	$\overline{PCS}$1/PIO17	65	V_{CC}	38
A17/PIO7	22	$\overline{DEN}$/$\overline{DS}$/PIO5	49	$\overline{PCS}$2/$\overline{CTS}$1/$\overline{ENRX}$1/ PIO18	63	V_{CC}	61
A18/PIO8	20	DRQ0/INT5/PIO12	77	$\overline{PCS}$3/$\overline{RTS}$1/$\overline{RTR}$1/ PIO19	62	V_{CC}	67
A19/PIO9	19	DRQ1/INT6/PIO13	76	$\overline{PCS}$5/A1/PIO3	60	V_{CC}	92
AD0	78	DT/$\overline{R}$/PIO4	48	$\overline{PCS}$6/A2/PIO2	59	$\overline{WHB}$	42
AD1	80	GND	12	$\overline{RD}$	6	$\overline{WLB}$	43
AD2	82	GND	18	$\overline{RES}$	71	$\overline{WR}$	5
AD3	84	GND	41	$\overline{RTS}$0/$\overline{RTR}$0/PIO20	3	X1	13
AD4	86	GND	64	RXD0/PIO23	1	X2	14

LOGIC SYMBOL—Am186ED/EDLV MICROCONTROLLERS



Notes:

** These signals are the normal function of a pin that can be used as a PIO. See Pin Descriptions beginning on page 21 and Table 2 on page 29 for information on shared function.*

*** All PIO signals are shared with other physical pins.*

PIN DESCRIPTIONS

Pins That Are Used by Emulators

The following pins are used by emulators: A19–A0, AD7–AD0, ALE, $\overline{BHE}$/$\overline{ADEN}$, CLKOUTA, $\overline{RD}$, $\overline{S}$2–$\overline{S}$0, S6/$\overline{CLKDIV}$2, and $\overline{UZI}$.

Many emulators require S6/$\overline{CLKDIV}$2 and $\overline{UZI}$ to be configured in their normal functionality as S6 and $\overline{UZI}$, not as PIOs. If $\overline{BHE}$/$\overline{ADEN}$ is held Low during the rising edge of $\overline{RES}$, S6 and $\overline{UZI}$ are configured in their normal functionality.

Pin Terminology

The following terms are used to describe the pins:

Input—An input-only pin.

Output—An output-only pin.

Input/Output—A pin that can be either input or output (I/O).

Synchronous—Synchronous inputs must meet setup and hold times in relation to CLKOUTA. Synchronous outputs are synchronous to CLKOUTA.

Asynchronous—Inputs or outputs that are asynchronous to CLKOUTA.

A19–A0 (A19/PIO9, A18/PIO8, A17/PIO7)

Address Bus (output, three-state, synchronous)

These pins supply nonmultiplexed memory or I/O addresses to the system one half of a CLKOUTA period earlier than the multiplexed address and data bus (AD15–AD0). During a bus hold or reset condition, the address bus is in a high-impedance state.

While the Am186ED/EDLV microcontrollers are directly connected to DRAM, A19–A0 will serve as the nonmultiplexed address bus for SRAM, FLASH, PROM, EPROM, and peripherals. The odd address pins (A17, A15, A13, A11, A9, A7, A5, A3, and A1) will have both the row and column address during a DRAM space access. The odd address signals connect directly to the row and column multiplexed address bus of the DRAM. The even address pins (A18, A16, A14, A12, A10, A8, A6, A4, A2, and A0) and A19 will have the initial address asserted during the full DRAM access. These signals will not transition during a DRAM access.

AD15–AD8

Address and Data Bus (input/output, three-state, synchronous, level-sensitive)

AD15–AD8—These time-multiplexed pins supply memory or I/O addresses and data to the system. This bus can supply an address to the system during the first period of a bus cycle (t_1). It supplies data to the system during the remaining periods of that cycle (t_2, t_3, and t_4).

The address phase of these pins can be disabled. See the $\overline{ADEN}$ description with the $\overline{BHE}$/$\overline{ADEN}$ pin. When $\overline{WHB}$ is deasserted, these pins are three-stated during t_2, t_3, and t_4.

During a bus hold or reset condition, the address and data bus is in a high-impedance state.

During a power-on reset, the address and data bus pins (AD15–AD0) can also be used to load system configuration information into the internal reset configuration register.

When accesses are made to 8-bit-wide memory regions, AD15–AD8 drive their corresponding address signals throughout the access. If the disable address phase and 8-bit mode are selected (see the $\overline{ADEN}$ description with the $\overline{BHE}$/$\overline{ADEN}$ pin), then AD15–AD8 are three-stated during t_1 and driven with their corresponding address signal from t_2 to t_4.

AD7–AD0

Address and Data Bus (input/output, three-state, synchronous, level-sensitive)

These time-multiplexed pins supply partial memory or I/O addresses, as well as data, to the system. This bus supplies the low-order 8 bits of an address to the system during the first period of a bus cycle (t_1), and it supplies data to the system during the remaining periods of that cycle (t_2, t_3, and t_4). In 8-bit mode, AD7–AD0 supplies the data for both high and low bytes.

The address phase of these pins can be disabled. See the $\overline{ADEN}$ pin description with the $\overline{BHE}$/$\overline{ADEN}$ pin. When $\overline{WLB}$ is deasserted, these pins are three-stated during t_2, t_3, and t_4.

During a bus hold or reset condition, the address and data bus is in a high-impedance state.

During a power-on reset, the address and data bus pins (AD15–AD0) can also be used to load system configuration information into the internal reset configuration register.

ALE

Address Latch Enable (output, synchronous)

This pin indicates to the system that an address appears on the address and data bus (AD15–AD0). The address is guaranteed to be valid on the trailing edge of ALE. This pin is three-stated during ONCE mode.

ALE is three-stated and held resistively Low during a bus hold condition. In addition, ALE has a weak internal pulldown resistor that is active during reset, so that an external device does not get a spurious ALE during reset.

ARDY

Asynchronous Ready (input, asynchronous, level-sensitive)

This pin is a true asynchronous ready that indicates to the microcontroller that the addressed memory space or I/O device will complete a data transfer. The ARDY pin is asynchronous to CLKOUTA and is active High. To guarantee the number of wait states inserted, ARDY or SRDY must be synchronized to CLKOUTA. If the falling edge of ARDY is not synchronized to CLKOUTA as specified, an additional clock period can be added.

To always assert the ready condition to the microcontroller, tie ARDY High. If the system does not use ARDY, tie the pin Low to yield control to SRDY.

$\overline{\text{BHE}}$/$\overline{\text{ADEN}}$

Bus High Enable (three-state, output, synchronous)
Address Enable (input, internal pullup)

$\overline{\text{BHE}}$—During a memory access, this pin and the least-significant address bit (AD0 or A0) indicate to the system which bytes of the data bus (upper, lower, or both) participate in a bus cycle. The $\overline{\text{BHE}}$/$\overline{\text{ADEN}}$ and AD0 pins are encoded as shown in Table 1.

Table 1. Data Byte Encoding

$\overline{\text{BHE}}$	AD0	Type of Bus Cycle
0	0	Word Transfer
0	1	High Byte Transfer (Bits 15–8)
1	0	Low Byte Transfer (Bits 7–0)
1	1	Reserved

$\overline{\text{BHE}}$ is asserted during t_1 and remains asserted through t_3 and t_W. $\overline{\text{BHE}}$ does not need to be latched. $\overline{\text{BHE}}$ floats during bus hold and reset.

$\overline{\text{WLB}}$ and $\overline{\text{WHB}}$ implement the functionality of $\overline{\text{BHE}}$ and AD0 for High and Low byte-write enables. $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ implement High and Low-byte selection for DRAM devices.

$\overline{\text{BHE}}$/$\overline{\text{ADEN}}$ also signals DRAM refresh cycles when using the multiplexed address and data (AD) bus. A refresh cycle is indicated when both $\overline{\text{BHE}}$/$\overline{\text{ADEN}}$ and AD0 are High. During refresh cycles, the A bus is indeterminate and the AD bus is driven to FFFFh during the address phase of the AD bus cycle. For this reason, the A0 signal cannot be used in place of the AD0 signal to determine refresh cycles.

$\overline{\text{ADEN}}$—If $\overline{\text{BHE}}$/$\overline{\text{ADEN}}$ is held High or left floating during power-on reset, the address portion of the AD bus (AD15–AD0) is enabled or disabled during $\overline{\text{LCS}}$ and $\overline{\text{UCS}}$ bus cycles based on the DA bit in the LMCS and UMCS registers. If the DA bit is set, the AD bus will not drive the address during t_1. There is a weak internal pullup resistor on $\overline{\text{BHE}}$/$\overline{\text{ADEN}}$ so no external pullup is required. Disabling the address phase reduces power consumption.

If $\overline{\text{BHE}}$/$\overline{\text{ADEN}}$ is held Low on power-on reset, the AD bus drives both addresses and data, regardless of the DA bit setting. The pin is sampled on the rising edge of $\overline{\text{RES}}$. (S6 and $\overline{\text{UZI}}$ also assume their normal functionality in this instance. See Table 2 on page 29.) The internal pullup on $\overline{\text{ADEN}}$ is ~9 kohm.

Note: *For 8-bit accesses, AD15–AD8 are driven with addresses during the t_2–t_4 bus cycle, regardless of the setting of the DA bit in the UMCS and LMCS registers.*

CLKOUTA

Clock Output A (output, synchronous)

This pin supplies the internal clock to the system. Depending on the value of the system configuration register (SYSCON), CLKOUTA operates at either the PLL frequency (X1), the power-save frequency, or is held Low. CLKOUTA remains active during reset and bus hold conditions.

All AC timing specs that use a clock relate to CLKOUTA.

CLKOUTB

Clock Output B (output, synchronous)

This pin supplies an additional clock with a delayed output compared to CLKOUTA. Depending upon the value of the system configuration register (SYSCON), CLKOUTB operates at either the PLL frequency (X1), the power-save frequency, or is held Low. CLKOUTB remains active during reset and bus hold conditions.

CLKOUTB is not used for AC timing specs.

$\overline{\text{CTS}}$0/$\overline{\text{ENRX}}$0/PIO21

Clear-to-Send 0 (input, asynchronous)
Enable-Receiver-Request 0 (input, asynchronous)

$\overline{\text{CTS}}$0—This pin provides the Clear-to-Send signal for asynchronous serial port 0 when the ENRX0 bit in the AUXCON register is 0 and hardware flow control is enabled for the port (FC bit in the serial port 0 control register is set). The $\overline{\text{CTS}}$0 signal gates the transmission of data from the associated serial port transmit register. When $\overline{\text{CTS}}$0 is asserted, the transmitter begins transmission of a frame of data, if any is available. If $\overline{\text{CTS}}$0 is deasserted, the transmitter holds the data in the serial port transmit register. The value of $\overline{\text{CTS}}$0 is checked only at the beginning of the transmission of the frame.

$\overline{\text{ENRX}}$0—This pin provides the Enable Receiver Request for asynchronous serial port 0 when the ENRX0 bit in the AUXCON register is 1 and hardware flow control is enabled for the port (FC bit in the serial

port 0 control register is set). The $\overline{ENRX0}$ signal enables the receiver for the associated serial port.

$\overline{DEN}$/$\overline{DS}$/PIO5

Data Enable (output, three-state, synchronous)
Data Strobe (output, three-state, synchronous)

$\overline{DEN}$—This pin supplies an output enable to an external data-bus transceiver. $\overline{DEN}$ is asserted during memory, I/O, and interrupt acknowledge cycles. $\overline{DEN}$ is deasserted when DT/$\overline{R}$ changes state. $\overline{DEN}$ floats during a bus hold or reset condition.

$\overline{DS}$—The data strobe provides a signal where the write cycle timing is identical to the read cycle timing. When used with other control signals, $\overline{DS}$ provides an interface for 68K-type peripherals without the need for additional system interface logic.

When $\overline{DS}$ is asserted, addresses are valid. When $\overline{DS}$ is asserted on writes, data is valid. When $\overline{DS}$ is asserted on reads, data can be asserted on the AD bus.

Note: *This pin resets to $\overline{DEN}$.*

DRQ0/INT5/PIO12

DMA Request 0 (input, synchronous, level-sensitive)
Maskable Interrupt Request 5 (input, asynchronous, edge-triggered)

DRQ0—This pin indicates to the microcontroller that an external device is ready for DMA channel 0 to perform a transfer. DRQ0 is level-triggered and internally synchronized. DRQ0 is not latched and must remain active until serviced.

INT5—If DMA 0 is not enabled or DMA 0 is not being used with external synchronization, INT5 can be used as an additional external interrupt request. INT5 shares the DMA 0 interrupt type (0Ah) and register control bits.

INT5 is edge-triggered only and must be held until the interrupt is acknowledged.

DRQ1/INT6/PIO13

DMA Request 1 (input, synchronous, level-sensitive)
Maskable Interrupt Request 6 (input, asynchronous, edge-triggered)

DRQ1—This pin indicates to the microcontroller that an external device is ready for DMA channel 1 to perform a transfer. DRQ1 is level-triggered and internally synchronized. DRQ1 is not latched and must remain active until serviced.

INT6—If DMA 1 is not enabled or DMA 1 is not being used with external synchronization, INT6 can be used as an additional external interrupt request. INT6 shares the DMA 1 interrupt type (0Bh) and register control bits.

INT6 is edge-triggered only and must be held until the interrupt is acknowledged.

DT/$\overline{R}$/PIO4

Data Transmit or Receive (output, three-state, synchronous)

This pin indicates in which direction data should flow through an external data-bus transceiver. When DT/$\overline{R}$ is asserted High, the microcontroller transmits data. When this pin is deasserted Low, the microcontroller receives data. DT/$\overline{R}$ floats during a bus hold or reset condition.

GND

Ground

Ground pins connect the microcontroller to the system ground.

HLDA

Bus Hold Acknowledge (output, synchronous)

This pin is asserted High to indicate to an external bus master that the microcontroller has released control of the local bus. When an external bus master requests control of the local bus (by asserting HOLD), the microcontroller completes the bus cycle in progress. It then relinquishes control of the bus to the external bus master by asserting HLDA and floating $\overline{DEN}$, $\overline{RD}$, $\overline{WR}$, $\overline{S}2$–$\overline{S}0$, AD15–AD0, S6, A19–A0, $\overline{BHE}$, $\overline{WHB}$, $\overline{WLB}$, and DT/$\overline{R}$. The following chip selects are three-stated (then will be held High with an ~10-kohm resistor): $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS}3$–$\overline{MCS}0$, $\overline{PCS}6$–$\overline{PCS}5$, $\overline{PCS}3$–$\overline{PCS}0$, $\overline{RAS}0$, $\overline{RAS}1$, $\overline{UCAS}$, and $\overline{LCAS}$. ALE is also three-stated (then will be held Low with an ~10-kohm resistor).

When the external bus master has finished using the local bus, it indicates this to the microcontroller by deasserting HOLD. The microcontroller responds by deasserting HLDA.

If the microcontroller requires access to the bus (for example, to refresh), it will deassert HLDA before the external bus master deasserts HOLD. The external bus master must be able to deassert HOLD and allow the microcontroller access to the bus. See the timing diagrams for bus hold on page 86.

HOLD

Bus Hold Request (input, synchronous, level-sensitive)

This pin indicates to the microcontroller that an external bus master needs control of the local bus.

The Am186ED/EDLV microcontrollers' HOLD latency time, that is, the time between HOLD request and HOLD acknowledge, is a function of the activity occurring in the processor when the HOLD request is received. A HOLD request is second only to DRAM

refresh requests in priority of activity requests received by the processor.

For more information, see the HLDA pin description on page 23.

INT0

Maskable Interrupt Request 0 (input, asynchronous)

This pin indicates to the microcontroller that an interrupt request has occurred. If the INT0 pin is not masked, the microcontroller transfers program execution to the location specified by the INT0 vector in the microcontroller interrupt vector table.

Interrupt requests are synchronized internally and can be edge-triggered or level-triggered. To guarantee interrupt recognition, the requesting device must continue asserting INT0 until the request is acknowledged.

INT1/$\overline{\text{SELECT}}$

Maskable Interrupt Request 1 (input, asynchronous)
Slave Select (input, asynchronous)

INT1—This pin indicates to the microcontroller that an interrupt request has occurred. If INT1 is not masked, the microcontroller transfers program execution to the location specified by the INT1 vector in the microcontroller interrupt vector table.

Interrupt requests are synchronized internally and can be edge-triggered or level-triggered. To guarantee interrupt recognition, the requesting device must continue asserting INT1 until the request is acknowledged.

$\overline{\text{SELECT}}$—When the microcontroller interrupt control unit is operating as a slave to an external interrupt controller, this pin indicates to the microcontroller that an interrupt type appears on the address and data bus. The INT0 pin must indicate to the microcontroller that an interrupt has occurred before the $\overline{\text{SELECT}}$ pin indicates to the microcontroller that the interrupt type appears on the bus.

INT2/$\overline{\text{INTA}}$0/PWD/PIO31

Maskable Interrupt Request 2 (input, asynchronous)
Interrupt Acknowledge 0 (output, synchronous)
Pulse Width Demodulator (input, Schmitt trigger)

INT2—This pin indicates to the microcontroller that an interrupt request has occurred. If the INT2 pin is not masked, the microcontroller transfers program execution to the location specified by the INT2 vector in the microcontroller interrupt vector table.

Interrupt requests are synchronized internally and can be edge-triggered or level-triggered. To guarantee interrupt recognition, the requesting device must continue asserting INT2 until the request is acknowledged. INT2 becomes $\overline{\text{INTA}}$0 when INT0 is configured in cascade mode.

$\overline{\text{INTA}}$0—When the microcontroller interrupt control unit is operating in cascade mode, this pin indicates to the system that the microcontroller needs an interrupt type to process the interrupt request on INT0. The peripheral issuing the interrupt request must provide the microcontroller with the corresponding interrupt type.

PWD—If pulse width demodulation is enabled, PWD processes a signal through the Schmitt trigger. PWD is used internally to drive TIMERIN0 and INT2, and PWD is inverted internally to drive TIMERIN1 and INT4. If INT2 and INT4 are enabled and timer 0 and timer 1 are properly configured, the pulse width of the alternating PWD signal can be calculated by comparing the values in timer 0 and timer 1.

In PWD mode, the signals TIMERIN0/PIO11, TIMERIN1/PIO0, and INT4/PIO30 can be used as PIOs. If they are not used as PIOs, they are ignored internally. The level of INT2/$\overline{\text{INTA}}$0/PWD/PIO31 is reflected in the PIO data register for PIO31 as if it was a PIO.

INT3/$\overline{\text{INTA}}$1/IRQ

Maskable Interrupt Request 3 (input, asynchronous)
Interrupt Acknowledge 1 (output, synchronous)
Slave Interrupt Request (output, synchronous)

INT3—This pin indicates to the microcontroller that an interrupt request has occurred. If the INT3 pin is not masked, the microcontroller then transfers program execution to the location specified by the INT3 vector in the microcontroller interrupt vector table.

Interrupt requests are synchronized internally, and can be edge-triggered or level-triggered. To guarantee interrupt recognition, the requesting device must continue asserting INT3 until the request is acknowledged. INT3 becomes $\overline{\text{INTA}}$1 when INT1 is configured in cascade mode.

$\overline{\text{INTA}}$1—When the microcontroller interrupt control unit is operating in cascade mode, this pin indicates to the system that the microcontroller needs an interrupt type to process the interrupt request on INT1. The peripheral issuing the interrupt request must provide the microcontroller with the corresponding interrupt type.

IRQ—When the microcontroller interrupt control unit is operating as a slave to an external master interrupt controller, this pin lets the microcontroller issue an interrupt request to the external master interrupt controller.

INT4/PIO30

Maskable Interrupt Request 4 (input, asynchronous)

This pin indicates to the microcontroller that an interrupt request has occurred. If the INT4 pin is not masked, the microcontroller then transfers program execution to the location specified by the INT4 vector in the microcontroller interrupt vector table.

Interrupt requests are synchronized internally, and can be edge-triggered or level-triggered. To guarantee interrupt recognition, the requesting device must continue asserting INT4 until the request is acknowledged.

When pulse width demodulation mode is enabled, the INT4 signal is used internally to indicate a High-to-Low transition on the PWD signal. When pulse width demodulation mode is enabled, INT4/PIO30 can be used as a PIO.

$\overline{\text{LCS}}$/$\overline{\text{ONCE}}$0/$\overline{\text{RAS}}$0

Lower Memory Chip Select (output, synchronous, internal pullup)
ONCE Mode Request 0 (input)
Row Address Strobe 0

$\overline{\text{LCS}}$—This pin indicates to the system that a memory access is in progress to the lower memory block. The base address and size of the lower memory block are programmable up to 512 Kbytes. $\overline{\text{LCS}}$ is configured for 8-bit or 16-bit bus size by the auxiliary configuration register.

$\overline{\text{LCS}}$ is three-stated and held resistively High during a bus hold condition. In addition, $\overline{\text{LCS}}$ has an ~9-kohm internal pullup resistor that is active during reset.

$\overline{\text{ONCE}}$0—During reset, this pin and $\overline{\text{ONCE}}$1 indicate to the microcontroller the mode in which it should operate. $\overline{\text{ONCE}}$0 and $\overline{\text{ONCE}}$1 are sampled on the rising edge of $\overline{\text{RES}}$. If both pins are asserted Low, the microcontroller enters ONCE mode; otherwise, it operates normally.

In ONCE mode, all pins assume a high-impedance state and remain in that state until a subsequent reset occurs. To guarantee that the microcontroller does not inadvertently enter ONCE mode, $\overline{\text{ONCE}}$0 has a weak internal pullup resistor that is active only during reset.

$\overline{\text{RAS}}$0—This pin is the row address strobe for the lower DRAM block. The selection of $\overline{\text{RAS}}$0 or $\overline{\text{LCS}}$ functionality, along with their configurations, are set using the LMCS register.

$\overline{\text{RAS}}$0 is three-stated and held resistively High during a bus hold condition. In addition, $\overline{\text{RAS}}$0 has a weak internal pullup resistor that is active during reset.

$\overline{\text{MCS}}$0/PIO14

Midrange Memory Chip Select 0 (output, synchronous, internal pullup)

This pin indicates to the system that a memory access is in progress to the corresponding region of the midrange memory block. The base address and size of the midrange memory block are programmable. $\overline{\text{MCS}}$0 can be programmed as the chip select for the entire middle chip select address range. This mode is recommended when using DRAM since the $\overline{\text{MCS}}$1, $\overline{\text{MCS}}$2, and $\overline{\text{MCS}}$3 chip selects function as $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals for the DRAM interface and are not available as chip selects.

$\overline{\text{MCS}}$0 is configured for 8-bit or 16-bit bus size by the auxiliary configuration register. $\overline{\text{MCS}}$0 is three-stated and held resistively High during a bus hold condition. In addition, $\overline{\text{MCS}}$0 has a weak internal pullup resistor that is active during reset.

$\overline{\text{MCS}}$1/$\overline{\text{UCAS}}$/PIO15

Midrange Memory Chip Select (output, synchronous, internal pullup)
Upper Column Address Strobe

This pin indicates to the system that a memory access is in progress to the corresponding region of the midrange memory block. The base address and size of the midrange memory block are programmable. $\overline{\text{MCS}}$1 is configured for 8-bit or 16-bit bus size via the auxiliary configuration register.

$\overline{\text{MCS}}$1 is three-stated and held resistively High during a bus hold condition. In addition, $\overline{\text{MCS}}$1 has a weak internal pullup resistor that is active during reset.

If $\overline{\text{MCS}}$0 is programmed to be active for the entire middle chip-select range, then this signal is available as a PIO or a DRAM control. If this signal is not programmed as a PIO or DRAM control and if $\overline{\text{MCS}}$0 is programmed for the entire middle chip-select range, this signal operates normally.

$\overline{\text{UCAS}}$—When either bank of DRAM is activated, the $\overline{\text{UCAS}}$ functionality is enabled. The $\overline{\text{UCAS}}$ activates when the DRAM access is for the AD15–AD8 byte. $\overline{\text{UCAS}}$ also activates at the start of a DRAM refresh access.

$\overline{\text{UCAS}}$ is three-stated and held resistively High during a bus hold condition. In addition, $\overline{\text{UCAS}}$ has a weak internal pullup resistor that is active during reset.

$\overline{\text{MCS}}$2/$\overline{\text{LCAS}}$/PIO24

Midrange Memory Chip Select (output, synchronous, internal pullup)
Lower Column Address Strobe

This pin indicates to the system that a memory access is in progress to the corresponding region of the midrange memory block. The base address and size of

the midrange memory block are programmable. $\overline{\text{MCS}}$2 is configured for 8-bit or 16-bit bus size via the auxiliary configuration register.

$\overline{\text{MCS}}$2 is three-stated and held resistively High during a bus hold condition. In addition, it has a weak internal pullup resistor that is active during reset.

If $\overline{\text{MCS}}$0 is programmed to be active for the entire middle chip-select range, then this signal is available as a PIO or a DRAM control. If this pin is not programmed as a PIO or DRAM control and if $\overline{\text{MCS}}$0 is programmed for the whole middle chip-select range, this signal operates normally.

$\overline{\text{LCAS}}$—When either bank of DRAM is activated, the $\overline{\text{LCAS}}$ functionality is enabled. The $\overline{\text{LCAS}}$ activates when the DRAM access is for the AD7–AD0 byte. $\overline{\text{LCAS}}$ also activates at the start of a DRAM refresh access.

$\overline{\text{LCAS}}$ is three-stated and held resistively High during a bus hold condition. In addition, $\overline{\text{LCAS}}$ has a weak internal pullup resistor that is active during reset.

$\overline{\text{MCS}}$3/$\overline{\text{RAS}}$1/PIO25

Midrange Memory Chip Select 3 (output, synchronous, internal pullup)
Row Address Strobe 1 (output, synchronous)

$\overline{\text{MCS}}$3—This pin indicates to the system that a memory access is in progress to the fourth region of the midrange memory block. The base address and size of the mid-range memory block are programmable. $\overline{\text{MCS}}$3 is configured for 8-bit or 16-bit bus size by the auxiliary configuration register.

$\overline{\text{MCS}}$3 is three-stated and held resistively High during a bus hold condition. In addition, this pin has a weak internal pullup resistor that is active during reset.

If $\overline{\text{MCS}}$0 is programmed for the entire middle chip-select range, then this signal is available as a PIO or a DRAM control. If $\overline{\text{MCS}}$3 is not programmed as a PIO or DRAM control and if $\overline{\text{MCS}}$0 is programmed for the entire middle chip-select range, this signal operates normally.

$\overline{\text{RAS}}$1—This pin is the row address strobe for the upper DRAM block. The selection of $\overline{\text{RAS}}$1 or $\overline{\text{UCS}}$ functionality, along with their configurations, are set using the UMCS register. When $\overline{\text{RAS}}$1 is activated, the code activating $\overline{\text{RAS}}$1 must not reside in the $\overline{\text{UCS}}$ memory block. When $\overline{\text{RAS}}$1 is activated, $\overline{\text{UCS}}$ is automatically deactivated and remains negated.

$\overline{\text{RAS}}$1 is three-stated and held resistively High during a bus hold condition. In addition, $\overline{\text{RAS}}$1 has a weak internal pullup resistor that is active during reset.

NMI

Nonmaskable Interrupt (input, synchronous, edge-sensitive)

This pin indicates to the microcontroller that an interrupt request has occurred. The NMI signal is the highest priority hardware interrupt and, unlike the INT6–INT0 pins, cannot be masked. The microcontroller always transfers program execution to the location specified by the nonmaskable interrupt vector in the microcontroller interrupt vector table when NMI is asserted.

Although NMI is the highest priority interrupt source, it does not participate in the priority resolution process of the maskable interrupts. There is no bit associated with NMI in the interrupt in-service or interrupt request registers. This means that a new NMI request can interrupt an executing NMI interrupt service routine. As with all hardware interrupts, the IF (interrupt flag) is cleared when the processor takes the interrupt, disabling the maskable interrupt sources. However, if maskable interrupts are re-enabled by software in the NMI interrupt service routine, via the STI instruction for example, the fact that an NMI is currently in service does not have any effect on the priority resolution of maskable interrupt requests. For this reason, it is strongly advised that the interrupt service routine for NMI should not enable the maskable interrupts.

An NMI transition from Low to High is latched and synchronized internally, and it initiates the interrupt at the next instruction boundary. To guarantee that the interrupt is recognized, the NMI pin must be asserted for at least one CLKOUTA period.

$\overline{\text{PCS}}$1/PIO17, $\overline{\text{PCS}}$0/PIO16

Peripheral Chip Selects (output, synchronous)

These pins indicate to the system that a memory access is in progress to the corresponding region of the peripheral memory block (either I/O or memory address space). The base address of the peripheral memory block is programmable.

The $\overline{\text{PCS}}$ chip selects can overlap either block of DRAM. The $\overline{\text{PCS}}$ chip selects must have the same or greater number of wait states as the bank of DRAM they overlap. The $\overline{\text{PCS}}$ signals take precedence over DRAM accesses when DRAM and memory-mapped peripherals overlap.

$\overline{\text{PCS}}$1–$\overline{\text{PCS}}$0 are three-stated and held resistively High during a bus hold condition. In addition, $\overline{\text{PCS}}$1–$\overline{\text{PCS}}$0 each have a weak internal pullup resistor that is active during reset.

Unlike the $\overline{\text{UCS}}$ and $\overline{\text{LCS}}$ chip selects, the $\overline{\text{PCS}}$ outputs assert with the multiplexed AD address bus. Note also that each peripheral chip select asserts over a 256-byte address range, which is twice the address range

covered by peripheral chip selects in the 80C186 and 80C188 microcontrollers. PCS0–PCS1 also have extended wait state options.

PCS2/CTS1/ENRX1/PIO18

Peripheral Chip Select 2 (output, synchronous)
Clear-to-Send 1 (input, asynchronous)
Enable-Receiver-Request 1 (input, asynchronous)

PCS2—This pin provides the Peripheral Chip Select 2 signal to the system when hardware flow control is not enabled for asynchronous serial port 1. The PCS2 signal indicates to the system that a memory access is in progress to the corresponding region of the peripheral memory block (either I/O or memory address space). The base address of the peripheral memory block is programmable.

The PCS chip selects can overlap either block of DRAM. The PCS chip selects must have the same or greater number of wait states as the bank of DRAM they overlap. The PCS signals take precedence over DRAM accesses when DRAM and memory-mapped peripherals overlap.

PCS2 is three-stated and held resistively High during a bus hold condition. In addition, PCS2 has a weak internal pullup resistor that is active during reset.

Unlike the UCS and LCS chip selects, the PCS outputs assert with the multiplexed AD address bus. Note also that each peripheral chip select asserts over a 256-byte address range, which is twice the address range covered by peripheral chip selects in the 80C186 and 80C188 microcontrollers. PCS2 also has extended wait state options.

CTS1—This pin provides the Clear-to-Send signal for asynchronous serial port 1 when the ENRX1 bit in the AUXCON register is 0 and hardware flow control is enabled for the port (FC bit in the serial port 1 control register is set). The CTS1 signal gates the transmission of data from the associated serial port transmit register. When CTS1 is asserted, the transmitter begins transmission of a frame of data, if any is available. If CTS1 is deasserted, the transmitter holds the data in the serial port transmit register. The value of CTS1 is checked only at the beginning of the transmission of the frame.

ENRX1—This pin provides the Enable Receiver Request for asynchronous serial port 1 when the ENRX1 bit in the AUXCON register is 1 and hardware flow control is enabled for the port (FC bit in the serial port 1 control register is set). The ENRX1 signal enables the receiver for the associated serial port.

PCS3/RTS1/RTR1/PIO19

Peripheral Chip Select 3 (output, synchronous)
Ready-to-Send 1 (output, asynchronous)
Ready-to-Receive 1 (output, asynchronous)

PCS3—This pin provides the Peripheral Chip Select 3 signal to the system when hardware flow control is not enabled for asynchronous serial port 1. The PCS3 signal indicates to the system that a memory access is in progress to the corresponding region of the peripheral memory block (either I/O or memory address space). The base address of the peripheral memory block is programmable.

The PCS chip selects can overlap either block of DRAM. The PCS chip selects must have the same or greater number of wait states as the bank of DRAM they overlap. The PCS signals take precedence over DRAM accesses when DRAM and memory-mapped peripherals overlap.

PCS3 is three-stated and held resistively High during a bus hold condition. In addition, PCS3 has a weak internal pullup resistor that is active during reset.

Unlike the UCS and LCS chip selects, the PCS outputs assert with the multiplexed AD address bus. Note also that each peripheral chip select asserts over a 256-byte address range, which is twice the address range covered by peripheral chip selects in the 80C186 and 80C188 microcontrollers. PCS3 also has extended wait state options.

RTS1—This pin provides the Ready-to-Send signal for asynchronous serial port 1 when the RTS1 bit in the AUXCON register is 1 and hardware flow control is enabled for the port (FC bit in the serial port 1 control register is set). The RTS1 signal is asserted when the associated serial port transmit register contains data which has not been transmitted.

RTR1—This pin provides the Ready-to-Receive signal for asynchronous serial port 1 when the RTS1 bit in the AUXCON register is 0 and hardware flow control is enabled for the port (FC bit in the serial port 1 control register is set). The RTR1 signal is asserted when the associated serial port receive register does not contain valid, unread data.

PCS5/A1/PIO3

Peripheral Chip Select 5 (output, synchronous)
Latched Address Bit 1 (output, synchronous)

PCS5—This pin indicates to the system that a memory access is in progress to the sixth region of the peripheral memory block (either I/O or memory address space). The base address of the peripheral memory block is programmable.

The PCS chip selects can overlap either block of DRAM. The PCS chip selects must have the same or greater number of wait states as the bank of DRAM

they overlap. The $\overline{PCS}$ signals take precedence over DRAM accesses when DRAM and memory-mapped peripherals overlap.

$\overline{PCS}5$ is three-stated and held resistively High during a bus hold condition. In addition, $\overline{PCS}5$ has a weak internal pullup resistor that is active during reset.

Unlike the $\overline{UCS}$ and $\overline{LCS}$ chip selects, the $\overline{PCS}$ outputs assert with the multiplexed AD address bus. Note also that each peripheral chip select asserts over a 256-byte address range, which is twice the address range covered by peripheral chip selects in the 80C186 and 80C188 microcontrollers. $\overline{PCS}5$ also has extended wait state options.

A1—When the EX bit in the $\overline{MCS}$ and $\overline{PCS}$ auxiliary register is 0, this pin supplies an internally latched address bit 1 to the system. During a bus hold condition, A1 retains its previously latched value.

$\overline{PCS}6$/A2/PIO2

Peripheral Chip Select 6 (output, synchronous)
Latched Address Bit 2 (output, synchronous)

$\overline{PCS}6$—This pin indicates to the system that a memory access is in progress to the seventh region of the peripheral memory block (either I/O or memory address space). The base address of the peripheral memory block is programmable.

The $\overline{PCS}$ chip selects can overlap either block of DRAM. The $\overline{PCS}$ chip selects must have the same or greater number of wait states as the bank of DRAM they overlap. The $\overline{PCS}$ signals take precedence over DRAM accesses when DRAM and memory-mapped peripherals overlap.

$\overline{PCS}6$ is three-stated and held resistively High during a bus hold condition. In addition, $\overline{PCS}6$ has a weak internal pullup resistor that is active during reset.

Unlike the $\overline{UCS}$ and $\overline{LCS}$ chip selects, the $\overline{PCS}$ outputs assert with the multiplexed AD address bus. Note also that each peripheral chip select asserts over a 256-byte address range, which is twice the address range covered by peripheral chip selects in the 80C186 and 80C188 microcontrollers. $\overline{PCS}6$ also has extended wait state options.

A2—When the EX bit in the $\overline{MCS}$ and $\overline{PCS}$ auxiliary register is 0, this pin supplies an internally latched address bit 2 to the system. During a bus hold condition, A2 retains its previously latched value.

PIO31–PIO0 (Shared)

Programmable I/O Pins (input/output, asynchronous, open-drain)

The Am186ED/EDLV microcontrollers provide 32 individually programmable I/O pins. Each PIO can be programmed with the following attributes: PIO function (enabled/disabled), direction (input/output), and weak pullup or pulldown. The pins that are multiplexed with PIO31–PIO0 are listed in Table 2 and Table 3.

After power-on reset, the PIO pins default to various configurations. The column titled *Power-On Reset Status* in Table 2 and Table 3 lists the defaults for the PIOs. Most of the PIO pins are configured as PIO inputs with pullup after power-on reset. The system initialization code must reconfigure any PIO pins as required.

The A19–A17 address pins default to normal operation on power-on reset, allowing the processor to correctly begin fetching instructions at the boot address FFFF0h. The DT/$\overline{R}$, $\overline{DEN}$, and SRDY pins also default to normal operation on power-on reset. PIO15 and PIO24 should be set to normal operation before enabling either bank of DRAM. PIO25 should be set to normal operation before enabling the upper bank of DRAM.

$\overline{RD}$

Read Strobe (output, synchronous, three-state)

$\overline{RD}$—This pin indicates to the system that the microcontroller is performing a memory or I/O read cycle. $\overline{RD}$ is guaranteed to not be asserted before the address and data bus is floated during the address-to-data transition. $\overline{RD}$ floats during a bus hold condition.

$\overline{RES}$

Reset (input, asynchronous, level-sensitive)

This pin requires the microcontroller to perform a reset. When $\overline{RES}$ is asserted, the microcontroller immediately terminates its present activity, clears its internal logic, and transfers CPU control to the reset address, FFFF0h.

$\overline{RES}$ must be held Low for at least 1 ms.

$\overline{RES}$ can be asserted asynchronously to CLKOUTA because $\overline{RES}$ is synchronized internally. For proper initialization, V_{CC} must be within specifications, and CLKOUTA must be stable for more than four CLKOUTA periods during which $\overline{RES}$ is asserted.

The microcontroller begins fetching instructions approximately 6.5 CLKOUTA periods after $\overline{RES}$ is deasserted. This input is provided with a Schmitt trigger to facilitate power-on $\overline{RES}$ generation via an RC network.

Table 2. Numeric PIO Pin Designations

PIO No	Associated Pin	Power-On Reset Status
0	TMRIN1	Input with pullup
1	TMROUT1	Input with pulldown
2	$\overline{PCS}$6/A2	Input with pullup
3	$\overline{PCS}$5/A1	Input with pullup
4	DT/$\overline{R}$	Normal operation(3)
5	$\overline{DEN}$/$\overline{DS}$	Normal operation(3)
6	SRDY	Normal operation(4)
7(1)	A17	Normal operation(3)
8(1)	A18	Normal operation(3)
9(1)	A19	Normal operation(3)
10	TMROUT0	Input with pulldown
11	TMRIN0	Input with pullup
12	DRQ0/INT5	Input with pullup
13	DRQ1/INT6	Input with pullup
14	$\overline{MCS}$0	Input with pullup
15	$\overline{MCS}$1/$\overline{UCAS}$	Input with pullup
16	$\overline{PCS}$0	Input with pullup
17	$\overline{PCS}$1	Input with pullup
18	$\overline{PCS}$2/$\overline{CTS}$1/$\overline{ENRX}$1	Input with pullup
19	$\overline{PCS}$3/$\overline{RTS}$1/$\overline{RTR}$1	Input with pullup
20	$\overline{RTS}$0/$\overline{RTR}$0	Input with pullup
21	$\overline{CTS}$0/$\overline{ENRX}$0	Input with pullup
22	TXD0	Input with pullup
23	RXD0	Input with pullup
24	$\overline{MCS}$2/$\overline{LCAS}$	Input with pullup
25	$\overline{MCS}$3/$\overline{RAS}$1	Input with pullup
26(1,2)	$\overline{UZI}$	Input with pullup
27	TXD1	Input with pullup
28	RXD1	Input with pullup
29(1,2)	S6/$\overline{CLKDIV}$2	Input with pullup
30	INT4	Input with pullup
31	INT2/$\overline{INTA}$0/PWD	Input with pullup

Table 3. Alphabetic PIO Pin Designations

Associated Pin	PIO No	Power-On Reset Status
A17(1)	7	Normal operation(3)
A18(1)	8	Normal operation(3)
A19(1)	9	Normal operation(3)
$\overline{CTS}$0/$\overline{ENRX}$0	21	Input with pullup
$\overline{DEN}$/$\overline{DS}$	5	Normal operation(3)
DRQ0/INT5	12	Input with pullup
DRQ1/INT6	13	Input with pullup
DT/$\overline{R}$	4	Normal operation(3)
INT2/$\overline{INTA}$0/PWD	31	Input with pullup
INT4	30	Input with pullup
$\overline{MCS}$0	14	Input with pullup
$\overline{MCS}$1/$\overline{UCAS}$	15	Input with pullup
$\overline{MCS}$2/$\overline{LCAS}$	24	Input with pullup
$\overline{MCS}$3/$\overline{RAS}$1	25	Input with pullup
$\overline{PCS}$0	16	Input with pullup
$\overline{PCS}$1	17	Input with pullup
$\overline{PCS}$2/$\overline{CTS}$1/$\overline{ENRX}$1	18	Input with pullup
$\overline{PCS}$3/$\overline{RTS}$1/$\overline{RTR}$1	19	Input with pullup
$\overline{PCS}$5/A1	3	Input with pullup
$\overline{PCS}$6/A2	2	Input with pullup
$\overline{RTS}$0/$\overline{RTR}$0	20	Input with pullup
RXD0	23	Input with pullup
RXD1	28	Input with pullup
S6/$\overline{CLKDIV}$2(1,2)	29	Input with pullup
SRDY	6	Normal operation(4)
TMRIN0	11	Input with pullup
TMRIN1	0	Input with pullup
TMROUT0	10	Input with pulldown
TMROUT1	1	Input with pulldown
TXD0	22	Input with pullup
TXD1	27	Input with pullup
$\overline{UZI}$(1,2)	26	Input with pullup

Notes:

The following notes apply to both tables.

1. *These pins are used by many emulators. (Emulators also use $\overline{S2}$–$\overline{S0}$, $\overline{RES}$, NMI, CLKOUTA, $\overline{BHE}$, ALE, AD15–AD0, and A16–A0.)*
2. *These pins revert to normal operation if $\overline{BHE}$/$\overline{ADEN}$ is held Low during power-on reset.*
3. *When used as a PIO, input with pullup option available.*
4. *When used as a PIO, input with pulldown option available.*

RTS0/RTR0/PIO20

Ready-to-Send 0 (output, asynchronous)
Ready-to-Receive 0 (output, asynchronous)

RTS0—This pin provides the Ready-to-Send signal for asynchronous serial port 0 when the RTS0 bit in the AUXCON register is 1 and hardware flow control is enabled for the port (FC bit in the serial port 0 control register is set). The RTS0 signal is asserted when the associated serial port transmit register contains data that has not been transmitted.

RTR0—This pin provides the Ready-to-Receive signal for asynchronous serial port 0 when the RTS0 bit in the AUXCON register is 0 and hardware flow control is enabled for the port (FC bit in the serial port 0 control register is set). The RTR0 signal is asserted when the associated serial port receive register does not contain valid, unread data.

RXD0/PIO23

Receive Data 0 (input, asynchronous)

This pin supplies asynchronous serial receive data from the system to asynchronous serial port 0.

RXD1/PIO28

Receive Data 1 (input, asynchronous)

This pin supplies asynchronous serial receive data from the system to asynchronous serial port 1.

S2/BTSEL

Bus Cycle Status (output, three-state, synchronous)
Boot Mode Select

S2—This pin indicates to the system the type of bus cycle in progress. S2 can be used as a logical memory or I/O indicator. S2–S0 float during bus hold and hold acknowledge conditions. The S2–S0 pins are encoded as shown in Table 4.

BTSEL—The Am186ED/EDLV microcontrollers can boot from 8- or 16-bit wide nonvolatile memory, based on the state of the BTSEL pin. If BTSEL is pulled High or left floating, an internal pullup sets the boot mode option to 16-bit. If BTSEL is pulled resistively Low during reset, the 8-bit boot mode option is selected. The status of the BTSEL pin is latched on the rising edge of reset. If 8-bit mode is selected, the width of the memory region associated with UCS can be changed in the AUXCON register.

This signal should never be tied to V_{CC} or V_{SS} directly since this pin is driven during normal operation. This signal should be tied Low with an external resistor if the 8-bit boot mode is to be used. The internal pullup resistor on BTSEL is ~9 kohm.

S1–S0

Bus Cycle Status (output, three-state, synchronous)

These pins indicate to the system the type of bus cycle in progress. S1 can be used as a data transmit or receive indicator. S1–S0 float during bus hold and hold acknowledge conditions. The S2–S0 pins are encoded as shown in Table 4.

Table 4. Bus Cycle Encoding

S2/BTSEL	S1	S0	Bus Cycle
0	0	0	Interrupt acknowledge
0	0	1	Read data from I/O
0	1	0	Write data to I/O
0	1	1	Halt
1	0	0	Instruction fetch
1	0	1	Read data from memory
1	1	0	Write data to memory
1	1	1	None (passive)

S6/CLKDIV2/PIO29

Bus Cycle Status Bit 6 (output, synchronous)
Clock Divide by 2 (input, internal pullup)

S6—During the second and remaining periods of a cycle (t_2, t_3, and t_4), this pin is asserted High to indicate a DMA-initiated bus cycle. During a bus hold or reset condition, S6 floats.

CLKDIV2—If S6/CLKDIV2/PIO29 is held Low during power-on reset, the chip enters clock divided by 2 mode where the processor clock is derived by dividing the external clock input by 2. If this mode is selected, the PLL is disabled. The pin is sampled on the rising edge of RES.

If S6 is to be used as PIO29 in input mode, the device driving PIO29 must not drive the pin Low during power-on reset. S6/CLKDIV2/PIO29 defaults to a PIO input with pullup, so the pin does not need to be driven High externally.

SRDY/PIO6

Synchronous Ready (input, synchronous, level-sensitive)

This pin indicates to the microcontroller that the addressed memory space or I/O device will complete a data transfer. The SRDY pin accepts an active High input synchronized to CLKOUTA.

Using SRDY instead of ARDY allows a relaxed system timing because of the elimination of the one-half clock period required to internally synchronize ARDY. To always assert the ready condition to the

microcontroller, tie SRDY High. If the system does not use SRDY, tie the pin Low to yield control to ARDY.

TMRIN0/PIO11

Timer Input 0 (input, synchronous, edge-sensitive)

This pin supplies a clock or control signal to the internal microcontroller timer 0. After internally synchronizing a Low-to-High transition on TMRIN0, the microcontroller increments the timer. TMRIN0 must be tied High if not being used. When PIO11 is enabled, TMRIN0 is pulled High internally.

TMRIN0 is driven internally by INT2/$\overline{\text{INTA}}$0/PWD when pulse width demodulation mode is enabled. The TMRIN0/PIO11 pin can be used as a PIO when pulse width demodulation mode is enabled.

TMRIN1/PIO0

Timer Input 1 (input, synchronous, edge-sensitive)

This pin supplies a clock or control signal to the internal microcontroller timer 1. After internally synchronizing a Low-to-High transition on TMRIN1, the microcontroller increments the timer. TMRIN1 must be tied High if not being used. When PIO0 is enabled, TMRIN1 is pulled High internally.

TMRIN1 is driven internally by INT2/$\overline{\text{INTA}}$0/PWD when pulse width demodulation mode is enabled. The TMRIN1/PIO0 pin can be used as a PIO when pulse width demodulation mode is enabled.

TMROUT0/PIO10

Timer Output 0 (output, synchronous)

This pin supplies the system with either a single pulse or a continuous waveform with a programmable duty cycle. TMROUT0 is floated during a bus hold or reset.

TMROUT1/PIO1

Timer Output 1 (output, synchronous)

This pin supplies the system with either a single pulse or a continuous waveform with a programmable duty cycle. TMROUT1 floats during a bus hold or reset.

TXD0/PIO22

Transmit Data 0 (output, asynchronous)

This pin supplies asynchronous serial transmit data to the system from serial port 0.

TXD1/PIO27

Transmit Data 1 (output, asynchronous)

This pin supplies asynchronous serial transmit data to the system from serial port 1.

$\overline{\text{UCS}}$/$\overline{\text{ONCE}}$1

Upper Memory Chip Select (output, synchronous)
ONCE Mode Request 1 (input, internal pullup)

$\overline{\text{UCS}}$—This pin indicates to the system that a memory access is in progress to the upper memory block. The base address and size of the upper memory block are programmable up to 512 Kbytes.

$\overline{\text{UCS}}$ is three-stated and held resistively High during a bus hold condition. In addition, $\overline{\text{UCS}}$ has an ~9-kohm internal pullup resistor that is active during reset.

After reset, $\overline{\text{UCS}}$ is active for the 64 Kbyte memory range from F0000h to FFFFFh, including the reset address of FFFF0h.

When $\overline{\text{RAS}}$1 is activated, the code activating $\overline{\text{RAS}}$1 must not reside in the $\overline{\text{UCS}}$ memory block. When $\overline{\text{RAS}}$1 is activated, $\overline{\text{UCS}}$ is automatically deactivated and remains negated. This allows code to boot from $\overline{\text{UCS}}$, copy its code to another memory device, then activate a DRAM bank in place of the $\overline{\text{UCS}}$ memory block.

$\overline{\text{ONCE}}$1—During reset, this pin and $\overline{\text{LCS}}$/$\overline{\text{ONCE}}$0 indicate to the microcontroller the mode in which it should operate. $\overline{\text{ONCE}}$0 and $\overline{\text{ONCE}}$1 are sampled on the rising edge of $\overline{\text{RES}}$. If both pins are asserted Low, the microcontroller enters ONCE mode. Otherwise, it operates normally. In ONCE mode, all pins assume a high-impedance state and remain in that state until a subsequent reset occurs. To guarantee that the microcontroller does not inadvertently enter ONCE mode, $\overline{\text{ONCE}}$1 has a weak internal pullup resistor that is active only during a reset.

$\overline{\text{UZI}}$/PIO26

Upper Zero Indicate (output, synchronous)

This pin lets the designer determine if an access to the interrupt vector table is in progress by ORing it with bits 15–10 of the address and data bus (AD15–AD10). $\overline{\text{UZI}}$ is the logical AND of the inverted A19–A16 bits. It asserts in the first period of a bus cycle and is held throughout the cycle.

V_{CC}

Power Supply (input)

These pins supply power (+5 V) to the microcontroller.

$\overline{\text{WHB}}$

Write High Byte (output, three-state, synchronous)

This pin and $\overline{\text{WLB}}$ indicate to the system which bytes of the data bus (upper, lower, or both) participate in a write cycle. In 80C186 microcontroller designs, information is provided by $\overline{\text{BHE}}$, AD0, and $\overline{\text{WR}}$. However, by using $\overline{\text{WHB}}$ and $\overline{\text{WLB}}$, the standard system interface logic and external address latch that were required are eliminated.

$\overline{WHB}$ is asserted with AD15–AD8. $\overline{WHB}$ is the logical OR of $\overline{BHE}$ and $\overline{WR}$. This pin floats during reset.

$\overline{WLB}$

Write Low Byte (output, three-state, synchronous)

$\overline{WLB}$—This pin and $\overline{WHB}$ indicate to the system which bytes of the data bus (upper, lower, or both) participate in a write cycle. In 80C186 microcontroller designs, this information is provided by $\overline{BHE}$, AD0, and $\overline{WR}$. However, by using $\overline{WHB}$ and $\overline{WLB}$, the standard system interface logic and external address latch that were required are eliminated.

$\overline{WLB}$ is asserted with AD7–AD0. $\overline{WLB}$ is the logical OR of AD0 and $\overline{WR}$. This pin floats during reset.

$\overline{WR}$

Write Strobe (output, synchronous)

$\overline{WR}$—This pin indicates to the system that the data on the bus is to be written to a memory or I/O device. $\overline{WR}$ floats during a bus hold or reset condition. $\overline{WR}$ should be used for DRAM write enable.

X1

Crystal Input (input)

This pin and the X2 pin provide connections for a fundamental mode or third-overtone, parallel-resonant crystal used by the internal oscillator circuit. To provide the microcontroller with an external clock source, connect the source to the X1 pin and leave the X2 pin unconnected.

X2

Crystal Output (output)

This pin and the X1 pin provide connections for a fundamental mode or third-overtone, parallel-resonant crystal used by the internal oscillator circuit. To provide the microcontroller with an external clock source, leave the X2 pin unconnected and connect the source to the X1 pin.

FUNCTIONAL DESCRIPTION

The Am186ED/EDLV microcontrollers are based on the architecture of the 80C186 and 80C188 microcontrollers. The Am186ED/EDLV microcontrollers function in the enhanced mode of earlier generations of 80C186 and 80C188 microcontrollers. Enhanced mode includes system features such as power-save control.

Each of the 8086, 8088, 80186, and 80188 microcontrollers contains the same basic set of registers, instructions, and addressing modes. The Am186ED/EDLV microcontrollers are backward-compatible with the 80C186 and 80C188 microcontrollers.

A full description of all the Am186ED/EDLV microcontroller registers and instructions is included in the *Am186ED/EDLV Microcontrollers User's Manual*, order# 21335A.

Memory Organization

Memory is organized in sets of segments. Each segment is a linear contiguous sequence of 64K (216) 8-bit bytes. Memory is addressed using a two-component address that consists of a 16-bit segment value and a 16-bit offset. The 16-bit segment values are contained in one of four internal segment registers (CS, DS, SS, or ES). The physical address is calculated by shifting the segment value left by 4 bits and adding the 16-bit offset value to yield a 20-bit physical address (see Figure 3). This allows for a 1-Mbyte physical address size.

All instructions that address operands in memory must specify the segment value and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for physical address generation is implied by the addressing mode used (see Table 5).

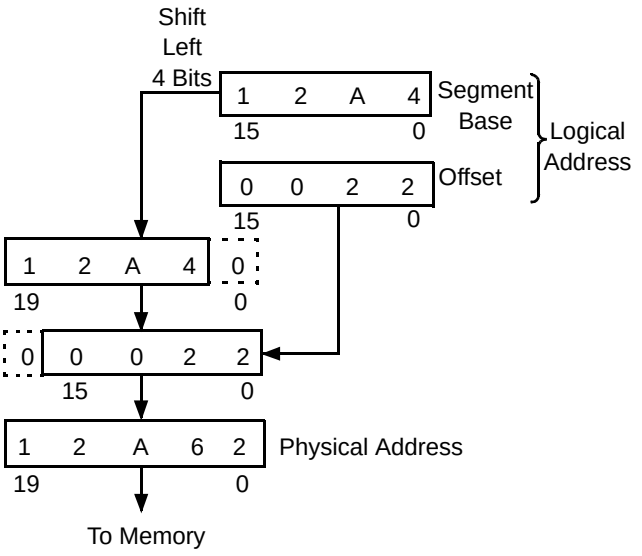


Figure 3. Two-Component Address

I/O Space

The I/O space consists of 64K 8-bit or 32K 16-bit ports. Separate instructions (IN, INS and OUT, OUTS) address the I/O space with either an 8-bit port address specified in the instruction, or a 16-bit port address in the DX register. Eight-bit port addresses are zero-extended such that A15–A8 are Low. I/O port addresses 00F8h through 00FFh are reserved.

Table 5. Segment Register Selection Rules

Memory Reference Needed	Segment Register Used	Implicit Segment Selection Rule
Instructions	Code (CS)	Instructions (including immediate data)
Local Data	Data (DS)	All data references
Stack	Stack (SS)	All stack pushes and pops; any memory references that use BP Register
External Data (Global)	Extra (ES)	All string instruction references that use the DI Register as an index

BUS OPERATION

The industry-standard 80C186 and 80C188 microcontrollers use a multiplexed address and data (AD) bus. The address is present on the AD bus only during the t_1 clock phase. The Am186ED/EDLV microcontrollers continue to provide the multiplexed AD bus and, in addition, provides a nonmultiplexed address (A) bus. The A bus provides an address to the system for the complete bus cycle (t_1–t_4).

For systems where power consumption is a concern, it is possible to disable the address from being driven on the AD bus during the normal address portion of the bus cycle for accesses to $\overline{\text{RAS}}$0, $\overline{\text{RAS}}$1, $\overline{\text{UCS}}$, and/or $\overline{\text{LCS}}$ address spaces. In this mode, the affected bus is placed in a high-impedance state during the address portion of the bus cycle. This feature is enabled through the DA bits in the UMCS and LMCS registers. When address disable is in effect, the number of signals that assert on the bus during all normal bus cycles to the associated address space is reduced, decreasing power consumption and reducing processor switching noise. In 8-bit mode, the address is driven on AD15–AD8 during the data portion of the bus cycle regardless of the setting of the DA bits.

If the $\overline{\text{ADEN}}$ pin is pulled Low during processor reset, the value of the DA bits in the UMCS and LMCS registers is ignored and the address is driven on the AD bus for all accesses, thus preserving the industry-standard 80C186 and 80C188 microcontrollers' multiplexed address bus and providing support for existing emulation tools.

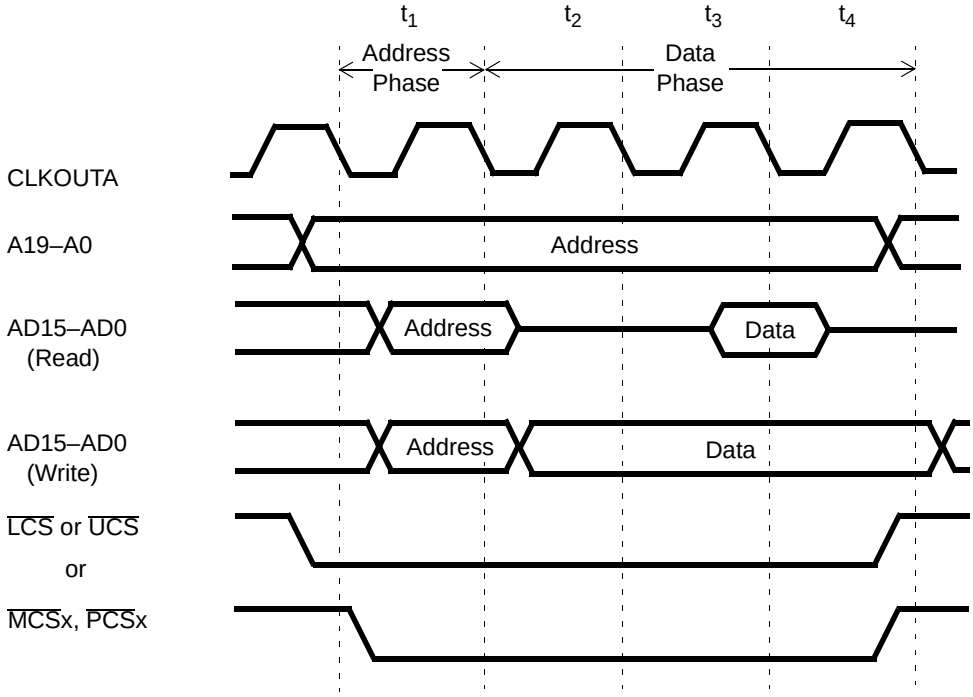
The following diagrams show the bus cycles of the Am186ED/EDLV microcontrollers when the address bus disable feature is in effect:

Figure 4 shows the affected signals during a normal read or write operation for 16-bit mode. The address and data are multiplexed onto the AD bus.

Figure 5 shows a 16-bit mode bus cycle when address bus disable is in effect. This results in the AD bus operating in a nonmultiplexed address/data mode. The A bus has the address during a read or write operation.

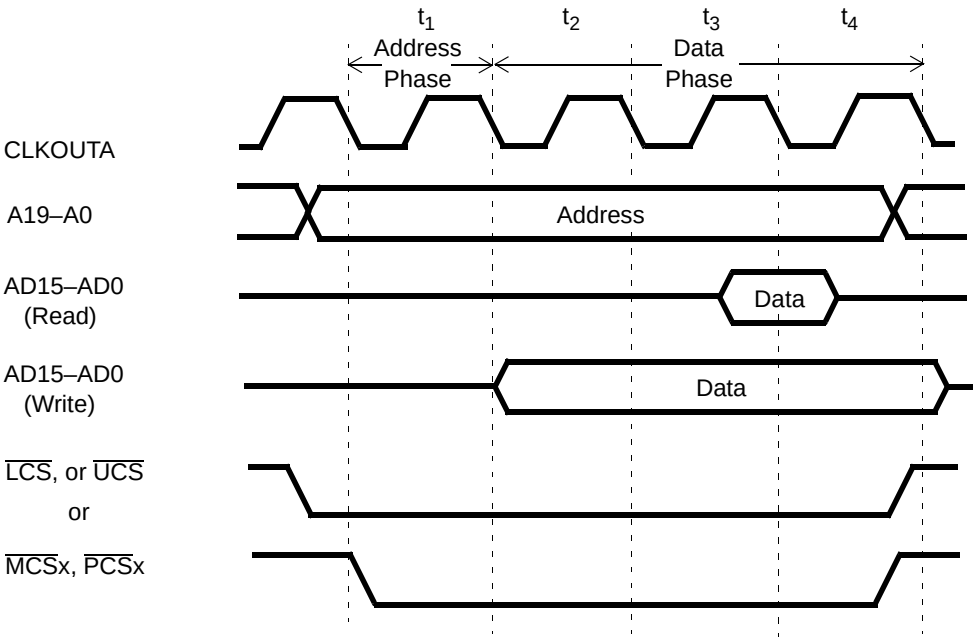
Figure 6 shows the affected signals during a normal read or write operation for 8-bit mode. The multiplexed address/data mode is compatible with the 80C186 and 80C188 microcontrollers and might be used to take advantage of existing logic or peripherals.

Figure 7 shows an 8-bit mode bus cycle when address bus disable is in effect. The address and data are not multiplexed. The AD7–AD0 signals have only data on the bus, while the AD bus has the address during a read or write operation.



Note: *For a detailed description of DRAM control signals, see DRAM switching characteristics beginning on page 70.*

Figure 4. 16-Bit Mode—Normal Read and Write Operation



Note: *For a detailed description of DRAM control signals, see DRAM switching characteristics beginning on page 70.*

Figure 5. 16-Bit Mode—Read and Write with Address Bus Disable In Effect

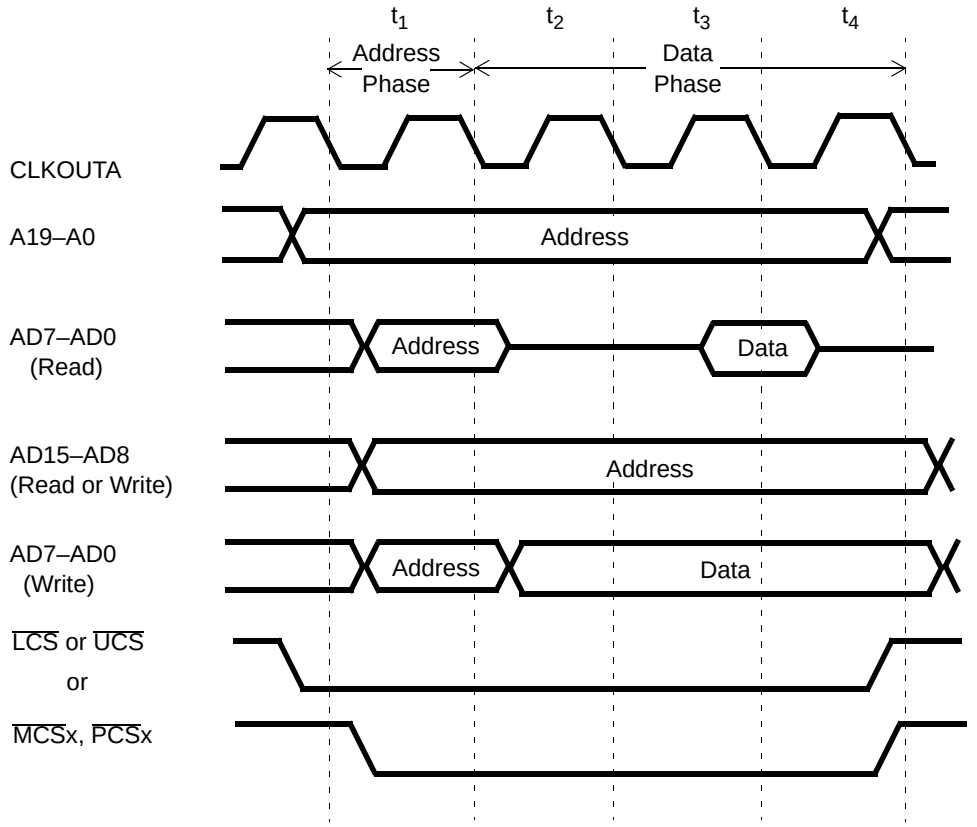


Figure 6. 8-Bit Mode—Normal Read and Write Operation

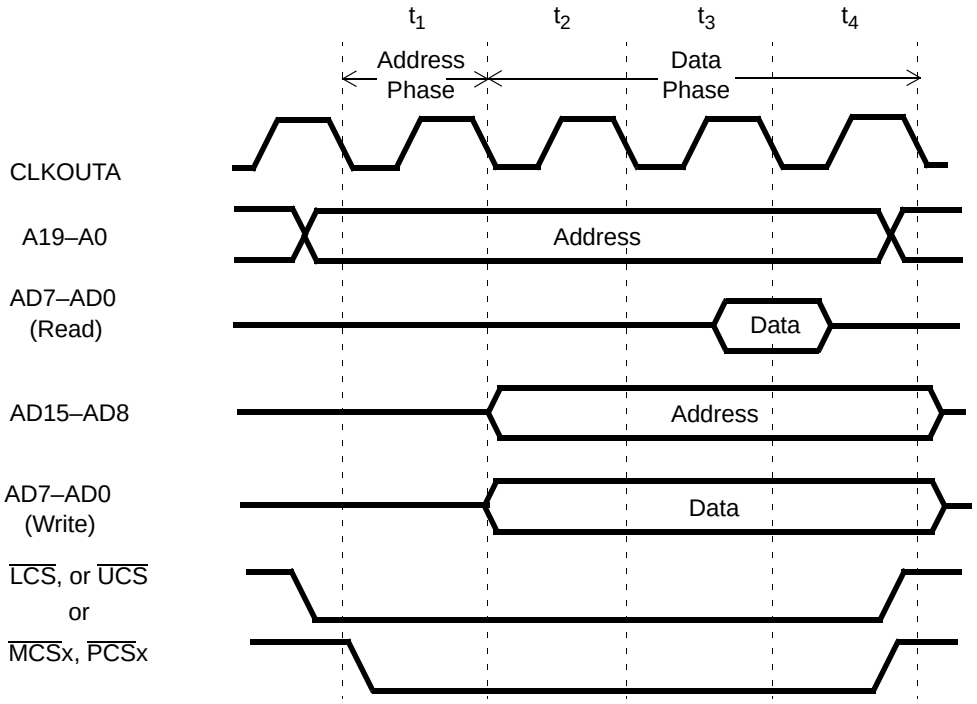


Figure 7. 8-Bit Mode—Read and Write with Address Bus Disable in Effect

BUS INTERFACE UNIT

The bus interface unit controls all accesses to external peripherals and memory devices. External accesses include those to memory devices, as well as those to memory-mapped and I/O-mapped peripherals and the peripheral control block. The Am186ED/EDLV microcontrollers provide an enhanced bus interface unit with the following features:

- A nonmultiplexed address bus
- DRAM address multiplexing
- A static bus-sizing option for 8-bit and 16-bit memory and I/O
- Separate byte write enables and $\overline{CAS}$ for High and Low bytes
- Data strobe bus interface option

The standard 80C186/188 microcontroller multiplexed address and data bus requires system interface logic and an external address latch. On the Am186ED/EDLV microcontrollers, new byte write enables, DRAM control logic, and a new nonmultiplexed address bus can reduce design costs by eliminating this external logic.

The standard 80C186/188 microcontroller required external DRAM controller logic and DRAM address multiplex circuitry for interfacing to DRAM. On the Am186ED/EDLV microcontrollers, the integrated DRAM controller and internal address multiplexing can reduce design costs by eliminating this external logic. Further, system costs can be reduced for systems using more than 64K of RAM by replacing SRAM with less expensive DRAM.

Nonmultiplexed Address Bus

The nonmultiplexed address bus (A19–A0) is valid one-half CLKOUTA cycle in advance of the address on the AD bus. When used in conjunction with the modified $\overline{UCS}$ and $\overline{LCS}$ outputs and the byte-write enable signals, the A19–A0 bus provides a seamless interface to SRAM, and Flash EPROM memory systems.

DRAM Address Multiplexing

The A19–A0 address bus also provides the addresses for the DRAM. When $\overline{RAS}$0 or $\overline{RAS}$1 asserts for a read or write, all the address signals are valid. This allows the DRAM to latch the odd addresses into the row address. Before the $\overline{UCAS}$ and/or $\overline{LCAS}$ asserts, the odd addresses A17–A1 change to reflect the even addresses. This allows the DRAM to latch in the even addresses into the column address. During a refresh cycle, the entire A19–A0 address bus is stable but undefined. The internal address and that reflected on the AD bus is all 1s. The DRAM pin interface is shown in Table 6.

Table 6. DRAM Pin Interface

AM186ED/EDLV Microcontroller Pins	DRAM Pin
A1	MA0
A3	MA1
A5	MA2
A7	MA3
A9	MA4
A11	MA5
A13	MA6
A15	MA7
A17	MA8
$\overline{RAS}$0	$\overline{RAS}$ (Bank 0)
$\overline{RAS}$1	$\overline{RAS}$ (Bank 1)
$\overline{UCAS}$	$\overline{UCAS}$ (AD15–AD8 Byte)
$\overline{LCAS}$	$\overline{LCAS}$ (AD7–AD0 Byte)
$\overline{RD}$	$\overline{OE}$
$\overline{WR}$	$\overline{WE}$

Programmable Bus Sizing

The Am186ED/EDLV microcontrollers allow programmability for data bus widths through fields in the Auxiliary Configuration Register (AUXCON) , as shown in Table 7. The USIZ bit in AUXCON is only configurable if the boot mode is 8-bit at reset.

The width of the data access should not be modified while the processor is fetching instructions from the associated address space.

Table 7. Programming the Bus Width of Am186ED/EDLV Microcontrollers

Space	AUXCON Field	Value	Bus Width	Comments
$\overline{UCS}$	USIZ	0	16 bits	Dependent on boot option[1]
		1	8 bits	
$\overline{LCS}$	LSIZ	0	16 bits	Default
		1	8 bits	
I/O	IOSIZ	0	16 bits	Default
		1	8 bits	
Other	MSIZ	0	16 bits	Default
		1	8 bits	

Note:

1. *$\overline{UCS}$ width on reset is determined by the $\overline{S2}$/BTSEL pin. If $\overline{UCS}$ boots as a 16-bit space, it is not re-configurable to 8-bit.*

Byte-Write Enables

The Am186ED/EDLV microcontrollers provide the $\overline{WHB}$ (Write High Byte) and $\overline{WLB}$ (Write Low Byte) signals, which act as byte-write enables.

$\overline{WHB}$ is the logical OR of $\overline{BHE}$ and $\overline{WR}$. $\overline{WHB}$ is Low when $\overline{BHE}$ and $\overline{WR}$ are both Low. $\overline{WLB}$ is the logical OR of A0 and $\overline{WR}$. $\overline{WLB}$ is Low when A0 and $\overline{WR}$ are both Low.

The byte-write enables are driven in conjunction with the nonmultiplexed address bus as required for the write timing requirements of common SRAMs.

Data Strobe Bus Interface Option

The Am186ED/EDLV microcontrollers provide an asynchronous bus interface that allows the use of 68K-type peripherals. This implementation combines a $\overline{DS}$ data strobe signal (multiplexed with $\overline{DEN}$) with an asynchronous ARDY ready input. When $\overline{DS}$ is asserted, the data and address signals are valid.

A chip select signal, ARDY, $\overline{DS}$, and other control signals ($\overline{RD}$/$\overline{WR}$) can control the interface of 68K-type external peripherals to the AD bus.

DRAM INTERFACE

The Am186ED/EDLV microcontrollers support up to two banks of DRAM. The use of DRAM can significantly reduce the memory costs for applications using more than 64K of RAM. No performance is lost except for the slight overhead of periodically refreshing the DRAM. The lower bank of DRAM uses the $\overline{LCS}$ space. The upper bank of DRAM uses the $\overline{UCS}$ space. Either, neither, or both banks can be activated. When either bank is activated, the $\overline{UCAS}$ and $\overline{LCAS}$ are enabled, and the DRAM address multiplexing is enabled on the A19–A0 bus. When DRAM is activated, the corresponding memory bus size should be set to 16-bit. The use of 8-bit-wide DRAM is not supported. All refreshes to DRAM are 7 clocks long. The refreshes must be separately enabled in the RCU.

The improved memory timing specifications of the Am186ED/EDLV microcontrollers allow for zero-wait-state operation using 50-ns DRAM at a 40-MHz clock speed. 60-ns DRAM requires one wait state at 40 MHz and zero wait states at 33 MHz and below. 70-ns DRAM requires two wait states at 40 MHz, one wait state at 33 MHz, and zero wait states at 25 MHz and below. This reduces overall system cost by enabling the use of commonly available memory speeds and taking advantage of DRAM's lower cost per bit over SRAM.

PERIPHERAL CONTROL BLOCK

The integrated peripherals of the Am186ED/EDLV microcontrollers are controlled by 16-bit read/write registers. The peripheral registers are contained within an internal 256-byte peripheral control block (PCB). The registers are physically located in the peripheral devices they control, but they are addressed as a single 256-byte block. Table 8 shows a map of these registers.

Reading and Writing the PCB

Code written for the Am186ED/EDLV microcontrollers should perform all writes to the PCB registers as byte writes. These writes transfer 16 bits of data to the PCB register even if an 8-bit register is named in the instruction. For example, `out dx, al` results in the value of `ax` being written to the port address in `dx`. Reads to the PCB should be done as word reads. Code written in this manner runs correctly on the Am186ED/EDLV microcontrollers with the PCB overlayed on either 8- or 16-bit address spaces.

Unaligned reads and writes to the PCB result in unpredictable behavior.

For a complete description of all the registers in the PCB, see the *Am186ED/EDLV Microcontrollers User's Manual*, order# 21335A.

Table 8. Peripheral Control Block Register Map

Register Name	Offset
Processor Control Registers:	
Peripheral control block relocation register	FEh
Reset configuration register	F6h
Processor release level register[1]	F4h
Auxiliary configuration register[1]	F2h
System configuration register[1]	F0h
Watchdog timer control register	E6h
Enable RCU register[1]	E4h
Clock prescaler register[1]	E2h
(*See note 2.*)	
DMA Registers:	
DMA 1 control register	DAh
DMA 1 transfer count register	D8h
DMA 1 destination address high register	D6h
DMA 1 destination address low register	D4h
DMA 1 source address high register	D2h
DMA 1 source address low register	D0h
DMA 0 control register	CAh
DMA 0 transfer count register	C8h
DMA 0 destination address high register	C6h
DMA 0 destination address low register	C4h
DMA 0 source address high register	C2h
DMA 0 source address low register	C0h
Chip-Select Registers:	
$\overline{PCS}$ and $\overline{MCS}$ auxiliary register	A8h
Midrange memory chip-select register	A6h
Peripheral chip-select register	A4h
Low memory chip-select register[1]	A2h
Upper memory chip-select register[1]	A0h
Serial Port 0 Registers:	
Serial port 0 baud rate divisor register	88h
Serial port 0 receive register	86h
Serial port 0 transmit register	84h
Serial port 0 status register	82h
Serial port 0 control register	80h
PIO Registers:	
PIO data 1 register	7Ah
PIO direction 1 register	78h
PIO mode 1 register	76h
PIO data 0 register	74h
PIO direction 0 register	72h
PIO mode 0 register	70h
Timer Registers:	
Timer 2 mode/control register	66h
Timer 2 max count compare A register	62h
Timer 2 count register	60h
Timer 1 mode/control register	5Eh
Timer 1 max count compare B register	5Ch
Timer 1 max count compare A register	5Ah
Timer 1 count register	58h
Timer 0 mode/control register	56h
Timer 0 max count compare B register	54h
Timer 0 max count compare A register	52h
Timer 0 count register	50h
Interrupt Registers:	
Serial port 0 interrupt control register	44h
Serial port 1 interrupt control register	42h
INT4 interrupt control register	40h
INT3 control register	3Eh
INT2 control register	3Ch
INT1 control register	3Ah
INT0 control register	38h
DMA1/INT6 interrupt control register	36h
DMA0/INT5 interrupt control register	34h
Timer interrupt control register	32h
Interrupt status register	30h
Interrupt request register	2Eh
Interrupt in-service register	2Ch
Interrupt priority mask register	2Ah
Interrupt mask register	28h
Interrupt poll status register	26h
Interrupt poll register	24h
End-of-interrupt register	22h
Interrupt vector register	20h
Serial Port 1 Registers:	
Serial port 1 baud rate divisor register	18h
Serial port 1 receive register	16h
Serial port 1 transmit register	14h
Serial port 1 status register	12h
Serial port 1 control register	10h

All unused addresses are reserved and should not be accessed.

Notes:

1. *The register has been modified from the Am186ES/ Am188ES microcontrollers.*
2. *The previous Memory Partition Register (MDRAM) has been removed and its functionality replaced with the $\overline{CAS}$-before-$\overline{RAS}$ refresh mode.*

CLOCK AND POWER MANAGEMENT

The clock and power management unit of the Am186ED/EDLV microcontrollers includes a phase-locked loop (PLL) and a second programmable system clock output (CLKOUTB).

Phase-Locked Loop

In a traditional 80C186/188 microcontroller design, the crystal frequency is twice that of the desired internal clock. Because of the PLL on the Am186ED/EDLV microcontrollers, the internal clock generated by the Am186ED/EDLV microcontrollers (CLKOUTA) is the same frequency as the crystal. The PLL takes the crystal inputs (X1 and X2) and generates a 45–55% (worst case) duty cycle intermediate system clock of the same frequency. This removes the need for an external 2x oscillator, reducing system cost. The PLL is reset during power-on reset by an on-chip power-on reset (POR) circuit.

Crystal-Driven Clock Source

The internal oscillator circuit of the Am186ED/EDLV microcontrollers is designed to function with a parallel resonant fundamental or third overtone crystal. Because of the PLL, the crystal frequency should be equal to the processor frequency. Do not replace a crystal with an LC or RC equivalent.

The X1 and X2 signals are connected to an internal inverting amplifier (oscillator) that provides, along with the external feedback loading, the necessary phase shift (Figure 8). In such a positive feedback circuit, the inverting amplifier has an output signal (X2) 180 degrees out of phase of the input signal (X1).

The external feedback network provides an additional 180-degree phase shift. In an ideal system, the input to X1 will have 360 or zero degrees of phase shift. The external feedback network is designed to be as close to ideal as possible. If the feedback network is not providing necessary phase shift, negative feedback dampens the output of the amplifier and negatively affects the operation of the clock generator. Values for the loading on X1 and X2 must be chosen to provide the necessary phase shift and crystal operation.

Selecting a Crystal

When selecting a crystal, the load capacitance should always be specified (C_L). This value can cause variance in the oscillation frequency from the desired specified value (resonance). The load capacitance and the loading of the feedback network have the following relationship:

$$C_L = \frac{(C_1 \cdot C_2)}{(C_1 + C_2)} + C_S$$

where C_S is the stray capacitance of the circuit. Placing the crystal and C_L in series across the inverting amplifier and tuning these values (C_1, C_2) allows the crystal to oscillate at resonance. This relationship is true for both fundamental and third-overtone operation. Finally, there is a relationship between C_1 and C_2. To enhance the oscillation of the inverting amplifier, these values need to be offset with the larger load on the output (X2). Equal values of these loads tend to balance the poles of the inverting amplifier.

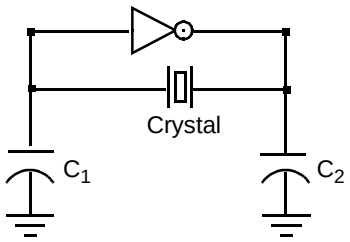
The characteristics of the inverting amplifier set limits on the following parameters for crystals:

ESR (Equivalent Series Resistance) ..... 60 Ω max
Drive Level ..... 1 mW max

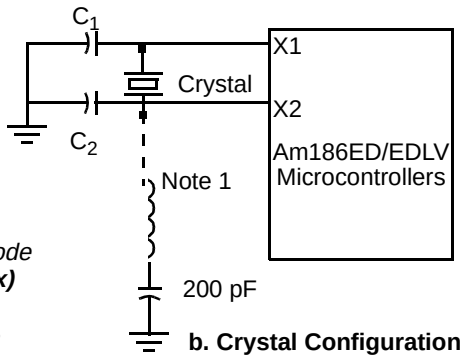
The recommended range of values for C_1 and C_2 are as follows:

C_1 ..... 15 pF ± 20%
C_2 ..... 22 pF ± 20%

The specific values for C_1 and C_2 must be determined by the designer and are dependent on the characteristics of the chosen crystal and board design.



a. Inverting Amplifier Configuration



b. Crystal Configuration

***Note 1**: Use for Third Overtone Mode*

XTAL Frequency	*L1 Value (Max)*
20 MHz	*12 µH ±20%*
25 MHz	*8.2 µH ±20%*
33 MHz	*4.7 µH ±20%*
40 MHz	*3.0 µH ±20%*

Figure 8. Am186ED/EDLV Microcontrollers Oscillator Configurations

External Source Clock

Alternately, the internal oscillator can be driven from an external clock source. This source should be connected to the input of the inverting amplifier (X1), with the output (X2) not connected.

System Clocks

The base system clock of AMD's original 80C186 and 80C188 microcontrollers is renamed CLKOUTA and the additional output is called CLKOUTB. CLKOUTA and CLKOUTB operate at either the processor frequency or the PLL frequency. The output drivers for both clocks are individually programmable for disable. Figure 9 shows the organization of the clocks.

The second clock output (CLKOUTB) allows one clock to run at the PLL frequency and the other clock to run at the power-save frequency. Individual drive enable bits allow selective enabling of just one or both of these clock outputs.

Power-Save Operation

The power-save mode of the Am186ED/EDLV microcontrollers reduces power consumption and heat dissipation, thereby extending battery life in portable systems. In power-save mode, operation of the CPU and internal peripherals continues at a slower clock frequency. When an interrupt occurs, the microcontroller automatically returns to its normal operating frequency on the internal clock's next rising edge of t_3.

Note: *Power-save operation requires that clock-dependent devices be reprogrammed for clock frequency changes. Software drivers must be aware of clock frequency. The power-save divisor should not be set to operate the processor core below 100 kHz.*

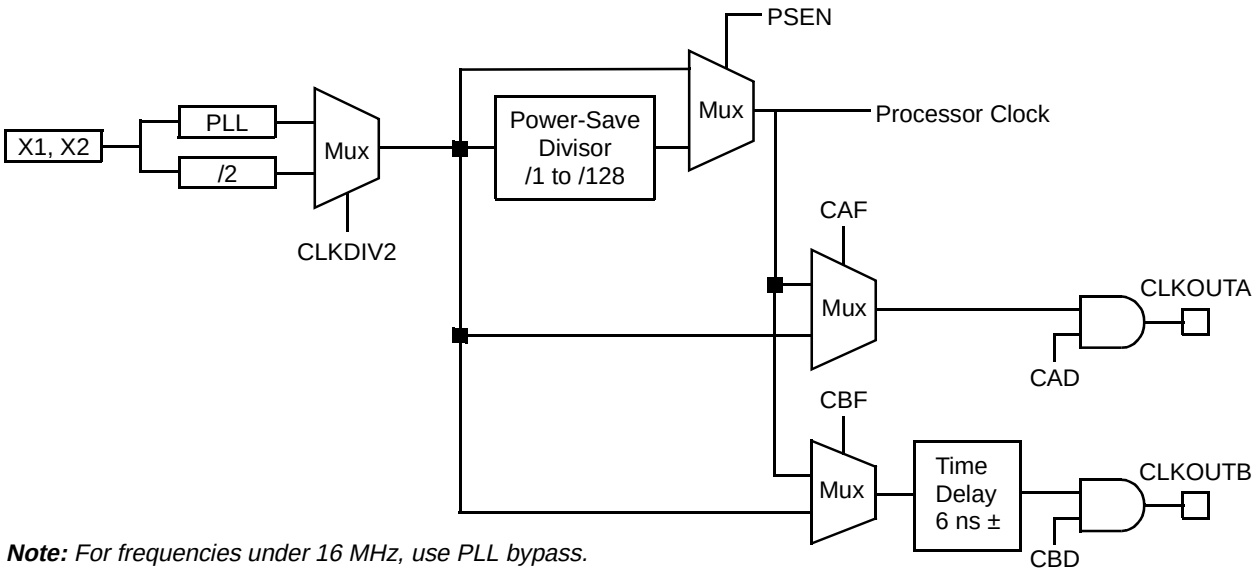
Initialization and Processor Reset

Processor initialization or startup is accomplished by driving the $\overline{RES}$ input pin Low. $\overline{RES}$ must be held Low for 1 ms during power-up to ensure proper device initialization. $\overline{RES}$ forces the Am186ED/EDLV microcontrollers to terminate all execution and local bus activity. No instruction or bus activity occurs as long as $\overline{RES}$ is active. After $\overline{RES}$ becomes inactive and an internal processing interval elapses, the microcontroller begins execution with the instruction at physical location FFFF0h, with $\overline{UCS}$ asserted with three wait states. $\overline{RES}$ also sets some registers to predefined values and resets the watchdog timer.

Reset Configuration Register

When the $\overline{RES}$ input is asserted Low, the contents of the address/data bus (AD15–AD0) are written into the reset configuration register. The system can place configuration information on the address/data bus using weak external pullup or pulldown resistors, or using an external driver that is enabled during reset. The processor does not drive the address/data bus during reset.

For example, the reset configuration register could be used to provide the software with the position of a configuration switch in the system. Using weak external pullup and pulldown resistors on the address and data bus, the system can provide the microcontroller with a value corresponding to the position of the jumper during a reset.



Note: *For frequencies under 16 MHz, use PLL bypass.*

Figure 9. Clock Organization

CHIP-SELECT UNIT

The Am186ED/EDLV microcontrollers contain logic that provides programmable chip-select generation for both memories and peripherals. The logic can be programmed to provide ready and wait-state generation and latched address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they are generated by the CPU or by the integrated DMA unit.

The Am186ED/EDLV microcontrollers provide six chip-select outputs for use with memory devices and six more for use with peripherals in either memory space or I/O space. The six memory chip selects can be used to address three memory ranges. Each peripheral chip select addresses a 256-byte block that is offset from a programmable base address. A write to a chip select register will enable the corresponding chip select logic even if the actual pin has another function (e.g., PIO).

Chip-Select Timing

The timing for the $\overline{UCS}$ and $\overline{LCS}$ outputs is modified from the original 80C186 microcontroller. These outputs now assert in conjunction with the nonmultiplexed address bus for normal memory timing. To allow these outputs to be available earlier in the bus cycle, the number of programmable memory size selections has been reduced.

Ready and Wait-State Programming

The Am186ED/EDLV microcontrollers can be programmed to sense a ready signal for each of the peripheral or memory chip-select lines. The ready signal can be either the ARDY or SRDY signal. Each chip-select control register (UMCS, LMCS, MMCS, PACS, and MPCS) contains a single-bit field that determines whether the external ready signal is required or ignored.

The number of wait states to be inserted for each access to a peripheral or memory region is programmable. The chip-select control registers for $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS}$3–$\overline{MCS}$0, $\overline{PCS}$6, and $\overline{PCS}$5 contain a two-bit field that determines the number of wait states from zero to three to be inserted. $\overline{PCS}$3–$\overline{PCS}$0 use three bits to provide additional values of 5, 7, 9, and 15 wait states.

When external ready is required, internally programmed wait states will always complete before external ready can terminate or extend a bus cycle. For example, if the internal wait states are set to insert two wait states, the processor samples the external ready pin during the first wait cycle. If external ready is asserted at that time, the access completes after six cycles (four cycles plus two wait states). If external ready is not asserted during the first wait cycle, the access is extended until ready is asserted, and one more wait state occurs followed by t_4.

The ARDY signal on the Am186ED/EDLV microcontrollers is a true asynchronous ready signal. The ARDY pin accepts a rising edge that is asynchronous to CLKOUTA and is active High. If the falling edge of ARDY is not synchronized to CLKOUTA as specified, an additional clock period may be added.

Chip-Select Overlap

Although programming the various chip selects on the Am186ED/EDLV microcontrollers so that multiple chip select signals are asserted for the same physical address is not recommended, it may be unavoidable in some systems. In such systems, the chip selects whose assertions overlap must have the same configuration for ready (external ready required or not required) and the number of wait states to be inserted into the cycle by the processor. The one exception to this is $\overline{PCS}$ overlapping DRAM.

The peripheral control block (PCB) is accessed using internal signals. These internal signals function as chip selects configured with zero wait states and no external ready. Therefore, the PCB can be programmed to addresses that overlap external chip-select signals only if those external chip selects are programmed to zero wait states with no external ready required.

When overlapping an additional chip select with either the $\overline{LCS}$ or $\overline{UCS}$ chip selects, it must be noted that setting the Disable Address (DA) bit in the LMCS or UMCS register disables the address from being driven on the AD bus for all accesses for which the associated chip select is asserted, including any accesses for which multiple chip selects assert.

The $\overline{MCS}$ and $\overline{PCS}$ chip-select pins can be configured as either chip selects (normal function) or as PIO inputs or outputs. It should be noted, however, that the ready and wait state generation logic for these chip selects is in effect regardless of their configurations as chip selects or PIOs. This means that if these chip selects are enabled (by a write to the MMCS and MPCS for the $\overline{MCS}$ chip selects, or by a write to the PACS and MPCS registers for the $\overline{PCS}$ chip selects), the ready and wait state programming for these signals must agree with the programming for any other chip selects with which their assertion would overlap if they were configured as chip selects.

Although the $\overline{PCS}$4 signal is not available on an external pin, the ready and wait state logic for this signal still exists internal to the part. For this reason, the $\overline{PCS}$4 address space must follow the rules for overlapping chip selects. The ready and wait-state logic for $\overline{PCS}$6–$\overline{PCS}$5 is disabled when these signals are configured as address bits A2–A1.

Failure to configure overlapping chip selects with the same ready and wait state requirements may cause

the processor to hang with the appearance of waiting for a ready signal. This behavior may occur even in a system in which ready is always asserted (ARDY or SRDY tied High).

Configuring $\overline{PCS}$ in I/O space with $\overline{LCS}$ or any other chip select configured for memory address 0 is not considered overlapping of the chip selects. Overlapping chip selects refers to configurations where more than one chip select asserts for the same physical address.

The $\overline{PCS}$ can overlap DRAM blocks with different wait states and without external or internal bus contention. The $\overline{RAS}$ will assert along with the appropriate $\overline{PCS}$. The $\overline{UCAS}$ and $\overline{LCAS}$ will not assert, preventing the DRAM from writing erroneously or driving the data bus during a read. The $\overline{PCS}$ must have the same or higher number of wait states than the DRAM. The $\overline{PCS}$ bus width will be determined by the LSIZ or USIZ bus widths. This will make a 1785-byte block of the DRAM inaccessible. In its place, the peripherals associated with the $\overline{PCS}$ can be accessed. This is especially useful when the entire memory space is used with two banks of DRAM or a bank of DRAM and a 512K Flash.

Upper Memory Chip Select

The Am186ED/EDLV microcontrollers provide a $\overline{UCS}$ chip select for the top of memory. On reset the Am186ED/EDLV microcontrollers begin fetching and executing instructions at memory location FFFF0h. Therefore, upper memory is usually used as instruction memory. To facilitate this usage, $\overline{UCS}$ defaults to active on reset, with a default memory range of 64 Kbytes from F0000h to FFFFFh, with external ready required and three wait states automatically inserted. The $\overline{UCS}$ memory range always ends at FFFFFh. The $\overline{UCS}$ lower boundary is programmable.

The bus width associated with $\overline{UCS}$ is determined on reset by the $\overline{S}$2/BTSEL. If $\overline{S}$2/BTSEL is pulled High or left floating, an internal pullup sets the boot mode option to 16-bit. If $\overline{S}$2/BTSEL is pulled resistively Low during reset, the boot mode option is for 8-bit. The status of the $\overline{S}$2/BTSEL pin is latched on the rising edge of reset. If 8-bit mode is selected, the width of the memory region associated with $\overline{UCS}$ can be changed in the AUXCON register. If $\overline{UCS}$ boots as a 16-bit space, it is not re-configurable to 8-bit. This allows for cheaper 8-bit-wide memory to be used for booting the Am186ED/EDLV microcontrollers, while speed-critical code and data can be executed from 16-bit-wide lower memory. Eight-bit or 16-bit-wide peripherals can be used in the memory area between $\overline{LCS}$ and $\overline{UCS}$ or in the I/O space. The entire memory map can be set to 16-bit or 8-bit or mixed between 8-bit and 16-bit based on the USIZ, LSIZ, MSIZ, and IOSIZ bits in the AUXCON register.

Low Memory Chip Select

The Am186ED/EDLV microcontrollers provide an $\overline{LCS}$ chip select for lower memory. The AUXCON register can be used to configure $\overline{LCS}$ for 8-bit or 16-bit accesses. Since the interrupt vector table is located at the bottom of memory starting at 00000h, the $\overline{LCS}$ pin is usually used to control data memory. The $\overline{LCS}$ pin is not active on reset.

The $\overline{LCS}$ signal is multiplexed with the $\overline{RAS}$0 signal when the DRAM mode is enabled in the LMCS register.

Midrange Memory Chip Selects

The Am186ED/EDLV microcontrollers provide four chip selects, $\overline{MCS}$3–$\overline{MCS}$0, for use in a user-locatable memory block. With some exceptions, the base address of the memory block can be located anywhere within the 1-Mbyte memory address space. The areas associated with the $\overline{UCS}$ and $\overline{LCS}$ chip selects are excluded. If they are mapped to memory, the address range of the peripheral chip selects, $\overline{PCS}$6, $\overline{PCS}$5, and $\overline{PCS}$3–$\overline{PCS}$0, are also excluded. The $\overline{MCS}$ address range can overlap the $\overline{PCS}$ address range if the $\overline{PCS}$ chip selects are mapped to I/O space.

$\overline{MCS}$0 can be configured to be asserted for the entire $\overline{MCS}$ range. When configured in this mode, the $\overline{MCS}$3–$\overline{MCS}$1 pins can be used as PIOs or DRAM control signals.

The AUXCON register can be used to configure $\overline{MCS}$ for 8-bit or 16-bit accesses. The bus width of the $\overline{MCS}$ range is determined by the width of the non-$\overline{UCS}$/non-$\overline{LCS}$ memory range.

Unlike the $\overline{UCS}$ and $\overline{LCS}$ chip selects, the $\overline{MCS}$ outputs assert with the same timing as the multiplexed AD address bus.

Activating either bank of DRAM will change the $\overline{MCS}$1 and $\overline{MCS}$2 functionality to $\overline{UCAS}$ and $\overline{LCAS}$. Activating the upper DRAM bank will change the $\overline{MCS}$3 functionality to $\overline{RAS}$1. It is recommended that when either bank of DRAM is activated, either $\overline{MCS}$0 be configured to assert for the entire $\overline{MCS}$ range or that $\overline{MCS}$ space be unused. If the lower bank of DRAM is activated, but not the upper bank of DRAM, $\overline{MCS}$3 can still be used as a chip select or PIO. The $\overline{MCS}$2 and $\overline{MCS}$1 portion of the middle chip select address space will not have a chip select signal asserted, but the wait states will still be valid.

Peripheral Chip Selects

The Am186ED/EDLV microcontrollers provide six chip selects, $\overline{PCS}$6–$\overline{PCS}$5 and $\overline{PCS}$3–$\overline{PCS}$0, for use within a user-configured memory or I/O block. $\overline{PCS}$4 is not available on the Am186ED/EDLV microcontrollers. The base address of the memory block can be located anywhere within the 1-Mbyte memory address space, exclusive of the areas associated with the $\overline{UCS}$, $\overline{LCS}$, and

MCS chip selects, or they can be configured to access the 64-Kbyte I/O space.

The PCS pins are not active on reset. PCS6–PCS5 can be programmed for zero to three wait states. PCS3–PCS0 can be programmed for four additional wait-state values: 5, 7, 9, and 15.

The AUXCON register can be used to configure PCS for 8-bit or 16-bit accesses. The bus width of the PCS range is determined by the width of the non-UCS/non-LCS memory range or by the width of the I/O area.

Unlike the UCS and LCS chip selects, the PCS outputs assert with the multiplexed AD address bus. Each peripheral chip select asserts over a 256-byte address range, which is twice the address range covered by peripheral chip selects in the 80C186/188 microcontrollers.

The PCS allows for overlap in memory space with the DRAM (RAS0, RAS1) space. Overlap of the PCS with LCS, MCS, or UCS in a non-DRAM mode is not recommended. If overlap of the PCS with MCS, LCS, or UCS occurs, the same number of wait states and external ready must be used. If overlap of PCS with DRAM space occurs, the DRAM controller will assert RAS and stop the CAS signal from asserting. This will not modify the contents of the DRAM and the access will continue as a normal PCS access. When overlapping the PCS with DRAM, the number of wait states can be different for PCS space. PCS wait states must be greater than or equal to DRAM wait states. The ready and wait states will be determined by the PCS programming in the MPCS and PACS registers.

PCS space should not contain the address FFFFFh, which is the address used for a refresh cycle. The AD15–AD0 bus will drive FFFFh during a refresh cycle for the address portion of cycle.

REFRESH CONTROL UNIT

The refresh control unit (RCU) automatically generates refresh bus cycles when enabled. After a programmable period of time, the RCU generates a CAS-before-RAS refresh bus cycle. The RCU should not be enabled if at least one bank of DRAM is not enabled. All refreshes will be 7 clocks, no matter how the DRAM wait states are programmed. During a refresh cycle, the A19–A0 bus is undefined; the AD15–AD0 bus is driven with all 1s (FFFFh). The PCS and MCS chip selects are decoded by the processor using a 20-bit version of the AD bus. The highest four bits of this internal bus are not available externally; however, internally these bits are set to all 1s during a refresh cycle, resulting in the 20-bit address FFFFFh. For this reason, the MCS and PCS chip selects should not contain the address FFFFFh while DRAM is enabled.

INTERRUPT CONTROL UNIT

The Am186ED/EDLV microcontrollers can receive interrupt requests from a variety of sources, both internal and external. The internal interrupt controller arranges these requests by priority and presents them one at a time to the CPU.

There are up to eight external interrupt sources on the Am186ED/EDLV microcontrollers—seven maskable interrupt pins and one nonmaskable interrupt (NMI) pin. In addition, there are eight internal interrupt sources (three timers, two DMA channels, two asynchronous serial ports, and the Watchdog Timer NMI) that are not connected to external pins. INT5 and INT6 are multiplexed with DRQ0 and DRQ1. These two interrupts are available if the associated DMA is not enabled or is being used with internal synchronization.

The Am186ED/EDLV microcontrollers provide up to six interrupt sources not present on the 80C186 and 80C188 microcontrollers. There are up to three additional external interrupt pins—INT4, INT5, and INT6. These pins operate much like the INT3–INT0 interrupt pins on the 80C186 and 80C188 microcontrollers. There are also two internal interrupts from the serial ports and the watchdog timer can generate interrupts.

INT5 and INT6 are multiplexed with the DMA request signals, DRQ0 and DRQ1. If a DMA channel is not enabled, or if it is not using external synchronization, then the associated pin can be used as an external interrupt. INT5 and INT6 can also be used in conjunction with the DMA terminal count interrupts.

The seven maskable interrupt request pins can be used as direct interrupt requests. INT4–INT0 can be either edge-triggered or level-triggered. INT6 and INT5 are edge-triggered only. In addition, INT0 and INT1 can be configured in cascade mode for use with an external 82C59A-compatible interrupt controller. When INT0 is configured in cascade mode, the INT2 pin is automatically configured in its INTA0 function. When INT1 is configured in cascade mode, the INT3 pin is automatically configured in its INTA1 function. An external interrupt controller can be used as the system master by programming the internal interrupt controller to operate in slave mode. INT6–INT4 are not available in slave mode.

Interrupts are automatically disabled when an interrupt is taken. Interrupt-service routines (ISRs) may re-enable interrupts by setting the IF flag. This allows interrupts of greater or equal priority to interrupt the currently executing ISR. Interrupts from the same source are disabled as long as the corresponding bit in the interrupt in-service register is set. INT1 and INT0 provide a special bit to enable special fully nested mode. When configured in special fully nested mode, the interrupt source may generate a new interrupt regardless of the setting of the in-service bit.

TIMER CONTROL UNIT

There are three 16-bit programmable timers and a watchdog timer on the Am186ED/EDLV microcontrollers.

Timer 0 and timer 1 are connected to four external pins (each one has an input and an output). These two timers can be used to count or time external events, or to generate nonrepetitive or variable-duty-cycle waveforms. When pulse width demodulation is enabled, timer 0 and timer 1 are used to measure the width of the High and Low pulses on the PWD pin. (See the Pulse Width Demodulation section on page 45.)

Timer 2 is not connected to any external pins. It can be used for real-time coding and time-delay applications. It can also be used as a prescaler to timers 0 and 1 or to synchronize DMA transfers.

The programmable timers are controlled by eleven 16-bit registers in the peripheral control block. A timer's timer-count register contains the current value of that timer. The timer-count register can be read or written with a value at any time, whether the timer is running or not. The microcontroller increments the value of the timer-count register each time a timer event occurs.

Each timer also has a maximum-count register that defines the maximum value the timer can reach. When the timer reaches the maximum value, it resets to 0 during the same clock cycle. The value in the maximum-count register is never stored in the timer-count register. Also, timers 0 and 1 have a secondary maximum-count register. Using both the primary and secondary maximum-count registers lets the timer alternate between two maximum values.

If the timer is programmed to use only the primary maximum-count register, the timer output pin switches Low for one clock cycle after the maximum value is reached. If the timer is programmed to use both of its maximum-count registers, the output pin indicates which maximum-count register is currently in control, thereby creating a waveform. The duty cycle of the waveform depends on the values in the maximum-count registers.

Each timer is serviced every fourth clock cycle, so a timer can operate at a speed of up to one-quarter of the internal clock frequency. A timer can be clocked externally at this same frequency; however, because of internal synchronization and pipelining of the timer circuitry, the timer output can take up to six clock cycles to respond to the clock or gate input.

Watchdog Timer

The Am186ED/EDLV microcontrollers provide a true watchdog timer function. The Watchdog Timer (WDT) can be used to regain control of the system when software fails to respond as expected. The WDT is active after reset. It can only be modified a single time by a keyed sequence of writes to the watchdog timer control register (WDTCON) following reset. This single write can either disable the timer or modify the timeout period and the action taken upon timeout. A keyed sequence is also required to reset the current WDT count. This behavior ensures that randomly executing code will not prevent a WDT event from occurring.

The WDT supports up to a 1.67-second timeout period in a 40-MHz system. After reset, the WDT is enabled and the timeout period is set to its maximum value.

The WDT can be configured to cause either an NMI interrupt or a system reset upon timeout. If the WDT is configured for NMI, the NMIFLAG in the WDTCON register is set when the NMI is generated. The NMI interrupt service routine (ISR) should examine this flag to determine if the interrupt was generated by the WDT or by an external source. If the NMIFLAG is set, the ISR should clear the flag by writing the correct keyed sequence to the WDTCON register. If the NMIFLAG is set when a second WDT timeout occurs, a WDT system reset is generated rather than a second NMI event.

When the processor takes a WDT reset, either due to a single WDT event with the WDT configured to generate resets or due to a WDT event with the NMIFLAG set, the RSTFLAG in the WDTCON register is set. This allows system initialization code to differentiate between a hardware reset and a WDT reset and take appropriate action. The RSTFLAG is cleared when the WDTCON register is read or written. The processor does not resample external pins during a WDT reset. This means that the clocking, the reset configuration register, and any other features that are user-selectable during reset do not change when a WDT system reset occurs. All other activities are identical to those of a normal system reset.

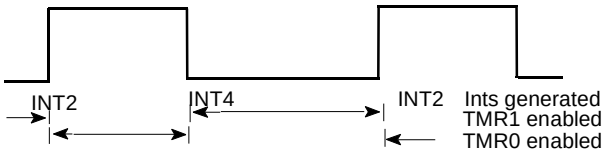
Note: *The Watchdog Timer (WDT) is active after reset.*

PULSE WIDTH DEMODULATION

For many applications, such as bar-code reading, it is necessary to measure the width of a signal in both its High and Low phases. The Am186ED/EDLV microcontrollers provide a pulse-width demodulation (PWD) option to fulfill this need. The PWD bit in the System Configuration Register (SYSCON) enables the PWD option. Analog-to-digital conversion is not supported.

In PWD mode, TMRIN0, TMRIN1, INT2, and INT4 are configured internal to the microcontroller to support the detection of rising and falling edges on the PWD input pin (INT2/$\overline{\text{INTA}}$0/PWD) and to enable either timer 0 when the signal is High or timer 1 when the signal is Low. The INT4, TMRIN0, and TMRIN1 pins are not used in PWD mode and so are available for use as PIOs.

The following diagram shows the behavior of a system for a typical waveform.



The interrupt service routine (ISR) for the INT2 and INT4 interrupts should examine the current count of the associated timer, timer 1 for INT2, and timer 0 for INT4, in order to determine the pulse width. The ISR should then reset the timer count register in preparation for the next pulse.

Since the timers count at one quarter of the processor clock rate, this determines the maximum resolution that can be obtained. Further, in applications where the pulse width may be short, it may be necessary to poll the INT2 and INT4 request bits in the interrupt request register in order to avoid the overhead involved in taking and returning from an interrupt. Overflow conditions, where the pulse width is greater than the maximum count of the timer, can be detected by monitoring the Maximum Count (MC) bit in the associated timer or by setting the INT bit to enable timer interrupt requests.

DIRECT MEMORY ACCESS

Direct memory access (DMA) permits transfer of data between memory and peripherals without CPU involvement. The DMA unit shown in Figure 10, provides two high-speed DMA channels. Data transfers can occur between memory and I/O spaces (e.g., memory to I/O) or within the same space (e.g., memory to memory or I/O to I/O). Table 9 shows maximum DMA transfer rates.

The DMA channels can be directly connected to the asynchronous serial ports. DMA and serial port transfer is accomplished by programming the DMA controller to perform transfers between a data source in memory or I/O space and a serial port transmit or receive register. The two DMA channels can support one serial port in full-duplex mode or two serial ports in half-duplex mode.

Either bytes or words can be transferred to or from even or odd addresses. However, word DMA transfers to or from memory configured for 8-bit accesses are not supported. Only two bus cycles (a minimum of eight clocks) are necessary for each data transfer.

Each channel accepts a DMA request from one of four sources: the channel request pin (DRQ1–DRQ0), Timer 2, a serial port, or the system software. The channels can be programmed with different priorities in the event of a simultaneous DMA request or if there is a need to interrupt transfers on the other channel.

DMA Operation

Each channel has six registers in the peripheral control block that define specific channel operations. The DMA registers consist of a 20-bit source address (two registers), a 20-bit destination address (two registers), a 16-bit transfer count register, and a 16-bit control register.

The DMA Transfer Count Register (DTC) specifies the number of DMA transfers to be performed. Up to 64K of byte or word transfers can be performed with automatic termination. The DMA control registers define the channel operation. All registers can be modified during any DMA activity. Any changes made to the DMA registers are reflected immediately in DMA operation.

Table 9. Am186ED/EDLV Microcontrollers Maximum DMA Transfer Rates

Type of Synchronization Selected	Maximum DMA Transfer Rate (Mbytes)			
	40 MHz	33 MHz	25 MHz	20 MHz
Unsynchronized	10	8.25	6.25	5
Source Synchronized	10	8.25	6.25	5
Destination Synchronized (CPU needs bus)	6.6	5.5	4.16	3.3
Destination Synch (CPU does not need bus)	8	6.6	5	4

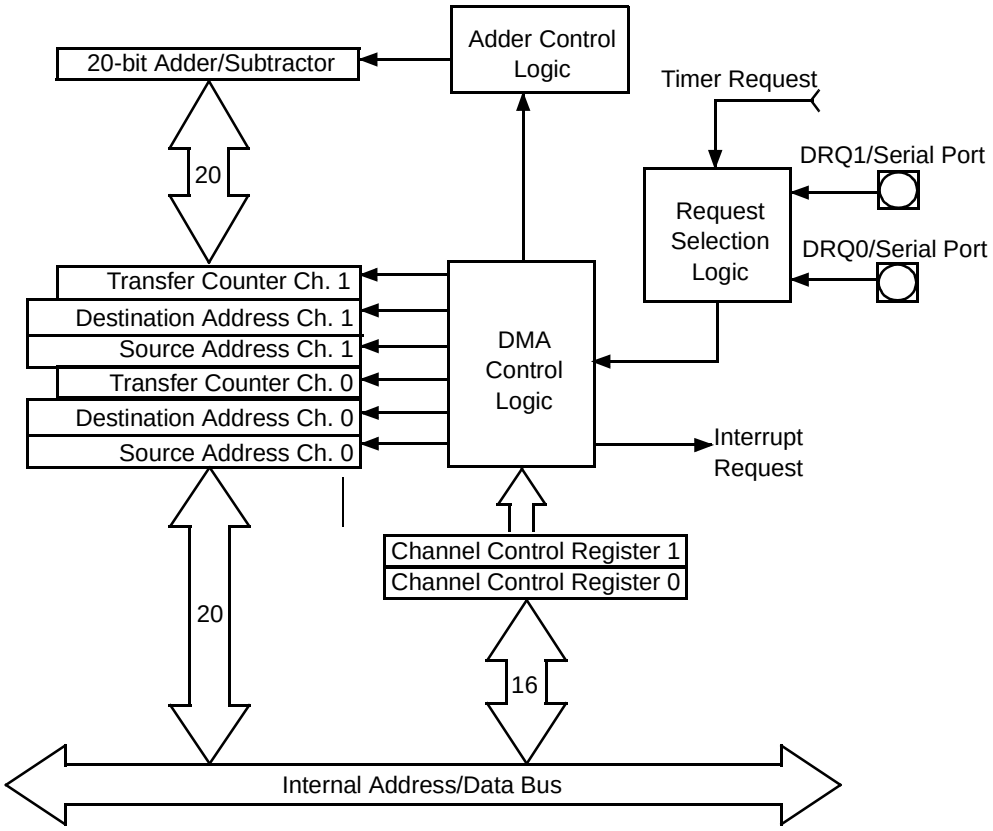


Figure 10. DMA Unit Block Diagram

DMA Channel Control Registers

Each DMA control register determines the mode of operation for the particular DMA channel. The DMA control registers specify the following:

- The mode of synchronization
- Whether bytes or words are transferred
- Whether an interrupt is generated after the last transfer
- Whether the DRQ pins are configured as INT pins
- Whether DMA activity ceases after a programmed number of DMA cycles
- The relative priority of the DMA channel with respect to the other DMA channel
- Whether the source address is incremented, decremented, or maintained constant after each transfer
- Whether the source address addresses memory or I/O space
- Whether the destination address is incremented, decremented, or maintained constant after transfers
- Whether the destination address addresses memory or I/O space

DMA Priority

The DMA channels can be programmed so that one channel is always given priority over the other, or they can be programmed to alternate cycles when both have DMA requests pending. DMA cycles always have priority over internal CPU cycles except between locked memory accesses or word accesses to odd memory locations. However, an external bus hold takes priority over an internal DMA cycle.

Because an interrupt request cannot suspend a DMA operation and the CPU cannot access memory during a DMA cycle, interrupt latency time suffers during sequences of continuous DMA cycles. An NMI request, however, causes all internal DMA activity to halt. This allows the CPU to respond quickly to the NMI request.

ASYNCHRONOUS SERIAL PORTS

The Am186ED/EDLV microcontrollers provide two independent asynchronous serial ports. These ports provide full-duplex, bidirectional data transfer using several industry-standard communications protocols. The serial ports can be used as sources or destinations of DMA transfers.

The asynchronous serial ports support the following features:

- Full-duplex operation
- Direct memory access (DMA) from the serial ports
- 7-bit, 8-bit, or 9-bit data transfers
- Odd, even, or no parity
- One stop bit
- Long or short break character recognition
- Error detection
  - — Parity errors
  - — Framing errors
  - — Overrun errors
  - — Break character recognition
- Hardware handshaking with the following selectable control signals:
  - — Clear-to-send ($\overline{CTS}$)
  - — Enable-receiver-request ($\overline{ENRX}$)
  - — Ready-to-send ($\overline{RTS}$)
  - — Ready-to-receive ($\overline{RTR}$)
- DMA to and from the serial ports
- Separate maskable interrupts for each port
- Multidrop protocol (9-bit) support
- Independent baud rate generators
- Maximum baud rate of 1/16th of the CPU clock
- Double-buffered transmit and receive
- Programmable interrupt generation for transmit, receive, and/or error detection

DMA Transfers through the Serial Port

The DMA channels can be directly connected to the asynchronous serial ports. DMA and serial port transfer is accomplished by programming the DMA controller to perform transfers between a memory or I/O space and a serial port transmit or receive register. The two DMA channels can support one serial port in full-duplex mode or two serial ports in half-duplex mode. See the DMA Control register descriptions in the *Am186ED/EDLV Microcontrollers User's Manual*, order# 21335A for more information.

PROGRAMMABLE I/O (PIO) PINS

There are 32 pins on the Am186ED/EDLV microcontrollers that are available as user-programmable I/O signals. Table 2 on page 29 and Table 3 on page 29 list the PIO pins. Each of these pins can be used as a user-programmable input or output signal if the normal shared function is not needed.

If a pin is enabled to function as a PIO signal, the preassigned signal function is disabled and does not affect the level on the pin. A PIO signal can be configured to operate as an input or output with or without a weak pullup or pulldown, or as an open-drain output.

After power-on reset, the PIO pins default to various configurations. The column titled *Power-On Reset Status* in Table 2 on page 29 and Table 3 on page 29 lists the defaults for the PIOs. The system initialization code must reconfigure the PIOs as required.

The A19–A17 address pins default to normal operation on power-on reset, allowing the processor to correctly begin fetching instructions at the boot address FFFF0h. The DT/$\overline{R}$, $\overline{DEN}$, and SRDY pins also default to normal operation on power-on reset.

Note that emulators use A19, A18, A17, S6, and $\overline{UZI}$. In environments where an emulator is needed, these pins must be configured for normal function—not as PIOs.

If the AD15–AD0 bus override is enabled on power-on reset, then S6/$\overline{CLKDIV2}$ and $\overline{UZI}$ revert to normal operation instead of PIO input with pullup. If $\overline{BHE}$/$\overline{ADEN}$ is held Low during power-on reset, the AD15–AD0 bus override is enabled.

When the $\overline{PCS}$ or $\overline{MCS}$ are used as PIO inputs (only) and the bus is arbitrated, an internal pullup of ~10 kohms is activated, even if the pullup option for the PIO is not selected.

ABSOLUTE MAXIMUM RATINGS

Storage temperature

Am186ED.....–65°C to +125°C
Am186EDLV.....–65°C to +125°C

Voltage on any pin with respect to ground

Am186ED.....–0.5 V to V_{cc} +0.5 V
Am186EDLV.....–0.5 V to V_{cc} +0.5 V

Note: *Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

OPERATING RANGES

Am186ED Microcontroller

Commercial (T_C).....0°C to +100°C
Industrial* (T_A).....–40°C to +85°C
Supply voltage (V_{CC}).....5 V ± 10%

Am186EDLV Microcontroller

Commercial (T_A).....0°C to +70°C
V_{CC} up to 25 MHz.....3.3 V ± 0.3 V

Where: T_C = case temperature
T_A = ambient temperature

**Industrial versions of Am186ED microcontrollers are available in 20 and 25 MHz operating frequencies only.*

DC CHARACTERISTICS OVER COMMERCIAL AND INDUSTRIAL OPERATING RANGES

Symbol	Parameter Description	Test Conditions	Preliminary Min	Preliminary Max	Unit
V_{IL}	Input Low Voltage (Except X1)		–0.5	$0.2V_{CC}$ –0.3	V
V_{IL1}	Clock Input Low Voltage (X1)		–0.5	0.8	V
V_{IH}	Input High Voltage (Except $\overline{RES}$ and X1)		2.0	V_{CC} +0.5	V
V_{IH1}	Input High Voltage ($\overline{RES}$)		2.4	V_{CC} +0.5	V
V_{IH2}	Clock Input High Voltage (X1)		V_{CC} –0.8	V_{CC} +0.5	V
V_{OL}	**Output Low Voltage**				
	Am186ED	I_{OL}= 2.5 mA ($\overline{S2}$–$\overline{S0}$) I_{OL}= 2.0 mA (others)		0.45	V
	Am186EDLV	I_{OL}= 1.5 mA ($\overline{S2}$–$\overline{S0}$) I_{OL}= 1.0 mA (others)		0.45	V
V_{OH}	**Output High Voltage**[a]				
	Am186ED	I_{OH}= –2.4 mA @ 2.4 V	2.4	V_{CC} +0.5	V
		I_{OH}= –200 µA @ V_{CC}–0.5	V_{CC} –0.5	V_{CC}	V
	Am186EDLV	I_{OH}= –200 µA @ V_{CC}–0.5	V_{CC} –0.5	V_{CC}	V
I_{CC}	Power Supply Current @ 0°C	V_{CC} = 5.5 V [b] V_{CC} = 3.6 V [b]		5.9 4.0	mA/MHz
I_{LI}	Input Leakage Current @ 0.5 MHz	0.45 V≤V_{IN}≤V_{CC}		±10	µA
I_{LO}	Output Leakage Current @ 0.5 MHz	0.45 V≤V_{OUT}≤V_{CC} [c]		±10	µA
V_{CLO}	Clock Output Low	I_{CLO}= 4.0 mA		0.45	V
V_{CHO}	Clock Output High	I_{CHO}= –500 µA	V_{CC} –0.5		V

Notes:

a The $\overline{LCS}$/$\overline{ONCE0}$/$\overline{RAS0}$ and $\overline{UCS}$/$\overline{ONCE1}$ pins have weak internal pullup resistors. Loading the $\overline{LCS}$/$\overline{ONCE0}$/$\overline{RAS0}$ and $\overline{UCS}$/$\overline{ONCE1}$ pins in excess of I_{OH} = –200 µA during reset can cause the device to go into ONCE mode.

b Current is measured with the device in RESET with X1 and X2 driven and all other non-power pins open but held High or Low.

c Testing is performed with the pins floating, either during HOLD or by invoking the ONCE mode.

CAPACITANCE

Symbol	Parameter Description	Test Conditions	Preliminary		Unit
			Min	Max	
C_{IN}	Input Capacitance	@ 1 MHz		10	pF
C_{IO}	Output or I/O Capacitance	@ 1 MHz		20	pF

Note:
Capacitance limits are guaranteed by characterization.

POWER SUPPLY CURRENT

For the following typical system specification shown in Figure 11, I_{CC} has been measured at 4.0 mA per MHz of system clock. For the following typical system specification shown in Figure 12, I_{CC} has been measured at 5.9 mA per MHz of system clock. The typical system is measured while the system is executing code in a typical application with nominal voltage and maximum case temperature. Actual power supply current is dependent on system design and may be greater or less than the typical I_{CC} figure presented here.

Typical current in Figure 11 is given by:

$I_{CC} = 4.0\ mA \cdot freq(MHz)$

Typical current in Figure 12 is given by:

$I_{CC} = 5.9\ mA \cdot freq(MHz)$

Please note that dynamic I_{CC} measurements are dependent upon chip activity, operating frequency, output buffer logic, and capacitive/resistive loading of the outputs. For these I_{CC} measurements, the devices were set to the following modes:

- No DC loads on the output buffers
- Output capacitive load set to 35 pF
- AD bus set to data only
- PIOs are disabled
- Timer, serial port, refresh, and DMA are enabled

Table 10 shows the variables that are used to calculate the typical power consumption value for the Am186EDLV microcontroller.

Table 10. Typical Power Consumption Calculation for the Am186EDLV Microcontroller

MHz · I_{CC} · Volts / 1000 = P			Typical Power in Watts
MHz	Typical I_{CC}	Volts	
20	4.0	3.6	0.288
25	4.0	3.6	0.360

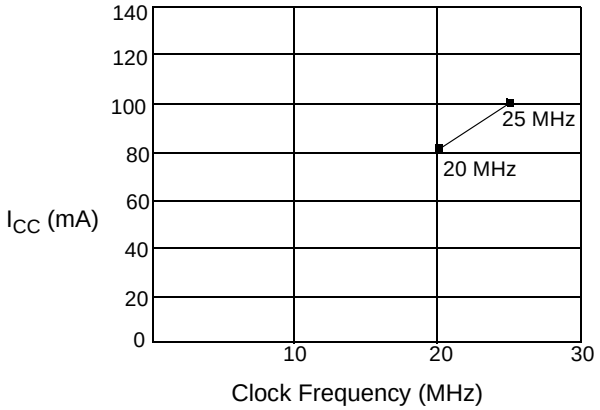


Figure 11. Typical I_{cc} Versus Frequency for Am186EDLV Microcontroller

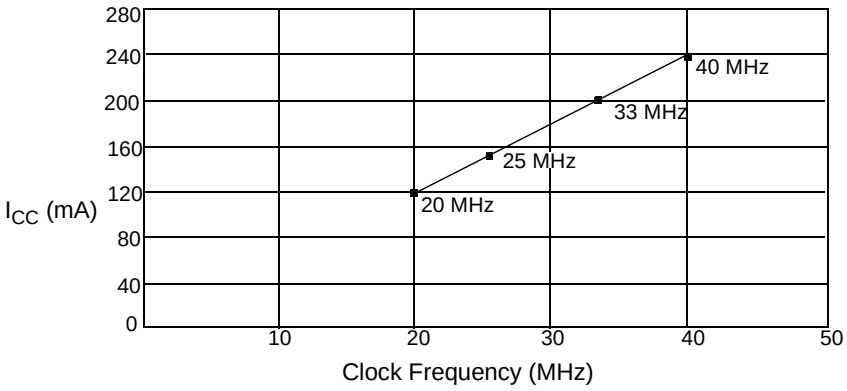


Figure 12. Typical I_{cc} Versus Frequency for Am186ED Microcontroller

THERMAL CHARACTERISTICS

TQFP Package

The Am186ED microcontroller is specified for operation with case temperature ranges from 0°C to +100°C for a commercial device. Case temperature is measured at the top center of the package as shown in Figure 13. The various temperatures and thermal resistances can be determined using the equations in Figure 14 with information given in Table 11.

The total thermal resistance is θ_{JA}; θ_{JA} is the sum of θ_{JC}, the internal thermal resistance of the assembly, and θ_{CA}, the case to ambient thermal resistance.

The variable *P* is power in watts. Power supply current (I_{CC}) is in mA per MHz of clock frequency.

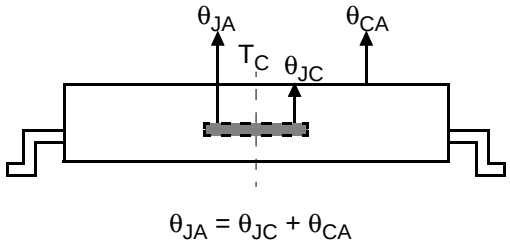


Figure 13. Thermal Resistance (°C/Watt)

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$
$$P = I_{CC} \cdot \text{freq (MHz)} \cdot V_{CC}$$
$$T_J = T_C + (P \cdot \theta_{JC})$$
$$T_J = T_A + (P \cdot \theta_{JA})$$
$$T_C = T_J - (P \cdot \theta_{JC})$$
$$T_C = T_A + (P \cdot \theta_{CA})$$
$$T_A = T_J - (P \cdot \theta_{JA})$$
$$T_A = T_C - (P \cdot \theta_{CA})$$

Figure 14. Thermal Characteristics Equations

Table 11. Thermal Characteristics (°C/Watt)

Package/Board	Airflow (Linear Feet per Minute)	θ_{JA}	θ_{JC}	θ_{CA}
PQFP/2-Layer	0 fpm	45	7	38
	200 fpm	39	7	32
	400 fpm	35	7	28
	600 fpm	33	7	26
TQFP/2-Layer	0 fpm	56	10	46
	200 fpm	46	10	36
	400 fpm	40	10	30
	600 fpm	38	10	28
PQFP/4-Layer to 6-Layer	0 fpm	23	5	18
	200 fpm	21	5	16
	400 fpm	19	5	14
	600 fpm	17	5	12
TQFP/4-Layer to 6-Layer	0 fpm	30	6	24
	200 fpm	28	6	22
	400 fpm	26	6	20
	600 fpm	24	6	18

Typical Ambient Temperatures

The typical ambient temperature specifications are based on the following assumptions and calculations:

The commercial operating range of the Am186ED microcontroller is a case temperature T_C of 0 to 100 degrees Centigrade. T_C is measured at the top center of the package. An increase in the ambient temperature causes a proportional increase in T_C.

Microcontrollers up to 40 MHz are specified as 5.0 V plus or minus 10%. Therefore, 5.0 V is used for calculating typical power consumption up to 40 MHz.

Typical power supply current (I_{CC}) in normal usage is estimated at 5.9 mA per MHz of microcontroller clock rate.

Typical power consumption (watts) = (5.9 mA/MHz) times microcontroller clock rate times V_{CC} divided by 1000.

Table 12 shows the variables that are used to calculate the typical power consumption value for each version of the Am186ED microcontroller.

Table 12. Typical Power Consumption Calculation

$P = MHz \cdot I_{CC} \cdot V_{CC}/1000$			Typical Power (P) in Watts
MHz	Typical I_{CC}	Volts	
40	5.9	5.0	1.2
33	5.9	5.0	1.0
25	5.9	5.0	0.7
20	5.9	5.0	0.6

Thermal resistance is a measure of the ability of a package to remove heat from a semiconductor device. A safe operating range for the device can be calculated using the formulas from Figure 14 and the variables in Table 11.

By using the maximum case rating T_C, the typical power consumption value from Table 12, and θ_{JC} from Table 11, the junction temperature T_J can be calculated by using the following formula from Figure 14.

$T_J = T_C + (P \cdot \theta_{JC})$

Table 13 shows T_J values for the various versions of the Am186ED microcontroller. The column titled *Speed/Pkg/Board* in Table 13 indicates the clock speed in MHz, the type of package (P for PQFP and T for TQFP), and the type of board (2 for 2-layer and 4-6 for 4-layer to 6-layer).

Table 13. Junction Temperature Calculation

Speed/ Pkg/ Board	T_J(°C)	$T_J = T_C + (P \cdot \theta_{JC})$		
		T_C	P	θ_{JC}
40/P2	108.3	100	1.2	7
40/T2	111.8	100	1.2	10
40/P4-6	105.9	100	1.2	5
40/T4-6	107.1	100	1.2	6
33/P2	106.8	100	1.0	7
33/T2	109.7	100	1.0	10
33/P4-6	104.9	100	1.0	5
33/T4-6	105.8	100	1.0	6
25/P2	105.2	100	0.7	7
25/T2	107.4	100	0.7	10
25/P4-6	103.7	100	0.7	5
25/T4-6	104.4	100	0.7	6
20/P2	104.1	100	0.6	7
20/T2	105.9	100	0.6	10
20/P4-6	103.0	100	0.6	5
20/T4-6	103.5	100	0.6	6

By using T_J from Table 13, the typical power consumption value from Table 12, and a θ_{JA} value from Table 11, the typical ambient temperature T_A can be calculated using the following formula from Figure 14:

$T_A = T_J – (P \cdot \theta_{JA})$

For example, T_A for a 40-MHz PQFP design with a 2-layer board and 0 fpm airflow is calculated as follows:

$T_A = 108.3 – (1.2 \cdot 45)$
$T_A = 55.2$

In this calculation, T_J comes from Table 13, P comes from Table 12, and θ_{JA} comes from Table 11. See Table 14.

T_A for a 33-MHz TQFP design with a 4-layer to 6-layer board and 200 fpm airflow is calculated as follows:

$T_A = 105.8 – (1.0 \cdot 28)$
$T_A = 78.6$

See Table 17 for the result of this calculation.

Table 14 through Table 17 and Figure 15 through Figure 18 show T_A based on the preceding assumptions and calculations for a range of θ_{JA} values with airflow from 0 linear feet per minute to 600 linear feet per minute.

Table 14 shows typical maximum ambient temperatures in degrees Centigrade for a PQFP package used on a 2-layer board. The typical ambient temperatures are based on a 100-degree Centigrade maximum case temperature. Figure 15 graphically illustrates the typical temperatures in Table 14.

Table 14. Typical Ambient Temperatures (°C) for PQFP with a 2-Layer Board

Microcontroller Speed	Typical Power (Watts)	Linear Feet per Minute Airflow			
		0 fpm	200 fpm	400 fpm	600 fpm
40 MHz	1.2	55.2	62.2	67.0	69.3
33 MHz	1.0	63.0	68.8	72.7	74.7
25 MHz	0.7	72.0	76.4	79.4	80.8
20 MHz	0.6	77.6	81.1	83.5	84.7

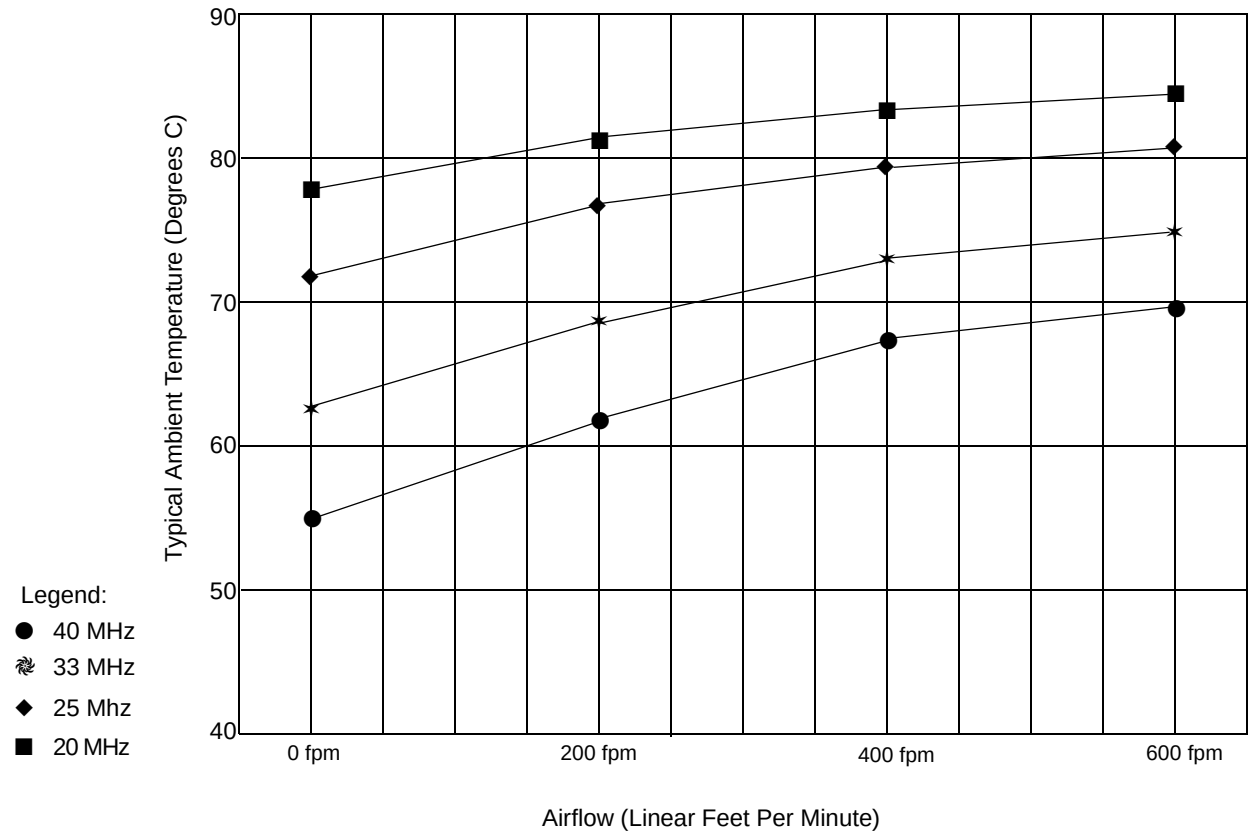


Figure 15. Typical Ambient Temperatures for PQFP with a 2-Layer Board

Table 15 shows typical maximum ambient temperatures in degrees Centigrade for a TQFP package used on a 2-layer board. The typical ambient temperatures are based on a 100-degree Centigrade maximum case temperature. Figure 16 graphically illustrates the typical temperatures in Table 15.

Table 15. Typical Ambient Temperatures (°C) for TQFP with a 2-Layer Board

Microcontroller Speed	Typical Power (Watts)	Linear Feet per Minute Airflow			
		0 fpm	200 fpm	400 fpm	600 fpm
40 MHz	1.2	45.7	57.5	64.6	67.0
33 MHz	1.0	55.2	65.0	70.8	72.7
25 MHz	0.7	66.1	73.5	77.9	79.4
20 MHz	0.6	72.9	78.8	82.3	83.5

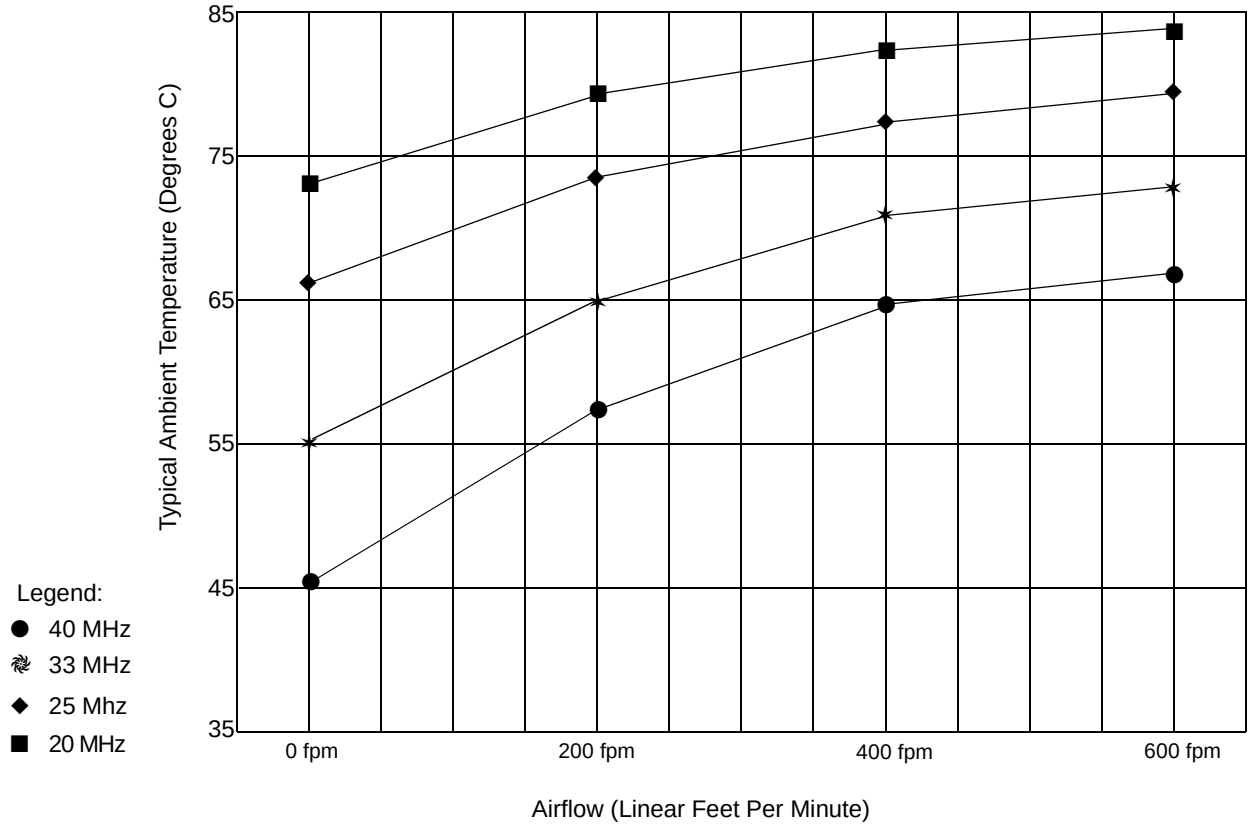


Figure 16. Typical Ambient Temperatures for TQFP with a 2-Layer Board

Table 16 shows typical maximum ambient temperatures in degrees Centigrade for a PQFP package used on a 4-layer to 6-layer board. The typical ambient temperatures are based on a 100-degree Centigrade maximum case temperature. Figure 17 graphically illustrates the typical temperatures in Table 16.

Table 16. Typical Ambient Temperatures (°C) for PQFP with a 4-Layer to 6-Layer Board

Microcontroller Speed	Typical Power (Watts)	Linear Feet per Minute Airflow			
		0 fpm	200 fpm	400 fpm	600 fpm
40 MHz	1.2	78.8	81.1	83.5	85.8
33 MHz	1.0	82.5	84.4	86.4	88.3
25 MHz	0.7	86.7	88.2	89.7	91.2
20 MHz	0.6	89.4	90.6	91.7	92.9

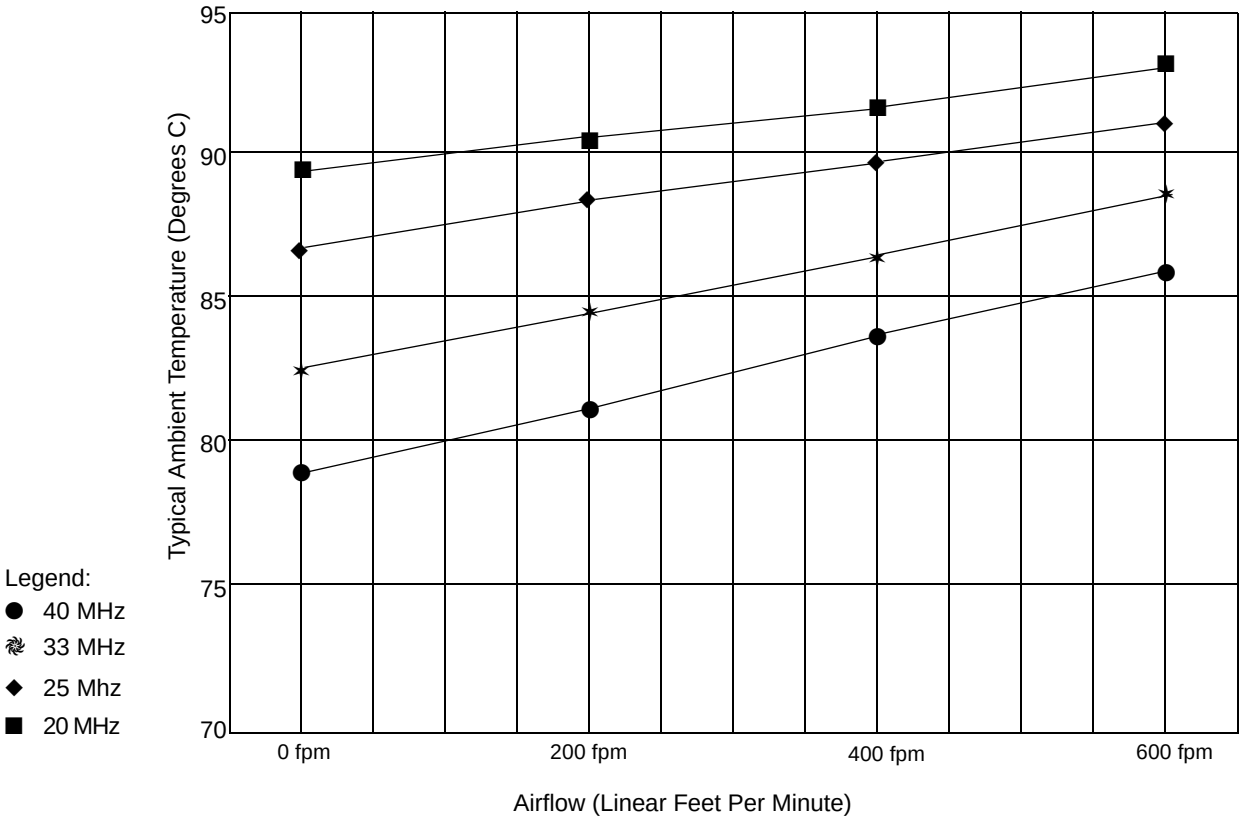


Figure 17. Typical Ambient Temperatures for PQFP with a 4-Layer to 6-Layer Board

Table 17 shows typical maximum ambient temperatures in degrees Centigrade for a TQFP package used on a 4-layer to 6-layer board. The typical ambient temperatures are based on a 100-degree Centigrade maximum case temperature. Figure 18 graphically illustrates the typical temperatures in Table 17.

Table 17. Typical Ambient Temperatures (°C) for TQFP with a 4-Layer to 6-Layer Board

Microcontroller Speed	Typical Power (Watts)	Linear Feet per Minute Airflow			
		0 fpm	200 fpm	400 fpm	600 fpm
40 MHz	1.2	71.7	74.0	76.4	78.8
33 MHz	1.0	76.6	78.6	80.5	82.5
25 MHz	0.7	82.3	83.8	85.3	86.7
20 MHz	0.6	85.8	87.0	88.2	89.4

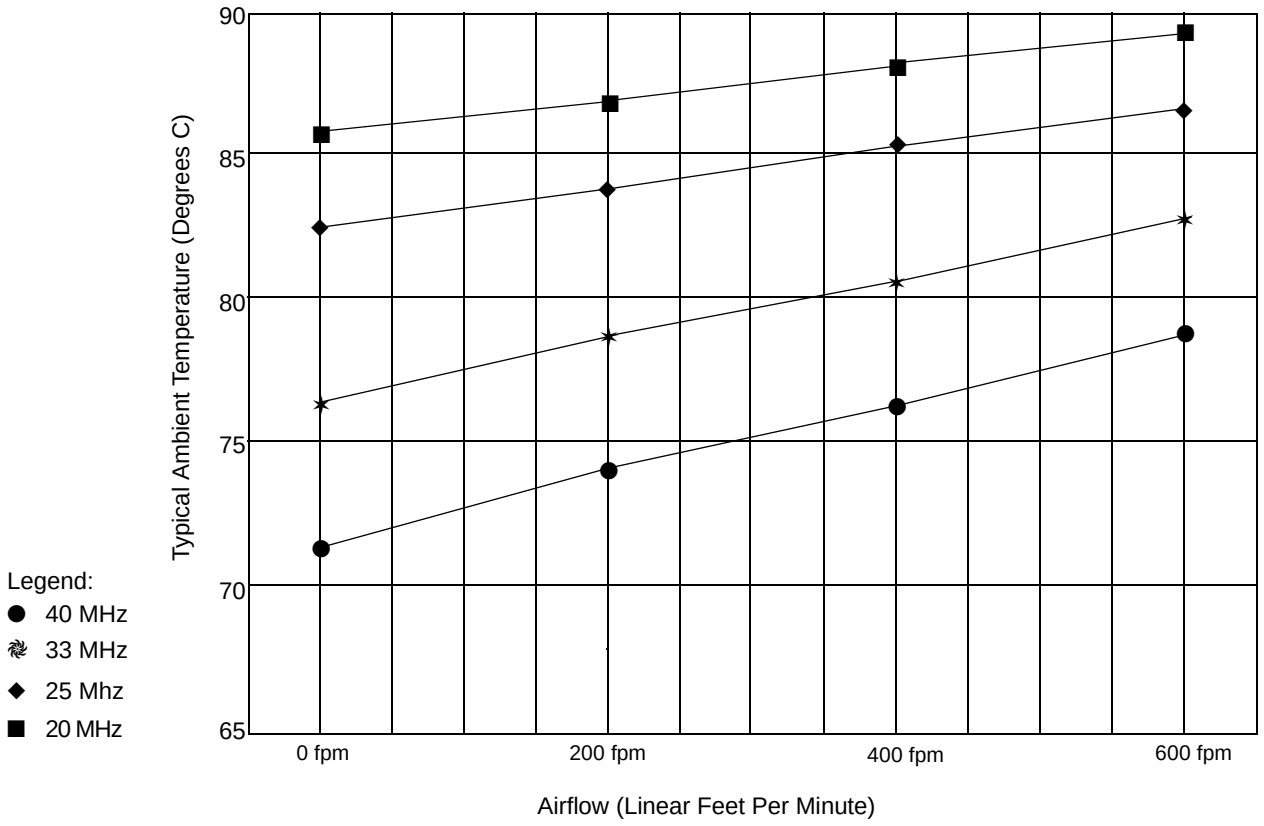


Figure 18. Typical Ambient Temperatures for TQFP with a 4-Layer to 6-Layer Board

COMMERCIAL AND INDUSTRIAL SWITCHING CHARACTERISTICS AND WAVEFORMS

In the switching waveforms that follow, several abbreviations are used to indicate the specific periods of a bus cycle. These periods are referred to as time states. A typical bus cycle is composed of four consecutive time states: t_1, t_2, t_3, and t_4. Wait states, which represent multiple t_3 states, are referred to as t_w states. When no bus cycle is pending, an idle (t_i) state occurs.

In the switching parameter descriptions, the *multiplexed* address is referred to as the AD address bus; the *demultiplexed* address is referred to as the A address bus.

Key to Switching Waveforms

WAVEFORM	INPUT	OUTPUT
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance *Off* State
	Invalid	Invalid

Alphabetical Key to Switching Parameter Symbols

Parameter Symbol	No.	Description
t_{ARYCH}	49	ARDY Resolution Transition Setup Time
t_{ARYCHL}	51	ARDY Inactive Holding Time
$t_{ARYHDSH}$[(a)]	95	ARDY High to $\overline{DS}$ High
t_{ARYHDV}[(a)]	89	ARDY Assert to Data Valid
t_{ARYLCL}	52	ARDY Setup Time
$t_{ARYLDSH}$[(a)]	96	ARDY Low to $\overline{DS}$ High
t_{AVBL}	87	A Address Valid to $\overline{WHB}$, $\overline{WLB}$ Low
t_{AVCH}	14	AD Address Valid to Clock High
t_{AVLL}	12	AD Address Valid to ALE Low
t_{AVRL}	66	A Address Valid to $\overline{RD}$ Low
t_{AVWL}	65	A Address Valid to $\overline{WR}$ Low
t_{AZRL}	24	AD Address Float to $\overline{RD}$ Active
t_{CH1CH2}	45	CLKOUTA Rise Time
t_{CHAV}	68	CLKOUTA High to A Address Valid
t_{CHCA}	104	CLKOUTA High to $\overline{CAS}$ Active
t_{CHCAV}	101	CLKOUTA Low to Column Address Valid
t_{CHCK}	38	X1 High Time
t_{CHCL}	44	CLKOUTA High Time
t_{CHCSV}	67	CLKOUTA High to $\overline{LCS}$/$\overline{UCS}$ Valid
t_{CHCSX}	18	$\overline{MCS}$/$\overline{PCS}$ Inactive Delay
t_{CHCTV}	22	Control Active Delay 2
t_{CHCV}	64	Command Lines Valid Delay (after Float)
t_{CHCZ}	63	Command Lines Float Delay
t_{CHDX}	8	Status Hold Time
t_{CHLH}	9	ALE Active Delay
t_{CHLL}	11	ALE Inactive Delay
t_{CHRA}	106	CLKOUTA High to $\overline{RAS}$ Active
t_{CHSV}	3	Status Active Delay
t_{CICOA}	69	X1 to CLKOUTA Skew
t_{CICOB}	70	X1 to CLKOUTB Skew
t_{CHRX}	103	CLKOUTA High to $\overline{RAS}$ Inactive
t_{CKHL}	39	X1 Fall Time
t_{CKIN}	36	X1 Period
t_{CKLH}	40	X1 Rise Time
t_{CL2CL1}	46	CLKOUTA Fall Time
t_{CLARX}	50	ARDY Active Hold Time
t_{CLAV}	5	AD Address Valid Delay and BHE
t_{CLAX}	6	Address Hold
t_{CLAZ}	15	AD Address Float Delay
t_{CLCH}	43	CLKOUTA Low Time
t_{CLCK}	37	X1 Low Time
t_{CLCL}	42	CLKOUTA Period

Alphabetical Key to Switching Parameter Symbols (continued)

Parameter Symbol	No.	Description
t_{CLCSV}	16	$\overline{MCS}$/$\overline{PCS}$ Active Delay
t_{CLCX}	105	CLKOUTA Low to $\overline{CAS}$ Inactive
t_{CLRX}	107	CLKOUTA Low to $\overline{RAS}$ Inactive
t_{CLDOX}	30	Data Hold Time
t_{CLDV}	7	Data Valid Delay
t_{CLDX}	2	Data in Hold
t_{CLHAV}	62	HLDA Valid Delay
t_{CLRA}	102	CLKOUTA Low to $\overline{RAS}$ Active
t_{CLRH}	27	$\overline{RD}$ Inactive Delay
t_{CLRL}	25	$\overline{RD}$ Active Delay
t_{CLSH}	4	Status Inactive Delay
t_{CLSRY}	48	SRDY Transition Hold Time
t_{CLTMV}	55	Timer Output Delay
t_{COAOB}[(a)]	83	CLKOUTA to CLKOUTB Skew
$t_{CSHARYL}$[(a)]	88	Chip Select to ARDY Low
t_{CVCTV}	20	Control Active Delay 1
t_{CVCTX}	31	Control Inactive Delay
t_{CVDEX}	21	$\overline{DEN}$ Inactive Delay
t_{CXCSX}	17	$\overline{MCS}$/$\overline{PCS}$ Hold from Command Inactive
t_{DSHDIR}[(a)]	92	$\overline{DS}$ High to Data Invalid—Read
t_{DSHDIW}	98	$\overline{DS}$ High to Data Invalid—Write
t_{DSHDX}[(a)]	93	$\overline{DS}$ High to Data Bus Turn-off Time
t_{DSHLH}	41	$\overline{DS}$ Inactive to ALE Inactive
t_{DSLDD}[(a)]	90	$\overline{DS}$ Low to Data Driven
t_{DSLDV}[(a)]	91	$\overline{DS}$ Low to Data Valid
t_{DVCL}	1	Data in Setup
t_{DVDSL}[(a)]	97	Data Valid to $\overline{DS}$ Low
t_{DXDL}	19	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low
t_{HVCL}	58	HOLD Setup
t_{INVCH}	53	Peripheral Setup Time
t_{INVCL}	54	DRQ Setup Time
t_{LHAV}	23	ALE High to Address Valid
t_{LHLL}	10	ALE Width
t_{LLAX}	13	AD Address Hold from ALE Inactive
t_{LOCK}	61	Maximum PLL Lock Time
t_{PLAL}	99	$\overline{PCS}$ Active to ALE Inactive
t_{RD0W}	110	$\overline{RAS}$ To Column Address Delay Time with 0 Wait States
t_{RD1W}	111	$\overline{RAS}$ to Column Address Delay Time with 1 or More Wait States
t_{RESIN}	57	$\overline{RES}$ Setup Time
t_{RHAV}	29	$\overline{RD}$ Inactive to AD Address Active
t_{RHDX}	59	$\overline{RD}$ High to Data Hold on AD Bus
t_{RHDZ}[(a)]	94	$\overline{RD}$ High to Data Bus Turn-off Time
t_{RHLH}	28	$\overline{RD}$ Inactive to ALE High

Alphabetical Key to Switching Parameter Symbols (continued)

Parameter Symbol	No.	Description
t_{RLRH}	26	$\overline{RD}$ Pulse Width
t_{RP0W}	108	$\overline{RAS}$ Inactive Pulse Width (0 Wait States)
t_{RP1W}	109	$\overline{RAS}$ Inactive Pulse Width (1 Wait State)
t_{SRYCL}	47	SRDY Transition Setup Time
t_{WHDEX}	35	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive
t_{WHDX}	34	Data Hold after $\overline{WR}$
t_{WHLH}	33	$\overline{WR}$ Inactive to ALE High
t_{WLWH}	32	$\overline{WR}$ Pulse Width

Note:

a Specs 83 and 88–97 are defined but not used at this time. Additionally, the following parameters are not defined nor used at this time: 56, 60, and 71–78.

Numerical Key to Switching Parameter Symbols

No.	Parameter Symbol	Description
1	t_{DVCL}	Data in Setup
2	t_{CLDX}	Data in Hold
3	t_{CHSV}	Status Active Delay
4	t_{CLSH}	Status Inactive Delay
5	t_{CLAV}	AD Address Valid Delay and BHE
6	t_{CLAX}	Address Hold
7	t_{CLDV}	Data Valid Delay
8	t_{CHDX}	Status Hold Time
9	t_{CHLH}	ALE Active Delay
10	t_{LHLL}	ALE Width
11	t_{CHLL}	ALE Inactive Delay
12	t_{AVLL}	AD Address Valid to ALE Low
13	t_{LLAX}	AD Address Hold from ALE Inactive
14	t_{AVCH}	AD Address Valid to Clock High
15	t_{CLAZ}	AD Address Float Delay
16	t_{CLCSV}	$\overline{MCS}$/$\overline{PCS}$ Active Delay
17	t_{CXCSX}	$\overline{MCS}$/$\overline{PCS}$ Hold from Command Inactive
18	t_{CHCSX}	$\overline{MCS}$/$\overline{PCS}$ Inactive Delay
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low
20	t_{CVCTV}	Control Active Delay 1
21	t_{CVDEX}	$\overline{DEN}$ Inactive Delay
22	t_{CHCTV}	Control Active Delay 2
23	t_{LHAV}	ALE High to Address Valid
24	t_{AZRL}	AD Address Float to $\overline{RD}$ Active
25	t_{CLRL}	$\overline{RD}$ Active Delay
26	t_{RLRH}	$\overline{RD}$ Pulse Width
27	t_{CLRH}	$\overline{RD}$ Inactive Delay
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High
29	t_{RHAV}	$\overline{RD}$ Inactive to AD Address Active
30	t_{CLDOX}	Data Hold Time
31	t_{CVCTX}	Control Inactive Delay
32	t_{WLWH}	$\overline{WR}$ Pulse Width
33	t_{WHLH}	$\overline{WR}$ Inactive to ALE High
34	t_{WHDX}	Data Hold after $\overline{WR}$
35	t_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive
36	t_{CKIN}	X1 Period
37	t_{CLCK}	X1 Low Time
38	t_{CHCK}	X1 High Time
39	t_{CKHL}	X1 Fall Time
40	t_{CKLH}	X1 Rise Time
41	t_{DSHLH}	$\overline{DS}$ Inactive to ALE Inactive
42	t_{CLCL}	CLKOUTA Period

Numerical Key to Switching Parameter Symbols (continued)

No.	Parameter Symbol	Description
43	t_{CLCH}	CLKOUTA Low Time
44	t_{CHCL}	CLKOUTA High Time
45	t_{CH1CH2}	CLKOUTA Rise Time
46	t_{CL2CL1}	CLKOUTA Fall Time
47	t_{SRYCL}	SRDY Transition Setup Time
48	t_{CLSRY}	SRDY Transition Hold Time
49	t_{ARYCH}	ARDY Resolution Transition Setup Time
50	t_{CLARX}	ARDY Active Hold Time
51	t_{ARYCHL}	ARDY Inactive Holding Time
52	t_{ARYLCL}	ARDY Setup Time
53	t_{INVCH}	Peripheral Setup Time
54	t_{INVCL}	DRQ Setup Time
55	t_{CLTMV}	Timer Output Delay
57	t_{RESIN}	$\overline{RES}$ Setup Time
58	t_{HVCL}	HOLD Setup
59	t_{RHDX}	$\overline{RD}$ High to Data Hold on AD Bus
61	t_{LOCK}	Maximum PLL Lock Time
62	t_{CLHAV}	HLDA Valid Delay
63	t_{CHCZ}	Command Lines Float Delay
64	t_{CHCV}	Command Lines Valid Delay (after Float)
65	t_{AVWL}	A Address Valid to $\overline{WR}$ Low
66	t_{AVRL}	A Address Valid to $\overline{RD}$ Low
67	t_{CHCSV}	CLKOUTA High to $\overline{LCS}$/$\overline{UCS}$ Valid
68	t_{CHAV}	CLKOUTA High to A Address Valid
69	t_{CICOA}	X1 to CLKOUTA Skew
70	t_{CICOB}	X1 to CLKOUTB Skew
83[a]	t_{COAOB}	CLKOUTA to CLKOUTB Skew
87	t_{AVBL}	A Address Valid to $\overline{WHB}$, $\overline{WLB}$ Low
88[a]	$t_{CSHARYL}$	Chip Select to ARDY Low
89[a]	t_{ARYHDV}	ARDY Assert to Data Valid
90[a]	t_{DSLDD}	$\overline{DS}$ Low to Data Driven
91[a]	t_{DSLDV}	$\overline{DS}$ Low to Data Valid
92[a]	t_{DSHDIR}	$\overline{DS}$ High to Data Invalid—Read
93[a]	t_{DSHDX}	$\overline{DS}$ High to Data Bus Turn-off Time

Numerical Key to Switching Parameter Symbols (continued)

No.	Parameter Symbol	Description
94[a]	t_{RHDZ}	$\overline{RD}$ High to Data Bus Turn-off Time
95[a]	$t_{ARYHDSH}$	ARDY High to $\overline{DS}$ High
96[a]	$t_{ARYLDSH}$	ARDY Low to $\overline{DS}$ High
97[a]	t_{DVDSL}	Data Valid to $\overline{DS}$ Low
98	t_{DSHDIW}	$\overline{DS}$ High to Data Invalid—Write
99	t_{PLAL}	$\overline{PCS}$ Active to ALE Inactive
101	t_{CHCAV}	CLKOUTA Low to Column Address Valid
102	t_{CLRA}	CLKOUTA Low to $\overline{RAS}$ Active
103	t_{CHRX}	CLKOUTA High to $\overline{RAS}$ Inactive
104	t_{CHCA}	CLKOUTA High to $\overline{CAS}$ Active
105	t_{CLCX}	CLKOUTA Low to $\overline{CAS}$ Inactive
106	t_{CHRA}	CLKOUTA High to $\overline{RAS}$ Active
107	t_{CLRX}	CLKOUTA Low to $\overline{RAS}$ Inactive
108	t_{RP0W}	$\overline{RAS}$ Inactive Pulse Width (0 Wait States)
109	t_{RP1W}	$\overline{RAS}$ Inactive Pulse Width (1 Wait State)
110	t_{RD0W}	$\overline{RAS}$ To Column Address Delay Time with 0 Wait States
111	t_{RD1W}	$\overline{RAS}$ to Column Address Delay Time with 1 or More Wait States

Note:

a Specs 83 and 88–97 are defined but not used at this time. Additionally, the following parameters are not defined nor used at this time: 56, 60, and 71–78.

SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges

Read Cycle (20 MHz and 25 MHz)

Parameter			Preliminary				Unit
			20 MHz		25 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Requirements							
1	t_{DVCL}	Data in Setup	10		10		ns
2	t_{CLDX}	Data in Hold[c]	3		3		ns
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	25	0	20	ns
4	t_{CLSH}	Status Inactive Delay	0	25	0	20	ns
5	t_{CLAV}	AD Address Valid Delay and BHE	0	25	0	20	ns
6	t_{CLAX}	Address Hold	0	25	0	20	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		25		20	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=40$		$t_{CLCL}-10=30$		ns
11	t_{CHLL}	ALE Inactive Delay		25		20	ns
12	t_{AVLL}	AD Address Valid to ALE Low[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
13	t_{LLAX}	AD Address Hold from ALE Inactive[a]	$t_{CHCL}-2$		$t_{CHCL}-2$		ns
14	t_{AVCH}	AD Address Valid to Clock High	0		0		ns
15	t_{CLAZ}	AD Address Float Delay	$t_{CLAX}=0$	25	$t_{CLAX}=0$	20	ns
16	t_{CLCSV}	$\overline{MCS}/\overline{PCS}$ Active Delay	0	25	0	20	ns
17	t_{CXCSX}	$\overline{MCS}/\overline{PCS}$ Hold from Command Inactive[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
18	t_{CHCSX}	$\overline{MCS}/\overline{PCS}$ Inactive Delay	0	25	0	20	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
20	t_{CVCTV}	Control Active Delay 1[b]	0	25	0	20	ns
21	t_{CVDEX}	$\overline{DEN}$ Inactive Delay	0	25	0	20	ns
22	t_{CHCTV}	Control Active Delay 2[b]	0	25	0	20	ns
23	t_{LHAV}	ALE High to Address Valid	20		15		ns
99	t_{PLAL}	$\overline{PCS}$ Active to ALE Inactive	15	28	15	24	ns
Read Cycle Timing Responses							
24	t_{AZRL}	AD Address Float to $\overline{RD}$ Active	0		0		ns
25	t_{CLRL}	$\overline{RD}$ Active Delay	0	25	0	20	ns
26	t_{RLRH}	$\overline{RD}$ Pulse Width	$2t_{CLCL}-15=85$		$2t_{CLCL}-15=65$		ns
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	0	25	0	20	ns
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High[a]	$t_{CLCH}-3$		$t_{CLCH}-3$		ns
29	t_{RHAV}	$\overline{RD}$ Inactive to AD Address Active[a]	$t_{CLCL}-10=40$		$t_{CLCL}-10=30$		ns
41	t_{DSHLH}	$\overline{DS}$ Inactive to ALE Active	$t_{CLCH}-2=21$		$t_{CLCH}-2=16$		ns
59	t_{RHDX}	$\overline{RD}$ High to Data Hold on AD Bus[c]	0		0		ns
66	t_{AVRL}	A Address Valid to $\overline{RD}$ Low[a]	$t_{CLCL}+t_{CHCL}-3$		$t_{CLCL}+t_{CHCL}-3$		ns
67	t_{CHCSV}	CLKOUTA High to $\overline{LCS}/\overline{UCS}$ Valid	0	25	0	20	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	25	0	20	ns

Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L =50 pF. For switching tests, V_{IL} =0.45 V and V_{IH} =2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.

a Equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$, $\overline{DS}$, $\overline{INTA1}$–$\overline{INTA0}$, $\overline{WR}$, $\overline{WHB}$, and $\overline{WLB}$ signals.

c If either spec 2 or spec 59 is met with respect to data hold time, the part will function correctly.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

Read Cycle (33 MHz and 40 MHz)

Parameter			Preliminary				Unit
			33 MHz		40 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Requirements							
1	t_{DVCL}	Data in Setup	8		5		ns
2	t_{CLDX}	Data in Hold[c]	3		2		ns
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	15	0	12	ns
4	t_{CLSH}	Status Inactive Delay	0	15	0	12	ns
5	t_{CLAV}	AD Address Valid Delay and BHE	0	15	0	12	ns
6	t_{CLAX}	Address Hold	0	15	0	12	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		15		12	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=20$		$t_{CLCL}-5=20$		ns
11	t_{CHLL}	ALE Inactive Delay		15		12	ns
12	t_{AVLL}	AD Address Valid to ALE Low[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
13	t_{LLAX}	AD Address Hold from ALE Inactive[a]	$t_{CHCL}-2$		$t_{CHCL}-2$		ns
14	t_{AVCH}	AD Address Valid to Clock High	0		0		ns
15	t_{CLAZ}	AD Address Float Delay	$t_{CLAX}=0$	15	$t_{CLAX}=0$	12	ns
16	t_{CLCSV}	$\overline{MCS}/\overline{PCS}$ Active Delay	0	15	0	12	ns
17	t_{CXCSX}	$\overline{MCS}/\overline{PCS}$ Hold from Command Inactive[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
18	t_{CHCSX}	$\overline{MCS}/\overline{PCS}$ Inactive Delay	0	15	0	12	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
20	t_{CVCTV}	Control Active Delay 1[b]	0	15	0	12	ns
21	t_{CVDEX}	$\overline{DEN}$ Inactive Delay	0	15	0	12	ns
22	t_{CHCTV}	Control Active Delay 2[b]	0	15	0	12	ns
23	t_{LHAV}	ALE High to Address Valid	10		7.5		ns
99	t_{PLAL}	$\overline{PCS}$ Active to ALE Inactive	12	20	10	18	ns
Read Cycle Timing Responses							
24	t_{AZRL}	AD Address Float to $\overline{RD}$ Active	0		0		ns
25	t_{CLRL}	$\overline{RD}$ Active Delay	0	15	0	10	ns
26	t_{RLRH}	$\overline{RD}$ Pulse Width	$2t_{CLCL}-15=45$		$2t_{CLCL}-10=40$		ns
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	0	15	0	12	ns
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High[a]	$t_{CLCH}-3$		$t_{CLCH}-2$		ns
29	t_{RHAV}	$\overline{RD}$ Inactive to AD Address Active[a]	$t_{CLCL}-10=20$		$t_{CLCL}-5=20$		ns
41	t_{DSHLH}	$\overline{DS}$ Inactive to ALE Active	$t_{CLCH}-2=11.5$		$t_{CLCH}-2=9.25$		
59	t_{RHDX}	$\overline{RD}$ High to Data Hold on AD Bus[c]	0		0		ns
66	t_{AVRL}	A Address Valid to $\overline{RD}$ Low[a]	$t_{CLCL}+t_{CHCL}-3$		$t_{CLCL}+t_{CHCL}-1.25$		ns
67	t_{CHCSV}	CLKOUTA High to $\overline{LCS}/\overline{UCS}$ Valid	0	15	0	10	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	15	0	10	ns

Notes:

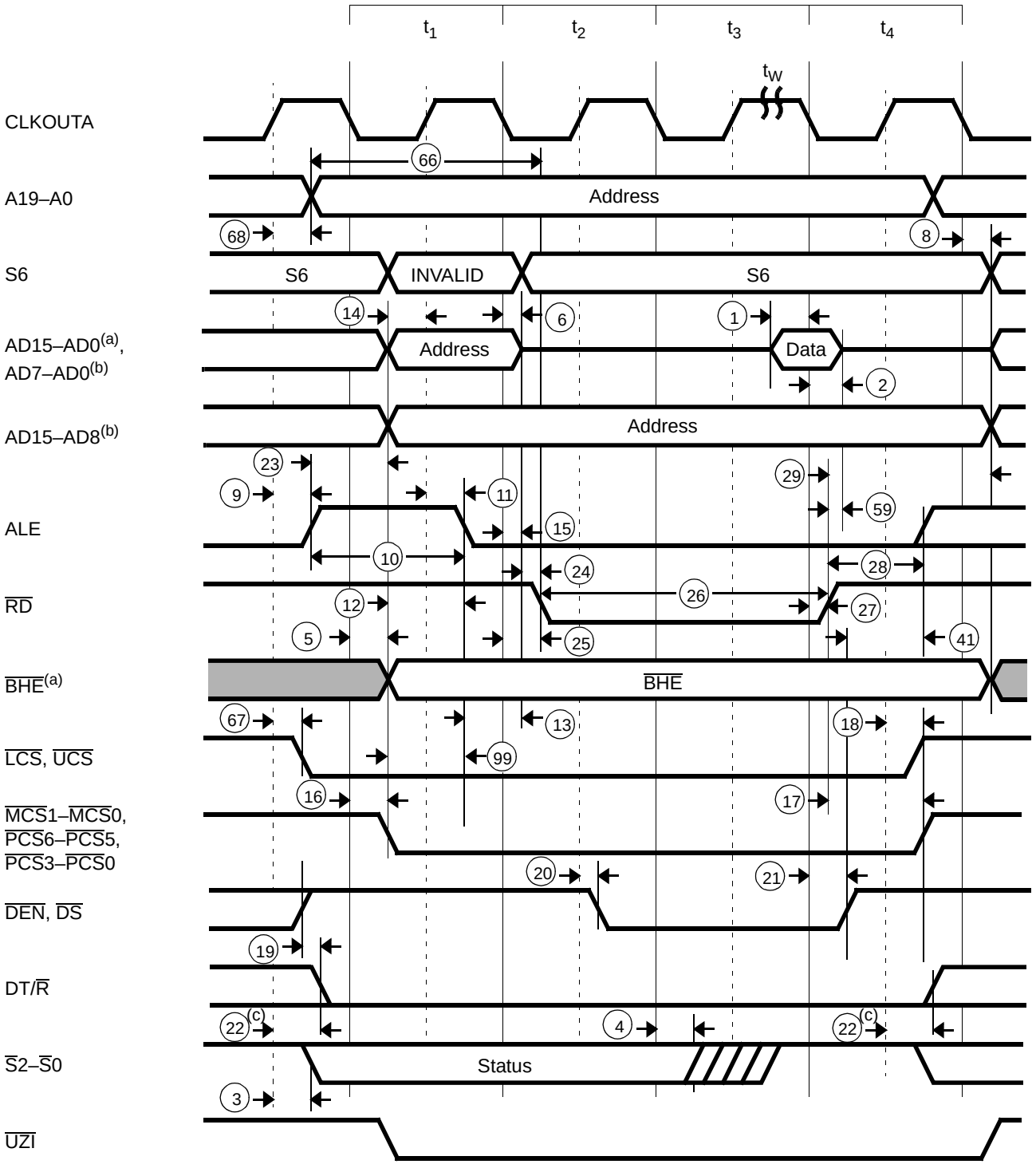
All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L =50 pF. For switching tests, V_{IL}=0.45 V and V_{IH} =2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.

a Equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$, $\overline{DS}$, $\overline{INTA1}$–$\overline{INTA0}$, $\overline{WR}$, $\overline{WHB}$, and $\overline{WLB}$ signals.

c If either spec 2 or spec 59 is met with respect to data hold time, the part will function correctly.

READ CYCLE WAVEFORMS



Notes:

a Am186ED/EDLV microcontrollers in 16-bit mode

b Am186ED/EDLV microcontrollers in 8-bit mode

c Changes in t phase preceding next bus cycle if followed by read, INTA, or halt.

SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges

Write Cycle (20 MHz and 25 MHz)

Parameter			Preliminary				Unit
			20 MHz		25 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	25	0	20	ns
4	t_{CLSH}	Status Inactive Delay	0	25	0	20	ns
5	t_{CLAV}	AD Address Valid Delay and BHE	0	25	0	20	ns
6	t_{CLAX}	Address Hold	0	25	0	20	ns
7	t_{CLDV}	Data Valid Delay	0	15	0	15	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		25		20	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=40$		$t_{CLCL}-10=30$		ns
11	t_{CHLL}	ALE Inactive Delay		25		20	ns
12	t_{AVLL}	AD Address Valid to ALE Low[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
13	t_{LLAX}	AD Address Hold from ALE Inactive[a]	$t_{CHCL}-2$		$t_{CHCL}-2$		ns
14	t_{AVCH}	AD Address Valid to Clock High	0		0		ns
16	t_{CLCSV}	$\overline{MCS}/\overline{PCS}$ Active Delay	0	25	0	20	ns
17	t_{CXCSX}	$\overline{MCS}/\overline{PCS}$ Hold from Command Inactive[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
18	t_{CHCSX}	$\overline{MCS}/\overline{PCS}$ Inactive Delay	0	25	0	20	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
20	t_{CVCTV}	Control Active Delay 1[b]	0	15	0	15	ns
21	t_{CVDEX}	$\overline{DS}$ Inactive Delay	0	25	0	20	ns
22	t_{CHCTV}	Control Active Delay 2	0	25	0	20	ns
23	t_{LHAV}	ALE High to Address Valid	20		15		ns
99	t_{PLAL}	$\overline{PCS}$ Active to ALE Inactive	15	28	15	24	ns
Write Cycle Timing Responses							
30	t_{CLDOX}	Data Hold Time	0		0		ns
31	t_{CVCTX}	Control Inactive Delay[b]	0	25	0	20	ns
32	t_{WLWH}	$\overline{WR}$ Pulse Width	$2t_{CLCL}-10=90$		$2t_{CLCL}-10=70$		ns
33	t_{WHLH}	$\overline{WR}$ Inactive to ALE High[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
34	t_{WHDX}	Data Hold after $\overline{WR}$[a]	$t_{CLCL}-10=40$		$t_{CLCL}-10=30$		ns
35	t_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive[a]	$t_{CLCH}-3$		$t_{CLCH}-3$		ns
41	t_{DSHLH}	$\overline{DS}$ Inactive to ALE Active	$t_{CLCH}-2=21$		$t_{CLCH}-2=16$		ns
65	t_{AVWL}	A Address Valid to $\overline{WR}$ Low	$t_{CLCL}+t_{CHCL}-3$		$t_{CLCL}+t_{CHCL}-3$		ns
67	t_{CHCSV}	CLKOUTA High to $\overline{LCS}/\overline{UCS}$ Valid	0	25	0	20	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	25	0	20	ns
87	t_{AVBL}	A Address Valid to $\overline{WHB}$, $\overline{WLB}$ Low	$t_{CHCL}-3$	25	$t_{CHCL}-3$	20	ns
98	t_{DSHDIW}	$\overline{DS}$ High to Data Invalid—Write	35		30		ns

Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L =50 pF. For switching tests, V_{IL}=0.45 V and V_{IH} =2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.

a Testing is performed with equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$, $\overline{DS}$, $\overline{INTA1}$–$\overline{INTA0}$, $\overline{WR}$, $\overline{WHB}$, and $\overline{WLB}$ signals.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

Write Cycle (33 MHz and 40 MHz)

Parameter			Preliminary				Unit
			33 MHz		40 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	15	0	12	ns
4	t_{CLSH}	Status Inactive Delay	0	15	0	12	ns
5	t_{CLAV}	AD Address Valid Delay and BHE	0	15	0	12	ns
6	t_{CLAX}	Address Hold	0		0		ns
7	t_{CLDV}	Data Valid Delay	0	15	0	12	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		15		12	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=20$		$t_{CLCL}-5=20$		ns
11	t_{CHLL}	ALE Inactive Delay		15		12	ns
12	t_{AVLL}	AD Address Valid to ALE Low[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
13	t_{LLAX}	AD Address Hold from ALE Inactive[a]	$t_{CHCL}-2$		$t_{CHCL}-2$		ns
14	t_{AVCH}	AD Address Valid to Clock High	0		0		ns
16	t_{CLCSV}	$\overline{MCS}/\overline{PCS}$ Active Delay	0	15	0	12	ns
17	t_{CXCSX}	$\overline{MCS}/\overline{PCS}$ Hold from Command Inactive[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
18	t_{CHCSX}	$\overline{MCS}/\overline{PCS}$ Inactive Delay	0	15	0	12	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
20	t_{CVCTV}	Control Active Delay 1[b]	0	15	0	12	ns
21	t_{CVDEX}	$\overline{DS}$ Inactive Delay	0	15	0	12	ns
22	t_{CHCTV}	Control Active Delay 2	0	15	0	12	ns
23	t_{LHAV}	ALE High to Address Valid	10		7.5		ns
99	t_{PLAL}	$\overline{PCS}$ Active to ALE Inactive	12	20	10	18	ns
Write Cycle Timing Responses							
30	t_{CLDOX}	Data Hold Time	0		0		ns
31	t_{CVCTX}	Control Inactive Delay[b]	0	15	0	12	ns
32	t_{WLWH}	$\overline{WR}$ Pulse Width	$2t_{CLCL}-10=50$		$2t_{CLCL}-10=40$		ns
33	t_{WHLH}	$\overline{WR}$ Inactive to ALE High[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
34	t_{WHDX}	Data Hold after $\overline{WR}$[a]	$t_{CLCL}-10=20$		$t_{CLCL}-10=15$		ns
35	t_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive[a]	$t_{CLCH}-3$		$t_{CLCH}-3$		ns
41	t_{DSHLH}	$\overline{DS}$ Inactive to ALE Active	$t_{CLCH}-2=11.5$		$t_{CLCH}-2=9.25$		ns
65	t_{AVWL}	A Address Valid to $\overline{WR}$ Low	$t_{CLCL}+t_{CHCL}-3$		$t_{CLCL}+t_{CHCL}-1.25$		ns
67	t_{CHCSV}	CLKOUTA High to $\overline{LCS}/\overline{UCS}$ Valid	0	15	0	10	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	15	0	10	ns
87	t_{AVBL}	A Address Valid to $\overline{WHB}$, $\overline{WLB}$ Low	$t_{CHCL}-3$	15	$t_{CHCL}-1.25$	12	ns
98	t_{DSHDIW}	$\overline{DS}$ High to Data Invalid—Write	20		15		ns

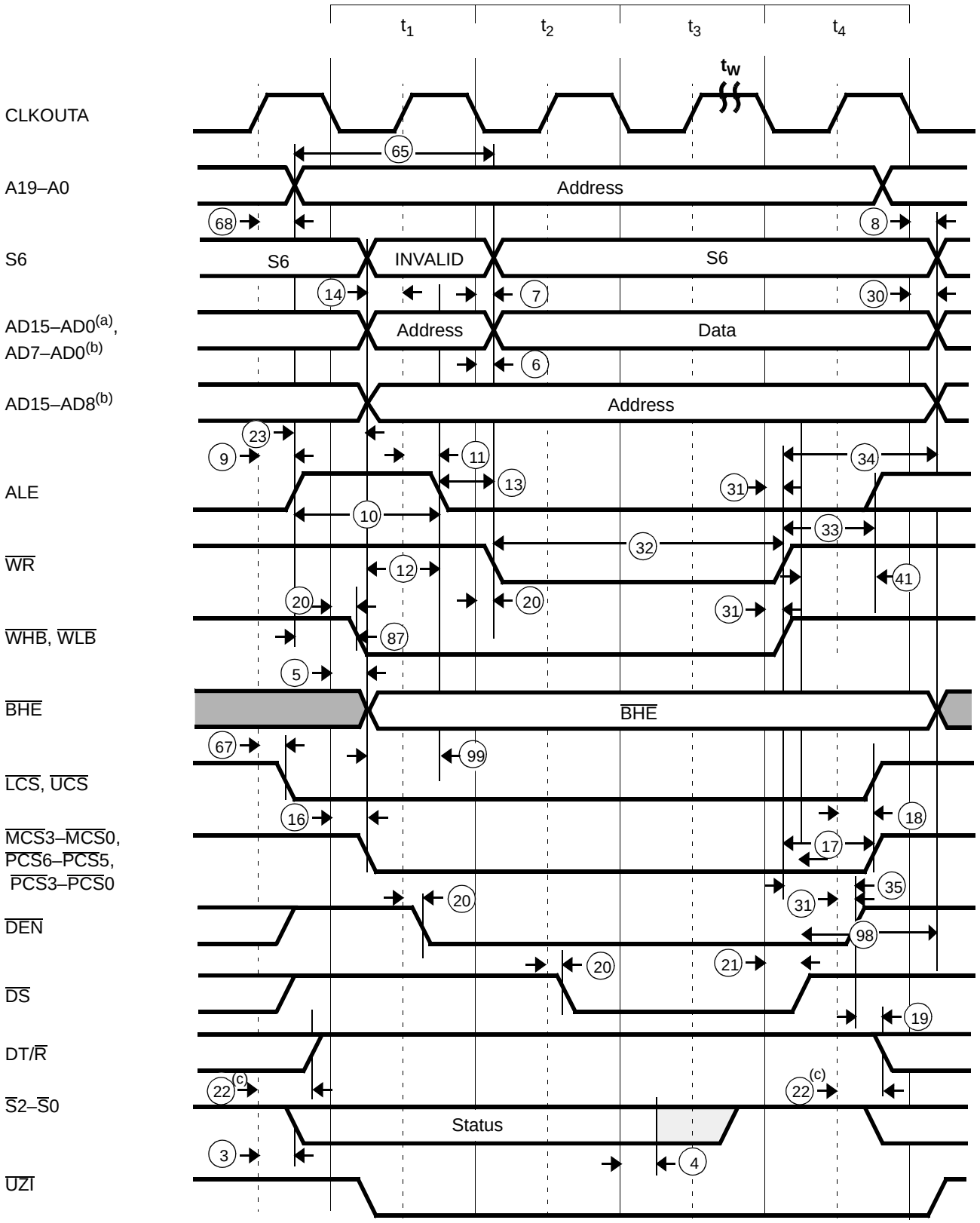
Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L =50 pF. For switching tests, V_{IL}=0.45 V and V_{IH} =2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.

a Testing is performed with equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$, $\overline{DS}$, $\overline{INTA1}$–$\overline{INTA0}$, $\overline{WR}$, $\overline{WHB}$, and $\overline{WLB}$ signals.

WRITE CYCLE WAVEFORMS



Notes:

a Am186ED/EDLV microcontrollers in 16-bit mode

b Am186ED/EDLV microcontrollers in 8-bit mode

c Changes in t phase preceding next bus cycle if followed by read, INTA, or halt

SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges

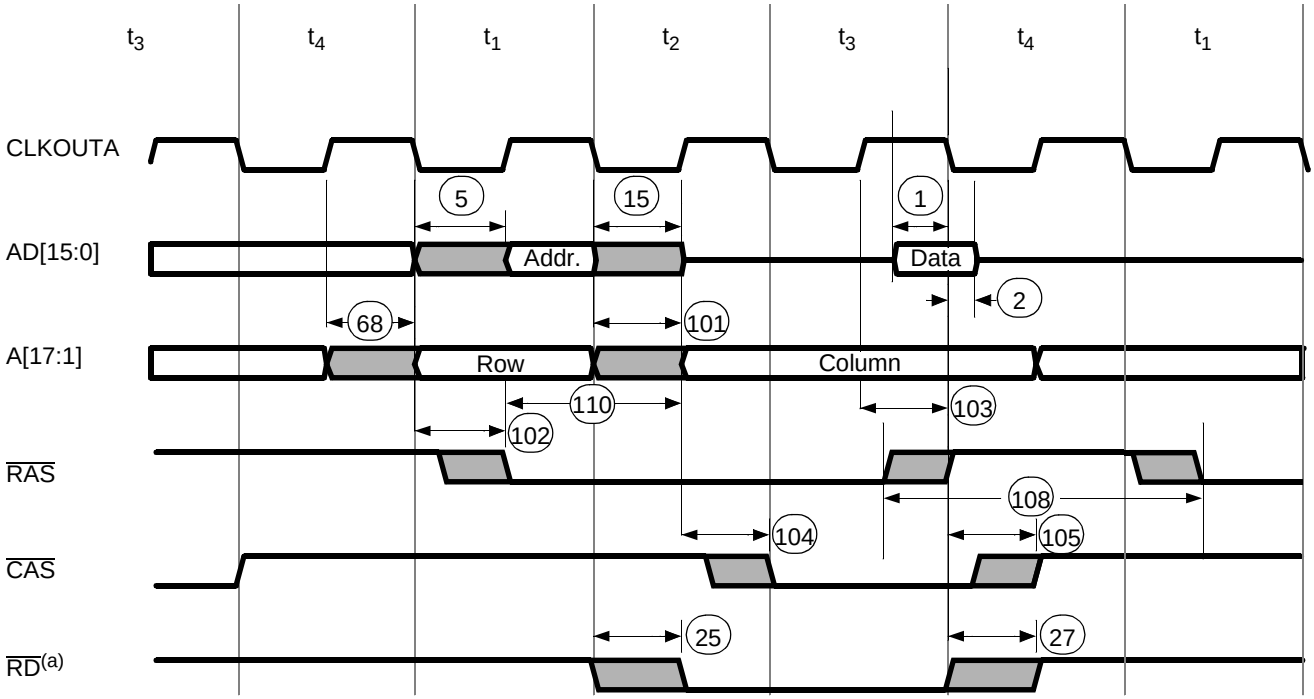
DRAM

Parameter			Preliminary								Unit
			20 MHz		25 MHz		33 MHz		40 MHz		
No.	Symbol	Description	Min	Max	Min	Max	Min	Max	Min	Max	
General Timing Responses											
101	t_{CHCAV}	CLKOUTA Low to Column Address Valid	0	25	0	20	0	15	0	12	ns
102	t_{CLRA}	CLKOUTA Low to $\overline{RAS}$ Active	3	25	3	20	3	15	3	12	ns
103	t_{CHRX}	CLKOUTA High to $\overline{RAS}$ Inactive	3	25	3	20	3	15	3	12	ns
104	t_{CHCA}	CLKOUTA High to $\overline{CAS}$ Active	3	25	3	20	3	15	3	12	ns
105	t_{CLCX}	CLKOUTA Low to $\overline{CAS}$ Inactive	3	25	3	20	3	15	3	12	ns
106	t_{CHRA}	CLKOUTA High to $\overline{RAS}$ Active	3	25	3	20	3	15	3	12	ns
107	t_{CLRX}	CLKOUTA Low to $\overline{RAS}$ Inactive	3	25	3	20	3	15	3	12	ns
108	t_{RP0W}	$\overline{RAS}$ Inactive Pulse Width with 0 Wait States	60	—	50	—	40	—	30	—	ns
109	t_{RP1W}	$\overline{RAS}$ Inactive Pulse Width with 1 or More Wait States	70	—	60	—	50	—	40	—	ns
110	t_{RD0W}	$\overline{RAS}$ To Column Address Delay Time with 0 Wait States	25	—	20	—	15	—	15	—	ns
111	t_{RD1W}	$\overline{RAS}$ to Column Address Delay Time with 1 or More Wait States	30	—	25	—	20	—	15	—	ns

As guaranteed by design, the following table shows the minimum time for $\overline{RAS}$ assertion to $\overline{RAS}$ assertion. These minimums correlate to DRAM spec t_{RC}.

		Wait States			
		0	1	2	3
Frequency	40 MHz	90	110	130	150
	33 MHz	110	130	150	170
	25 MHz	130	150	170	190
	20 MHz	150	170	190	210

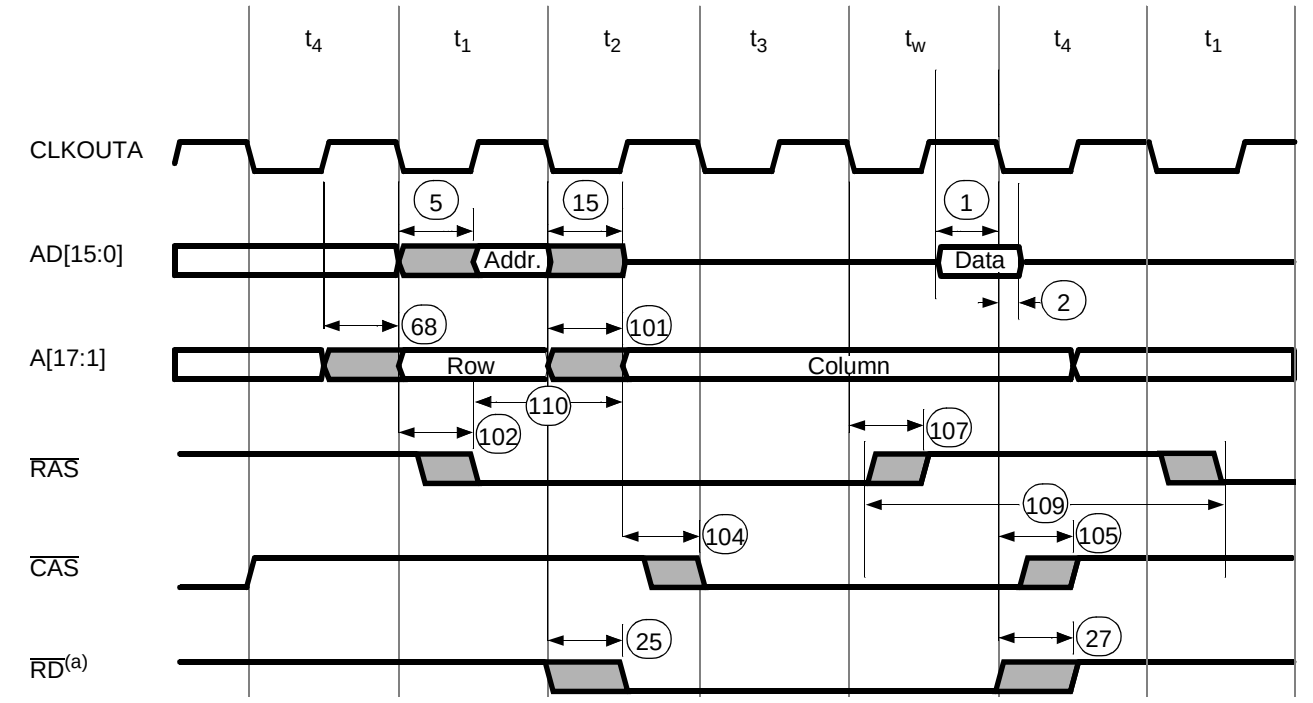
DRAM Read Cycle Timing with No-Wait States



Note:

a The $\overline{RD}$ output connects to the DRAM output enable ($\overline{OE}$) pin for read operations.

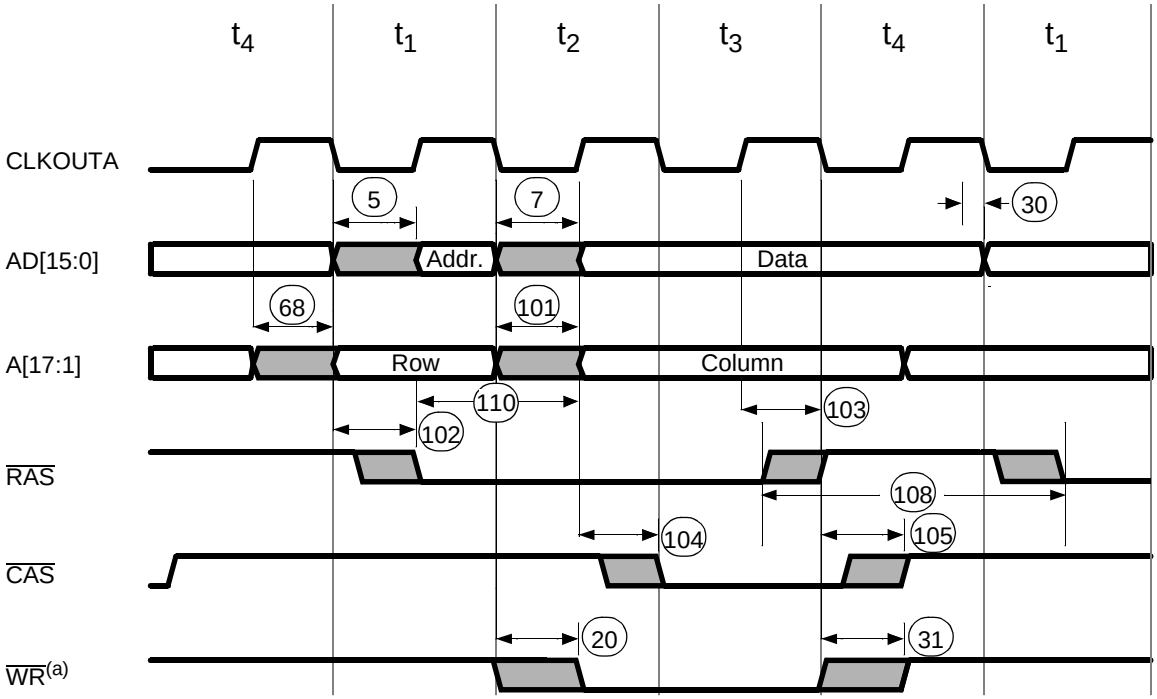
DRAM Read Cycle Timing with Wait State(s)



Note:

a The $\overline{RD}$ output connects to the DRAM output enable ($\overline{OE}$) pin for read operations.

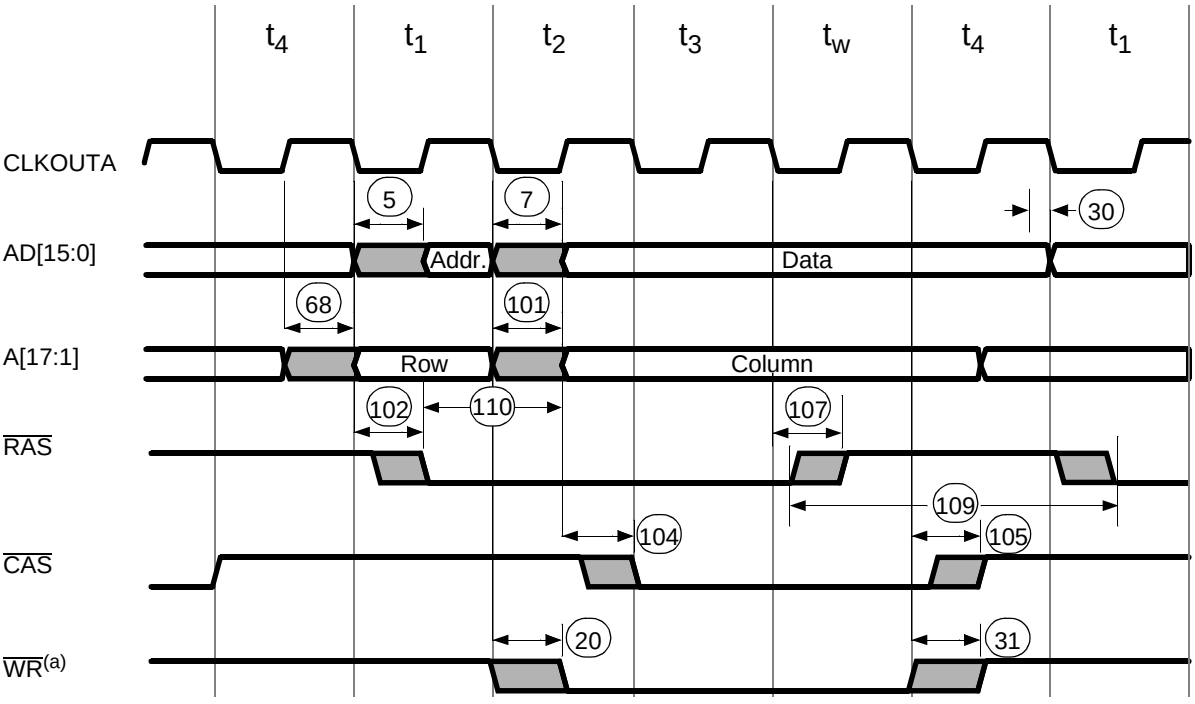
DRAM Write Cycle Timing with No-Wait States



Note:

a Write operations use the $\overline{WR}$ output connected to the DRAM write enable ($\overline{WE}$) pin.

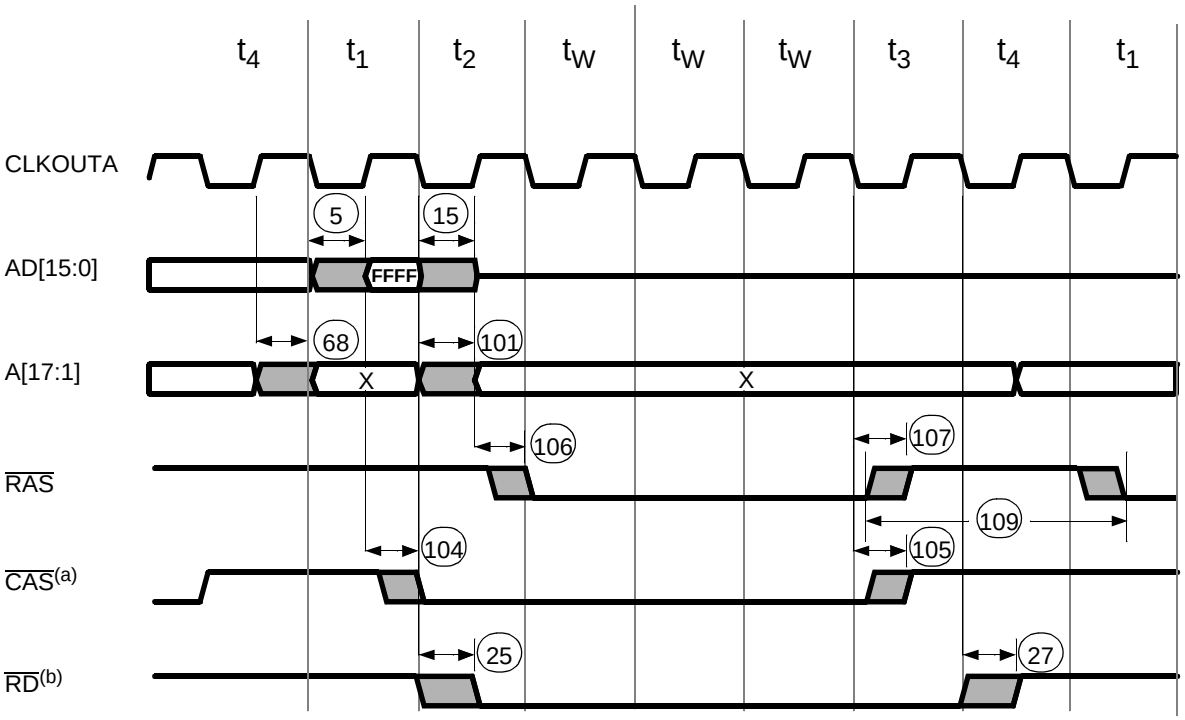
DRAM Write Cycle Timing With Wait State(s)



Note:

a Write operations use the $\overline{WR}$ output connected to the DRAM write enable ($\overline{WE}$) pin.

DRAM $\overline{CAS}$-before-$\overline{RAS}$ Cycle Timing



Notes:

a *$\overline{CAS}$ before $\overline{RAS}$ cycle timing is always 7 clocks, independent of wait state timing.*

b *The $\overline{RD}$ output connects to the DRAM output enable ($\overline{OE}$) pin for read operations.*

SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges

Interrupt Acknowledge Cycle (20 MHz and 25 MHz)

Parameter			Preliminary				Unit
			20 MHz		25 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Requirements							
1	t_{DVCL}	Data in Setup	10		10		ns
2	t_{CLDX}	Data in Hold	3		3		ns
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	25	0	20	ns
4	t_{CLSH}	Status Inactive Delay	0	25	0	20	ns
7	t_{CLDV}	Data Valid Delay	0	25	0	20	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		25		20	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=40$		$t_{CLCL}-10=30$		ns
11	t_{CHLL}	ALE Inactive Delay		25		20	ns
12	t_{AVLL}	AD Address Invalid to ALE Low[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
15	t_{CLAZ}	AD Address Float Delay	$t_{CLAX}=0$	25	$t_{CLAX}=0$	20	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
20	t_{CVCTV}	Control Active Delay 1[b]	0	25	0	20	ns
21	t_{CVDEX}	$\overline{DEN}$ Inactive Delay	0	25	0	20	ns
22	t_{CHCTV}	Control Active Delay 2[c]	0	25	0	20	ns
23	t_{LHAV}	ALE High to Address Valid	20		15		ns
31	t_{CVCTX}	Control Inactive Delay[b]	0	25	0	20	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	25	0	20	ns

Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L =50 pF. For switching tests, V_{IL}=0.45 V and V_{IH}=2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.

a Testing is performed with equal loading on referenced pins.

b This parameter applies to the $\overline{INTA1}$–$\overline{INTA0}$ signals.

c This parameter applies to the $\overline{DEN}$ and DT/$\overline{R}$ signals.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

Interrupt Acknowledge Cycle (33 MHz and 40 MHz)

Parameter			Preliminary				Unit
			33 MHz		40 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Requirements							
1	t_{DVCL}	Data in Setup	8		5		ns
2	t_{CLDX}	Data in Hold	3		2		ns
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	15	0	12	ns
4	t_{CLSH}	Status Inactive Delay	0	15	0	12	ns
7	t_{CLDV}	Data Valid Delay	0	15	0	12	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		15		12	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=20$		$t_{CLCL}-5=20$		ns
11	t_{CHLL}	ALE Inactive Delay		15		12	ns
12	t_{AVLL}	AD Address Invalid to ALE Low[a]	t_{CLCH}		t_{CLCH}		ns
15	t_{CLAZ}	AD Address Float Delay	$t_{CLAX}=0$	15	$t_{CLAX}=0$	12	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
20	t_{CVCTV}	Control Active Delay 1[b]	0	15	0	12	ns
21	t_{CVDEX}	$\overline{DEN}$ Inactive Delay	0	15	0	12	ns
22	t_{CHCTV}	Control Active Delay 2[c]	0	15	0	12	ns
23	t_{LHAV}	ALE High to Address Valid	10		7.5		ns
31	t_{CVCTX}	Control Inactive Delay[b]	0	15	0	12	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	15	0	10	ns

Notes:

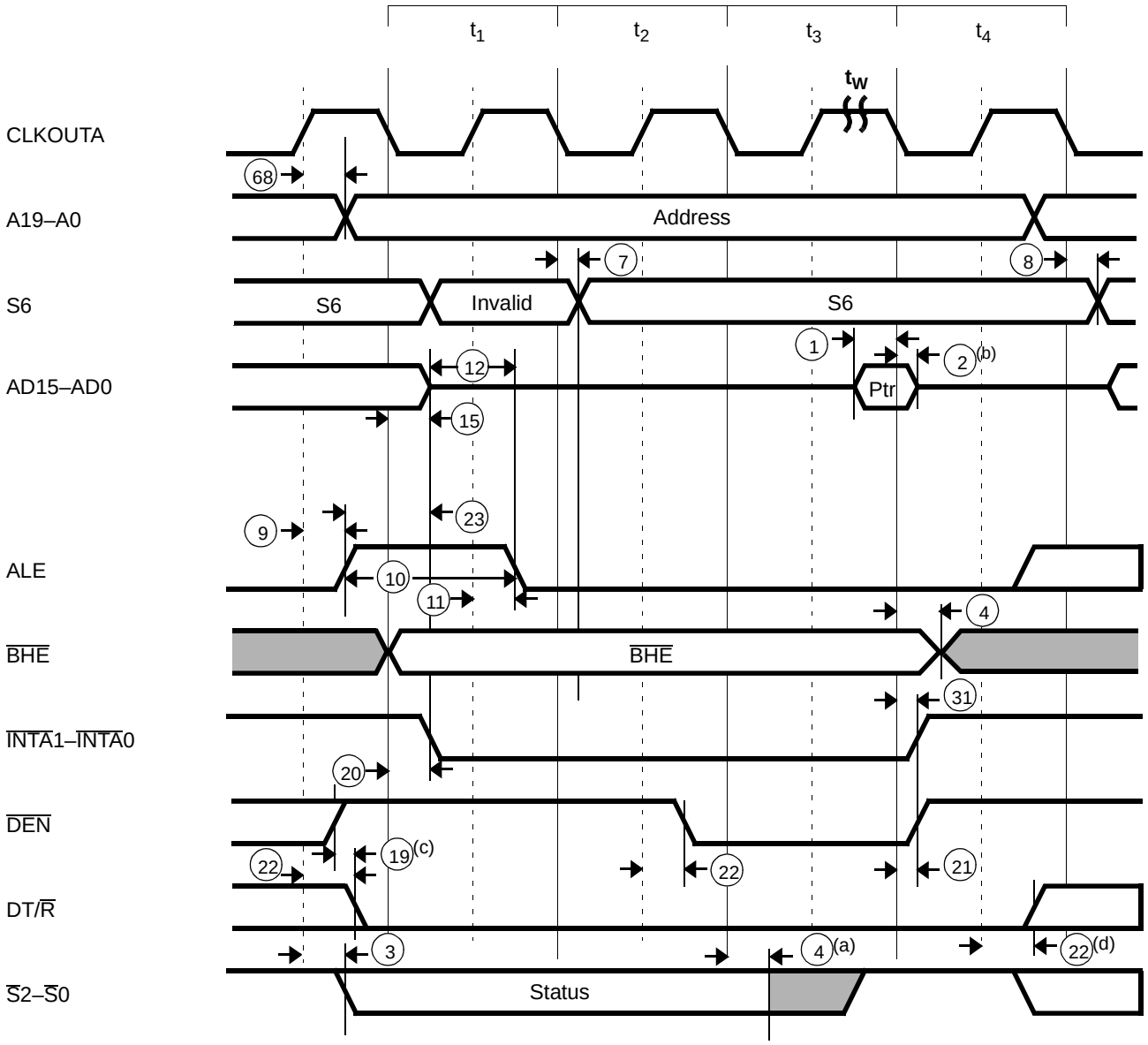
All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L =50 pF. For switching tests, V_{IL}=0.45 V and V_{IH}=2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.

a Testing is performed with equal loading on referenced pins.

b This parameter applies to the $\overline{INTA1}$–$\overline{INTA0}$ signals.

c This parameter applies to the $\overline{DEN}$ and DT/$\overline{R}$ signals.

INTERRUPT ACKNOWLEDGE CYCLE WAVEFORMS



Notes:

a The status bits become inactive in the state preceding t_4.

b The data hold time lasts only until the interrupt acknowledge signal deasserts, even if the interrupt acknowledge transition occurs prior to t_{CLDX} (min).

c This parameter applies for an interrupt acknowledge cycle that follows a write cycle.

d If followed by a write cycle, this change occurs in the state preceding that write cycle.

SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges Software Halt Cycle (20 MHz and 25 MHz)

Parameter			Preliminary				Unit
			20 MHz		25 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	25	0	20	ns
4	t_{CLSH}	Status Inactive Delay	0	25	0	20	ns
5	t_{CLAV}	AD Address Invalid Delay and BHE	0	25	0	20	ns
9	t_{CHLH}	ALE Active Delay		25		20	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=40$		$t_{CLCL}-10=30$		ns
11	t_{CHLL}	ALE Inactive Delay		25		20	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
22	t_{CHCTV}	Control Active Delay 2[b]	0	25	0	20	ns
68	t_{CHAV}	CLKOUTA High to A Address Invalid	0	25	0	20	ns

Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L =50 pF. For switching tests, V_{IL}=0.45 V and V_{IH}=2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.

a Testing is performed with equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$ signal.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges Software Halt Cycle (33 MHz and 40 MHz)

Parameter			Preliminary				Unit
			33 MHz		40 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	15	0	12	ns
4	t_{CLSH}	Status Inactive Delay	0	15	0	12	ns
5	t_{CLAV}	AD Address Invalid Delay and BHE	0	15	0	12	ns
9	t_{CHLH}	ALE Active Delay		15		12	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=20$		$t_{CLCL}-5=20$		ns
11	t_{CHLL}	ALE Inactive Delay		15		12	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
22	t_{CHCTV}	Control Active Delay 2[b]	0	15	0	12	ns
68	t_{CHAV}	CLKOUTA High to A Address Invalid	0	15	0	10	ns

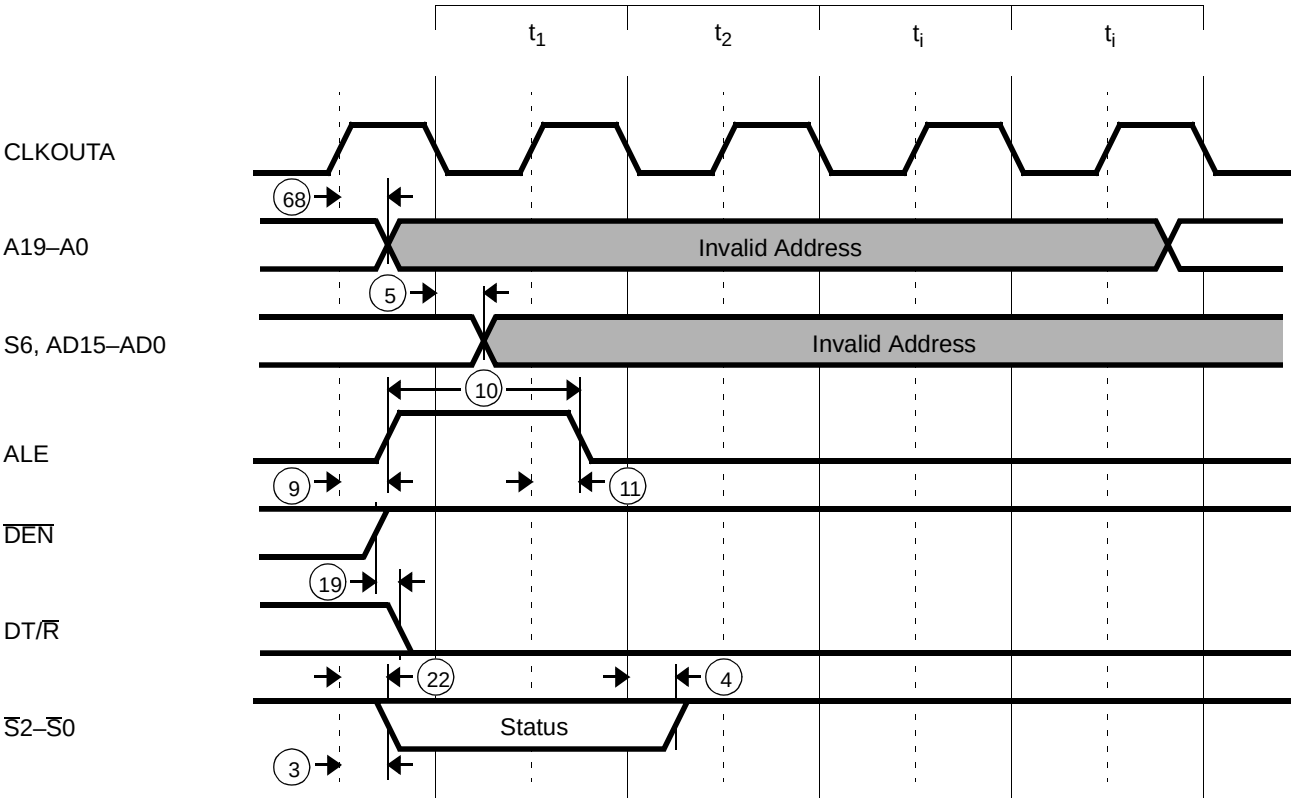
Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L =50 pF. For switching tests, V_{IL}=0.45 V and V_{IH}=2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.

a Testing is performed with equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$ signal.

SOFTWARE HALT CYCLE WAVEFORMS



SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges

Clock (20 MHz and 25 MHz)

Parameter			Preliminary				Unit
			20 MHz		25 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
CLKIN Requirements							
36	t_{CKIN}	X1 Period[a]	50	60	40	60	ns
37	t_{CLCK}	X1 Low Time (1.5 V)[a]	15		15		ns
38	t_{CHCK}	X1 High Time (1.5 V)[a]	15		15		ns
39	t_{CKHL}	X1 Fall Time (3.5 to 1.0 V)[a]		5		5	ns
40	t_{CKLH}	X1 Rise Time (1.0 to 3.5 V)[a]		5		5	ns
CLKOUT Timing							
42	t_{CLCL}	CLKOUTA Period	50		40		ns
43	t_{CLCH}	CLKOUTA Low Time (C_L=50 pF)	$0.5t_{CLCL}-2=23$		$0.5t_{CLCL}-2=18$		ns
44	t_{CHCL}	CLKOUTA High Time (C_L=50 pF)	$0.5t_{CLCL}-2=23$		$0.5t_{CLCL}-2=18$		ns
45	t_{CH1CH2}	CLKOUTA Rise Time (1.0 to 3.5 V)		3		3	ns
46	t_{CL2CL1}	CLKOUTA Fall Time (3.5 to 1.0 V)		3		3	ns
61	t_{LOCK}	Maximum PLL Lock Time		1		1	ms
69	t_{CICOA}	X1 to CLKOUTA Skew		15		15	ns
70	t_{CICOB}	X1 to CLKOUTB Skew		25		25	ns

Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L =50 pF. For switching tests, V_{IL}=0.45 V and V_{IH}=2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.

a The specifications for CLKIN are applicable to the normal PLL and CLKDIV2 modes.

The PLL should be used for operations from 16.667 MHz to 40 MHz. For operations below 16.667 MHz, the CLKDIV2 mode should be used.

Because the CLKDIV2 input frequency is two times the system frequency, the specifications for twice the frequency should be used for CLKDIV2 mode. For example, use the 20 MHz CLKIN specifications for 10 MHz operation.

SWITCHING CHARACTERISTICS over Commercial operating ranges

Clock (33 MHz and 40 MHz)

Parameter			Preliminary				
			33 MHz		40 MHz		
No.	Symbol	Description	Min	Max	Min	Max	Unit
CLKIN Requirements							
36	t_{CKIN}	X1 Period[a]	30	60	25	60	ns
37	t_{CLCK}	X1 Low Time (1.5 V)[a]	10		7.5		ns
38	t_{CHCK}	X1 High Time (1.5 V)[a]	10		7.5		ns
39	t_{CKHL}	X1 Fall Time (3.5 to 1.0 V)[a]		5		5	ns
40	t_{CKLH}	X1 Rise Time (1.0 to 3.5 V)[a]		5		5	ns
CLKOUT Timing							
42	t_{CLCL}	CLKOUTA Period	30		25		ns
43	t_{CLCH}	CLKOUTA Low Time (C_L=50 pF)	$0.5t_{CLCL}-1.5$ =13.5		$0.5t_{CLCL}-1.25$ =11.25		ns
44	t_{CHCL}	CLKOUTA High Time (C_L=50 pF)	$0.5t_{CLCL}-1.5$ =13.5		$0.5t_{CLCL}-1.25$ =11.25		ns
45	t_{CH1CH2}	CLKOUTA Rise Time (1.0 to 3.5 V)		3		3	ns
46	t_{CL2CL1}	CLKOUTA Fall Time (3.5 to 1.0 V)		3		3	ns
61	t_{LOCK}	Maximum PLL Lock Time		1		1	ms
69	t_{CICOA}	X1 to CLKOUTA Skew		15		15	ns
70	t_{CICOB}	X1 to CLKOUTB Skew		25		25	ns

Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L=50 pF. For switching tests, V_{IL}=0.45 V and V_{IH}=2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.

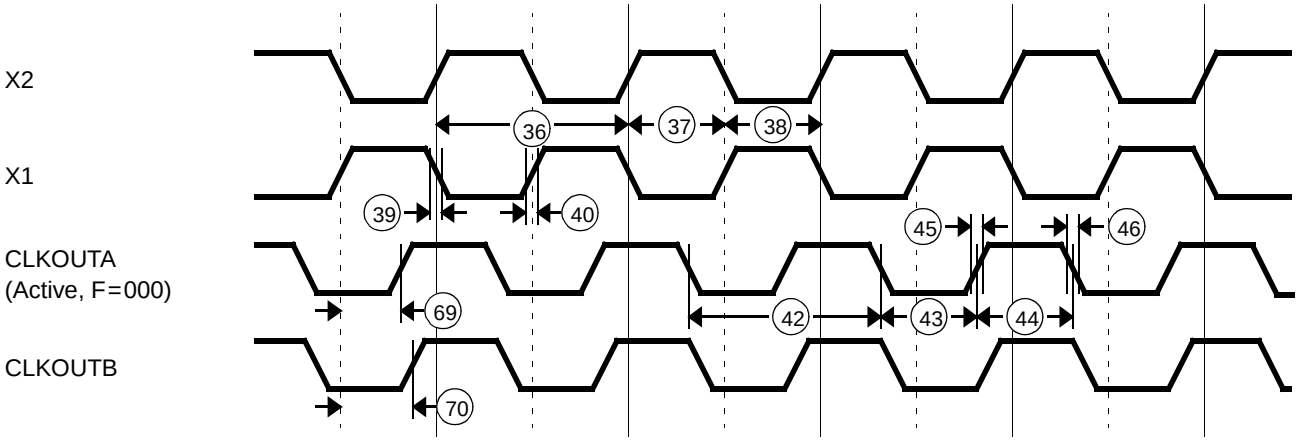
a The specifications for CLKIN are applicable to the normal PLL and CLKDIV2 modes.

The PLL should be used for operations from 16.667 MHz to 40 MHz. For operations below 16.667 MHz, the CLKDIV2 mode should be used.

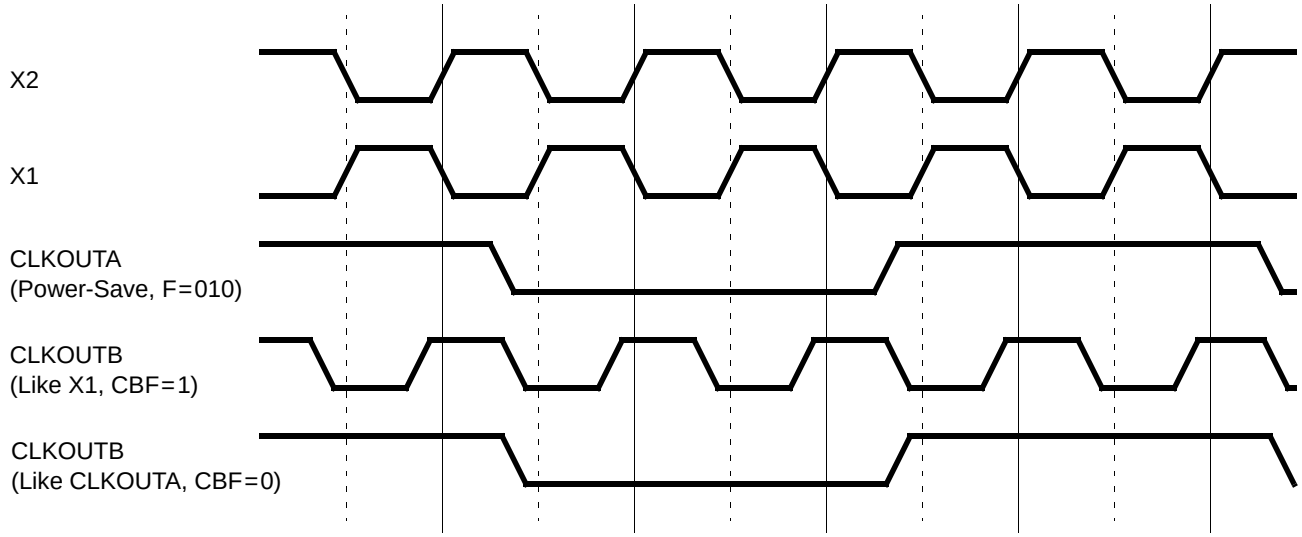
Because the CLKDIV2 input frequency is two times the system frequency, the specifications for twice the frequency should used for CLKDIV2 mode. For example, use the 20 MHz CLKIN specifications for 10 MHz operation.

CLOCK WAVEFORMS

Clock Waveforms—Active Mode



Clock Waveforms—Power-Save Mode



SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges
Ready and Peripheral (20 MHz and 25 MHz)

Parameter			Preliminary 20 MHz		Preliminary 25 MHz		Unit
No.	Symbol	Description	Min	Max	Min	Max	
Ready and Peripheral Timing Requirements							
47	t_{SRYCL}	SRDY Transition Setup Time[a]	10		10		ns
48	t_{CLSRY}	SRDY Transition Hold Time[a]	3		3		ns
49	t_{ARYCH}	ARDY Resolution Transition Setup Time[b]	10		10		ns
50	t_{CLARX}	ARDY Active Hold Time[a]	4		4		ns
51	t_{ARYCHL}	ARDY Inactive Holding Time	6		6		ns
52	t_{ARYLCL}	ARDY Setup Time[a]	15		15		ns
53	t_{INVCH}	Peripheral Setup Time[b]	10		10		ns
54	t_{INVCL}	DRQ Setup Time[b]	10		10		ns
Peripheral Timing Responses							
55	t_{CLTMV}	Timer Output Delay		25		20	ns

Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L =50 pF. For switching tests, V_{IL}=0.45 V and V_{IH}=2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.

a This timing must be met to guarantee proper operation.

b This timing must be met to guarantee recognition at the clock edge.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges
Ready and Peripheral (33 MHz and 40 MHz)

Parameter			Preliminary 33 MHz		Preliminary 40 MHz		Unit
No.	Symbol	Description	Min	Max	Min	Max	
Ready and Peripheral Timing Requirements							
47	t_{SRYCL}	SRDY Transition Setup Time[a]	8		5		ns
48	t_{CLSRY}	SRDY Transition Hold Time[a]	3		2		ns
49	t_{ARYCH}	ARDY Resolution Transition Setup Time[b]	8		5		ns
50	t_{CLARX}	ARDY Active Hold Time[a]	4		3		ns
51	t_{ARYCHL}	ARDY Inactive Holding Time	6		5		ns
52	t_{ARYLCL}	ARDY Setup Time[a]	10		5		ns
53	t_{INVCH}	Peripheral Setup Time[b]	8		5		ns
54	t_{INVCL}	DRQ Setup Time[b]	8		5		ns
Peripheral Timing Responses							
55	t_{CLTMV}	Timer Output Delay		15		12	ns

Notes:

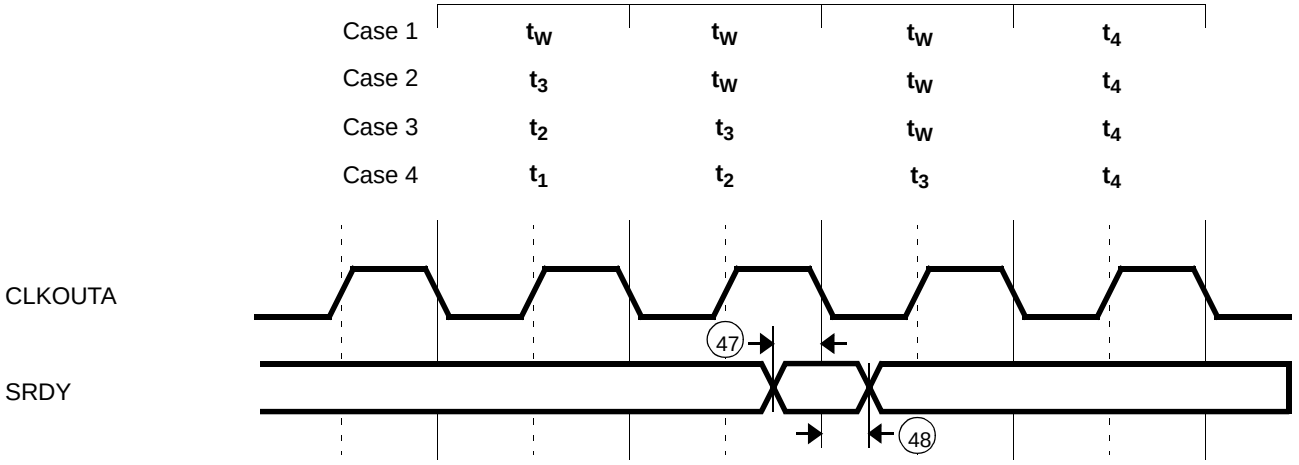
All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L =50 pF. For switching tests, V_{IL}=0.45 V and V_{IH}=2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.

a This timing must be met to guarantee proper operation.

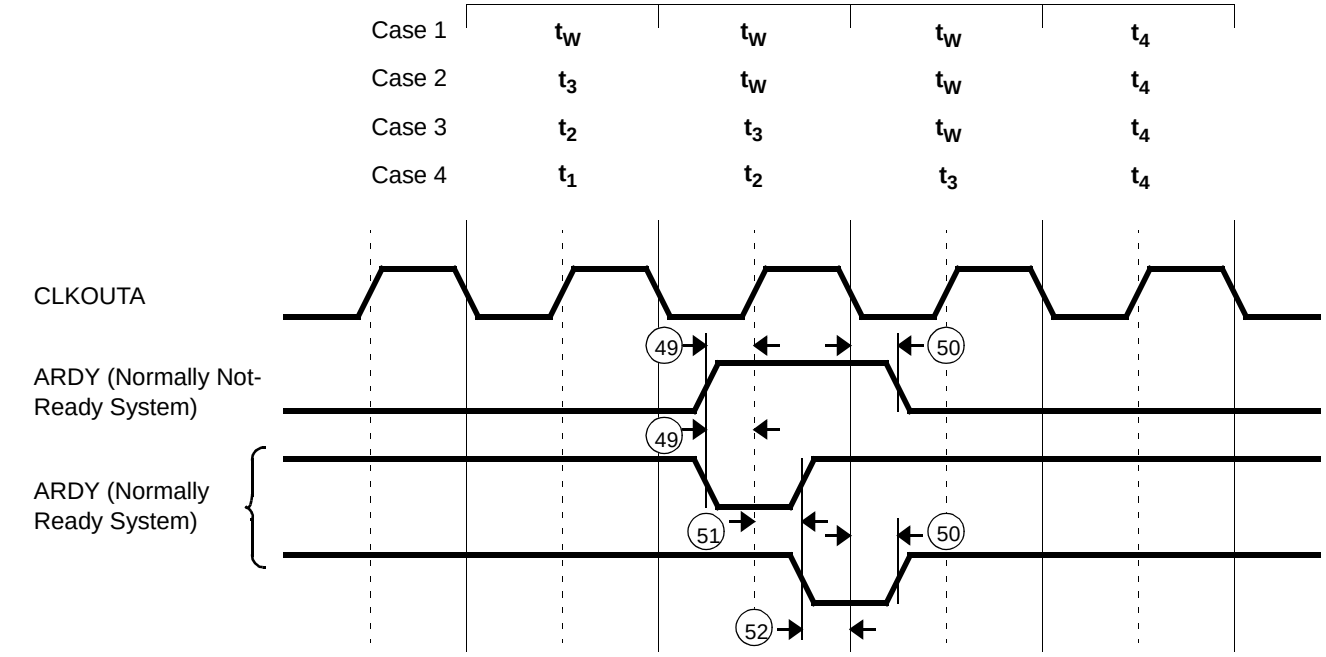
b This timing must be met to guarantee recognition at the clock edge.

SYNCHRONOUS, ASYNCHRONOUS, and PERIPHERAL WAVEFORMS

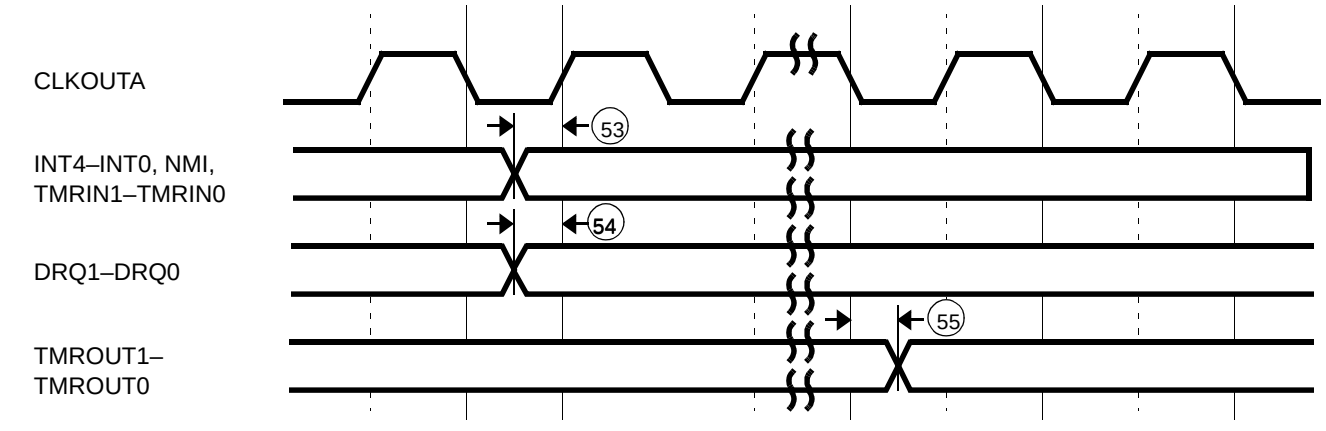
Synchronous Ready Waveforms



Asynchronous Ready Waveforms



Peripheral Waveforms



SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges
Reset and Bus Hold (20 MHz and 25 MHz)

Parameter			Preliminary				Unit
			20 MHz		25 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
Reset and Bus Hold Timing Requirements							
5	t_{CLAV}	AD Address Valid Delay and BHE	0	25	0	20	ns
15	t_{CLAZ}	AD Address Float Delay	0	25	0	20	ns
57	t_{RESIN}	$\overline{RES}$ Setup Time	10		10		ns
58	t_{HVCL}	HOLD Setup[(a)]	10		10		ns
Reset and Bus Hold Timing Responses							
62	t_{CLHAV}	HLDA Valid Delay	0	25	0	20	ns
63	t_{CHCZ}	Command Lines Float Delay		25		20	ns
64	t_{CHCV}	Command Lines Valid Delay (after Float)		25		20	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges
Reset and Bus Hold (33 MHz and 40 MHz)

Parameter			Preliminary				Unit
			33 MHz		40 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
Reset and Bus Hold Timing Requirements							
5	t_{CLAV}	AD Address Valid Delay and BHE	0	15	0	12	ns
15	t_{CLAZ}	AD Address Float Delay	0	15	0	12	ns
57	t_{RESIN}	$\overline{RES}$ Setup Time	8		5		ns
58	t_{HVCL}	HOLD Setup[(a)]	8		5		ns
Reset and Bus Hold Timing Responses							
62	t_{CLHAV}	HLDA Valid Delay	0	15	0	12	ns
63	t_{CHCZ}	Command Lines Float Delay		15		12	ns
64	t_{CHCV}	Command Lines Valid Delay (after Float)		15		12	ns

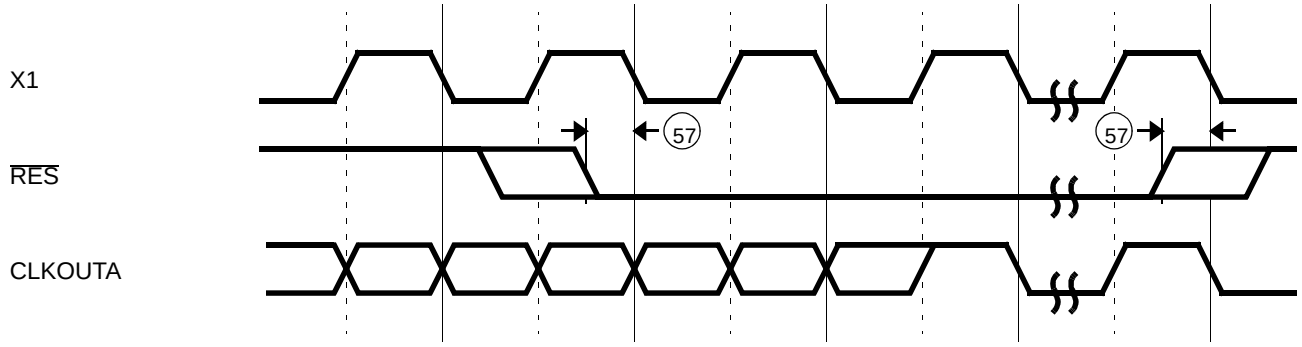
Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L =50 pF. For switching tests, V_{IL} =0.45 V and V_{IH} =2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.

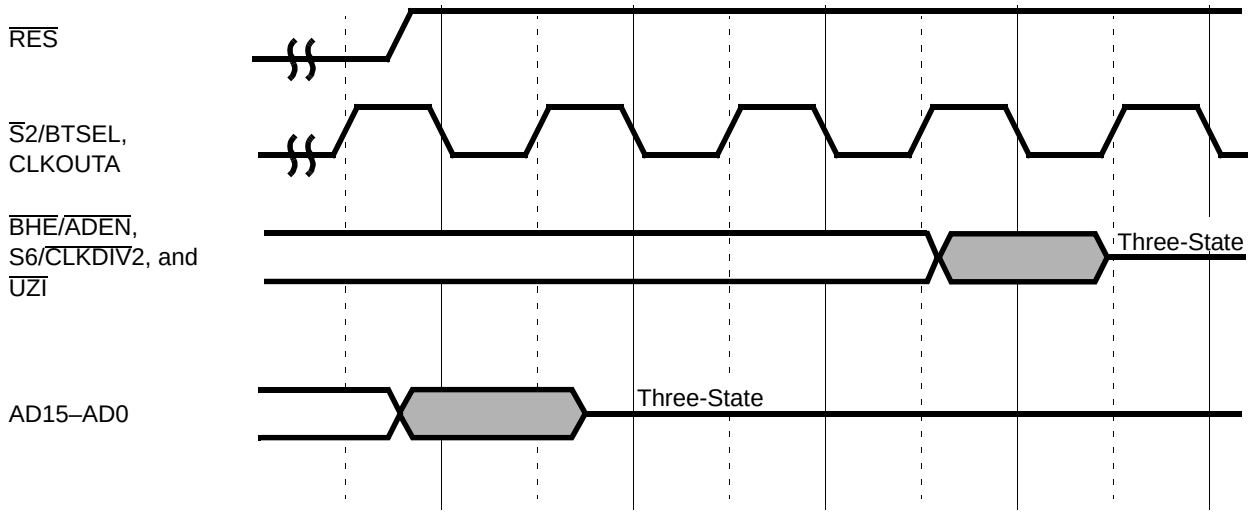
a This timing must be met to guarantee recognition at the next clock.

RESET and BUS HOLD WAVEFORMS

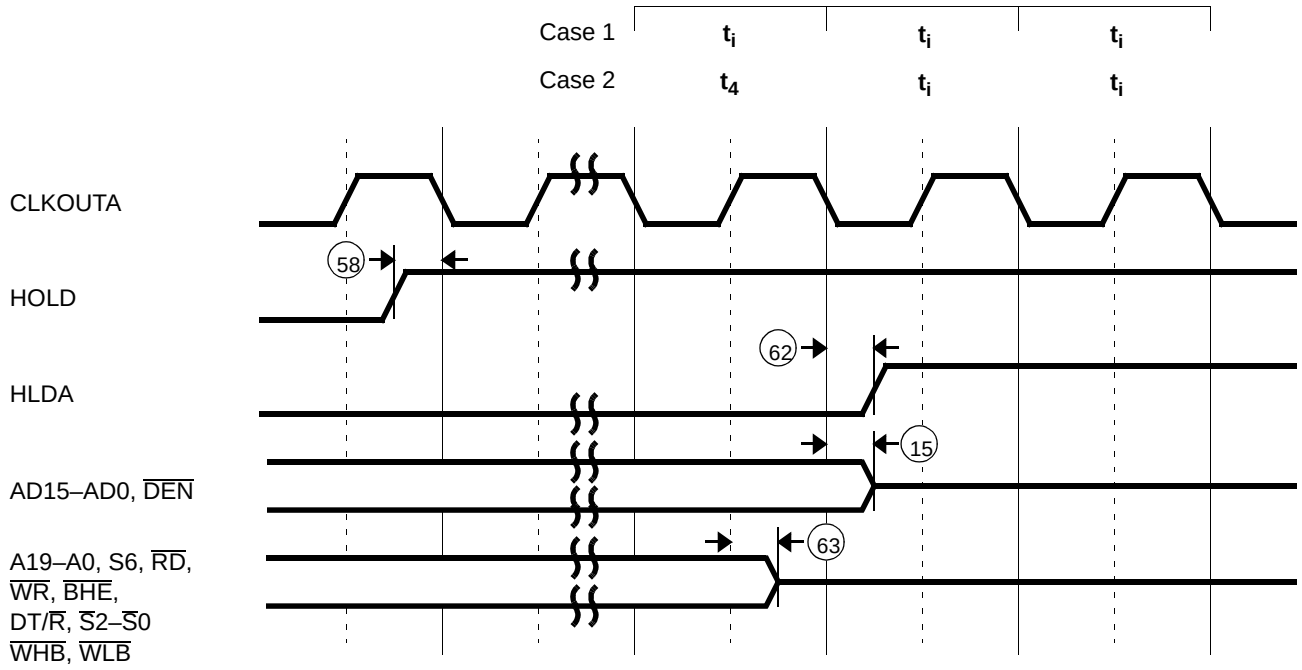
Reset Waveforms



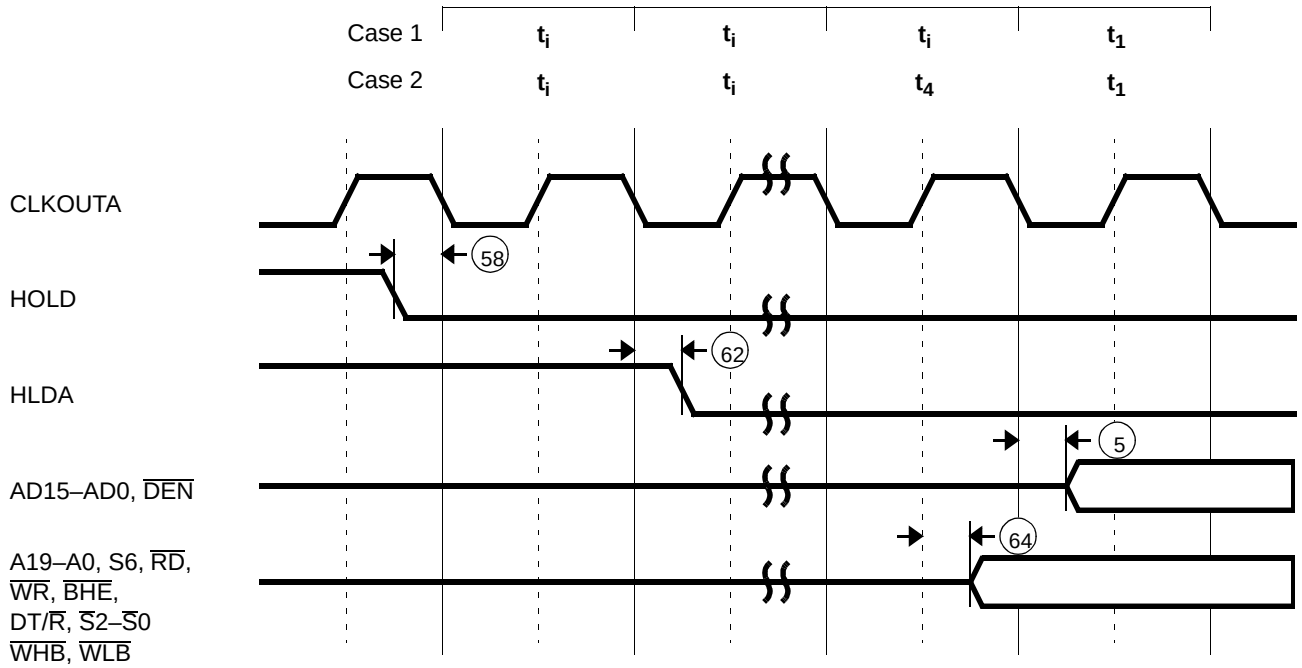
Signals Related to Reset Waveforms



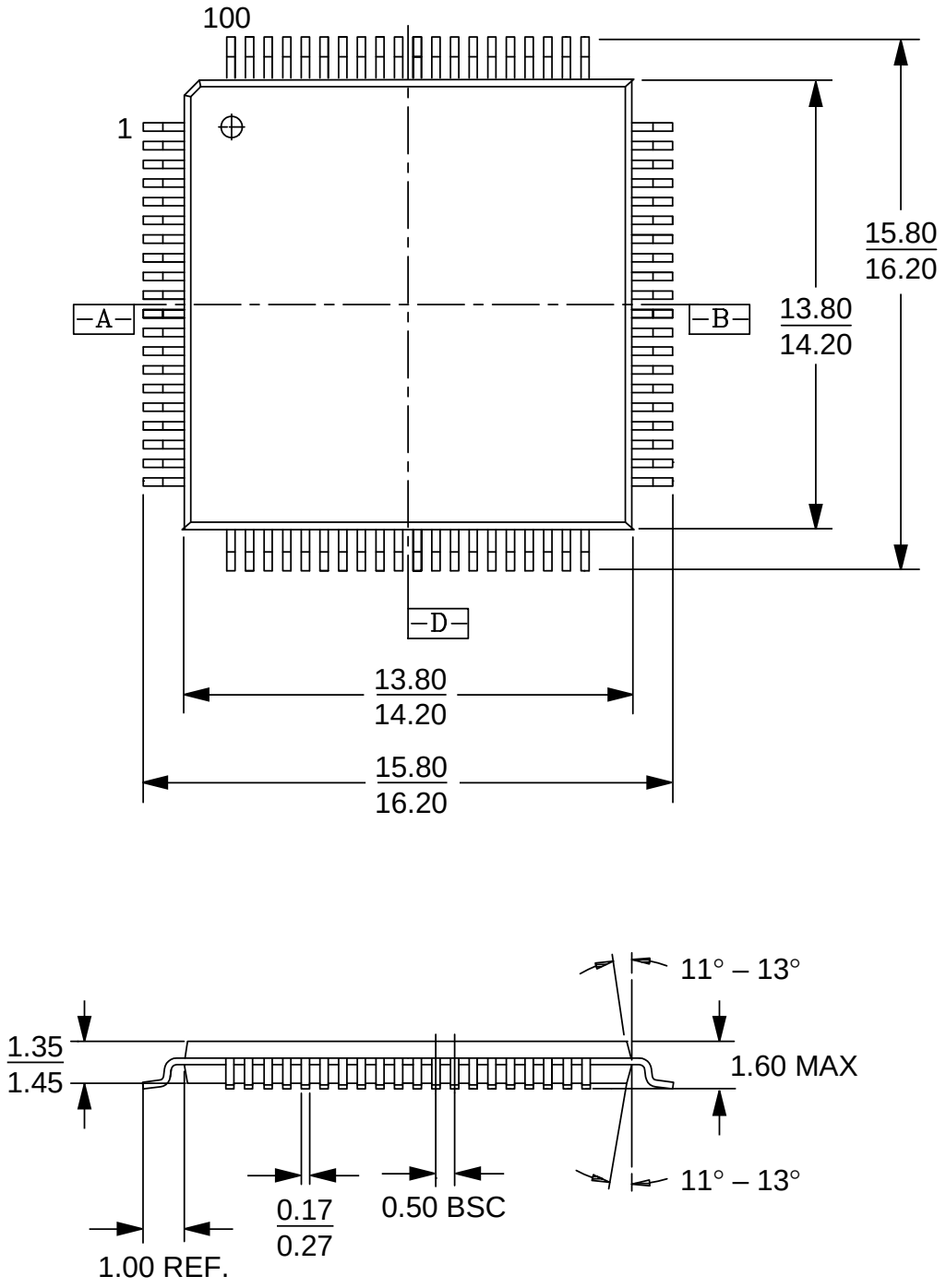
Bus Hold Waveforms—Entering



Bus Hold Waveforms—Leaving



TQFP PHYSICAL DIMENSIONS
PQL 100, Trimmed and Formed
Thin Quad Flat Pack

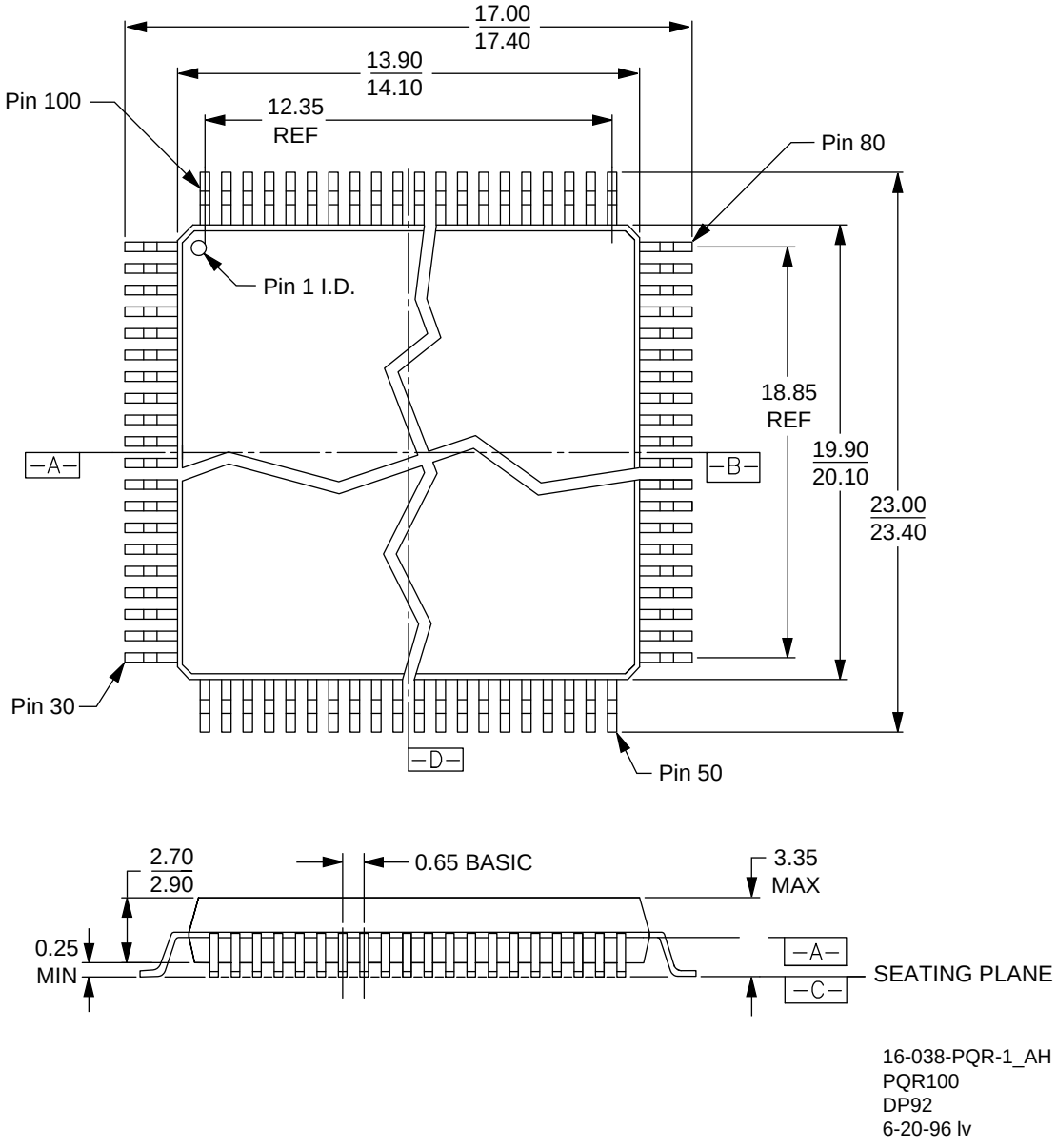


16-038-PQT-2_AI
PQL100
9.3.96 lv

Notes:

1. *All measurements are in millimeters, unless otherwise noted.*
2. *Not to scale; for reference only.*

PQFP PHYSICAL DIMENSIONS
PQR 100, Trimmed and Formed
Plastic Quad Flat Pack



16-038-PQR-1_AH
PQR100
DP92
6-20-96 lv

Notes:

1. *All measurements are in millimeters, unless otherwise noted.*
2. *Not to scale; for reference only.*