PRELIMINARY

DEVICE SPECIFICATION

AMCC®

# Q3500 SERIES ECL/TTL LOGIC ARRAYS

## FEATURES

### RANGE OF ARRAY SIZES
1300, 2400, and 3500 equivalent gate versions to support a wide range of circuit requirements.

### UP TO 120 I/O CAPABILITY
Each of the arrays in the series has a high I/O to gate ratio. The Q1300S, Q2400S, and Q3500S support 76, 98, and 120 I/O respectively.

### VERY HIGH SPEED
.275 to .700nS typical gate delay for complex circuits depending upon the macro performance level chosen.

### ECL & TTL COMPATIBLE
The Q3500 Series logic arrays are compatible with ECL, TTL or mixed ECL/TTL systems, in both single or dual power supply configurations. This flexible I/O structure eliminates the need for external ECL/TTL and TTL/ECL translation logic in high performance applications.

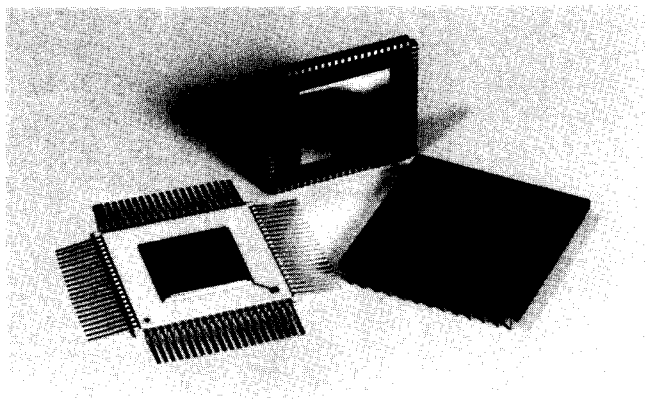
### SPEED/POWER PROGRAMMABILITY
The Q3500 Series offers the advantage of a flexible performance macro library. This feature allows the designer to customize the device capabilities to obtain the highest possible circuit throughput with the lowest possible overall power consumption.

### FULL MILITARY AVAILABILITY
These logic arrays are available for applications requiring MIL-STD-883C Class B screening including burn-in, and will operate over the military temperature range of −55° ambient to +125°C case.

### RADIATION HARD TECHNOLOGY
These devices feature an oxide-isolated bipolar process which is inherently tolerant to radiation.

| | |
|---|---|
| Typical gate delay* | .275 to .700ns |
| Maximum ECL input frequency | 300MHZ |
| Maximum TTL input frequency | 160 MHZ |
| Maximum ECL output frequency | 200 MHZ |
| Maximum TTL output frequency | 90 MHZ |
| ECL output drive | 50Ω |
| TTL output drive ($I_{OL}$) | 20MA |
| Average cell utilization | 95% |

TABLE 1



## DESCRIPTION
The AMCC Q3500 Series consists of the Q1300S, Q2400S, and Q3500S logic arrays providing equivalent densities of 1300, 2400, and 3500 gates, respectively. The series is optimized to provide a system approach to high performance semicustom applications. High speed ECL logic and proven reliability are combined with an advanced, interactive CAD system to provide a quick and cost-effective solution to discrete I.C. replacement.

Each device shares a common I/O logic and MSI macro library. The Q3500 Series arrays utilize advanced 3-level series gating techniques providing both density and speed improvements over gate-oriented and other macro-oriented designs.

An extensive library of predefined single and multiple cell logic macros is provided for the Q3500 Series. The library contains basic logic functions such as gates and flip-flops, in low power, standard and high speed versions. The extended MSI library provides commonly used logic functions, such as four-bit counters and shift registers, which are organized to provide improved speed and circuit density over logically equivalent SSI macros. The availability of extended macro libraries, combined with a flexible I/O structure, provides the circuit designer with a very versatile solution to high performance circuit design.

| | | | |
|---|---|---|---|
| Equivalent gate complexity | 1300 | 2400 | 3500 |
| Internal logic cells | 84 | 153 | 242 |
| I/O cells | 76 | 98 | 120 |
| % of high speed macros supported (Typical) | 100% | 30-40% | 30 to 40% |
| Typical power dissipation per internal cell in mW | 4 to 15 | 4 to 15 | 4 to 15 |
| Typical total circuit dissipation in watts @ 95% utilization* | 1.1W to 1.6 W | 2.1W to 2.9W | 3.4W to 4.5W |

TABLE 2

*Based upon the use of complex macros and the availability of macro speed/power options.

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# Q3500 SERIES DIE LAYOUTS

**Q3500S** — Die Size 362 Mils x 367 Mils

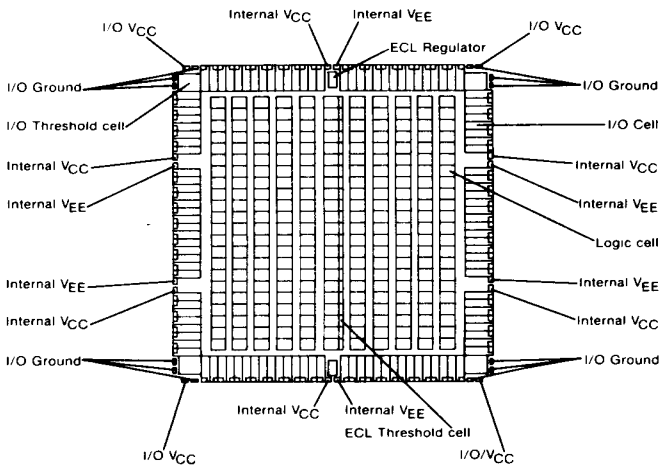



FIGURE 1

**Q2400S** — Die Size 314 Mils x 308 Mils

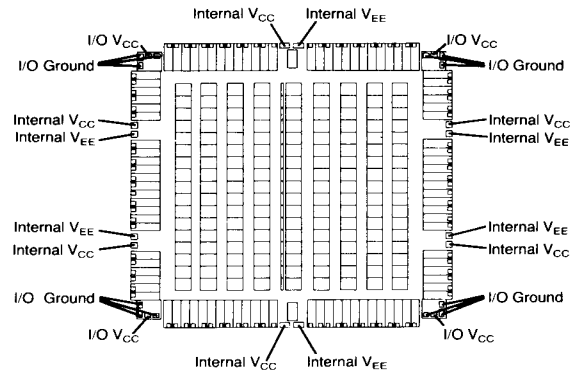



FIGURE 2

**Q1300S** — Die Size 272 Mils x 257 Mils

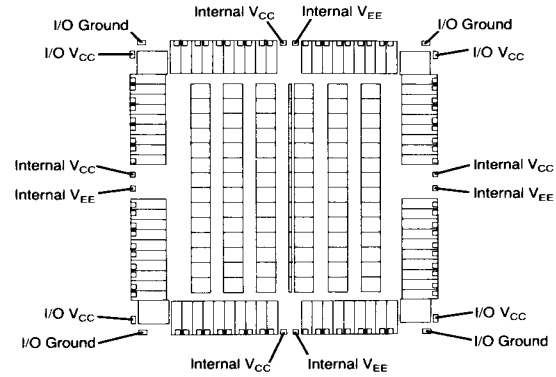



FIGURE 3

## ARRAY ARCHITECTURE

The Q3500 Series logic array structure is comprised of two basic configurable cell types, plus array overhead circuitry such as bias generators, voltage references and voltage regulators. The macro libraries provide the available and I/O logic functions which can be assigned to the user-configurable internal logic cells and I/O cells. The internal overhead circuitry is predefined by AMCC. Multiple power and ground connections are provided on the perimeter of the devices to support the various I/O modes minimizing noise feedback due to output switching. These power connections are isolated from the internal power busses.

| INTERNAL RESOURCE SUMMARY | | | |
|---|---|---|---|
| | Q1300S | Q2400S | Q3500S |
| Internal logic cells | 84 | 153 | 242 |
| I/O cells | 76 | 98 | 120 |

TABLE 3

As shown in Table 3, each array in the Q3500 Series has a different quantity of configurable cell resources available. However these arrays all contain identical cell types and are supported by a single macro library. The logic cells make up the array core.

The I/O cells are located around the perimeter of the array. They are used to implement ECL 10K, ECL 100K or TTL I/O. Additional logic can be incorporated into the I/O cell depending upon the macro chosen.

**I/O RESOURCES**

| MODE | DESCRIPTION | Q1300S | Q2400S | Q3500S |
|---|---|---|---|---|
| TTL SYSTEMS | I/O Cells<br>$V_{CC}$ (+5.0$V_{DC}$ nom.)<br>Ground | 76<br>8<br>8 | 98<br>10<br>18 | 120<br>10<br>18 |
| ECL SYSTEMS | I/O Cells<br>$V_{EE}$ (−4.5$V_{DC}$ to -5.2$V_{DC}$)<br>Ground | 76<br>8<br>8 | 98<br>6<br>22 | 120<br>6<br>22 |
| MIXED ECL/TTL SYSTEMS | I/O Cells (TTL or ECL)<br>$V_{CC}$ (+5.0$V_{DC}$ nom.)<br>$V_{EE}$ (−4.5$V_{DC}$ to −5.2$V_{DC}$)<br>TTL Ground<br>ECL Ground | 76<br>4<br>4<br>4<br>4 | 98<br>4<br>6<br>8<br>10 | 120<br>4<br>6<br>8<br>10 |
| +5.0V ONLY ECL ECL/TTL SYSTEMS | I/O Cells<br>$V_{DC}$(+5.0$V_{DC}$nom.)<br>Ground | 76<br>8<br>8 | 98<br>14<br>14 | 120<br>14<br>14 |

TABLE 4

## INTERNAL LOGIC CELL CAPABILITIES

The Q3500 Series arrays have 84, 153, and 242 internal logic cells respectively. These cells have identical structure, and are positioned in uniform columns across the arrays. Containing 80 uncommitted transistors and resistors each, these cells are individually configurable to provide a variety of logic functions through the use of the Q3500 Series internal logic macro library. As shown in Figure 4, the macro library provides for SSI, MSI, and some basic LSI functions. An MSI library is available for the more frequently used complex logic functions (adders, counters, shift registers, parity generators, etc.). These MSI logic macros uniquely interconnect a larger number of transistor and resistor components than may be contained in a single cell. This higher level of integration provides the advantages of higher speed, lower power, and higher circuit density over a logically equivalent macro implementation.

## TYPICAL MACROS

Illustrated in Figures 5 and 6 are typical examples of macros found in the library. Each of the standard macros occupies up to one internal logic cell location and is organized much like circuits in a TTL or ECL logic catalog. Additionally, the MSI logic macros are available for frequently required high level logic functions.

## HIGH SPEED/LOW POWER MACROS

The Q3500 Series macro library offers maximum flexibility in regard to circuit performance and power consumption. A full complement of macros is offered with low power, standard and high speed options. The high speed options require somewhat more power, but provide enhanced performance. The Q3500 Series macro library also contains low power versions of the macros which can be used to reduce power consumption in non-critical paths.

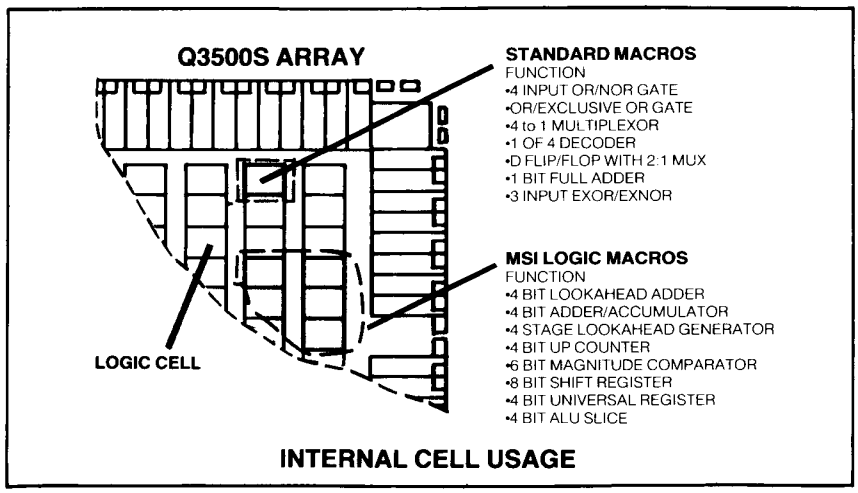



FIGURE 4

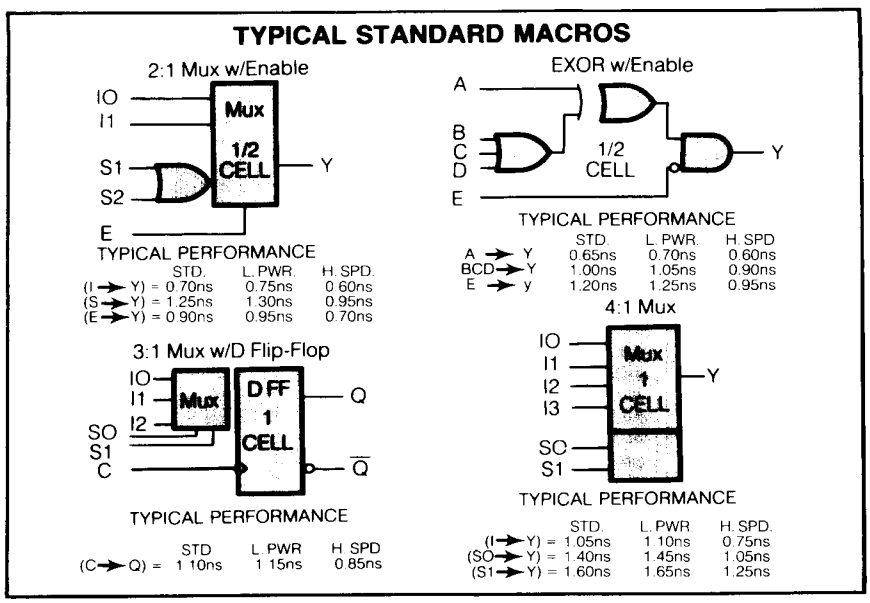



FIGURE 5

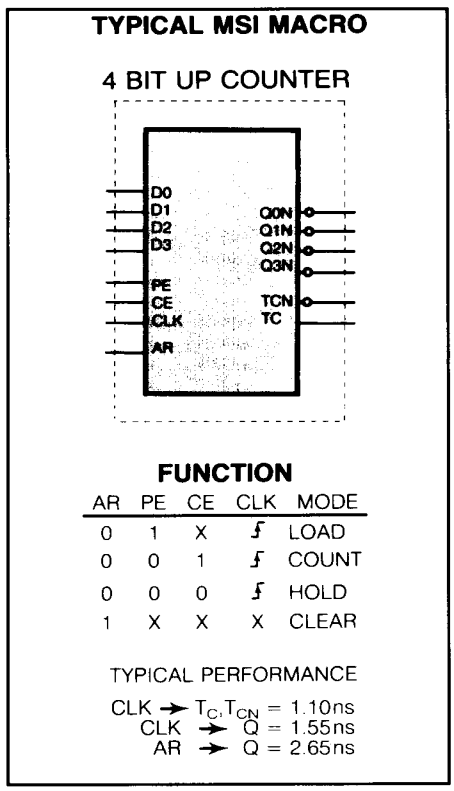



FIGURE 6

Table 5 illustrates the performance and power differences of typical Q3500 Series macros. As shown, the overall macro performance versus power consumption can significantly vary, allowing the circuit designer maximum flexibility for performance enhancement and/or power savings.

| Macro Options | | | |
|---|---|---|---|
| Internal | HS | Std. | LP |
| Equivalent Gate Delay (ps) | 350 | 500 | 700 |
| Equivalent Gate Power (mW) | 1.7 | 1.3 | 1 |
| I/O Pair Delay | HS | Std. | LP |
| TTL (ns) | 5 | 6 | 9 |
| ECL (ns) | | 1.3 | – |

TABLE 5

## HIGH PERFORMANCE, LOW POWER

Figure 7 illustrates the power savings of a complex logic circuit which has been designed using a mix of high speed and low power macros. Only a portion of the circuit requires high performance macros, with the remainder designed with standard or low power macros.

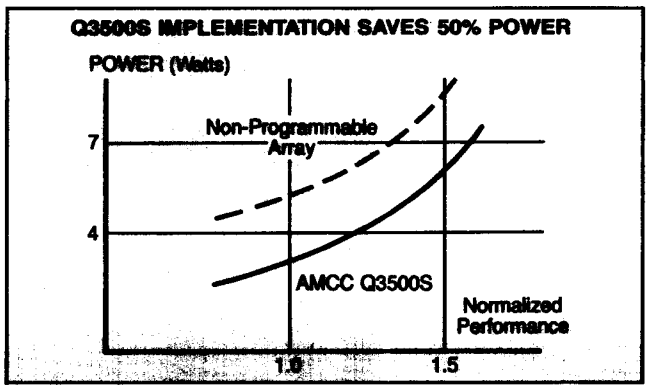



FIGURE 7

## FLEXIBLE I/O STRUCTURE

The Q3500 Series I/O cells are configurable to provide a full range of interface options.

| INPUT | BI-DIRECTIONAL | OUTPUT |
|---|---|---|
| TTL<br>ECL 10K<br>ECL 100K<br>TTL 3-state enable<br>ECL output enable | TTL transceiver<br>ECL 10K transceiver<br>ECL 100K transceiver | TTL totem pole<br>TTL 3-state<br>TTL open collector<br>ECL 10K<br>ECL 100K |

The Q3500 Series arrays also offer the following special options to support unique I/O requirements: high speed and low power TTL I/O (see Table 5), differential ECL I/O, +5V power only ECL and TTL.

The mixed ECL/TTL capabilities allow the use of both technologies in a single design without the use of external translators.

The +5V only ECL allows partitioning of a high speed TTL design into multiple AMCC devices using a single +5V supply, while providing high speed ECL I/O between arrays and full system TTL compatibility.

## DESIGN INTERFACE

The AMCC circuit development interface has been structured to provide maximum flexibility with respect to customer involvement. AMCC provides the MacroMatrix™ design kit with fully supported macro libraries on several popular engineering workstations for on-site array development. The following MacroMatrix CAD software tools are available.

WORKSTATION SUPPORT
- Schematic capture
- Logic simulation
- Engineering rule checks
- Post route timing verification

In addition, AMCC has developed a comprehensive set of CAD tools to assure "correct by construction" quick turnaround logic array designs.

AMCC CAD TOOLS
- Auto placement and routing
- Interactive preplace, preroute
- Test vector generation
- Test fault coverage grading
- Design rule & interconnect verification
- Post-route timing verification

These CAD tools are used by AMCC to complete a circuit design from an engineering workstation-generated schematic and simulation output.

## AMCC-PROVIDED SERVICES

In addition to providing the required CAD capability to allow customer design of arrays, AMCC provides a number of services to support customer design including: logic conversion and simulation, custom macro development, high-level engineering support, comprehensive training courses.

## PACKAGING

The Q3500 Series devices are available in any of the following package configurations. Requirements for special packaging will be evaluated on an individual basis.

| PACKAGE PIN COUNT | PACKAGE TYPE | Q1300S 92 PADS | Q2400S 126 PADS | Q3500S 148 PADS |
|---|---|---|---|---|
| 24 | DIP | • | | |
| 28 | DIP | • | | |
| 40 | DIP<br>LCC | •<br>• | | |
| 44 | LCC | • | | |
| 48 | DIP | • | | |
| 64 | LDCC<br>LDFP | •<br>• | | |
| 68 | PGA<br>LCC | •<br>• | •<br>• | • |
| 84 | PGA<br>LDFP | •<br>• | •<br>• | •<br>• |
| 100 | PGA*<br>LDCC | •<br>• | •<br>• | •<br>• |
| 148 | PGA* | | • | • |

LDCC — Leaded Chip Carrier
LCC — Leadless Chip Carrier
DIP — Dual In Line
PGA — Pin Grid Array
LDFP — Leaded Flat Pack
*Cavity Down

TABLE 6

# Q3500 SERIES ECL MODE OPERATING CONDITIONS

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|
| Supply Voltage ($V_{EE}$) $V_{CC}$ = 0 | | | | |
| ECL 10K Mode | −4.7 | −5.2 | −5.7 | V |
| ECL 100K Mode | −4.2 | −4.5 | −5.7 | V |
| Input Signal Rise/Fall Time | | | 1.0 | ns |
| Junction Temperature | | | | |
| Military | | | 150 | °C |
| Commercial | | | 130 | °C |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage $V_{EE}$ ($V_{CC}$ = 0) | −8.0 V DC |
| Input Voltage ($V_{CC}$ = 0) | GND to $V_{EE}$ |
| Output Source Current Continuous | −50mA DC |
| Operating Temperature | −55°C (Ambient) to +125°C (Case) |
| Operating Junction Temperature $T_J$ | +150°C |
| Storage Temperature | −65°C to +150°C |

## ECL 10K INPUT/OUTPUT DC CHARACTERISTICS $V_{EE}$ = −5.2V[1]

| | $T_{ambient}$ | | | | $T_{case}$ | |
|---|---|---|---|---|---|---|
| | −55°C | 0°C | 25°C | 75°C | 125°C | UNIT |
| $V_{OH\,max}$ | $V_{CC}$–850 | $V_{CC}$–770 | $V_{CC}$–730 | $V_{CC}$–650 | $V_{CC}$–575 | mV |
| $V_{IH\,max}$ | $V_{CC}$–800 | $V_{CC}$–720 | $V_{CC}$–680 | $V_{CC}$–600 | $V_{CC}$–525 | mV |
| $V_{OH\,min}$ | $V_{CC}$–1080 | $V_{CC}$–1000 | $V_{CC}$–980 | $V_{CC}$–920 | $V_{CC}$–850 | mV |
| $V_{IH\,min}$ | $V_{CC}$–1255 | $V_{CC}$–1145 | $V_{CC}$–1105 | $V_{CC}$–1045 | $V_{CC}$–1000 | mV |
| $V_{IL\,max}$ | $V_{CC}$–1510 | $V_{CC}$–1490 | $V_{CC}$–1475 | $V_{CC}$–1450 | $V_{CC}$–1400 | mV |
| $V_{OL\,max}$ | $V_{CC}$–1655 | $V_{CC}$–1625 | $V_{CC}$–1620 | $V_{CC}$–1585 | $V_{CC}$–1545 | mV |
| $V_{OL\,min}$ | $V_{CC}$–1980 | $V_{CC}$–1980 | $V_{CC}$–1980 | $V_{CC}$–1980 | $V_{CC}$–1980 | mV |
| $V_{IL\,min}$ | $V_{CC}$–2000 | $V_{CC}$–2000 | $V_{CC}$–2000 | $V_{CC}$–2000 | $V_{CC}$–2000 | mV |
| $I_{in}$ H max[2] | 30 | 30 | 30 | 30 | 30 | µA |
| $I_{in}$ L min[2] | .5 | .5 | .5 | .5 | .5 | µA |

## ECL 100K INPUT/OUTPUT DC CHARACTERISTICS $V_{EE}$ = -4.5V[3]

| SYMBOL | PARAMETER | TEST DC CONDITIONS | COMM 0° / +70°C | | | MIL–55° / +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{EE}$ = −4.2V to −4.8V | | | $V_{EE}$ = −4.5V to −4.8V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ | Output Voltage HIGH | Loading is 50 Ohms to -2V | $V_{CC}$-1035 | | $V_{CC}$-850 | $V_{CC}$-1080 | | $V_{CC}$-835 | mV |
| $V_{OL}$ | Output Voltage LOW | Loading is 50 Ohms to -2V | $V_{CC}$-1830 | | $V_{CC}$-1605 | $V_{CC}$-1880 | | $V_{CC}$-1595 | mV |
| $V_{IH\,min}$ | Input Voltage HIGH | Maximum input voltage HIGH | $V_{CC}$-1145 | | $V_{CC}$-800 | $V_{CC}$-1145 | | $V_{CC}$-800 | mV |
| $V_{IL\,max}$ | Input Voltage LOW | Maximum input voltage LOW | $V_{CC}$-1950 | | $V_{CC}$-1475 | $V_{CC}$-1950 | | $V_{CC}$-1475 | mV |
| $I_{INL}$[2] | Input Current | $V_{IN}$ = $V_{ILmin}$ | 0.5 | | | 0.5 | | | µA |

## AC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | | TEST CONDITIONS | COMM 0° / +70°C | | | MIL–55° / +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{IPD}$ | Input Propagation Delay Including Buffer | | | | 0.5 | | | 0.5 | | ns |
| $t_{OPD}$ | Output Propagation Delay | | 5pF,50Ω to -2V | | 0.8 | | | 0.8 | | ns |
| $t_{FPD}$ | Internal Equivalent Gate Delay[4] | Standard | | | 0.5 | | | 0.5 | | ns |
| | | Low Power | | | 0.7 | | | 0.7 | | ns |
| | | High Speed | | | 0.35 | | | 0.35 | | ns |
| $F_{MAXT}$ | Max. Internal Flip/Flop Toggle Frequency | Standard | | | 250 | | | 250 | | MHz |
| | | Low Power | | | 200 | | | 200 | | MHz |
| | | High Speed | | | 400 | | | 400 | | MHz |
| $F_{IN}$[5] | Maximum Input Frequency At Package Pin | Standard | | | 175 | | | 175 | | MHz |
| | | High Speed | | | 300 | | | 300 | | MHz |

1 Data measured with $V_{EE}$ = −5.2 ± .1V (or $V_{CC}$ = 5.0 ± .1V for +5V ref. ECL 10K) assuming a +50°C rise between ambient ($T_a$) and junction temperature ($T_J$) for −55°C, 0°C, +25°C, and +70°C, and a +25°C rise for +125°C. Specifications will vary based upon $T_J$. See AMCC Packaging and Design Guides concerning $V_{OH}$ and $V_{OL}$ adjustments associated with $T_J$ for specific packages and operating conditions.
2 Per fan-in.
3 Data measured at thermal equilibrium, with maximum $T_J$ not to exceed recommended limits. See AMCC Packaging Guide to compute $T_J$ for specific package and operating conditions. For +5V ref. ECL 100K, $V_{OH}$ and $V_{OL}$ specifications will vary based upon power supply. See AMCC Design Guide for adjustment factors.
4 Logic cell delays are for each gating level of a more complex logic function (i.e. D flip/flop, 4 to 1 mux, etc.)
5 Package selection will determine the maximum input frequency. Consult AMCC.

# Q3500 SERIES TTL MODE OPERATING CONDITIONS

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage ($V_{CC}$) | | | | |
| Military | 4.5 | 5.0 | 5.5 | V |
| Commercial | 4.75 | 5.0 | 5.25 | V |
| Output Current Low ($I_{OL}$) | | | | |
| Military | | | 20 | mA |
| Commercial | | | 20 | mA |
| Operating Temperature | | | | |
| Military | −55 (ambient) | | +125 (case) | °C |
| Commercial | 0 (ambient) | | 70 (ambient) | °C |
| Junction Temperature $T_J$ | | | | |
| Military | | | 150 | °C |
| Commercial | | | 130 | °C |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage ($V_{CC}$), $V_{EE}$ = 0 | 7.0V |
| Input Voltage | 5.5V |
| Operating Temperature | −55°C (Ambient) to +125°C(Case) |
| Junction Temperature (Operating) | 150°C |
| Storage Temperature | −65°C to +150°C |

## INPUT/OUTPUT DC CHARACTERISTICS

| SYMBOL | PARAMETER | TEST DC CONDITIONS | COMM -0° / +70°C | | | MIL-55° / +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Typ[1] | Max | |
| $V_{IH}$[2] | Input HIGH voltage | Guaranteed input HIGH voltage for all inputs | 2.0 | | | 2.0 | | | V |
| $V_{IL}$[2] | Input LOW voltage | Guaranteed input LOW voltage for all inputs | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp diode voltage | $V_{CC}$ − Min, $I_{IN}$ = − 18mA | | -.8 | -1.2 | | -.8 | -1.2 | V |
| $V_{OH}$ | Output HIGH voltage | $V_{CC}$ − Min, $I_{OH}$ = − 1mA | 2.7 | 3.4 | | 2.4 | 3.4 | | V |
| $V_{OL}$ | Output LOW voltage | $V_{CC}$ = Min, $I_{OL}$ = 4mA | | | 0.4 | | | 0.4 | V |
| | | $I_{OL}$ = 20mA | | | 0.5 | | | 0.5 | V |
| $I_{OZH}$ | Output "off" current HIGH (3-state) | $V_{CC}$ = Max, $V_{OUT}$ = 2.4V | -50 | | 50 | -50 | | 50 | µA |
| $I_{OZL}$ | Output "off" current LOW (3-state) | $V_{CC}$ = Max, $V_{OUT}$ = 0.4V | -50 | | 50 | -50 | | 50 | µA |
| $I_{IH}$ | Input HIGH current | $V_{CC}$ = Max, $V_{IN}$ = 2.7V | | | 50 | | | 50 | µA |
| $I_I$ | Input HIGH current at Max. | $V_{CC}$ = Max, $V_{IN}$ = 5.5V | | | 1.0 | | | 1.0 | mA |
| $I_{IL}$ | Input LOW current | $V_{CC}$ = Max, $V_{IN}$ = 0.5V | | | -0.4 | | | -0.4 | mA |
| $I_{OS}$ | Output short circuit current | $V_{CC}$ = Max, $V_{OUT}$ = 0V | -25 | | -100 | -25 | | -100 | mA |

**NOTES**

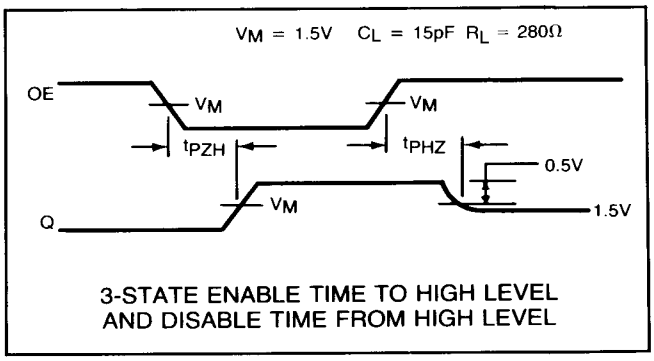
1 Typical limits are at 25°C, $V_{CC}$ = 5.0V

2a These input levels provide zero noise immunity and should only be tested in a static, noise-free environment

2b Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach $V_{IL}$ or $V_{IH}$ until the noise has settled. AMCC recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests

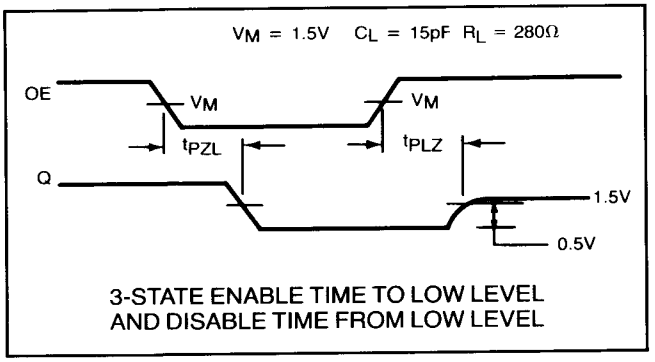
## AC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | | TEST CONDITIONS | COMM 0°/+75° | | | MIL -55°/+125° | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{IPD}$ | Input Propagation Delay Through Input Buffer | Standard | | | 2.8 | | | 2.8 | | ns |
| | | High Speed | | | 0.8 | | | 0.8 | | ns |
| $t_{OPD}$ | Output Propagation Delay | Standard | RL = 280Ω, CL = 15pF Load[2] | | 5 | | | 5 | | ns |
| | | High Speed | | | 3.8 | | | 3.8 | | ns |
| $t_{FPD}$[1] | Internal Equivalent Gate Delay | Standard | | | 0.5 | | | 0.5 | | ns |
| | | Low Power | | | 0.7 | | | 0.7 | | ns |
| | | High Speed | | | 0.35 | | | 0.35 | | ns |
| $F_{MAXT}$ | Max. Internal Flip-Flop Toggle Frequency | Standard | | | 250 | | | 250 | | MHz |
| | | Low Power | | | 200 | | | 200 | | MHz |
| | | High Speed | | | 400 | | | 400 | | MHz |
| $t_{PZH}$ | Enable time to high level | | Fig 8. 3 state output | | 9 | | | 9 | | ns |
| $t_{PZL}$ | Enable time to low level | | Fig 9. 3 state output | | 9 | | | 9 | | ns |
| $t_{PHZ}$ | Disable time from high level | | Fig 8. 3 state output | | 9 | | | 9 | | ns |
| $t_{PLZ}$ | Disable time from low level | | Fig 9. 3 state output | | 9 | | | 9 | | ns |
| $F_{IN}$[3] | Maximum input frequency at package pin | Standard | | | 120 | | | 120 | | MHz |
| | | High Speed | | | 160 | | | 160 | | MHz |



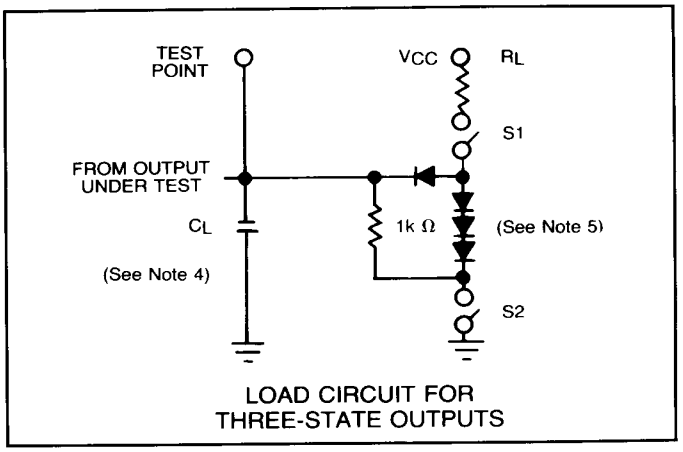

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL

FIGURE 8




3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL

FIGURE 9




LOAD CIRCUIT FOR THREE-STATE OUTPUTS

FIGURE 10

### TEST CIRCUIT SWITCH TABLE

| TEST FUNCTIONS | S1 | S2 |
|---|---|---|
| $tp_{ZH}$ | Open | Closed |
| $tp_{ZL}$ | Closed | Open |
| $tp_{HZ}$ | Closed | Closed |
| $tp_{LZ}$ | Closed | Closed |

**NOTES:**

1 Logic cell delays are for each gate level of a more complex logic function (i.e. D flip/flop, 4 to 1 mux, etc.)
2 Standard TTL load circuit used, see Figure 10 (S1 and S2 closed)
3 Package selection will determine the maximum input frequency. Consult AMCC
4 CL includes probe and jig capacitance
5 All diodes are 1N916 or 1N3064

# NOTES

REPRESENTED BY:

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