Upcoming Stratix V Device Features

This document lists the Stratix® V device family features that are not enabled in the Quartus® II software version 12.0. However, these features will be supported in a future release of the Quartus II software.

Table 1 lists the future support for Stratix V devices.

Table 1. Future Support for Stratix V Devices

Device Variant	Support
Stratix V E	The Stratix V E FPGAs will be supported in a future release of the Quartus II software.

Features of the Stratix V Device Family

Table 2 lists the configuration features that will be supported in a future version of the Quartus II software.

Table 2. Configuration Support for Stratix V Devices

Feature	Future Support
Partial reconfiguration	You will be able to partially reconfigure Stratix V devices while the rest of the device is still operating.
Configuration via Protocol (CvP)	Configuration via Protocol will allow you to configure the FPGA fabric via the PCI Express® (PCIe®) link using the designated PCIe Hard IP. Initialization mode using PCIe Gen2 will be supported in a future release of the Quartus II software.
Unique ID	Unique ID will allow each device to be uniquely identified. This feature requires an IP that will be supported in a future release of the Quartus II software.

Table 3 lists the FPGA fabric features that will be supported in a future version of the Quartus II software.

Table 3. FPGA Fabric Support for Stratix V Devices

Feature	Future Support
Single event upset (SEU) mitigation	The following SEU features will be supported in a future version of the Quartus II software: ■ Error classification ■ Scrubbing

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Table 4 lists the external memory features that will be supported in a future version of the Quartus II software.

Table 4. External Memory Support for Stratix V Devices

Feature	Future Support
DDR3	■ Final IP that enables DDR3 functionality up to 1,066 MHz. ■ Ping-pong PHY and controller ■ LRDIMM ■ 1-slot quad rank DIMM
RLDRAM III	PHY only

Table 5 lists the transceiver standard physical coding sublayer (PCS) features that will be supported in a future version of the Quartus II software.

Table 5. Transceiver Standard PCS Support for Stratix V Devices

Feature	Future Support
Protocols supported using standard PCS	The following transceiver protocol mode will be supported in a future release of the Quartus II software: ■ PCIe Gen1/Gen2/Gen3 x2 mode

Table 6 lists the transceiver 10G PCS features that will be supported in a future version of the Quartus II software.

Table 6. Transceiver 10G PCS Support for Stratix V Devices

Feature	Future Support
Protocols supported using 10G PCS	The following transceiver protocol mode using the transceiver 10G PCS will be supported in a future release of the Quartus II software: ■ 10GBASE-KR (full support)

Table 7 lists the transceiver clocking features that will be supported in a future version of the Quartus II software.

Table 7. Transceiver Clocking Support for Stratix V Devices (Part 1 of 2)

Feature	Future Support
Input reference clock sources	In addition to dedicated `refclk` pins, the following input reference clock sources will be enabled: ■ Dual-purpose receiver/`refclk` pins—receiver pins of **Transmit-only** or unused transceiver channels can be used for sourcing input reference clocks. They will support fewer I/O standards when compared with dedicated `refclk` pins.
Fractional PLL	The following fractional PLL features will be supported: ■ Ability to use fractional PLLs as transmit PLLs for transceivers ■ Cascading output counters to create counters larger than 512 ■ Dynamic phase shift

Table 7. Transceiver Clocking Support for Stratix V Devices (Part 2 of 2)

Feature	Future Support
PLL cascading	The following transceiver PLL cascading will be supported in the future: ■ Clock divider to fractional PLL cascade—to save clock sources in systems by using clocks generated by a transmit PLL in the FPGA fabric.
Multi-Channel Bonding	The following will be supported: ■ Side-wide bonding for configurations using standard PCS. Data rates will vary based on the number of channels bonded. The data rates will be determined after characterization. ■ Side-wide bonding for configurations using 10G PCS. Data rates will vary based on the number of channels bonded. The data rates will be determined after characterization.

Table 8 lists the transceiver PMA features that will be supported in a future version of the Quartus II software.

Table 8. Transceiver PMA Support for Stratix V Devices

Feature	Future Support
Signal detect and electrical idle	■ Electrical idle inference for PCIe Gen3
Built-in Self Test modes	The following patterns will be supported for Built-in Self Test mode: ■ PRBS 7 (Standard PCS, 10G PCS) ■ PRBS 8 (Standard PCS) ■ PRBS 9 (10G PCS) ■ PRBS 10 (Standard PCS, 10G PCS) ■ PRBS 23 (Standard PCS, 10G PCS) ■ PRBS 31 (10G PCS) ■ High Frequency (Standard PCS) ■ Low Frequency (Standard PCS)

Table 9 lists the signal conditioning features that will be supported in a future version of the Quartus II software.

Table 9. Signal Conditioning Features Support for Stratix V Devices

Feature	Future Support
Decision feedback equalization (DFE)	High-speed signals transmitted across a backplane experience signal attenuation due to skin effect, dielectric losses, and crosstalk. Stratix V devices will provide multi-tap DFE to primarily compensate the backplane attenuation due to crosstalk. DFE is effective in canceling post cursor inter-symbol interference (ISI) by boosting only the high frequency components of a signal without noise amplification. You can use DFE in conjunction with pre-emphasis, linear equalization (manual equalization), and AEQ.

Table 10 lists the transceiver dynamic reconfiguration features that will be supported in a future version of the Quartus II software.

Table 10. Transceiver Dynamic Reconfiguration Support for Stratix V Devices

Feature	Future Support
Dynamic reconfiguration	Future versions of the Quartus II software will support dynamic reconfiguration of the following transceiver features: ■ ATX PLL reconfiguration ■ EyeQ for GT channel
PCIe hard IP reconfiguration	Stratix V devices will support dynamic reconfiguration of the following in the PCIe hard IP: ■ Endpoint modes in PCIe Gen1/Gen2 ■ Rootport modes in PCIe Gen1/Gen2 ■ Runtime reconfiguration of PCIe read only registers ■ Runtime switching between endpoint and rootport modes

Document Revision History

Table 11 lists the revision history for this document.

Table 11. Document Revision History

Date	Version	Changes
June 2012	1.7	Updated for the Quartus II software 12.0 release.
March 2012	1.6	Updated Table 4.
November 2011	1.5	Updated for the Quartus II software 11.1 release.
July 2011	1.4	Updated for the Quartus II software 11.0 release.
December 2010	1.3	Updated document for the Quartus II software 10.1 release.
July 2010	1.2	Updated document for Quartus II software 10.0 release.
April 2010	1.1	Updated item 22 and 23 in Table 1.
April 2010	1.0	Initial release.