Stratix® V E, GS, and GX Device Family Pin Connection Guidelines
PCG-01011-1.4

These pin connection guidelines should only be used as a recommendation, not as a specification.
The use of the pin connection guidelines for any particular design should be verified for device operation, with the datasheet and Altera.

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Stratix V (transceiver-based device) Pin Name	Stratix V E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Clock and PLL Pins				
CLK[0:27]p	CLK[0:27]p	I/O, Clock Input	Dedicated high speed clock input pins that can also be used for data inputs/outputs. Differential input OCT Rd, single ended input OCT Rt and single ended output OCT Rs are supported on these pins.	Unused pins can be tied to GND or left unconnected. If unconnected, use the Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
CLK[0:27]n	CLK[0:27]n	I/O, Clock Input	Dedicated high speed clock input pins that can also be used for data inputs/outputs. Differential input OCT Rd, single ended input OCT Rt and single ended output OCT Rs are supported on these pins.	Unused pins can be tied to GND or left unconnected. If unconnected, use the Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
FPLL_[B,T][L,C,R]_FB/CLKOUTp	FPLL_[B,T][L,C,R]_FB/CLKOUTp	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
FPLL_[B,T][L,C,R]_FB/CLKOUTn	FPLL_[B,T][L,C,R]_FB/CLKOUTn	I/O, Clock		These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
FPLL_[B,T][L,C,R]_CLKOUTp	FPLL_[B,T][L,C,R]_CLKOUTp	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
FPLL_[B,T][L,C,R]_CLKOUTn	FPLL_[B,T][L,C,R]_CLKOUTn	I/O, Clock		These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
Dedicated Configuration/JTAG Pins				
nIO_PULLUP	nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (DATA[0:31], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high turns off the weak pull-up, while a logic low turns them on.	The nIO-PULLUP can be tied directly to VCCPGM, use a 1 kΩ pull-up resistor or tied directly to GND depending on the use desired for the device. This pin has an internal 5-kΩ pull-down.
TEMPDIODEp	TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the FPGA.	If the temperature sensing diode is not used with an external temperture sensing device then connect this pin to GND. When connecting the TEMPDIODE pins to an external temperture sense device refer to the "Power Management in Stratix V Devices" chapter in the Stratix V Handbook.
TEMPDIODEn	TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the FPGA.	If the temperature sensing diode is not used with an external temperture sensing device then connect this pin to GND. When connecting the TEMPDIODE pins to an external temperture sense device refer to the "Power Management in Stratix V Devices" chapter in the Stratix V Handbook.
MSEL[0:4]	MSEL[0:4]	Input	Configuration input pins that set the FPGA device configuration scheme.	These pins are internally connected through a 25-kΩ resistor to GND. Do not leave these pins floating. When these pins are unused connect them to GND. Depending on the configuration scheme used these pins should be tied to VCCPGM or GND. Refer to the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter in the Stratix V Handbook for the configuration scheme options. If only JTAG configuration is used, connect these pins to ground.

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nCE	nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.	In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration and JTAG programming, nCE should be connected to GND.
nCONFIG	nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.	nCONFIG should be connected directly to the configuration controller when the FPGA uses a passive configuration scheme, or through a 10-kΩ resistor tied to VCCPGM when using an active serial configuration scheme. If this pin is not used, it requires a connection directly or through a 10-kΩ resistor to VCCPGM.
CONF_DONE	CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.	If internal pull-up resistors on the configuration controller or enhanced configuration device are used, external 10-kΩ pull-up resistors should not be used on this pin. Otherwise an external 10-kΩ pull-up resistor to VCCPGM should be used. When using passive configuration schemes this pin should also be monitored by the configuration controller.
nCEO	nCEO	I/O, Output (open-drain)	Output that drives low when device configuration is complete. If this pin is not enabled for use as a configuration pin, it can be used as a user I/O pin.	During multi-device configuration, this pin feeds the nCE pin of a subsequent device. Connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. During single device configuration, this pin may be left floating.
nSTATUS	nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.	The OE and nCE pins of the enhanced configuration devices have optional internal programmable pull-up resistors. If internal pull-up resistors on the enhanced configuration device are used, external 10-kΩ pull-up should not be used on these pins. Otherwise, an external 10-KΩ pull-up resistors to VCCPGM should be used. When using Passive configuration schemes this pin should also be monitored by the configuration controller.
TCK	TCK	Input	Dedicated JTAG test clock input pin.	Connect this pin to a 1-kΩ pull-down resistor to GND. This pin has an internal 25-kΩ pull-down.
TMS	TMS	Input	Dedicated JTAG test mode select input pin.	Connect this pin to a 1-kΩ - 10-kΩ pull-up resistor to VCCPD. To disable the JTAG circuitry connect TMS to VCCPD via a 1-kΩ resistor. This pin has an internal 25-kΩ pull-up.

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Stratix V (transceiver-based device) Pin Name	Stratix V E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
TDI	TDI	Input	Dedicated JTAG test data input pin.	Connect this pin to a 1-kΩ - 10-kΩ pull-up resistor to VCCPD. To disable the JTAG circuitry connect TDI to VCCPD via a 1-kΩ resistor. This pin has an internal 25-kΩ pull-up.
TDO	TDO	Output	Dedicated JTAG test data output pin.	The JTAG circuitry can be disabled by leaving TDO unconnected. In cases where TDO uses VCCPD = 2.5 V to drive a 3.3 VJTAG interface, there may be leakage current in the TDI input buffer of the interfacing devices. An external pull-up resistor tied to 3.3 V on their TDI pin may be used to eliminate the leakage current if needed.
TRST	TRST	Input	Dedicated active low JTAG test reset input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.	Utilization of TRST is optional. When using this pin ensure that TMS is held high or TCK is static when TRST is changed from low to high. If not using TRST, tie this pin to a 1-kΩ pull-up resistor to VCCPD. To disable the JTAG circuitry, tie this pin to GND. This pin has an internal 25-kΩ pull-up.
Optional/Dual-Purpose Configuration Pins				
nCSO	nCSO	Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.	When not programming the device in AS mode nCSO is not used. Also, when this pin is not used as an output then it is recommended to leave the pin unconnected.
DCLK	DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.	Do not leave this pin floating. Drive this pin either high or low.
CRC_ERROR	CRC_ERROR	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.	When using as optionally open-drain output dedicated CRC_ERROR pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When not using as the dedicated CRC_ERROR optionally open-drain output, and when this pin is not used as an I/O pin, then connect this pin as defined in the Quartus II software.
DEV_CLRn	DEV_CLRn	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high (VCCPGM), all registers behave as programmed.	When the dedicated input DEV_CLRn is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground.
DEV_OE	DEV_OE	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high (VCCPGM), all I/O pins behave as defined in the design.	When the dedicated input DEV_OE is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground.
DATA0	DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for PS or FPP configuration or as an I/O pin after configuration is complete.	When the dedicated input for DATA[0] is not used and this pin is not used as an I/O then it is recommended to leave this pin unconnected.

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Stratix V (transceiver-based device) Pin Name	Stratix V E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
DATA[1:31]	DATA[1:31]	I/O, Input	Dual-purpose configuration input data pins. Use DATA [1:7] pins for FPP x8, DATA [1:15] pins for FPP x16, and DATA [1:31] pins for FPP x32 configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.	When the dedicated inputs for DATA[1:31] are not used and these pins are not used as an I/O then it is recommended to leave these pins unconnected.
INIT_DONE	INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.	When using as optionally open-drain output dedicated INIT_DONE pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When using in an AS or PS multi-device configuration mode ensure that the INIT_DONE pin is enabled in the Quartus II designs. When not using as the dedicated INIT_DONE optionally open-drain output, and when this pin is not used as an I/O pin, then connect this pin as defined in the Quartus II software.
CLKUSR	CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.	If the CLKUSR pin is not used as a configuration clock input and the pin is not used as an I/O then it is recommended to connect this pin to ground.
nPERST[L,R][0:1]	NA	I/O, Input	Dedicated Fundamental Reset pin is only available when used in conjunction with PCIe HIP. When low the transcievers are in reset. When high the transceivers are out of reset. When this pin is not used as the fundamental reset, this pin may be used as a user I/O.	Connect this pin as defined in the Quartus II software. This pin may be driven by 3.3V regardless of the VCCIO voltage level of the bank without a level translator as long as the input signal meets the LVTTL VIH/VIL specification, and as long as it meets the overshoot specifications for 100% operation as defined in Table 1-2 in the "DC and Switching Characteristics for Stratix V Devices." chapter of the Stratix V handbook. Only one nPERST pin is used per PCIe HIP. The Stratix V components always have all four pins listed, even when the specific component might only have 1 or 2 PCIe HIPs. nPERSTL0 = Bottom Left PCIe HIP & CvP, nPERSTL1 = Top Left PCIe HIP (When available), nPERSTR0 = Bottom Right PCIe HIP (When available), nPERSTR1 = Top Right PCIe HIP (When available), For maximum compatibility we recommend that the bottom left PCIe Hard IP always be used first, as this is the only location that supports CvP (Configuration via Protocol - Over the PCIe link). Assuming you are using the bottom left location, then simply connect nPERST from your PCIe slot directly to nPERSTL0.
External Memory Interface Pins				
AS_DATA0 / ASDO	AS_DATA0 / ASDO	Bidirectional	Dedicated AS configuration pin. When using an EPCS device (x1 mode) this is the ASDO pin and used to send address and control signals between the FPGA and the EPCS/EPCQ.	When not programming the device in AS mode ASDO is not used. Also, when this pin is not used it is recommended to leave the pin unconnected.
AS_DATA[1:3]	AS_DATA[1:3]	Bidirectional	Dedicated AS configuration data pins. Configuration data is transported on these pins when connected to the EPCQ devices.	When this pin is not used it is recommended to leave the pin unconnected.

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Partial Reconfiguration Pins				
PR_REQUEST	PR_REQUEST	I/O, Input	Partial Reconfiguration Request pin. Drive this pin high to start partial reconfiguration. Drive this pin low to end reconfiguration. This pin can only be used in Partial Reconfiguration using external host mode in FPP x16 configuration scheme.	When the dedicated input PR_REQUEST is not used and this pin is not used as an I/O, then it is recommended to tie this pin to GND.
PR_READY	PR_READY	I/O, Output or Output (open-drain)	The partial reconfiguration ready pin is driven low until the device is ready to begin partial reconfiguration. When the device is ready to start reconfiguration, this signal is released and is pulled high by an external pull-up resistor.	When using as optionally open-drain output dedicated PR_READY pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When not using as the dedicated PR_READY optionally open-drain output, and when this pin is not used as an I/O pin, then connect this pin as defined in the Quartus II software.
PR_ERROR	PR_ERROR	I/O, Output or Output (open-drain)	The partial reconfiguration error pin is driven low during partial reconfiguration unless the device detects an error. If an error is detected, this signal is released and pulled high by an external pull-up resistor.	When using as optionally open-drain output dedicated PR_ERROR pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When not using as the dedicated PR_ERROR optionally open-drain output, and when this pin is not used as an I/O pin, then connect this pin as defined in the Quartus II software.
PR_DONE	PR_DONE	I/O, Output or Output (open-drain)	The partial reconfiguration done pin is driven low until the partial reconfiguration is complete. When the reconfiguration is complete, this signal is released and is pulled high by an external pull-up resistor.	When using as optionally open-drain output dedicated PR_DONE pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When not using as the dedicated PR_DONE optionally open-drain output, and when this pin is not used as an I/O pin, then connect this pin as defined in the Quartus II software.
CvP_CONFDONE	NA	I/O, Output (open-drain)	Configuration Via Protocol Done pin is driven low during configuration. When configuration via PCIe is complete, this signal is released and is pulled high by an external pull-up resistor. Status of this pin is only valid if CONF_DONE is high.	When using as optionally open-drain output dedicated CvP_CONFDONE pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When not using as the dedicated CvP_CONFDONE optionally open-drain output, and when this pin is not used as an I/O pin, then connect this pin as defined in the Quartus II software.
Differential I/O Pins				
DIFFIO_RX_[T,B,L,R][#:#]p, DIFFIO_RX_[T,B.L,R][#:#]n	DIFFIO_RX_[T,B,L,R][#:#]p, DIFFIO_RX_[T,B.L,R][#:#]n	I/O, RX channel	These are true LVDS receiver channels on row and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in Quartus II software.

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DIFFIO_TX_[T,B,L,R][#:#]p, DIFFIO_TX_[T,B,L,R][#:#]n	DIFFIO_TX_[T,B,L,R][#:#]p, DIFFIO_TX_[T,B,L,R][#:#]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in Quartus II software.
DIFFOUT_[T,B,L,R][##]p, DIFFOUT_[T,B,L,R][##]n	DIFFOUT_[T,B,L,R][##]p, DIFFOUT_[T,B,L,R][##]n	I/O, TX channel	These are emulated LVDS output channels. All user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in Quartus II software.
External Memory Interface Pins				
DQS[1:70][T,B], DQS[1:70][L,R]	DQS[1:70][T,B], DQS[1:70][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.	Connect unused pins as defined in Quartus II software.
DQSn[1:70][T,B], DQSn[1:70][L,R]	DQSn[1:70][T,B], DQSn[1:70][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	Connect unused pins as defined in Quartus II software.
DQ[1:70][T,B], DQ[1:70][L,R]	DQ[1:70][T,B], DQ[1:70][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	Connect unused pins as defined in Quartus II software.
CQ[1:35][T,B], CQ[1:35][L,R]	CQ[1:35][T,B], CQ[1:35][L,R]	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.	Connect unused pins as defined in Quartus II software.

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CQn[1:35][T,B], CQn[1:35][L,R]	CQn[1:35][T,B], CQn[1:35][L,R]	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.	Connect unused pins as defined in Quartus II software.
Reference Pins				
RZQ_[#]	RZQ_[#]	I/O, Input	Reference pins for I/O banks. The RZQ pins share the same VCCIO with the I/O bank where they are located. The external precision resistor must be connected to the designated pin within the bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O it is recommended that the pin be connected to GND. When using OCT tie these pins to GND through either a 240Ω or 100Ω resistor, depending on the desired OCT impedence. Refer to the Stratix V handbook for the OCT impedence options for the desired OCT scheme.
DNU	DNU	Do Not Use	Do Not Use (DNU).	Do not connect to power, ground or any other signal. These pins must be left floating.
NC	NC	No Connect	Do not drive signals into these pins.	When designing for device migration these pins may be connected to power, ground, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern leave these pins floating.
Supply Pins ***(See Notes 4 through 7)***				
VCC	VCC	Power	VCC supplies power to the core and periphery.	VCC is either 0.85V or 0.9V depending on the core speed grade of the device. -1 and -2 core speed grade use 0.9V, -3 and -4 core speed grade use 0.85V. Connect all VCC pins to a low noise switching regulator. When VCCHIP and VCCHSSI are used, these pins must be tied to the same plane as VCC. For data rates less than 6.5 Gbps and with a proper isolation filter VCCR_GXB and VCCT_GXB may be sourced from the same regulator as VCC when the power rails require the same voltage level. Use the Stratix V Early Power Estimator to determine the current requirements for VCC and other power supplies. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3 and 6.
VCCD_FPLL	VCCD_FPLL	Power	PLL Digital power.	Connect all VCCD_FPLL pins -to a 1.5V linear or low noise switching power supply. These pins may be tied to the same regulator as VCCPT, VCCBAT, and VCCH_GXB. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2 and 3.
VCCPT	VCCPT	Power	Power supply for the programmable power technology.	Connect all VCCPT pins to a 1.5V linear or low noise switching power supply. These pins may be tied to the same regulator as VCCD_FPLL, VCCBAT and VCCH_GXB. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4 and 7.
VCCA_FPLL	VCCA_FPLL	Power	PLL Analog power.	Connect these pins to a 2.5V low noise switching power supply through a proper isolation filter. This power rail may be shared with VCC_AUX. With a proper isolation filter these pins may be sourced from the same regulator as VCCIO, VCCPD and VCCPGM when each of these power supplies require 2.5V. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 7.
VCC_AUX	VCC_AUX	Power	Auxiliary supply for the programmable power technology.	Connect all VCC_AUX pins to a 2.5V low noise switching power supply through a proper isolation filter. This power rail may be shared with VCCA_FPLL. With a proper isolation filter these pins may be sourced from the same regulator as VCCIO, VCCPD and VCCPGM when each of these power supplies require 2.5V. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 7.
VCCIO[1:8]	VCCIO[1:8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. supported VCCIO standards include LVDS, LVCMOS(3.0V), HSTL(12, 15, 18), SSTL(12, 125, 135, 15, 18, 2), LVTTL (3.0V), HSUL(12), LVPECL(2.5V),1.2V, 1.5V, 1.8V, 2.5V I/O standards.	Connect these pins to 1.2V, 1.25V, 1.35V, 1.5V, 1.8V, 2.5V or 3.0V supplies, depending on the I/O standard connected to the specified bank. When these pins require the same voltage level as VCCPD and/or VCCPGM, they may be tied to the same regulator as VCCPD and/or VCCPGM, but only if each of these supplies requires the same voltage level. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3 and 8.
VCCPGM	VCCPGM	Power	Configuration pins power supply.	Connect these pins to either 1.8V, 2.5V or 3.0V power supply. When these pins require the same voltage level as VCCPD and/or VCCIO, they may be tied to the same regulator as VCCPD and/or VCCIO, but only if each of these supplies requires the same voltage level. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2 and 3.

Stratix® V E, GS, and GX Device Family Pin Connection Guidelines
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Altera recommends that you create a Quartus® II design, enter your device I/O assignments, and compile the design. The Quartus II software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Stratix V (transceiver-based device) Pin Name	Stratix V E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VCCPD[1:8]	VCCPD[1:8]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers. This can be connected to 2.5V or 3.0V. For 1.2V, 1.25V, 1.35V, 1.5V, 1.8V or 2.5V I/O standards connect VCCPD to 2.5V and for 3.0V I/O standard connect VCCPD to 3.0V.	The VCCPD pins require 2.5V or 3.0V. When these pins require the same voltage level as VCCPGM and/or VCCIO, they may be tied to the same regulator as VCCPGM and/or VCCIO, but only if each of these supplies requires the same voltage level. The voltage on these pins must be equal to or greater than VCCIO of the respective banks. For instance if VCCIO is 3.0V then VCCPD must be 3.0V. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3 and 8.
VCCBAT	VCCBAT	Power	Battery back-up power supply for design security volatile key register.	Connect this pin to a Non-volatile battery power source in the range of 1.2V - 3.0V when using design security volatile key. In this case, do not connect this pin to a volatile power source on the board. 3.0V is the typical battery power selected for this supply. When not using the volatile key, tie this to a 1.5V, 2.5V or 3.0V supply. Stratix V devices will not exit POR if VCCBAT stays at logic low.
GND	GND	Ground	Device ground pins.	All GND pins should be connected to the board ground plane.
VREF[1:8]N0	VREF[1:8]N0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.	If VREF pins are not used, designers should connect them to either the VCCIO in the bank in which the pin resides or GND. Decoupling depends on the design decoupling requirements of the specific board. See Note 2 and 8.
Transceiver Pins ***(See Notes 4 through 10)***				
VCCHIP_[L,R]	NA	Power	PCIe Hard IP digital power supply, specific to the left (L) side or right (R) side of the device..	VCCHIP is either 0.85V or 0.9V depending on the core speed grade of the device. -1 and -2 core speed grade use 0.9V, -3 and -4 core speed grade use 0.85V. When VCCHIP is used, it must be tied to the same plane as VCC. When not using any of the HIPs on one side of the device, VCCHIP pins on that side of the device may be connected to GND. For data rates less than 6.5Gbps and with a proper isolation filter VCCR_GXB and VCCT_GXB may be sourced from the same regulator as VCC, VCCHIP and VCCHSSI. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, and 3.
VCCHSSI_[L,R]	NA	Power	PCS power supply, specific to the left (L) side or right (R) side of the device.	VCCHSSI is either 0.85V or 0.9V depending on the core speed grade of the device. -1 and -2 core speed grade use 0.9V, -3 and -4 core speed grade use 0.85V. When VCCHSSI is used, it must be tied to the same plane as VCC. When not using any of the transceivers on one side of the device, VCCHSSI on that side of the device may be tied to GND. For data rates less than 6.5Gbps and with a proper isolation filter VCCR_GXB and VCCT_GXB may be sourced from the same regulator as VCC, VCCHIP and VCCHSSI. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2 and 3.
VCCR_GXB[L,R][0:3]	NA	Power	Analog power, receiver, specific to the left (L) side or right (R) side of the device.	Connect VCCR_GXB pins to a linear or low noise switching regulator. VCCR_GXB and VCCT_GXB are either set to 1.0V, or are set to match the VCC of the device. If the ATX PLL is being used, the CMU data rate is > 6.5Gbps, or you are using any of DFE/AEQ/EyeQ, or you want to make provision to use any of these capabilities in the future, then you must set VCCR_GXB and VCCT_GXB to 1.0V. If you are not using any of the above features, and you don't want to make any provision to use them in the future, then you can set VCCR_GXB and VCCT_GXB to the same level as VCC, or you can set them to 1.0V, it's your choice. Note that the choice you make for VCCR_GXB and VCCT_GXB must track the choice you make for VCCA_GXB. The allowable combinations are: VCCR_GXB/VCCT_GXB = VCC and VCCA_GXB = 2.5V, or VCCR_GXB/VCCT_GXB = 1.0V and VCCA_GXB = 3.0V. For data rates less than 6.5Gbps and ATX PLL, DFE, AEQ, or EyeQ is not used, these pins may be tied to the same regulator as VCC, VCCHIP and VCCHSSI with a proper isolation filter. For data rates less than 12.5Gbps these pins may share the same power rail as VCCT_GXB. However, for better performance VCCR_GXB and VCCT_GXB should be isolated by at least 60dB for a 1MHz to 100MHz bandwidth. For data rates greater than 12.5Gbps this power rail must be tied to its own power regulator. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 2, 3, 4, 7 and 10.

Altera recommends that you create a Quartus® II design, enter your device I/O assignments, and compile the design. The Quartus II software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Stratix V (transceiver-based device) Pin Name	Stratix V E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VCCT_GXB[L,R][0:3]	NA	Power	Analog power, transmitter, specific to the left (L) side or right (R) side of the device.	Connect VCCT_GXB pins to a linear or low noise switching regulator. VCCR_GXB and VCCT_GXB are either set to 1.0V, or are set to match the VCC of the device. If the ATX PLL is being used, the CMU data rate is > 6.5Gbps, or you are using any of DFE/AEQ/EyeQ, or you want to make provision to use any of these capabilities in the future, then you must set VCCR_GXB and VCCT_GXB to 1.0V. If you are not using any of the above features, and you don't want to make any provision to use them in the future, then you can set VCCR_GXB and VCCT_GXB to the same level as VCC, or you can set them to 1.0V, it's your choice. Note that the choice you make for VCCR_GXB and VCCT_GXB must track the choice you make for VCCA_GXB. The allowable combinations are: VCCR_GXB/VCCT_GXB = VCC and VCCA_GXB = 2.5V, or VCCR_GXB/VCCT_GXB = 1.0V and VCCA_GXB = 3.0V. For data rates less than 6.5Gbps and ATX PLL, DFE, AEQ, or EyeQ is not used, these pins may be tied to the same regulator as VCC, VCCHIP and VCCHSSI with a proper isolation filter. For data rates less than 12.5Gbps these pins may share the same power rail as VCCR_GXB. However, for better performance VCCR_GXB and VCCT_GXB should be isolated by at least 60dB for a 1MHz to 100MHz bandwidth. For data rates greater than 12.5Gbps this power rail must be tied to its own power regulator. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 2, 3, 4, 7 and 10.
VCCH_GXB[L,R][0:3]	NA	Power	Analog power, block level TX buffers.	Connect VCCH_GXB to a 1.5V linear or low noise switching regulator. These pins may be sourced from the same regulator as VCCPT, VCCD_FPLL and VCCBAT. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 2, 3, 4, 7 and 10.
VCCA_GXB[L,R][0:3]	NA	Power	Analog power, TX driver, RX receiver, CDR, specific to the left (L) side or right (R) side of the device.	Use a linear or low noise switching regulator to supply power to this power plane. VCCA_GXB is either set to 2.5V or 3.0V. If the ATX PLL is being used, the CMU data rate is > 6.5Gbps, or you are using any of DFE/AEQ/EyeQ, or you want to make provision to use any of these capabilities in the future, then you must set VCCA_GXB to 3.0V. If you are not using any of the above features, and you don't want to make any provision to use them in the future, then you can set VCCA_GXB to 2.5V or 3.0V, it's your choice. Note that the choice you make for VCCA_GXB must track the choice you make for VCCR_GXB and VCCT_GXB. The allowable combinations are: VCCR_GXB/VCCT_GXB = VCC and VCCA_GXB = 2.5V, or VCCR_GXB/VCCT_GXB = 1.0V and VCCA_GXB = 3.0V. This power rail may be shared with VCCA_FPLL and VCC_AUX. With a proper isolation filter these pins may be sourced from the same regulator as VCCIO, VCCPD and VCCPGM when each of these power supplies require 2.5V. Decoupling depends on the design decoupling requirements of the specific board design. See Notes 2, 3, 7 and 10.
GXB_RX_[L,R][0:32]p	NA	Input	High speed positive differential receiver channels. Specific to the left (L) side or right (R) side of the device.	These pins may be AC-coupled or DC-coupled when used. Connect all unused GXB_RXp pins directly to GND or VCCR_GXB or VCCT_GXB. For more information about pin connection guidelines for Stratix V GX board designs that are intended to migrate to the Stratix V GT device, refer to AN644: Migration Between Stratix V GX and Stratix V GT Devices. See Note 9.
GXB_RX_[L,R][0:32]n	NA	Input	High speed negative differential receiver channels. Specific to the left (L) side or right (R) side of the device.	These pins may be AC-coupled or DC-coupled when used. Connect all unused GXB_RXn pins directly to GND. For more information about pin connection guidelines for Stratix V GX board designs that are intended to migrate to the Stratix V GT device, refer to AN644: Migration Between Stratix V GX and Stratix V GT Devices. See Note 9.
GXB_TX_[L,R][0:32]p	NA	Output	High speed positive differential transmitter channels. Specific to the left (L) side or right (R) side of the device.	Leave all unused GXB_TXp pins floating.
GXB_TX_[L,R][0:32]n	NA	Output	High speed negative differential transmitter channels. Specific to the left (L) side or right (R) side of the device.	Leave all unused GXB_TXn pins floating.
REFCLK_[L,R][0:9]p	NA	Input	High speed differential reference clock positive receiver channels, specific to the left (L) side or right (R) side of the device.	These pins should be AC-coupled . Connect all unused pins either individually to GND through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Note 9.

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Altera recommends that you create a Quartus® II design, enter your device I/O assignments, and compile the design. The Quartus II software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Stratix V (transceiver-based device) Pin Name	Stratix V E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
REFCLK_[L,R][0:9]n	NA	Input	High speed differential reference clock complement, complementary receiver channel, specific to the left (L) side or right (R) side of the device.	These pins should be AC-coupled . Connect all unused pins either individually to GND through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Note 9.
RREF_[T,B][L,R]	NA	Input	Reference resistor for transceiver, specific to the left (L) side or right (R) side of the device.	If any REFCLK pin or transceiver channel on one side (left or right) of the device is used, you must connect each RREF pin on that side of the device to its own individual 1.8kΩ +/- 1% resistor to GND. Otherwise, you may connect each RREF pin on that side of the device directly to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.

Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1) This pin connection guidelines is created based on the Stratix V device family. Shaded cells indicate pin name differences between the Stratix V (transceiver-based devices) and Stratix V E devices.
2) Capacitance values for the power supply should be selected after consideration of the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage droop requirements of the device/supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling.

3) Use the Stratix V Early Power Estimator to determine the current requirements for VCC and other power supplies.
4) These supplies may share power planes across multiple Stratix V devices.
5) Examples 1 - 4 and Figures 1 - 4 illustrate power supply sharing guidelines that are data rate dependent. Example 5 and Figure 5 illustrate the power supply sharing guidelines for the Stratix V E.
Example 1 and Figure 1, "Power Regs <= 6.5Gbps", show recommendations for designs using the Stratix V transceviers that will not exceed 6.5Gbps option 1.
Example 2 and Figure 2, "Power Regs <= 6.5Gbps", show recommendations for designs using the Stratix V transceviers that will not exceed 6.5Gbps option 2.
Example 3 and Figure 3, "Power Regs > 6.5Gbps <= 12.5Gbps", show recommendations for designs using the Stratix V transceviers that are between 6.5Gbps and 12.5Gbps.
Example 4 and Figure 4, "Power Regs >12.5Gbps", show recommendations for designs using the Stratix V transceviers with data rates greater than 12.5Gbps.
Example 5 and Figure 5, "Power Regs Stratix V E", show recommendations for designs that use the non-transceiver based Stratix V E.
6) Power pins should not share breakout vias from the BGA. Each ball on the BGA needs to have its own dedicated breakout via. VCC must not share breakout vias.
7) Low Noise Switching Regulator - defined as a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800kHz and 1MHz and has fast transient response.
Line Regulation < 0.4%
Load Regulation < 1.2%
8) The number of modular I/O banks on Stratix V devices depends on the device density. For the indexes available for a specific device, please refer to the I/O Bank section in the Stratix V device handbook.
9) For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
10) If none of the transceivers within a bank are used then the transceiver power pins within that bank may be tied to GND. These pins include VCCR_GXB, VCCT_GXB, VCCH_GXB, and VCCA_GXB.

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Example 1. Power Supply Sharing Guidelines for Stratix V Transceivers with Data Rates <= 6.5Gbps, and all of the following conditions are true:
ATX PLL is not being used, DFE/AEQ/EyeQ are not being used, and no provision is being made to use any of these features in the future (Option 1)

Example Requiring 3 Power Regulators

Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC VCCHIP_[L,R] VCCHSSI_[L,R]	1	0.85 or 0.9 (**)	± 30mV	Switcher (*)	Share	VCC, VCCHIP and VCCHSSI must share regulators. If not using HIP, VCCHIP may be tied to GND. Also, when not using any of the transceivers on one side of the device, VCCHSSI on that side of the device may be tied to GND.
VCCR_GXB[L,R] VCCT_GXB[L,R]					Isolate	May be able to share VCCR_GXB and VCCT_GXB with VCC, VCCHIP and VCCHSSI with a proper isolation filter.
VCCIO VCCPD VCCPGM	2	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require as many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCC_AUX VCCA_GXB[L,R] VCCA_FPLL		2.5			Isolate	May be able to share VCCA_GXB, VCC_AUX and VCCA_FPLL with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Stratix V devices.
VCCPT VCCH_GXB[L,R] VCCD_FPLL VCCBAT	3	1.5	± 50mV	Linear or Switcher (*)	Share	If not sharing a regulator, the VCCPT supply should not exceed a tolerance of ± 50mV, however the other power supplies in this group can tolerate ± 5%. Depending on the regulator capabilities this supply may be shared with multiple Stratix V devices.

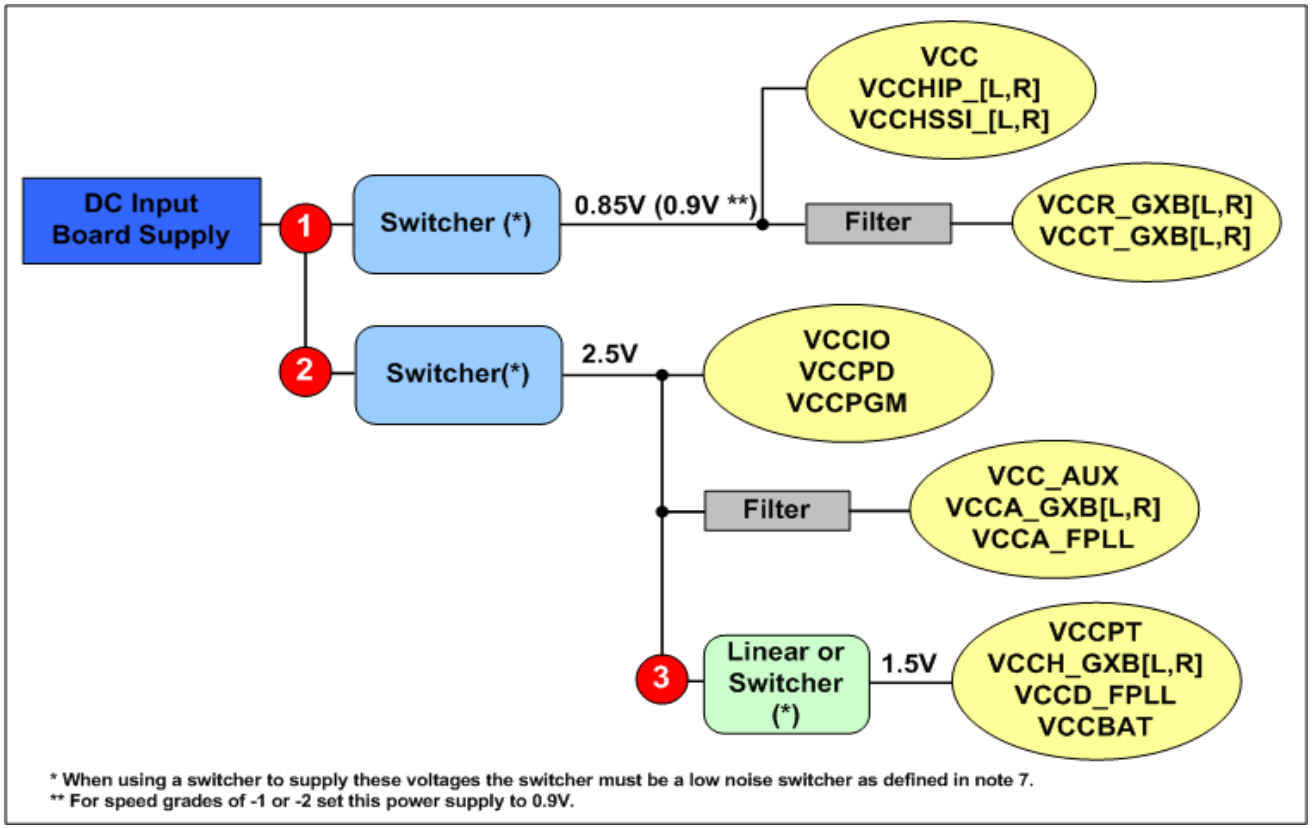
(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.

(**) If you are using a -1 or -2 core speed grade, you must connect the core VCC to 0.9V.

Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Stratix V transceiver-based device with data rates less than or equal to 6.5Gbps is provided in Figure 1.

Figure 1. Example Power Supply Block Diagram for Stratix V Transceivers with Data Rates <= 6.5Gbps, and all of the following conditions are true: ATX PLL is not being used, DFE/AEQ/EyeQ are not being used, and no provision is being made to use any of these features in the future (Option 1)



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Example 2. Power Supply Sharing Guidelines for Stratix V Transceivers with Data Rates <= 6.5Gbps, and at least one of the following conditions is true: ATX PLL is being used, DFE/AEQ/EyeQ are being used, or provision is being made to use any of these features in the future (Option 2)

Example Requiring 5 Power Regulators

Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC VCCHIP_[L,R] VCCHSSI_[L,R]	1	0.85 or 0.9 (**)	± 30mV	Switcher (*)	Share	VCC, VCCHIP and VCCHSSI must share regulators. If not using HIP, VCCHIP may be tied to GND. Also, when not using any of the transceivers on one side of the device, VCCHSSI on that side of the device may be tied to GND.
VCCR_GXB[L,R] VCCT_GXB[L,R]	2	1.0	± 30mV	Linear or Switcher (*)	Isolate	
VCCIO VCCPD VCCPGM	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require as many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCC_AUX VCCA_FPLL		2.5				May be able to share VCC_AUX and VCCA_FPLL with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Stratix V devices.
VCCA_GXB[L,R]	4	3.0	± 5%	Linear or Switcher (*)	Isolate	
VCCPT VCCH_GXB[L,R] VCCD_FPLL VCCBAT	5	1.5	± 50mV	Linear or Switcher (*)	Share	If not sharing a regulator, the VCCPT supply should not exceed a tolerance of ± 50mV, however the other power supplies in this group can tolerate ± 5%. Depending on the regulator capabilities this supply may be shared with multiple Stratix V devices.

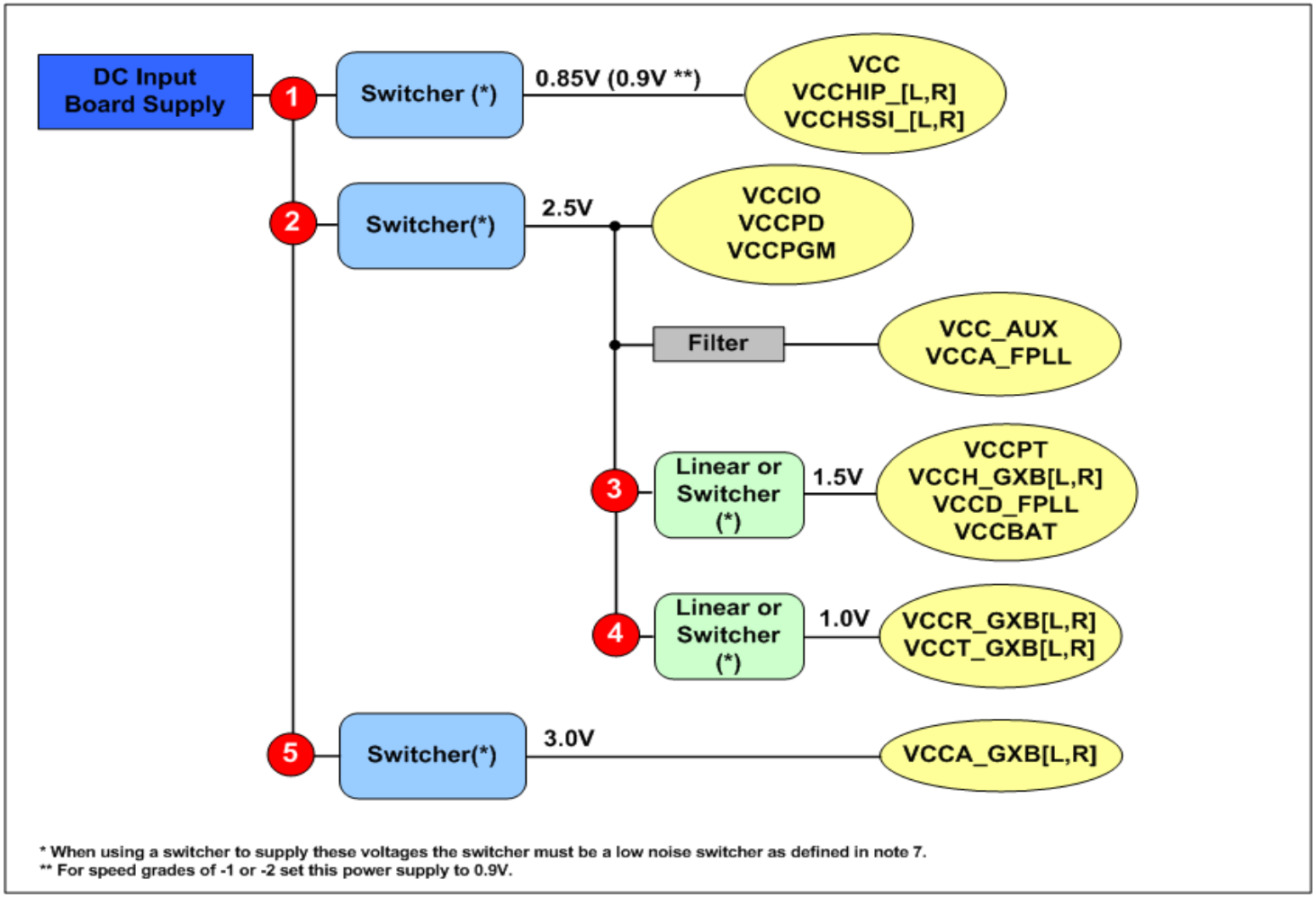
(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.

(**) If you are using a -1 or -2 core speed grade, you must connect the core VCC to 0.9V.

Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Stratix V transceiver-based device with data rates less than or equal to 6.5Gbps is provided in Figure 2.

Figure 2. Example Power Supply Block Diagram for Stratix V Transceivers with Data Rates <= 6.5Gbps, and at least one of the following conditions is true: ATX PLL is being used, DFE/AEQ/EyeQ are being used, or provision is being made to use any of these features in the future (Option 2)



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Example 3. Power Supply Sharing Guidelines for Stratix V Transceivers with Data Rates Between 6.5Gbps and 12.5Gbps

Example Requiring 5 Power Regulators

Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC VCCHIP_[L,R] VCCHSSI_[L,R]	1	0.85 or 0.9 (**)	± 30mV	Switcher (*)	Share	VCC, VCCHIP and VCCHSSI must share regulators. If not using HIP, VCCHIP may be tied to GND. Also, when not using any of the transceivers on one side of the device, VCCHSSI on that side of the device may be tied to GND.
VCCIO VCCPD VCCPGM	2	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require as many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCC_AUX VCCA_FPLL		2.5			Isolate	May be able to share VCC_AUX and VCCA_FPLL with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Stratix V devices.
VCCR_GXB[L,R] VCCT_GXB[L,R]	3	1.0	± 30mV	Linear or Switcher (*)	Share	Although VCCR_GXB and VCCT_GXB may share a regulator, for better performance and in order to meet PCIe Gen. 3 jitter specifications these power supplies should be isolated from each other with at least 60dB of isolation for a 1MHz to 100MHz bandwidth.
VCCPT VCCH_GXB[L,R] VCCD_FPLL VCCBAT	4	1.5	± 50mV	Linear or Switcher (*)	Share	If not sharing a regulator, the VCCPT supply should not exceed a tolerance of ± 50mV, however the other power supplies in this group can tolerate ± 5%. Depending on the regulator capabilities this supply may be shared with multiple Stratix V devices.
VCCA_GXB[L,R]	5	3.0	± 5%	Linear or Switcher (*)	Isolate	

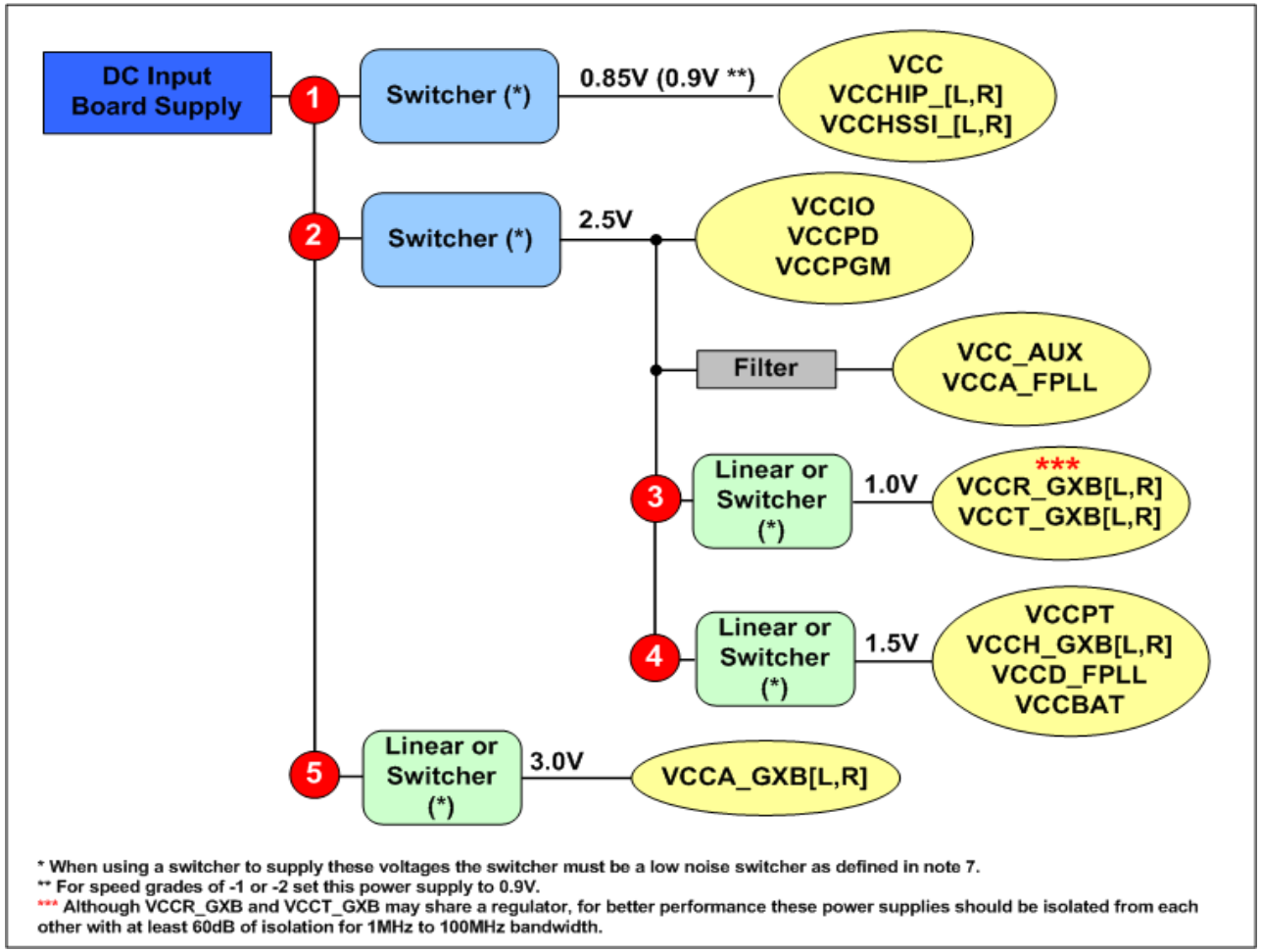
(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.

(**) If you are using a -1 or -2 core speed grade, you must connect the core VCC to 0.9V.

Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Stratix V transceiver-based device with data rates between 6.5Gbps and 12.5Gbps is provided in Figure 3.

Figure 3. Example Power Supply Block Diagram for Stratix V Transceivers with Data Rates Between 6.5Gbps and 12.5Gbps



Example 4. Power Supply Sharing Guidelines for Stratix V Transceivers with Data Rates Greater than 12.5 Gbps

Example Requiring 6 Power Regulators

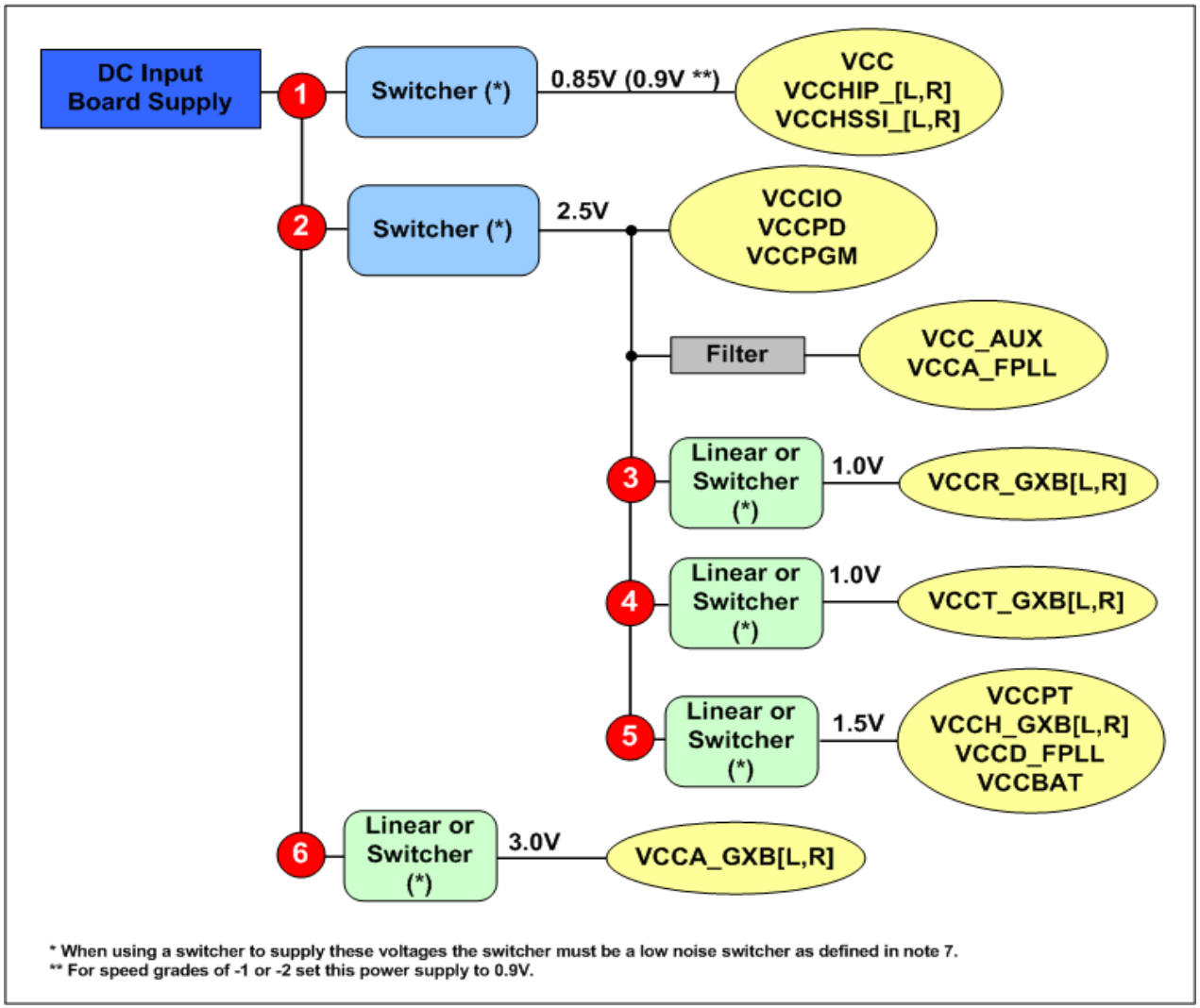
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC VCCHIP_[L,R] VCCHSSI_[L,R]	1	0.85 or 0.9 (**)	± 30mV	Switcher (*)	Share	VCC, VCCHIP and VCCHSSI must share regulators. If not using HIP, VCCHIP may be tied to GND. Also, when not using any of the transceivers on one side of the device, VCCHSSI on that side of the device may be tied to GND.
VCCIO VCCPD VCCPGM	2	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require as many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCC_AUX VCCA_FPLL		2.5			Isolate	May be able to share VCC_AUX and VCCA_FPLL with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Stratix V devices.
VCCR_GXB[L,R]	3	1.0	± 30mV	Linear or Switcher (*)	Isolate	
VCCT_GXB[L,R]	4	1.0	± 30mV	Linear or Switcher (*)	Isolate	
VCCPT VCCH_GXB[L,R] VCCD_FPLL VCCBAT	5	1.5	± 50mV	Linear or Switcher (*)	Share	If not sharing a regulator, the VCCPT supply should not exceed a tolerance of ± 50mV, however the other power supplies in this group can tolerate ± 5%. Depending on the regulator capabilities this supply may be shared with multiple Stratix V devices.
VCCA_GXB[L,R]	6	3.0	± 5%	Linear or Switcher (*)	Isolate	

(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.

(**) If you are using a -1 or -2 core speed grade, you must connect the core VCC to 0.9V.
Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Stratix V transceiver-based device with data rates between greater than 12.5 Gbps is provided in Figure 4.

Figure 4. Example Power Supply Block Diagram for Stratix V Transceivers with Data Rates Greater than 12.5 Gbps



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Example 5. Stratix V E Power Supply Sharing Guidelines

Example Requiring 3 Power Regulators

Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	0.85 or 0.9 (**)	± 30mV	Switcher (*)	Isolate	
VCCIO	2	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require as many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD						
VCCPGM						
VCC_AUX		2.5			Isolate	May be able to share VCC_AUX and VCCA_FPLL with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Stratix V devices.
VCCA_FPLL						
VCCPT	3	1.5	± 50mV	Linear or Switcher (*)	Share	If not sharing a regulator, the VCCPT supply should not exceed a tolerance of ± 50mV, however the other power supplies in this group can tolerate ± 5%. Depending on the regulator capabilities this supply may be shared with multiple Stratix V devices.
VCCD_FPLL						
VCCBAT						

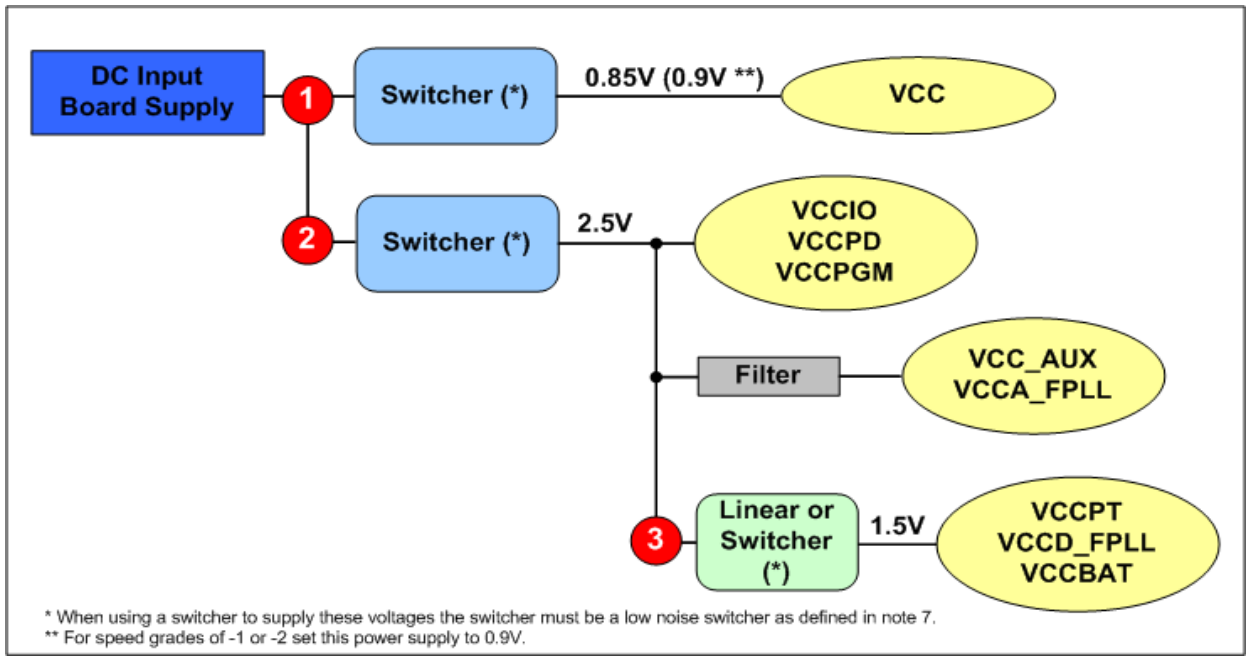
(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.

(**) If you are using a -1 or -2 core speed grade, you must connect the core VCC to 0.9V.

Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Stratix V E is provided in Figure 5.

Figure 5. Example Stratix V E Power Supplies Block Diagram



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Revision History

Revision	Description of Changes	Date
1.0	Initial Release.	6/25/2010
1.1	Added user pins. Updated rows 40, 78-85 and 102 for the "Pin Connection Guidelines" sheet. Also moved the "CvPCIe_CONFDONE"(to row 40) and "nPERST" (to row 49) out of the "Transceiver pins section".	10/4/2010
1.2	Changes to RZQ and nPERST connections, removed PORSEL. Name change to CvP_CONFDONE and VCC_AUX. VCC/VCCHSSI/VCCHIP/VCCT_GXB/VCCR_GXB/GXB_RX connection guidelines updated, added DIFFOUT, Example 3, and Figure 3 (>12.5Gbps). Updated notes 5 and 10. Changed the bus width for transceiver channels TX/RX to [0:32], REFCLK to [0:9] and CLK to [0:27]. Added bus width to VCCT_GXB, VCCR_GXB, VCCA_GXB, VCCH_GXB.	5/23/2011
1.3	Remove "Preliminary" status, MSEL internal resistor is 25k, change RREF resistor to 1.8k, C1/C2 devices VCC/VCCHIP/VCCHSSI = 0.9V. VCCA_GXB/VCCR_GXB/VCCT_GXB updated, also VCCPD/VCCPGM/VCCIO corrected, nPERST notes added, updated all figures, added a second figure for <=6.5Gbps, changed VCCR_GXB and VCCT_GXB to +/- 30mV supply tolerance.	5/31/2012
1.4	Updated the titles of the Power Supply Sharing Guidelines for Stratix V Transceivers with Data Rates <= 6.5Gbps (Option 2), Power Supply Sharing Guidelines for Stratix V Transceivers with Data Rates Between 6.5Gbps and 12.5Gbps, and Power Supply Sharing Guidelines for Stratix V Transceivers with Data Rates Greater than 12.5 Gbps.	6/1/2012