Stratix® III Device Family Pin Connection Guidelines
PCG-01004-1.3

The pin connection guidelines are considered preliminary. These pin connection guidelines should only be used as a recommendation, not as a specification. The use of the pin connection guidelines for any particular design should be verified for device operation, with the datasheet and Altera.

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Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description	Connection Guidelines
Supply and Reference Pins			
VCCL	Power	VCCL supplies power to the core voltage power supply pins.	Altera recommends that you tie these pins to 1.1 V. However, for low power designs using Stratix III -4L speed grade devices, VCCL is powered by 0.9 V. If 1.1 V is used, this plane may be connected to the same power plane as VCC. See note 3.
VCC	Power	VCC supplies power to the periphery circuitry.	Connect these pins to 1.1V power supply. This plane may be shared with the VCCL power plane if VCCL is using 1.1V. With a Proper isolation filter these pins may be shared with VCCD_PLL. For low power designs using Stratix III -4L speed grade devices, VCCL is powered by 0.9 V and VCCPT and VCC must be fully ramped before powering VCCL. For best jitter performance on your PLL dedicated output clock, it is recommended that you isolate VCC from VCCL and use separate power supply decoupling (see note 2) when all the following design conditions are true: • Core clock domain frequencies < 100MHz (found in Quartus II output report file) • Design utilization (in sub-100MHz clock domains) > 40% of total resources (found in Quartus II output report file) • Combinatorial logic (in sub-100MHz clock domains) with toggle rate > 100%, as reported by Quartus II PowerPlay Power Analyzer See note 3.
RUP[1:8]A	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O, Altera recommends that the pin be connected to the VCCIO of the bank in which the Rup pin resides, or GND. When using OCT, tie these pins to the required VCCIO banks through either a 25-Ω or 50-Ω resistor, depending on the desired I/O standard. Refer to the Stratix III data sheet for the desired resistor value of the I/O standard used.
RDN[1:8]A	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O it is recommended that the pin be connected to GND. When using OCT tie these pins to GND through either a 25Ω or 50Ω resistor depending on the desired I/O standard. Refer to the Stratix III data sheet for the desired resistor value for the I/O standard used.
VCCIO[1:8][A,B,C]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, 3.3 V), HSTL(12, 15, 18), SSTL(15, 18, 2), 3.0-V PCI/PCI-X I/O, and LVTTL(3.0 V, 3.3 V) I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, 3.3 V), 3.0-V PCI/PCI-X and LVTTL(3.0 V, 3.3 V) I/O standards.	Connect these pins to the desired voltage level required for the I/O standard on these banks. Decoupling depends on the design decoupling requirements of the specific board. See Notes 2 and 3.
VREF[1:8][A,B,C]	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.	If VREF pins are not used, designers should connect them to either the VCCIO in the bank in which the pin resides or GND. Decoupling depends on the design decoupling requirements of the specific board. See Notes 2 and 3.
VCCA_PLL[L[1:4],R[1:4],T[1:2],B[1:2]]	Power	Analog power for PLLs[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to 2.5 V, even if the PLL is not used. Designer is advised to keep isolated from other VCC for better jitter performance.	Connect these pins to 2.5 V, even if the PLL is not used. Use an isolated linear or low noise switching power supply. Power on the PLLs operating at the same frequency should be decoupled. Decoupling depends on the design decoupling requirements of the specific board. See Notes 2 and 3.
VCCD_PLL[L[1:4],R[1:4],T[1:2],B[1:2]]	Power	Digital power for PLLs[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to 1.1 V, even if the PLL is not used.	Connect these pins to 1.1 V, even if the PLL is not used. Use an isolated linear or low noise switching power supply. With a proper isolation filter these pins may be sourced from the same regulator as VCC and/or VCCL if VCCL requires 1.1V. Decoupling depends on the design decoupling requirements of the specific board. See Notes 2 and 3.

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Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description	Connection Guidelines
VCCPT	Power	Power supply for the programmable power technology. Connect to 2.5 V.	Connect these pins to 2.5 V. Use an isolated linear or low noise switching power supply. The voltage on these pins must ramp-up from 0 to 2.5 V within 5 ms to ensure successful configuration. For low power designs using Stratix III -4L speed grade devices, VCCL is powered by 0.9 V and VCCPT and VCC must be fully ramped before powering VCCL. Decoupling depends on the design decoupling requirements of the specific board. See Notes 2 and 3.
VCCPGM	Power	Dedicated Configuration power supply. Can be connected to 1.8V, 2.5V, 3.0V or 3.3V depending on the particular design.	Connect this pin to either 1.8, 2.5, 3.0, or 3.3-V power supply. Decoupling depends on the design decoupling requirements of the specific board. See Notes 2 and 3.
VCCPD[1:8][A,B,C]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers. This can be connected to 3.3 V, 3.0 V, or 2.5 V. VCCPD for 3.3-V I/O standard is 3.3 V, VCCPD for 3.0-V I/O standard is 3.0 V, and VCCPD for 2.5-V/1.8-V/1.2-V I/O standards is 2.5 V.	The VCCPD pins require 2.5, 3.0, or 3.3V and must ramp-up from 0 to 2.5, 3.0, or 3.3V within 100 ms to ensure successful configuration. Decoupling depends on the design decoupling requirements of the specific board. See Notes 2 and 3.
VCCBAT	Power	Battery back-up power supply for design security volatile key register.	Connect this pin to a Non-volatile battery power source in the range of 1.0 - 3.3 V when using design security volatile key. 3.0 V is the typical power selected for this supply. When not using the volatile key, tie this to a 3.0 V supply or GND. Do not share this source with other FPGA power supplies.
VCC_CLKIN[3,4,7,8]	Power	Differential clock input power supply for top and bottom I/O bank. Connect to 2.5 V.	Connect these pins to 2.5 V power source. Decoupling depends on the design decoupling requirements of the specific board. See Note 2.
GND	Ground	Device ground pins.	All GND pins should be connected to the board ground plane.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.	These Pins must be left unconnected.
NC	No Connect	Do not drive signals into these pins.	When designing for device migration these pins may be connected to power, ground, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern leave these pins floating.
Dedicated Configuration/JTAG Pins			
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (DATA[7:0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn, CRC_ERROR) are on or off before and during configuration. A logic high (1.8, 2.5, 3.0, or 3.3 V) turns off the weak pull-up, while a logic low turns them on.	The nIO-PULLUP can be tied directly to VCCPGM, use a 1-kΩ pull-up resistor or tied directly to GND depending on the use desired for the device. Refer to the description column.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix III device.	If the temperature sensing diode is not used then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix III device.	If the temperature sensing diode is not used then connect this pin to GND.
MSEL[2:0]	Input	Configuration input pins that set the Stratix III device configuration scheme.	These pins are internally connected through a 5-kΩ resistor to GND. Do not leave these pins floating. When these pins are unused connect them to GND. Depending on the configuration scheme used these pins should be tied to VCCPGM or GND. Refer to chapter 11, "Configuring Stratix III Devices", of the Stratix III Handbook. If only JTAG configuration is used then connect these pins to ground.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.	In multi-device configuration, nCE of the first device is tied directly to GND while its nCEO pin drives the nCE of the next device in the chain. In single device configuration and JTAG programming, nCE should be connected directly to GND.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.	If this pin is not used this pin requires a connection directly or through a 10-kΩ resistor to VCCPGM.

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CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration Done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.	Connect this pin to an external 10-kΩ pull-up resistor to a supply that provides an acceptable input signal for the Stratix III device. VCCPGM should be high enough to meet the V_{IH} specification of the I/O on the external device.
nCEO	Output	Output that drives low when device configuration is complete.	During multi-device configuration, this pin feeds a subsequent device's nCE pin. During single device configuration, this pin is left floating. For recommendations on how to connect nCEO in a chain with multiple voltages across the devices in the chain, refer to the Stratix III chapter in Volume 1 of the Stratix III Device Handbook.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.	Connect this pin to an external 10-kΩ pull-up resistor to a supply that provides an acceptable input signal for the Stratix III device. VCCPGM should be high enough to meet the V_{IH} specification of the I/O on the external device.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high (1.8, 2.5, 3.0, or 3.3 V) selects a POR time of 12 ms and a logic low selects POR time of 100 ms.	The PORSEL pin should be tied directly to VCCPGM or GND.
TCK	Input	Dedicated JTAG test clock input pin.	Connect this pin to a 1-kΩ pull-down resistor to GND. The JTAG circuitry can be disabled by connecting TCK to GND. TCK is powered by VCCPD1A.
TMS	Input	Dedicated JTAG test mode input pin.	Connect this pin to a 1k - 10kΩ pull-up resistor to VCCPD. To disable the JTAG circuitry connect TMS to VCCPD. TMS is powered by VCCPD1A.
TDI	Input	Dedicated JTAG test data input pin.	Connect this pin to a 1k - 10kΩ pull-up resistor to VCCPD. To disable the JTAG circuitry connect TDI to VCCPD. TDI is powered by VCCPD1A.
TDO	Output	Dedicated JTAG test data output pin.	The JTAG circuitry can be disabled by leaving TDO unconnected. TDO is powered by VCCPD1A.
TRST	Input	Dedicated active low JTAG test reset input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.	Utilization of TRST is optional. When using the JTAG circuitry but not using TRST tie this pin directly to VCCPD. To disable the JTAG circuitry, tie this pin to GND. TRST is powered by VCCPD1A.
Clock and PLL Pins			
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.	Connect unused pins to GND.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.	Connect unused pins to GND.
CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
CLK[4:7,12:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.

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Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description	Connection Guidelines
CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.	Connect unused pins to GND.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L1, L4, R1, and R4 respectively.	Connect unused pins to GND.
PLL_[L1:L4,R1:R4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[L1:L4,R1:R4]_FB_CLKOUT0p	I/O, Clock		These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual-purpose I/O pin that can be used as a single-ended output, a single ended external feedback input, or as the positive pin of a differential external feedback input.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	Dual-purpose I/O pin that can be used as a single-ended output or as the negative pin of a differential external feedback input.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[T1,T2,B1,B2]_CLKOUT0[p,n]	I/O, Clock	I/O pins that be used as two single-ended clock output pins or one differential clock output pair.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
Optional/Dual-Purpose Configuration Pins			
nCSO	Output	Dedicated output control signal from the Stratix III FPGA to the serial configuration device in AS mode that enables the configuration device.	When not programming the device in AS mode nCSO is not used. Also, when this pin is not used as an output then it is recommended to leave the pin unconnected.
ASDO	Output	Control signal from the Stratix III FPGA to the serial configuration device in AS mode used to read out configuration data.	When not programming the device in AS mode ASDO is not used. Also, when this pin is not used as an output then it is recommended to leave the pin unconnected.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the Stratix III device. In AS mode, DCLK is an output from the Stratix III device that provides timing for the configuration interface.	
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.	Connect this pin to an external 10-kΩ pull-up resistor to VCCPGM.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high (VCCPGM), all registers behave as programmed.	When the dedicated input DEV_CLRn is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground.

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DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high (VCCPGM), all I/O pins behave as defined in the design.	When the dedicated input DEV_OE is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.	When the dedicated input for DATA[0] is not used and this pin is not used as an I/O then it is recommended to leave this pin unconnected.
DATA[7:1]	I/O, Input	Dual-purpose configuration input data pins. The DATA[7:0] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.	When the dedicated inputs for DATA[7:1] are not used and these pins are not used as an I/O then it is recommended to leave these pins unconnected.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.	Connect this pin to an external 10-kΩ pull-up resistor to VCCPGM.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.	If the CLKUSR pin is not used as a configuration clock input and the pin is not used as an I/O then it is recommended to connect this pin to ground.
Differential I/O Pins			
DIFFIO_RX[##]p/n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Unused pins can be tied to GND or unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
DIFFIO_TX[##]p/n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Unused pins can be tied to GND or unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
DIFFOUT_[##]p/n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Unused pins can be tied to GND or unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
External Memory Interfaces Pins			
DQS[1:44][T,B], DQS[1:40][L,R]	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.	Unused pins can be tied to GND or unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
DQSn[1:44][T,B], DQSn[1:40][L,R]	I/O, DQSn	Optional complementary data strobe signal for use in QDRII SRAM. These pins drive to dedicated DQS phase shift circuitry.	Unused pins can be tied to GND or unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
DQ[1:44][T,B], DQ[1:40][L,R]	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	Unused pins can be tied to GND or unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
CQ[1:44][T,B], CQ[1:40][L,R]	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.	Unused pins can be tied to GND or unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.

You should create a Quartus II design, enter your device I/O assignments and compile the design. Quartus II will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this document or the device handbook.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description	Connection Guidelines
CQn[1:44][T,B], CQn[1:40][L,R]	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.	Unused pins can be tied to GND or unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.

Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

Notes:

1) This pin connection guideline is created based on the largest Stratix III device (EP3SL340)

2) Capacitance values for the power supply should be selected after consideration of the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage droop requirements of the device/supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as innerplane capacitance with low inductance should be considered for higher frequency decoupling.

3) Low Noise Switching Regulator - defined as a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz and has fast transient response.
Line Regulation < 0.4%
Load Regulation < 1.2%

Example 1. Stratix III Power Supply Sharing Guidelines

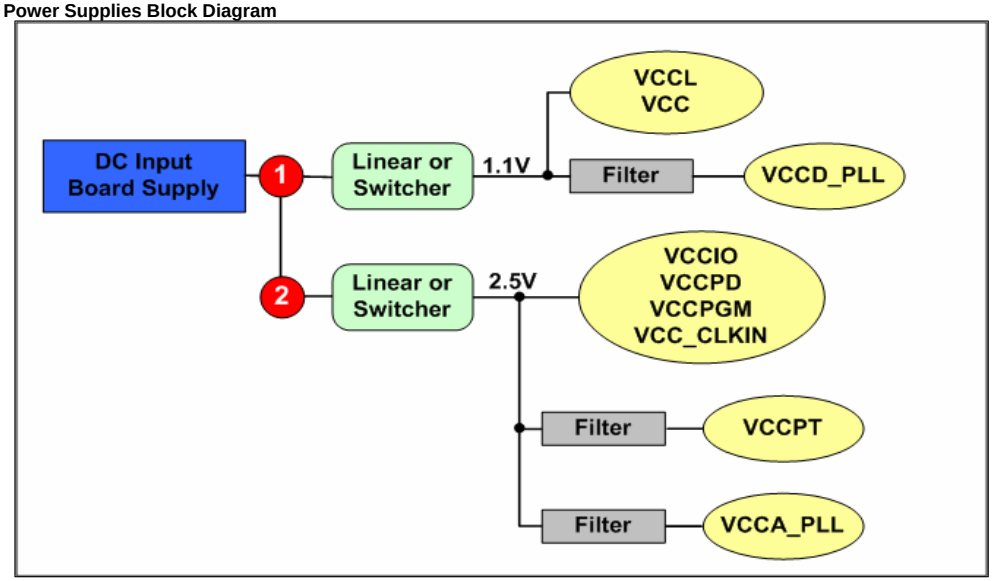
Example Requiring 2 Power Regulators

Power	Regulator	Voltage	Supply	Power	Regulator	Notes
VCCL	1	1.1	± 50 mV	Switcher	Share	Depending on the regulator capabilities this supply may be shared with multiple Stratix III devices. Use the EPE tool to assist in determining the power required for your specific design.
VCC						
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]					Isolate	
VCCIO[1:8][A,B,C]	2	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5 V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require a 2.5-V regulator for VCC_CLKIN and as many regulators as there are variations of supplies in your specific design. Depending on the regulator capabilities this supply may be shared with multiple Stratix III devices. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD[1:8][A,B,C]						
VCCPGM						
VCC_CLKIN[3,4,7,8]		2.5			Share	
VCCPT					Isolate	
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]					Isolate	

* When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 3.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Stratix III device is provided in Figure 1.

Figure 1. Example Stratix III Power Supplies Block Diagram



Example 2. Stratix III Power Supply Sharing Guidelines (Low Power VCCL Devices)

Example Requiring 3 Power Regulators

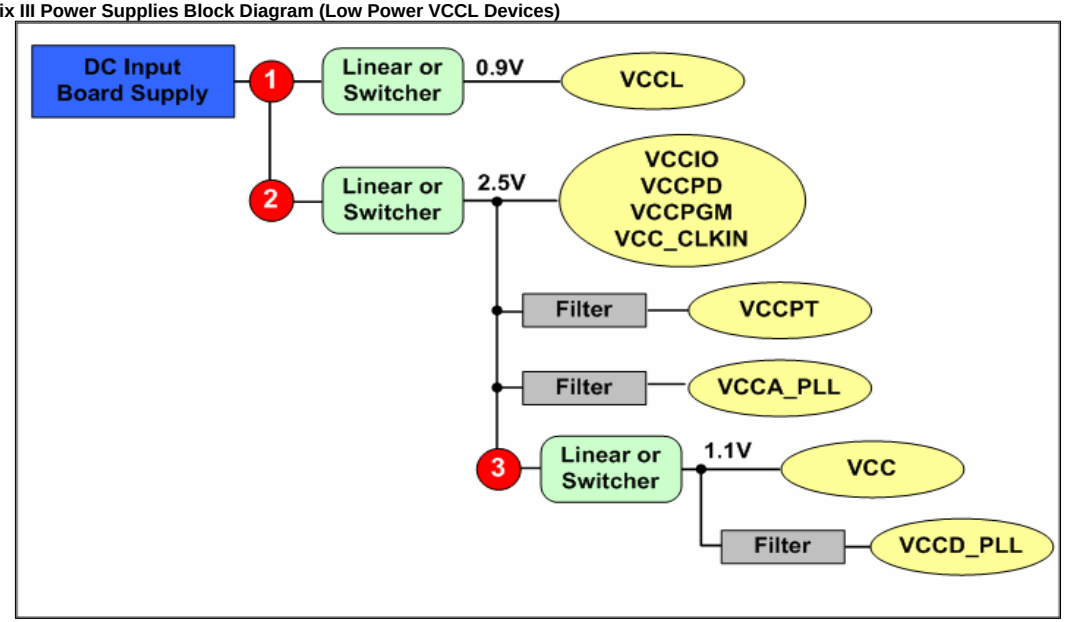
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCL**	1	0.9	± 40 mV	Switcher	Share	Depending on the regulator capabilities this supply may be shared with multiple Stratix III devices. Use the EPE tool to assist in determining the power required for your specific design.
VCCIO[1:8][A,B,C]	2	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require a 2.5-V regulator for VCC_CLKIN and as many regulators as there are variations of supplies in your specific design. Depending on the regulator capabilities this supply may be shared with multiple Stratix III devices. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD[1:8][A,B,C]						
VCCPGM						
VCC_CLKIN[3,4,7,8]		2.5			Share	
VCCPT **					Isolate	
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]					Isolate	
VCC **	3	1.1	± 50 mV	Switcher	Share	Depending on the regulator capabilities this supply may be shared with multiple Stratix III devices. Use the EPE tool to assist in determining the power required for your specific design.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]					Isolate	

* When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 3.

** VCCPT and VCC must be fully ramped before powering VCCL.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Stratix III device is provided in Figure 2.

Figure 2. Example Stratix III Power Supplies Block Diagram (Low Power VCCL Devices)



Stratix® III Device Family Pin Connection Guidelines
PCG-01009-1.3

Revision History

Rev	Description of Changes	Date
1.0	Initial release	10/19/2007
1.1	Changed VCCPD[1..8][A,B,C] pin description and guidelines	4/9/2008
1.2	Changed VCCPGM, RUP[1..8]A, VCCL, VCC, VCCIO[1..8][A,B,C], PORSEL, and nIO_PULLUP connection guidelines. Divided CLK[0,2,4,5,6,7,9,11..15]p,n into separate CLK[0,2,9,11]p,CLK[0,2,9,11]n, CLK[4..7,12..15]p, CLK[4..7,12..15]n.	4/11/2008
1.3	Added Power Regs examples. Updated VCCD_PLL, JTAG, VCCPT, NC, VCCBAT,nCE, nCONFIG,CONF_DONE, nSTATUS, Clocks and PLLs, DIFFIO, and Ext. Memory guidelines, Added note 3, Changed TMS/TDI pull up to a range of 1k - 10kΩ.	1/25/2010