Reliability Report 53
Q2 2012

Overview

Altera® designs and manufactures Programmable Logic Devices (PLDs). These are user configurable integrated circuits used to implement custom digital logic functions. Altera offers a wide assortment of PLD and configuration device families. These are all described in detail in the appropriate device data sheet.

Product information, such as device architecture, detailed packaging information, handling and surface mount guidelines, and product change notifications can also be found at Altera's Web site: http://www.altera.com. Altera literature is available in Adobe Acrobat and postscript format.

Altera Technical Support is also available at Altera's Support web site, which includes mySupport <https://www.altera.com/myaltera/mal-index.jsp>, Altera's technical on-line support system and the Altera Knowledge Database, both of which can be used to find answers to technical questions. Additionally, Altera maintains a toll-free customer hotline for general assistance: 800-800-EPLD (1-408-544-8767 if calling from outside US).

Altera has a closed loop quality and reliability system that conforms to the requirements of ISO 9001:2008, MIL-I-45208 and JEDEC standards. Altera and all of its major suppliers are ISO 9000 certified. Altera's Reliability qualification and monitoring programs are also governed by internal specifications, which define procedures, pass/fail requirements, and corrective actions. Altera has been ISO9001 certified since October, 1994. Altera's ISO 9001 auditor is the National Standards Authority of Ireland, NSAI.

Altera's mission is to be a preeminent supplier of programmable silicon solutions to the electronics industry through product leadership, excellent value, and superior quality and service. To achieve and maintain this preeminent supplier status, Altera must provide cost–effective, state–of–the–art solutions to our customers in a timely manner while consistently meeting or exceeding their quality, reliability, and service expectations.

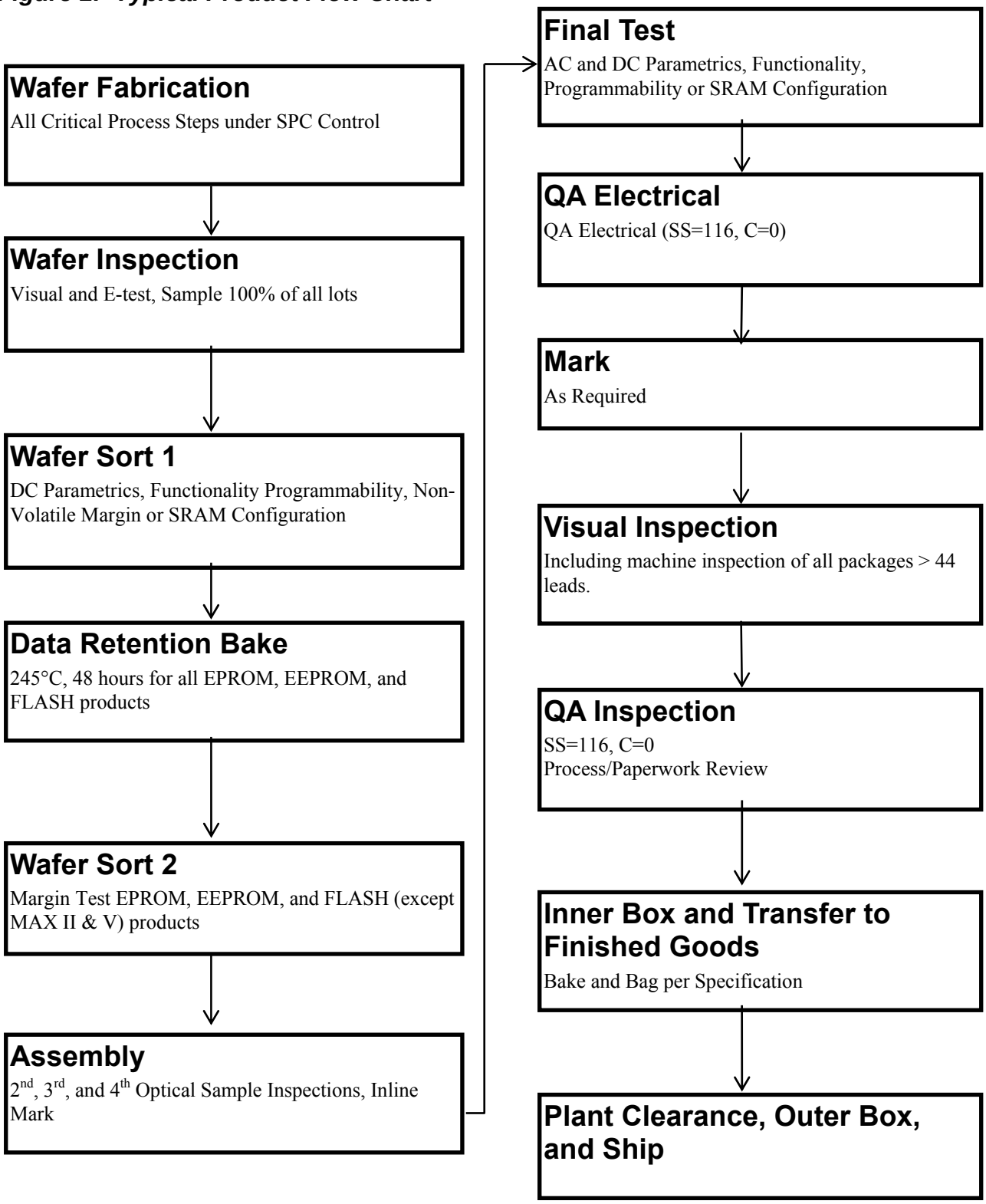
Altera Quality Systems

Altera's quality system is designed to meet all the requirements of ISO 9001, and is described in Altera's Quality Manual, 11G-00000. Altera's quality systems have also been reviewed and assessed in great detail by some of its major customers, which include multinational corporations from all over the world. Altera maintains complete on-line documentation and computer aided manufacturing systems to control product manufacturing. Internal specifications are in compliance with applicable JEDEC standards. Altera's computer aided manufacturing enables complete fabrication and assembly lot traceability. Altera maintains a network of Applications and Quality engineering personnel to support customers in the design, debug, manufacturing, and distribution of its products.

Altera is able to provide the automotive supply chain with the highest levels of quality and reliability because all of Altera's manufacturing partners (TSMC, ASE and Amkor) are certified and registered to the ISO/TS 16949 automotive industry quality standard.

Altera performs comprehensive testing and manufacturing controls on all its products. Figure 1 shows a typical product manufacturing flow.

Figure 1: Typical Product Flow Chart



Reliability Methodology

Reliability qualifications and monitoring are performed specifically for each product family. All members of a product family utilize the same circuit architecture, fabrication process, and share the same package types. Examples of Altera's product families are MAX® 3000, MAX 7000, Stratix®, Stratix GX, Cyclone®, Arria, Stratix II, Stratix II GX, Cyclone II, Stratix III, Cyclone III, Stratix IV, Arria II, Cyclone IV, Stratix V, Arria V, Cyclone V, MAX II, MAX V and HardCopy®. A product family will contain several products, all based upon the same logic elements, embedded storage elements, and programmable interconnect technology. Product families have 2 to 10 members, with a range of densities and packaging options. For reliability purposes such as data reporting and failure rate prediction, a product family will be reported on a fabrication process technology. The fabrication process is described by the storage element technology (i.e. SRAM, EPROM, or EEPROM) and feature size (i.e. 0.13µ or 65 nm).

Product families are qualified based upon the requirements specified in Table I. Reliability monitors are based on the schedules specified in Table II. Product family qualification will include products with a range of densities, package types, and package leadcounts. If a new product is added to the product family with a significant increase (more than 50%) in logic elements, a product qualification will be performed.

Products shipped into the automotive market are also qualified to the Automotive Electronics Council standard AEC-Q100 requirements, which require a much larger sample size. Altera is a member of the AEC, and automotive products meet the requirements of AEC-Q100. Details may be found at www.aecouncil.com.

Products shipped into the military/aerospace market are qualified to the requirements of the AQEC (Aerospace Qualified Electronic Component) standard, GEIA-Std-0002-1 and IEC-62564. Altera was the first semiconductor supplier to announce compliance to this standard for the Cyclone, Stratix and MAX II families. This standard emphasizes the communication between the IC supplier and the military/aerospace and defense contractors.

Customers are notified of changes to products through Altera's Product Change Notification system. Notifications are based on changes affecting form, fit, or function. Notifications are also found at Altera's Web site at www.altera.com. Customers can also sign up to Altera's PCN mailing list at https://www.altera.com/literature/updates/registration/upd-registration.jsp

Reliability monitors are performed on a regular basis in order to assure that Altera's normal production testing and process control methodologies produce reliable products. The Reliability monitor program is also based upon a product family methodology. Different products and package types are procured from normal production on a Last In First Out (LIFO) schedule to monitor product reliability. Results in this report cover data gathered in the last 24 months.

Table I: Reliability Qualification Requirements

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TYPE OF TEST			**Full Qualification**	
MIL-STD-883 or JEDEC Std.	**METHOD /CONDITION**	**SAMPLE SIZE**	**# of Lots**	**Accept Criteria # Rej./Lot**
Life Test JESD22-A108	1000 hours @ 1.1 - 1.2 x Vcc, T_j: 110°C min, 140°C max 2000 hours for reference	≤100 pins (77) 101-240 pins (45) >240 pins (25)	3	1 1 0 < 200 FIT@55°C
Retention Bake JESD22-A103	1000 hours min. @ 150°C, 168 hours min @ 245°C for wafer level may be substituted.	≤100 pins 45 >100 pins 25	3	1 0
Temperature Cycling JESD22-A104	Preconditioning + 700 cycles. -55°C to +125°C (condition B)	≤100 pins 45 >100 pins 25	3	1 0
Biased Humidity/Temp JESD-A101 Or H.A.S.T JESD-A110	Preconditioning + 85°C, 85% R.H.; 1000 hours @ Vcc nom; Or 130°C, 85% RH, 48 or 96 hours, @ Vcc nom.	≤100 pins 45 >100 pins 25	3	1 0
Autoclave JESD22-A102 Or Unbiased H.A.S.T JESD-A118	121°C, 15 PSIG; 96 hours, 168 hours for reference Or 130°C, 85% RH, 96 hours	≤100 pins 45 >100 pins 25	3	1 0
ESD HBM JESD22-A114 Mil Std 3015.7	100pf, & 1500Ω. Record Distribution of all Failing Pins	3	1	≥ 1000V
ESD Charged Device Model JESD22-C101	Field Induced Charge Device	3	1	≥ 500 V for GIO; ≥ 200 V for high-speed pins < 10 GHz; Characterize for high-speed pins ≥10 GHz
Latch-up JESD 78	(Icc nom. + 100mA) or Icc nom. + 50% on I/O, Vcc + 50% on Power Supplies	6	1	0
Program/Erase Cycling	Program/Erase 100 cycles (EEPROM or FLASH)	25	1	0
PCB Interconnect Reliability IPC 9701 JESD22-A104	0°C to +100°C, Single Chamber	25	1 Daisy Chain	>2000 Cycles to 0.1% Predicted Failure

Table II: Reliability Monitor Program

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TYPE OF TEST MIL-STD-883 or JEDEC Std.	**METHOD/CONDITION**	**SAMPLE SIZE**	**FREQUENCY**
Life Test JESD22-A108	1000 hours @ 1.1 - 1.2 x Vcc nom. T_j :110°C min, 140°C max 2000 hours for reference	≤100 pins 77 >100 -240 pins 45 >240 pins 22	Any month of a Qtr./ Process
Retention Bake Non-Volatile Products JESD22-A103	1000 hours min. @ 150°C	≤100 pins 45 >100 pins 22	Any month of a Qtr./ Process
Temperature Cycling JESD22-A104	Preconditioning + 700 cycles. -55°C to +125°C Industrial, 0°C to +125°C Commercial,	≤100 pins 45 >100 pins 22	Any month of a Qtr./ Process
Biased Humidity/Temp. JESD-A101 Or H.A.S.T. JESD-A110	Preconditioning + 85°C, 85% R.H. 1000 hours min. @ Vcc nominal; Or 130°C, 85% RH, 96 hours, @ Vcc nominal	≤100 pins 45 >100 pins 22	Any month of a Qtr./ Process
Autoclave JESD22-A102 Or Unbiased H.A.S.T. JESD-A118	121°C, 15 PSIG; 96 hours min. 168 hours for reference Or 130°C, 85% RH, 96 hours	≤100 pins 45 >100 pins 22	Any month of a Qtr./ Process
Program/Erase	Program/Erase 100 cycles (EEPROM or FLASH only)	22	Any month of a Qtr./ Process

Lifetest: Methodology and Failure Rate Prediction

Lifetest Methodology

Altera performs a high temperature / high voltage Lifetest on its products to accelerate failure mechanisms. Failure mechanisms are accelerated by elevating the ambient temperature of the Lifetest chamber in order to increase the junction temperature to at least 125°C and by increasing the voltage of the Vcc power supply by 10-20%. In some cases where increasing junction temperature to 125°C is not possible because of risk of thermal runaway, a minimum junction temperature of 110°C is used. The lifetest boards have special high temperature sockets that maintain lead integrity.

FLEX, APEX, Mercury, Stratix, Stratix GX, Cyclone, Stratix II, Stratix II GX, and Cyclone II devices use static life test mode. 65/60 nm, 40nm and 28 nm products use dynamic life with a real clocked configuration. MAX 3000, MAX 7000, MAX 9000 devices (EEPROM devices), MAX II and MAX V (FLASH devices) are first subjected to 100 Program Erase Cycles before starting Lifetest.

Each device is tested using production test equipment to data sheet specifications before being stressed. All readouts are also done on the same production test equipment to data sheet parameters. A device is considered a failure if it does not pass data sheet specifications.

For non-volatile configuration elements except those on MAX II and V devices, there is a test mode that allows the configuration elements to be margin tested to determine the amount of charge on the floating gate. At each readout, the margin of every configuration element is tested and the lowest margin is recorded.

MAX II and V devices are uniquely designed so that the functionality of the device is only affected by charge gain on erased bits and will not be affected by charge loss on programmed bits. We challenge erased bits at 25 uA during MAX II and V testing, although 10 uA is all we need to assure functionality.

Failure Rate Prediction

Altera uses industry standard techniques for failure rate prediction. Failure rates are predicted based upon an exponential distribution of failures in time (constant failure rate).

As noted above, both elevated temperatures and voltages are used to accelerate failures in lifetest, and the overall acceleration is simply the product of the thermal and voltage acceleration:

Equivalent Hours in typical use conditions = (Hours in lifetest) x (Acceleration factor)

Acceleration Factor = (Thermal Acceleration) x (Voltage Acceleration)

Thermal and voltage acceleration factors are based on standard acceleration formulas and published acceleration factors. Acceleration Factors are based upon JEDEC Publication JEP122. The formulas are presented below, and the acceleration factors are listed in Table III. As we are moving to thin gate-oxide (< 70 Å) technology, we have observed the power-law dependence on voltage acceleration. We use the power-law model for gate oxide voltage acceleration on 65 nm and smaller process technology.

Note that a dielectric breakdown acceleration factor of 0.7eV is used for all processes of 90 nm and larger. Published papers have demonstrated that modern oxides have higher thermal activation energy than the previously reported 0.3eV. Values of 0.3eV to 0.9eV have been reported. [i] [ii] Altera has verified through multiple temperature Burn-In studies that 0.7eV is applicable for 90 nm and larger process. Different acceleration factors are used on 65 nm and smaller process based on power-law model.

Junction temperatures, not ambient temperatures, must be used in calculating thermal acceleration factors. A designer can determine device power dissipation using the Early Power Estimator (EPE) available on www.altera.com, or using the PowerPlay power analyzer in the Quartus II design tool. Junction temperatures are calculated from ambient temperature or case temperature measurements using the thermal resistance values found in the Altera Device Package Information Data Sheet. Thermal resistance values are specific to each product and package combination. For convenience, formulas to calculate junction temperatures are included with the acceleration formulas below.

Note also that temperatures must be converted to Degrees Kelvin when using the Temperature Acceleration formula below. Degrees Kelvin = Degrees Centigrade + 273.

Temperature Acceleration Factor = $\exp[Ea/((k)(Toperation)) - Ea/((k)(Tstress))]$

k = Boltzmann's constant = 8.62 x 10-5 eV/°K

Ea = Activation energy in eV (see Table III)

T = Junction Temperature in Degrees Kelvin

kT(eV) = 0.0258 x (temperature in Centigrade + 273)/298

Gate Oxide Voltage Acceleration Factor = $\exp[(\gamma/(tox/10\ nm))(Vstress - Voperation)]$

γ = Voltage exponent factor (see Table III)

Interlayer Dielectric Acceleration Factor = $\exp[(\gamma)(Vstress - Voperation)]$

Junction Temperature = (Ambient Temperature)+(Power dissipation)*(θja)

= (Case Temperature)+(Power dissipation)*(θjc)

θja and θjc are found in the Altera Device Package Information Data Sheet.

Table III: Common Failure Mechanisms and Acceleration Factors [iii]

Mechanism	Activation Energy "Ea" [eV]	Voltage Exponent Factor
Gate Oxide Breakdown (≥ 90 nm)*	0.7	$\gamma = 3.2$
Interlayer defect	0.7	$\gamma = 2.0$
Via Voiding (0. 15 µm & 0. 13 µm)	0.8	0.0
Via Voiding (≤ 90 nm)	1.0	0.0
Silicon Junction Defect	0.8	0.0
Masking (Poly, Diffusion, etc.) Defect	0.5	0.0
Metallization Defect	0.5	0.0
Al Electromigration	0.7 (Al-Si), 0.85 (Al-Cu)	Current density dependence ($1/J^2$)
Cu Electromigration (0. 13 µm, FSG dielectric)	0.8	Current density dependence ($1/J^2$)
Cu Electromigration (≤ 90 nm low-k dielectric)	0.9	Current density dependence ($1/J$)
Contamination (Surface & Bulk)	1.0	0.0
Data Retention		
Charge Loss (EPROM)	0.6	0.0
Charge Detrapping (FLASH &EEPROM, ≤ 168 hrs)	1.1	0.0
SILC (FLASH & EEPROM, > 168 hrs)	0	2.3

*≤ 65 nm process uses different values with power-law model

Failure rates are calculated on a product family basis (as in the tables of data on the following pages). Device hours accumulated at the stress conditions are converted to normal use conditions using the acceleration factors described above. Equivalent hours are calculated at a typical use condition of Vcc nominal in a 55°C still-air ambient or 70°C junction.

Failure mechanisms are determined by failure analysis. For each failure mechanism observed in stress, the acceleration factor is calculated using the formulas and acceleration factors above. If two failure mechanisms are active, the failure rate due to each one is summed to produce a combined failure rate. If there are no failures, the failure mechanism with lowest acceleration factor is used to calculate failure rate.

Failure rates are expressed in terms of FITs or Failures In Time, where one FIT is equivalent to one failure in one billion or 10^9 device-hours. Altera calculates the FIT rate using the JESD85 (Methods for Calculating Failure Rates in Units of FITs) standard.

The failure rate is calculated using a Chi-squared distribution to predict a 60% confidence level from the small number of failures and limited sample size of the population tested. The Chi-squared value is calculated from the inverse Chi-squared distribution using the desired probability level and the degrees of freedom. [iv] The degrees of freedom are calculated as: $\nu = 2n+2$, where n= # of failures observed. The failure rate is then calculated from the Chi-squared value:

$$Failure\ Rate = \frac{X^2}{(2 * A.F. * Device\ hours)}\ failures/hour$$

The FIT rate is 10^9*Failure Rate and the Mean Time to Failure is simply the inverse of the failure rate for an exponential distribution.

Lifetest Results

Lifetest Results are reported by Product Family. Where a product family is produced on different wafer fabrication technologies the results are reported separately for each fabrication technology. Within a product family the same logic configuration elements, macrocells, and programmable interconnect are used. The only variable is the size of the product, with each family having 3 to 10 different numbers of macrocells or logic elements. A brief description of the product family and process technology is included in each section.

FLEX 0.42µ Products

FLEX 8000, FLEX 10K, and FLEX 6000 products are fabricated on a 0.42µ feature size on the same process technology. This technology supports 3 layers of metallization. Lifetests are conducted at 6.0V, which is a 20% overvoltage.

FLEX 0.42µ Lifetest Results

REL LOT #	DEVICE	PACKAGE TYPE	TA	# UNITS	L.T. HOURS	# FAIL		DEVICE HOURS	Pkg. Fail. EQUIV. HRS.	Date Code
9020001	EPF10K10	208 PQFP	125	44	1015	0		44660	6.13E+06	0901
10030001	EPF10K50	240 RQFP	125	25	1000	0		25000	2.99E+06	1008
10040004	EPF10K70	240 RQFP	125	24	1000	0		24000	2.86E+06	1013
10110029	EPF10K70	240 RQFP	125	45	1000	0		45000	5.35E+06	1048
11040014	EPF10K70	240 RQFP	125	45	1000	0		45000	5.35E+06	1107
11030014	EPF6016	208 PQFP	125	45	1000	0		45000	5.45E+06	1101
9070001	EPF8282A	84 PLCC	125	77	1000	0		77000	8.69E+06	0919
									3.68E+07	
Failure Mechanism				**# Fail**	**Chi Sq.**			**Equiv. Hrs.**	**FITs**	
Package Failure(Ea=1.0,C=0)				0	1.83			3.68E+07	**24.9**	

FLEX 0.3/0.35µ Products

FLEX 10KA and FLEX 6000A products are fabricated on a 0.3/0.35µ process technology that supports up to 4 layers of metallization. The process technology operates with a 3.3V supply voltage and has I/Os that are 2.5V and 5.0V tolerant. Devices are available in TQFP, PQFP, RQFP, FBGA and BGA packages with logic density ranging from 576 LEs to 12,160 LEs. Lifetests are conducted at 4.0V, which is a 20% overvoltage.

FLEX 0.3/0.35µ Lifetest Results

REL LOT #	DEVICE	PACKAGE TYPE	TA	# UNITS	L.T. HOURS	# FAIL		DEVICE HOURS	Interlayer EQUIV. HRS.	Date Code
10080023	EPF10K30A	144 TQFP	125	45	1000	0		45000	1.75E+06	1019
9050005	EPF10K50V	356 BGA	125	25	1000	0		25000	1.52E+06	0913
10020042	EPF10K100A	240 RQFP	125	25	1000	0		25000	1.44E+06	1001
10040033	EPF10K100A	240 RQFP	125	45	2000	0		90000	5.30E+06	1016
11070013	EPF10K100A	484 FBGA	125	25	1000	0		25000	9.99E+05	0937
9080008	EPF6016A	144 TQFP	125	45	1000	0		45000	3.11E+06	0932
									1.41E+07	
Failure Mechanism				**# Fail**	**Chi Sq.**			**Equiv. Hrs.**	**FITs**	
Interlayer Defect				0	1.83			1.41E+07	**64.8**	

FLEX, ACEX, and APEX 0.22µ Products

FLEX 10KE, FLEX 10KS, ACEX, and APEX 20K products are fabricated on a 0.22µ process technology that supports up to 5 layers of metallization. Devices are available in TQFP, PQFP, RQFP, FBGA and BGA packages with logic density ranging from 1728 LEs to 16,640 LEs. The process technology operates with a 2.5V supply. Lifetests are conducted at 3.0V, which is a 20% overvoltage

FLEX, ACEX, and APEX 0.22µ Lifetest Results

REL LOT #	DEVICE	PACKAGE TYPE	TA	# UNITS	L.T. HOURS	# FAIL		DEVICE HOURS	Interlayer EQUIV. HRS.	Date Code
10050025	EP1K50	256 FBGA	125	25	1000	0		25000	3.73E+06	1013
10090006	EP1K50	256 FBGA	125	45	2000	0		90000	1.34E+07	1031
11100016	EP20K100	208 PQFP	125	45	1000	0		45000	4.83E+06	1119
9100008	EP20K100	356 BGA	125	25	1000	0		25000	4.57E+06	0931
9040003	EPF10K100E	208 PQFP	125	45	1000	0		45000	3.34E+06	0913
10020025	EPF10K100E	356 BGA	125	25	1000	0		25000	3.74E+06	1001
11110023	EPF10K100E	356 BGA	125	25	1000	0		25000	3.74E+06	1131
10050019	EPF10K50S	256 FBGA	125	45	2000	0		90000	1.34E+07	1018
10120008	EPF10K200S	672 FBGA	125	25	2000	0		50000	3.70E+06	1050
									5.45E+07	
Failure Mechanism				**# Fail**	**Chi Sq.**			**Equiv. Hrs.**	**FITs**	
Silicon Defect (Ea=0.9)				0	1.83			5.45E+07	**16.8**	

APEX, Excalibur, and Mercury 0.18µ Products

APEX 20KE, Excalibur, and Mercury products are fabricated on a 0.18µ process technology that supports up to 8 layers of metallization. Devices are available in TQFP, PQFP, RQFP, FBGA, BGA & PGA packages with logic density ranging from 4,160 LEs to 42,240 LEs. The process technology operates with a 1.8V supply. Lifetests are conducted at 2.3V, which is over 25% overvoltage.

APEX, Excalibur, and Mercury 0.18µ Lifetest Results

REL LOT #	DEVICE	PACKAGE TYPE	TA	# UNITS	L.T. HOURS	# FAIL		DEVICE HOURS	Interlayer EQUIV. HRS.	Date Code
10020023	EP20K100E	208 PQFP	125	46	1000	0		46000	3.31E+06	1001
12020014	EP20K100E	240 PQFP	125	45	1000	0		45000	2.04E+06	1125
9030002	EP20K160E	240 PQFP	125	45	1000	0		45000	2.20E+06	0907
11080018	EP20K160E	356 BGA	125	25	1000	0		25000	1.94E+06	1101
10040002	EP20K200E	208 PQFP	125	45	1000	0		45000	2.08E+06	1007
9090020	EP20K300E	672 FBGA	125	25	1000	0		25000	2.90E+06	0925
11040003	EP20K300E	672 FBGA	125	28	1000	0		28000	3.25E+06	1115
9060011	EP20K400E	672 FBGA	125	25	1063	0		26575	1.19E+06	0919
									1.89E+07	
Failure Mechanism				**# Fail**	**Chi Sq.**			**Equiv. Hrs.**	**FITs**	
Interlayer Defect				0	1.83			1.89E+07	**48.4**	

APEX and Mercury 0.15µ Products

APEX 20KC, APEX II and Mercury products are fabricated on a 0.15µ process technology that supports up to 8 layers of Cu metallization. Devices are available in FBGA, QFP, BGA, and FlipChip FBGA packages with logic density ranging from 8,320 LEs to 67,200 LEs and 106Kbits to 1.1Mbits of embedded RAM. These devices offer 1 Gbps LVDS I/Os, Clock-Data Synchronization, and support for numerous high-speed memory interfaces. The APEX 20KC product family operates with a 1.8V supply and the lifetest is conducted at 2.3V, which is a 25% overvoltage. The APEX II product family operates at 1.5V and the lifetests are conducted at 1.8V, which is a 20% overvoltage.

APEX and Mercury 0.15µ Lifetest Results

REL LOT #	DEVICE	PACKAGE TYPE	TA	# UNITS	L.T. HOURS	# FAIL		DEVICE HOURS	Dielectric EQUIV. HRS.	Date Code
9020002	EP20K400C	672 FBGA	125	25	1000	0		25000	5.13E+07	0901
10090008	EP20K400C	672 FBGA	125	25	1000	0		25000	5.13E+07	1031
11050015	EP20K400C	672 FBGA	125	25	1000	0		25000	5.13E+07	1121
									1.54E+08	
Failure Mechanism				**# Fail**	**Chi Sq.**			**Equiv. Hrs.**	**FITs**	
Dielectric Breakdown				0	1.83			1.54E+08	**5.96**	

Stratix, Stratix GX, Cyclone and HardCopy 0.13µ Products

Stratix, Stratix GX, Cyclone and HardCopy products are fabricated on a 0.13µ process technology that supports up to 9 layers of Cu metallization. Devices are available in FBGA, QFP, BGA, and FlipChip FBGA packages with logic density ranging from 2,910 LEs to 79,040 LEs and 59Kbits to 10.1Mbits of embedded RAM. Stratix devices offer DSP blocks, Clock-Data Synchronization, and support for numerous high-speed memory interfaces. Stratix GX devices add 3.125-Gbps I/Os to the Stratix features. Cyclone devices are optimized for low cost/Logic Element. The Stratix, Stratix GX, Cyclone and HardCopy product families operate with a 1.5V supply and the lifetest is conducted at 1.8V, which is a 20% overvoltage. A lifetest temperature of 100°C is used on some devices to keep junction temperature below absolute maximum ratings.

Stratix, Stratix GX, Cyclone and HardCopy 0.13µ Lifetest Results

REL LOT #	DEVICE	PACKAGE TYPE	TA	# UNITS	L.T. HOURS	# FAIL		DEVICE HOURS	Via voiding Fail. EQUIV. HRS.	Date Code
11060013	EP1C3	144 TQFP	125	77	1000	0		77000	4.48E+06	0937
9050010	EP1C6	144 TQFP	125	24	1000	0		24000	1.37E+06	0918
9060034	EP1C6	144 TQFP	125	77	1000	0		77000	4.40E+06	0925
10030015	EP1C6	144 TQFP	125	77	1000	0		77000	4.14E+06	1012
10030016	EP1C6	144 TQFP	125	77	1000	0		77000	4.14E+06	1012
10040015	EP1C6	144 TQFP	125	74	1000	0		74000	3.87E+06	1007
9060004	EP1C12	324 FBGA	125	75	1000	0		75000	4.12E+06	0919
10050013	EP1C12	324 FBGA	125	25	1000	0		25000	1.41E+06	1019
10050014	EP1C12	324 FBGA	125	25	1000	0		25000	1.41E+06	1019
10050015	EP1C12	324 FBGA	125	25	1000	0		25000	1.52E+06	1019
10100017	EP1C12	324 FBGA	125	77	1000	0		77000	5.85E+06	1037
11110022	EP1C20	324 FBGA	125	77	1000	0		77000	5.68E+06	1119
9030008	EP1S40	1020 FBGA	125	29	1058	0		30682	2.44E+06	0911
9030007	EP1S40	1508 FBGA	125	29	2027	0		58783	4.47E+06	0913
12010023	EP1S40	1508 FBGA	125	25	1000	0		25000	1.90E+06	1149
10030002	EP1S60	1020 FBGA	125	25	1000	0		25000	2.27E+06	1001
10070028	EP1S80	1020 FBGA	125	25	1000	0		25000	2.53E+06	1028
									8.00E+07	

Failure Mechanism	**# Fail**	**Chi Sq.**	**Equiv. Hrs**	**FITs**
Via voiding Failure(Ea=0.8)	0	1.83	8.00E+07	**11.4**

Note: Typical application Tj=70°C.

Stratix II, Stratix II GX, Cyclone II, Arria GX and HardCopy II - 90 nm Products

Stratix II, Stratix II GX, Cyclone II, Arria GX and HardCopy II products are fabricated on a 90 nm process technology that supports up to 9 layers of Cu metallization and Low-k with one layer of Salicided polysilicon. Stratix II and GX devices are available in FlipChip FBGA packages with logic density ranging from 6,240 to 71,760 ALMs and 419 Kbits to 9.4 Mbits of embedded RAM. Cyclone II devices are available in QFP, FBGA and UBGA packages with logic density ranging from 4,608 to 68,416 LEs and 119 Kbits to 1.1 Mbits of embedded RAM The Stratix II, Stratix II GX, Cyclone II, Arria GX and HardCopy II product families operate with a 1.2V supply and the lifetest is conducted at 1.44V, which is a 20% overvoltage. Lifetest was run at junction temperature of 125°C to keep it below absolute maximum ratings.

Stratix II, Stratix II GX, Cyclone II, Arria GX and HardCopy II - 90 nm Lifetest Results

REL LOT #	DEVICE	PACKAGE TYPE	Stress Tj (C)	# UNITS	L.T. HOURS	# FAIL		DEVICE HOURS	Interlayer EQUIV. HRS.	Date Code
10020010	EP2C8	256 FBGA	125	77	1000	0		77000	3.28E+06	1001
11030026	EP2C20	256 FBGA	125	77	1000	0		77000	3.28E+06	1049
9040021	EP2C35	672 FBGA	125	77	1006	0		77462	3.30E+06	0913
9100029	EP2C70	672 FBGA	125	25	1037	0		25925	1.10E+06	0942
10090028	EP2C70	672 FBGA	125	76	1049	0		79724	3.40E+06	1025
10100001	EP2S30	672 FBGA	125	24	1046	0		25104	1.07E+06	1039
9020005	EP2S90	1020 FBGA	125	25	2000	0		50000	2.13E+06	0901
9100003	EP2S90	1020 FBGA	125	25	1086	0		27150	1.16E+06	0937
10040020	EP2S90	1020 FBGA	125	28	1014	0		28392	1.21E+06	1013
11060011	EP2S90	1020 FBGA	125	25	1000	0		25000	1.06E+06	1125
9010010	EP2S130	1020 FBGA	125	25	1001	0		25025	1.07E+06	0901
9040029	EP2S130	1508 FBGA	125	24	1004	0		24096	1.03E+06	0913
11120011	EP2S130	1508 FBGA	125	25	1000	0		25000	1.06E+06	1119
9090024	EP2SGX90	1152 FBGA	125	25	1074	0		26850	1.14E+06	0931
									2.53E+07	
Failure Mechanism				**# Fail**	**Chi Sq.**			**Equiv. Hrs.**	**FITs**	
Interlayer Breakdown (Ea=0.7)				0	1.83			2.53E+07	**36.2**	
Note: Typical application Tj=70°C.										

Stratix III, Cyclone III and Cyclone IV- 65/60 nm Products

Stratix III, Cyclone III and Cyclone IV products are fabricated on a 65/60 nm process technology that supports up to 9 layers of Cu metallization and Low-k with one layer of Salicided polysilicon. Stratix III devices are available in FlipChip FBGA packages with logic density ranging from 47.5K to 337.5K LEs and 2,430 to 20,491 Kbits of total memory. Cyclone III and Cyclone IV devices are available in QFP, QFN, FBGA and UBGA packages with logic density ranging from 5,136 to 149,760 LEs and 414 to 6,480 Kbits of memory. The Stratix III product families operate with a 1.1V supply. Cyclone III and Cyclone IV product families operate with a 1.2V supply. Lifetest is conducted at 1.32V and 1.44V respectively, which is a 20% overvoltage. Lifetest uses dynamic life with a real clocked configuration and was run at junction temperature of 125°C to keep it below absolute maximum ratings.

Stratix III, Cyclone III and Cyclone IV - 65/60 nm Lifetest

REL LOT #	DEVICE	PACKAGE TYPE	Stress Tj (C)	# UNITS	L.T. HOURS	# FAIL		DEVICE HOURS	Interlayer EQUIV. HRS.	Date Code
10010012	EP3C5	144 EQFP	125	30	1033	0		30990	1.32E+06	1001
10040029	EP3C5	144 EQFP	125	78	1066	0		83148	3.54E+06	1016
10050001	EP3C16	144 EQFP	125	80	1010	0		80800	3.44E+06	1018
9090042	EP3C25	144 EQFP	125	77	1019	0		78463	3.34E+06	0931
10020005	EP3C25	144 EQFP	125	79	1004	0		79316	3.38E+06	1005
9050016	EP3C25	256 FBGA	125	77	1000	0		77000	3.28E+06	0913
9010016	EP3C120	780 FBGA	125	25	1061	0		26525	1.13E+06	0903
9090022	EP3C120*	780 FBGA	125	43	1001	0		43043	1.83E+06	0937
9090023	EP3C120*	780 FBGA	125	44	1001	0		44044	1.88E+06	0937
10030008	EP3C120*	780 FBGA	125	36	2000	0		72000	3.07E+06	1009
10030013	EP3C120*	780 FBGA	125	41	2012	0		82492	3.51E+06	1010
10100014	EP3C120*	780 FBGA	125	43	2014	0		86602	3.69E+06	1040
11040013	EP3C120*	780 FBGA	125	30	1002	0		30060	1.28E+06	1117
9070009	EP3CLS200*	780 FBGA	125	35	3004	0		105140	4.48E+06	0916
9070010	EP3CLS200*	780 FBGA	125	35	3004	0		105140	4.48E+06	0925
11070014	EP3SL50	780 FBGA	125	25	1000	0		25000	1.02E+06	1112
9040010	EP3SL110	1152 FBGA	125	25	1000	0		25000	1.02E+06	0912
10100010	EP3SL150	1152 FBGA	125	25	1000	0		25000	1.02E+06	1041
11100002	EP3SL150	1152 FBGA	125	25	1000	0		25000	1.02E+06	1119
9040015	EP3SL200	1152 FBGA	125	25	1001	0		25025	1.02E+06	0907
10080012	EP3SL200	1152 FBGA	125	25	1066	0		26650	1.09E+06	1019
11080004	EP3SL200	1152 FBGA	125	25	1000	0		25000	1.02E+06	1049
12010021	EP3SL200	1152 FBGA	125	25	1000	0		25000	1.02E+06	1146
10020043	EP4CGX15*	148 QFN	125	48	2000	0		96000	4.09E+06	1007
10080028	EP4CGX15*	148 QFN	125	77	1000	0		77000	3.28E+06	1025
11030010	EP4CGX15*	148 QFN	125	78	1000	0		78000	3.32E+06	1101
11100015	EP4CGX15*	148 QFN	125	77	2000	0		154000	6.56E+06	1131
* 60 nm Feature Size									**6.92E+07**	
Failure Mechanism				**# Fail**	**Chi Sq.**			**Equiv. Hrs.**	**FITs**	
Interlayer Breakdown (Ea=0.7)				0	1.83			6.92E+07	**13.3**	
Note: Typical application Tj=70°C.										

Stratix IV, Arria II GX and HardCopy III & IV - 40 nm Products

Stratix IV, Arria II GX and HardCopy III & IV products are fabricated on a 40 nm process technology that supports up to 11 layers of Cu metallization and one Al redistribution layer. Stratix IV and Arria II GX devices are available in FlipChip FBGA packages with up to 820K logic elements (LEs), 23.1 Mbits of embedded memory, and up to 1,288 18 x 18 multipliers. The Stratix IV, Arria II GX and HardCopy III & IV product families operate with a 0.9 V supply. Stratix IV lifetest is conducted at 1.1 x Vcc while Arria II and HardCopy III & IV lifetest is conducted at 1.2 x Vcc. Lifetest uses dynamic life with a real clocked configuration and was run at junction temperature of 125°C to keep it below absolute maximum ratings.

Stratix IV, Arria II GX and HardCopy III & IV - 40 nm Lifetest

REL LOT #	DEVICE	PACKAGE TYPE	Stress Tj (C)	# UNITS	L.T. HOURS	# FAIL		DEVICE HOURS	Dielectric EQUIV. HRS.	Via voiding Fail. EQUIV. HRS.	Interlayer EQUIV. HRS.	Date Code
9090041	EP4SGX230	1517 FBGA	125	27	2000	0		54000	6.43E+06	5.78E+06	1.74E+06	0938
9100001	EP4SGX230	1517 FBGA	125	30	1000	0		30000	3.57E+06	3.21E+06	9.66E+05	0939
9100005	EP4SGX230	1517 FBGA	125	30	2000	0		60000	7.15E+06	6.43E+06	1.93E+06	0940
10080001	EP4SGX230	1517 FBGA	125	11	1069	0		11759	1.40E+06	1.26E+06	3.79E+05	0950
9120003	EP4SGX290	1517 FBGA	125	27	2000	0		54000	6.43E+06	5.78E+06	1.74E+06	0946
10010020	EP4SGX530	1517 FBGA	125	29	2000	1	a	58000	6.91E+06	6.21E+06	1.87E+06	0952
10030004	EP4SGX530	1517 FBGA	125	46	2000	0		92000	1.10E+07	9.85E+06	2.96E+06	1008
10030036	EP4SGX530	1517 FBGA	125	36	2000	1	b	72000	8.58E+06	7.71E+06	2.32E+06	1012
10100018	EP4SGX530	1517 HBGA	125	31	1019	0		31589	3.76E+06	3.38E+06	1.02E+06	1026
10110013	EP4SGX530	1517 HBGA	125	28	2021	0		56588	6.74E+06	6.06E+06	1.82E+06	1026
10080027	EP2AGX65	358 UBGA	125	61	1000	0		61000	4.53E+07	6.53E+06	2.40E+06	1034
10090017	EP2AGX65	358 UBGA	125	60	1000	0		60000	4.46E+07	6.43E+06	2.36E+06	1037
10090018	EP2AGX65	358 UBGA	125	51	1000	0		51000	3.79E+07	5.46E+06	2.01E+06	1037
10090019	EP2AGX65	358 UBGA	125	65	168	0		10920	8.11E+06	1.17E+06	4.29E+05	1037
10100012	EP2AGX95	780 FBGA	125	12	1015	0		12180	9.05E+06	1.30E+06	4.79E+05	1040
10110012	EP2AGX125	780 FBGA	125	25	1048	0		26200	1.95E+07	2.81E+06	1.03E+06	1040
9120004	EP2AGX125	780 FBGA	125	27	1000	0		27000	2.01E+07	2.89E+06	1.06E+06	0940
10020045	EP2AGX260	780 FBGA	125	22	2000	0		44000	5.24E+06	4.71E+06	1.42E+06	1008
10060022	HC335	1152 FBGA	125	29	1000	0		29000	2.15E+07	3.11E+06	1.14E+06	1020
									2.73E+08	9.01E+07	2.91E+07	

Failure Mechanism	# Fail	Chi Sq.	Equiv. Hrs.	FITs
Via voiding Failure(Ea=1.0)	1	4.04	9.01E+07	**22.4**
Dielectric Breakdown*(1)	1	4.04	2.73E+08	**7.4**
Interlayer Breakdown (Ea=0.7)	0	1.83	2.91E+07	**31.5**
Combined Failure Rate				**61.4**

a- IPATPG reject at 2000 hours due to a faulty scan chain caused by a random defect. Suspect Via 1 failure.

b - CRAM min/max reject that is intermittent oxide failure at 500 hrs. Damaged during FA.

Note: Typical application Tj=70°C.

***(1) Using the Power-law TDDB model for thin-gate oxide**

ttf=to*V^-n*exp(Ea/kT)

n and Ea values are available upon request.

Stratix V - 28 nm Products

Stratix V products are fabricated on a TSMC 28 nm HP process technology. Stratix V devices are available in FlipChip FBGA packages with up to 952K logic elements (LEs). Stratix V product families operate with a 0.85 V supply and lifetest is conducted at 1.1 and 1.2 x Vcc. Lifetest uses dynamic life with a real clocked configuration and was run at junction temperature of 125°C to keep it below absolute maximum ratings.

Stratix V GX 28 nm Lifetest –Preliminary Results

REL LOT #	DEVICE	PACKAGE TYPE	Stress Tj (C)	Condition	# UNITS	L.T. HOURS	# FAIL	
11080015	5SGXA7	1517 FBGA	125	Dynamic @ 1.1x Vcc	25	1000	0	
11100001	5SGXA7	1517 FBGA	125	Dynamic @ 1.1x Vcc	31	1000	0	
11110005	5SGXA7	1517 FBGA	125	Dynamic @ 1.1x Vcc	28	1000	0	
11110008	5SGXA7	1517 FBGA	125	Dynamic @ 1.2x Vcc	29	2000	0	
12010001	5SGXA7	1517 FBGA	125	Dynamic @ 1.2x Vcc	25	1000	0	

Note: Due to limited number of lots tested up to date and ongoing qualification tests, a statistically significant FIT rate cannot be provided in this edition of Reliability Report. Altera's FIT rate goal is < 100 at Tj=70°C.

MAX 7000S and MAX 9000 - Third Generation

These MAX 7000 and MAX 9000 products are fabricated on a 0.5µ triple layer metal CMOS EEPROM process. Devices are available in logic densities from 32 to 560 macrocells and in PLCC, TQFP, PQFP, RQFP, and PGA packages. Lifetests are conducted at 6.0V, which is a 20% overvoltage.

Third Generation MAX 7000S & MAX 9000 Lifetest Results

REL LOT#	DEVICE	PACKAGE TYPE	TA	# UNITS	Life Test HOURS	# Fail		DEVICE HOURS	Data Retention Equiv Hrs.	Date Code
9040002	EPM7032S	44 PLCC	125	77	1055	0		81235	4.34E+06	0907
11040002	EPM7064S	44 PLCC	125	77	1000	0		77000	5.46E+06	1101
9100028	EPM7064S	44 TQFP	125	77	1000	0		77000	6.60E+06	0937
10040017	EPM7064S	44 TQFP	125	77	1000	0		77000	5.89E+06	1007
10060027	EPM7064S	44 TQFP	125	77	1000	0		77000	7.11E+06	1019
									2.94E+07	
Failure Mechanism				**# Fail**	**Chi Sq.**			**Equiv. Hrs.**	**FITs**	
Data retention failure				0	1.83			2.94E+07	**31.17**	

MAX 7000A and MAX 3000A - Fourth Generation

The MAX 7000A and MAX 3000A products are fabricated on a 0.3/0.35µ CMOS EEPROM process. This process supports up to four layers of metallization, which supports a 3.3V operating voltage. Devices are available in logic densities from 32 to 512 macrocells and in PLCC, TQFP, PQFP, BGA, and FBGA packages. Lifetest are conducted at 4.0V, which is a 20% overvoltage.

Fourth Generation MAX 7000A and MAX 3000A Lifetest Results

REL LOT#	DEVICE	PACKAGE TYPE	TA	# UNITS	L.T. HOURS	# Fail		DEVICE HOURS	Data Retention Equiv Hrs.	Date Code
11100003	EPM3064A	44 TQFP	125	77	1000	0		77000	7.49E+06	1125
9010009	EPM7064AE	100 TQFP	125	232	2000	0		464000	2.96E+07	0851
9010008	EPM7256AE	144 TQFP	125	274	1000	0		274000	1.84E+07	0851
10100013	EPM7512AE	208 PQFP	125	45	1000	0		45000	1.72E+06	1037
11070008	EPM7512AE	208 PQFP	125	45	1000	0		45000	1.72E+06	0919
9050031	EPM7512AE	256 FBGA	125	25	1000	0		25000	8.88E+05	0922
10030018	EPM7512AE	256 FBGA	125	25	1000	0		25000	7.48E+05	1001
									6.06E+07	
Failure Mechanism				**# Fail**	**Chi Sq.**			**Equiv. Hrs.**	**FITs**	
Data retention failure				0	1.83			6.06E+07	**15.1**	

MAX 7000B - Fifth Generation

These MAX 7000B products are fabricated on a 0.22µ quadruple layer metal CMOS EEPROM process. Devices are available in logic densities from 32 to 512 macrocells and in PLCC, TQFP, UBGA, PQFP & FBGA packages. Lifetests are conducted at 3.0V, which is a 20% overvoltage.

Fifth Generation MAX 7000 Lifetest Results

REL LOT#	DEVICE	PACKAGE TYPE	TA	# UNITS	L.T. HOURS	# Fail		DEVICE HOURS	Data Retention Equiv Hrs.	Date Code
8070001	EPM7256B	256 FBGA	125	25	1000	0		25000	3.90E+06	0819
9080001	EPM7256B	256 FBGA	125	25	1000	0		25000	3.90E+06	0919
10080013	EPM7512B	256 FBGA	125	25	1000	0		25000	8.36E+06	1025
11100018	EPM7512B	256 FBGA	125	25	1000	0		25000	8.36E+06	1137
									2.45E+07	
Failure Mechanism				**# Fail**	**Chi Sq.**			**Equiv. Hrs.**	**FITs**	
Data retention failure				0	1.83			2.45E+07	**37.4**	

MAX II, MAX V - 0.18 µm FLASH Products

These MAX II & V products are fabricated on an 8", 0.18um CMOS flash memory process technology. The MAX II &V family supports up to 6 layers of metal. Devices are available in logic densities from 240 to 2,210 LEs and in TQFP and FBGA packages. The operating supply voltage is 3.3V for the MAX II &V device and lifetests are conducted at 3.96V. The operating supply voltage is 1.8V for the MAX II G and MAX II Z devices and lifetests are conducted at 2.16V. Both are 20% overvoltage.

MAX II & V Lifetest Results

REL LOT #	DEVICE	PACKAGE TYPE	TA	# UNITS	L.T. HOURS	# FAIL		DEVICE HOURS	Data Retention EQUIV.HRS.	Date Code
9100012	EPM570	144 TQFP	125	77	1000	0		77000	5.55E+06	0937
9090007	EPM570	256 FBGA	125	75	1000	0		75000	3.36E+06	0931
9050008	EPM1270	144 TQFP	125	77	1000	0		77000	3.34E+06	0913
10030003	EPM1270	144 TQFP	125	77	1000	0		77000	3.34E+06	1001
10070001	EPM1270	144 TQFP	125	75	1000	0		75000	3.26E+06	1019
9020008	EPM2210	256 FBGA	125	76	1000	0		76000	3.82E+06	0901
10080014	EPM2210G	256 FBGA	125	25	1000	0		25000	1.05E+06	1032
9100011	EPM240Z	100 MBGA	125	77	1000	0		77000	2.85E+06	0925
10040030	EPM240Z	100 MBGA	125	77	1000	0		77000	2.85E+06	1017
11030013	EPM240Z	100 MBGA	125	77	2000	0		154000	3.62E+06	1101
11090026	5M570Z	144 TQFP	125	78	2000	0		156000	6.40E+06	1136
11120013	5M570Z	144 TQFP	125	80	2000	0		160000	6.57E+06	1131
11050006	5M1270Z	144 TQFP	125	75	2000	0		150000	4.00E+06	1118
11120012	5M1270Z	144 TQFP	125	80	2000	0		160000	4.27E+06	1143
11030028	5M1270Z	256 FBGA	125	73	2000	0		146000	4.22E+06	1107
11080001	5M2210Z	256 FBGA	125	80	1000	0		80000	3.35E+06	1130
									6.19E+07	
Failure Mechanism				**# Fail**	**Chi Sq.**			**Equiv. Hrs.**	**FITs**	
Data retention failure				0	1.83			6.19E+07	**14.8**	

Configuration Devices - EPROM

These Configuration EPROMs are fabricated on a 0.5µm double layer metal CMOS EPROM process. These devices are erasable with UV light when supplied in windowed hermetic packages for prototyping. Lifetests are conducted at least 6.0V, which is a minimum of 20% overvoltage.

Third Generation Classic and Configuration Devices Lifetest Results

REL LOT#	DEVICE	PACKAGE TYPE	TA	# UNITS	L.T. HOURS	# FAIL		DEVICE HOURS	C.L. Equiv. Hrs.	Date Code
9040001	EPC1	20 PLCC	125	77	1000	0		77000	3.70E+06	0907
11090028	EPC1	20 PLCC	125	77	1000	0		77000	3.70E+06	1127
9010014	EPC1441	20 PLCC	125	77	1000	0		77000	3.48E+06	0901
10020046	EPC1441	20 PLCC	125	77	1000	0		77000	3.63E+06	1001
12030019	EPC1441	20 PLCC	125	77	1000	0		77000	3.63E+06	1207
									1.81E+07	
Failure Mechanism				**# Fail**	**Chi Sq.**			**Equiv. Hrs.**	**FITs**	
Data retention failure				0	1.83			1.81E+07	50.5	

Configuration Devices – Flash Memory

The EPC2 configuration device is fabricated on a 0.4µ double layer metal CMOS Flash process. EPC4, EPC8 and EPC16 are stacked-die configuration devices in which the controller die is fabricated on a 0.35µ double layer metal CMOS logic process and the memory die is fabricated on 0.13µ triple layer metal CMOS Flash process. These devices are electrically erasable. Lifetests are conducted at least at 6.0V and 4.0V for EPC2 and EPC16 respectively, which is a minimum of 20% overvoltage.

Flash Memory Devices Lifetest Results

REL LOT#	DEVICE	PACKAGE TYPE	TA	# UNITS	L.T. HOURS	# FAIL		DEVICE HOURS	Data Retention Equiv. Hrs.	Date Code
9070002	EPC2	20 PLCC	125	76	1000	0		76000	1.30E+07	0919
10050020	EPC2	20 PLCC	125	77	1000	0		77000	1.84E+07	1013
10110001	EPC2	20 PLCC	125	77	1000	0		77000	1.84E+07	1037
11080010	EPC2	20 PLCC	125	77	1000	0		77000	1.84E+07	1113
12020028	EPC2	20 PLCC	125	77	1000	0		77000	1.84E+07	1204
10010008	EPC16	88 UBGA	125	77	1000	0		77000	1.29E+07	0949
10080009	EPC16	88 UBGA	125	78	1000	0		78000	1.33E+07	1019
									1.13E+08	
Failure Mechanism				**# Fail**	**Chi Sq.**			**Equiv. Hrs.**	**FITs**	
Data retention failure				0	1.83			1.13E+08	8.12	

High Temperature Storage

High temperature storage is performed at 150°C or greater. This stress detects bonding failures due to intermetallic formation in all product families and data retention failures in non-volatile memory elements. The ability of non-volatile memory elements to retain their charge is crucial for reliability. The leakage of charge off of the floating gate of a non-volatile configuration element can be measured by margin test modes built into every Altera device. Charge loss mechanisms in EPROMs and EEPROMs have been well documented in the literature. [v] [vi]

High Temperature Storage Results

REL LOT #	DEVICE	PACKAGE TYPE	BAKE TEMP.	# UNITS	STRESS HOURS	# FAIL		Technology	Date Code
11120013	5M570Z	144 TQFP	150	102	2000	0		0.18µ FLASH	1131
11090026	5M570Z	144 FBGA	150	102	2000	0		0.18µ FLASH	1136
11050006	5M1270Z	144 TQFP	150	102	2000	0		0.18µ FLASH	1118
11120012	5M1270Z	144 TQFP	150	102	2000	0		0.18µ FLASH	1143
11030028	5M1270Z	256 FBGA	150	102	1000	0		0.18µ FLASH	1107
11050011	5M1270Z	256 FBGA	150	37	2000	0		0.18µ FLASH	1118
11080001	5M2210Z	256 FBGA	150	102	2000	0		0.18µ FLASH	1130
11080020	5M2210Z	256 FBGA	150	30	2001	0		0.18µ FLASH	1134
11080021	5M2210Z	256 FBGA	150	30	2001	0		0.18µ FLASH	1134
11080022	5M2210Z	256 FBGA	150	29	2001	0		0.18µ FLASH	1134
12010017	5M2210Z	256 FBGA	150	77	2000	0		0.18µ FLASH	1201
11100001	5SGXA7	1517 FBGA	150	29	2983	0		28 nm SRAM	1135
11110002	5SGXA7	1517 FBGA	150	29	2697	0		28 nm SRAM	1136
11110009	5SGXA7	1517 FBGA	150	30	2086	0		28 nm SRAM	1136
11080016	5SGXA7	1517 FBGA	150	27	1042	0		28 nm SRAM	1127
11110006	5SGXA7	1517 FBGA	150	30	2675	0		28 nm SRAM	1136
11060013	EP1C3	144 TQFP	150	77	1000	0		0.13µ SRAM	1137
10030015	EP1C6	144 TQFP	150	77	2000	0		0.13µ SRAM	1012
10030016	EP1C6	144 TQFP	150	77	2000	0		0.13µ SRAM	1012
10040015	EP1C6	144 TQFP	150	77	2000	0		0.13µ SRAM	1007
10050015	EP1C12	324 FBGA	150	25	1000	0		0.13µ SRAM	1019
10100017	EP1C12	324 FBGA	150	77	1000	0		0.13µ SRAM	1037
11110022	EP1C20	324 FBGA	150	77	2000	0		0.13µ SRAM	1119
10090006	EP1K50	256 FBGA	150	25	2000	0		0.22µ SRAM	1031
9030006	EP1S10	672 FBGA	150	25	2004	0		0.13µ SRAM	0907
9030017	EP1S25	672 FBGA	150	24	2000	0		0.13µ SRAM	0912
11030011	EP1S40	1508 FBGA	150	25	1000	0		0.13µ SRAM	1001
10070028	EP1S80	1020 FBGA	150	17	2000	0		0.13µ SRAM	1028
11040003	EP20K300E	672 FBGA	150	25	1000	0		0.18µ SRAM	1115
10090008	EP20K400C	672 FBGA	150	25	1000	0		0.15µ SRAM	1031
9020002	EP20K400C	672 FBGA	150	25	2000	0		0.15µ SRAM	0901
11050015	EP20K400C	672 FBGA	150	25	1000	0		0.15µ SRAM	1121
10100015	EP2AGX65	358 UBGA	150	25	2000	0		40 nm SRAM	1039
11120001	EP2AGX190	780 FBGA	150	25	1005	0		40 nm SRAM	1131
10030009	EP2AGX260	780 FBGA	150	25	2050	0		40 nm SRAM	0910
10020010	EP2C8	256 FBGA	150	77	2000	0		0.09µ SRAM	1001
11030026	EP2C20	256 FBGA	150	77	1000	0		0.09µ SRAM	1049
10090028	EP2C70	672 FBGA	150	77	2000	0		0.09µ SRAM	1025
11100005	EP2C70	672 FBGA	150	77	2000	0		0.09µ SRAM	1119
10090025	EP2S30	484 FBGA	150	25	1000	0		0.09µ SRAM	1039
10100001	EP2S30	672 FBGA	150	25	1576	0		0.09µ SRAM	1039

REL LOT #	DEVICE	PACKAGE TYPE	BAKE TEMP.	# UNITS	STRESS HOURS	# FAIL		Technology	Date Code
10040020	EP2S90	1020 FBGA	150	25	2000	0		0.09µ SRAM	1013
11060011	EP2S90	1020 FBGA	150	25	1000	0		0.09µ SRAM	1125
11120011	EP2S130	1508 FBGA	150	25	2000	0		0.09µ SRAM	1119
10010012	EP3C5	144 EQFP	150	45	1000	0		65 nm SRAM	1001
10040029	EP3C5	144 EQFP	150	45	1000	0		65 nm SRAM	1016
10050001	EP3C16	144 EQFP	150	45	1000	0		60 nm SRAM	1018
10040009	EP3C16	240 PQFP	150	25	1000	0		65 nm SRAM	1014
11040006	EP3C16	144 EQFP	150	30	1000	0		60 nm SRAM	1116
10040008	EP3C25	240 PQFP	150	25	1000	0		65 nm SRAM	1014
11060006	EP3C40	240 PQFP	150	76	1000	0		60 nm SRAM	1113
10090012	EP3C55	484 UBGA	150	25	1000	0		60 nm SRAM	1031
10050021	EP3C55	780 FBGA	150	25	2000	0		60 nm SRAM	1013
10010022	EP3C80	484 UBGA	150	25	2000	0		65 nm SRAM	1003
10070020	EP3C80	484 UBGA	150	25	2000	0		60 nm SRAM	1019
11070010	EP3C120	780 FBGA	150	25	1502	0		60 nm SRAM	1126
11040010	EP3C120	780 FBGA	150	30	1000	0		60 nm SRAM	1117
11040013	EP3C120	780 FBGA	150	30	1000	0		60 nm SRAM	1117
9070009	EP3CLS200	780 FBGA	150	45	3007	0		60 nm SRAM	0916
9070010	EP3CLS200	780 FBGA	150	45	3003	0		60 nm SRAM	0925
11030015	EP3SE50	780 FBGA	150	25	1000	0		65 nm SRAM	1043
11070014	EP3SL50	780 FBGA	150	25	1000	0		65 nm SRAM	1112
10070023	EP3SL150	1152 FBGA	150	25	2000	0		65 nm SRAM	1027
11100002	EP3SL150	1152 FBGA	150	25	2000	0		65 nm SRAM	1119
10080012	EP3SL200	1152 FBGA	150	25	1500	0		65 nm SRAM	1019
11080004	EP3SL200	1152 FBGA	150	25	1000	0		65 nm SRAM	1049
12010021	EP3SL200	1152 FBGA	150	25	2000	0		65 nm SRAM	1146
10080028	EP4CGX15	148 QFN	150	77	1000	0		60 nm SRAM	1025
11030010	EP4CGX15	148 QFN	150	73	1000	0		60 nm SRAM	1101
11100015	EP4CGX15	148 QFN	150	77	2000	0		60 nm SRAM	1131
10070022	EP4CGX150	896 FBGA	150	30	2000	0		60 nm SRAM	1028
10090024	EP4CGX150	896 FBGA	150	25	1000	0		60 nm SRAM	1038
11070025	EP4CGX150	896 FBGA	150	77	1000	0		60 nm SRAM	1119
11030012	EP4SGX230	1517 FBGA	150	23	2014	0		40 nm SRAM	1108
11120033	EP4SGX230	1517 FBGA	150	25	2058	0		40 nm SRAM	1137
10080018	EP4SGX530	1517 HBGA	150	40	2088	0		40 nm SRAM	1027
10020046	EPC1441	20 PLCC	150	45	2000	0		0.5µ EPROM	1001
11090028	EPC1	20 PLCC	150	45	2000	0		0.5µ EPROM	1127
10050020	EPC2	20 PLCC	150	45	2000	0		0.4µ FLASH	1013
11080010	EPC2	20 PLCC	150	45	2000	0		0.4µ FLASH	1113
10070002	EPC4	100 PQFP	150	45	2000	0		0.35µ FLASH	1013
10010008	EPC16	88 UBGA	150	45	2000	0		0.35µ FLASH	0949
10030001	EPF10K50A	240 RQFP	150	25	1000	0		0.3µ SRAM	1008
10050019	EPF10K50S	256 FBGA	150	25	2000	0		0.22µ SRAM	1018
10040004	EPF10K70R	240 RQFP	150	25	2000	0		0.42µ SRAM	1013
10020042	EPF10K100A	240 RQFP	150	25	1000	0		0.3µ SRAM	1001
10040033	EPF10K100A	240 RQFP	150	25	2000	0		0.3µ SRAM	1016
9050030	EPF10K100E	256 FBGA	150	25	2017	0		0.22µ SRAM	0922
9030019	EPF10K130E	240 PQFP	150	25	1000	0		0.22µ SRAM	0913
10040030	EPM240Z	100 MBGA	150	77	2000	0		0.18µ FLASH	1017
11030013	EPM240Z	100 MBGA	150	101	1000	0		0.18µ FLASH	1101
10020013	EPM570	100 TQFP	150	77	2000	0		0.18µ FLASH	1001
10070003	EPM570	100 TQFP	150	76	2000	0		0.18µ FLASH	1013
9090007	EPM570	256 FBGA	150	45	2000	0		0.18µ FLASH	0931

REL LOT #	DEVICE	PACKAGE TYPE	BAKE TEMP.	# UNITS	STRESS HOURS	# FAIL		Technology	Date Code
9050008	EPM1270	144 TQFP	150	77	2000	0		0.18µ FLASH	0913
10080014	EPM2210G	256 FBGA	150	25	1000	0		0.18µ FLASH	1032
11100003	EPM3064A	44 TQFP	150	45	2000	0		0.35µ EEPROM	1125
11040002	EPM7064	44 PLCC	150	45	1000	0		0.5µ EEPROM	1101
9010009	EPM7064AE	100 TQFP	150	45	2000	0		0.3µ EEPROM	0851
10040017	EPM7064S	44 TQFP	150	45	2000	0		0.5µ EEPROM	1007
10030018	EPM7256AE	256 FBGA	150	25	2000	0		0.35µ EEPROM	1001
11100018	EPM7256B	256 FBGA	150	25	2000	0		0.22µ EEPROM	1137
10100013	EPM7512AE	208 PQFP	150	25	2000	0		0.35µ EEPROM	1037
11070008	EPM7512AE	208 PQFP	150	25	1000	0		0.35µ EEPROM	1119
10080013	EPM7512B	256 FBGA	150	25	1000	0		0.22µ EEPROM	1025
10020024	HC335	1517 FBGA	150	28	2002	0		40 nm SRAM	0949

Reflow Simulation and Moisture Preconditioning

Surface mount devices are subject to failure due to entrapped moisture that can rapidly expand during the reflow soldering process. [vii] [viii] Whereas dual in-line package devices are shielded from the rapid heat excursion of wave soldering by the printed circuit board, surface mount devices receive the full temperature shock of reflow soldering. Reflow soldering can be accomplished by Vapor Phase Soldering, Infrared Reflow Soldering, or Convection Reflow Soldering. Altera's reflow recommendations are contained in Application Note 81 for tin-lead soldering and Application Note 353 for lead-free soldering. Reflow soldering typically has a preheat stage and then rapidly heats the device above the solder reflow temperature. Altera moisture soaks devices according to their J-STD020D moisture classification and then passes them through simulated 100% convention reflow soldering 3 times. For the conventional tin-lead reflow, Altera uses a prebake cycle above 150°C for 2 minutes, a temperature ramp of 1°-3° C / second, time above 183°C of at least 1 minute, and a peak temperature of 220°C for large packages and 235°C for packages $\leq 350mm^3$. For lead free/ROHS Compliant reflow, Altera preheats the devices at temperature between 150°-200°C for 90 seconds, a temperature ramp of 2°-2.5°C / second, time above 217°C for 115 seconds, and a peak temperature between 245°-260° C suitable for the package size according to J-STD-020D standard. Devices are examined for package cracks and electrically tested after preconditioning and reflow soldering. The devices are then subjected to Temperature Cycle Condition B or Temperature Humidity Bias to assess reliability. The moisture preconditioning stress level is listed in the Temperature Cycling and Temperature/Humidity Bias tables for those devices that were subjected to moisture preconditioning. The moisture classification of Altera products is imprinted on the device's moisture barrier bag.

Accelerated Moisture Resistance

Four different stresses are commonly used to assess moisture resistance of integrated circuits: Temperature Humidity Bias (THB) at 85°C/85%RH, Autoclave at 121°C/100%RH, Biased HAST at 130°C/85%RH and Unbiased HAST at 130°C/85%RH. All four stresses can detect metallization corrosion and moisture induced charge loss in nonvolatile devices. In addition, THB and biased HAST can detect galvanic corrosion since they are biased. Per JESD47F recommendation, BGA packages will no longer be subjected to Autoclave testing. Unbiased HAST will be used instead.

Autoclave

The Autoclave stress subjects semiconductor devices to a 121°C saturated DI water steam environment. At 121°C in a sealed vessel this results in a 15 PSIG pressure, or two atmospheres. The chamber used by Altera uses temperature to control the stress environment. Using pressure to control the environment as in a pressure pot, results in drastic swings in temperature as steam is vented outside the chamber. The autoclave stress is designed to detect corrosion of the metallization of integrated circuits. This test can also detect charge loss in non-volatile memory elements due to increased leakage if moisture reaches the floating gate storage element. [ix]

Unbiased HAST

In this stress devices are placed in a HAST chamber at 130°C/85%RH. The test does not subject the devices to a saturated moisture environment and there is no water condensed on the devices.

Autoclave & Unbiased HAST Results

REL LOT #	DEVICE	PACKAGE TYPE	RELIABILITY TEST	# UNITS	STRESS HOURS	# FAIL		Technology	Date Code
12020024	5M240Z	144 TQFP	PRECON 3- 130°C/85% RH	77	192	0		0.18µ FLASH	1201
11090026	5M570Z	144 FBGA	PRECON 3- 130°C/85% RH	80	96	0		0.18µ FLASH	1136
11120013	5M570Z	144 TQFP	PRECON 3- 130°C/85% RH	80	96	0		0.18µ FLASH	1131
11050006	5M1270Z	144 TQFP	PRECON 3- 130°C/85% RH	77	96	0		0.18µ FLASH	1118
11120012	5M1270Z	144 TQFP	PRECON 3- 130°C/85% RH	80	96	0		0.18µ FLASH	1143
11030028	5M1270Z	256 FBGA	PRECON 3- 130°C/85% RH	77	96	0		0.18µ FLASH	1107
11050011	5M1270Z	256 FBGA	PRECON 3- 130°C/85% RH	77	96	0		0.18µ FLASH	1118
11080001	5M2210Z	256 FBGA	PRECON 3- 130°C/85% RH	80	96	0		0.18µ FLASH	1130
11080022	5M2210Z	256 FBGA	PRECON 3- 130°C/85% RH	80	192	0		0.18µ FLASH	1134
12010017	5M2210Z	256 FBGA	PRECON 3- 130°C/85% RH	77	192	0		0.18µ FLASH	1201
11060002	5SGXA7	1517 FBGA	PRECON 4- 130°C/85% RH	20	96	0		28 nm SRAM	1122
12020026	5SGXA7	1760 FBGA	PRECON 4- 130°C/85% RH	30	192	0		28 nm SRAM	1202
11090002	5SGXA7	1932 FBGA	PRECON 4- 130°C/85% RH	25	192	0		28 nm SRAM	1135
10050024	EP1C3	100 TQFP	PRECON 3- 130°C/85% RH	25	96	0		0.13µ SRAM	1020
11060013	EP1C3	144 TQFP	PRECON 3- 130°C/85% RH	77	96	0		0.13µ SRAM	1137
10040015	EP1C6	144 TQFP	PRECON 3- 121°C/100% RH	77	96	0		0.13µ SRAM	1007
12010023	EP1S40	1508 FBGA	PRECON 3- 130°C/85% RH	25	96	0		0.13µ SRAM	1149
10070028	EP1S80	1020 FBGA	PRECON 3- 130°C/85% RH	25	96	0		0.13µ SRAM	1028
10090021	EP1S80	1020 FBGA	PRECON 4- 130°C/85% RH	25	96	0		0.13µ SRAM	1036
10090022	EP1S80	1508 FBGA	PRECON 4- 130°C/85% RH	25	96	0		0.13µ SRAM	1036

REL LOT #	DEVICE	PACKAGE TYPE	RELIABILITY TEST	# UNITS	STRESS HOURS	# FAIL		Technology	Date Code
9110032	EP1SGX25	1020 FBGA	PRECON 3- 130°C/85% RH	25	96	0		0.13µ SRAM	0943
11100016	EP20K100	208 PQFP	PRECON 3- 130°C/85% RH	25	96	0		0.22µ SRAM	1119
10120025	EP20K200	356 BGA	PRECON 3- 130°C/85% RH	25	96	0		0.22µ SRAM	1037
10010021	EP20K100E	144 TQFP	PRECON 3- 121°C/100% RH	25	96	0		0.18µ SRAM	1001
12020014	EP20K100E	240 PQFP	PRECON 3- 130°C/85% RH	25	96	0		0.18µ SRAM	1125
11080018	EP20K160E	356 BGA	PRECON 3- 130°C/85% RH	25	96	0		0.18µ SRAM	1101
10040002	EP20K200E	208 PQFP	PRECON 3- 121°C/100% RH	25	96	0		0.18µ SRAM	1007
11040003	EP20K300E	672 FBGA	PRECON 3- 130°C/85% RH	28	96	0		0.18µ SRAM	1115
10090008	EP20K400C	672 FBGA	PRECON 3- 130°C/85% RH	25	96	0		0.15µ SRAM	1031
11050015	EP20K400C	672 FBGA	PRECON 3- 130°C/85% RH	25	96	0		0.15µ SRAM	1121
10030006	EP2AGX65	358 UBGA	PRECON 3- 130°C/85% RH	25	96	0		40 nm SRAM	1003
10100015	EP2AGX65	358 UBGA	PRECON 3- 130°C/85% RH	25	96	0		40 nm SRAM	1039
9100021	EP2AGX65	780 FBGA	PRECON 3- 130°C/85% RH	25	192	0		40 nm SRAM	0942
10070038	EP2AGX125	1152 FBGA	PRECON 3- 130°C/85% RH	27	192	0		40 nm SRAM	1027
11120001	EP2AGX190	780 FBGA	PRECON 3- 130°C/85% RH	24	192	0		40 nm SRAM	1131
10050026	EP2AGX260	1152 FBGA	PRECON 3- 130°C/85% RH	30	192	0		40 nm SRAM	1020
10020010	EP2C8	256 FBGA	PRECON 3- 130°C/85% RH	77	96	0		0.09µ SRAM	1001
11060014	EP2C8	256 FBGA	PRECON 3- 130°C/85% RH	25	96	0		0.09µ SRAM	1126
11030026	EP2C20	256 FBGA	PRECON 3- 130°C/85% RH	77	96	0		0.09µ SRAM	1049
11100005	EP2C70	672 FBGA	PRECON 3- 130°C/85% RH	77	96	0		0.09µ SRAM	1119
10060019	EP2C70	896 FBGA	PRECON 3- 130°C/85% RH	25	96	0		0.09µ SRAM	1023
10090025	EP2S30	484 FBGA	PRECON 3- 130°C/85% RH	25	96	0		0.09µ SRAM	1039
10100001	EP2S30	672 FBGA	PRECON 3- 130°C/85% RH	25	192	0		0.09µ SRAM	1039
10040020	EP2S90	1020 FBGA	PRECON 3- 130°C/85% RH	25	96	0		0.09µ SRAM	1013
11060011	EP2S90	1020 FBGA	PRECON 3- 130°C/85% RH	25	96	0		0.09µ SRAM	1125
11120011	EP2S130	1508 FBGA	PRECON 3- 130°C/85% RH	25	96	0		0.09µ SRAM	1119
10110015	EP2S180	1020 FBGA	PRECON 3- 130°C/85% RH	25	96	0		0.09µ SRAM	1044
10110006	EP2S180	1508 FBGA	PRECON 4- 130°C/85% RH	25	96	0		0.09µ SRAM	1037
9090024	EP2SGX90	1152 FBGA	PRECON 3- 130°C/85% RH	25	96	0		0.09µ SRAM	0931
10010012	EP3C5	144 EQFP	PRECON 3- 121°C/100% RH	80	96	0		65 nm SRAM	1001
10040029	EP3C5	144 EQFP	PRECON 3- 130°C/85% RH	80	96	0		65 nm SRAM	1016
11040006	EP3C16	144 EQFP	PRECON 3- 130°C/85% RH	78	96	0		60 nm SRAM	1116
10040009	EP3C16	240 PQFP	PRECON 3- 130°C/85% RH	25	96	0		65 nm SRAM	1014
10050017	EP3C25	144 EQFP	PRECON 3- 130°C/85% RH	80	96	0		65 nm SRAM	1019
10040008	EP3C25	240 PQFP	PRECON 3- 130°C/85% RH	25	96	0		65 nm SRAM	1014
10060018	EP3C25	256 FBGA	PRECON 3- 130°C/85% RH	79	96	0		60 nm SRAM	1019
10040010	EP3C40	240 PQFP	PRECON 3- 130°C/85% RH	25	96	0		65 nm SRAM	1014
11080002	EP3C40	240 PQFP	PRECON 3- 130°C/85% RH	77	96	0		60 nm SRAM	1119
10060015	EP3C40	484 FBGA	PRECON 3- 130°C/85% RH	25	96	0		60 nm SRAM	1021
10120003	EP3C55	484 UBGA	PRECON 3- 130°C/85% RH	25	192	0		60 nm SRAM	1031
10110024	EP3C55	780 FBGA	PRECON 3- 130°C/85% RH	25	96	0		60 nm SRAM	1046
11040001	EP3C80	484 UBGA	PRECON 3- 130°C/85% RH	80	96	0		60 nm SRAM	1127
11050010	EP3C80	484 UBGA	PRECON 3- 130°C/85% RH	78	96	0		60 nm SRAM	1101

REL LOT #	DEVICE	PACKAGE TYPE	RELIABILITY TEST	# UNITS	STRESS HOURS	# FAIL		Technology	Date Code
11040010	EP3C120	780 FBGA	PRECON 3- 130°C/85% RH	77	96	0		60 nm SRAM	1117
11040013	EP3C120	780 FBGA	PRECON 3- 130°C/85% RH	77	96	0		60 nm SRAM	1117
11060010	EP3C120	780 FBGA	PRECON 3- 130°C/85% RH	30	96	0		60 nm SRAM	1124
9070009	EP3CLS200	780 FBGA	PRECON 3- 130°C/85% RH	28	192	0		60 nm SRAM	0916
9070010	EP3CLS200	780 FBGA	PRECON 3- 130°C/85% RH	32	192	0		60 nm SRAM	0925
11030015	EP3SE50	780 FBGA	PRECON 3- 130°C/85% RH	25	96	0		65 nm SRAM	1043
11070014	EP3SL50	780 FBGA	PRECON 3- 130°C/85% RH	25	96	0		65 nm SRAM	1112
10070021	EP3SL150	780 FBGA	PRECON 3- 130°C/85% RH	25	192	0		65 nm SRAM	1027
10100010	EP3SL150	1152 FBGA	PRECON 3- 130°C/85% RH	25	96	0		65 nm SRAM	1041
11100002	EP3SL150	1152 FBGA	PRECON 3- 130°C/85% RH	25	96	0		65 nm SRAM	1119
11080004	EP3SL200	1152 FBGA	PRECON 3- 130°C/85% RH	25	96	0		65 nm SRAM	1049
12010021	EP3SL200	1152 FBGA	PRECON 3- 130°C/85% RH	25	96	0		65 nm SRAM	1146
10040014	EP4CE40	484 FBGA	PRECON 3- 130°C/85% RH	25	96	0		60 nm SRAM	1014
11050008	EP4CGX15	148 QFN	PRECON 3- 130°C/85% RH	80	96	0		60 nm SRAM	1119
11100015	EP4CGX15	148 QFN	PRECON 3- 130°C/85% RH	77	96	0		60 nm SRAM	1131
10060001	EP4CGX15	169 FBGA	PRECON 3- 130°C/85% RH	25	96	0		60 nm SRAM	1022
10060002	EP4CGX15	169 FBGA	PRECON 3- 130°C/85% RH	25	96	0		60 nm SRAM	1022
11070025	EP4CGX150	896 PBGA	PRECON 3- 130°C/85% RH	77	96	0		60 nm SRAM	1119
10020008	EP4SGX230	1517 FBGA	PRECON 3- 130°C/85% RH	25	192	0		40 nm SRAM	1005
10090005	EP4SGX230	1517 FBGA	PRECON 3- 130°C/85% RH	25	192	0		40 nm SRAM	1005
11030012	EP4SGX230	1517 FBGA	PRECON 3- 130°C/85% RH	25	96	0		40 nm SRAM	1108
11120033	EP4SGX230	1517 FBGA	PRECON 3- 130°C/85% RH	22	192	0		40 nm SRAM	1137
11010001	EP4SGX530	1517 HBGA	PRECON 4- 130°C/85% RH	25	192	0		40 nm SRAM	1101
10090001	EP4SGX530	1932 FBGA	PRECON 3- 130°C/85% RH	38	192	0		40 nm SRAM	1030
11090028	EPC1	20 PLCC	PRECON 3- 130°C/85% RH	45	96	0		0.5µ EPROM	1127
9070011	EPC1	8 PDIP	PRECON 1- 121°C/100% RH	45	96	0		0.5µ EPROM	0929
12030019	EPC1441	20 PLCC	PRECON 3- 130°C/85% RH	45	96	0		0.5µ EPROM	1207
11120037	EPC16	100 PQFP	PRECON 3- 130°C/85% RH	45	96	0		0.35µ FLASH	1142
10010008	EPC16	88 UBGA	PRECON 3- 130°C/85% RH	45	96	0		0.35µ FLASH	0949
11080010	EPC2	20 PLCC	PRECON 3- 130°C/85% RH	45	96	0		0.4µ FLASH	1113
12020028	EPC2	20 PLCC	PRECON 3- 130°C/85% RH	45	96	0		0.4µ FLASH	1204
10070002	EPC4	100 PQFP	PRECON 3- 121°C/100% RH	45	96	0		0.35µ FLASH	1013
9020001	EPF10K10	208 PQFP	PRECON 3- 121°C/100% RH	25	96	0		0.42µ SRAM	0901
9050032	EPF10K20	144 TQFP	PRECON 3- 121°C/100% RH	25	168	0		0.42µ SRAM	0922
10080023	EPF10K30A	144 TQFP	PRECON 3- 121°C/100% RH	25	96	0		0.3µ SRAM	1019
10030001	EPF10K50	240 RQFP	PRECON 3- 121°C/100% RH	25	168	0		0.42µ SRAM	1008
9120008	EPF10K50E	144 TQFP	PRECON 3- 121°C/100% RH	25	96	0		0.22µ SRAM	0943
11040014	EPF10K70	240 RQFP	PRECON 3- 130°C/85% RH	25	96	0		0.42µ SRAM	1107
12030028	EPF10K100E	208 PQFP	PRECON 3- 130°C/85% RH	25	96	0		0.22µ SRAM	1143
9060024	EPF10K130E	240 PQFP	PRECON 3- 121°C/100% RH	25	168	0		0.22µ SRAM	0925
11030014	EPF6016	208 PQFP	PRECON 3- 130°C/85% RH	25	96	0		0.42µ SRAM	1101
9080008	EPF6016A	144 TQFP	PRECON 3- 121°C/100% RH	25	96	0		0.3µ SRAM	0932
9070001	EPF8282A	84 PLCC	PRECON 3- 121°C/100% RH	45	96	0		0.42µ SRAM	0919
12030003	EPM240	100 TQFP	PRECON 3- 130°C/85% RH	65	192	0		0.18µ FLASH	1207
11030013	EPM240Z	100 MBGA	PRECON 3- 130°C/85% RH	77	96	0		0.18µ FLASH	1101

REL LOT #	DEVICE	PACKAGE TYPE	RELIABILITY TEST	# UNITS	STRESS HOURS	# FAIL		Technology	Date Code
11070012	EPM570	100 TQFP	PRECON 3- 130°C/85% RH	78	96	0		0.18µ FLASH	1128
10080014	EPM2210G	256 FBGA	PRECON 3- 130°C/85% RH	25	96	0		0.18µ FLASH	1032
11100003	EPM3064A	44 TQFP	PRECON 3- 130°C/85% RH	45	96	0		0.35µ EEPROM	1125
11040002	EPM7064	44 PLCC	PRECON 3- 130°C/85% RH	45	96	0		0.5µ EEPROM	1101
9010009	EPM7064AE	100 TQFP	PRECON 3- 121°C/100% RH	45	96	0		0.3µ EEPROM	0901
10040017	EPM7064S	44 TQFP	PRECON 3- 121°C/100% RH	45	96	0		0.5µ EEPROM	1007
10100013	EPM7512AE	208 PQFP	PRECON 3- 121°C/100% RH	25	96	0		0.3µ EEPROM	1037
11070008	EPM7512AE	208 PQFP	PRECON 3- 130°C/85% RH	25	96	0		0.35µ EEPROM	1119

Temperature Humidity Bias

THB testing is commonly performed at 85°C/85%RH in order to keep condensation from forming on the devices under test. Voltage is applied to the devices under stress, but power consumption is kept low or cycled on and off to keep internal power dissipation from driving off moisture. Typical stress times are 1000 to 2000 hours, with 1000 hours used for qualification. An all stainless steel chamber and deionized (DI) water are used to ensure that contamination does not affect the results.

The chamber is loaded, then brought up to temperature, and finally humidity is applied to ensure no condensation occurs. When the chamber reaches temperature/humidity equilibrium, voltage is applied to the device under stress. The chamber is powered down in the following order to again ensure condensation does not occur: voltage to the device, humidity, and finally temperature. Devices are tested to datasheet parameters after 500, 1000, 1500, and 2000 hours of stress. Surface mount devices are subjected to moisture preconditioning and simulated 3 times through Convention Reflow Soldering before starting the THB stress. The JEDEC level of moisture preconditioning is listed in the table below.

Temperature Humidity Bias Results

REL LOT #	DEVICE	PACKAGE TYPE	RELIABILITY TEST	# UNITS	STRESS HOURS	# FAIL		Technology	Date Code
11060002	5SGXA7	1517 FBGA	PRECON 4-85/85THB	25	1000	0		28 nm SRAM	1122
11090002	5SGXA7	1932 FBGA	PRECON 4-85/85THB	23	1000	0		28 nm SRAM	1136
11110038	5SGXA7	1517 FBGA	PRECON 4-85/85THB	30	1000	0		28 nm SRAM	1110
9030005	EP1S40	1020 FBGA	PRECON 3-85/85THB	25	1000	0		0.13µ SRAM	0908
11030011	EP1S40	1508 FBGA	PRECON 3-85/85THB	25	1000	0		0.13µ SRAM	1001
12010023	EP1S40	1508 FBGA	PRECON 3-85/85THB	25	1000	0		0.13µ SRAM	1149
10070028	EP1S80	1020 FBGA	PRECON 3-85/85THB	25	1000	0		0.13µ SRAM	1028
11080018	EP20K160E	356 BGA	PRECON 3-85/85THB	25	1000	0		0.18µ SRAM	1101
10090008	EP20K400C	672 FBGA	PRECON 3-85/85THB	25	1000	0		0.15µ SRAM	1031
11050015	EP20K400C	672 FBGA	PRECON 3-85/85THB	25	1000	0		0.15µ SRAM	1121
9060011	EP20K400E	672 FBGA	PRECON 3-85/85THB	25	1000	0		0.18µ SRAM	0919
10040006	EP2AGX65	358 UBGA	PRECON 3-85/85THB	35	1000	0		40 nm SRAM	1011
10040007	EP2AGX65	358 UBGA	PRECON 3-85/85THB	35	1000	0		40 nm SRAM	1011
10070038	EP2AGX125	1152 FBGA	PRECON 3-85/85THB	27	2000	0		40 nm SRAM	1027
10050026	EP2AGX260	1152 FBGA	PRECON 3-85/85THB	32	1000	0		40 nm SRAM	1020
10120006	EP2AGX260	1152 FBGA	PRECON 3-85/85THB	25	1000	0		40 nm SRAM	1049
10020010	EP2C8	256 FBGA	PRECON 3-85/85THB	25	1000	0		0.09µ SRAM	1001
11080019	EP2C20	256 FBGA	PRECON 3-85/85THB	77	1000	0		0.09µ SRAM	1107
9040021	EP2C35	672 FBGA	PRECON 3-85/85THB	25	1000	0		0.09µ SRAM	0913
11100005	EP2C70	672 FBGA	PRECON 3-85/85THB	25	1000	0		0.09µ SRAM	1119
10040020	EP2S90	1020 FBGA	PRECON 3-85/85THB	25	1000	0		0.09µ SRAM	1013
11060011	EP2S90	1020 FBGA	PRECON 3-85/85THB	25	1000	0		0.09µ SRAM	1125
11030025	EP2S130	1508 FBGA	PRECON 3-85/85THB	25	1000	0		0.09µ SRAM	1011
10110006	EP2S180	1508 FBGA	PRECON 4-85/85THB	25	1000	0		0.09µ SRAM	1037
10040029	EP3C5	144 EQFP	PRECON 3-85/85THB	80	1000	0		65 nm SRAM	1016
11090017	EP3C10	256 FBGA	PRECON 3-85/85THB	22	1000	0		60 nm SRAM	1130
10050001	EP3C16	144 EQFP	PRECON 3-85/85THB	79	1000	0		60 nm SRAM	1018

REL LOT #	DEVICE	PACKAGE TYPE	RELIABILITY TEST	# UNITS	STRESS HOURS	# FAIL		Technology	Date Code
11040006	EP3C16	144 EQFP	PRECON 3-85/85THB	78	1000	0		60 nm SRAM	1116
10040009	EP3C16	240 PQFP	PRECON 3-85/85THB	24	1000	0		65 nm SRAM	1014
10040008	EP3C25	240 PQFP	PRECON 3-85/85THB	30	1000	0		65 nm SRAM	1014
9020007	EP3C25	256 FBGA	PRECON 3-85/85THB	77	1020	0		65 nm SRAM	0906
11060006	EP3C40	240 PQFP	PRECON 3-85/85THB	77	1000	0		60 nm SRAM	1113
10110024	EP3C55	780 FBGA	PRECON 3-85/85THB	25	1000	0		60 nm SRAM	1046
11050010	EP3C80	484 UBGA	PRECON 3-85/85THB	90	1000	0		60 nm SRAM	1101
11040001	EP3C80	484 UBGA	PRECON 3-85/85THB	28	1000	0		60 nm SRAM	1127
10070005	EP3C120	780 FBGA	PRECON 3-85/85THB	25	1000	0		60 nm SRAM	0951
10090029	EP3C120	780 FBGA	PRECON 3-85/85THB	25	2000	0		60 nm SRAM	1039
11040010	EP3C120	780 FBGA	PRECON 3-85/85THB	26	1000	0		60 nm SRAM	1117
11040013	EP3C120	780 FBGA	PRECON 3-85/85THB	29	1000	0		60 nm SRAM	1117
9090010	EP3CLS200	780 FBGA	PRECON 3-85/85THB	44	1000	0		60 nm SRAM	0936
11030015	EP3SE50	780 FBGA	PRECON 3-85/85THB	25	1000	0		65 nm SRAM	1043
10070023	EP3SL150	1152 FBGA	PRECON 3-85/85THB	25	1000	0		65 nm SRAM	1027
10100010	EP3SL150	1152 FBGA	PRECON 3-85/85THB	25	1000	0		65 nm SRAM	1041
10080012	EP3SL200	1152 FBGA	PRECON 4-85/85THB	25	1000	0		65 nm SRAM	1019
11080004	EP3SL200	1152 FBGA	PRECON 3-85/85THB	25	1000	0		65 nm SRAM	1049
11070014	EP3SL50	780 FBGA	PRECON 3-85/85THB	25	1012	0		65 nm SRAM	1112
11030010	EP4CGX15	148 QFN	PRECON 3-85/85THB	77	1000	0		60 nm SRAM	1101
11050008	EP4CGX15	148 QFN	PRECON 3-85/85THB	80	1000	0		60 nm SRAM	1119
11100015	EP4CGX15	148 QFN	PRECON 3-85/85THB	77	2000	0		60 nm SRAM	1131
10090024	EP4CGX150	896 FBGA	PRECON 3-85/85THB	25	1000	0		60 nm SRAM	1038
11070025	EP4CGX150	896 FBGA	PRECON 3-85/85THB	76	1000	0		60 nm SRAM	1119
10090004	EP4SE530	1760 FBGA	PRECON 4-85/85THB	25	1000	0		40 nm SRAM	1030
10020008	EP4SGX230	1517 FBGA	PRECON 3-85/85THB	25	1000	0		40 nm SRAM	1005
10090005	EP4SGX230	1517 FBGA	PRECON 3-85/85THB	25	1000	0		40 nm SRAM	1005
11030012	EP4SGX230	1517 FBGA	PRECON 3-85/85THB	24	1000	0		40 nm SRAM	1108
9070011	EPC1	8 PDIP	PRECON 1-85/85THB	45	1000	0		0.5µ EPROM	0929
10010008	EPC16	88 UBGA	PRECON 3-85/85THB	45	1000	0		0.35µ FLASH	0949
9090007	EPM570	256 FBGA	PRECON 3-85/85THB	25	1000	0		0.18µ FLASH	0931
9020008	EPM2210	256 FBGA	PRECON 3-85/85THB	25	1000	0		0.18µ FLASH	0901
11040002	EPM7064	44 PLCC	PRECON 3-85/85THB	45	1000	0		0.5µ EEPROM	1101

Highly Accelerated Stress Testing

HAST is an acronym for Highly Accelerated Stress Testing, which is a method for accelerating THB testing. HAST testing takes place in a closed stainless steel chamber that allows Temperature Humidity Bias to be performed under pressure. The ambient conditions are set up to ensure that the devices are stressed in an atmosphere that is not saturated so moisture cannot condense on the device leads. Altera runs its HAST conditions at 130°C / 85% RH, which has been shown to provide at least 10X acceleration in time over 85°C/85% RH testing.[x] Devices are biased similar to THB with alternate pin bias. Altera uses Polyimide printed circuit boards with buried PCB traces to keep them from corroding in the severe environment of HAST.

HAST Results

REL LOT #	DEVICE	PACKAGE TYPE	RELIABILITY TEST	# UNITS	STRESS HOURS	# FAIL		Technology	Date Code
12020024	5M240Z	144 TQFP	PRECON 3-H.A.S.T.	77	192	0		0.18µ FLASH	1201
11120013	5M570Z	144 TQFP	PRECON 3-H.A.S.T.	80	96	0		0.18µ FLASH	1131
11090026	5M570Z	144 FBGA	PRECON 3-H.A.S.T.	80	96	0		0.18µ FLASH	1136
11050006	5M1270Z	144 TQFP	PRECON 3-H.A.S.T.	75	96	0		0.18µ FLASH	1118
11060012	5M1270Z	144 TQFP	PRECON 3-H.A.S.T.	77	96	0		0.18µ FLASH	1123
11030028	5M1270Z	256 FBGA	PRECON 3-H.A.S.T.	77	96	0		0.18µ FLASH	1107
11050011	5M1270Z	256 FBGA	PRECON 3-H.A.S.T.	77	96	0		0.18µ FLASH	1118
11080021	5M2210Z	256 FBGA	PRECON 3-H.A.S.T.	79	192	0		0.18µ FLASH	1134
11080022	5M2210Z	256 FBGA	PRECON 3-H.A.S.T.	78	192	0		0.18µ FLASH	1134
12010017	5M2210Z	256 FBGA	PRECON 3-H.A.S.T.	77	192	0		0.18µ FLASH	1201
11060013	EP1C3	144 TQFP	PRECON 3-H.A.S.T.	77	96	0		0.13µ SRAM	1137
10040015	EP1C6	144 TQFP	PRECON 3-H.A.S.T.	77	96	0		0.13µ SRAM	1007
9050026	EP1C6	240 PQFP	PRECON 3-H.A.S.T.	26	96	0		0.13µ SRAM	0918
10100017	EP1C12	324 FBGA	PRECON 3-H.A.S.T.	77	96	0		0.13µ SRAM	1037
11110022	EP1C20	324 FBGA	PRECON 3-H.A.S.T.	77	96	0		0.13µ SRAM	1119
9080009	EP1C20	400 FBGA	PRECON 3-H.A.S.T.	76	96	0		0.13µ SRAM	0931
10050025	EP1K50	256 FBGA	PRECON 3-H.A.S.T.	25	96	0		0.22µ SRAM	1013
9050006	EP20K100	144 TQFP	PRECON 3-H.A.S.T.	25	192	0		0.22µ SRAM	0919
11100016	EP20K100	208 PQFP	PRECON 3-H.A.S.T.	25	96	0		0.22µ SRAM	1119
9100008	EP20K100	356 BGA	PRECON 3-H.A.S.T.	24	96	0		0.22µ SRAM	0931
10010021	EP20K100E	144 TQFP	PRECON 3-H.A.S.T.	25	96	0		0.18µ SRAM	1001
12020014	EP20K100E	240 PQFP	PRECON 3-H.A.S.T.	25	96	0		0.18µ SRAM	1125
10020009	EP20K160E	144 TQFP	PRECON 3-H.A.S.T.	25	96	0		0.18µ SRAM	1005
10040002	EP20K200E	208 PQFP	PRECON 3-H.A.S.T.	25	96	0		0.18µ SRAM	1007
9060022	EP20K200E	240 PQFP	PRECON 3-H.A.S.T.	25	192	0		0.18µ SRAM	0925
11040003	EP20K300E	672 FBGA	PRECON 3-H.A.S.T.	26	96	0		0.18µ SRAM	1115
9080012	EP20K600E	652 BGA	PRECON 3-H.A.S.T.	25	96	0		0.18µ SRAM	0935
11060014	EP2C8	256 FBGA	PRECON 3-H.A.S.T.	24	192	0		0.09µ SRAM	1126
11090028	EPC1	20 PLCC	PRECON 3-H.A.S.T.	45	96	0		0.5µ EPROM	1127
10020046	EPC1441	20 PLCC	PRECON 3-H.A.S.T.	45	96	0		0.5µ EPROM	1001
12030019	EPC1441	20 PLCC	PRECON 3-H.A.S.T.	45	96	0		0.5µ EPROM	1207
11120037	EPC16	100 PQFP	PRECON 3-H.A.S.T.	45	96	0		0.35µ FLASH	1142

REL LOT #	DEVICE	PACKAGE TYPE	RELIABILITY TEST	# UNITS	STRESS HOURS	# FAIL		Technology	Date Code
11080010	EPC2	20 PLCC	PRECON 3-H.A.S.T.	45	96	0		0.4µ FLASH	1113
12020028	EPC2	20 PLCC	PRECON 3-H.A.S.T.	45	96	0		0.4µ FLASH	1204
10070002	EPC4	100 PQFP	PRECON 3-H.A.S.T.	43	96	0		0.35µ FLASH	1013
10070002	EPC4	100 PQFP	PRECON 3-H.A.S.T.	43	96	0		0.35µ FLASH	1013
9020001	EPF10K10	208 PQFP	PRECON 3-H.A.S.T.	25	96	0		0.42µ SRAM	0901
9080013	EPF10K100A	356 BGA	PRECON 3-H.A.S.T.	25	96	0		0.3µ SRAM	0935
12030028	EPF10K100E	208 PQFP	PRECON 3-H.A.S.T.	25	96	0		0.22µ SRAM	1143
9050030	EPF10K100E	256 FBGA	PRECON 3-H.A.S.T.	25	96	0		0.22µ SRAM	0922
10020025	EPF10K100E	356 BGA	PRECON 3-H.A.S.T.	25	96	0		0.22µ SRAM	1001
11110023	EPF10K100E	356 BGA	PRECON 3-H.A.S.T.	25	96	0		0.22µ SRAM	1131
9060024	EPF10K130E	240 PQFP	PRECON 3-H.A.S.T.	25	192	0		0.22µ SRAM	0925
10080023	EPF10K30A	144 TQFP	PRECON 3-H.A.S.T.	25	96	0		0.3µ SRAM	1019
10030001	EPF10K50	240 RQFP	PRECON 3-H.A.S.T.	24	96	0		0.42µ SRAM	1008
12030020	EPF10K50V	356 BGA	PRECON 3-H.A.S.T.	25	96	0		0.3µ SRAM	1201
11040014	EPF10K70	240 RQFP	PRECON 3-H.A.S.T.	25	96	0		0.42µ SRAM	1107
11030014	EPF6016	208 PQFP	PRECON 3-H.A.S.T.	25	96	0		0.42µ SRAM	1101
9080008	EPF6016A	144 TQFP	PRECON 3-H.A.S.T.	25	96	0		0.3µ SRAM	0932
9070001	EPF8282A	84 PLCC	PRECON 3-H.A.S.T.	45	96	0		0.42µ SRAM	0919
12030003	EPM240	100 TQFP	PRECON 3-H.A.S.T.	48	192	0		0.18µ FLASH	1207
11030018	EPM570	100 TQFP	PRECON 3-H.A.S.T.	25	96	0		0.18µ FLASH	1112
11070012	EPM570	100 TQFP	PRECON 3-H.A.S.T.	79	96	0		0.18µ FLASH	1128
9070020	EPM570	256 MBGA	PRECON 3-H.A.S.T.	25	96	0		0.18µ FLASH	0919
9050008	EPM1270	144 TQFP	PRECON 3-H.A.S.T.	25	96	0		0.18µ FLASH	0913
10120011	EPM2210	256 FBGA	PRECON 3-H.A.S.T.	25	96	0		0.18µ FLASH	1031
10080014	EPM2210G	256 FBGA	PRECON 3-H.A.S.T.	25	96	0		0.18µ FLASH	1032
11100003	EPM3064A	44 TQFP	PRECON 3-H.A.S.T.	45	96	0		0.35µ EEPROM	1125
10040027	EPM3064A	100 TQFP	PRECON 3-H.A.S.T.	80	96	0		0.35µ EEPROM	1007
10110005	EPM3512A	208 PQFP	PRECON 3-H.A.S.T.	25	96	0		0.3µ EEPROM	1037
10010030	EPM7032AE	44 TQFP	PRECON 3-H.A.S.T.	45	96	0		0.35µ EEPROM	1001
10040017	EPM7064S	44 TQFP	PRECON 3-H.A.S.T.	45	96	0		0.5µ EEPROM	1007
9050022	EPM7128AE	100 TQFP	PRECON 3-H.A.S.T.	25	192	0		0.3µ EEPROM	0920
9010008	EPM7256AE	144 TQFP	PRECON 3-H.A.S.T.	25	96	0		0.3µ EEPROM	0851
11100018	EPM7256B	256 FBGA	PRECON 3-H.A.S.T.	25	96	0		0.22µ EEPROM	1137
9030015	EPM7512AE	208 PQFP	PRECON 3-H.A.S.T.	25	192	0		0.3µ EEPROM	0918
10030018	EPM7512AE	256 FBGA	PRECON 3-H.A.S.T.	25	96	0		0.35µ EEPROM	1001
10080013	EPM7512B	256 FBGA	PRECON 3-H.A.S.T.	25	96	0		0.22µ EEPROM	1025

Temperature Cycling

Temperature cycling accelerates the effects of changes in temperature on integrated circuits. Changes in temperature cause the different materials used in an integrated circuit to expand and contract at different rates since they have different coefficients of expansion. For example, coefficients of expansion vary from 17 x 10^{-6} mm/mm/°C for many molding compounds & AlCu leadframes to 4.2 for Silicon & Alloy 42 leadframes. The temperature extremes in temperature cycling give rise to mechanical stresses from the difference in thermal coefficients of expansion.[xi] The stress is greatest for large die and large packages. Altera uses dual chamber temperature cycling machines. The top chamber is maintained at the high temperature and the bottom chamber is maintained at the low temperature. The devices under stress are placed in an elevator platform that transfers the devices between the two chambers. The devices are transferred between chambers in a few seconds and reach the chamber temperature within 5 minutes, and are maintained at that temperature for a minimum of 5 minutes. Altera uses the MIL Std. 883 condition B (-55°C to +125°C) for temperature cycling. Devices are tested after 500, 700 and 1000 cycles. 700 cycles is all we need for qualification per new JESD47F standard. 1000 cycles reading is for reference only. Devices, which have been moisture preconditioned, are listed by the JEDEC moisture level.

Temperature Cycling Results

REL LOT #	DEVICE	PACKAGE TYPE	RELIABILITY TEST	# UNITS	# OF CYCLES	# FAIL		Technology	Date Code
12020024	5M240Z	144 TQFP	PRECON 3-TEMP CYC B	77	1000	0		0.18µ FLASH	1201
11090026	5M570Z	144 FBGA	PRECON 3-TEMP CYC B	76	1000	0		0.18µ FLASH	1136
11050006	5M1270Z	144 TQFP	PRECON 3-TEMP CYC B	77	1000	0		0.18µ FLASH	1118
11120012	5M1270Z	144 TQFP	PRECON 3-TEMP CYC B	77	2000	0		0.18µ FLASH	1143
11030028	5M1270Z	256 FBGA	PRECON 3-TEMP CYC B	77	1000	0		0.18µ FLASH	1107
11050011	5M1270Z	256 FBGA	PRECON 3-TEMP CYC B	77	1000	0		0.18µ FLASH	1118
11080001	5M2210Z	256 FBGA	PRECON 3-TEMP CYC B	77	1000	0		0.18µ FLASH	1130
11080020	5M2210Z	256 FBGA	PRECON 3-TEMP CYC B	80	2000	0		0.18µ FLASH	1134
11080021	5M2210Z	256 FBGA	PRECON 3-TEMP CYC B	80	2000	0		0.18µ FLASH	1134
11080022	5M2210Z	256 FBGA	PRECON 3-TEMP CYC B	79	2000	0		0.18µ FLASH	1134
12010017	5M2210Z	256 FBGA	PRECON 3-TEMP CYC B	77	1000	0		0.18µ FLASH	1201
12020026	5SGXA7	1760 FBGA	PRECON 4-TEMP CYC B	29	1000	0		28 nm SRAM	1202
11090002	5SGXA7	1932 FBGA	PRECON 4-TEMP CYC B	25	2000	0		28 nm SRAM	1135
10050024	EP1C3	100 TQFP	PRECON 3-TEMP CYC B	25	1000	0		0.13µ SRAM	1020
11060013	EP1C3	144 TQFP	PRECON 3-TEMP CYC B	77	1000	0		0.13µ SRAM	1137
10040015	EP1C6	144 TQFP	PRECON 3-TEMP CYC B	77	1000	0		0.13µ SRAM	1007
9050026	EP1C6	240 PQFP	PRECON 3-TEMP CYC B	27	1000	0		0.13µ SRAM	0918
10100017	EP1C12	324 FBGA	PRECON 3-TEMP CYC B	77	1000	0		0.13µ SRAM	1037
11110022	EP1C20	324 FBGA	PRECON 3-TEMP CYC B	77	1000	0		0.13µ SRAM	1119
9080009	EP1C20	400 FBGA	PRECON 3-TEMP CYC B	76	1000	0		0.13µ SRAM	0931
10050025	EP1K50	256 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.22µ SRAM	1013
9030006	EP1S10	672 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.13µ SRAM	0907
9100030	EP1S25	672 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.13µ SRAM	0942
11030011	EP1S40	1508 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.13µ SRAM	1001
12010023	EP1S40	1508 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.13µ SRAM	1149
10090021	EP1S80	1020 FBGA	PRECON 4-TEMP CYC B	25	1000	0		0.13µ SRAM	1036

REL LOT #	DEVICE	PACKAGE TYPE	RELIABILITY TEST	# UNITS	# OF CYCLES	# FAIL		Technology	Date Code
11040009	EP1S80	1508 FBGA	PRECON 3-TEMP CYC B	26	1000	0		0.13µ SRAM	1112
9110032	EP1SGX25	1020 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.13µ SRAM	0943
9060036	EP20K30E	144 TQFP	PRECON 3-TEMP CYC B	25	1000	0		0.18µ SRAM	0926
11100016	EP20K100	208 PQFP	PRECON 3-TEMP CYC B	25	1000	0		0.22µ SRAM	1119
9100008	EP20K100	356 BGA	PRECON 3-TEMP CYC B	25	1000	0		0.22µ SRAM	0931
10010021	EP20K100E	144 TQFP	PRECON 3-TEMP CYC B	25	1000	0		0.18µ SRAM	1001
12020014	EP20K100E	240 PQFP	PRECON 3-TEMP CYC B	25	1000	0		0.18µ SRAM	1125
10020009	EP20K160E	144 TQFP	PRECON 3-TEMP CYC B	25	1000	0		0.18µ SRAM	1005
9030002	EP20K160E	240 PQFP	PRECON 3-TEMP CYC B	25	1000	0		0.18µ SRAM	0907
11080018	EP20K160E	356 BGA	PRECON 3-TEMP CYC B	25	1000	0		0.18µ SRAM	1101
10040002	EP20K200E	208 PQFP	PRECON 3-TEMP CYC B	25	1000	0		0.18µ SRAM	1007
9060022	EP20K200E	240 PQFP	PRECON 3-TEMP CYC B	25	1000	0		0.18µ SRAM	0925
9090020	EP20K300E	672 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.18µ SRAM	0925
11050015	EP20K400C	672 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.15µ SRAM	1121
9060011	EP20K400E	672 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.18µ SRAM	0919
9080012	EP20K600E	652 BGA	PRECON 3-TEMP CYC B	25	1000	0		0.18µ SRAM	0935
10100015	EP2AGX65	358 UBGA	PRECON 3-TEMP CYC B	25	1000	0		40 nm SRAM	1039
10100012	EP2AGX95	780 FBGA	PRECON 3-TEMP CYC B	25	1000	0		40 nm SRAM	1040
10070038	EP2AGX125	1152 FBGA	PRECON 3-TEMP CYC B	27	1000	0		40 nm SRAM	1027
11120001	EP2AGX190	780 FBGA	PRECON 3-TEMP CYC B	25	1000	0		40 nm SRAM	1131
10050026	EP2AGX260	1152 FBGA	PRECON 3-TEMP CYC B	30	1000	0		40 nm SRAM	1020
9100006	EP2C8	148 QFN	PRECON 3-TEMP CYC B	25	1000	0		0.09µ SRAM	0940
10020010	EP2C8	256 FBGA	PRECON 3-TEMP CYC B	77	1000	0		0.09µ SRAM	1001
11030026	EP2C20	256 FBGA	PRECON 3-TEMP CYC B	77	1000	0		0.09µ SRAM	1049
10090028	EP2C70	672 FBGA	PRECON 3-TEMP CYC B	77	1000	0		0.09µ SRAM	1025
11100005	EP2C70	672 FBGA	PRECON 3-TEMP CYC B	77	1000	0		0.09µ SRAM	1119
10090025	EP2S30	484 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.09µ SRAM	1039
10040020	EP2S90	1020 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.09µ SRAM	1013
11060011	EP2S90	1020 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.09µ SRAM	1125
11120011	EP2S130	1508 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.09µ SRAM	1119
10110015	EP2S180	1020 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.09µ SRAM	1044
10110006	EP2S180	1508 FBGA	PRECON 4-TEMP CYC B	25	1000	0		0.09µ SRAM	1037
9090024	EP2SGX90	1152 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.09µ SRAM	0931
10010012	EP3C5	144 EQFP	PRECON 3-TEMP CYC B	79	1000	0		65 nm SRAM	1001
10040029	EP3C5	144 EQFP	PRECON 3-TEMP CYC B	80	1000	0		65 nm SRAM	1016
10050001	EP3C16	144 EQFP	PRECON 3-TEMP CYC B	80	1000	0		60 nm SRAM	1018
10040009	EP3C16	240 PQFP	PRECON 3-TEMP CYC B	25	1000	0		65 nm SRAM	1014
10050017	EP3C25	144 EQFP	PRECON 3-TEMP CYC B	80	1000	0		65 nm SRAM	1019
10040008	EP3C25	240 PQFP	PRECON 3-TEMP CYC B	25	2000	0		65 nm SRAM	1014
10050016	EP3C25	256 FBGA	PRECON 3-TEMP CYC B	78	1000	0		60 nm SRAM	1019
10060018	EP3C25	256 FBGA	PRECON 3-TEMP CYC B	79	1000	0		60 nm SRAM	1019
10040010	EP3C40	240 PQFP	PRECON 3-TEMP CYC B	25	1000	0		65 nm SRAM	1014
11060006	EP3C40	240 PQFP	PRECON 3-TEMP CYC B	77	1000	0		60 nm SRAM	1113
10060015	EP3C40	484 FBGA	PRECON 3-TEMP CYC B	25	1000	0		60 nm SRAM	1021

REL LOT #	DEVICE	PACKAGE TYPE	RELIABILITY TEST	# UNITS	# OF CYCLES	# FAIL		Technology	Date Code
10120003	EP3C55	484 UBGA	PRECON 3-TEMP CYC B	25	1000	0		60 nm SRAM	1031
10110024	EP3C55	780 FBGA	PRECON 3-TEMP CYC B	25	1000	0		60 nm SRAM	1046
10070020	EP3C80	484 UBGA	PRECON 3-TEMP CYC B	25	1000	0		60 nm SRAM	1019
11040001	EP3C80	484 UBGA	PRECON 3-TEMP CYC B	80	1000	0		60 nm SRAM	1127
11050010	EP3C80	484 UBGA	PRECON 3-TEMP CYC B	78	1000	0		60 nm SRAM	1101
11040010	EP3C120	780 FBGA	PRECON 3-TEMP CYC B	77	1000	0		60 nm SRAM	1117
11040013	EP3C120	780 FBGA	PRECON 3-TEMP CYC B	77	1000	0		60 nm SRAM	1117
11060010	EP3C120	780 FBGA	PRECON 3-TEMP CYC B	30	1000	0		60 nm SRAM	1124
9070009	EP3CLS200	780 FBGA	PRECON 3-TEMP CYC B	28	1000	0		60 nm SRAM	0916
9070010	EP3CLS200	780 FBGA	PRECON 3-TEMP CYC B	44	1000	0		60 nm SRAM	0925
11030015	EP3SE50	780 FBGA	PRECON 3-TEMP CYC B	25	1000	0		65 nm SRAM	1043
11070014	EP3SL50	780 FBGA	PRECON 3-TEMP CYC B	25	1000	0		65 nm SRAM	1112
10070021	EP3SL150	780 FBGA	PRECON 3-TEMP CYC B	25	1000	0		65 nm SRAM	1027
10100010	EP3SL150	1152 FBGA	PRECON 3-TEMP CYC B	25	1000	0		65 nm SRAM	1041
11100002	EP3SL150	1152 FBGA	PRECON 3-TEMP CYC B	25	1000	0		65 nm SRAM	1119
10080012	EP3SL200	1152 FBGA	PRECON 4-TEMP CYC B	25	1000	0		65 nm SRAM	1019
11080004	EP3SL200	1152 FBGA	PRECON 3-TEMP CYC B	25	1000	0		65 nm SRAM	1049
12010021	EP3SL200	1152 FBGA	PRECON 3-TEMP CYC B	25	1000	0		65 nm SRAM	1146
10040013	EP4CE40	484 FBGA	PRECON 3-TEMP CYC B	23	1000	0		60 nm SRAM	1014
10040014	EP4CE40	484 FBGA	PRECON 3-TEMP CYC B	24	1000	0		60 nm SRAM	1014
10050009	EP4CGX15	148 QFN	PRECON 3-TEMP CYC B	25	1000	0		60 nm SRAM	1012
10080028	EP4CGX15	148 QFN	PRECON 3-TEMP CYC B	77	1000	0		60 nm SRAM	1025
11030010	EP4CGX15	148 QFN	PRECON 3-TEMP CYC B	77	1000	0		60 nm SRAM	1101
11100015	EP4CGX15	148 QFN	PRECON 3-TEMP CYC B	77	1000	0		60 nm SRAM	1131
10060001	EP4CGX15	169 FBGA	PRECON 3-TEMP CYC B	25	1000	0		60 nm SRAM	1022
10060002	EP4CGX15	169 FBGA	PRECON 3-TEMP CYC B	25	1000	0		60 nm SRAM	1022
10080015	EP4CGX150	672 FBGA	PRECON 3-TEMP CYC B	30	1000	0		60 nm SRAM	1028
10090024	EP4CGX150	896 FBGA	PRECON 3-TEMP CYC B	25	1000	0		60 nm SRAM	1038
10110002	EP4CGX150	896 FBGA	PRECON 3-TEMP CYC B	30	1000	0		60 nm SRAM	1044
11070025	EP4CGX150	896 FBGA	PRECON 3-TEMP CYC B	77	1000	0		60 nm SRAM	1119
10020008	EP4SGX230	1517 FBGA	PRECON 3-TEMP CYC B	25	2000	0		40 nm SRAM	1005
11010007	EP4SGX230	1517 FBGA	PRECON 3-TEMP CYC B	25	1000	0		40 nm SRAM	1101
11030012	EP4SGX230	1517 FBGA	PRECON 3-TEMP CYC B	24	1000	0		40 nm SRAM	1108
11120033	EP4SGX230	1517 FBGA	PRECON 3-TEMP CYC B	25	1000	0		40 nm SRAM	1137
11010001	EP4SGX530	1517 HBGA	PRECON 4-TEMP CYC B	25	1000	0		40 nm SRAM	1101
10090001	EP4SGX530	1932 FBGA	PRECON 3-TEMP CYC B	40	1000	0		40 nm SRAM	1030
11090028	EPC1	20 PLCC	PRECON 3-TEMP CYC B	45	1000	0		0.5µ EPROM	1127
9070011	EPC1	8 PDIP	PRECON 1-TEMP CYC B	45	1000	0		0.5µ EPROM	0929
10020046	EPC1441	20 PLCC	PRECON 3-TEMP CYC B	45	1000	0		0.5µ EPROM	1001
12030019	EPC1441	20 PLCC	PRECON 3-TEMP CYC B	45	1000	0		0.5µ EPROM	1207
11080010	EPC2	20 PLCC	PRECON 3-TEMP CYC B	45	1000	0		0.4µ FLASH	1113
12020028	EPC2	20 PLCC	PRECON 3-TEMP CYC B	45	1000	0		0.4µ FLASH	1204
10070002	EPC4	100 PQFP	PRECON 3-TEMP CYC B	45	1000	0		0.35µ FLASH	1013
11120037	EPC16	100 PQFP	PRECON 3-TEMP CYC B	45	1000	0		0.35µ FLASH	1142

REL LOT #	DEVICE	PACKAGE TYPE	RELIABILITY TEST	# UNITS	# OF CYCLES	# FAIL		Technology	Date Code
10010008	EPC16	88 UBGA	PRECON 3-TEMP CYC B	45	1000	0		0.35µ FLASH	0949
9020001	EPF10K10	208 PQFP	PRECON 3-TEMP CYC B	24	1000	0		0.42µ SRAM	0901
9050032	EPF10K20	144 TQFP	PRECON 3-TEMP CYC B	25	1000	0		0.42µ SRAM	0922
10080023	EPF10K30A	144 TQFP	PRECON 3-TEMP CYC B	25	1000	0		0.3µ SRAM	1019
10030001	EPF10K50	240 RQFP	PRECON 3-TEMP CYC B	25	1000	0		0.42µ SRAM	1008
9050005	EPF10K50V	356 BGA	PRECON 3-TEMP CYC B	25	1000	0		0.3µ SRAM	0913
10110029	EPF10K70	240 RQFP	PRECON 3-TEMP CYC B	25	1000	0		0.42µ SRAM	1048
11040014	EPF10K70	240 RQFP	PRECON 3-TEMP CYC B	25	1000	0		0.42µ SRAM	1107
9080013	EPF10K100A	356 BGA	PRECON 3-TEMP CYC B	25	1000	0		0.3µ SRAM	0935
11070013	EPF10K100A	484 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.3µ SRAM	1137
9050001	EPF10K100E	208 PQFP	PRECON 3-TEMP CYC B	25	1000	0		0.22µ SRAM	0916
12030028	EPF10K100E	208 PQFP	PRECON 3-TEMP CYC B	25	1000	0		0.22µ SRAM	1143
9050030	EPF10K100E	256 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.22µ SRAM	0922
10020025	EPF10K100E	356 BGA	PRECON 3-TEMP CYC B	25	1000	0		0.22µ SRAM	1001
11110023	EPF10K100E	356 BGA	PRECON 3-TEMP CYC B	25	1000	0		0.22µ SRAM	1131
9040018	EPF10K130E	240 PQFP	PRECON 3-TEMP CYC B	25	1000	0		0.22µ SRAM	0915
11030014	EPF6016	208 PQFP	PRECON 3-TEMP CYC B	25	1000	0		0.42µ SRAM	1101
9080008	EPF6016A	144 TQFP	PRECON 3-TEMP CYC B	25	1000	0		0.3µ SRAM	0932
9070001	EPF8282A	84 PLCC	PRECON 3-TEMP CYC B	45	1000	0		0.42µ SRAM	0919
10040030	EPM240Z	100 MBGA	PRECON 3-TEMP CYC B	45	1000	0		0.18µ FLASH	1017
11030013	EPM240Z	100 MBGA	PRECON 3-TEMP CYC B	77	1000	0		0.18µ FLASH	1101
10020013	EPM570	100 TQFP	PRECON 3-TEMP CYC B	77	1000	0		0.18µ FLASH	1001
10070003	EPM570	100 TQFP	PRECON 3-TEMP CYC B	44	1000	0		0.18µ FLASH	1013
11030018	EPM570	100 TQFP	PRECON 3-TEMP CYC B	24	1000	0		0.18µ FLASH	1112
11070012	EPM570	100 TQFP	PRECON 3-TEMP CYC B	78	1000	0		0.18µ FLASH	1128
9090007	EPM570	256 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.18µ FLASH	0931
9070020	EPM570	256 MBGA	PRECON 3-TEMP CYC B	24	1000	0		0.18µ FLASH	0919
9050008	EPM1270	144 TQFP	PRECON 3-TEMP CYC B	25	1000	0		0.18µ FLASH	0913
10120011	EPM2210	256 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.18µ FLASH	1031
10040027	EPM3064A	100 TQFP	PRECON 3-TEMP CYC B	80	1000	0		0.35µ EEPROM	1007
11100003	EPM3064A	44 TQFP	PRECON 3-TEMP CYC B	45	1000	0		0.35µ EEPROM	1125
10010030	EPM7032AE	44 TQFP	PRECON 3-TEMP CYC B	45	1000	0		0.35µ EEPROM	1001
11040002	EPM7064	44 PLCC	PRECON 3-TEMP CYC B	45	1000	0		0.5µ EEPROM	1101
10040017	EPM7064S	44 TQFP	PRECON 3-TEMP CYC B	45	1000	0		0.5µ EEPROM	1007
9050022	EPM7128AE	100 TQFP	PRECON 3-TEMP CYC B	25	1000	0		0.3µ EEPROM	0920
11100018	EPM7256B	256 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.22µ EEPROM	1137
10070004	EPM7256E	192 PGA	PRECON 3-TEMP CYC B	50	1000	0		0.5µ EEPROM	1025
10100013	EPM7512AE	208 PQFP	PRECON 3-TEMP CYC B	25	1000	0		0.35µ EEPROM	1037
11070008	EPM7512AE	208 PQFP	PRECON 3-TEMP CYC B	25	1000	0		0.35µ EEPROM	1119
10030018	EPM7512AE	256 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.35µ EEPROM	1001
10080013	EPM7512B	256 FBGA	PRECON 3-TEMP CYC B	25	1000	0		0.22µ EEPROM	1025
10090007	HC4GX25	1152 FBGA	PRECON 3-TEMP CYC B	25	1000	0		40 nm SRAM	1036

Solder Joint Reliability

Solder Joint Reliability is measured by temperature cycling devices on a printed circuit board from 0°C to 100°C at 1-2 cycles per hour. This test is designed to identify failures due to the mismatch of temperature coefficients of expansion between the device and printed circuit board. Devices are soldered onto a 2.36 mm thick, 40cm long, and 10cm wide FR4 printed circuit board by convection reflow soldering. MBGA (0.5 mm pitch) package is soldered on 1.6 mm thick FR4 printed circuit board in addition to 2.36 mm thick one. QFN package is soldered on 0.8 mm thick FR4 printed circuit board. The devices are continuously monitored for failure of second level interconnects. Creep failures occur in the solder ball at points of maximum stress. The actual fatigue life is obtained by fitting failure data using a log-normal or Weibull distribution to predict the number of cycles to 0.1% fail. In many cases no failures are observed and the test was stopped after 5000 cycles. The effects of various package and printed circuit board parameters can be predicted via finite element modeling. [xii] [xiii] The results of finite element modeling are used to optimize package reliability and to extend the results to similar die/package combinations.

Tin-Lead (Sn-Pb) Solder Joint Reliability

Package	Substrate pad size	Pitch	Technology	heat sink	Die Size (mm)	MTTF	Cycles to 0.1% fails (Extrapolated)
U88	0.4 mm	0.8 mm	Wire-bonded Stacked Die + 2L FR4 substrate	None	6.9 * 4.6	4068	3162
E144	NA	0.5mm	lead frame + ground pad	None	5.12 * 5.21	0 fails to 6000	0 fails to 6000
QFN148	NA	0.5mm	lead frame + ground pad	None	5.12 * 5.21	2839	2119
F256	0.45mm	1.0mm	low k die + Wire Bond + 4 Layer BT	None	5.80*6.22	4798	3775
F256	0.45mm	1.0mm	low k die + Wire Bond + 4 Layer BT	None	5.80*6.22	5058	3236
F256	0.45mm	1.0mm	low k die + Wire Bond + 4 Layer BT	None	5.80*6.22	4194	2161
F256	0.45 mm	1.0 mm	Wire Bond + 2 Layer BT	None	8.8 * 7.9	4437	3687
F256 thin outline	0.45 mm	1.0 mm	low k die + Wire Bond + 4 Layer BT	None	7.68 * 6.81	3574	2888
F256	0.45mm	1.0mm	Wire bond + 2Layer BT	None	5.46 x 5.85	4437	3713
B356	0.58 mm	1.27 mm	Wire Bond + 2 Layer BT	None	9 * 9.8	0 fails to 5000	0 fails to 5000
U358	0.4mm	0.8mm	Lid-less Flip-Chip + 4L build up BT	None	10.11*10	2777	2740
U484	0.4mm	0.8mm	low k die + Wire Bond + 4 Layer BT	None	8.4 * 8.03	0 fails to 5000	0 fails to 5000
B652	0.58 mm	1.27 mm	Wire bond + 1 Layer Tape	Cu	17.01 * 15.38	0 fails to 5000	0 fails to 5000
B724	0.55 mm	1.27 mm	Flip Chip + 6 layer build-up BT	2 pc Cu	18.1 * 13.4	0 fails to 2800	0 fails to 2800
F484	0.45 mm	1.0 mm	Wire bond + 2 layer BT	None	11.5 * 11.5	6534	3408

Package	Substrate pad size	Pitch	Technology	heat sink	Die Size (mm)	MTTF	Cycles to 0.1% fails (Extrapolated)
F672	0.45 mm	1.0 mm	Wire Bond + 4 Layer BT	None	11.19*11.12	5601	4448
F672	0.45 mm	1.0 mm	Wire Bond + 4 Layer BT	None	16 * 11.8	0 fails at 5200	0 fails at 5200
F672	0.45 mm	1.0 mm	Wire Bond + 4 Layer BT	None	16 * 11.8	0 fails at 5400	0 fails at 5400
F672	0.45mm	1.0mm	Low K die + Wire Bond + 4 Layer BT	None	8.4 * 8.03	0 fails to 5400	0 fails to 5400
F672	0.55 mm	1.0 mm	Flip Chip + 8 layer build-up BT	AlSiC	19.1 * 16.5	4419	3284
F672	0.55 mm	1.0 mm	Flip Chip + 8 layer build-up BT	AlSiC	19.1 * 16.5	0 fails to 5700	0 fails to 5700
F672	0.55 mm	1.0 mm	Flip Chip + 6 layer build-up BT	AlSiC	16.5 * 13.1	5304	3437
F672	0.55 mm	1.0 mm	Flip Chip + 6 layer build-up BT	AlSiC	16.5 * 13.1	4130	3487
F672	0.55 mm	1.0 mm	Flip Chip + 6 layer build-up BT	AlSiC	16.5 * 13.1	0 fails to 5100	0 fails to 5100
F672	0.55 mm	1.0 mm	Flip Chip + 6 layer build-up BT	2 pc Cu	16.5 * 13.1	0 fails to 5400	0 fails to 5400
F780	0.45mm	1.0mm	Wire bond + 4Layer BT	None	10.7 5* 11.62	5087	3413
F780	0.45mm	1.0mm	Wire bond + 2Layer BT	None	10.7 5* 11.62	5318	4380
F780	0.55 mm	1.0 mm	Flip Chip + 6 layer build-up BT	2 pc Cu	16.3 * 13.5	5890	4614
F780	0.55 mm	1.0 mm	Flip Chip + 6 layer build-up BT	2 pc Cu	16.3 * 13.5	0 fails to 4500	0 fails to 4500
F896	0.45	1.0 mm	Wire bonded + 4 layer BT	None	8.86 * 9.96	0 fails to 4000	0 fails to 4000
F896	0.45	1.0 mm	Wire bonded + 4 layer BT	None	11.19*11.12	5148	3080
F1020	0.55 mm	1.0 mm	Flip Chip + 6 layer build-up BT	AlSiC	22.6 * 19.9	0 fails to 6000	0 fails to 6000
F1020	0.55 mm	1.0 mm	Flip Chip + 6 layer build-up BT	AlSiC	22.6 * 19.9	8897	5670
F896	0.45	1.0 mm	Wire Bond + 2 Layer BT	None	13.16 X 12.39	3911	2927
F896	0.45mm	1.0mm	N20 triple row staggered Wire bond + 2Layer BT	None	10.9 X 10.5	4512	3307
F1020	0.55 mm	1.0 mm	Flip Chip + 6 layer build-up BT	2 pc Cu	22.1 * 19.4	5781	5174
F1020	0.55mm	1.0mm	Low k Die + Flip Chip + 8 layer BT build-up	2 pc Cu	15.33 * 14.24	5432	4510
F1020	0.55mm	1.0mm	Low k Die + Flip Chip + 8 layer BT build-up	2 pc Cu	15.33 * 14.24	4333	3705
F1020	0.55mm	1.0mm	Low k Die + Flip Chip + 8 layer BT build-up	2 pc Cu	22.56 * 25.54	5579	4603

Package	Substrate pad size	Pitch	Technology	heat sink	Die Size (mm)	MTTF	Cycles to 0.1% fails (Extrapolated)
F1020	0.55mm	1.0mm	Flip Chip + 8 layer BT build-up	2 pc Cu	22.6X19.9	0 fails to 4000	0 fails to 4000
F1020	0.55 mm	1.0 mm	Lidless Flip Chip + 6 layer build-up BT	None	17.62*15.94	4804	3104
F1020	0.55 mm	1.0 mm	Lidless Flip Chip + 6 layer build-up BT	None	18.03*17.29	4551	3168
F1152	0.55 mm	1.0 mm	Flip Chip + 6 layer build-up BT	2 pc Cu	16*14	4106	3216
F1152	0.55 mm	1.0 mm	Lidless Flip Chip + 6 layer build-up BT	None	16*14	4421	3474
F1508	0.55mm	1.0mm	Low k Die + Flip Chip + 8 layer BT build-up	SPL	22.17 * 19.24	6506	3651
F1508	0.55 mm	1.0 mm	Flip Chip + 6 layer build-up BT	2 pc Cu	23.9 * 23.3	4233	2694
F1508	0.55 mm	1.0 mm	Flip Chip + 6 layer build-up BT	2 pc Cu	23.9 * 23.3	3074	2040
F1508	0.55 mm	1.0 mm	Flip Chip + 6 layer build-up BT	SPL	23.9 * 23.3	4797	3182
F1517	0.55 mm	1.0 mm	Flip Chip + 14 layer build-up BT	2 pc Cu	25.6 * 26.5 (N40 ELK die)	4497	3564
F1517	0.55 mm	1.0 mm	Flip Chip + 14 layer build-up BT	SPL	25.6 * 26.5 (N40 ELK die)	4733	4100
F1760	0.55 mm	1.0 mm	Flip Chip + 12 layer build-up BT	2 pc Cu	20.0 * 20.0 (N40 ELK die)	3541	2572
F1760	0.55 mm	1.0 mm	Flip Chip + 8 layer build-up BT	SPL	25 * 26 (N28 die)	3703	3296
F1932	0.55 mm	1.0 mm	Flip Chip + 14 layer build-up BT	2 pc Cu	25.6 * 26.5 (N40 ELK die)	3552	2932

Pb-Free Solder Joint Reliability

Package	Substrate pad size	Pitch	Technology	heat sink	Die Size (mm)	MTTF	Cycles to 0.1% fails (Extrapolated)
M100	0.3 mm	0.5 mm	Wire Bond + 2 Layer BT	None	3.2 * 3.2	0 fails to 6000 0 fails to 6000	0 fails to 6000 0 fails to 6000
M256	0.3 mm	0.5 mm	Wire Bond + 4 Layer BT	None	3.9 * 3.9	0 fails to 6000 0 fails to 6000	0 fails to 6000 0 fails to 6000
U88	0.4 mm	0.8 mm	Wire-bonded Stacked Die + 2L FR4 substrate	None	6.9 * 4.6	0 fails to 6000	0 fails to 6000
T144	N/A	0.5 mm	lead frame	N/A	4.9*6.0	0 fails to 5500	0 fails to 5500
E144	NA	0.5mm	lead frame + ground pad	None	5.12 * 5.21	0 fails to 6000	0 fails to 6000
QFN148	NA	0.5mm	lead frame + ground pad	None	5.12 * 5.21	2938	2511
F256 thin outline	0.45 mm	1.0 mm	Wire Bond + 4 Layer BT	None	7.68 * 6.81	0 fails to 5000	0 fails to 5000

Package	Substrate pad size	Pitch	Technology	heat sink	Die Size (mm)	MTTF	Cycles to 0.1% fails (Extrapolated)
F256	0.45mm	1.0mm	low k die + Wire Bond + 4 Layer BT	None	5.80*6.22	0 fails to 6000	0 fails to 5000
F256	0.45mm	1.0mm	Wire bond + 2Layer BT	None	5.46 x 5.85	6000 no failure	6000 no failure
Q240	N/A	0.5 mm	lead frame	N/A	8.0*7.9	0 fails to 6000	0 fails to 6000
U358	0.4mm	0.8mm	Lid-less Flip-Chip + 4 Layer build up BT	None	10.11*10	0 fails to 6000	0 fails to 6000
U484	0.4mm	0.8mm	low k die + Wire Bond + 4 Layer BT	None	8.4 * 8.03	0 fails to 3500	0 fails to 3500
F484	0.45	1.0 mm	Wire-bonded + 4 layer BT	None	10.8 * 8.8	0 fails to 6000	0 fails to 6000
F672	0.45 mm	1.0 mm	Wire Bond + 4 Layer BT	None	11.19*11.12	0 fails to 6000	0 fails to 6000
F780	0.55 mm	1.0 mm	Flip Chip + 6 layer build-up BT	2 pc Cu	16.3 * 13.5	0 fails to 5000	0 fails to 5000
F896	0.45	1.0 mm	Wire-bonded + 4 layer BT	None	8.86 * 9.96	0 fails to 4000	0 fails to 4000
F896	0.45	1.0 mm	Wire bonded + 4 layer BT	None	11.19*11.12	0 fails to 6000	0 fails to 6000
F896	0.45mm	1.0mm	N20 triple row staggered Wire bond + 2Layer BT	None	10.9 X 10.5	6000 no failure	6000 no failure
M1019	0.3mm	0.5mm	Lid-less Flip-Chip + 3-2-3 build up substrate	None	10.16*10.52	0 fails to 6000	0 fails to 6000
F1020	0.55 mm	1.0 mm	Flip Chip + 6 layer build-up BT	2 pc Cu	22.6 * 19.9	0 fails to 5887	0 fails to 5887
F1020	0.55 mm	1.0 mm	Flip Chip + 6 layer build-up BT	SPL	17.62*15.94	0 fails to 6000	0 fails to 6000
F1020	0.55 mm	1.0 mm	Lidless Flip Chip + 6 layer build-up BT	None	17.62*15.94	0 fails to 6000	0 fails to 6000
F1020	0.55 mm	1.0 mm	Flip Chip + 6 layer build-up BT	SPL	18.03*17.29	0 fails to 6000	0 fails to 6000
F1020	0.55 mm	1.0 mm	Lidless Flip Chip + 6 layer build-up BT	None	18.03*17.29	0 fails to 6000	0 fails to 6000
F1508	0.55 mm	1.0 mm	Flip Chip + 6 layer build-up BT	2 pc Cu	23.9 * 23.3	0 fails to 6000	0 fails to 6000
F1681	0.55 mm	1.0 mm	Molded Flip Chip + 8 layer build-up BT	None	18 * 22	0 fails to 5700	0 fails to 5700
F1760	0.55 mm	1.0 mm	Flip Chip + 8 layer build-up BT	SPL	25 * 26 (N28 die)	0 fails to 7000	0 fails to 7000

Serial Configuration Devices

The EPCS4, EPCS16 and EPCS64 serial configuration devices are fabricated on Micron 0.11 µm CMOS process technology, EPCS1 is on 0.15 µm and EPCS128 on 65 nm. These products operate at a nominal Vcc of 3.3V. The EPCS1, EPCS4 and EPCS 16 are available in the 8-pin small outline integrated circuit (SOIC) package while EPCS64 and EPCS128 are available in 16-pin SOIC package.

0.15 µm process - Die Related Results

Test Procedure	Test Conditions	Lot 1	Lot 2	Lot 3
High Temperature Operating Life	140°C, 4.2V 504hrs 1008hrs	 0/80 0/80	 0/77 0/77	 0/80 0/80
Low Temperature Operating Life	–40°C, 4.2V 504hrs	 0/80	 0/77	 0/80
High Temperature Bake	200°C, 500hrs 1000hrs	 0/77 0/77	 0/77 0/77	 0/77 0/77
Erase/Write Cycles and Bake	10,000 E/W cycles + Bake 200°C, 48hrs 100,000 E/W cycles + Bake 200°C, 48hrs	0/77 0/77	0/77 0/77	0/77 0/77
Electrostatic Discharge	Human body model: 1.5kΩ, 100pF	>2000V	>2000V	>2000V
Latch-up	Class II - Level A (at 85°C)	Pass	Pass	Pass

0.11 µm process - Die Related Results

Test Procedure	Test Conditions	Lot 1	Lot 2	Lot 3
High Temperature Operating Life	140°C, 4.2V 168 hrs 500 hrs	 0/77 0/77	 0/77 0/77	 0/77 0/77
Low Temperature Operating Life	–40°C, 4.2V 168 hrs	 0/15	 0/15	 0/15
High Temperature Bake	250°C, 168 hrs 500 hrs	 0/77 0/77	 0/77 0/77	 0/77 0/77
Erase/Write Cycles and Bake	10,000 E/W cycles 100,000 E/W cycles + Bake 250°C, 168 hrs	0/77 0/77 0/77	0/77 0/77 0/77	0/77 0/77 0/77
Electrostatic Discharge	Human body model: 1.5kΩ, 100pF Machine Model: 0 Ω, 200pF	>2000V >200 V	>2000V > 200 V	>2000V >200 V
Latch-up	Class II - Level A (at 150°C)	Pass	Pass	Pass

65 nm process – Die Related Results

Test Procedure	Test Conditions	Lot 1	Lot 2	Lot 3
High Temperature Operating Life	125°C, 4.2V 168 hrs 500 hrs	 0/77 0/77	 0/77 0/77	 0/77 0/77
High Temperature Bake	150°C 168 hrs 500 hrs 1,000 hrs	 0/77 0/77 0/77	 0/77 0/77 0/77	 0/77 0/77 0/77
Erase/Write Cycles and Bake	10,000 E/W cycles + Bake 150°C, 168 hrs	0/77	0/77	0/77
Electrostatic Discharge	Human body model: 1.5kΩ, 100pF Machine Model: 0Ω, 200pF	>2000V > 200V	—	—
Latch-Up	Class II - 150°C	0/6	0/6	0/6

Package Qualification Data

Package	Qualification Test	Read Out	Lot 1	Lot 2	Lot 3
SOIC8	High Temp Storage Life @ 150°C	1000 hrs	0/77	0/77	0/77
	Temp Humidity Bias (85°C /85%RH)	1000 hrs	0/77	0/77	0/77
	Temperature Cycle "C" (-65°C to 150°C)	500 cyc	0/77	0/77	0/77
	Unbiased HAST (130°C / 85%RH)	96 hrs	0/77	0/77	0/77
SOIC16	High Temp Storage Life @ 150°C	1000 hrs	0/77	0/77	0/77
	Temp Humidity Bias (85°C /85%RH)	1000 hrs	0/77	0/77	0/77
	Temperature Cycle "C" (-65°C to 150°C)	500 cyc	0/77	0/77	0/77
	Unbiased HAST (130°C / 85%RH)	96 hrs	0/77	0/77	0/77

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