Cyclone® II EP2C15A, EP2C20 & EP2C20A Device Pin-Out
PT-EP2C20-2.1

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Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F256	F484	DQS for x8/x9 in Q240	DQS for x16/x18 in Q240	DQS for x8/x9 in F256	DQS for x16/x18 in F256	DQS for x8/x9 in F484	DQS for x16/x18 in F484
B2	VREFB2N0	GND_PLL3			1	D5	F5						
B2	VREFB2N0	VCCD_PLL3			2	E5	E5						
B2	VREFB2N0	GND_PLL3			3	F5	F6						
B2	VREFB2N0	GND											
B2	VREFB2N0	IO	ASDO	ASDO	4	C3	C4						
B2	VREFB2N0	IO	nCSO	nCSO	5	F4	C3						
B2	VREFB2N0	IO	LVDS26p	CRC_ERROR	6	C1	D3	DQ0L0	DQ1L0				
B2	VREFB2N0	IO	LVDS26n	CLKUSR	7	C2	D4	DQ0L1	DQ1L1				
B2	VREFB2N0	IO	PLL3_OUTp		8	D3	D5	DQ0L2	DQ1L2	DQ0L0	DQ1L0		
B2	VREFB2N0	IO	PLL3_OUTn		9	D4	D6	DQ0L3	DQ1L3	DQ0L1	DQ1L1		
B2	VREFB2N0	VCCIO2			10								
B2	VREFB2N0	IO	LVDS25p				E3					DQ2L0	DQ1L0
B2	VREFB2N0	IO	LVDS25n				E4					DQ2L1	DQ1L1
B2	VREFB2N0	IO	LVDS24p				C1					DQ2L2	DQ1L2
B2	VREFB2N0	IO	LVDS24n				C2					DQ2L3	DQ1L3
B2	VREFB2N0	IO	VREFB2N0		11	F3	F4						
B2	VREFB2N0	IO	LVDS23p				G6					DQ2L4	DQ1L4
B2	VREFB2N0	IO	LVDS23n				G5					DQ2L5	DQ1L5
B2	VREFB2N0	GND			12								
B2	VREFB2N0	IO					F3					DQ2L6	DQ1L6
B2	VREFB2N0	IO	LVDS22p				D1					DQ2L7	DQ1L7
B2	VREFB2N0	IO	LVDS22n				D2						DQ1L8
B2	VREFB2N0	IO	LVDS21p				G3					DM2L	DM1L0/ BWS#1L0
B2	VREFB2N0	IO	LVDS21n				H4					DQ0L0	DQ1L9
B2	VREFB2N0	VCCIO2											
B2	VREFB2N0	IO	LVDS20p		13	D2	H5	CDPCLK0/ DQS2L	CDPCLK0/ DQS2L	CDPCLK0/ DQS2L	CDPCLK0/ DQS2L	CDPCLK0/ DQS2L	CDPCLK0/ DQS2L
B2	VREFB2N0	IO	LVDS20n		14	D1	H6	DQ0L4	DQ1L4	DQ0L2	DQ1L2	DQ0L1	DQ1L10
B2	VREFB2N1	IO	LVDS19p		15	E3	E1	DQ0L5	DQ1L5	DQ0L3	DQ1L3	DQ0L2	DQ1L11
B2	VREFB2N1	IO	LVDS19n		16	E4	E2	DQ0L6	DQ1L6	DQ0L4	DQ1L4	DQ0L3	DQ1L12
B2	VREFB2N1	IO	LVDS18p				F1					DQ0L4	DQ1L13
B2	VREFB2N1	IO	LVDS18n				F2					DQ0L5	DQ1L14
B2	VREFB2N1	IO	LVDS17p				H1					DQ0L6	DQ1L15
B2	VREFB2N1	GND			17								
B2	VREFB2N1	IO	LVDS17n				H2					DQ0L7	DQ1L16
B2	VREFB2N1	IO					L8						
B2	VREFB2N1	IO	VREFB2N1		18	G4	H3						

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B2	VREFB2N1	VCCIO2			19								
B2	VREFB2N1	IO					J4						DQ1L17
B2	VREFB2N1	IO	LVDS16p		20	E1	J1	DPCLK0/ DQS0L	DPCLK0/ DQS0L	DPCLK0/ DQS0L	DPCLK0/ DQS0L	DPCLK0/ DQS0L	DPCLK0/ DQS0L
B2	VREFB2N1	IO	LVDS16n		21	E2	J2	DQ0L7	DQ1L7	DQ0L5	DQ1L5		
B2	VREFB2N1	TDI		TDI	22	H5	K5						
B2	VREFB2N1	TCK		TCK	23	F2	K2						
B2	VREFB2N1	TMS		TMS	24	G1	K6						
B2	VREFB2N1	TDO		TDO	25	G2	L5						
B2	VREFB2N1	DCLK	DCLK	DCLK	26	H4	L6						
B2	VREFB2N1	DATA0	DATA0	DATA0	27	F1	K4						
B2	VREFB2N1	VCCINT			28								
B2	VREFB2N1	nCE		nCE	29	G5	K1						
B2	VREFB2N1	CLK0	LVDSCLK0p/input(3)		30	H2	L1						
B2	VREFB2N1	CLK1	LVDSCLK0n/input(3)		31	H1	L2						
B2	VREFB2N1	GND			32								
B2	VREFB2N1	nCONFIG		nCONFIG	33	J5	L4						
B1	VREFB1N0	CLK2	LVDSCLK1p/input(3)		34	J2	M1						
B1	VREFB1N0	CLK3	LVDSCLK1n/input(3)		35	J1	M2						
B1	VREFB1N0	VCCIO1			36								
B1	VREFB1N0	IO	LVDS15p		37	K2	M5	DPCLK1/ DQS1L	DPCLK1/ DQS1L	DPCLK1/ DQS1L	DPCLK1/ DQS1L	DPCLK1/ DQS1L	DPCLK1/ DQS1L
B1	VREFB1N0	IO	LVDS15n		38	K1	M6		DQ1L8	DQ0L6	DQ1L6		
B1	VREFB1N0	IO	LVDS14p		39	K4	N1	DM0L	DM1L0/ BWS#1L0	DQ0L7	DQ1L7	DM0L	DM1L1/ BWS#1L1
B1	VREFB1N0	VCCINT			40								
B1	VREFB1N0	IO	LVDS14n		41	K5	N2	DQ1L0	DQ1L9		DQ1L8	DQ1L0	DQ3L0
B1	VREFB1N0	GND											
B1	VREFB1N0	IO	LVDS13p		42	L1	P1	DQ1L1	DQ1L10	DM0L	DM1L0/ BWS#1L0	DQ1L1	DQ3L1
B1	VREFB1N0	GND			43								
B1	VREFB1N0	IO	LVDS13n			L2	P2			DQ1L0	DQ1L9	DQ1L2	DQ3L2
B1	VREFB1N0	IO					N6					DQ1L3	DQ3L3
B1	VREFB1N0	IO	VREFB1N0		44	J4	P3						
B1	VREFB1N0	VCCIO1											
B1	VREFB1N0	IO	LVDS12p				N3					DQ1L4	DQ3L4
B1	VREFB1N0	IO	LVDS12n				N4					DQ1L5	DQ3L5
B1	VREFB1N0	IO	LVDS11p				R8						
B1	VREFB1N0	IO	LVDS11n				R7						
B1	VREFB1N0	IO	LVDS10p				P5					DQ1L6	DQ3L6

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B1	VREFB1N0	IO	LVDS10n				P6					DQ1L7	DQ3L7
B1	VREFB1N0	IO	LVDS9p				R1					DQ1L8	DQ3L8
B1	VREFB1N0	GND			45								
B1	VREFB1N0	IO	LVDS9n				R2					DM1L/ BWS#1L	DM3L0/ BWS#3L0
B1	VREFB1N0	IO	LVDS8p				T1						
B1	VREFB1N0	IO	LVDS8n				T2						
B1	VREFB1N1	IO	LVDS7p		46	M1	U1	CDPCLK1/ DQS3L	CDPCLK1/ DQS3L	CDPCLK1/ DQS3L	CDPCLK1/ DQS3L	CDPCLK1/ DQS3L	CDPCLK1/ DQS3L
B1	VREFB1N1	IO	LVDS7n		47	M2	U2	DQ1L2	DQ1L11	DQ1L1	DQ1L10		
B1	VREFB1N1	VCCIO1											
B1	VREFB1N1	IO	LVDS6p				R5					DQ3L0	DQ3L9
B1	VREFB1N1	IO	LVDS6n				R6					DQ3L1	DQ3L10
B1	VREFB1N1	IO	LVDS5p				V1					DQ3L2	DQ3L11
B1	VREFB1N1	IO	LVDS5n				V2					DQ3L3	DQ3L12
B1	VREFB1N1	IO	LVDS4p				T5					DQ3L4	DQ3L13
B1	VREFB1N1	IO	LVDS4n				T6						
B1	VREFB1N1	IO				M3	T3			DQ1L2	DQ1L11		
B1	VREFB1N1	GND			48								
B1	VREFB1N1	IO	VREFB1N1		49	L3	U3						
B1	VREFB1N1	IO	LVDS3p		50	N1	W1	DQ1L3	DQ1L12	DQ1L3	DQ1L12	DQ3L5	DQ3L14
B1	VREFB1N1	IO	LVDS3n		51	N2	W2	DQ1L4	DQ1L13	DQ1L4	DQ1L13	DQ3L6	DQ3L15
B1	VREFB1N1	IO	LVDS2p		52	P1	Y1	DQ1L5	DQ1L14	DQ1L5	DQ1L14	DQ3L7	DQ3L16
B1	VREFB1N1	IO	LVDS2n			P2	Y2			DQ1L6	DQ1L15	DQ3L8	DQ3L17
B1	VREFB1N1	VCCIO1			53								
B1	VREFB1N1	IO	LVDS1p				W3					DM3L/ BWS#3L	DM3L1/ BWS#3L1
B1	VREFB1N1	IO	LVDS1n				W4						
B1	VREFB1N1	IO	LVDS0p		54	N3	Y3	DQ1L6	DQ1L15	DQ1L7	DQ1L16		
B1	VREFB1N1	IO	LVDS0n		55	N4	Y4	DQ1L7	DQ1L16	DQ1L8	DQ1L17		
B1	VREFB1N1	IO			56	P3	W5	DQ1L8	DQ1L17	DM1L/ BWS#1L	DM1L1/ BWS#1L1		
B1	VREFB1N1	IO	PLL1_OUTp		57	L4	U4	DM1L/ BWS#1L	DM1L1/ BWS#1L1				
B1	VREFB1N1	IO	PLL1_OUTn		58	M4	V4						
B1	VREFB1N1	GND											
B1	VREFB1N1	GND_PLL1			59	L5	U5						
B1	VREFB1N1	VCCD_PLL1			60	L6	U6						
B1	VREFB1N1	GND_PLL1			61	N5	V5						

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B8	VREFB8N1	VCCA_PLL1			62	M5	U7						
B8	VREFB8N1	GNDA_PLL1			63	M6	V7						
B8	VREFB8N1	GND											
B8	VREFB8N1	IO	LVDS127n	DEV_OE	64	R3	AA3	DM1B/ BWS#1B	DM1B1/ BWS#1B1				
B8	VREFB8N1	IO	LVDS127p			T3	AB3			DM1B/ BWS#1B	DM1B1/ BWS#1B1		
B8	VREFB8N1	IO	LVDS126p		65	P5	AB4	DQ1B8	DQ1B17	DQ1B8	DQ1B17		
B8	VREFB8N1	IO	LVDS126n		66	P4	AA4	DQ1B7	DQ1B16	DQ1B7	DQ1B16		
B8	VREFB8N1	IO	LVDS125p		67	T4	Y5	DQ1B6	DQ1B15	DQ1B6	DQ1B15		
B8	VREFB8N1	IO	LVDS125n		68	R4	Y6	DQ1B5	DQ1B14	DQ1B5	DQ1B14	DM3B/ BWS#3B	DM3B1/ BWS#3B1
B8	VREFB8N1	VCCIO8			69								
B8	VREFB8N1	IO	LVDS124p		70	T5	AB5	CDPCLK2/ DQS1B	CDPCLK2/ DQS1B	CDPCLK2/ DQS1B	CDPCLK2/ DQS1B	CDPCLK2/ DQS1B	CDPCLK2/ DQS1B
B8	VREFB8N1	GND			71								
B8	VREFB8N1	IO	LVDS124n		72	R5	AA5	DQ1B4	DQ1B13	DQ1B4	DQ1B13		
B8	VREFB8N1	IO	LVDS123p				T8						
B8	VREFB8N1	IO	LVDS123n				T7						
B8	VREFB8N1	IO					U8					DQ3B8	DQ3B17
B8	VREFB8N1	IO	VREFB8N1		73	N7	Y7						
B8	VREFB8N1	IO	LVDS122p				P9						
B8	VREFB8N1	IO	LVDS122n				P8						
B8	VREFB8N1	VCCIO8											
B8	VREFB8N1	IO	LVDS121p				AB6					DQ3B7	DQ3B16
B8	VREFB8N1	GND			74								
B8	VREFB8N1	IO	LVDS121n				AA6					DQ3B6	DQ3B15
B8	VREFB8N1	IO	LVDS120p				V8					DQ3B5	DQ3B14
B8	VREFB8N1	IO	LVDS120n				W7					DQ3B4	DQ3B13
B8	VREFB8N1	GND			75								
B8	VREFB8N1	IO	LVDS119p				W8					DQ3B3	DQ3B12
B8	VREFB8N1	IO	LVDS119n				V9					DQ3B2	DQ3B11
B8	VREFB8N1	IO	LVDS118p				AB7					DQ3B1	DQ3B10
B8	VREFB8N1	VCCINT			76								
B8	VREFB8N1	IO	LVDS118n				AA7					DQ3B0	DQ3B9
B8	VREFB8N1	VCCIO8			77								
B8	VREFB8N0	IO	LVDS117p		78	T6	Y9	DPCLK2/ DQS3B	DPCLK2/ DQS3B	DPCLK2/ DQS3B	DPCLK2/ DQS3B	DPCLK2/ DQS3B	DPCLK2/ DQS3B
B8	VREFB8N0	GND											

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F256	F484	DQS for x8/x9 in Q240	DQS for x16/x18 in Q240	DQS for x8/x9 in F256	DQS for x16/x18 in F256	DQS for x8/x9 in F484	DQS for x16/x18 in F484
B8	VREFB8N0	IO	LVDS117n			R6	W9						
B8	VREFB8N0	IO	LVDS116p		79	P6	U9	DQ1B3	DQ1B12	DQ1B3	DQ1B12	DM5B/ BWS#5B	DM3B0/ BWS#3B0
B8	VREFB8N0	IO	LVDS116n		80	N6	U10	DQ1B2	DQ1B11	DQ1B2	DQ1B11	DQ5B8	DQ3B8
B8	VREFB8N0	GND			81								
B8	VREFB8N0	IO	LVDS115p				R10						
B8	VREFB8N0	IO	LVDS115n				R9						
B8	VREFB8N0	IO	LVDS114p				AB8					DQ5B7	DQ3B7
B8	VREFB8N0	VCCINT			82								
B8	VREFB8N0	IO	LVDS114n				AA8					DQ5B6	DQ3B6
B8	VREFB8N0	VCCIO8			83								
B8	VREFB8N0	IO	VREFB8N0		84	N8	Y10						
B8	VREFB8N0	GND			85								
B8	VREFB8N0	IO	LVDS113p		86	T7	AB9	DQ1B1	DQ1B10	DQ1B1	DQ1B10	DQ5B5	DQ3B5
B8	VREFB8N0	IO	LVDS113n		87	R7	AA9	DQ1B0	DQ1B9	DQ1B0	DQ1B9	DQ5B4	DQ3B4
B8	VREFB8N0	IO	LVDS112p				T11						
B8	VREFB8N0	IO	LVDS112n				R11						
B8	VREFB8N0	IO	LVDS111p				W11					DQ5B3	DQ3B3
B8	VREFB8N0	IO	LVDS111n				V11					DQ5B2	DQ3B2
B8	VREFB8N0	IO	LVDS110p				AB10					DQ5B1	DQ3B1
B8	VREFB8N0	VCCIO8											
B8	VREFB8N0	IO	LVDS110n				AA10					DQ5B0	DQ3B0
B8	VREFB8N0	GND											
B8	VREFB8N0	IO	LVDS109p		88	T8	AB11	DPCLK3/ DQS5B	DPCLK3/ DQS5B	DPCLK3/ DQS5B	DPCLK3/ DQS5B	DPCLK3/ DQS5B	DPCLK3/ DQS5B
B8	VREFB8N0	GND			89								
B8	VREFB8N0	IO	LVDS109n		90	R8	AA11		DM1B0/ BWS#1B0		DM1B0/ BWS#1B0		
B8	VREFB8N0	CLK15	LVDSCLK7p/input(3)		91	T9	U11						
B8	VREFB8N0	CLK14	LVDSCLK7n/input(3)		92	R9	U12						
B8	VREFB8N0	VCCINT			93								
B7	VREFB7N1	CLK13	LVDSCLK6p/input(3)		94	N9	W12						
B7	VREFB7N1	CLK12	LVDSCLK6n/input(3)		95	N10	V12						
B7	VREFB7N1	IO	LVDS108p		96	T11	AB12	DPCLK4/ DQS4B	DPCLK4/ DQS4B	DPCLK4/ DQS4B	DPCLK4/ DQS4B	DPCLK4/ DQS4B	DPCLK4/ DQS4B
B7	VREFB7N1	VCCIO7											
B7	VREFB7N1	IO	LVDS108n		97	R11	AA12	DM0B	DQ1B8	DM0B	DQ1B8		
B7	VREFB7N1	GND											
B7	VREFB7N1	IO	LVDS107p				AB13					DM4B	DM5B1/ BWS#5B1

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B7	VREFB7N1	GND			98								
B7	VREFB7N1	IO	LVDS107n				AA13						DQ5B17
B7	VREFB7N1	IO	LVDS106p				T12						
B7	VREFB7N1	IO	LVDS106n				U13					DQ4B7	DQ5B16
B7	VREFB7N1	VCCINT			99								
B7	VREFB7N1	IO	VREFB7N1		100	P11	Y13						
B7	VREFB7N1	IO					R12						
B7	VREFB7N1	IO	LVDS105p				AB14					DQ4B6	DQ5B15
B7	VREFB7N1	VCCIO7			101								
B7	VREFB7N1	IO	LVDS105n				AA14					DQ4B5	DQ5B14
B7	VREFB7N1	GND			102								
B7	VREFB7N1	IO	LVDS104p				AB15					DQ4B4	DQ5B13
B7	VREFB7N1	GND			103								
B7	VREFB7N1	IO	LVDS104n				AA15					DQ4B3	DQ5B12
B7	VREFB7N1	IO	LVDS103p				AB16					DQ4B2	DQ5B11
B7	VREFB7N1	IO	LVDS103n				AA16					DQ4B1	DQ5B10
B7	VREFB7N1	VCCINT			104								
B7	VREFB7N1	IO	LVDS102p				W14					DQ4B0	DQ5B9
B7	VREFB7N1	IO	LVDS102n				V14					DM2B	DM5B0/ BWS#5B0
B7	VREFB7N1	IO	LVDS101p		105	R10	AB17	DPCLK5/ DQS2B	DPCLK5/ DQS2B	DPCLK5/ DQS2B	DPCLK5/ DQS2B	DPCLK5/ DQS2B	DPCLK5/ DQS2B
B7	VREFB7N1	VCCIO7											
B7	VREFB7N1	IO	LVDS101n		106	T10	AA17	DQ0B7	DQ1B7	DQ0B7	DQ1B7		
B7	VREFB7N1	GND											
B7	VREFB7N0	IO					R13						
B7	VREFB7N0	GND			107								
B7	VREFB7N0	IO	LVDS100p				U14						DQ5B8
B7	VREFB7N0	IO	LVDS100n				T15						
B7	VREFB7N0	IO	LVDS99p				Y14					DQ2B7	DQ5B7
B7	VREFB7N0	VCCINT			108								
B7	VREFB7N0	IO	LVDS99n				W15					DQ2B6	DQ5B6
B7	VREFB7N0	IO	LVDS98p				R14						
B7	VREFB7N0	IO	LVDS98n				R15						
B7	VREFB7N0	VCCIO7											
B7	VREFB7N0	IO	LVDS97p		109	P12	AB18	DQ0B6	DQ1B6	DQ0B6	DQ1B6	DQ2B5	DQ5B5
B7	VREFB7N0	GND											
B7	VREFB7N0	IO	LVDS97n		110	P13	AA18	DQ0B5	DQ1B5	DQ0B5	DQ1B5	DQ2B4	DQ5B4
B7	VREFB7N0	IO	VREFB7N0		111	N11	Y16						

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F256	F484	DQS for x8/x9 in Q240	DQS for x16/x18 in Q240	DQS for x8/x9 in F256	DQS for x16/x18 in F256	DQS for x8/x9 in F484	DQS for x16/x18 in F484
B7	VREFB7N0	IO	LVDS96p				R16						
B7	VREFB7N0	GND			112								
B7	VREFB7N0	IO	LVDS96n				T16						
B7	VREFB7N0	IO	LVDS95p		113	T12	U15	CDPCLK3/ DQS0B	CDPCLK3/ DQS0B	CDPCLK3/ DQS0B	CDPCLK3/ DQS0B	CDPCLK3/ DQS0B	CDPCLK3/ DQS0B
B7	VREFB7N0	IO	LVDS95n		114	R12	V15	DQ0B4	DQ1B4	DQ0B4	DQ1B4		
B7	VREFB7N0	VCCIO7			115								
B7	VREFB7N0												
B7	VREFB7N0	IO	LVDS94p				Y17					DQ2B3	DQ5B3
B7	VREFB7N0	IO	LVDS94n				W16					DQ2B2	DQ5B2
B7	VREFB7N0	IO	LVDS93p		116	T13	AB19	DQ0B3	DQ1B3	DQ0B3	DQ1B3	DQ2B1	DQ5B1
B7	VREFB7N0	IO	LVDS93n		117	R13	AA19	DQ0B2	DQ1B2	DQ0B2	DQ1B2	DQ2B0	DQ5B0
B7	VREFB7N0	IO	LVDS92p		118	T14	AB20	DQ0B1	DQ1B1	DQ0B1	DQ1B1		
B7	VREFB7N0	IO	LVDS92n		119	R14	AA20	DQ0B0	DQ1B0	DQ0B0	DQ1B0		
B7	VREFB7N0	GND											
B7	VREFB7N0	GNDA_PLL4			120	M11	V16						
B7	VREFB7N0	VCCA_PLL4			121	L11	U16						
B6	VREFB6N1	GND_PLL4			122	N12	V18						
B6	VREFB6N1	VCCD_PLL4			123	M12	U17						
B6	VREFB6N1	GND_PLL4			124	L12	T17						
B6	VREFB6N1	GND											
B6	VREFB6N1	IO			125	K13	Y18						
B6	VREFB6N1	IO	LVDS91n	INIT_DONE	126	N13	V19						
B6	VREFB6N1	IO	LVDS91p	nCEO	127	N14	W20						
B6	VREFB6N1	IO	LVDS90n				Y19						
B6	VREFB6N1	IO	LVDS90p				Y20					DM3R/ BWS#3R	DM3R1/ BWS#3R1
B6	VREFB6N1	IO	PLL4_OUTn		128	P15	U18	DM1R/ BWS#1R	DM1R1/ BWS#1R1	DM1R/ BWS#1R	DM1R1/ BWS#1R1		
B6	VREFB6N1	VCCIO6			129								
B6	VREFB6N1	IO	PLL4_OUTp		130	P16	T18	DQ1R8	DQ1R17	DQ1R8	DQ1R17		
B6	VREFB6N1	IO	LVDS89n		131	N15	U19	DQ1R7	DQ1R16	DQ1R7	DQ1R16	DQ3R8	DQ3R17
B6	VREFB6N1	IO	LVDS89p		132	N16	V20	DQ1R6	DQ1R15	DQ1R6	DQ1R15	DQ3R7	DQ3R16
B6	VREFB6N1	IO	LVDS88n				W21					DQ3R6	DQ3R15
B6	VREFB6N1	IO	LVDS88p				W22					DQ3R5	DQ3R14
B6	VREFB6N1	GND			133								
B6	VREFB6N1	IO	VREFB6N1		134	M14	U20						
B6	VREFB6N1	IO			135	P14	R17	DQ1R5	DQ1R14	DQ1R5	DQ1R14	DQ3R4	DQ3R13
B6	VREFB6N1	IO	LVDS87n				Y21					DQ3R3	DQ3R12

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F256	F484	DQS for x8/x9 in Q240	DQS for x16/x18 in Q240	DQS for x8/x9 in F256	DQS for x16/x18 in F256	DQS for x8/x9 in F484	DQS for x16/x18 in F484
B6	VREFB6N1	IO	LVDS87p				Y22					DQ3R2	DQ3R11
B6	VREFB6N1	IO	LVDS86n				V21					DQ3R1	DQ3R10
B6	VREFB6N1	IO	LVDS86p				V22					DQ3R0	DQ3R9
B6	VREFB6N1	IO	LVDS85n		136	M15	U21	DQ1R4	DQ1R13	DQ1R4	DQ1R13		
B6	VREFB6N1	VCCIO6											
B6	VREFB6N1	IO	LVDS85p		137	M16	U22	CDPCLK4/ DQS3R	CDPCLK4/ DQS3R	CDPCLK4/ DQS3R	CDPCLK4/ DQS3R	CDPCLK4/ DQS3R	CDPCLK4/ DQS3R
B6	VREFB6N0	IO	LVDS84n				R18					DM1R/ BWS#1R	DM3R0/ BWS#3R0
B6	VREFB6N0	IO	LVDS84p				R19					DQ1R8	DQ3R8
B6	VREFB6N0	IO	LVDS83n				P17					DQ1R7	DQ3R7
B6	VREFB6N0	IO	LVDS83p				P18					DQ1R6	DQ3R6
B6	VREFB6N0	GND			138								
B6	VREFB6N0	IO	LVDS82n				T21					DQ1R5	DQ3R5
B6	VREFB6N0	IO	LVDS82p				T22					DQ1R4	DQ3R4
B6	VREFB6N0	IO	LVDS81n				R21					DQ1R3	DQ3R3
B6	VREFB6N0	IO	LVDS81p				R22					DQ1R2	DQ3R2
B6	VREFB6N0	IO	VREFB6N0		139	L14	R20						
B6	VREFB6N0	IO	LVDS80n		140	L15	P15	DQ1R3	DQ1R12	DQ1R3	DQ1R12		
B6	VREFB6N0	IO	LVDS80p		141	L16	N15	DQ1R2	DQ1R11	DQ1R2	DQ1R11		
B6	VREFB6N0	VCCIO6			142								
B6	VREFB6N0	nSTATUS		nSTATUS	143	M13	N20						
B6	VREFB6N0	GND											
B6	VREFB6N0	CONF_DONE		CONF_DONE	144	L13	N18						
B6	VREFB6N0	GND			145								
B6	VREFB6N0	MSEL1		MSEL1	146	K12	N17						
B6	VREFB6N0	MSEL0		MSEL0	147	J13	M17						
B6	VREFB6N0	IO	LVDS79n				N21					DQ1R1	DQ3R1
B6	VREFB6N0	VCCINT			148								
B6	VREFB6N0	IO	LVDS79p				N22					DQ1R0	DQ3R0
B6	VREFB6N0	VCCIO6											
B6	VREFB6N0	IO	LVDS78n		149	K16	M19	DQ1R1	DQ1R10	DQ1R1	DQ1R10		
B6	VREFB6N0	IO	LVDS78p		150	K15	M18	DPCLK6/ DQS1R	DPCLK6/ DQS1R	DPCLK6/ DQS1R	DPCLK6/ DQS1R	DPCLK6/ DQS1R	DPCLK6/ DQS1R
B6	VREFB6N0	CLK7	LVDSCLK3n/input(3)		151	J16	M21						
B6	VREFB6N0	CLK6	LVDSCLK3p/input(3)		152	J15	M22						
B5	VREFB5N1	CLK5	LVDSCLK2n/input(3)		153	H15	L21						
B5	VREFB5N1	CLK4	LVDSCLK2p/input(3)		154	H16	L22						
B5	VREFB5N1	IO	LVDS77n		155	H12	L19	DQ1R0	DQ1R9	DQ1R0	DQ1R9		

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F256	F484	DQS for x8/x9 in Q240	DQS for x16/x18 in Q240	DQS for x8/x9 in F256	DQS for x16/x18 in F256	DQS for x8/x9 in F484	DQS for x16/x18 in F484
B5	VREFB5N1	IO	LVDS77p		156	J12	L18	DPCLK7/ DQS0R	DPCLK7/ DQS0R	DPCLK7/ DQS0R	DPCLK7/ DQS0R	DPCLK7/ DQS0R	DPCLK7/ DQS0R
B5	VREFB5N1	IO	LVDS76n		157	G16	K21	DM0R	DM1R0/ BWS#1R0	DM0R	DM1R0/ BWS#1R0	DM0R	DM1R1/ BWS#1R1
B5	VREFB5N1	VCCINT			158								
B5	VREFB5N1	IO	LVDS76p		159	G15	K22		DQ1R8		DQ1R8		DQ1R17
B5	VREFB5N1	VCCIO5			160								
B5	VREFB5N1	IO	LVDS75n		161	F15	J21	DQ0R7	DQ1R7	DQ0R7	DQ1R7	DQ0R7	DQ1R16
B5	VREFB5N1	GND											
B5	VREFB5N1	IO	LVDS75p		162	F16	J22	DQ0R6	DQ1R6	DQ0R6	DQ1R6	DQ0R6	DQ1R15
B5	VREFB5N1	GND			163								
B5	VREFB5N1	IO	LVDS74n				J20					DQ0R5	DQ1R14
B5	VREFB5N1	IO	LVDS74p				H19					DQ0R4	DQ1R13
B5	VREFB5N1	IO	VREFB5N1		164	H13	K20						
B5	VREFB5N1	VCCIO5											
B5	VREFB5N1	IO	LVDS73n		165	G12	J19	DQ0R5	DQ1R5	DQ0R5	DQ1R5	DQ0R3	DQ1R12
B5	VREFB5N1	IO	LVDS73p		166	G13	J18	DQ0R4	DQ1R4	DQ0R4	DQ1R4	DQ0R2	DQ1R11
B5	VREFB5N1	IO	LVDS72n		167	E13	J17	DQ0R3	DQ1R3	DQ0R3	DQ1R3	DQ0R1	DQ1R10
B5	VREFB5N1	IO	LVDS72p		168	F13	H16	DQ0R2	DQ1R2	DQ0R2	DQ1R2		
B5	VREFB5N1	IO					J15						
B5	VREFB5N1	GND			169								
B5	VREFB5N1	IO	LVDS71n				G21					DQ0R0	DQ1R9
B5	VREFB5N1	IO	LVDS71p				G22					DM2R	DM1R0/ BWS#1R0
B5	VREFB5N0	IO	LVDS70n		170	D15	F21						
B5	VREFB5N0	IO	LVDS70p		171	D16	F22	CDPCLK5/ DQS2R	CDPCLK5/ DQS2R	CDPCLK5/ DQS2R	CDPCLK5/ DQS2R	CDPCLK5/ DQS2R	CDPCLK5/ DQS2R
B5	VREFB5N0	IO	LVDS69n				H18						DQ1R8
B5	VREFB5N0	IO	LVDS69p				H17					DQ2R7	DQ1R7
B5	VREFB5N0	IO	LVDS68n			E15	E21			DQ0R1	DQ1R1	DQ2R6	DQ1R6
B5	VREFB5N0	VCCIO5											
B5	VREFB5N0	IO	LVDS68p			E16	E22			DQ0R0	DQ1R0	DQ2R5	DQ1R5
B5	VREFB5N0	IO	LVDS67n				D21					DQ2R4	DQ1R4
B5	VREFB5N0	IO	LVDS67p				D22						
B5	VREFB5N0	IO	LVDS66n				G17					DQ2R3	DQ1R3
B5	VREFB5N0	IO	LVDS66p				G18					DQ2R2	DQ1R2
B5	VREFB5N0	GND			172								
B5	VREFB5N0	IO	VREFB5N0		173	F14	G20						
B5	VREFB5N0	IO	LVDS65n				E20					DQ2R1	DQ1R1

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F256	F484	DQS for x8/x9 in Q240	DQS for x16/x18 in Q240	DQS for x8/x9 in F256	DQS for x16/x18 in F256	DQS for x8/x9 in F484	DQS for x16/x18 in F484
B5	VREFB5N0	IO	LVDS65p				F20					DQ2R0	DQ1R0
B5	VREFB5N0	IO	LVDS64n		174	C15	C21	DQ0R1	DQ1R1				
B5	VREFB5N0	IO	LVDS64p		175	C16	C22	DQ0R0	DQ1R0				
B5	VREFB5N0	VCCIO5			176								
B5	VREFB5N0	IO	LVDS63n				C19						
B5	VREFB5N0	IO	LVDS63p				C20						
B5	VREFB5N0	IO	LVDS62n			C14	D19						
B5	VREFB5N0	IO	LVDS62p			D13	D20						
B5	VREFB5N0	IO	PLL2_OUTp		177	E14	E19						
B5	VREFB5N0	IO	PLL2_OUTn		178	D14	E18						
B5	VREFB5N0	GND											
B5	VREFB5N0	GND_PLL2			179	F12	F18						
B5	VREFB5N0	VCCD_PLL2			180	F11	F17						
B5	VREFB5N0	GND_PLL2			181	D12	E17						
B4	VREFB4N0	VCCA_PLL2			182	E12	F16						
B4	VREFB4N0	GNDA_PLL2			183	E11	E16						
B4	VREFB4N0	GND											
B4	VREFB4N0	IO	LVDS61n		184	B14	C18						
B4	VREFB4N0	IO	LVDS61p		185	A14	C17	DQ0T0	DQ1T0	DQ0T0	DQ1T0		
B4	VREFB4N0	IO	LVDS60n		186	C13	B20	DQ0T1	DQ1T1	DQ0T1	DQ1T1	DQ2T0	DQ5T0
B4	VREFB4N0	IO	LVDS60p		187	C12	A20	DQ0T2	DQ1T2	DQ0T2	DQ1T2	DQ2T1	DQ5T1
B4	VREFB4N0	IO	LVDS59n		188	B13	B19	DQ0T3	DQ1T3	DQ0T3	DQ1T3	DQ2T2	DQ5T2
B4	VREFB4N0	IO	LVDS59p		189	A13	A19	DQ0T4	DQ1T4	DQ0T4	DQ1T4	DQ2T3	DQ5T3
B4	VREFB4N0												
B4	VREFB4N0	VCCIO4			190								
B4	VREFB4N0	IO	LVDS58n		191	B12	B18	DQ0T5	DQ1T5	DQ0T5	DQ1T5		
B4	VREFB4N0	IO	LVDS58p		192	A12	A18	CDPCLK6/ DQS0T	CDPCLK6/ DQS0T	CDPCLK6/ DQS0T	CDPCLK6/ DQS0T	CDPCLK6/ DQS0T	CDPCLK6/ DQS0T
B4	VREFB4N0	IO	LVDS57n				G16						
B4	VREFB4N0	GND			193								
B4	VREFB4N0	IO	LVDS57p				H15						
B4	VREFB4N0	IO	VREFB4N0		194	C11	C16						
B4	VREFB4N0	IO	LVDS56n				D16					DQ2T4	DQ5T4
B4	VREFB4N0	GND											
B4	VREFB4N0	IO	LVDS56p				E15					DQ2T5	DQ5T5
B4	VREFB4N0	VCCIO4											
B4	VREFB4N0	IO	LVDS55n				H14						
B4	VREFB4N0	IO	LVDS55p				J14						

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F256	F484	DQS for x8/x9 in Q240	DQS for x16/x18 in Q240	DQS for x8/x9 in F256	DQS for x16/x18 in F256	DQS for x8/x9 in F484	DQS for x16/x18 in F484
B4	VREFB4N0	IO	LVDS54n		195	B11	D15	DQ0T6	DQ1T6	DQ0T6	DQ1T6	DQ2T6	DQ5T6
B4	VREFB4N0	VCCINT			196								
B4	VREFB4N0	IO	LVDS54p		197	A11	C14	DQ0T7	DQ1T7	DQ0T7	DQ1T7	DQ2T7	DQ5T7
B4	VREFB4N0	IO	LVDS53n				G15						
B4	VREFB4N0	IO	LVDS53p				F15						DQ5T8
B4	VREFB4N0	GND			198								
B4	VREFB4N1	IO					H13						
B4	VREFB4N1	GND											
B4	VREFB4N1	IO	LVDS52n		199	B10	B17		DQ1T8		DQ1T8		
B4	VREFB4N1	VCCIO4											
B4	VREFB4N1	IO	LVDS52p		200	A10	A17	DPCLK8/ DQS2T	DPCLK8/ DQS2T	DPCLK8/ DQS2T	DPCLK8/ DQS2T	DPCLK8/ DQS2T	DPCLK8/ DQS2T
B4	VREFB4N1	IO	LVDS51n				E14					DM2T	DM5T0/ BWS#5T0
B4	VREFB4N1	IO	LVDS51p				D14					DQ4T0	DQ5T9
B4	VREFB4N1	VCCINT			201								
B4	VREFB4N1	IO	LVDS50n				F14					DQ4T1	DQ5T10
B4	VREFB4N1	IO	LVDS50p				F13					DQ4T2	DQ5T11
B4	VREFB4N1	IO	LVDS49n				B16					DQ4T3	DQ5T12
B4	VREFB4N1	GND			202								
B4	VREFB4N1	IO	LVDS49p				A16					DQ4T4	DQ5T13
B4	VREFB4N1	GND											
B4	VREFB4N1	IO	LVDS48n				B15					DQ4T5	DQ5T14
B4	VREFB4N1	VCCIO4											
B4	VREFB4N1	IO	LVDS48p				A15					DQ4T6	DQ5T15
B4	VREFB4N1	IO					H12						
B4	VREFB4N1	IO	VREFB4N1		203	D9	C13						
B4	VREFB4N1	VCCINT			204								
B4	VREFB4N1	IO	LVDS47n				F12					DQ4T7	DQ5T16
B4	VREFB4N1	IO	LVDS47p				G12						
B4	VREFB4N1	IO	LVDS46n				B14						DQ5T17
B4	VREFB4N1	GND			205								
B4	VREFB4N1	IO	LVDS46p				A14					DM4T	DM5T1/ BWS#5T1
B4	VREFB4N1	GND			206								
B4	VREFB4N1	IO	LVDS45n			D11	B13			DM0T	DM1T0/ BWS#1T0		
B4	VREFB4N1	VCCIO4			207								
B4	VREFB4N1	IO	LVDS45p		208	D10	A13	DPCLK9/ DQS4T	DPCLK9/ DQS4T	DPCLK9/ DQS4T	DPCLK9/ DQS4T	DPCLK9/ DQS4T	DPCLK9/ DQS4T

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F256	F484	DQS for x8/x9 in Q240	DQS for x16/x18 in Q240	DQS for x8/x9 in F256	DQS for x16/x18 in F256	DQS for x8/x9 in F484	DQS for x16/x18 in F484
B4	VREFB4N1	CLK8	LVDSCLK4n/input(3)		209	A9	B12						
B4	VREFB4N1	CLK9	LVDSCLK4p/input(3)		210	B9	A12						
B3	VREFB3N0	VCCINT			211								
B3	VREFB3N0	CLK10	LVDSCLK5n/input(3)		212	A8	D12						
B3	VREFB3N0	CLK11	LVDSCLK5p/input(3)		213	B8	E12						
B3	VREFB3N0	IO	LVDS44n		214	A7	B11	DM0T	DM1T0/ BWS#1T0	DQ1T0	DQ1T9		
B3	VREFB3N0	GND			215								
B3	VREFB3N0	IO	LVDS44p		216	B7	A11	DPCLK10/ DQS5T	DPCLK10/ DQS5T	DPCLK10/ DQS5T	DPCLK10/ DQS5T	DPCLK10/ DQS5T	DPCLK10/ DQS5T
B3	VREFB3N0	GND											
B3	VREFB3N0	IO	LVDS43n				E11					DQ5T0	DQ3T0
B3	VREFB3N0	VCCIO3											
B3	VREFB3N0	IO	LVDS43p				D11					DQ5T1	DQ3T1
B3	VREFB3N0	IO	LVDS42n				H11						
B3	VREFB3N0	IO	LVDS42p				G11						
B3	VREFB3N0	IO	LVDS41n				B10					DQ5T2	DQ3T2
B3	VREFB3N0	IO	LVDS41p				A10					DQ5T3	DQ3T3
B3	VREFB3N0	IO	LVDS40n				F11					DQ5T4	DQ3T4
B3	VREFB3N0	IO	LVDS40p				F10					DQ5T5	DQ3T5
B3	VREFB3N0	GND			217								
B3	VREFB3N0	IO	VREFB3N0		218	D8	C10						
B3	VREFB3N0	VCCIO3			219								
B3	VREFB3N0	IO	LVDS39n				B9					DQ5T6	DQ3T6
B3	VREFB3N0	VCCINT			220								
B3	VREFB3N0	IO	LVDS39p				A9					DQ5T7	DQ3T7
B3	VREFB3N0	IO	LVDS38n				H10						
B3	VREFB3N0	IO	LVDS38p				H9						
B3	VREFB3N0	GND			221								
B3	VREFB3N0	IO	LVDS37n				E9					DQ5T8	DQ3T8
B3	VREFB3N0	IO	LVDS37p				D9					DM5T/ BWS#5T	DM3T0/ BWS#3T0
B3	VREFB3N0	IO	LVDS36n		222	B6	B8	DQ1T0	DQ1T9	DQ1T1	DQ1T10		
B3	VREFB3N0	GND											
B3	VREFB3N0	IO	LVDS36p		223	A6	A8	DPCLK11/ DQS3T	DPCLK11/ DQS3T	DPCLK11/ DQS3T	DPCLK11/ DQS3T	DPCLK11/ DQS3T	DPCLK11/ DQS3T
B3	VREFB3N1	VCCIO3											
B3	VREFB3N1	IO	LVDS35n				B7					DQ3T0	DQ3T9
B3	VREFB3N1	VCCINT			224								
B3	VREFB3N1	IO	LVDS35p				A7					DQ3T1	DQ3T10

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F256	F484	DQS for x8/x9 in Q240	DQS for x16/x18 in Q240	DQS for x8/x9 in F256	DQS for x16/x18 in F256	DQS for x8/x9 in F484	DQS for x16/x18 in F484
B3	VREFB3N1	IO	LVDS34n				F9					DQ3T2	DQ3T11
B3	VREFB3N1	IO	LVDS34p				E8					DQ3T3	DQ3T12
B3	VREFB3N1	GND			225								
B3	VREFB3N1	IO	LVDS33n				D8					DQ3T4	DQ3T13
B3	VREFB3N1	IO	LVDS33p				C9					DQ3T5	DQ3T14
B3	VREFB3N1	IO			226	D7	D7	DQ1T1	DQ1T10	DQ1T2	DQ1T11	DQ3T6	DQ3T15
B3	VREFB3N1	GND			227								
B3	VREFB3N1	IO	LVDS32n		228	D6	F8	DQ1T2	DQ1T11	DQ1T3	DQ1T12	DQ3T7	DQ3T16
B3	VREFB3N1	VCCIO3			229								
B3	VREFB3N1	IO	LVDS32p		230	C6	G8	DQ1T3	DQ1T12	DQ1T4	DQ1T13		
B3	VREFB3N1	IO					H8						
B3	VREFB3N1	IO	VREFB3N1		231	C5	C7						
B3	VREFB3N1	IO			232	C4	E7	DQ1T4	DQ1T13	DQ1T5	DQ1T14	DQ3T8	DQ3T17
B3	VREFB3N1	IO	LVDS31n				G7						
B3	VREFB3N1	IO	LVDS31p				H7						
B3	VREFB3N1	IO	LVDS30n		233	B5	B6	DQ1T5	DQ1T14	DQ1T6	DQ1T15		
B3	VREFB3N1	GND											
B3	VREFB3N1	IO	LVDS30p		234	A5	A6	CDPCLK7/ DQS1T	CDPCLK7/ DQS1T	CDPCLK7/ DQS1T	CDPCLK7/ DQS1T	CDPCLK7/ DQS1T	CDPCLK7/ DQS1T
B3	VREFB3N1	VCCIO3											
B3	VREFB3N1	IO	LVDS29n				B5					DM3T/ BWS#3T	DM3T1/ BWS#3T1
B3	VREFB3N1	IO	LVDS29p				A5						
B3	VREFB3N1	IO	LVDS28n		235	B4	B4	DQ1T6	DQ1T15	DQ1T7	DQ1T16		
B3	VREFB3N1	IO	LVDS28p		236	A4	A4	DQ1T7	DQ1T16	DQ1T8	DQ1T17		
B3	VREFB3N1	IO	LVDS27p		237	A3	A3	DQ1T8	DQ1T17	DM1T/ BWS#1T	DM1T1/ BWS#1T1		
B3	VREFB3N1	IO	LVDS27n	DEV_CLRn	238	B3	B3	DM1T/ BWS#1T	DM1T1/ BWS#1T1				
B3	VREFB3N1	GND											
B3	VREFB3N1	GNDA_PLL3			239	E6	F7						
B3	VREFB3N1	VCCA_PLL3			240	F6	E6						
		VCCINT				F9	J10						
		VCCINT				F10	J11						
		VCCINT				G7	J12						
		VCCINT				G9	J13						
		VCCINT				G11	K9						
		VCCINT				H7	K14						
		VCCINT				H10	L9						

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F256	F484	DQS for x8/x9 in Q240	DQS for x16/x18 in Q240	DQS for x8/x9 in F256	DQS for x16/x18 in F256	DQS for x8/x9 in F484	DQS for x16/x18 in F484
		VCCINT				H11	L14						
		VCCINT				J6	M9						
		VCCINT				J7	M14						
		VCCINT				J10	N9						
		VCCINT				K6	N14						
		VCCINT				K8	P10						
		VCCINT				K10	P11						
		VCCINT				L7	P12						
		VCCINT				L8	P13						
		VCCIO2				B1	B1						
		VCCIO2					J7						
		VCCIO2				G3	L3						
		VCCIO1				K3	AA1						
		VCCIO1					M3						
		VCCIO1					P7						
		VCCIO1				R1	T4						
		VCCIO8				M7	AB2						
		VCCIO8					T9						
		VCCIO8				P7	V10						
		VCCIO8					W6						
		VCCIO8				T2	Y11						
		VCCIO7				M10	AB21						
		VCCIO7					T14						
		VCCIO7				P10	V13						
		VCCIO7					W17						
		VCCIO7				T15	Y12						
		VCCIO6				K14	AA22						
		VCCIO6					M20						
		VCCIO6				R16	P16						
		VCCIO6					T19						
		VCCIO5				B16	B22						
		VCCIO5					G19						
		VCCIO5					J16						
		VCCIO5				G14	L20						
		VCCIO4				A15	A21						
		VCCIO4				C10	C12						
		VCCIO4					D17						
		VCCIO4					E13						
		VCCIO4				E10	G14						

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F256	F484	DQS for x8/x9 in Q240	DQS for x16/x18 in Q240	DQS for x8/x9 in F256	DQS for x16/x18 in F256	DQS for x8/x9 in F484	DQS for x16/x18 in F484
		VCCIO3				A2	A2						
		VCCIO3					C6						
		VCCIO3				C7	C11						
		VCCIO3					E10						
		VCCIO3				E7	G9						
		GND				F7	K10						
		GND				F8	K11						
		GND				G6	K12						
		GND				G8	K13						
		GND				G10	L10						
		GND				H6	L11						
		GND				H8	L12						
		GND				H9	L13						
		GND				J8	M10						
		GND				J9	M11						
		GND				J11	M12						
		GND				K7	M13						
		GND				K9	N10						
		GND				K11	N11						
		GND				L9	N12						
		GND				L10	N13						
		GND				A1	A1						
		GND					A22						
		GND				A16	AA2						
		GND				B2	AA21						
		GND					AB1						
		GND					AB22						
		GND				B15	B2						
		GND				C8	B21						
		GND					C5						
		GND					C8						
		GND				C9	C15						
		GND					D10						
		GND				E8	D13						
		GND				E9	D18						
		GND					F19						
		GND				H3	G4						
		GND					G10						
		GND					G13						

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F256	F484	DQS for x8/x9 in Q240	DQS for x16/x18 in Q240	DQS for x8/x9 in F256	DQS for x16/x18 in F256	DQS for x8/x9 in F484	DQS for x16/x18 in F484
		GND				H14	H20						
		GND				J3	K3						
		GND					K7						
		GND					K16						
		GND				J14	K19						
		GND				M8	M4						
		GND					N7						
		GND					N16						
		GND				M9	N19						
		GND				P8	R3						
		GND					T10						
		GND				P9	T13						
		GND					T20						
		GND					V3						
		GND				R2	V6						
		GND				R15	V17						
		GND					W10						
		GND				T1	W13						
		GND					W19						
		GND					Y8						
		GND				T16	Y15						
		NC					G1						
		NC					G2						
		NC					H21						
		NC					H22						
		NC					J3						
		NC					J5						
		NC					J6						
		NC					J8						
		NC					J9						
		NC					K8						
		NC					K15						
		NC					K17						
		NC					K18						
		NC					L7						
		NC					L15						
		NC					L16						
		NC					L17						
		NC					M7						

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F256	F484	DQS for x8/x9 in Q240	DQS for x16/x18 in Q240	DQS for x8/x9 in F256	DQS for x16/x18 in F256	DQS for x8/x9 in F484	DQS for x16/x18 in F484
		NC					M8						
		NC					M15						
		NC					M16						
		NC					N5						
		NC					N8						
		NC					P4						
		NC					P14						
		NC					P19						
		NC					P20						
		NC					P21						
		NC					P22						
		NC					R4						
		NC					W18						

Notes:

(1) The optional functions (e.g. LVDS, DDR) are not available for some pins in certain packages.
For example, for the EP2C8 device, the LVDS70 pair is available for the Q208 and F256 packages, but not for the T144 package.

(2) The DQS0T, DQS1T, DQS0B, and DQS1B pin functions are only available in the F672 and F896 packages.

(3) If the dedicated CLK pins are not used to feed the global clock networks, they can be used as general-purpose input pins to feed the core logic.
The dedicated CLK pins do not support the I/O register.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
		Supply and Reference Pins	
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVPECL, LVDS (regular I/O and CLK pins), differential HSTL, and differential SSTL I/O standards.	Connect all VCCINT pins to 1.2 V. Decoupling depends on the design decoupling requirements of the specific board. *(Note 2)*
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X, differential SSTL, differential HSTL, and LVDS (regular I/O) I/O standards.	Verify that the VCCIO voltage level connected is consistent with the **.pin** report from the Quartus® II software. Decoupling depends on the design decoupling requirements of the specific board. *(Note 2)*
GND	Ground	Device ground pins.	Connect all GND pins to the board GND plane.
VREFB[1..8]N[0..3]	I/O	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-referenced pins for the bank.	If voltage-referenced I/O standards are not used in the bank, the VREF pins are available as user I/O pins. Decoupling depends on the design decoupling requirements of the specific board. *(Note 2)*
VCCA_PLL[1..4]*(Note 4)*	Power	Analog power for PLLs[1..4].	Connect these pins to 1.2 V, even if the PLL is not used. Use an isolated linear supply for better jitter performance. You can connect all VCCA_PLL pins to a single linear supply to minimize cost. Power on the PLLs should be decoupled. Decoupling depends on the design decoupling requirements of the specific board *(Note 2)* . For more information on this pin, refer to the *PLLs in Cyclone II Devices* chapter in the Cyclone II Device Handbook.
VCCD_PLL[1..4]*(Note 4)*	Power	Digital power for PLLs[1..4].	Connect these pins to the quietest digital supply on board (1.2 V), which is also supplied to the VCCINT, even if the PLL is not used. Power on the PLLs should be decoupled. Decoupling depends on the design decoupling requirements of the specific board *(Note 2)* . For more information on this pin, refer to the *PLLs in Cyclone II Devices* chapter in the Cyclone II Device Handbook.
GNDA_PLL[1..4]*(Note 4)*	Ground	Analog ground for PLLs[1..4].	Connect these pins directly to the same ground plane as the digital ground of the device, even if the PLL is not used. For more information on this pin, refer to the *PLLs in Cyclone II Devices* chapter in the Cyclone II Device Handbook.
GND_PLL[1..4]*(Note 4)*	Ground	Ground for PLLs[1..4].	Connect these pins to the GND plane on the board.
NC	No Connect	No Connect	Do not drive signals into these pins.
		Dedicated Configuration/JTAG Pins	
DCLK	Input (PS) Output (AS)	Dedicated configuration clock pin. In PS configuration, DCLK is used to clock configuration data from an external source into the Cyclone II device. In AS mode, DCLK is an output from the Cyclone II device that provides timing for the configuration interface. The input buffer on this pin supports hysteresis using the Schmitt trigger circuitry.	DCLK should not be left floating. You should drive it high or low, whichever is more convenient on the board.
DATA0	Input	Dedicated configuration data input pin. In serial configuration modes, bit-wide configuration data is received through this pin. In AS mode, DATA0 has an internal pull-up resistor that is always active. The input buffer on this pin supports hysteresis using the Schmitt trigger circuitry.	DATA0 should not be left floating. You should drive it high or low, whichever is more convenient on the board.
MSEL[0..1]	Input	Configuration input pins that set the Cyclone II device configuration scheme.	These pins must be hardwired to VCCIO of the bank they reside in or GND. Do not leave these pins floating. When these pins are unused, connect them to GND. For MSEL pin settings for different configuration schemes, refer to the Configuring Cyclone II Devices chapter in the Cyclone II Device Handbook.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled. The input buffer on this pin supports hysteresis using the Schmitt trigger circuitry.	In a multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In a single-device configuration, nCE is tied low.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user mode causes the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level initiates reconfiguration. The input buffer on this pin supports hysteresis using the Schmitt trigger circuitry.	nCONFIG should be pulled high by an external 10-kΩ pull-up resistor to a 3.3-V supply. If the configuration scheme uses an enhanced configuration device or EPC2, nCONFIG can be tied directly to the nINIT_CONF pin of the configuration device. If this pin is not used, this pin can be connected through a resistor to VCCIO.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin. The input buffer on this pin supports hysteresis using the Schmitt trigger circuitry.	CONF_DONE should be pulled high by an external 10-kΩ pull-up resistor to a 3.3-V supply. If internal pull-up resistors on the enhanced configuration device are used, external 10-kΩ pull-up resistors should not be used on this pin.

nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin. The input buffer on this pin supports hysteresis using the Schmitt trigger circuitry.	nSTATUS should be pulled high by an external 10-kΩ pull-up resistor to a 3.3-V supply.
TCK	Input	Dedicated JTAG clock input pin. This pin has weak internal pull-down resistors. The input buffer on this pin supports hysteresis using the Schmitt trigger circuitry.	Connect this pin to GND via a 1-kΩ resistor. If the JTAG circuitry is not used, connect TCK to GND.
TMS	Input	Dedicated JTAG input pin that provides the control signal to determine the transitions of the TAP controller state machine. This pin has weak internal pull-up resistors. The input buffer on this pin supports hysteresis using the Schmitt trigger circuitry.	Connect this pin to a 1-kΩ resistor via the VCCIO of the bank it resides in. If the JTAG circuitry is not used, connect TMS to VCCIO.
TDI	Input	Dedicated JTAG test data input pin for instructions, and test and programming data. This pin has weak internal pull-up resistors. The input buffer on this pin supports hysteresis using the Schmitt trigger circuitry.	Connect this pin to a 1-kΩ resistor via the VCCIO of the bank it resides in. If the JTAG circuitry is not used, connect TDI to VCCIO.
TDO	Output	Dedicated JTAG data output pin for instructions, and test and programming data.	When not in JTAG mode, this pin should be left unconnected.
Clock and PLL Pins			
CLK[0,2,4,6,8,10,12,14], LVDSCLK[0..7]p	Clock, Input	Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins.	Connect unused pins to GND.
CLK[1,3,5,7,9,11,13,15], LVDSCLK[0..7]n	Clock, Input	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins.	Connect unused pins to GND.
PLL[1..4]_OUTp*(Note 4)*	I/O, Output	Optional positive terminal for external clock outputs from PLLs[1..4]. These pins can only use the differential I/O standard if it is being fed by a PLL output.	When not used as PLL output pins, these pins can be used as user I/O pins. When these pins are not used, they may be left floating.
PLL[1..4]_OUTn*(Note 4)*	I/O, Output	Optional negative terminal for external clock outputs from PLLs[1..4]. These pins can only use the differential I/O standard if it is being fed by a PLL output.	When not used as PLL output pins, these pins can be used as user I/O pins. When these pins are not used, they may be left floating.
Optional/Dual-Purpose Configuration Pins			
nCEO	I/O, Output	Output that drives low when device configuration is complete.	During a multi-device configuration, this pin feeds the nCE pin of a subsequent device and must be pulled high to VCCIO by an external 10-kΩ pull-up resistor. During a single-device configuration and for the last device in a multi-device configuration, this pin can be left unconnected or used as an user I/O after configuration.
nCSO	I/O, Output	Output control signal from the Cyclone II FPGA to the nCS pin of the serial configuration device in AS mode that enables the configuration device by driving it low. In AS mode, the nCSO has internal weak pull-up resistor, which is always active.	When not programming the device in AS mode, the nCSO pin can be used as user I/O. When this pin is not used as an I/O, Altera recommends that you leave the pin unconnected.
ASDO	I/O, Output	Output control signal from the Cyclone II FPGA to the serial configuration device in AS mode used to read out configuration data. In AS mode, the ASDO has internal weak pull-up resistor, which is always active.	When not programming the device in AS mode, the ASDO pin can be used as user I/O. When this pin is not used as an I/O, Altera recommends that you leave the pin unconnected.
CRC_ERROR	I/O, Output	Active-high signal that indicates the error-detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error-detection circuit is enabled.	When the dedicated output for CRC_ERROR is not used and this pin is not used as an I/O, Altera recommends that you leave the pin unconnected.
DEV_CLRn	I/O (when option off), Input (when option on)	Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. The DEV_CLRn pin does not affect JTAG boundary-scan or programming operations. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.	When the dedicated output for DEV_CLRn is not used and this pin is not used as an I/O, Altera recommends that you tie this pin to the VCCIO of the bank that it resides in or ground. *(Note 6)*
DEV_OE	I/O (when option off), Input (when option on)	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.	When the dedicated output for DEV_OE is not used and this pin is not used as an I/O, Altera recommends that you tie this pin to the VCCIO of the bank that it resides in or ground. *(Note 6)*
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.	When INIT_DONE is enabled, connect this pin to a 10-kΩ resistor via the VCCIO of the bank that it resides in.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software.	If the CLKUSR pin is not used as a configuration clock input and the pin is not used as an I/O, Altera recommends that you connect this pin to ground.
Dual-Purpose Differential & External Memory Interface Pins			
LVDS[0-256][p,n]*(Note 3)*	I/O, TX/RX channel	Dual-purpose differential transmitter/receiver channels 0 to 256. These channels can be used for transmitting or receiving LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	When these pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND. *(Note 6)*

DPCLK[0..11]/ DQS[[0,1]L,[3,5,4,2]B,[1,0]R,[2,4,5,3]T] *(Note 5)*	I/O, DPCLK/DQS	Dual-purpose DPCLK/DQS pins can connect to the global clock network for high-fanout control signals such as clocks, asynchronous clears, presets, and clock enables. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry, which allows for the fine-tuning of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.	When these pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND. *(Note 6)*
CDPCLK[0..7]/ DQS[[2,3]L,[1,0]B,[3,2]R,[0,1]T]*(Note 5)*	I/O, CDPCLK/DQS	Dual-purpose CDPCLK/DQS pins can connect to the global clock network for high-fanout control signals such as clocks, asynchronous clears, presets, and clock enables. Only one of the two CDPCLK in each corner can feed the clock control block at a time. The other pin can be used as a general-purpose I/O pin. The CDPCLK signals incur more delay to the clock block control because they are multiplexed before being driven into the clock block control. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry, which allows for the fine-tuning of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.	When these pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND. *(Note 6)*
DQ[[[1,3][L,R]],[[3,5][B,T]]][0..17]*(Note 5)*	I/O, DQ	Optional data signal for use in external memory interfacing in the x16 or x18 modes.	When these pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND. *(Note 6)*
DQ[[[0..3][L,R]],[[0..5][B,T]]][0..8]*(Note 5)*	I/O, DQ	Optional data signal for use in external memory interfacing in the x8 or x9 modes.	When these pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND. *(Note 6)*
DM[[[0..3][L,R]],[[0..5][B,T]]]*(Note 5)*	I/O, DM	Optional data mask pins for x8/x9 modes are required when writing to DDR SDRAM and DDR2 SDRAM devices. A low signal indicates that the write is valid. If the DM signal is high, the memory masks the DQ signals. Each group of DQ and DQS signals requires a DM pin.	When these pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND. *(Note 6)*
DM[[[1,3][L,R]],[[3,5][B,T]]][0,1]*(Note 5)*	I/O, DM	Optional data mask pins for x16/x18 modes are required when writing to DDR SDRAM and DDR2 SDRAM devices. A low signal indicates that the write is valid. If the DM signal is high, the memory masks the DQ signals. Each group of DQ and DQS signals requires a DM pin.	When these pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND. *(Note 6)*
DM[[[0..3][L,R]],[[0..5][B,T]]]*(Note 5)*	I/O, BWS	Byte Write Select is an active-low pin. When asserted active, BWS selects which byte is written into the device during write operation. Bytes not written remain unchanged. Deselecting BWS causes write data to be ignored and not written into device.	When these pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND. *(Note 6)*
DM[[[1,3][L,R]],[[3,5][B,T]]][0,1]*(Note 5)*	I/O, BWS	Byte Write Select is an active-low pin. When asserted active, BWS selects which byte is written into the device during write operation. Bytes not written remain unchanged. Deselecting BWS causes write data to be ignored and not written into device.	When these pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND. *(Note 6)*

Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

Notes:

1) These pin connection guidelines are created based on the largest Cyclone II device, EP2C70F896. Refer to the pin list for the availability of pins in each density.

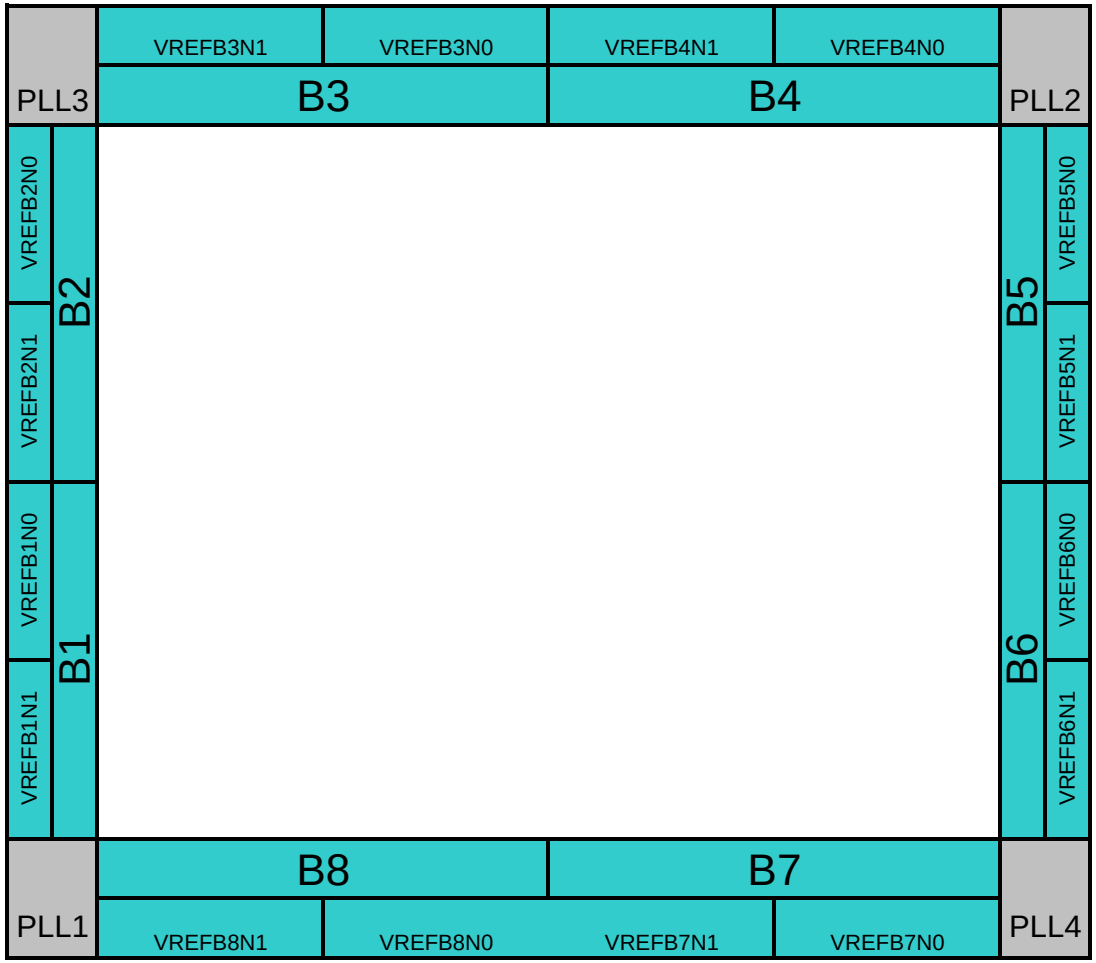
2) Capacitance values for the power supply should be selected after considering the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage droop requirements of the device or supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as interplaning capacitance with low inductance should be considered for higher frequency decoupling.

3) The differential transmitter/receiver channel count for each device and package is different; smaller packages may contain less than the maximum number of differential transmitter/receiver channels. For details on the differential transmitter/receiver channel count for each device, refer to the corresponding pin-out from www.altera.com.

4) The EP2C5, EP2C8, and EP2C8A devices have only PLL1 and PLL2.

5) The DQ, DQS, DM, and BWS# bus mode count for each device and package is different. Smaller packages may contain less than the maximum number of DQ, DQS, DM, and BWS# bus modes. For details on the DQ, DQS, DM, and BWS# bus mode count for each device, refer to the corresponding pin-out from www.altera.com.

6) Make sure that unused pins are set to input tristated in the Quartus II software. For instructions on how to set this, refer to the Quartus II Handbook.



Notes:

1. This is a top view of the silicon die.
2. This is only a pictorial representation to get an idea of placement on the device.
   Refer to the pin list and the Quartus® II software for exact locations.

Pin Information for the Cyclone® II EP2C15A, EP2C20 & EP2C20A Devices
Version 2.1

Version Number	Date	Changes Made
1.0	10/6/2004	Initial revision
1.1	1/10/2005	Added CRC_ERROR pin in Pin List and Pin Definition
		Changed pin name from GNDD_PLL and GNDG_PLL to GND_PLL
		For F256 package:
		LVDS19p changed from pin E1 to E3
		LVDS19n changed from pin E2 to E4
		LVDS16p changed from pin F1 to E1
		LVDS16n changed from pin F2 to E2
		TDI changed from pin G1 to H5
		TCK changed from pin G2 to F2
		TMS changed from pin H5 to J1
		TDO changed from pin E4 to G2
		DATA0 changed from pin E3 to F1
1.2	2/24/2005	Modified Pin Definitions for DATA0 pin
	5/7/2005	Finalize
1.3	5/25/2005	Added Q240 package
1.4	6/2/2005	Modified Pin Type column in Pin Definitions for VREFB[1..8]N[0..1] pins
1.5	2/10/2006	Added footnote for pins that do not support Optional Functions (LVDS, DDR, etc)
		Added footnote for DQS0T, DQS1T, DQS0B and DQS1B pins
		Modified pin definition for NC pins
		Modified Pin Description of VREFB[1..8]N[0..1] pins
		Modified Pin Description of VCCA_PLL[1..4] and VCCD_PLL[1..4] pins
		Added Pin Description for BWS pins
1.6	3/1/2006	Added comment for PLL_OUT pins in Pin Definitions
1.7	5/9/2006	Modified "DQS for x16/x18 in Q240" column from DQ0B[3:0] to DQ1B[3:0] in Pin List
1.8	6/16/2006	Added EP2C15A and EP2C20A support
1.9	11/13/2006	Modified Pin Description of VCCIO and VCCINT.
		Added "I/O" to pin type of pin nCEO, nCSO and ASDO
		Moved nCEO Discription from section "Dedicated Configuration/JTAG Pins" to section "Optional/Dual-Purpose Configuration Pins"
2.0	3/7/2007	Modified Pin Description for MSEL
2.1	5/2/2008	Incorporated pin connection guidelines into pin definitions worksheet.