Technical Brief

# High-Speed Board Design Advisor
## *Power Distribution Network*

## Introduction

This document contains a step-by-step tutorial and checklist of best-practice guidelines to design and review a power distribution network (PDN). Altera provides the Decoupling Design Tool to facilitate the process of selection of the decoupling capacitors for a PDN design. The method described here uses the Frequency Domain Target Impedance Method. Additional PDN-related papers and online lectures can be found in "Further Information".

This document assumes familiarity with the following tools and support collateral:

- *Stratix® II GX Handbook*:
  **www.altera.com/literature/lit-s2gx.jsp**
- Stratix II GX Pinouts:
  **www.altera.com/literature/lit-dp.jsp**
- PowerPlay Early Power Estimator (EPE) Spreadsheet and User Guide:
  **www.altera.com/support/devices/estimator/pow-powerplay.jsp**
- Decoupling Design Tool and User Guide: Available from an Altera sales representative:
  **www.altera.com/corporate/contact/con-index.html**
- *Quartus® II Development Software Handbook*:
  **www.altera.com/literature/lit-qts.jsp**

Altera® Stratix II GX FPGA-based development kits deliver quality-proven implementations and comprise board schematics, layout files, and board-specific guidelines documents which can be used as a starting point for user designs:

- Transceiver Signal Integrity Development Kit, Stratix II GX Edition:
  **www.altera.com/products/devkits/altera/kit-signal_integrity_s2gx.html**
- PCI Express Development Kit, Stratix II GX Edition:
  **www.altera.com/products/devkits/altera/kit-pciexpress_s2gx.html**
- Audio Video Development Kit, Stratix II GX Edition:
  **www.altera.com/products/devkits/altera/kit-dsp-professional.html**

## Calculate the Target Impedance for Each Voltage Rail

Refer to the Stratix II GX Transceiver User Guide section of the *Stratix II GX Handbook* for further information about transceivers modes and features.

- ❒ Determine the settings for each transceiver quad (number of channels, data rate, mode, pre-emphasis settings, $V_{OD}$). Choose the maximum expected values for conservative estimations.
- ❒ Use the PowerPlay EPE spreadsheet and enter the transceiver settings in the XCVR tab.
- ❒ Design separate power supply rails and decoupling networks for the power supplies of the following groups. Power supply voltage may vary and further separation of power supplies may be needed depending on the requirements of the application.
  - $V_{CCT}$, $V_{CCL}$, and $V_{CCR}$ (1.2V analog transceiver power supply)
  - $V_{CCH}$ (1.2/1.5V transceiver buffer)
  - $V_{CCA}$ (3.3V analog transceiver power supply)
  - $V_{CCP}$ (1.2V digital transceiver power supply)
  - $V_{CCINT}$ (1.2V core power supply)
  - $V_{CCPD}$ (3.3V I/O pre-driver supply)
  - $V_{CCIO}$ (1.2V, 1.5V, 1.8V, 2.5V, 3.3V I/O power supply)

Refer to *High-Speed Board Design Advisor: Pinout Definition* for a detailed pin description: **www.altera.com/literature/tb/tb-094.pdf**.

- Use a contiguous ground (VSS) plane without splits for all transceiver functions.
- Derive maximum current (A) values from the PowerPlay EPE Spreadsheet and enter the values in Table 1.

Refer to the EPE User Guide and the *Quartus II Handbook*, Volume 3, Section III for a detailed description of the tools used with Quartus II development software.

- Calculate the maximum transient currents. A best practice guideline is to use 50 percent of the maximum current as estimation for the transient current. The maximum transient current is calculated from maximum current used minus minimum current used for a given design or by measurement or simulations. Since none of these methods are routinely available, Altera recommends the 50 percent rule for the PDN design.
- Specify the maximum tolerable ripple. A good design practice is to allow ±2 percent or less ripple for all analog transceiver supplies $V_{CCT}$, $V_{CCL}$, $V_{CCR}$, $V_{CCA}$, $V_{CCH}$ and $V_{CCP}$, ±5 percent total power supply tolerance for $V_{CCIO}$ and $V_{CCPD}$, and ±50mV for $V_{CCINT}$.
- Use Table 1 to calculate the target impedance for a PDN using the equation $Z_{Target} = \frac{VoltageRail \times \%Ripple}{MaxTransientCurrent}$.
- Enter target impedance values into Decoupling Design Tool.

*Table 1. Calculation of the Target Impedance*

| Voltage Rail | Voltage (V) | % Ripple | Max Current (A) | Maximum Transient Current (A) | Target Impedance $Z_{Target}$ |
|---|---|---|---|---|---|
| $V_{CCT}$ | 1.2V | 2% | | | |
| $V_{CCL}$ | 1.2V | 2% | | | |
| $V_{CCR}$ | 1.2V | 2% | | | |
| $V_{CCH}$ | 1.2/1.5V | 2% | | | |
| $V_{CCA}$ | 3.3V | 2% | | | |
| $V_{CCP}$ | 1.2V | 2% | | | |
| $V_{CCINT}$ | 1.2V | ±50mV | | | |
| $V_{CCPD}$ | 3.3V | 5% | | | |
| $V_{CCIO}$ | 1.5V<br>1.8V<br>2.5V<br>3.3V | 5% | | | |

- The Decoupling Design Tool requires choosing three capacitor values per decade (n). The first tab in the spreadsheet contains the capacitor library. Enter the capacitor values, ESL, and ESR for all capacitors used.

## Select the Voltage Regulator Module and Determine the Decoupling Capacitance Values at the Lowest Frequency

- Set the Voltage Regulator Modules (VRM) as either switching regulators or linear regulators.

For VRM design examples, refer to the Stratix II GX development kit documentation.
The following voltage regulator vendors provide recommendations about Altera device power supply options:
**www.altera.com/support/devices/vendors/pow-vendors.html**.

- Obtain the ESR and ESL values from the VRM vendor. Alternatively, take measurements using a low frequency network analyzer or get the impedance profile from the VRM vendor and extract ESR and ESL values.
- Enter the ESR and ESL values in the Decoupling Design Tool.

- Determine the effective frequency range of the VRM (target frequency = VRM impedance, typical ~10 kHz). Above this minimum frequency the board-level PDN must be designed to keep the impedance below the target impedance.
- Choose enough low C for low frequency decoupling (bulk capacitors).
- Use the Decoupling Design Tool to adjust the composite frequency response to stay below the target impedance in the low-frequency range by changing the lower frequency decoupling capacitance value or number of capacitors for each voltage rail.
- Allow a comfortable margin, but take into account the trade-off between performance and cost.

## Determine Decoupling Capacitance Values at the Highest Frequency

- The highest frequency of interest determines the maximum frequency at which the board decoupling can be effective. Beyond this frequency, the FPGA device and package impedance dominates the PDN. For Stratix II GX FPGAs, use 50 MHz for $V_{CCINT}$ and 200 MHz for all other power rails. Those values are preconfigured in the Decoupling Design Tool for each voltage rail.
- The PCB power and ground planes are used for high-frequency decoupling. Model the impedance of the planes as an ideal transmission line using the formulas in the Decoupling Design Tool User Guide, Section 3.2.3, and calculate the equivalent ESR and ESL values.
- Enter the results in the Decoupling Design Tool for each voltage rail. The capacitance is insignificant compared to the capacitance of the chip and can be neglected.
- Ideally, the lowest impedance frequency of the planes matches the range of the highest frequency of interest.

## Select the Decoupling Capacitor Network for Each Power Rail

- In the mid- to high-frequency range, a single capacitor cannot provide a low enough ESL to meet the target impedance. Therefore, use multiple capacitors in parallel.
- Get the ESR and ESL value from the capacitor vendor. ESL from the vendor does not reflect the total mounted inductance ($ESL_{Total}$) since this is dependant on how and where the capacitor is mounted on the planes.
- Get the lowest, practical total mounted inductance of the capacitors by using the following guidelines:
  - Use short, wide capacitors, such as 0402, 0508, IDC, or X2Y
  - Use short surface traces to connect capacitor pads to the vias connected to the planes below (minimum size solder dams, vias as close to device as possible)
  - Use wide surface traces
  - Use multiple via pairs
  - Place capacitors on the back side of the package within the power and ground ring (eliminates spreading inductance)
  - Place power and ground planes close to the surface where the capacitors are attached
  - Use a thin dielectric between power and ground planes
  - Use multiple power and ground plane pairs
  - Don't use a surface trace to route to a package pad (cost is ~13 pH/mil)
  - Don't share vias of adjacent capacitors
  - Use large diameter vias
  - Place capacitors close to package
  - Bring opposite current vias close together
  - Place same current vias far apart
  - Place capacitor in the middle of the board rather than at edges and corners
  - Use $V_{CC}$ planes for high frequency and transient currents at the surface of the FPGA side of the PCB stackup

- Estimate or calculate the total ESL ($ESL_{Total}$ = intrinsic ESL + mounting inductance) of the decoupling capacitors using the formulas in the Decoupling Design Tool User Guide, Section 2.2.2. Alternatively, use the default ESR, ESL, and mounting inductance values in the Decoupling Design Tool for 0402 or 0603 capacitor footprints.
- Enter the values in the Decoupling Design Tool spreadsheet. The capacitor values selected in the tool use three different capacitance values per decade.

- Adjust the composite frequency response to stay below the target impedance in the target frequency range with the least amount of capacitors, while continuously evaluating the trade-off between extra margin and cost. An example result is shown in Figure 2.

## Effective Decoupling Radius

- The effectiveness of the decoupling capacitor is directly proportional to its distance to the associated load. Decoupling capacitors are most effective when they are located at the point of load or using the "wavelength over 40" rule: $D_{EFF}$ = effective distance = 1/10 of 1/4 wavelength at the resonant frequency of the decoupling capacitor

  $$D_{EFF} = \frac{\lambda}{40} \text{ with } \lambda = \frac{1}{velocity \times f_R}, f_R = \frac{1}{2\pi\sqrt{ESL_{Total} \times C}}$$

- Use the following equation to calculate the effective decoupling radius/distance:

  $$D_{EFF} = \frac{2\pi\sqrt{ESL_{Total} \times C}}{velocity \times 40}$$, velocity = 180 ps/in (e.g., for FR-4)

- Examples using $ESL_{Total}$ = 1.9 nH = 0.4 nH (ESL) + 1.5 nH (mounting inductance), are shown in Table 2.

*Table 2. $ESL_{Total}$ Examples*

| Cap Value (uF) | 1.0 uF | 0.1 uF | 0.01 uF | 0.001 uF |
|---|---|---|---|---|
| Effective Decoupling Radius (in) | 38.04 | 12.03 | 3.80 | 1.20 |

- Highest frequency response capacitors would ideally be mounted close to the power supply pins.
- Use low mounting inductance placement guidelines for low $ESL_{Total}$.

## Optimize the Board Stackup for Low Impedance Power and Ground Planes Under Consideration of Manufacturability and Cost

- Choose the thinnest possible dielectric between power and ground planes.
- Place power and ground planes as close to the surfaces as possible.
- Use as many power and ground plane pairs as practical:
  - One plane—place close to the surface with capacitors and package on the same side
  - Two planes—place close to the top and bottom surface
  - Three planes—place one close to top surface, one close to bottom surface, and one in the middle
  - Use the highest dissipation factor laminate as possible
- Validate the PDN performance with measurements or simulations from DC to the highest frequency of interest.

The following figures are screen shots taken from the Decoupling Design Tool. Figure 1 illustrates the use of the capacitor spreadsheets. Figure 2 shows the adjustment of the composite frequency response in order to match the target frequency.

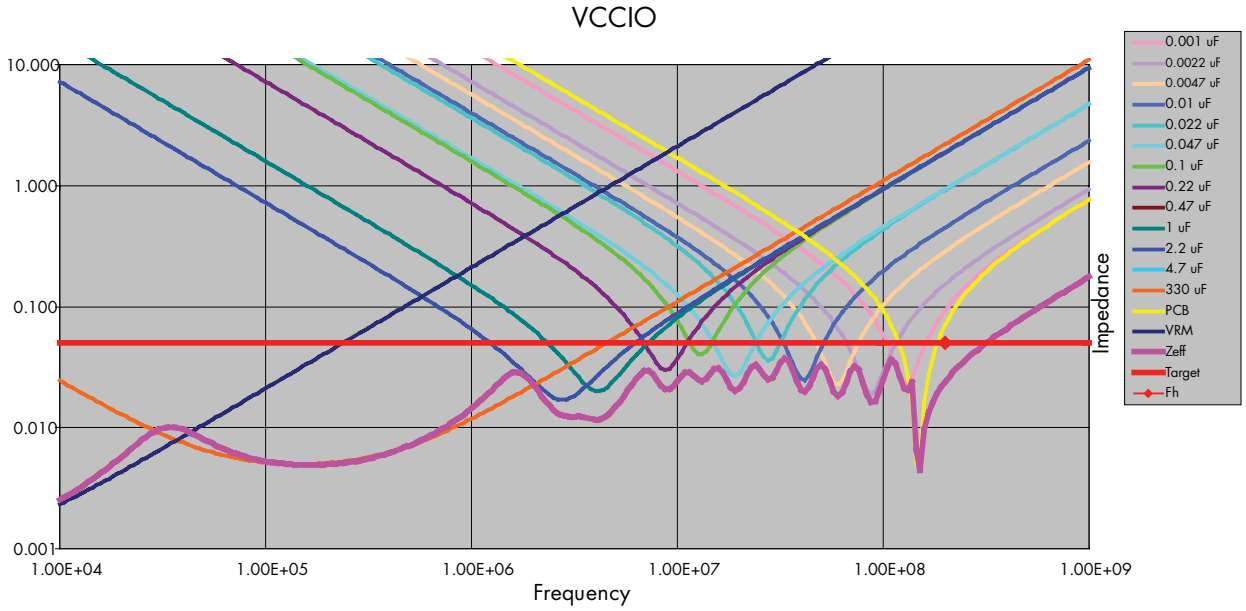
*Figure 1. Capacitor Spreadsheet*

| Cap Value | Units | Footprint | Number of Caps | ESR (ohm) | ESL (nH) | Mounting Inductance (nH) | Total Inductance (nH) |
|---|---|---|---|---|---|---|---|
| 0.001 | uF | 0603 | 12 | 0.272 | 0.5 | 1 | 1.5 |
| 0.0022 | uF | 0603 | 10 | 0.189 | 0.5 | 1 | 1.5 |
| 0.0047 | uF | 0603 | 6 | 0.135 | 0.5 | 1 | 1.5 |
| 0.01 | uF | 0603 | 4 | 0.098 | 0.5 | 1 | 1.5 |
| 0.022 | uF | 0603 | 2 | 0.072 | 0.5 | 1 | 1.5 |
| 0.047 | uF | 0603 | 2 | 0.053 | 0.5 | 1 | 1.5 |
| 0.1 | uF | 0603 | 1 | 0.04 | 0.5 | 1 | 1.5 |
| 0.22 | uF | 0603 | 1 | 0.03 | 0.5 | 1 | 1.5 |
| 0.47 | uF | 0603 | 0 | 0.023 | 0.5 | 1 | 1.5 |
| 1 | uF | 0603 | 1 | 0.02 | 0.5 | 1 | 1.5 |
| 2.2 | uF | 0603 | 1 | 0.017 | 0.5 | 1 | 1.5 |
| 4.7 | uF | 0603 | 0 | 0.015 | 0.5 | 1 | 1.5 |
| 330 | uF | 0603 | 2 | 0.01 | 3 | 0.5 | 3.5 |
| 0.0093 | uF | PCB | 1 | 0 | 0.1248 | 0 | 0.1248 |
| 0 | uF | VRM | 1 | 0.001 | 33.6 | 0 | 33.6 |

| Target Impedance (ohm) | 0.05 |
|---|---|

| High Frequency Target (Fh) (MHz) | 200 |
|---|---|

*Figure 2. Composite Frequency Response Adjustment*




## Further Information

- "Frequency Domain Target Impedance Method for Bypass Capacitor Selection for Power Distribution Systems", Larry D. Smith of Altera Corporation, DesignCon 2006.
- Dr. Eric Bogatin's online lecture, "*OLL-803 - Best Board Design Practices for Power Distribution Network*": **www.bethesignal.com**.
- "Power Distribution system Design Methodology and Capacitor selection for Modern CMOS Technology", Manuscript of paper published in IEEE Transaction on Advanced Packaging, August, 1999, pp284-291 by Larry Smith, Raymond Anderson, Doug Forehand, Tom Pelc, and Tanmoy Roy, all of Sun Microsystems Inc.

- "Power Plane SPICE Models and Simulated Performance for Materials and Geometries", Manuscript of paper published in IEEE Transactions on Advanced Packaging, August 2001 edition by Larry Smith, Raymond Anderson, and Tanmoy Roy.
- "Distributed SPICE Circuit Model for Ceramic Capacitors", Presented at IEEE ECTC Conference, Lake Buena Vista, Florida May 29-June 1, 2001 by Larry Smith and David Hockanson of Sun Microsystems.
- "A Transmission-Line Model for Ceramic Capacitors for CAD Tools Based on Measured Parameters", Published in the Conference Record, Electrical Components Technology Conference (ECTC) May 2002, San Diego, CA by Larry D. Smith, David Hockanson, Krina Kothari, all of Sun Microsystems Inc.
- "Model to Hardware Correlation for Power Distribution Induced I/O Noise in a Functioning Computer System", Published in the Conference Record of ECTC 2002 at San Diego, Calif. by Sungjun Chun (GaTech), Larry Smith, Ray Anderson (both of Sun Microsystems), and Madhavan Swaminathan (GaTech).
- "ESR and ESL of Ceramic Capacitors Applied to Decoupling Applications", presented at the IEEE Electrical Performance of Electronic Packaging Conference (EPEP) Oct. 1998 by Larry Smith of Sun Microsystems and John Prymak of Kemet Electronic Corporation.
- "Chip-Package Resonance in Core Power Supply Structures for a High Power Microprocessor", Published in the Proceedings of IPACK'01, the Pacific Rim/ASME International Electronics Packaging Technical Conference and Exhibition, July 8-13, 2001, Kauai, Hawaii USA by Larry Smith, Raymond Anderson, Tanmoy Roy, all of Sun Microsystems.
- "Simultaneous Switch Noise and Power Plane Bounce for CMOS Technology", presented at the IEEE electrical Performance of Electrical Packaging (EPEP) Conference, San Diego, CA October 17-25, 1999 by Larry Smith of Sun Microsystems.
- "Power Plane Spice Models for Frequency and Time Domains", presented at the IEEE Performance of Electrical Packaging (EPEP) Conference 2000 (EPEP 2000), October 2000 at Scottsdale, Arizona by Larry Smith, Raymond Anderson, and Tanmoy Roy, all of Sun Microsystems.
- "Power Distribution System for JEDEC DDR2 Memory DIMM", published in Conference Record, IEEE Electrical Performance of Electronic Packages 2003 (EPEP 2003), Princeton, NJ, pp. 121-124 October 2003 by Larry D. Smith and Jeffrey Lee of Sun Microsystems Inc.
- *High-Speed Board Design Advisor: Thermal Management*: **www.altera.com/literature/tb/tb-093.pdf**
- *High-Speed Board Design Advisor: Pinout Definition*: **www.altera.com/literature/tb/tb-094.pdf**
- *High-Speed Board Design Advisor: High-Speed Channel Design and Layout*: **www.altera.com/literature/tb/tb-095.pdf**
- *High-Speed Board Design Advisor: Hardware Integration, Test, and Debug*: **www.altera.com/literature/tb/tb-096.pdf**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